



RV College of Engineering®

Mysore Road, RV Vidyaniketan Post,
Bengaluru - 560059, Karnataka, India

NBA Accredited (UG - 6 Years)

Department of Electronics & Communication Engineering

Date: 12/12/2024

Semester: I

Test - 2

UG

Max. Marks: 50

Duration: 1 ½ Hrs

Course: Principles of Electronics Engineering

Code: EC113ATC

S No	Questions	M	BT	C O
1. a	Draw the circuit of an RC phase shift oscillator using a transistor in the common emitter configuration as an amplifier, and explain its operation. Determine the 'C', if frequency of oscillation $f=100\text{Hz}$, $R=3.3\text{K}\Omega$ and the collector resistance, $R_C=5\text{K}\Omega$.	06	3	1
b	State and illustrate Barkhausen's criterion for sustained oscillations.	04	1	2
2. a	Draw a circuit and calculate the values of different resistors of a summer circuit using two ideal op-amp to get $v_o = v_1 + 3v_2 + 5v_3 - 7v_4 - 9v_5 - 11v_6$, where v_1, v_2, v_3, v_4, v_5 and v_6 are the available inputs.	06	2	1
b	Draw the circuit diagram for integrator using an op-amp, Derive the expression for output voltage.	04	3	2
3. a	List at least eight important characteristics of ideal op-amp and indicate their typical practical values. Write the Pin configuration of op amp(741).	06	3	2
b	A logic circuit has two inputs P and Q and an output Y. The output is False when either of the two inputs are False but not both. Write the logic expression and realize using NAND gates only.	04	2	1
4. a	Write the truth table for SUM and CARRYOUT of a full adder. From the truth table, obtain the logic expressions for the same and then realize the full adder using 2 half adders.	06	3	1
b	Perform Subtraction using 1's complement and 2's complement $(11010)_2 - (10000)_2$	04	2	2
5. a	Convert the following: i. 3456 ₁₀ to the binary system ii. 3A4 ₁₆ to the decimal number. iii. 1011 ₂ to octal number system. iv. 542 ₈ to the hexadecimal number system	06	3	3
b	Simplify the logic expression using K-map: $Y(W,X,Y,Z) = \Sigma m(1,2,3,5,7,11,13)$	04	3	3

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars		CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	Max Marks	16	18	10	-	4	14	28	-	-	-



Department of Electronics & Communication Engineering

Date: 5/11/2024	Test - 1	Max. Marks: 50
Semester: I	UG	Duration: 1 $\frac{1}{2}$ Hrs
Course: Principles of Electronics Engineering		Code: EC113AT

QNo.	Questions	M	BT	CO
1a.	With necessary circuit and waveform, explain the working of a bridge rectifier with capacitive filter.	6M	L1	CO2
b.	A DC power supply drops from 18V to 17.95V when the AC source voltage falls by 10%. The output also falls from 18V to 17.9V when the load is increased from 0 to maximum. Calculate load and line Regulation	4M	L1	CO1
2a.	Design a Zener regulator and draw the circuit for given specifications: V_{in} varies from 22 V to 28 V, R_L varies from 50 Ω to 500 Ω , $V_Z = 12$ V, $I_{Z(min)} = 10$ mA, and $P_{d(max)} = 6$ W.	6M	L3	CO2
b.	Distinguish between Avalanche breakdown and Zener breakdown in diodes.	4M	L1	CO1
3a.	An amplifier has a gain of 40dB, bandwidth of 300KHz, distortion of 15%, input impedance of 10K Ω and Output impedance of 10K Ω . If Voltage series negative feedback of 3.9% is given to this amplifier, calculate the Gain, Z_{in} , Z_o , BW and distortion of the amplifier with negative feedback.	6M	L2	CO3
b.	Draw the frequency response of an RC coupled amplifier and the effect of capacitors.	4M	L1	CO2
4a.	A full wave bridge rectifier drives a load resistance of 150 Ω in parallel with a filter capacitor, C. If the ac input to the rectifier is $50\sin 628t$, calculate the capacitor value needed so that the ripple factor is 1.5 %. Also determine the output DC voltage, peak to peak ripple voltage and the load regulation.	6M	L3	CO3
b.	Draw the DC power supply block diagram and explain each components.	4M	L2	CO2
5a.	With respect to common emitter configuration, explain three regions of operations of a bipolar junction transistor. Draw input and output characteristics for the same.	6M	L2	CO2
b.	Three amplifiers stages are working in cascade with 0.04V peak to peak input, providing 160V peak to peak output. If the voltage gain of the first stage is 15 and the input to the third stage is 10V peak to peak, Find i. Overall voltage gain ii. Voltage gain of the second and third stages iii. Input voltage to the second stage	4M	L1	CO2

BT-Blooms Taxonomy, CO-Course Outcomes, M-Marks

Marks Distribution	Particulars	CO1	CO2	CO3	CO4	L1	L2	L3	L4	L5	L6
	Test	8	30	12		22	16	12	-	-	-
	Max Marks										