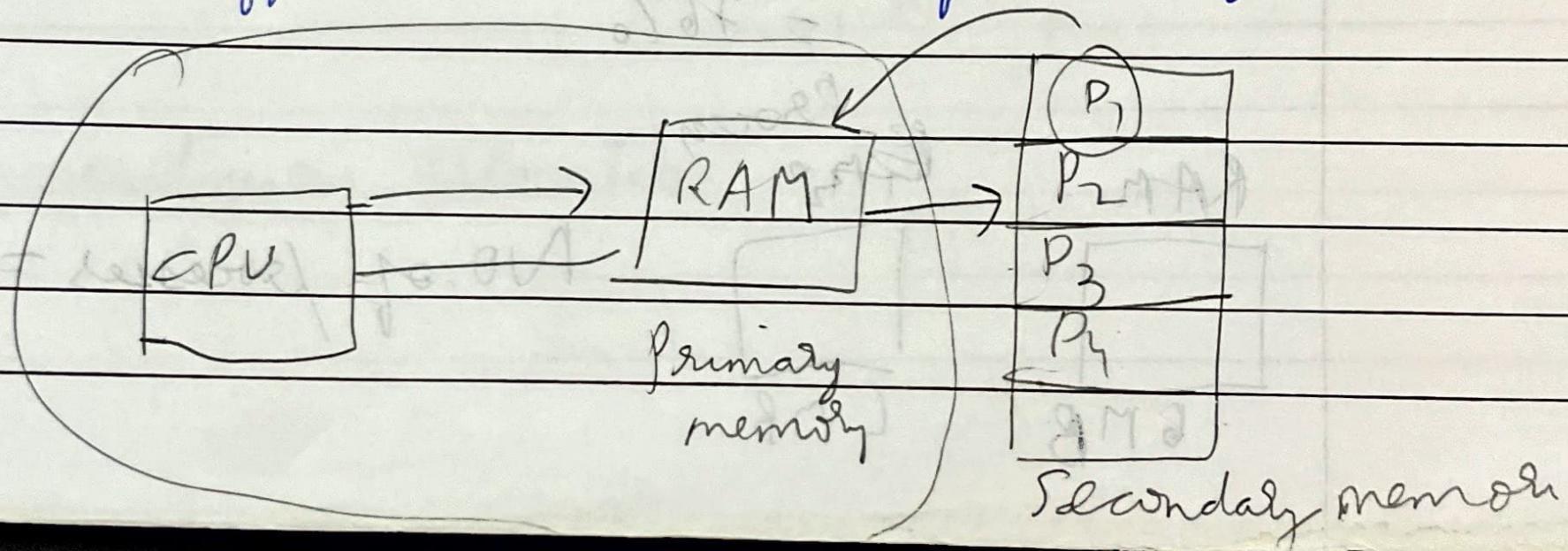


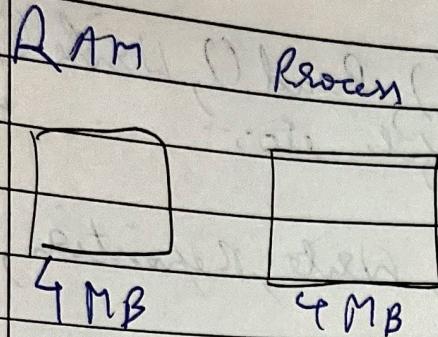
## L-5.1 Memory management and degree of multiprogramming

Memory management → method of managing primary memory

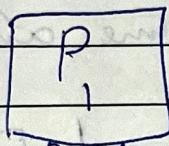
Goal: Efficient Utilisation of memory



Process  
CPU S/I



$$\frac{4 \text{ MB}}{9 \text{ MB}} = 1$$

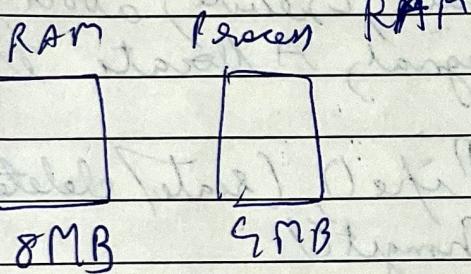


Probability of

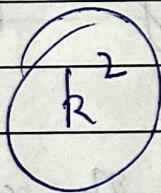
$k' = I/O \text{ operation} (70\%)$

$$CPU = (1 - k) = 30\%$$

CPU Utilisation



$$\text{No. of Processes} = \frac{8 \text{ MB}}{4 \text{ MB}} = 2$$

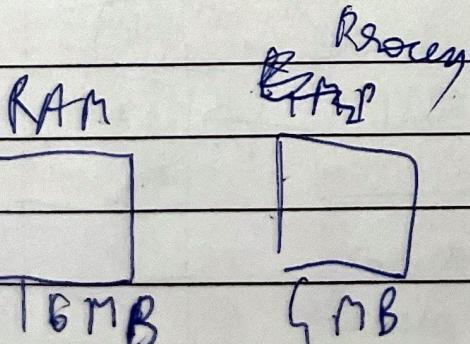


$$CPU \text{ utilisation} = (1 - k)$$

$$k = 70\%$$

$$CPU = 1 - (0.7)^2$$

$$= 26\%$$



$$\text{No. of processes} = 4$$

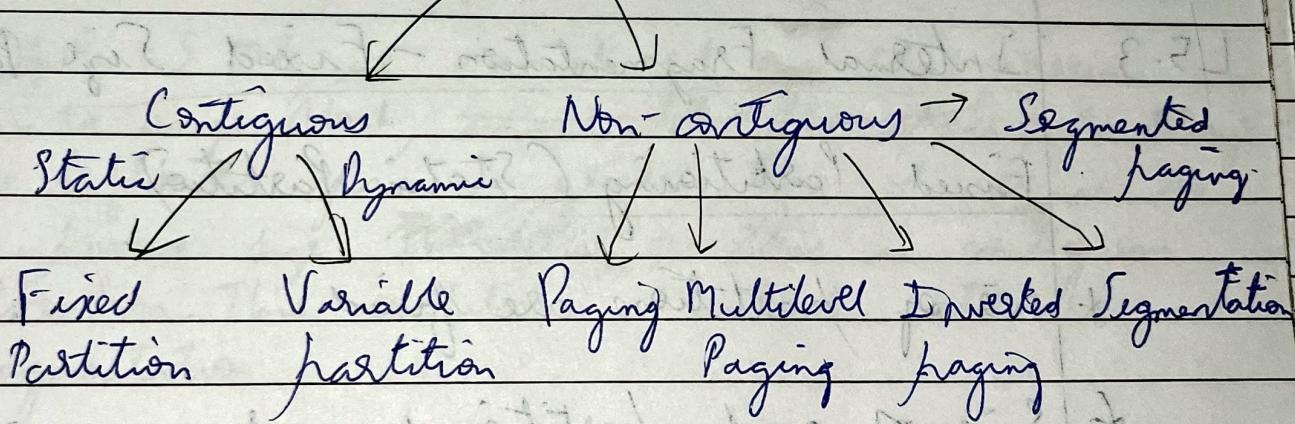
R<sup>4</sup>

$$\text{CPU utilization} = 1 - R^4 = 93\%$$

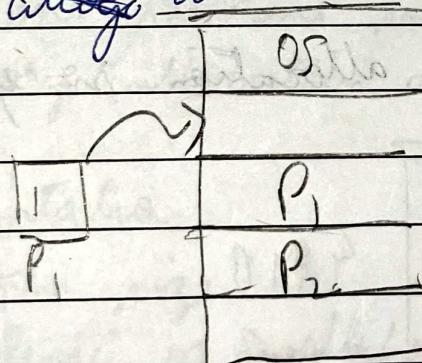
Observation:- The size of the ram is directly related to the CPU utilization.

Ques:- Memory management techniques - Contiguous and non-contiguous

### Memory management techniques

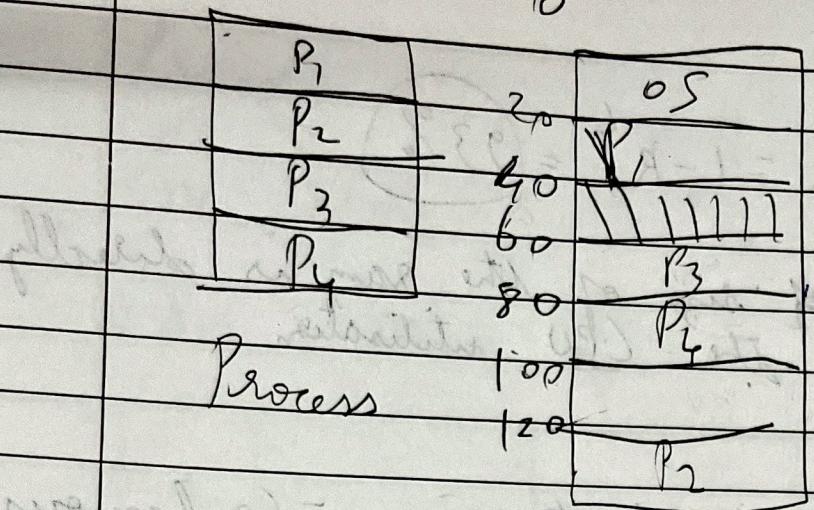


### Contiguous memory allocation



Memory blocks  
(RAM)

### Non-contiguous allocation



Memory

Blocks

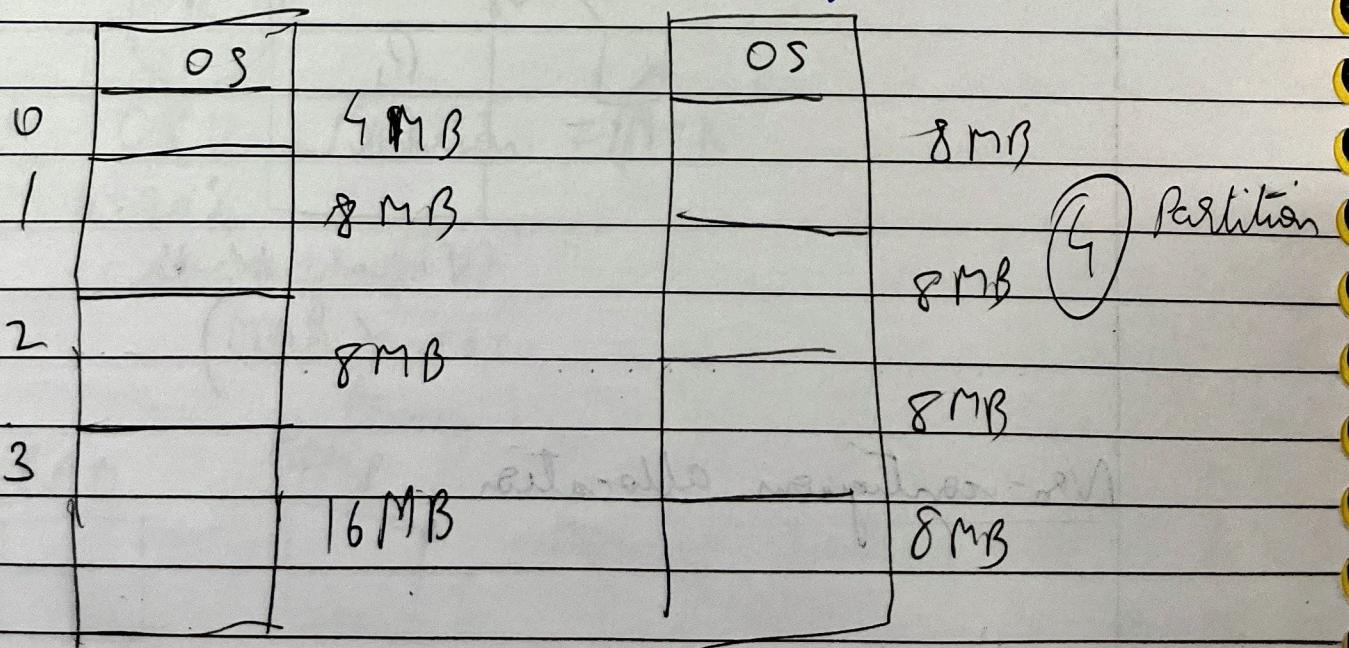
RAM

L5-3

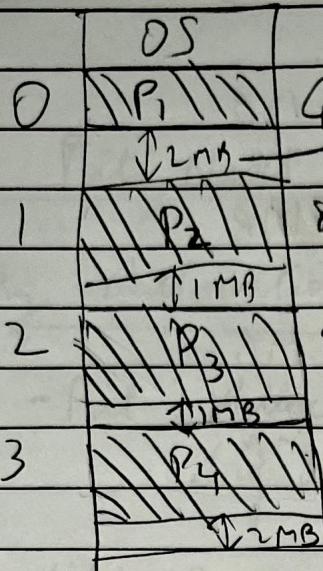
Internal Fragmentation - Fixed Size Partitioning

Fixed Partitioning (Static Partition)

- \* No. of partitions are fixed
- \* Size of each partition may or may not be same
- \* Contiguous allocation so spanning is not allowed



If there are 2 MB process,



4 MB

OS

↓ 2 MB

4 MB

↓ 2 MB

8 MB

↓ 1 MB

8 MB

↓ 1 MB

8 MB

↓ 2 MB

6 MB

↓ 2 MB

3

2

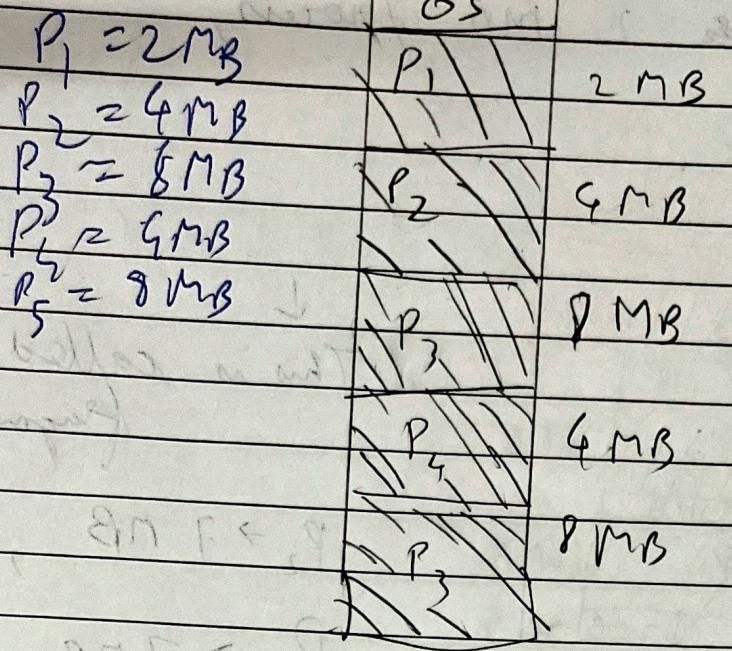
1

0

16 MB

↓ 2 MB

</div



### Advantages

- 1) No internal fragmentation
- 2) No limitation on no. of processes
- 3) No limitation on process size

Disadvantage: If  $P_2$  &  $P_5$  processes are removed, there are collectively 3 MB space left. If we want to add another process of 6 MB, we cannot add as this is contiguous allocation. This leads to external fragmentation.

- 1) This problem can be solved through compaction, where the processes  $P_1, P_3, P_5$  can be put in contiguous spaces through copy-paste. But, for this, we have to kill the processes.
- 2) When holes are created, (hole means empty spaces between 2 already occupied process memories),

it is difficult to allocate/deallocate in those holes.

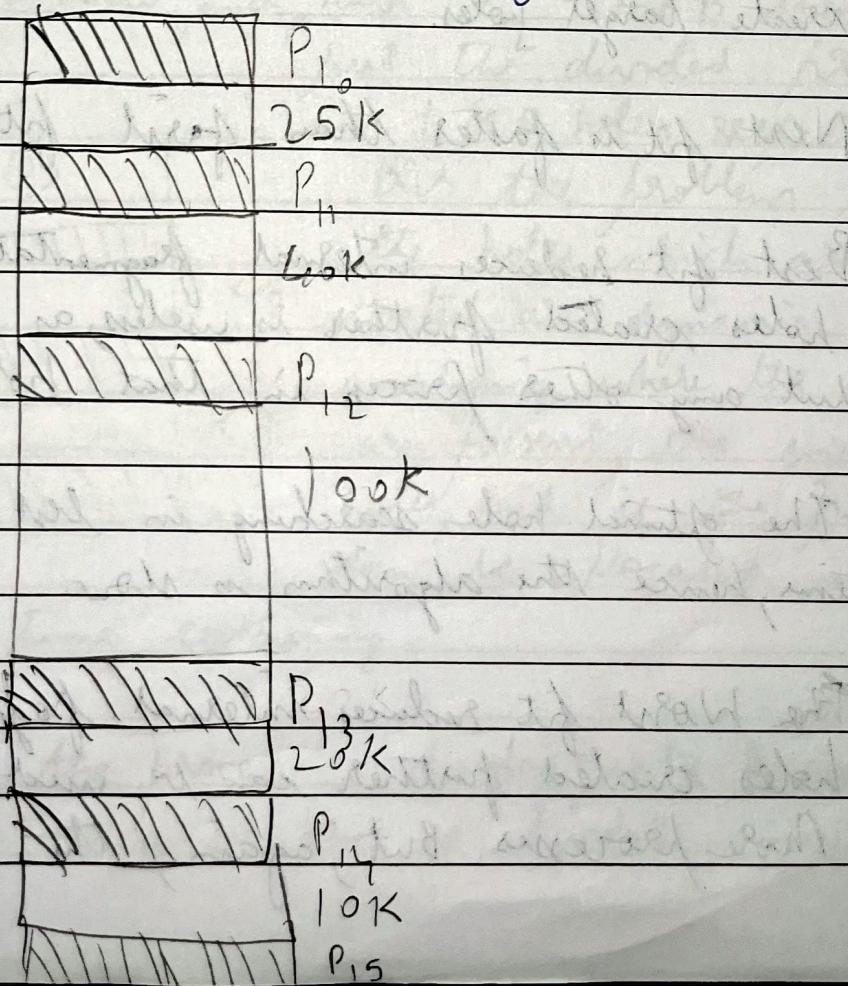
## L5-5 First Fit, Next Fit, Best Fit, Worst Fit & Memory Allocation

First - Fit : Allocate the first hole that is big enough

Next - fit : Same as first fit start search always from last allocated file

Best - fit : Allocate the smallest hole that is big enough

Worst fit) Allocate the largest hole



Suppose  $P_1 = 15K$

Through first fit, the  $P_1$  process will be fit into 25K hole

Next, we have  $P_2 = 18K$ . We are using next fit.  
P<sub>1</sub> : Here, we know that P<sub>1</sub> was last allocated.  
Therefore, we start searching from P<sub>1</sub> process,  
and we fit P<sub>2</sub> into 40K hole.

If we start allocating P<sub>1</sub> = 15K by removing P<sub>2</sub>,  
then by best fit, P<sub>1</sub> will be allocated in  
20K hole, as the difference is very small.

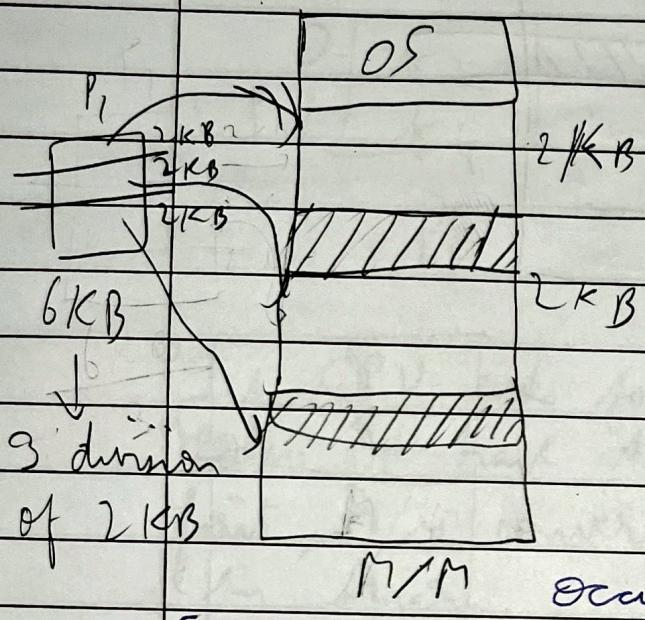
Through worst case, P<sub>1</sub> will be allocated into  
100K hole, because it has the largest space.

- \* First fit is simple and fast, but it can create larger holes.
- \* Next fit is faster than first fit.
- \* Best fit reduces internal fragmentation, but the holes created further is useless, as we cannot put any other process in that hole.
- \* The optimal hole searching in best fit will take time, hence the algorithm is slow.
- \* The Worst fit reduces internal fragmentation, and holes created further can be used to allocate more processes. But, again, the algorithm is slow.

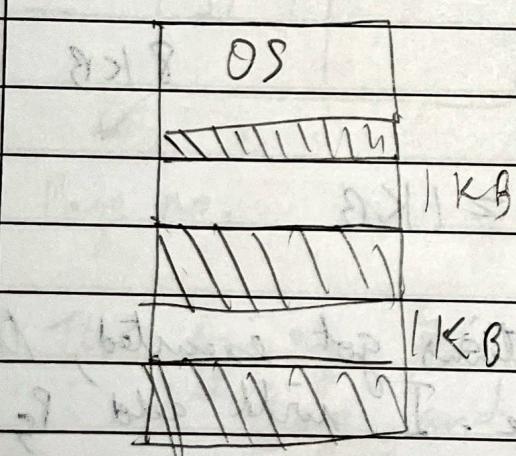
In real life, first fit is the ~~most~~ most convenient method as it takes less time.

## L-5-8 Need of Paging

Non-contiguous memory allocation



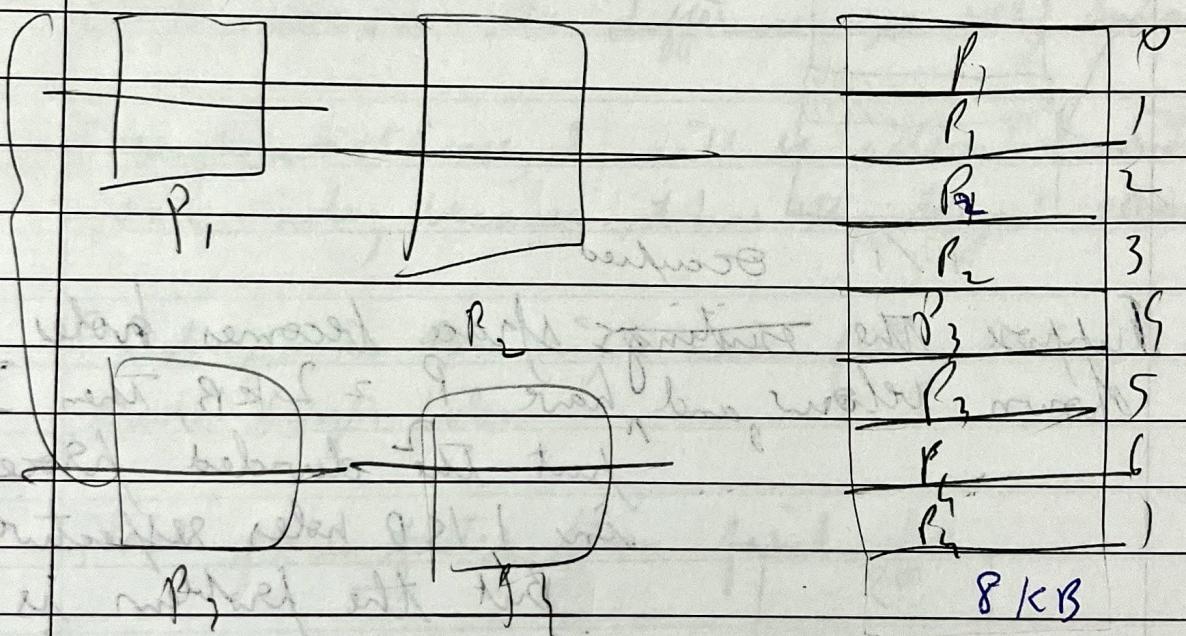
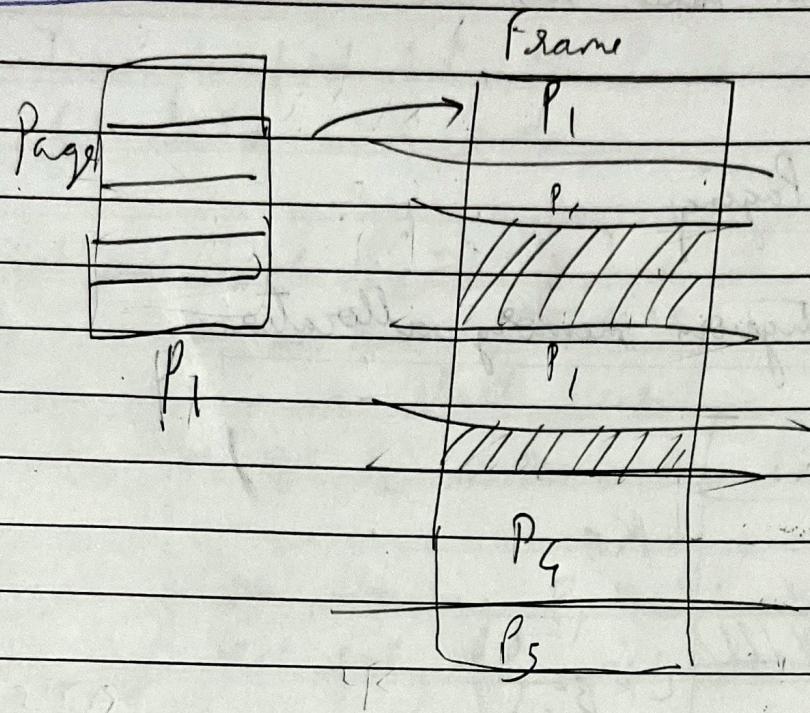
Suppose the existing space becomes holes as shown below, and have  $P = 2\text{KB}$ , then I can put the divided process in  $1\text{KB}$  holes respectively.



But the problem is that the holes which are created are dynamic, and analysing where the holes are present, the size of holes, and if the process can be allocated in these holes is time consuming.

Therefore, the process is divided into ~~the~~ pages and the main memory is divided into frames.

Page size = Frame size



Page size = Frame size = 1 KB

Now if  $P_2$  &  $P_3$  instructions got executed, there will be 4 KB space - I will add  $P_5 \approx 5$  KB early to the main memory

L-5-9

What is paging?

Page no

Byes

— / — / —

0	0	7	4	1	0	6	1	8	1
					1		2	1	3
1	2	3			2	4	5		

~~0 6 18  
11 13~~

2 | 4 5

3. ~~6~~ 7  
6. ~~8~~ 9

$\frac{1}{2} \times 10 = 5$

~~6~~ 13

## Page table of P

~~6~~ 13

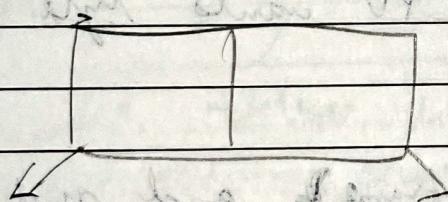
~~7 11 15~~

0	<u>b<sub>2</sub></u>
1	<u>b<sub>6</sub></u>

P

If CPU asks for  $\overline{3}$  as a random bit (CPU doesn't have the idea of paging), say 3, first, 3 is converted to logical address in binary

## Structure of logical address (2 bits)



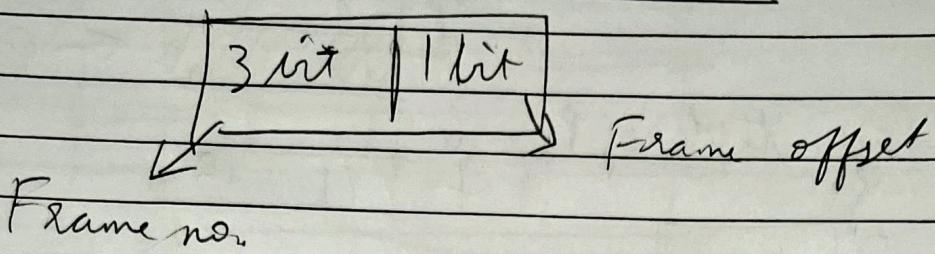
Page no. 10 Page offset

The binary form of 3 is 11  
∴ 1<sup>st</sup> page and 1's bit of the page is accessed. ∵ 3 is accessed.

Now, the same byte is stored at another location of the main memory, as another location representation. How to recognise that?

For this, the logical address is converted to physical address (4 bits), as there are 11 bits.

### Structure of physical address



Now, we have the logical address as 91, and we have got the frame number as 4. Converting this into binary gives the frame number  $\rightarrow 100$ . The frame offset and the page offset remains the same. The resultant physical address is  $1001 \rightarrow 9_{(10)}$ .

- \* The page table is stored and managed by memory management unit (MMU)

Another example:- CPU wants byte 1

Logical address :- 01

1 is present in frame 2, and offset is 1  
the physical address is 0101, which is 5.  
The bit representation byte is in position 5 in the main memory.

LRU  $\rightarrow$  Least recently used

L5-12 Page table entries | Enable/Disable

FRAME No.		Valid(0) Invalid(1)	Protection (R/W)	Reference (0/1)	Caching	Dirty

Mandatory Field

optional fields

R = Read  
W = Write  
X = Execute

Caching is done to store the data in the cache memory, if that particular data is called multiple number of times. Caching is mainly for static data, and not for dynamic data.

Dirty bit tells us whether the page is modified or not, 1 if modified, 0 if not.

L-5.13

## 2-Level Paging in OS

If the size of the page table is greater than the size of main memory, we have to divide the page table.

Eg:-

Physical Address Space = 256 MB  $\rightarrow 2^{28}$  B

Logical Address space = 4 GB  $\rightarrow 2^{32}$  B

Frame size = 4 KB

Page Table Entry = 2 B

LA $\rightarrow$	16	12
------------------	----	----

Total = 28

PA $\rightarrow$	20	12
------------------	----	----

Total = 32

Page Table  $\rightarrow$   ~~$2^8 \times 2^8 \times 2 = 2 \text{ MB}$~~

This is the inner page table

Now we have to divide the page table into divisions

$$\text{No. of divisions} = \frac{32}{4 \text{ KB}} = \frac{2^5}{2^{12}} = 2^9$$

Now, we create an outer page table

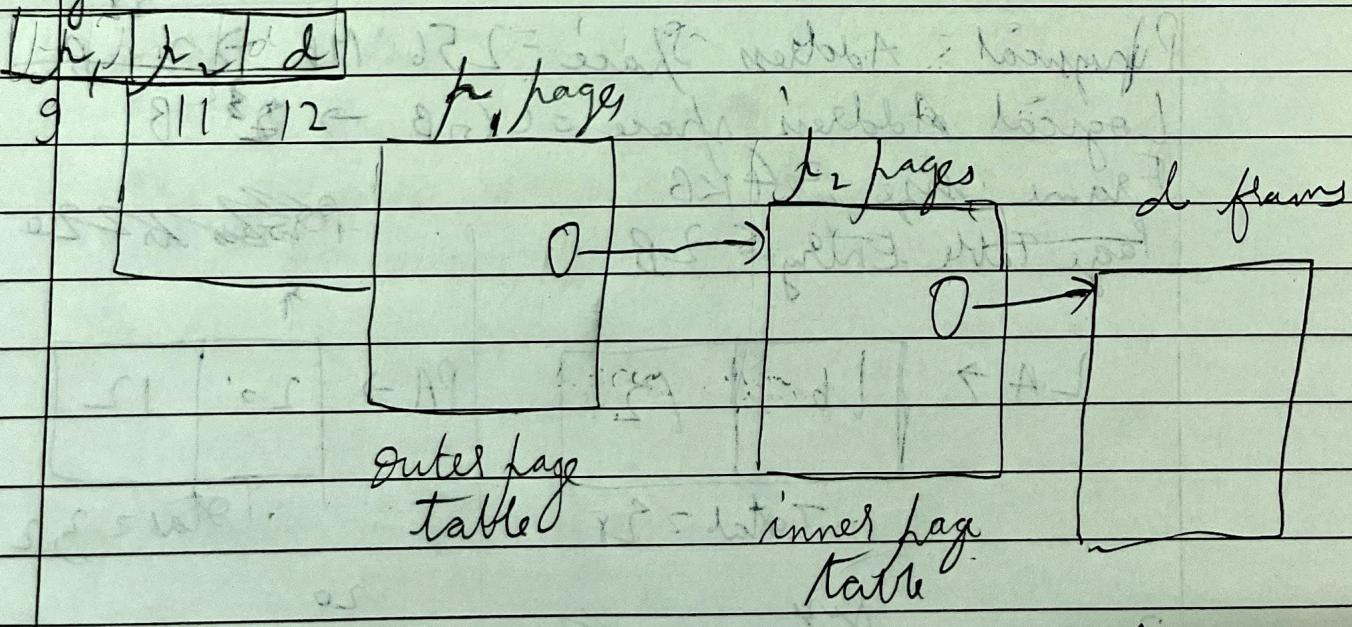
$2^9$	$2^8$	
$2^8$	$2^8$	
	$2^8$	
	$2^8$	

Outer Page Table

The total outer page Table size =  $2^9 \times 2^8 \times 1 \text{ KB}$

Now how do we  
Address translation scheme

Logical address



Main  
Memory

Segmentation VS Paging

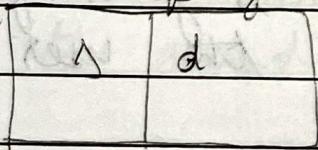
Segment		BA	SIZE	segment size	
main	add 0	3300	200		
S <sub>0</sub>	s <sub>1</sub>	1800	400	d ≤ size	1500 S <sub>5</sub>
S <sub>1</sub>	stack	2700	600	Yes	1800 S <sub>5</sub>
S <sub>2</sub>	s <sub>3</sub>	2300	400	-	2200 S <sub>3</sub>
S <sub>3</sub>	s <sub>4</sub>	2200	100	No	2300 S <sub>3</sub>
S <sub>4</sub>	s <sub>5</sub>	1500	300	Try	2100 S <sub>3</sub>
					3300 S <sub>2</sub>
					3500 S <sub>0</sub>

Segment Table

All are of various sizes, unlike pages 17/M

- \* Just like paging, logical address tells the CPU the location of the byte in the process, and physical address tells us the CPU the location of byte in the main memory.
- \* Memory Management Unit (MMU) is required to convert from logical address to physical address.

Logical address



Segment Segment

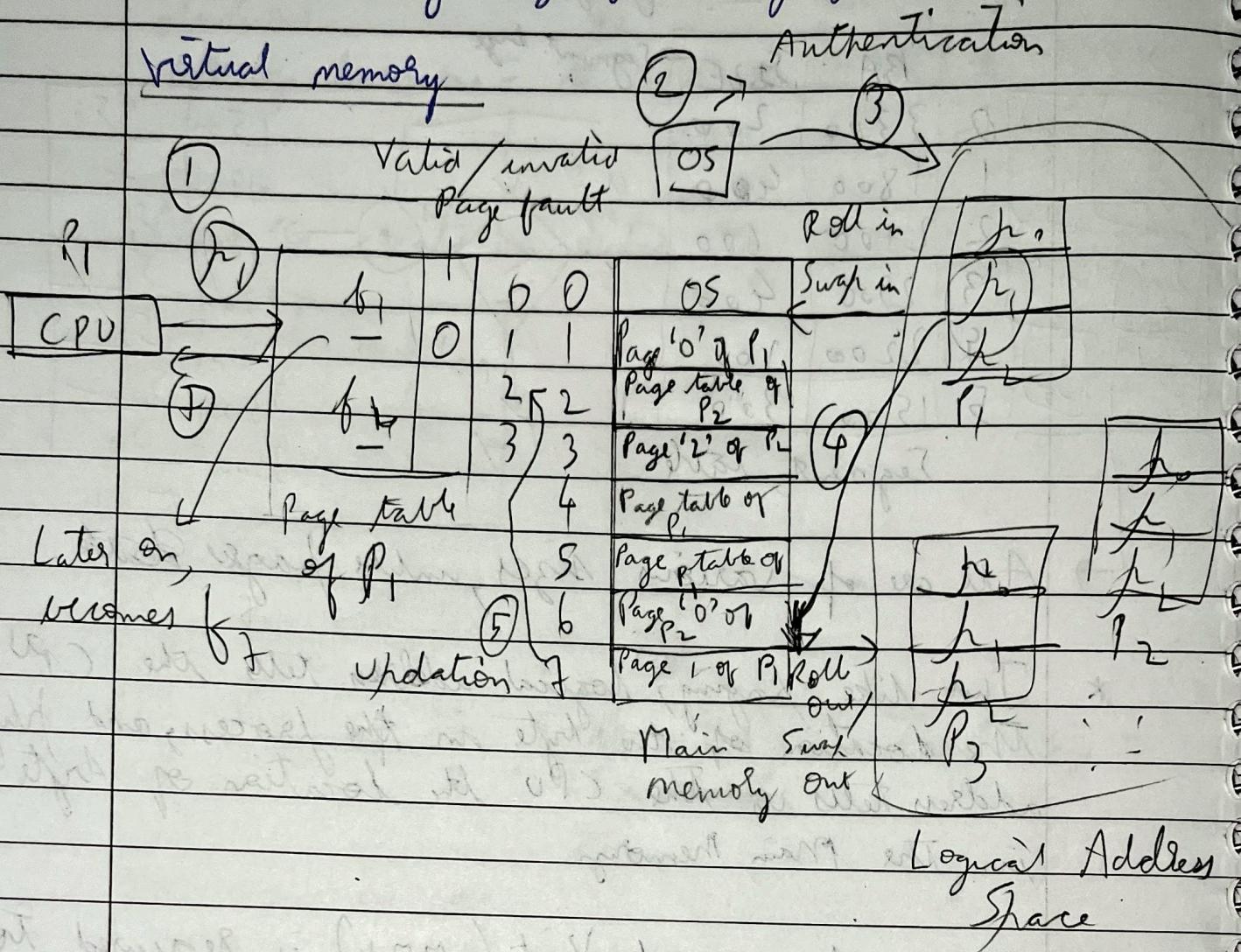
no size/offset

CPU has

~~a~~ is the no of bytes we have to read in that segment

L-5.19

## Virtual Memory - Page fault - Significance of virtual memory



If page fault is 0, trap is generated

Through this method, control is given from user to OS, and then to the user

$\rightarrow$  Probability of page fault.

Effective memory access time, EMAT =

$$h(\text{page fault. service time}) + (1-h)(\text{main memory access time})$$

(in ms) (in ns)

\* We are not considering the main memory access time during page fault service time.