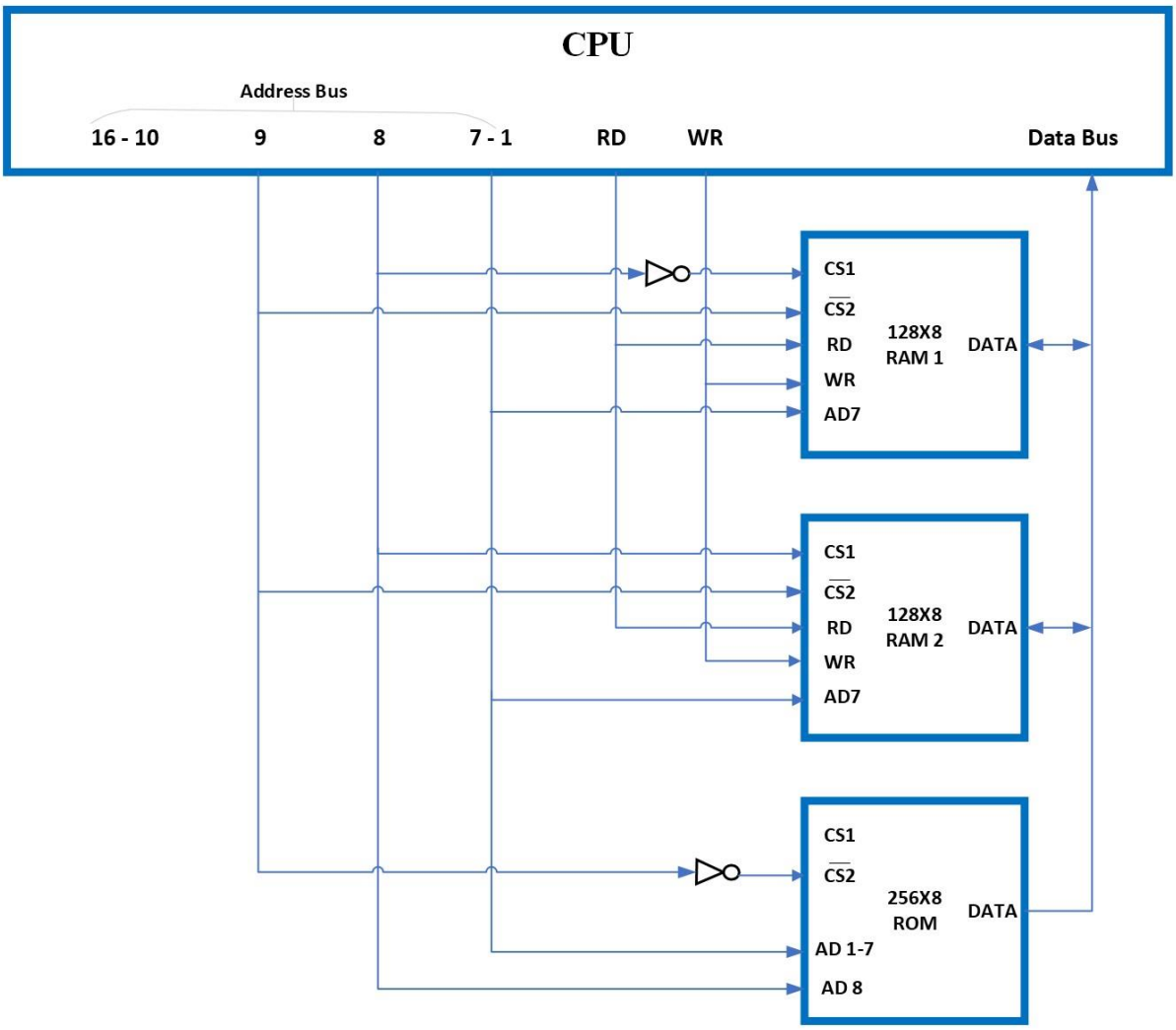
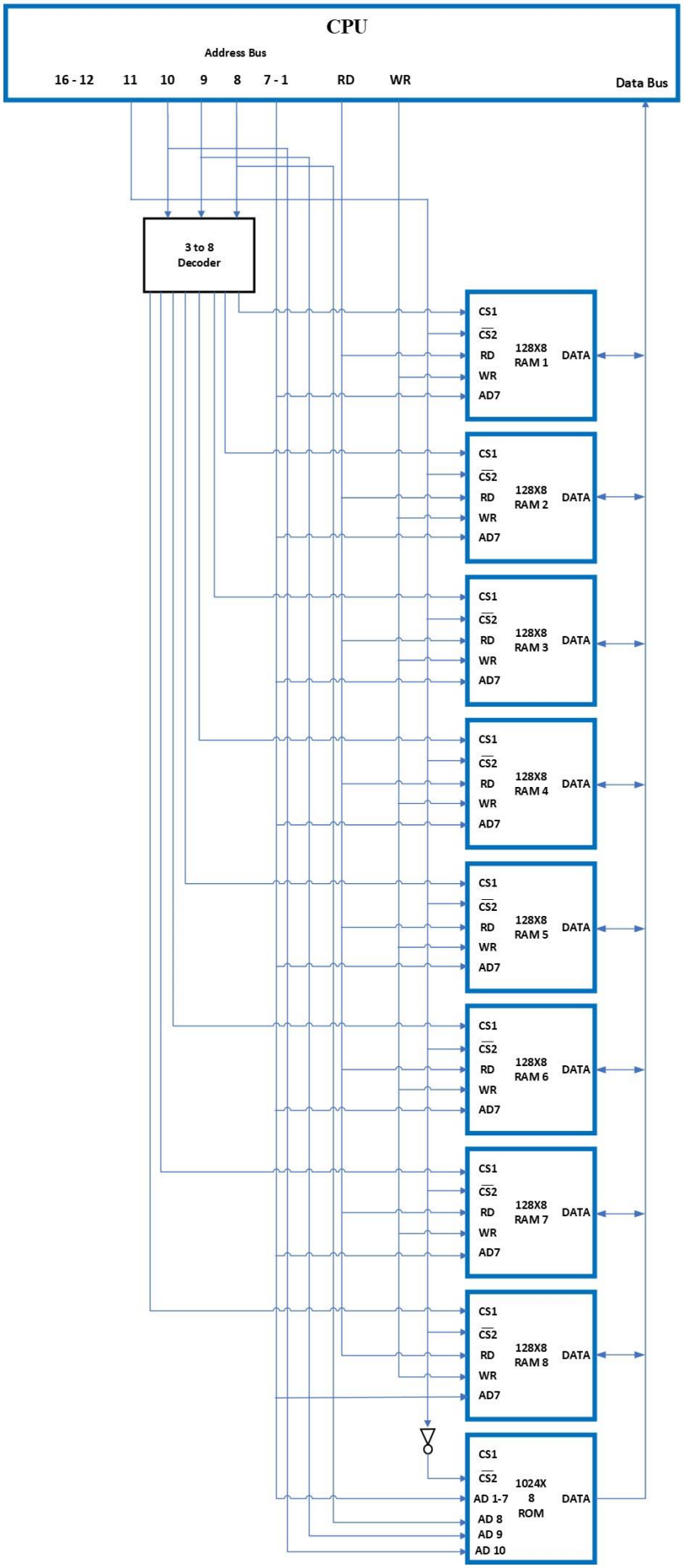
1. Design a memory map for 256B of RAM (128B per block) and 256B of ROM

		Address bus									
Components	Hexadecimal Address	10	9	8	7	6	5	4	3	2	1
RAM 1	0x0000 - 0x007F		0	0	x	x	x	x	x	x	x
RAM 2	0x0080 - 0x00FF		0	1	x	x	x	x	x	x	x
ROM	0x0100 - 0x01FF		1	x	x	x	x	x	x	x	x



2. Design a memory map for 1024B of RAM (128B per block) and 1024B of ROM

		Address bus										
Components	Hexadecimal Address	11	10	9	8	7	6	5	4	3	2	1
RAM 1	0x0000 - 0x007F	0	0	0	0	x	x	x	x	x	x	x
RAM 2	0x0080 - 0x00FF	0	0	0	1	x	x	x	x	x	x	x
RAM 3	0x0100 - 0x017F	0	0	1	0	x	x	x	x	x	x	x
RAM 4	0x0180 - 0x01FF	0	0	1	1	x	x	x	x	x	x	x
RAM 5	0x0200 - 0x027F	0	1	0	0	x	x	x	x	x	x	x
RAM 6	0x0280 - 0x02FF	0	1	0	1	x	x	x	x	x	x	x
RAM 7	0x0300 - 0x037F	0	1	1	0	x	x	x	x	x	x	x
RAM 8	0x0380 - 0x03FF	0	1	1	1	x	x	x	x	x	x	x
ROM	0x0400 - 0x07FF	1	x	x	x	x	x	x	x	x	x	x


CPU
Address Bus
16 - 12
11
10
9
8
7 - 1
RD
WR
Data Bus
3 to 8
Decoder
CS1
CS2
RD
WR
AD7
128X8
RAM 1
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 2
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 3
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 4
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 5
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 6
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 7
DATA
CS1
CS2
RD
WR
AD7
128X8
RAM 8
DATA
CS1
CS2
AD 1-7
AD 8
AD 9
AD 10
1024X
8
ROM
DATA

3. Design a memory map for 2048B of RAM (512B per block) and 2048B of ROM

		Address bus											
Components	Hexadecimal Address	12	11	10	9	8	7	6	5	4	3	2	1
RAM 1	0x0000 - 0x01FF	0	0	0	x	x	x	x	x	x	x	x	x
RAM 2	0x0200 - 0x03FF	0	0	1	x	x	x	x	x	x	x	x	x
RAM 3	0x0400 - 0x05FF	0	1	0	x	x	x	x	x	x	x	x	x
RAM 4	0x0600 - 0x07FF	0	1	1	x	x	x	x	x	x	x	x	x
ROM	0x0800 - 0x0FFF	1	x	x	x	x	x	x	x	x	x	x	x