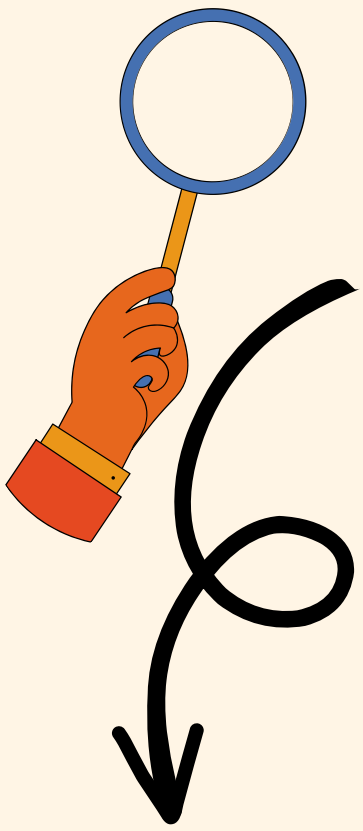
CODTECH

INTERNSHIP

TASKS

VLSI



NOTE:

- MUST ATTEMPT FOUR OUT FOUR TASKS
- SUBMIT BEFORE DEADLINE
- USE INTERNET RESOURCES
- FOLLOW GROUP UPDATES

COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH

CODTECH

INTERNSHIP

TASK -1

ARITHMETIC LOGIC UNIT (ALU)

INSTRUCTIONS:

- DESIGN A BASIC ALU SUPPORTING OPERATIONS LIKE ADDITION, SUBTRACTION, AND, OR, AND NOT.
- DELIVERABLE: A VERILOG/VHDL CODE, TESTBENCH, AND SIMULATION REPORT.

COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH

CODTECH

INTERNSHIP

TASK -2

RAM DESIGN

INSTRUCTIONS:

- DEVELOP A SIMPLE SYNCHRONOUS RAM MODULE WITH READ AND WRITE OPERATIONS.
- DELIVERABLE: CODE, TESTBENCH, AND SIMULATION DEMONSTRATING RAM FUNCTIONALITY.

COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH

CODTECH

INTERNSHIP

TASK -3

PIPELINE PROCESSOR DESIGN

INSTRUCTIONS:

- DESIGN A 4-STAGE PIPELINED PROCESSOR WITH BASIC INSTRUCTIONS LIKE ADD, SUB, AND LOAD.
- DELIVERABLE: A FUNCTIONAL DESIGN WITH SIMULATION SHOWING EACH STAGE'S OPERATION.

COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH

CODTECH

INTERNSHIP

TASK -4

DIGITAL FILTER DESIGN

INSTRUCTIONS:

- DESIGN AND SIMULATE A DIGITAL FIR (FINITE IMPULSE RESPONSE) FILTER USING VERILOG OR MATLAB.
- DELIVERABLE: VERILOG CODE, SIMULATION RESULTS, AND PERFORMANCE ANALYSIS

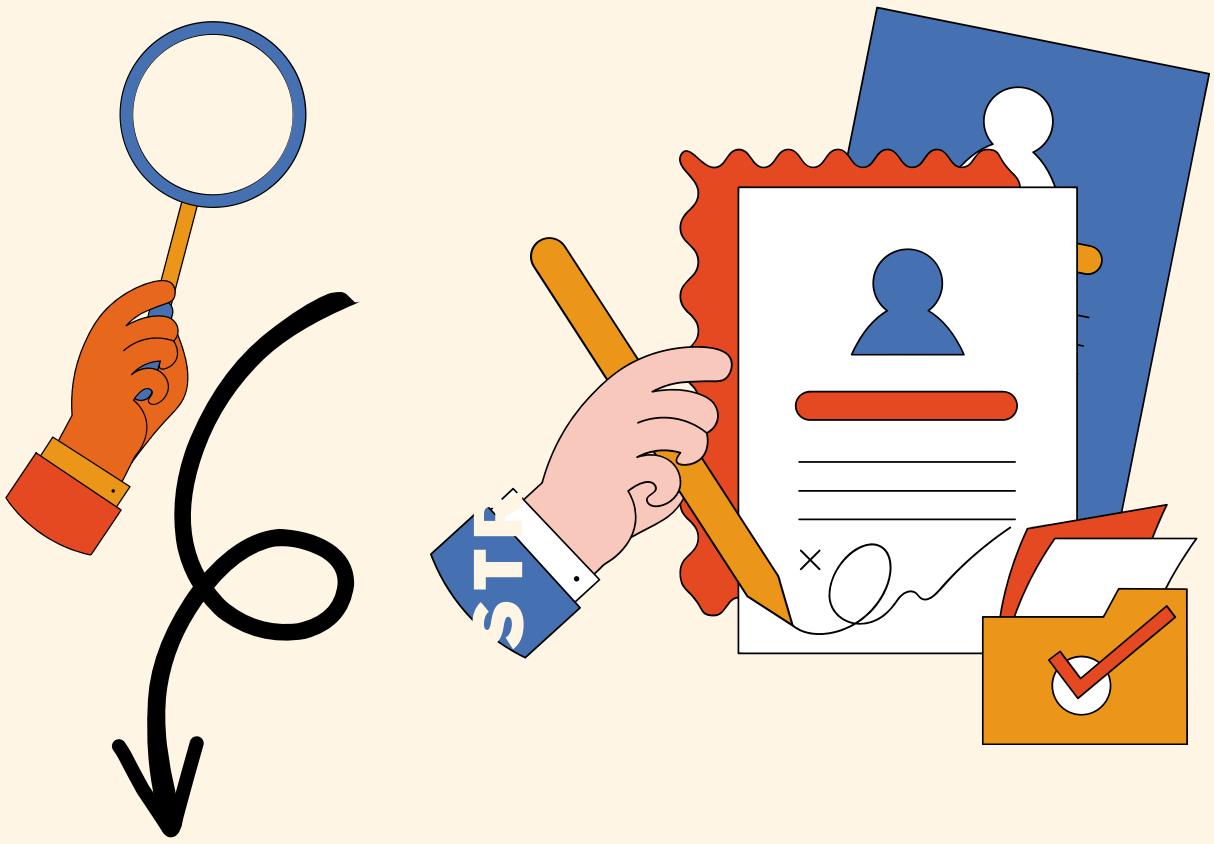
COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH

CODTECH

INSTRUCTIONS

- STORE ALL YOUR WORK-RELATED CODE AND FILES IN A GITHUB REPOSITORY.
- MAINTAIN PROPER COMMENTING IN YOUR CODE FOR BETTER UNDERSTANDING AND READABILITY.
- USE RESOURCES LIKE YOUTUBE, GOOGLE, AND CHATGPT TO HELP YOU COMPLETE TASKS EFFICIENTLY.
- FOLLOW THE VIDEO GUIDANCE PROVIDED IN WHATSAPP WHILE SUBMITTING YOUR TASKS.
- COMPLETE ALL FOUR TASKS AND SUBMIT THEM WITHIN THE DEADLINE WHILE WORKING AT YOUR CONVENIENCE.



CODTECH IT SOLUTIONS

COMPLETION CERTFICATE WILL BE ISSUED ON Y0UR INTERNSHIP END DATE .

CODTECH