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# **Module 1:- VLSI Design flow and Technology Trends**

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**1.1 VLSI Design Flow: Full custom and Semi Custom IC design flow**

**1.2 MOSFET Scaling: Types of scaling**

**1.3 Technology Comparison: Comparison of BJT and MOS technologies, MOSFET Capacitor, MOSFET characteristics.**

# Identify the Image



*Cost  
10,000 \$*

*5 Mb Hard disk being shipped by IBM in 1956*

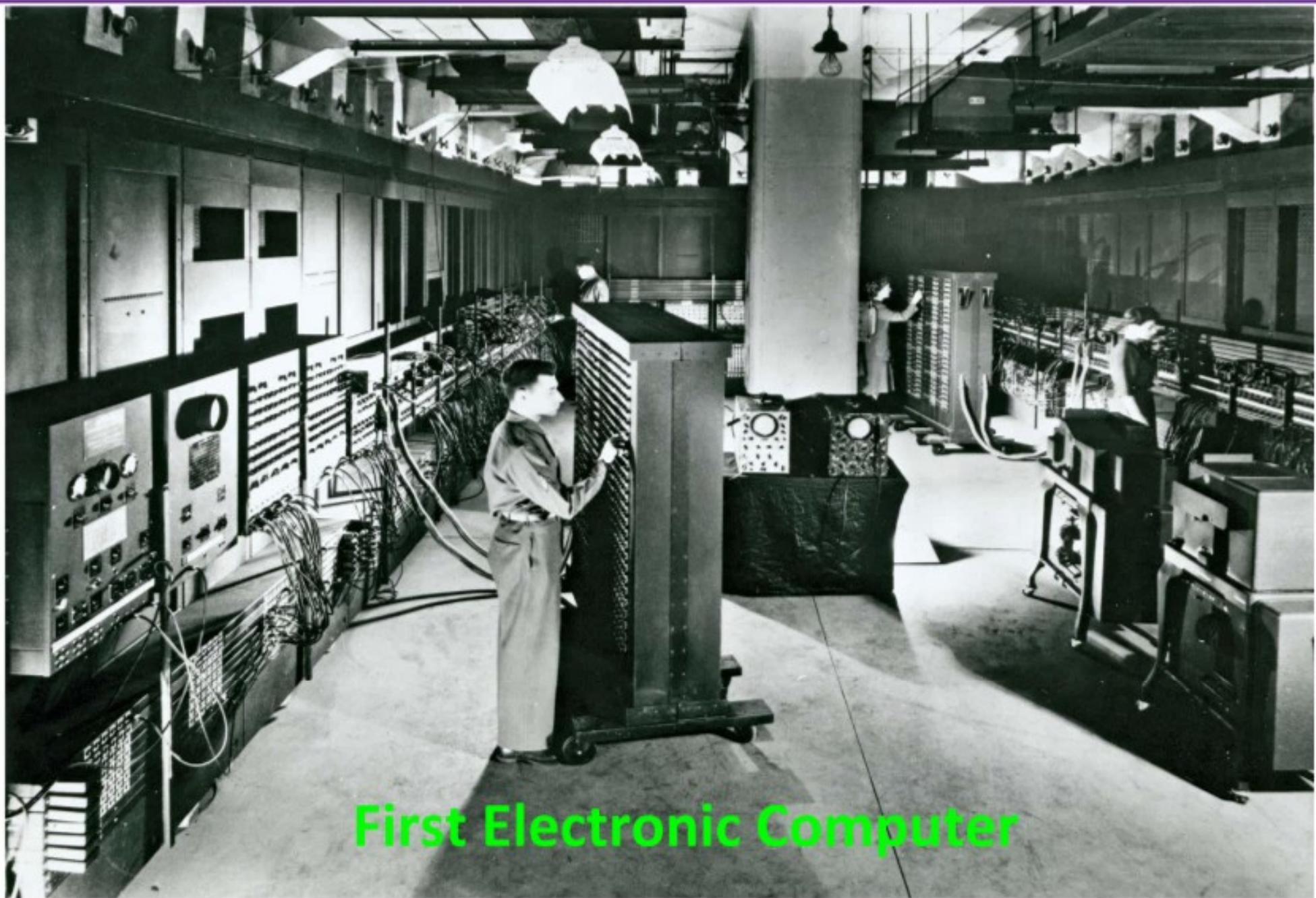
This is called VLSI advancement !!!



*Cost  
800 \$*

*36 Tb Hard disk*

# Identify the Image

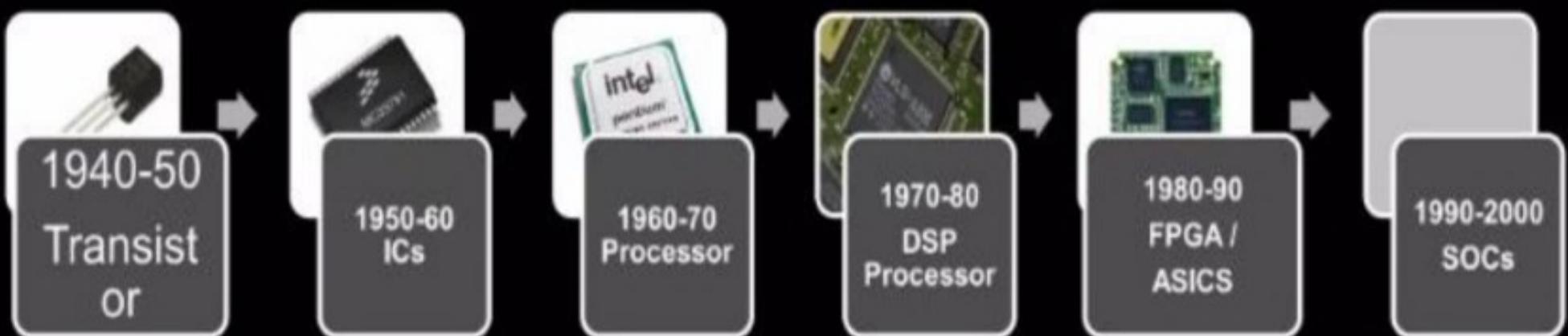


First Electronic Computer

# This achieved because of VLSI

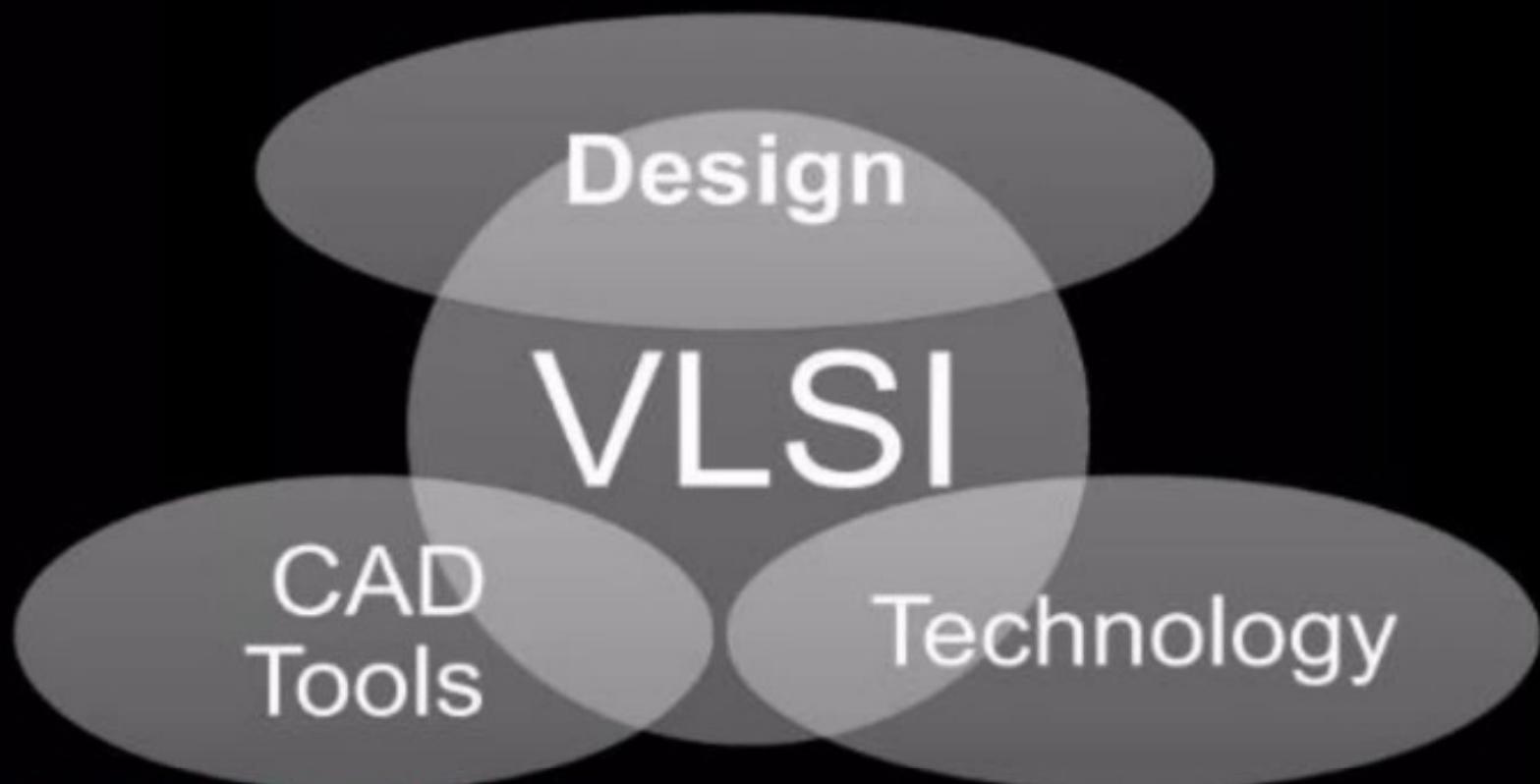


# Timeline of Electronic Devices



# VLSI Domain

Circuit Design, Programming and Analysis



Tools use to Design for  
Circuits and Layout

IC Manufacturing

## VLSI CAD Tools



**SYNOPSYS®**

**cādence™**



**MAGMA**

**Mentor  
Graphics®**

**Tanner  
EDA**

# Top VLSI Companies in India

**AVAGO**  
TECHNOLOGIES



**BOSCH**  
Invented for life



**BROADCOM**



**WIPRO**  
Applying Thought



**HCL** **QUALCOMM**



**TATA ELXSI LIMITED**

**SYNAPSE**  
design

**QUEST**  
BORN TO ENGINEER

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Answering needs. Integrating technologies.

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we are committed



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connect • create • conserve

**SFO TECHNOLOGIES**  
A NeST Group Company



**BHARAT ELECTRONICS**  
QUALITY. TECHNOLOGY. INNOVATION.



National Aerospace Laboratories (NAL)

**PATHPARTNER**

**VVDN**  
TECHNOLOGIES

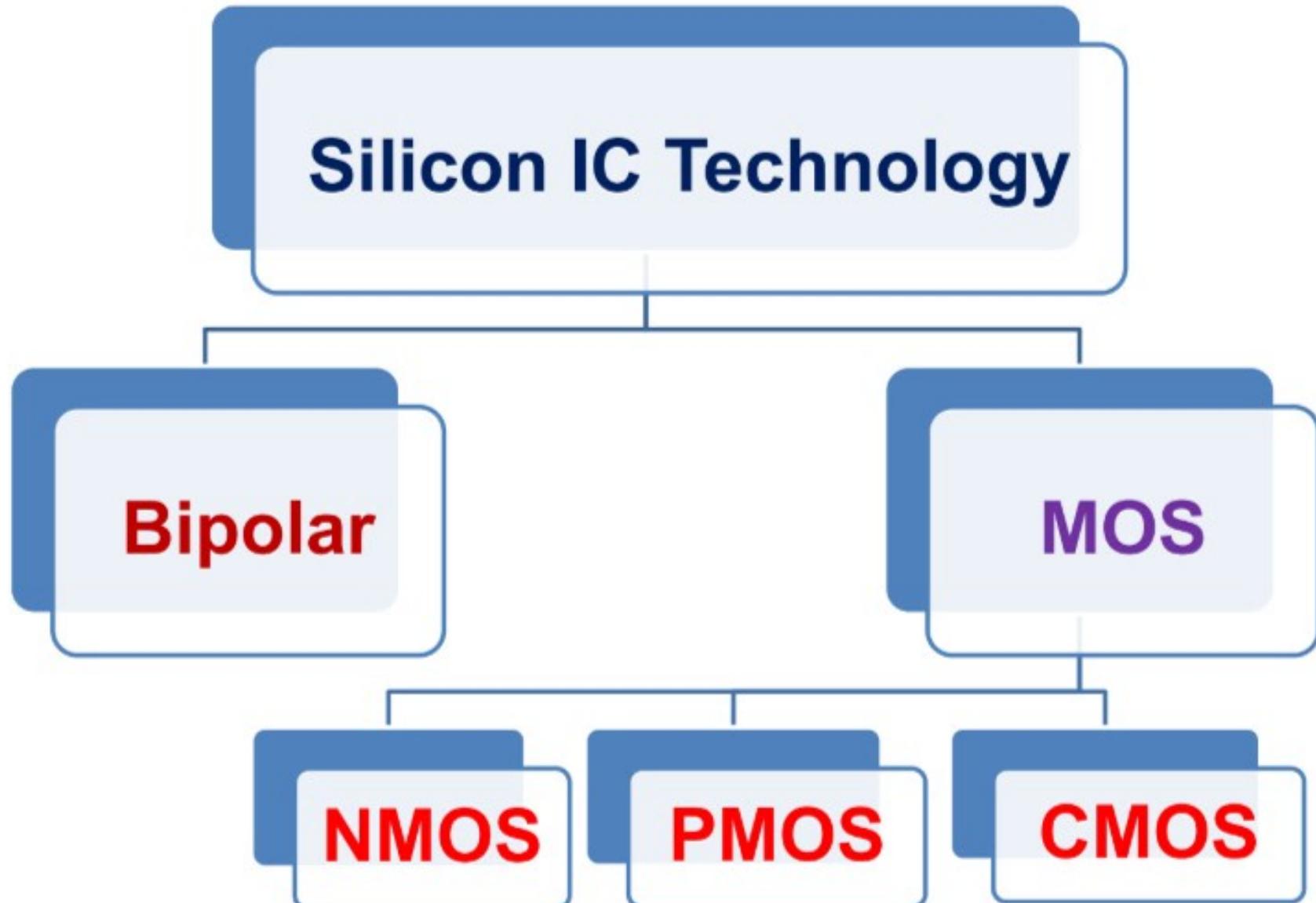
## What is VLSI ?

- Very-large-scale integration (VLSI) is the process of creating an integrated circuit (IC) by combining millions or billions of MOS transistors onto a single chip.
- VLSI began in 1970s when complex semiconductor and communication technologies were being developed.
- Before the introduction of VLSI technology, most ICs had a limited set of functions they could perform.
- With the advent of VLSI designs, the number of applications of integrated circuits (ICs) in high-performance computing, controls, telecommunications, image and video processing, and consumer electronics has been rising at a very fast pace.

## IC Generations

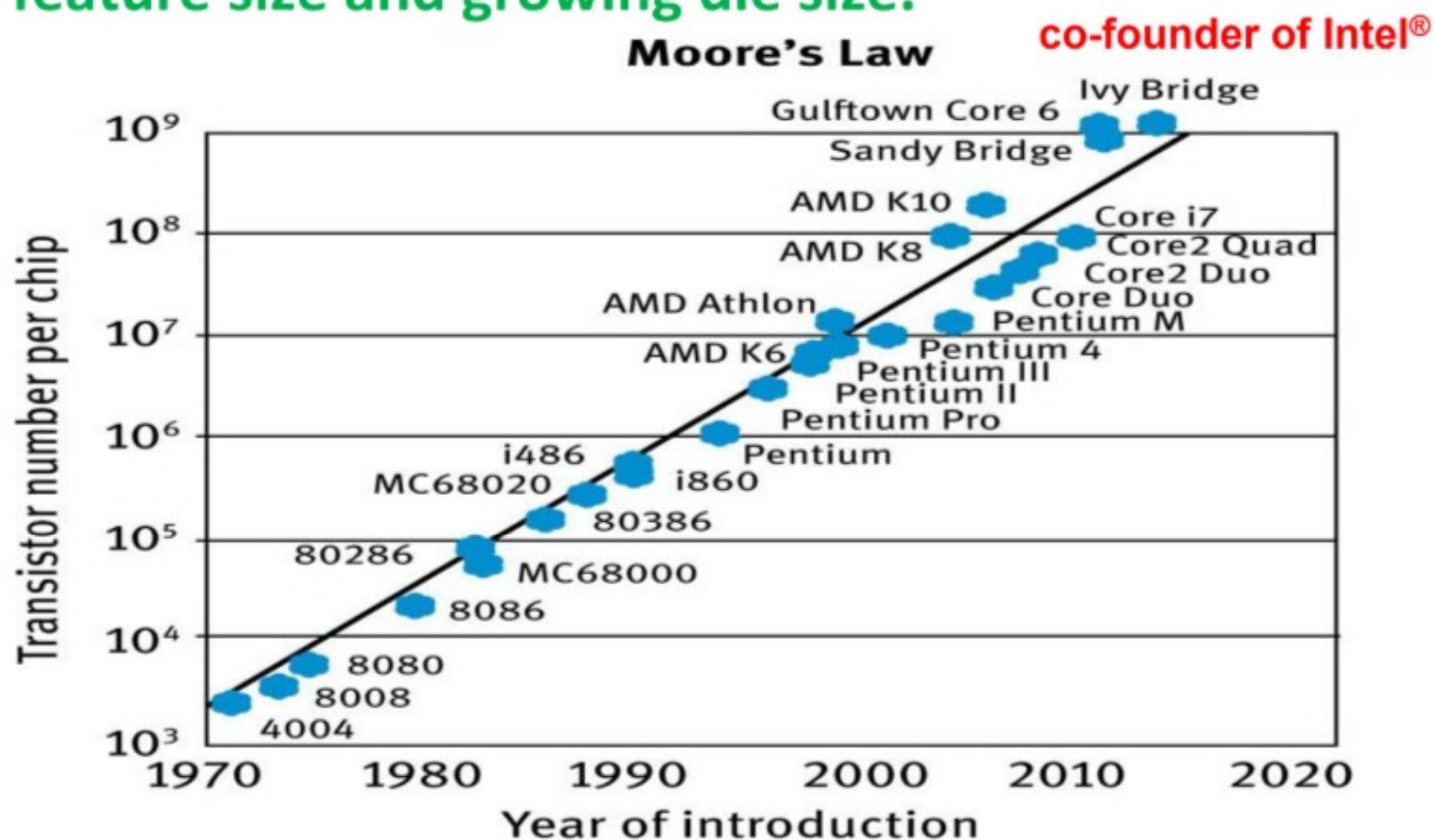
Level of Integration	No. of gates / chip
SSI	1-20
MSI	20-200
LSI	200-2000
VLSI	> 1 Million transistors
ULSI	> 1 Billion transistors

# Technology Trend



## Moore's Prediction

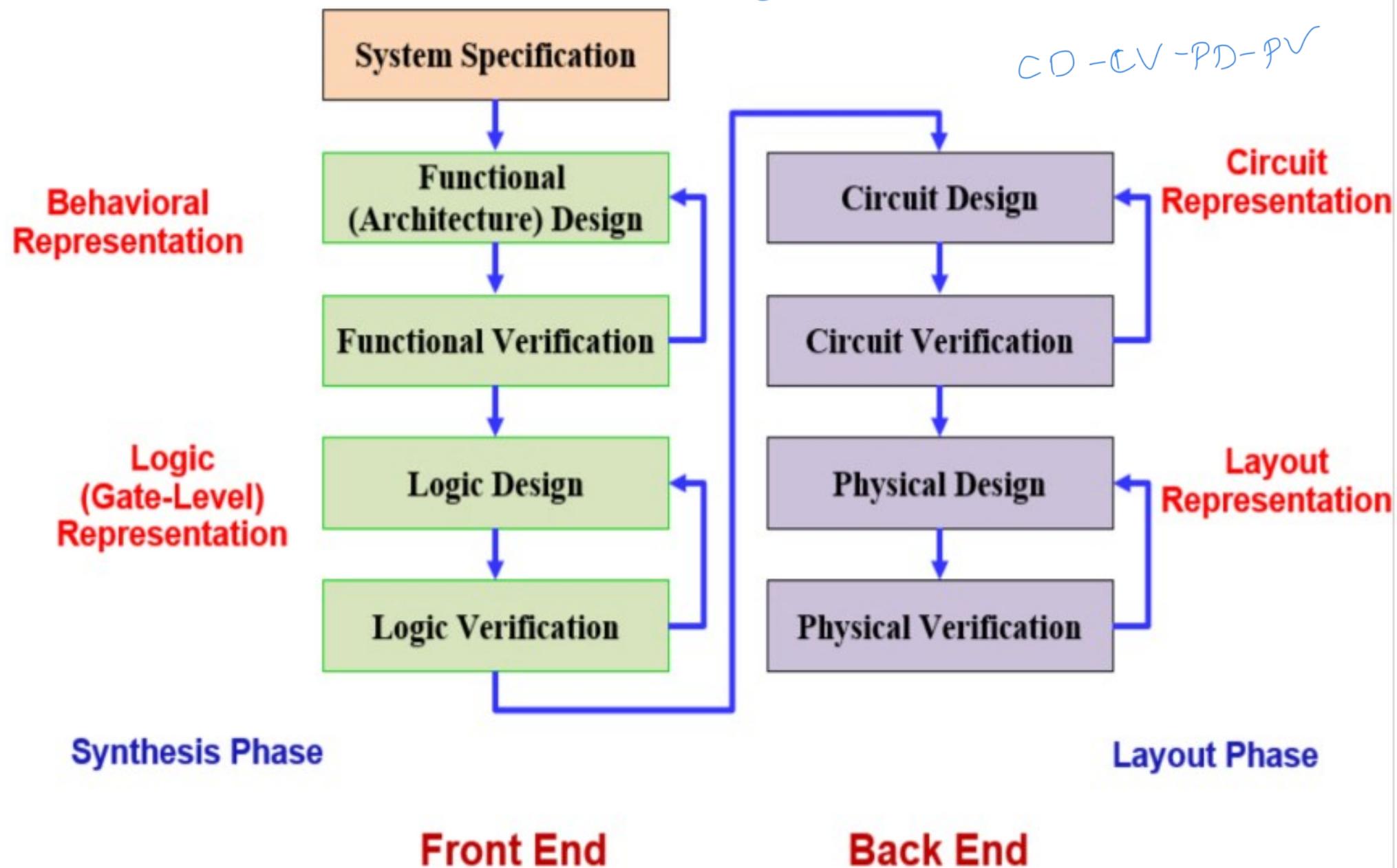
- In the year 1960 ,he predicted that the number of transistors that can be implemented per chip doubles every 1 ½ years because of the shrinking feature size and growing die size.



<b>Year</b>	<b>Chip Type</b>	<b>Capacity</b>	<b>Approx. Transistors</b>
1970	Intel 1103 DRAM	1 Kbit	~1,000
1982	Intel 4164 DRAM	64 Kbit	~65,000
1993	4 Mbit DRAM	4 Mbit	~4 million
2000	256 Mbit DRAM	256 Mbit	~256 million
2015	8 Gbit DDR4 DRAM	8 Gbit	~8 billion
2020	128 Gbit NAND/DRAM	128 Gbit	~100 billion
2025	1 Tb 3D NAND / DDR5 DRAM	1 Tb	~200–300 billion

# **1.1 VLSI Design Flow**

# VLSI Design Flow



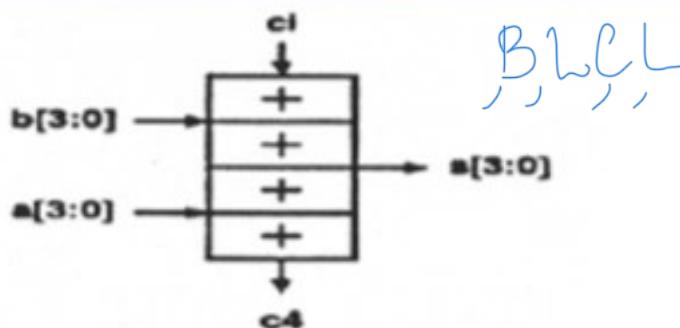
Synthesis Phase

Front End

Back End

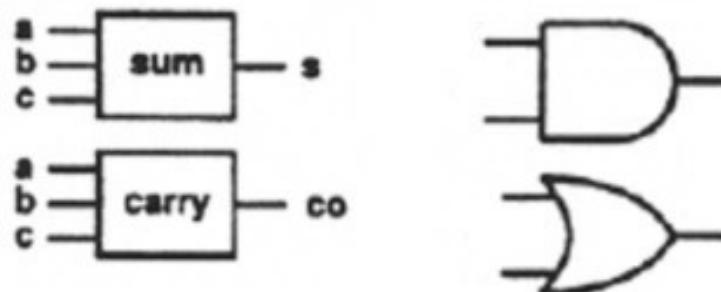
# Four Levels of Design Representation

Behavioral Representation



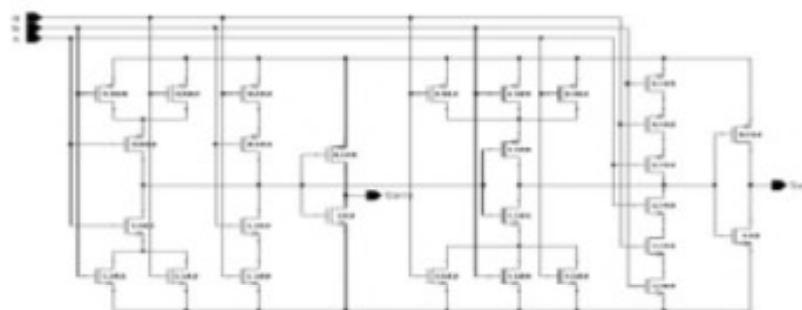
Functional Blocks, FSM

Logic (Gate-Level) Representation



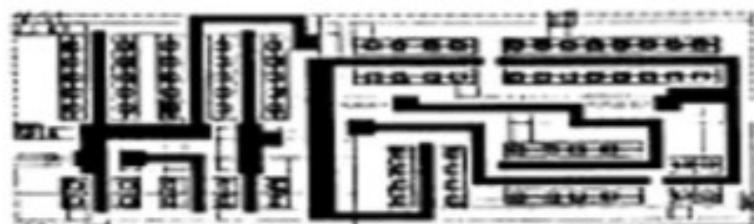
Logic Blocks, Gates

Circuit (Transistor-Level) Representation

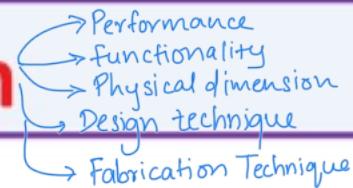


Transistor Schematics

Layout Representation



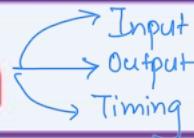
Physical Devices



- First step of design process is to lay down the specification of the system.
- High level representation of the system.

## Factors considered:

- **Performance, Functionality, Physical dimension, Design technique, Fabrication technology**
- It is a compromise between market requirements, technological and economical viability.



- Main functional units, Interconnect requirements of the system are identified.
- The area, power and other parameters of each unit are estimated.
- The key idea is to specify behavior, in terms of **Input, Output, Timing of each unit**
- This information leads to improvement of the overall design process and reduction of complexity of the subsequent phases.

# Logic Design

→ RTL

- Design the logic, that is,  
**Boolean expressions, word width, register allocation, etc.**
- The outcome is called an **RTL (Register Transfer Level)** description.
- RTL is expressed in a **HDL (Hardware Description Language)**, such as **VHDL and Verilog**.

# Circuit Design

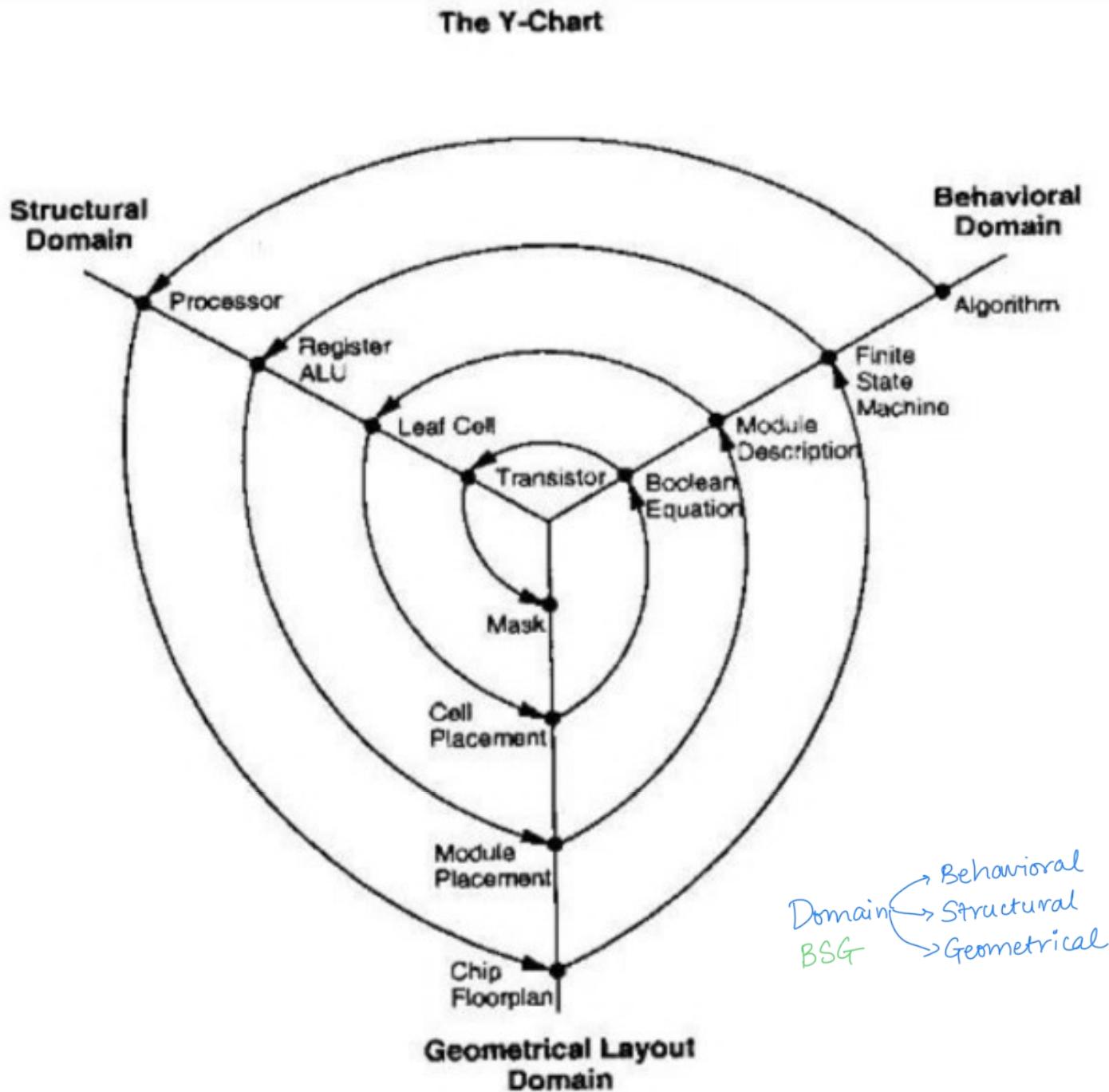
→ speed & power requirements  
→ netlist!

- The purpose of the circuit design is to develop a circuit representation based on the logic design.
- The Boolean expression can be converted into a circuit representation by taking into consideration the speed and power requirements of the original design.
- Design the circuit including gates, transistors, interconnections, etc. The outcome is called a netlist.
- Circuit simulation is used to verify the correctness and timing of component.

# **Physical Design**

**Given a circuit after logic synthesis, to convert it into a layout.**

# Y-chart representation of design flow



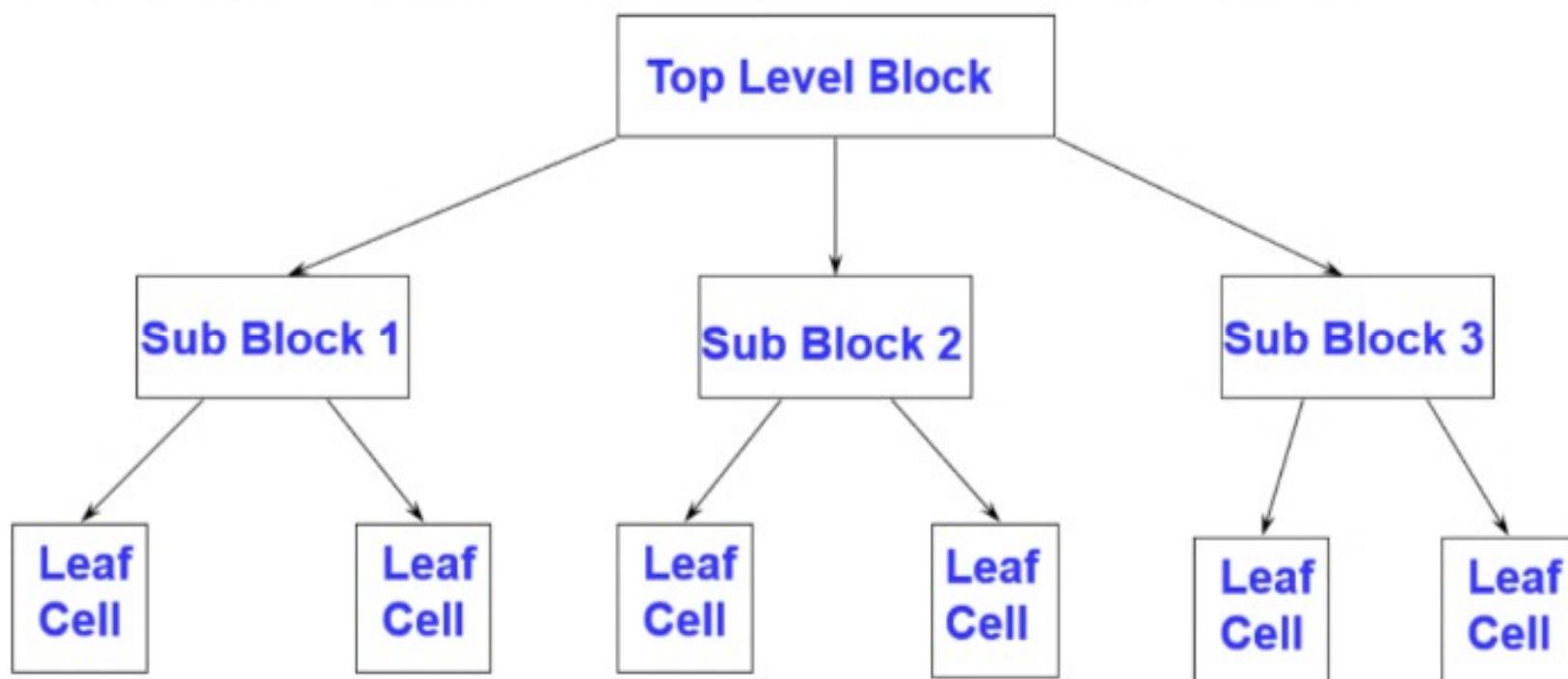
- The Y-chart consist of 3 domain of representation,  
**(1) Behavioral domain, (2) Structural domain and (3) Geometrical layout domain.**
- As shown in figure, the design flow starts from the **Algorithm** that describes the behavior of the target chip , the corresponding **Architecture** of the processor is defined and henceforth mapped on to the chip surface by **Floor planning**.
- In the next level of the abstraction the design in the behavioral domain can be defined using **FSM**, which are structurally implemented with the functional modules ( **Registers / Adder**) and then using automatic **module placement** feature of CAD tools , these modules are then geometrically placed on chip surface followed by Routing.
- The next evolution starts with the **Module description**, individual modules are then implemented using **Logic gates** , which are placed and interconnected by a **cell program and routing program**.

- The last evolution involves description of gates using Boolean equation that is implemented by employing Transistor and finally Mask is generated which is required by various processing steps in the fabrication process.

# Design Methodology

Top-Down  
Bottom-Up

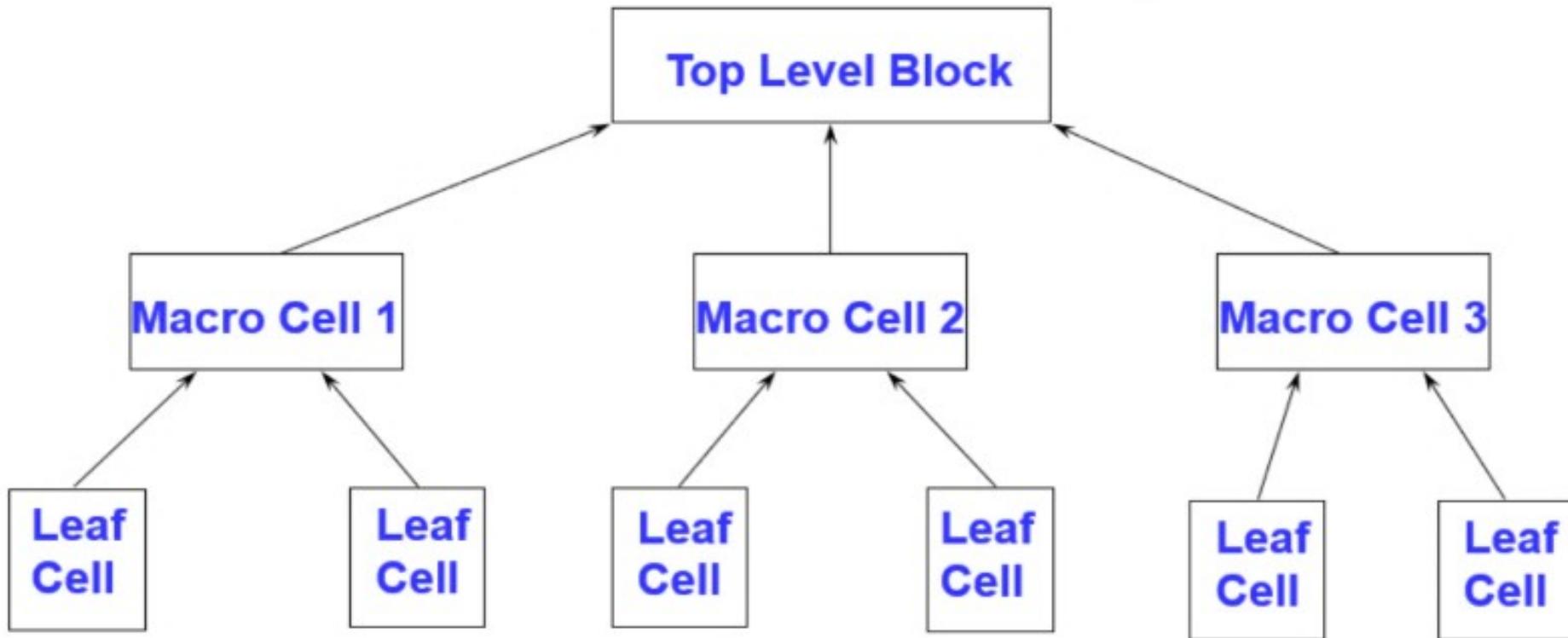
- There are two basic types of design methodologies,
  - ❖ Top-Down design methodology
  - ❖ Bottom-Up design methodology
- ❖ Top-Down Design Methodology top level blocks → Sub-blocks → Leaf cells
- Define top-level block and identify the sub-blocks
- Divide sub-block until we come to leaf cells



## ❖ Bottom-Up Design Methodology

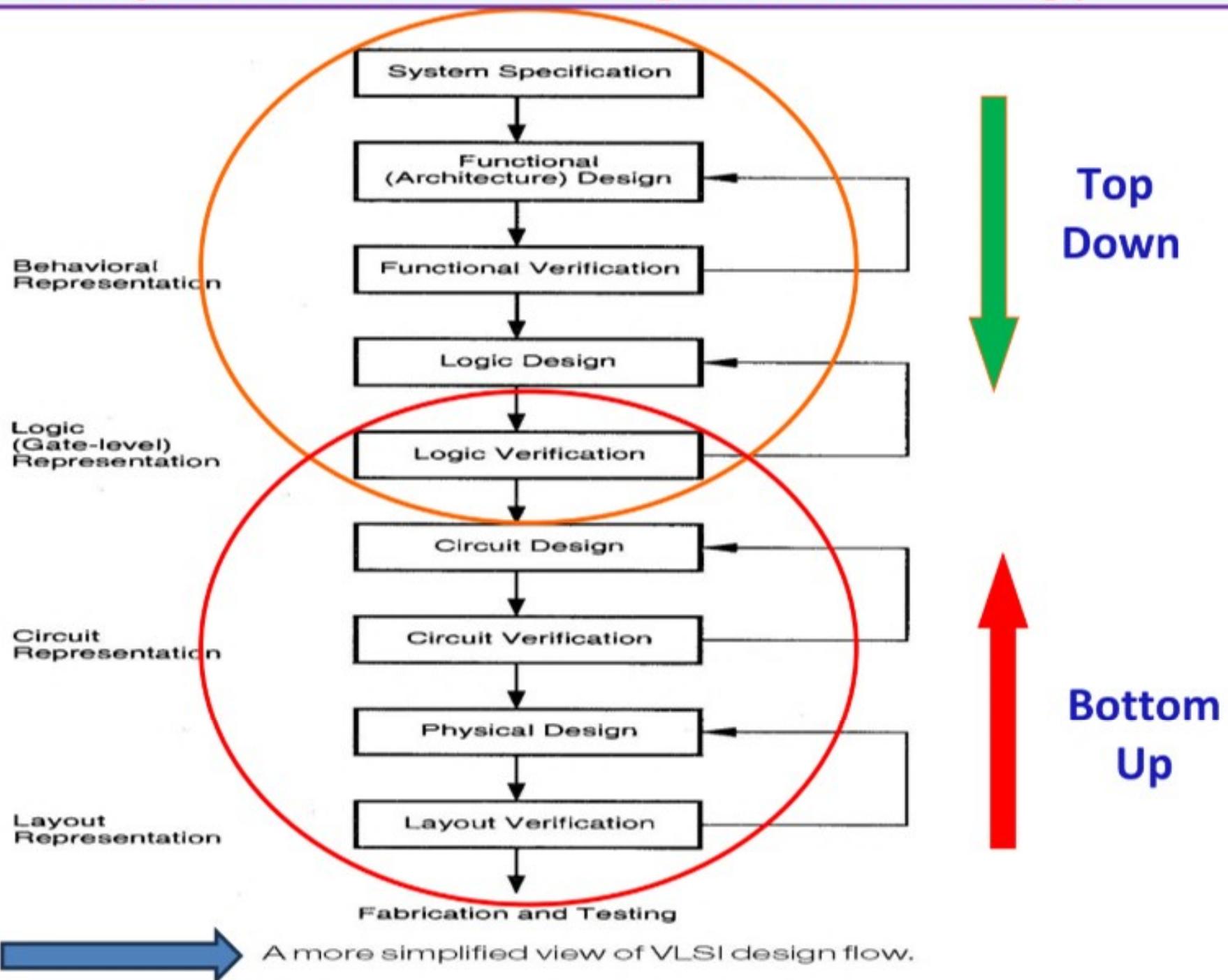
Building Blocks → Bigger cells → Top level

- Identify building block that are available for us
- Build a bigger cells using these block
- Continue build a cell until we build top level

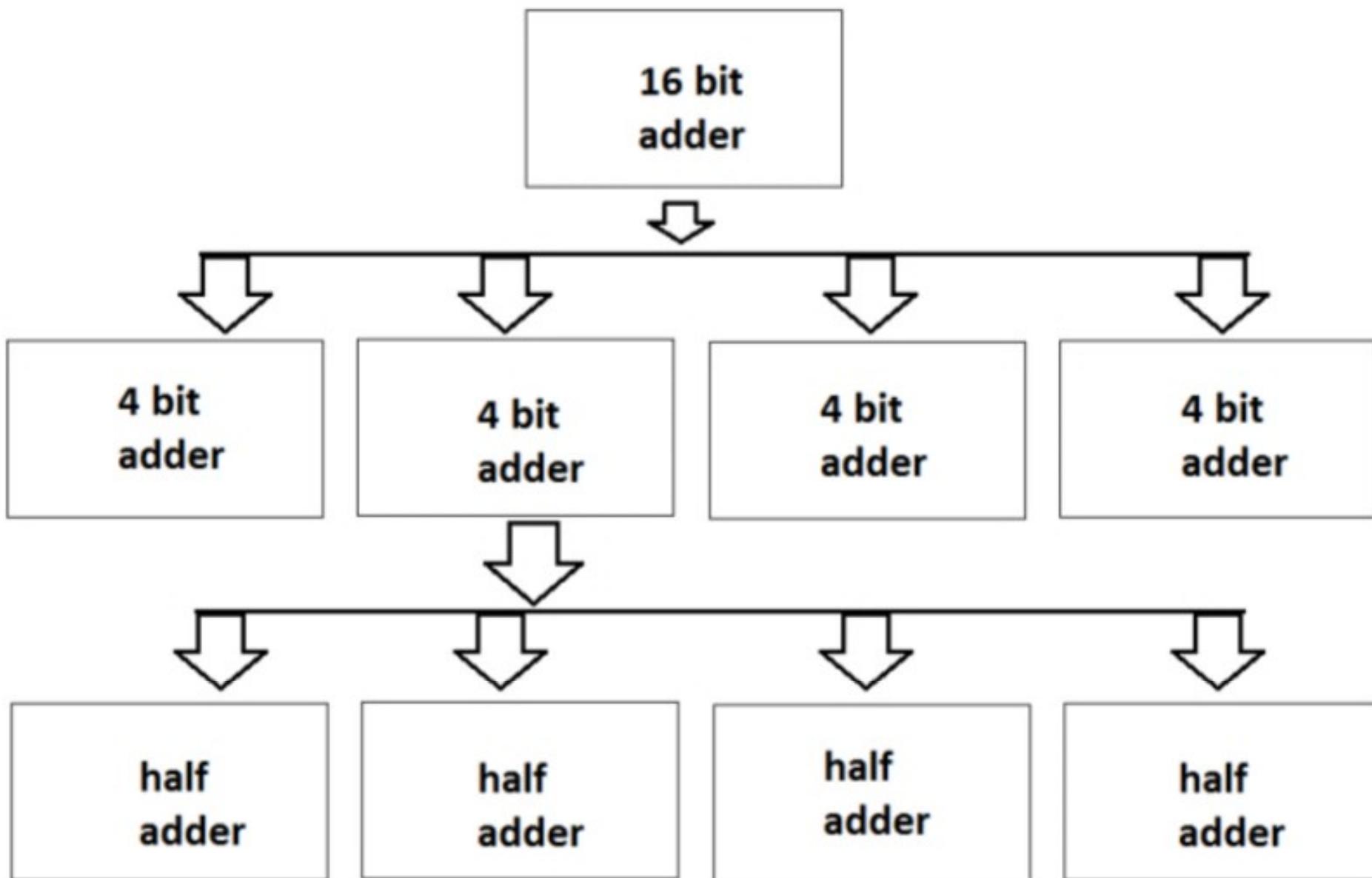


**Note :- A combination of Top-Down and Bottom-Up designs are used in today's digital design**

# Simplified view of Design Methodology



# Structural hierarchy of 16 bit adder circuit



## Design Methodology

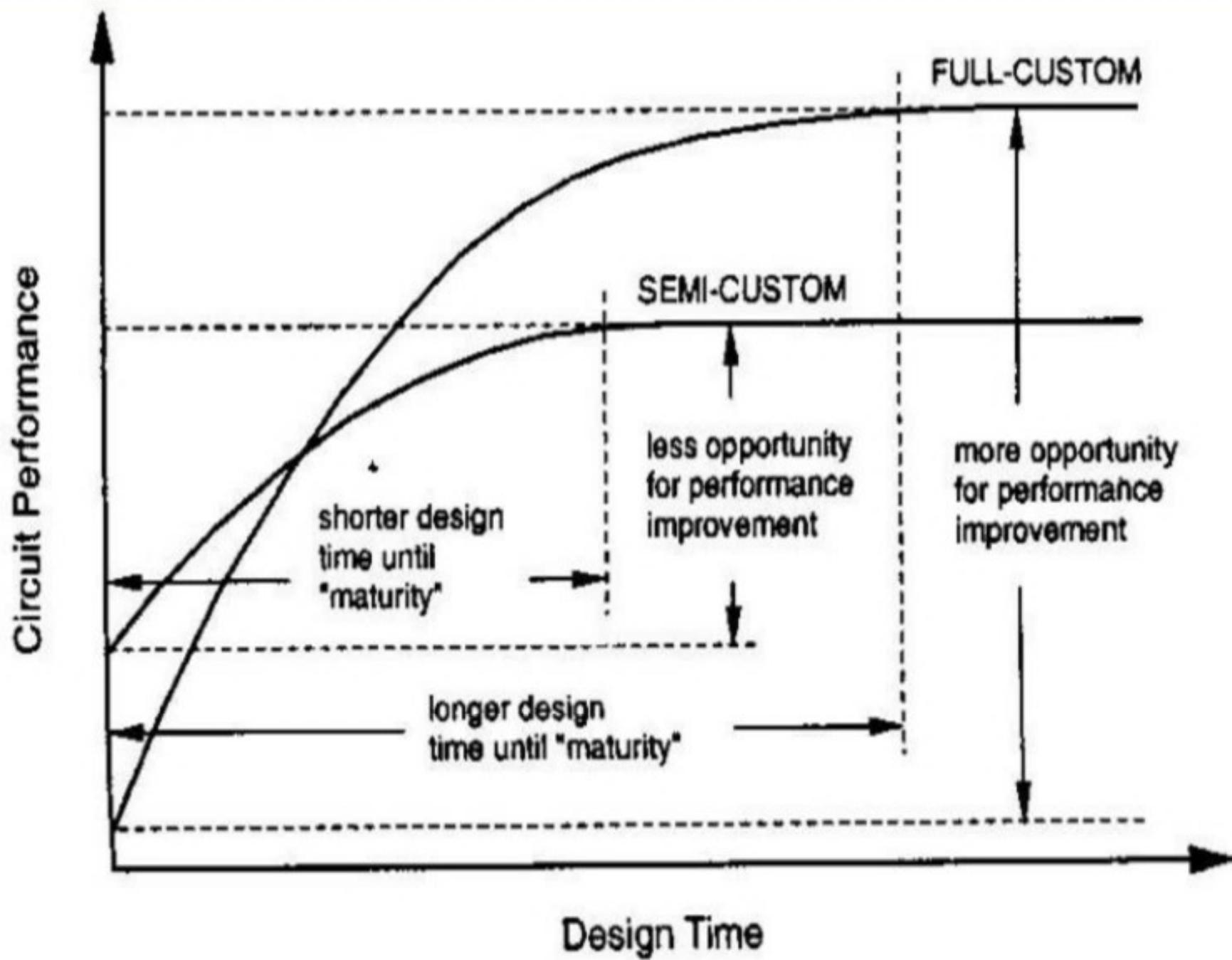
- There are two types of design methodologies,
  - ❖ Full custom design
  - ❖ Semi custom design
  - ❖ Full custom design *GOP*
- In this design method, the geometry, orientation and placement of each transistor is done individually by the designer.
- It increases the performance of the chip and reduces the area.
- Design or production time of full custom design is more
- Development cost is high.
- Use for mass production and to optimize speed and power. Eg . Microprocessor , ASIC etc...

## ❖ Semi custom design

PP

- It uses predefined and pretested modules in its design.
- This will reduce the design time but it is not optimized and cost-efficient for mass production.
- This design methodology is used where there is less time for design and fewer quantities.
- Eg. Programmable logic devices ( PLD ,CPLD , FPGA etc..) ,  
Gate array , standard cells etc...

# Impact of Different VLSI design styles



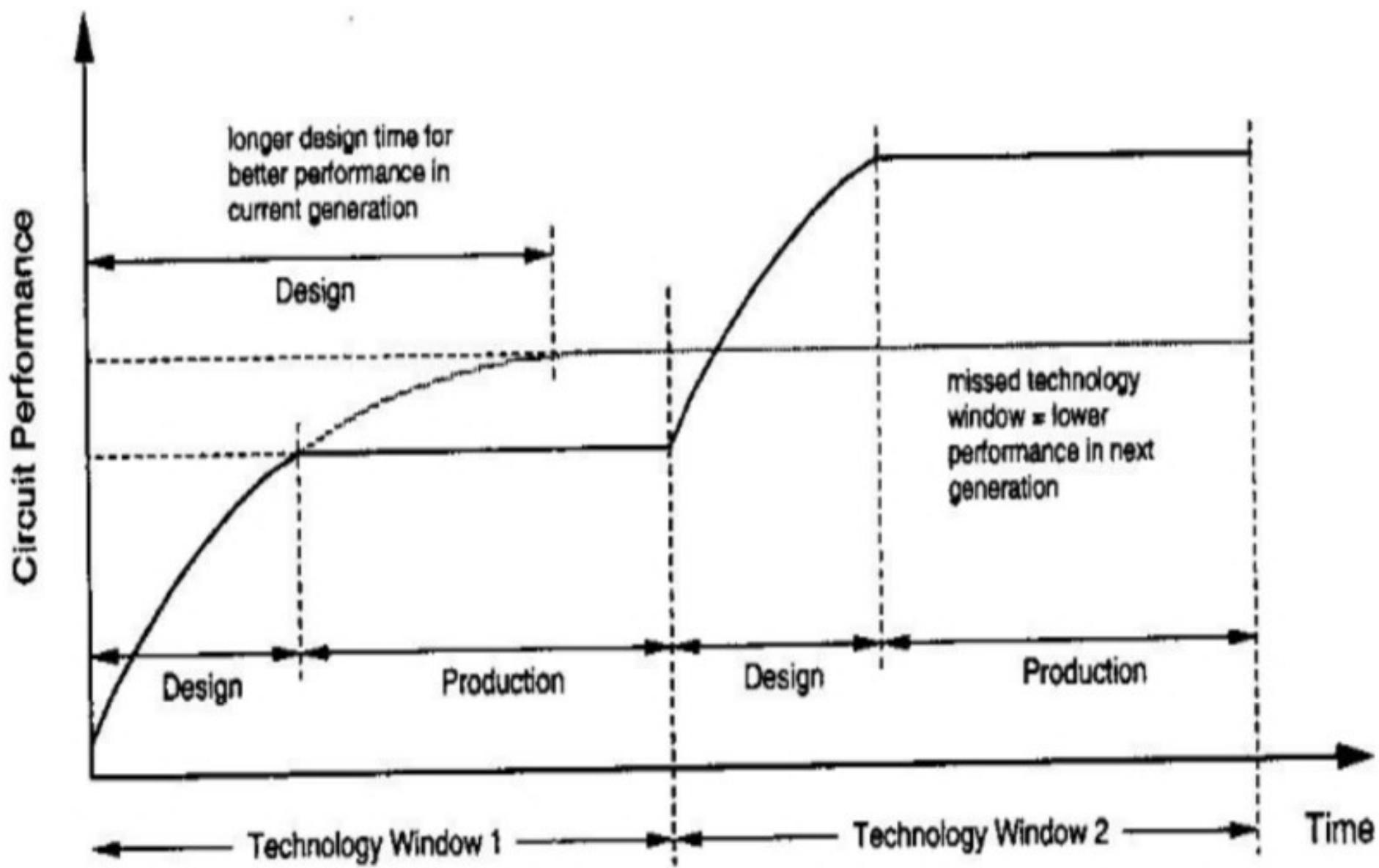
- As shown in fig. full custom design requires longer time, until the design maturity can be reached, thus allows more opportunity for the circuit performance improvement.
- The final product typically has high level performance.  
eg. High processing speed, low power dissipation etc..
- Also Silicon area is relatively small because of better area utilization.
- But, due to the large product time, this method is costlier.
- It is useful only for mass production.
- In contrast, semi custom design allows shorter design time but it offers less opportunity for performance improvement thus performance of final product will inevitably less than that of full custom design.

# Difference between full custom and semi custom

Parameters	Full custom	Semi custom
Methodology	Complete design, implementation , placement is done from transistor level	Predesigned and pretested modules are used for designing
Cost	High	Low
Time required	More	Less
Circuit performance	High	Low
Circuit speed	High	Less
Circuit complexity	More complex	Simple
Mass production	It can be used	It can not be used
Example	Microprocessor, ASIC	FPGA,CPLD,Standard cell

- The choice of particular design style of VLSI product depends upon,
  1. The performance requirements → PR
  2. The technology being used → T
  3. The expected lifetime of the product → lifetime
  4. Cost of the project → cost

# Progressive performance improvement



- It can be seen that, the design cycle time of a successful VLSI product is kept shorter, which would be necessary for developing an optimum performing chip, thus leaving enough time for the production and marketing of chip during the current generation or Technology window.
- When the next generation manufacturing technology arrives, the design can be updated to take the advantage of higher integration density & better performance.
- On the other hand, if the design time of particular product is kept excessively long to achieve the highest possible performance for the current generation technology, there is danger of missing the next technology window.
- A longer design cycle time usually results in a better overall performance, but this product must then remain viable in the market for certain amount of time in order to recover the development cost.

- Thus, the advantage brought by the next generation manufacturing technologies can not be utilized and product becomes less competitive.
- In reality, the design cycle of the next generation chips usually overlaps with the production cycle of the current generation chips, thereby assuring continuity.
- The use of sophisticated CAD tools and methodologies are also essential for reducing the design cycle time and for managing the increasing design complexity.
- Thus, at an early stage of design, the designer needs to make the decision of which methodology should be adopted for the design and choice is normally based on available design time, cost and functionality of the circuit.

# **1.2 MOSFET**

# Metal Oxide Semiconductor Field effect Transistor (MOSFET)

- MOSFETs is an electronic device used to switch or amplify voltages in circuits.
- It is a voltage controlled device.
- It is constructed by three terminals.
- The terminals of MOSFET are named as follows:



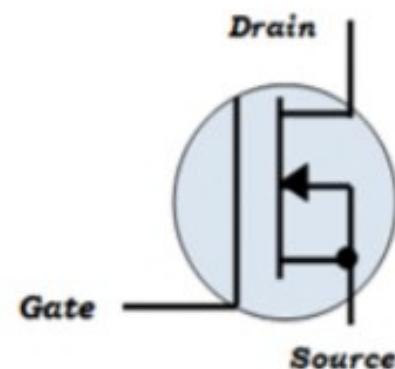
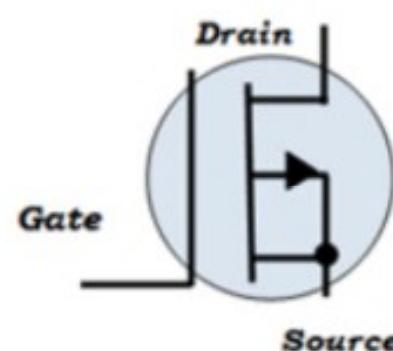
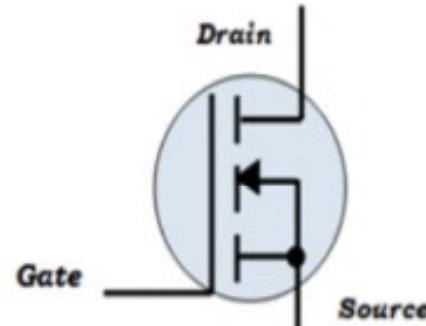
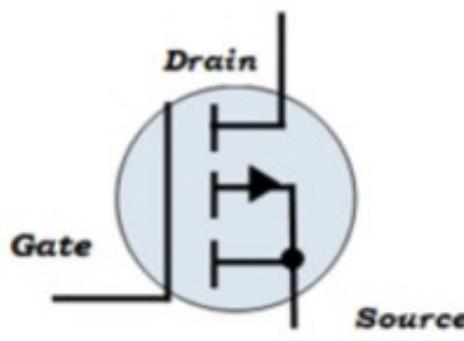
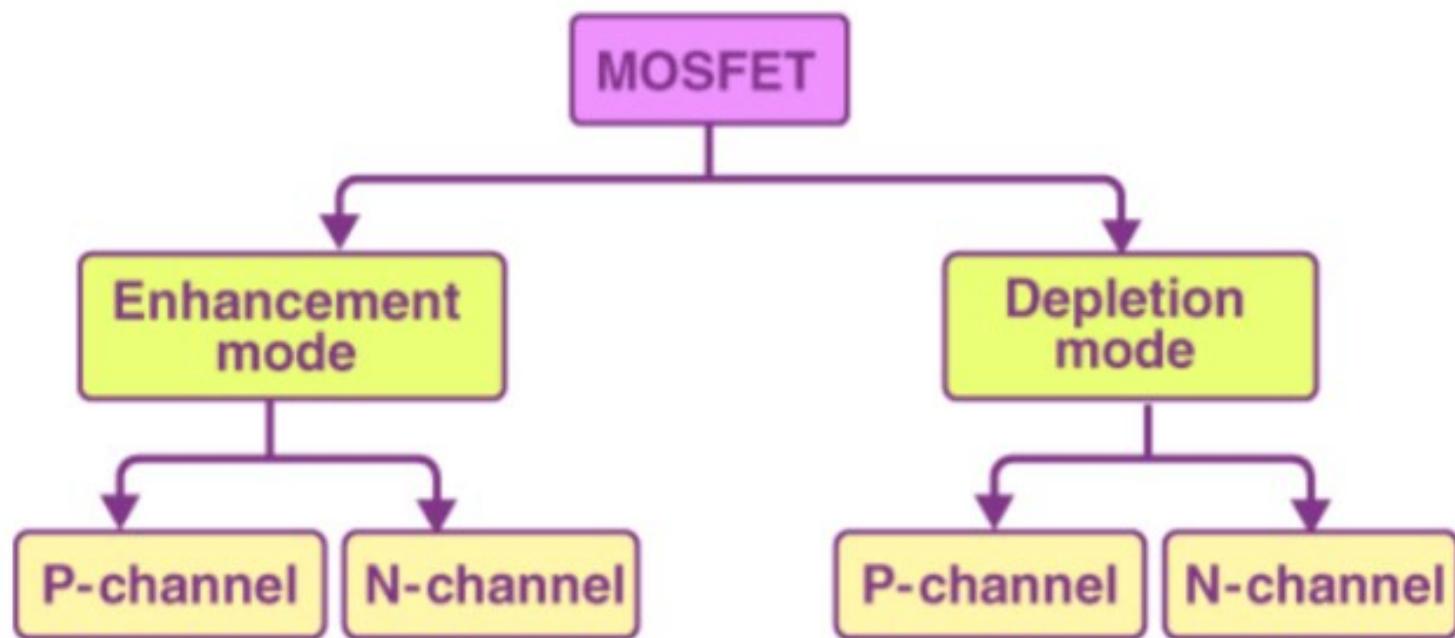
**Source**  
**Gate**  
↓  
**Drain**  
**Body**

## Working Principle of MOSFET

- When voltage is applied to the gate, an electrical field is generated that changes the width of the channel region, where the electrons flow.
- The wider the channel region, the better is the conductivity of a device.

volt. app@gate → EF generated → changes width of channel.

# Classification of MOSFET

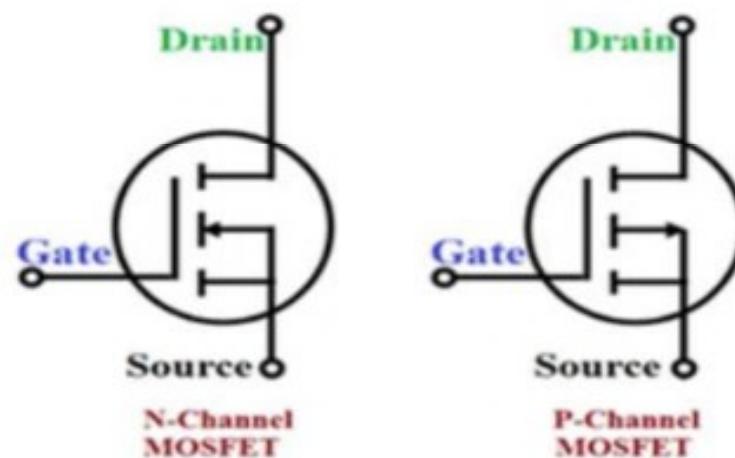


# Enhancement MOSFET

- They are normally OFF device.
- Channel is formed only after applying the Gate voltage.
- Gate to Source voltage is responsible for the flow of current from Drain to Source terminal of the MOSFET.
- An enhancement-type MOSFET is so named an enhancement device, because as the voltage to the gate increases, the current increases more and more, until at maximum level.

Symbol

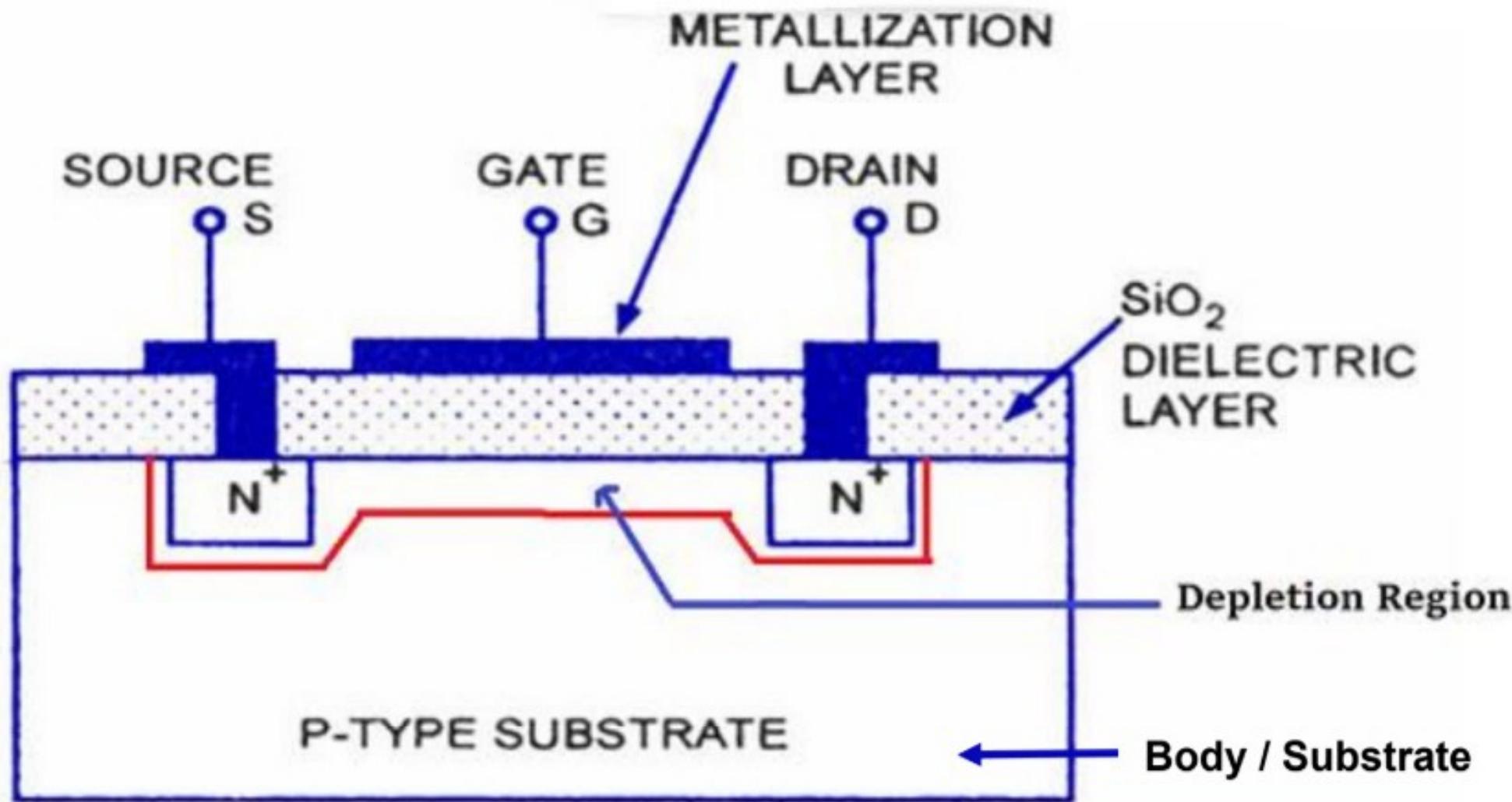
$$V_{GS} \rightarrow I_{DS}$$



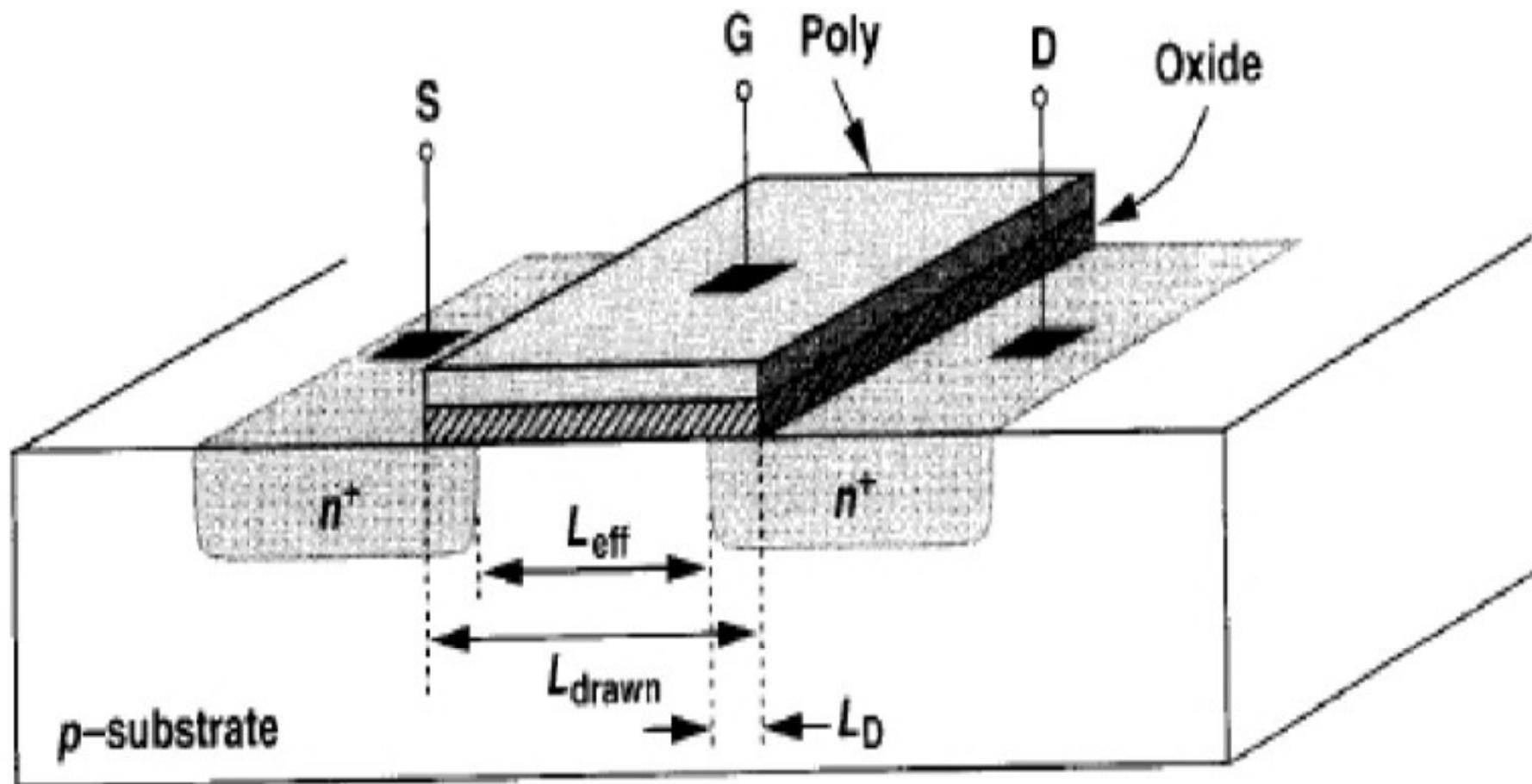
## Construction of Enhancement MOSFET

- The MOSFET consists of three terminals, they are source(S), Gate (G), Drain (D) and the body which is called as substrate. The substrate is connected to the source internally.
- The metallic gate terminal in the MOSFET is insulated from the semiconductor layer by a SiO<sub>2</sub> layer or dielectric layer.
- In N channel Enhancement MOSFET the source and drain are of N type semiconductor which is heavily doped and the Substrate is of P type semiconductor. Majority charge carriers are electrons. The source and drain terminals are physically separated in Enhancement mode.
- In P channel Enhancement MOSFET the source and drain are of P type semiconductor which is heavily doped and the Substrate is of N type semiconductor. Majority charge carriers are holes.

# Construction of n-channel Enhancement MOSFET

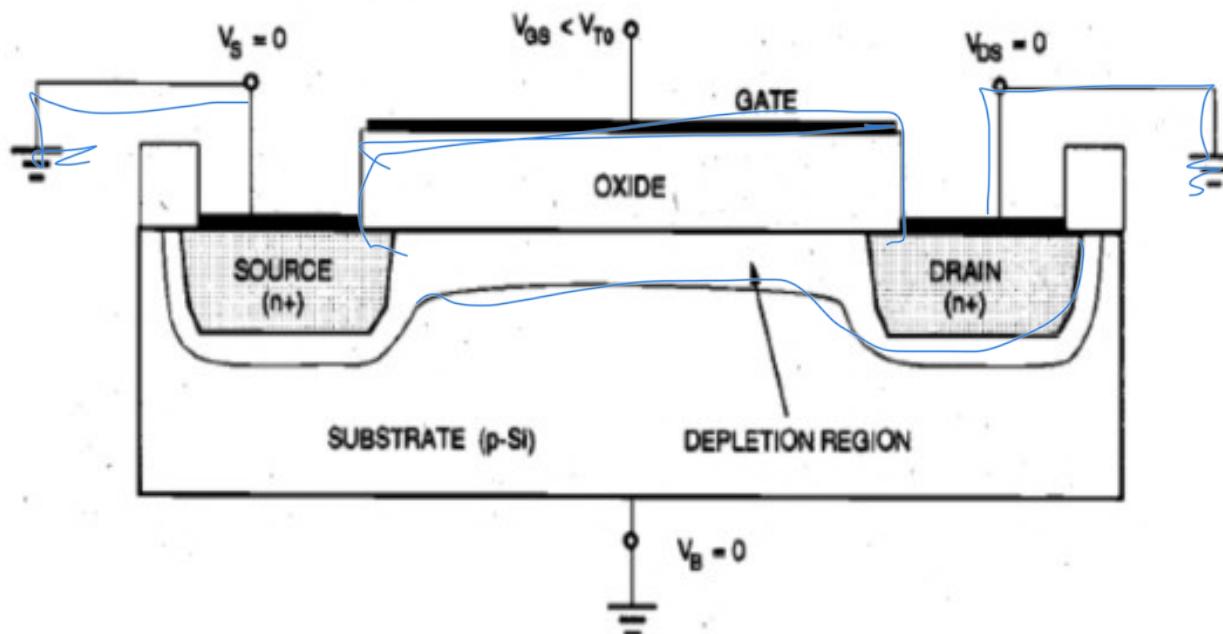


# Cross sectional view of n-channel Enhancement MOSFET



# Working of n channel Enhancement MOSFET

Case 1 :- Small Positive Gate voltage is applied ( $V_G < V_{th}$ )

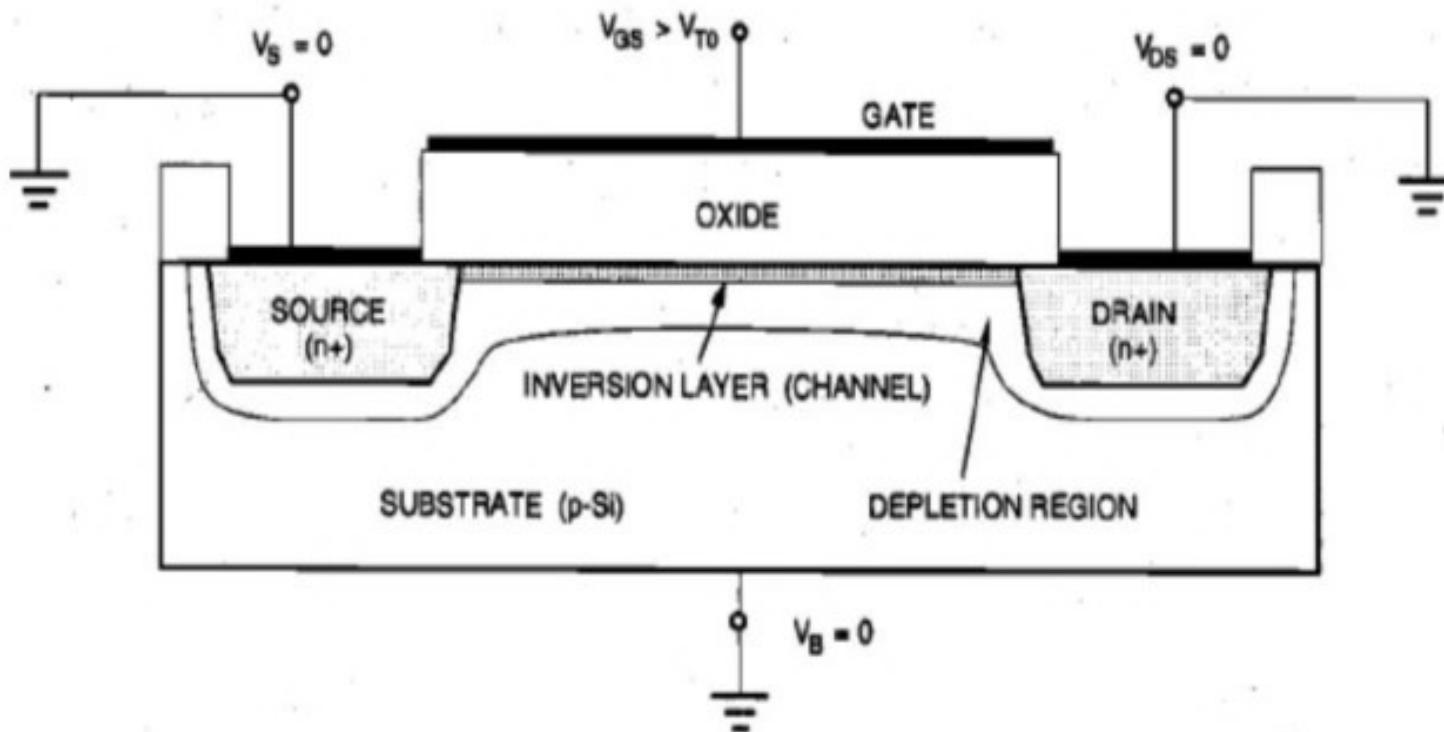


( $V_G < V_{th}$ )

$V_{th}$  is threshold voltage which when applied to gate, channel is formed beneath the  $\text{SiO}_2$  layer and Drain current start flowing from Drain to Source.

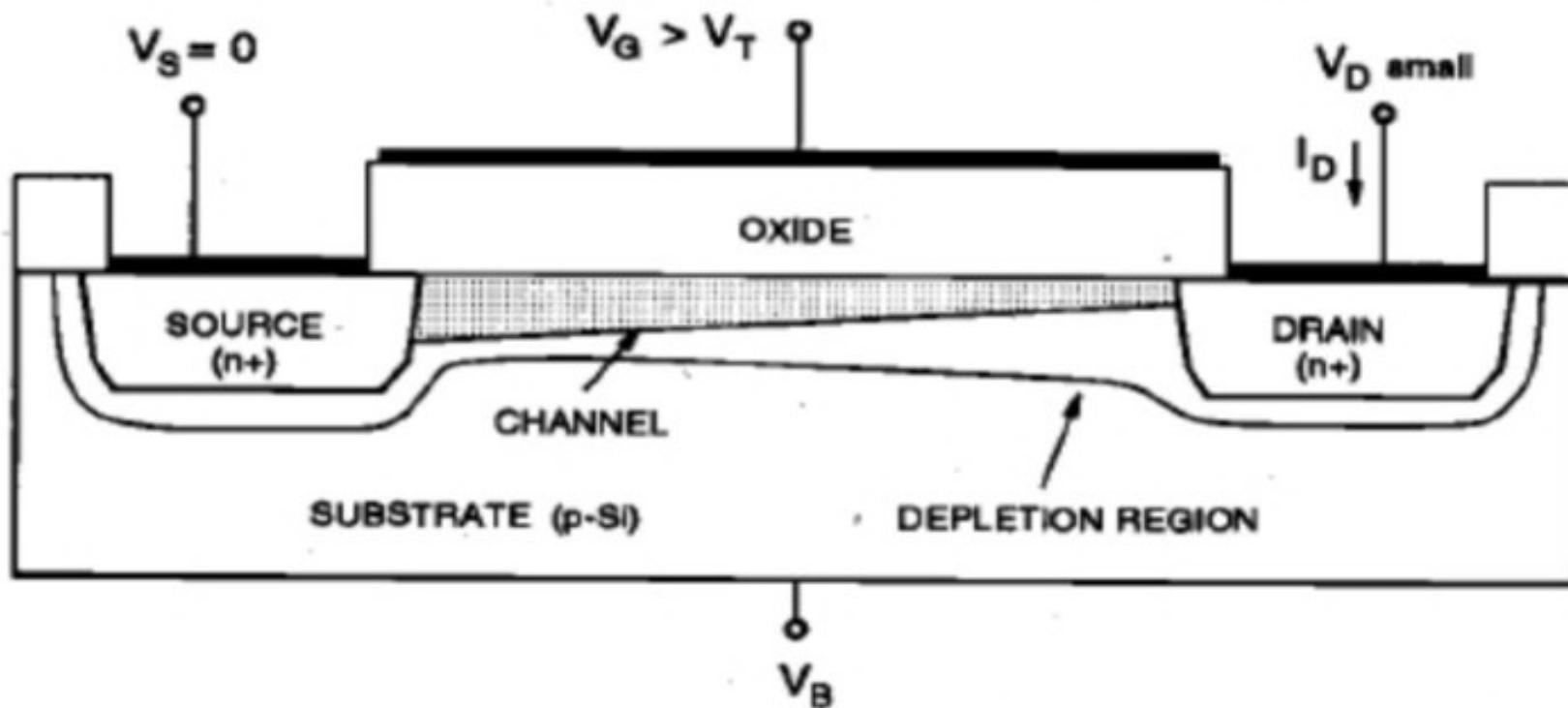
- When positive gate voltage with  $V_G < V_{th}$ , is applied to the gate terminal, the holes in the p type substrate is repelled and produces fixed immobile ions at the oxide layer.
- Because of the fixed immobile ions current conduction between source and drain is not possible ( ie channel is not formed)

## Case 2 :- More Positive Gate voltage is applied ( $V_G > V_{th}$ )



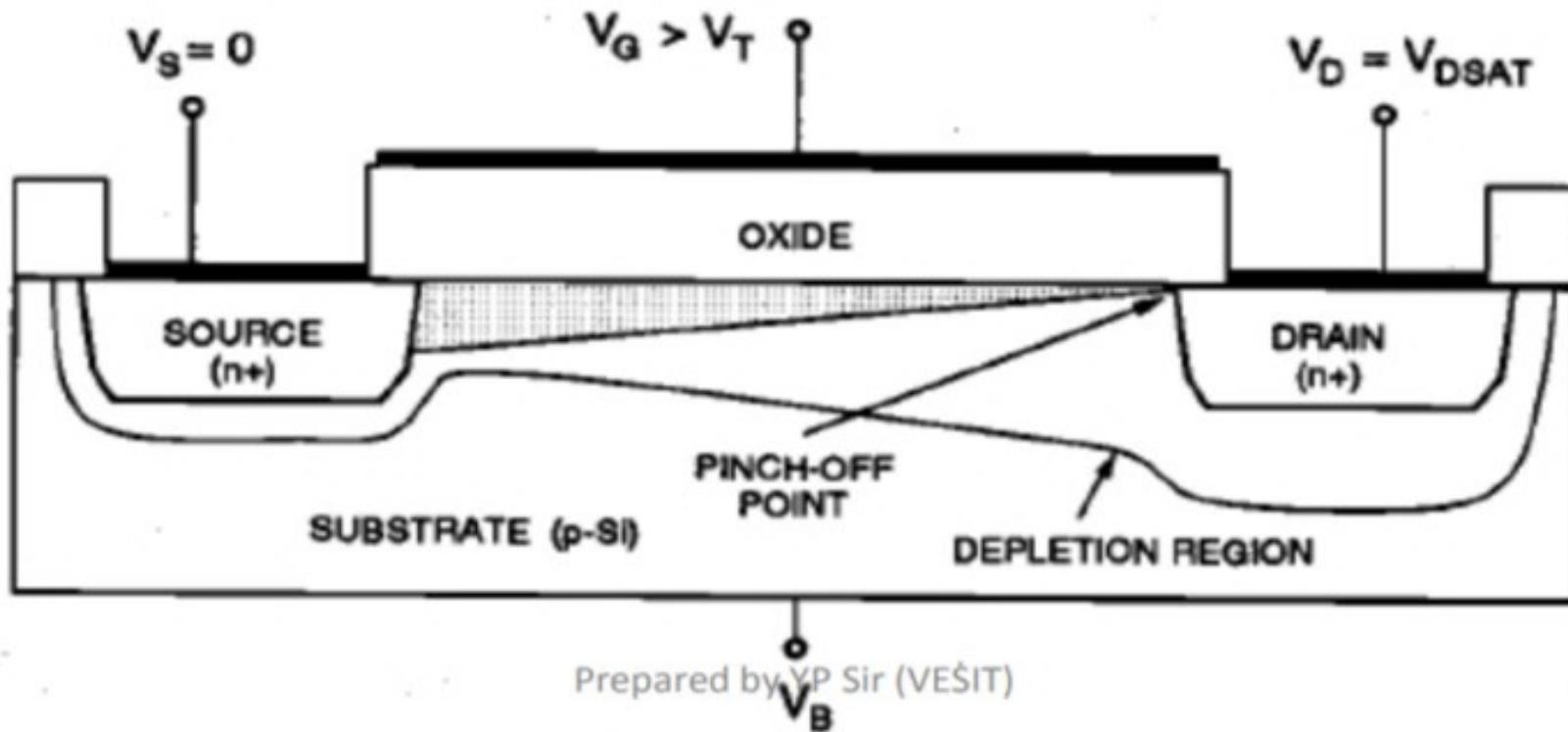
- When  $V_G > V_{th}$ , is applied to the gate terminal, the minority electrons present in the p type substrate is attracted underneath of the surface , the surface inversion will be established.
- Conducting n type layer will be formed between source and drain.
- This channel now provides electrical connection between the two n+ regions which allows current to flow.

### Case 3 :- If $V_G > V_{th}$ and small $V_{DS}$ is applied



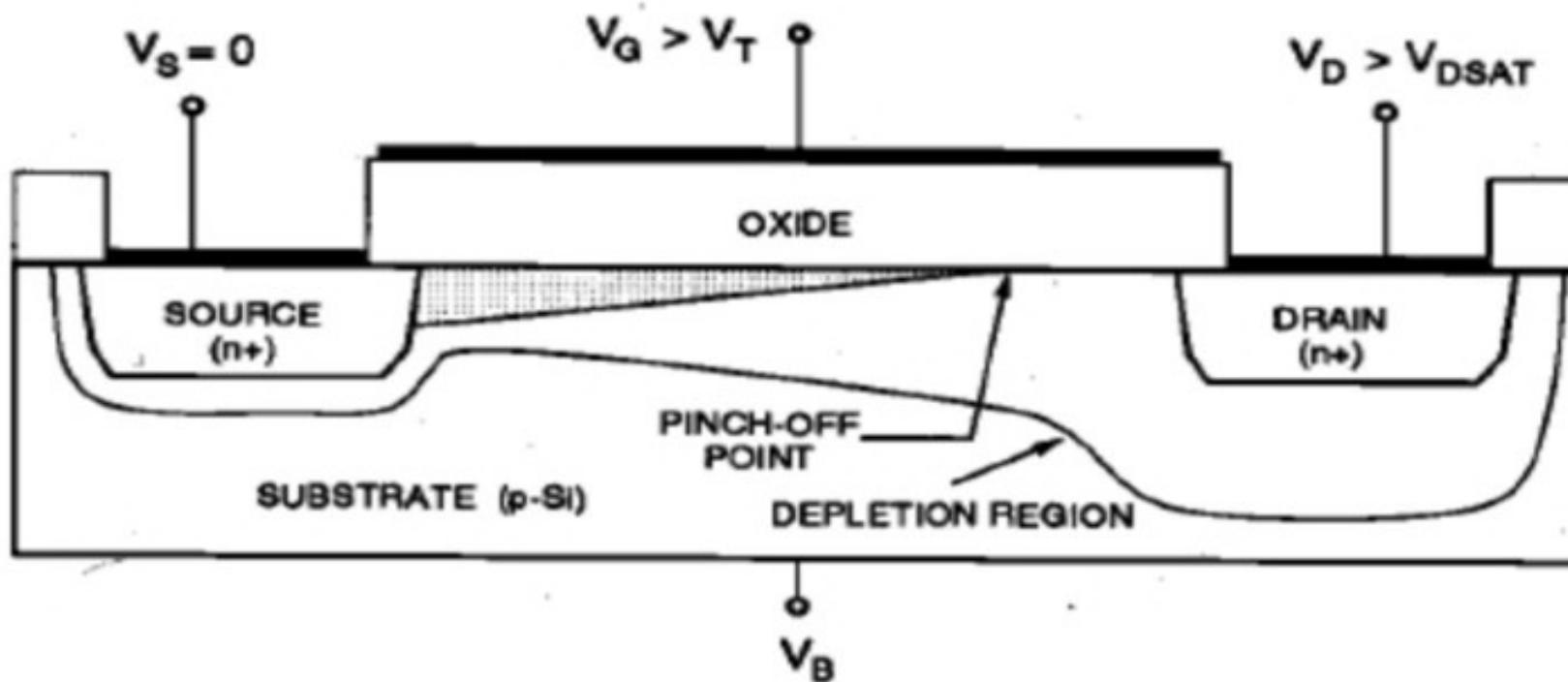
- If the small drain voltage  $V_D$  is applied , a drain current  $I_D$  will flow through the conducting channel.
- The channel forms a continuous path from source to the drain. This mode of operation is called as Linear mode or linear region.
- In this region , the MOSFET is acts as Voltage controlled resistor.

## Case 4 :- If $V_G > V_{th}$ and $V_{DS} = V_{Dsat}$ is applied



- As shown in fig, further increase in  $V_{DS}$  voltage causes a drain end to decreases more.
- Eventually, for  $V_D = V_{Dsat}$ , the channel at the drain side reduces to zero, which is called as Pinch-off point.

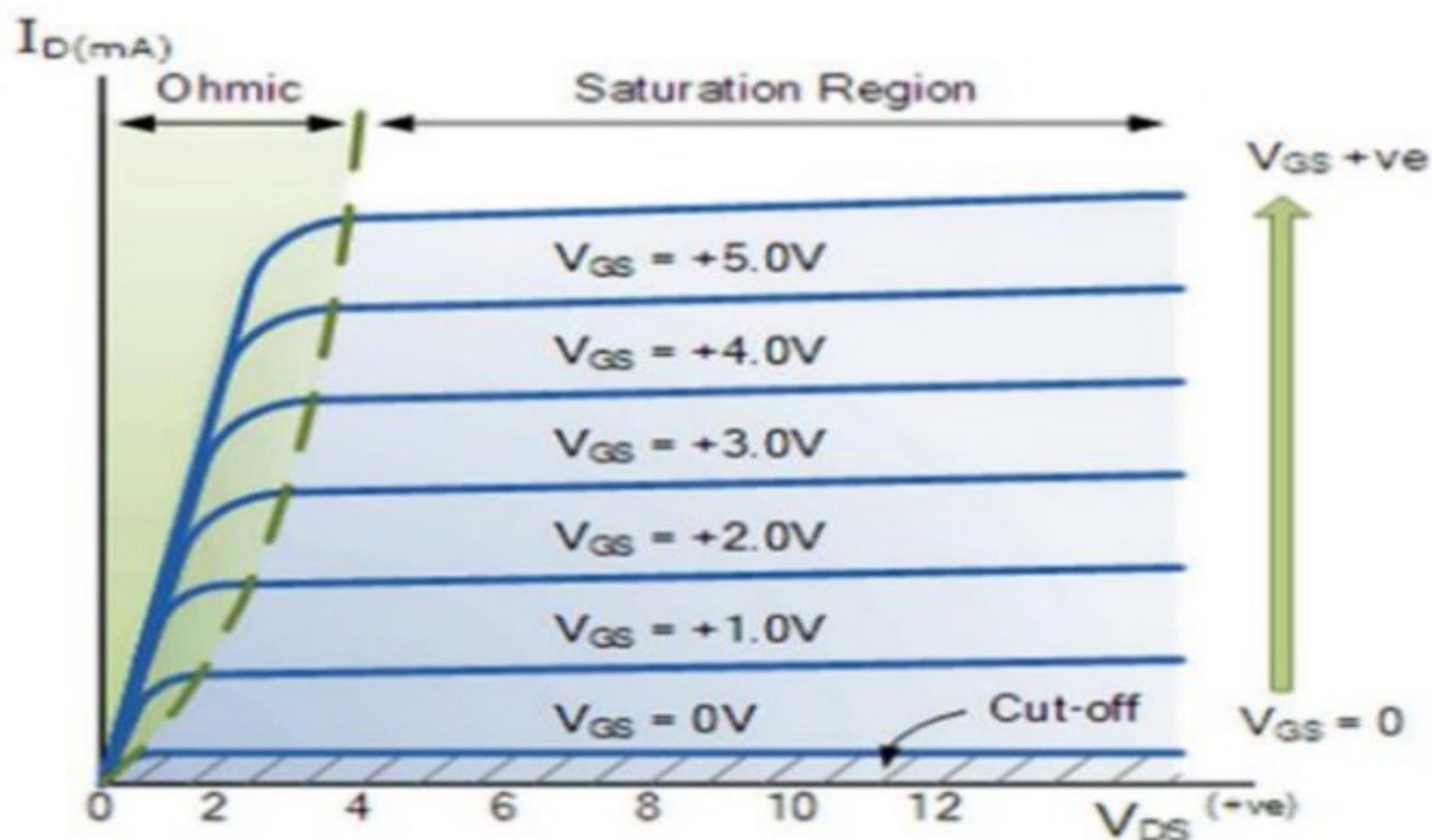
## Case 5 :- If $V_G > V_{th}$ and $V_{DS} > V_{Dsat}$ is applied



- Further increase in  $V_{DS}$  voltage beyond  $V_{Dsat}$  causes further reduction of the channel length due to the increase in the depletion region at the drain side.
- This operation mode of MOSFET is called as **Saturation mode or Saturation region.**

# Output / Drain characteristics of n-channel MOSFET

- It is the curve drawn between  $V_{DS}$  and  $I_D$  by keeping  $V_{GS}$  constant.



### **Ohmic Region :-**

- In this region , drain current ( $I_D$ ) varies with variation in  $V_{DS}$  .
- The **MOSFET** operates as **voltage variable resistance** in this region.
- The drain to source resistance is linear in this region.

### **Pinch off / Saturation Region :-**

- In this region , drain current ( $I_D$ ) remains constant with variation in  $V_{DS}$  .
- At  $V_{DS} = V_P$  , current  $I_D$  is maximum.
- To use **MOSFET** as an **amplifier** it is operated in this region.

### **Cut-off Region :-**

- In this region , drain current ( $I_D$ ) does not flow because there is no channel formation between source and drain for  $V_{GS} < V_{th}$  .

# Current-Voltage equation of n-channel MOSFET

$$I_D = 0, \text{ for } V_{GS} < V_T \quad (1)$$

$$I_D(\text{lin}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \geq V_T \quad (2)$$

and  $V_{DS} < V_{GS} - V_T$

Where  $V_{GS} - V_T = V_{DSAT}$

$$I_D(\text{sat}) = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \quad \text{for } V_{GS} \geq V_T \quad (3)$$

and  $V_{DS} \geq V_{GS} - V_T$

Where  $\mu n C_{ox}$  = Process parameters

W/L = Channel width and length ratio

$$K_n = \frac{\mu_n \cdot C_{ox}}{2} \cdot \frac{W}{L}$$

## Current-Voltage equation of p-channel MOSFET

$$I_D = 0, \text{ for } V_{GS} > V_T \quad (1)$$

$$I_D(\text{lin}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] \quad \text{for } V_{GS} \leq V_T \\ \text{and } V_{DS} > V_{GS} - V_T \quad (2)$$

$$I_D(\text{sat}) = \frac{\mu_p \cdot C_{ox}}{2} \cdot \frac{W}{L} \cdot (V_{GS} - V_T)^2 \cdot (1 + \lambda \cdot V_{DS}) \quad \text{for } V_{GS} \leq V_T \\ \text{and } V_{DS} \leq V_{GS} - V_T \quad (3)$$

# **MOSFET Scaling**



## What is Scaling?

- In order to meet the demand of high density chips in MOS technology, it is required that MOSFET are scaled down ie. Reduction in the size of transistor, so that high packaging density can be achieved.
- Thus, the scaling of MOS transistor is concerned with systematic reduction of overall dimension of the device as allowed by the available technology, while preserving the geometric ratios found in the larger devices.
- We introduce a constant scaling factor  $S > 1$ .
- The scaled device is obtained by dividing all horizontal & vertical dimensions of a large size transistor by this scaling factor.
- It is expected that the operational characteristics of the MOS transistor will change with the reduction of its dimensions.

## Types of scaling

- (1) Constant Field scaling ( Full scaling)
- (2) Constant Voltage scaling

### (1) Constant Field scaling ( Full scaling )

- This scaling technique attempts to preserve the magnitude of internal electric fields in the MOSFET, while dimensions are scaled down by factor of 'S'.
- To achieve this goal , all the potentials must be scaled down proportionally by the same scaling factor.
- Let us analyze the affect of scaling on various parameters.

$$V_T' = \frac{V_T}{S} \quad L' = \frac{L}{S}, \quad W' = \frac{W}{S}$$

$$t_{ox}' = \frac{t_{ox}}{S} \quad C_{ox}' = \frac{C_{ox}}{S} \cdot C_{ox}$$

① Threshold voltage  $V_T' = \frac{V_T}{S}$

② Channel Length & width  $L' = \frac{L}{S}$  &  $W' = \frac{W}{S}$

③ Gate oxide thickness  $t_{ox}' = \frac{t_{ox}}{S}$

④ Gate oxide capacitance per Unit area  $C_{ox}' = \frac{C_{ox}}{t_{ox}} = \frac{C_{ox}}{\left(\frac{t_{ox}}{S}\right)} = S \cdot C_{ox}$

⑤ Junction depth  $x_j' = \frac{x_j}{S}$

⑥ Power supply voltage  $V_{DD}' = \frac{V_{DD}}{S}$

$$\textcircled{7} \quad \text{Doping Densities} \quad N_A' = S \cdot N_A$$

$$\quad \quad \quad \& \quad N_D' = S \cdot N_D$$

$$N_A' = S \cdot N_A$$

$$N_D' = S \cdot N_D$$

$$I_D = \frac{Kn'}{2} [2(V_{GS}' - V_T') V_{DS} - V_{DS}'^2]$$

$$\textcircled{8} \quad \text{Drain Current} \quad I_D'(cm) = \frac{Kn'}{2} [2(V_{GS}' - V_T') V_{DS}' - V_{DS}'^2]$$

$$I_D'(cm) = \frac{SKn}{2} \left[ 2 \left( \frac{V_{GS}}{S} - \frac{V_T}{S} \right) \cdot \frac{V_{DS}}{S} - \frac{V_{DS}^2}{S^2} \right]$$

$$\therefore I_D'(cm) = \frac{I_D(cm)}{S}$$

$$I_D'(sat) = \frac{Kn'}{2} (V_{GS}' - V_T')^2$$

$$= \frac{S \cdot Kn}{2} \left[ \frac{V_{GS}}{S} - \frac{V_T}{S} \right]^2$$

$$\textcircled{9} \quad I_D'(sat) = \frac{Kn'}{2} (V_{GS}' - V_T')^2 = \frac{S \cdot Kn}{2} \left[ \frac{V_{GS}}{S} - \frac{V_T}{S} \right]^2$$

$$I_D'(sat) = \frac{I_D(sat)}{S}$$

$$\textcircled{10} \quad \text{Power Dissipation} \quad p' = I_D' \cdot V_{DS}$$

$$= \frac{I_D}{S} \cdot \frac{V_{DS}}{S} = \frac{1}{S^2} I_D V_{DS}$$

$$\therefore p' = \frac{p}{S^2}$$

$$\textcircled{11} \quad \text{Power density} = \text{Power / Area} = \frac{p'}{A'} = \frac{p/S^2}{A/S^2}$$

$$\therefore \text{Power density} = \frac{p}{A} \quad (\text{i.e. } \underline{\underline{\text{same}}})$$

$\frac{p}{A} = \text{Same}$

## Disadvantages

- As in this technique, power supply voltage and all terminal voltages are scaled down proportionally with the device dimensions, but the scaling of voltages may not be very practical in many cases.
- In particular, the peripheral and interface circuitry may require certain voltage levels for all i/p and o/p voltages , which in turn would necessitate multiple power supply voltages and complicated level shifter arrangements.
- Hence for this reason constant Voltage scaling is preferred over the constant field scaling.

peripheral & interface circuitry levels  
for all i/p & o/p → necessitate  
multiple power supply

const. volt.  
scaling is pref  
over const

## (2) Constant Voltage scaling

power supply &  
terminal voltages  
remain unchanged

- In this scaling technique, all dimensions of MOSFET are reduced by factor of 'S', but power supply and terminal voltages remain unchanged.
- The doping densities must be increased by factor of  $S^2$  in order to preserve the charge field relations.

- Threshold voltage  $V_T'$  remain unchanged  $= V_T$   
 $V_T' = V_T$   
 $L' = \frac{L}{S}$   
 $w' = \frac{w}{S}$
- channel length & width  $L' = \frac{L}{S}$  &  $w' = \frac{w}{S}$   
 $L_{ox}' = \frac{L_{ox}}{S}$   
 $L_{ox} = S \cdot L_{ox}'$   
 $w_{ox}' = \frac{w_{ox}}{S}$   
 $w_{ox} = S \cdot w_{ox}'$
- gate oxide thickness  $t_{ox}' = \frac{t_{ox}}{S}$
- Gate oxide capacitance / Unit Area  $C_{ox}' = S \cdot C_{ox}$
- Junction depth  $x_j' = \frac{x_j}{S}$

⑥ Power supply voltage  $V_{DD}$  remains unchanged  $= V_{DD}$

⑦ Doping densities  $N_A' = S^2 \cdot N_A$  &  $N_D' = S^2 \cdot N_D$

⑧ Drain current  $I_D'(lm) = \frac{Kn'}{2} [2 \cdot (V_{GS}' - V_T') V_{DS} - V_{DS}^2]$   
 $= \frac{SKn}{2} [2 \cdot (V_{GS} - V_T) V_{DS} - V_{DS}^2] = S \cdot I_D(lm)$

⑨  $I_D'(sat) = \frac{Kn'}{2} (V_{GS}' - V_T')^2 = \frac{SKn}{2} (V_{GS} - V_T)^2$   
 $= S I_D(sat)$

⑩ Power Dissipation  $P' = I_D' \cdot V_{DS}$   
 $= (S I_D) \cdot V_{DS} = S \cdot P$

⑪ Power density = Power / Area  $= \frac{P'}{A_l} = \frac{S \cdot P}{A_l / S^2} = S^3 \left( \frac{P}{\text{Area}} \right)$

## Disadvantages

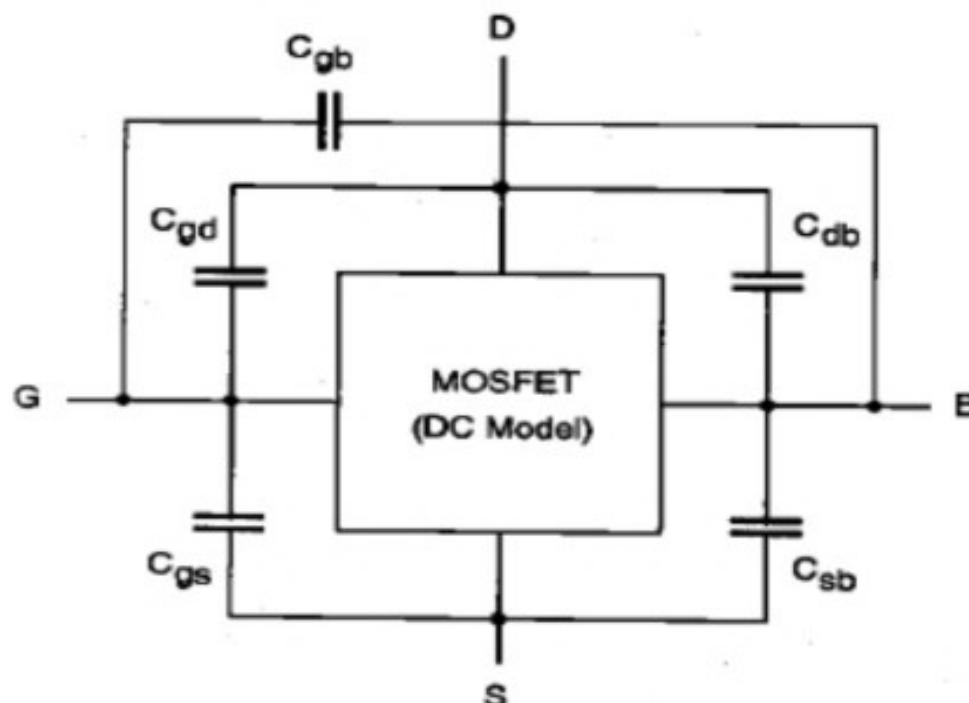
drain current density increase.  
power density increase  
→ serious reliability

- In this technique, Drain current density and Power density are increases which may eventually causes the serious reliability problem for scaled transistor such as electromigration, hot carrier degradation, oxide breakdown and electrical over stress.

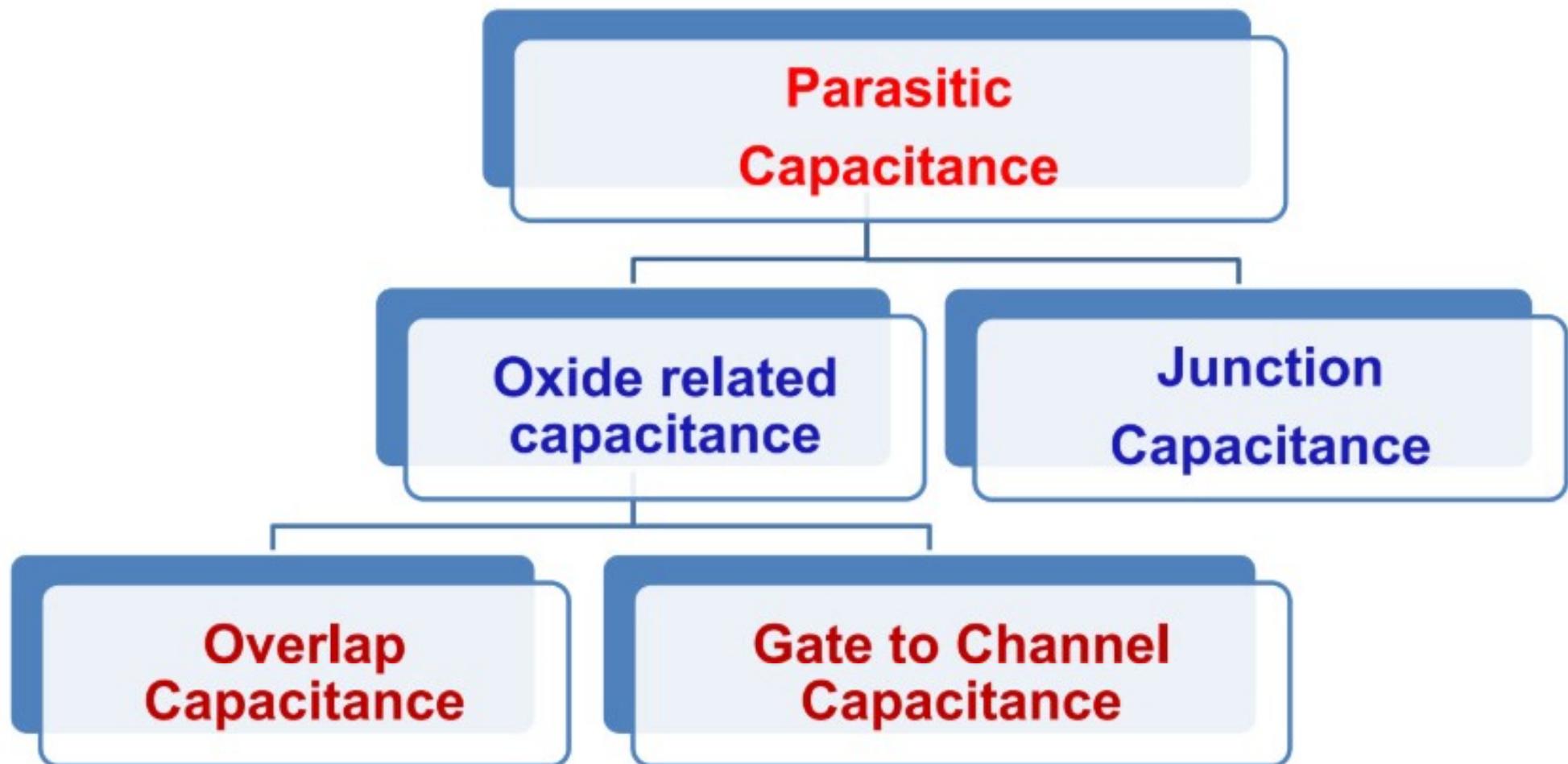
Parameters	Constant field scaling	Constant voltage scaling
Threshold voltage ( $V_T$ )	$V_T / S$	$V_T$
Channel Length ( L )	$L/S$	$L/S$
Channel Width ( W )	$W/S$	$W/S$
Gate oxide thickness ( $t_{ox}$ )	$t_{ox} / S$	$t_{ox} / S$
Oxide capacitance ( $C_{ox}$ )	$S C_{ox}$	$S C_{ox}$
Junction Depth ( $X_j$ )	$X_j / S$	$X_j / S$
Power supply voltage ( $V_{dd}$ )	$V_{dd} / S$	$V_{dd}$
Doping densities	$S N_A$ and $S N_D$	$S^2 N_A$ and $S^2 N_D$
Drain current ( $I_D$ )	$I_D / S$	$S I_D$
Power dissipation	$P / S^2$	$S P$
Power density	$P / A$	$S^3(P / A)$

## MOSFET Capacitance

- In order to examine the transient ( AC) response of MOSFET, it is necessary to determine the nature and amount of parasitic capacitance associated with the MOS transistor.
- Following fig. shows lumped representation of the parasitic MOSFET capacitance.



➤ Based on the physical origins, parasitic device capacitance can be classified into ,



## Overlap Capacitance

- As the gate electrode overlaps both the Source and Drain regions at the edges , this results in the overlap capacitance called as  $C_{GS\text{ (overlap)}}$  &  $C_{GD\text{ (overlap)}}$  and can be given as,

$$C_{GS\text{ (overlap)}} = C_{OX} \cdot W \cdot L_D$$
$$C_{GD\text{ (overlap)}} = C_{OX} \cdot W \cdot L_D$$

where  $C_{OX} = \epsilon_{ox} / t_{ox}$

Both these overlap capacitances are voltage – independent  
(ie Do not depend upon the bias conditions)

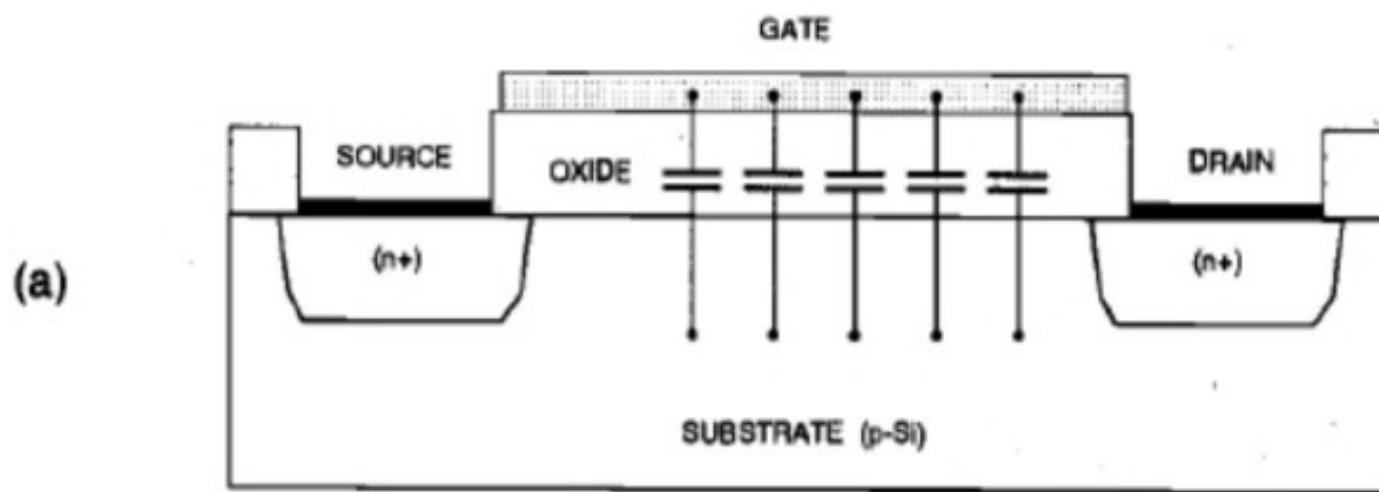
## Gate to Channel Capacitance

- These capacitance results from the interaction between the gate voltage and channel charge.
- These capacitances are distributed and voltage dependent.
- Since, the channel region is connected to the Source, Drain and Substrate thus these capacitances between the Gate and these regions are  $C_{gs}$ ,  $C_{gd}$  &  $C_{gb}$  respectively.
- As the MOSFET is operating in the different regions , these capacitance values are different.

## Case I :- During cut-off condition

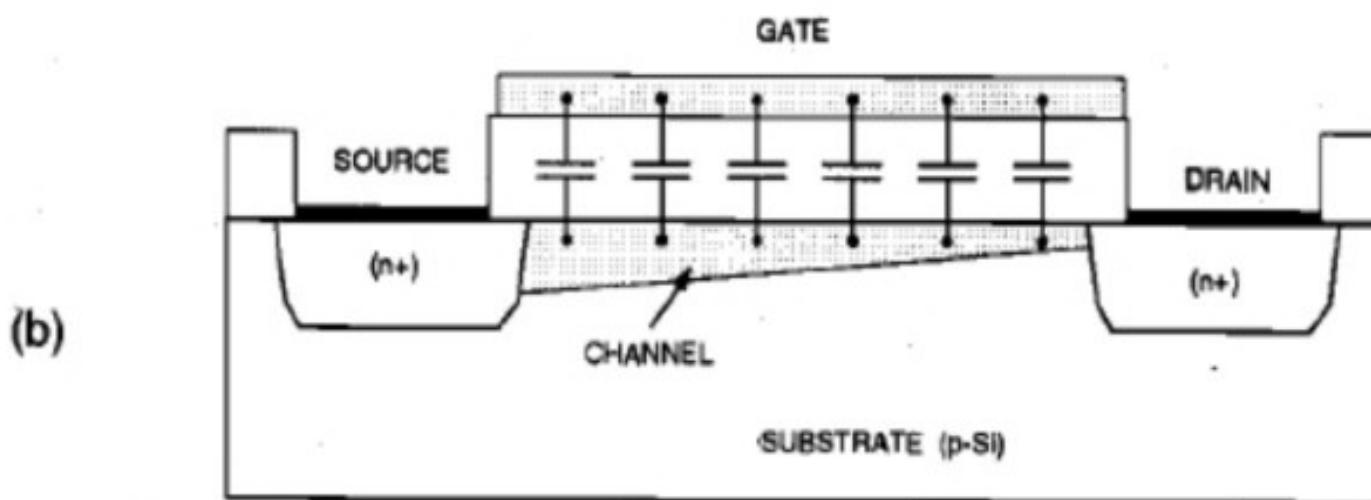
- In this condition, surface is not inverted and there is no conduction channel that links to Source and Drain.
- Gate to Source capacitance  $C_{gs} = 0$  and also
- Gate to Drain capacitance  $C_{gd} = 0$
- But only capacitance between Gate and Substrate is present.

$$C_{gb} = C_{ox} \cdot W \cdot L$$



## Case II :- During Liner mode condition

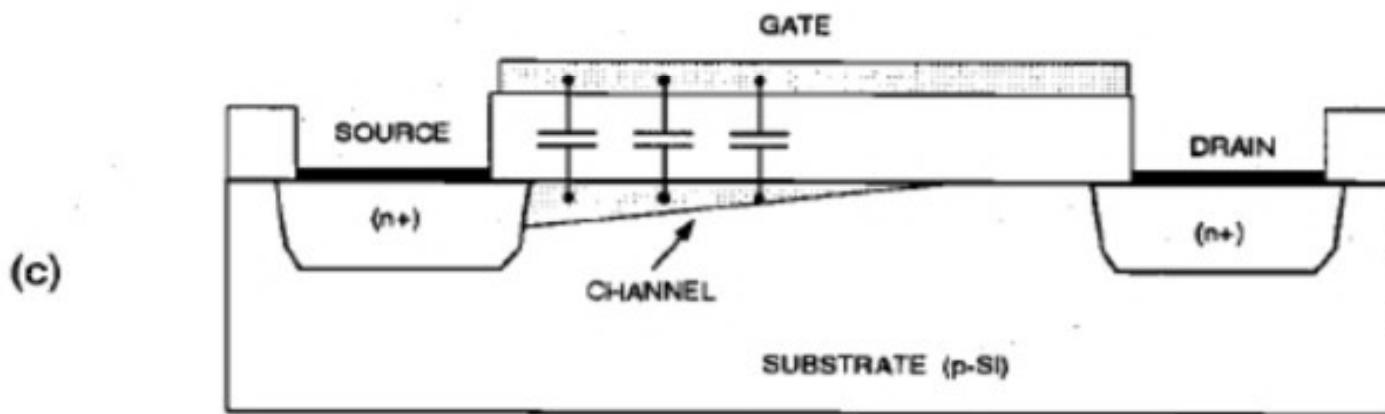
- In this condition, an inverted channel is present between the Source and Drain.
- In this case, the distributed gate to channel capacitance is shared equally between Source and Drain. ( looks like parallel)  
$$C_{gs} = C_{gd} = \frac{1}{2} C_{ox} \cdot W \cdot L$$
- But, as the conducting inversion layer on the surface effectively shields the substrate from the gate electric field thus,  $C_{gb} = 0$  as shown in diagram,



### Case III :- During Saturation mode condition

- In this condition, the inversion layer on the surface does not extend to the drain , but it is pinched off as shown in fig.
- Thus, Gate to Drain capacitance is zero ,  $C_{gd} = 0$
- Since, the source is still linked to the conducting channel, its shielding effect also forces  $C_{gb} = 0$
- So distributed gate channel capacitance is seen between the Gate and Source & can be approximated by,

$$C_{gs} = \frac{2}{3} C_{ox} \cdot W \cdot L$$

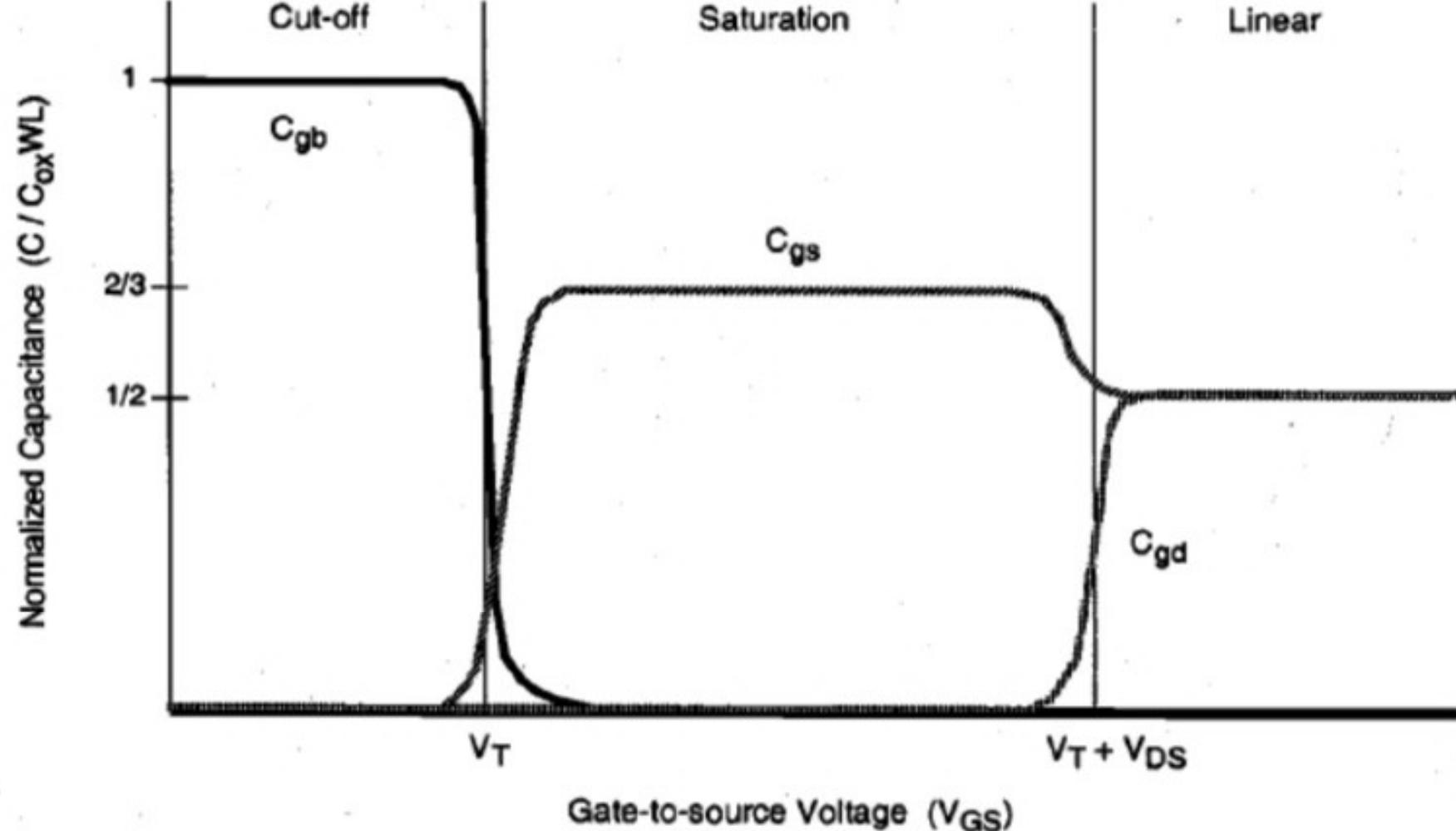


- Thus, in order to calculate the total capacitance between the external device terminals,
- **Total capacitance = Overlap capacitance + Gate to channel capacitance**

Total cap = overlap cap + Gate to channel cap.

Capacitance	Cut-off	Linear	Saturation
$C_{gb}$ (total)	$C_{ox}WL$	0	0
$C_{gd}$ (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$C_{ox}WL_D$
$C_{gs}$ (total)	$C_{ox}WL_D$	$\frac{1}{2}C_{ox}WL + C_{ox}WL_D$	$\frac{2}{3}C_{ox}WL + C_{ox}WL_D$

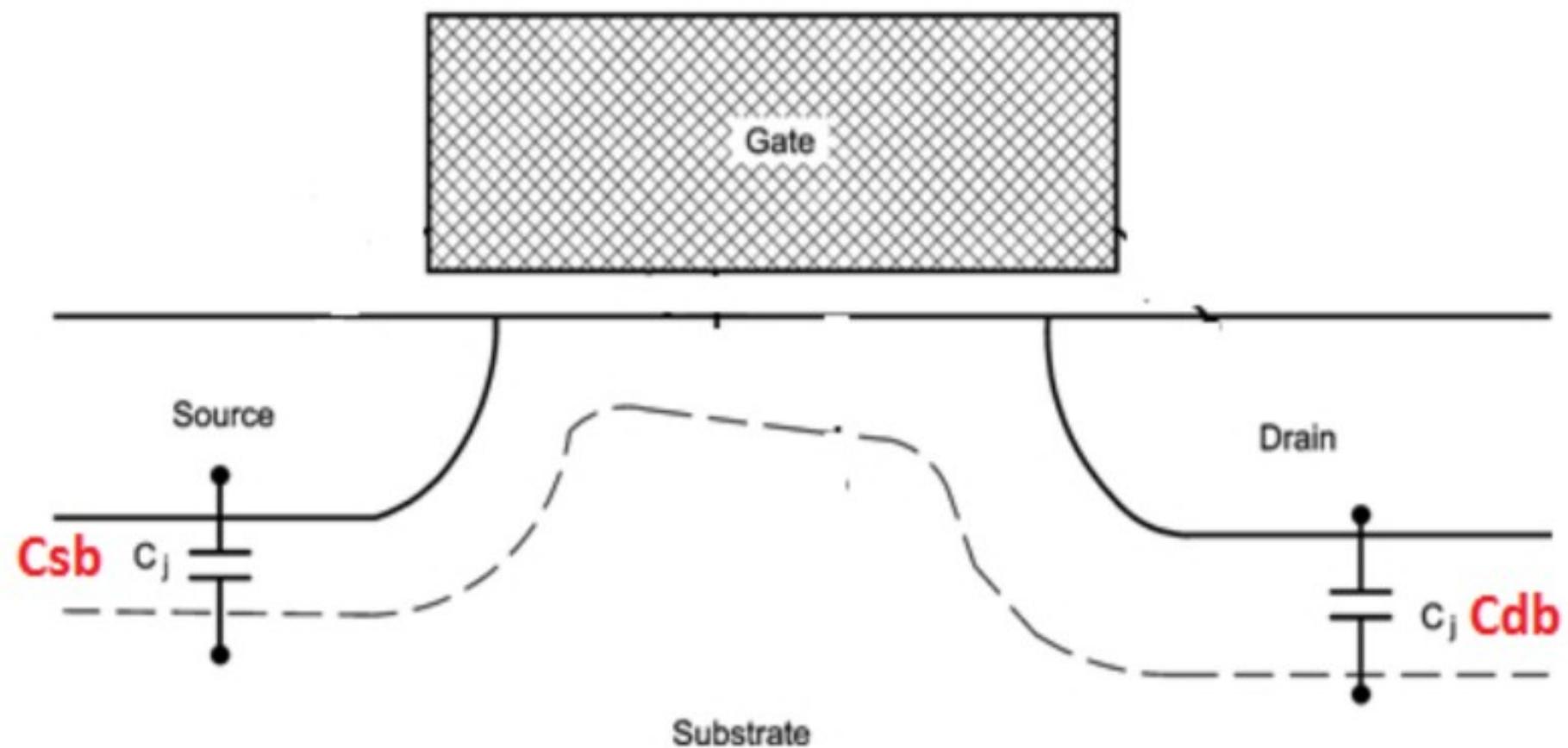
➤ Following fig shows the variation of the distributed ( Gate to channel) oxide capacitance as a function of Gate to Source voltage ( $V_{GS}$ )



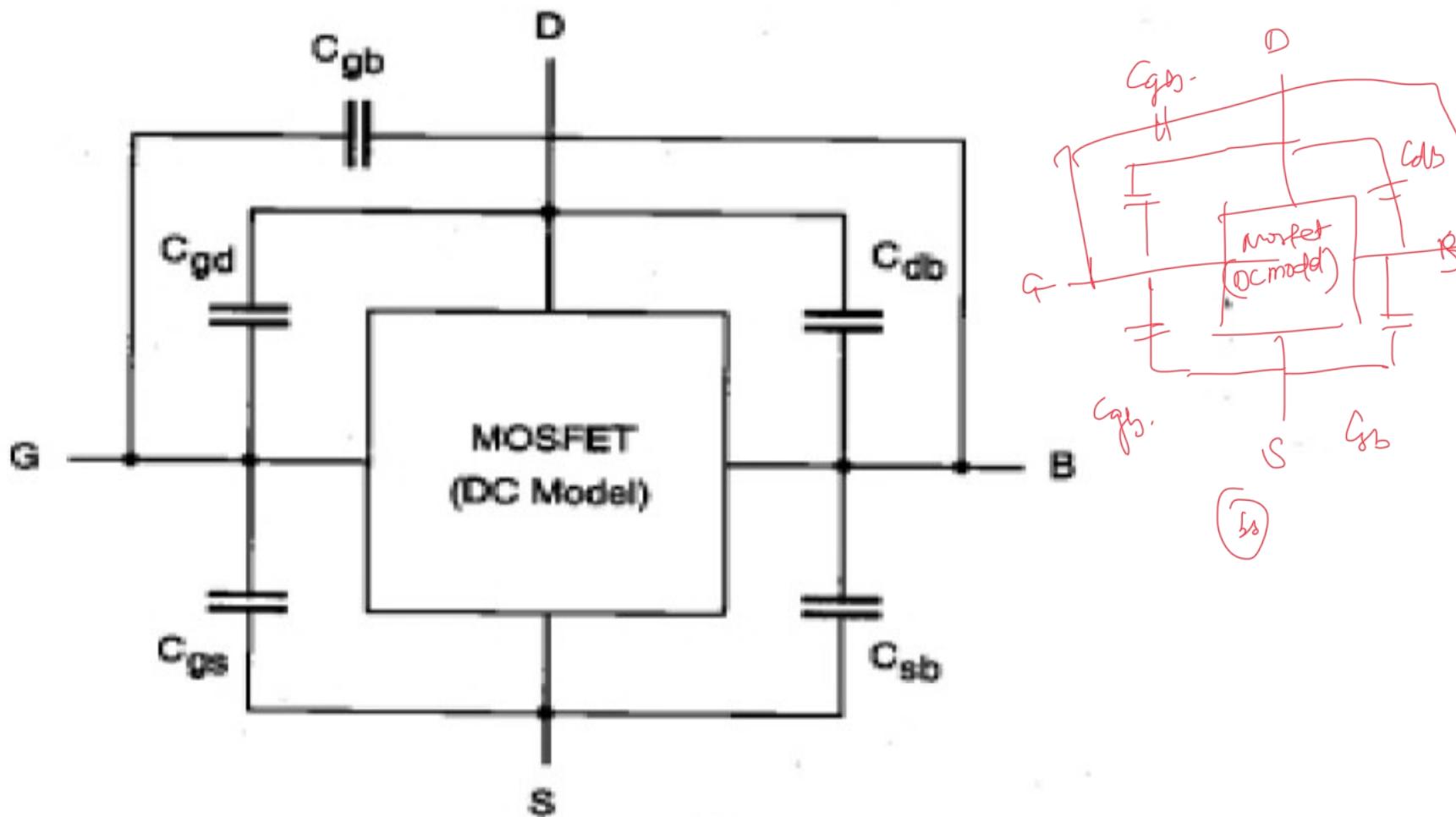
$C_{sb}$     $C_{ds}$

## (2) Junction Capacitance

- These are Voltage-dependent capacitances, namely source to substrate ( $C_{sb}$ ) & drain to substrate ( $C_{ds}$ )
- Both of these capacitances are due to the depletion charge surrounding the respective source and drain diffusion regions embedded in the substrate.
- Both of these junctions are reverse biased under the normal operating conditions & amount of junction capacitance is function of applied terminal voltages.
- It is given by,

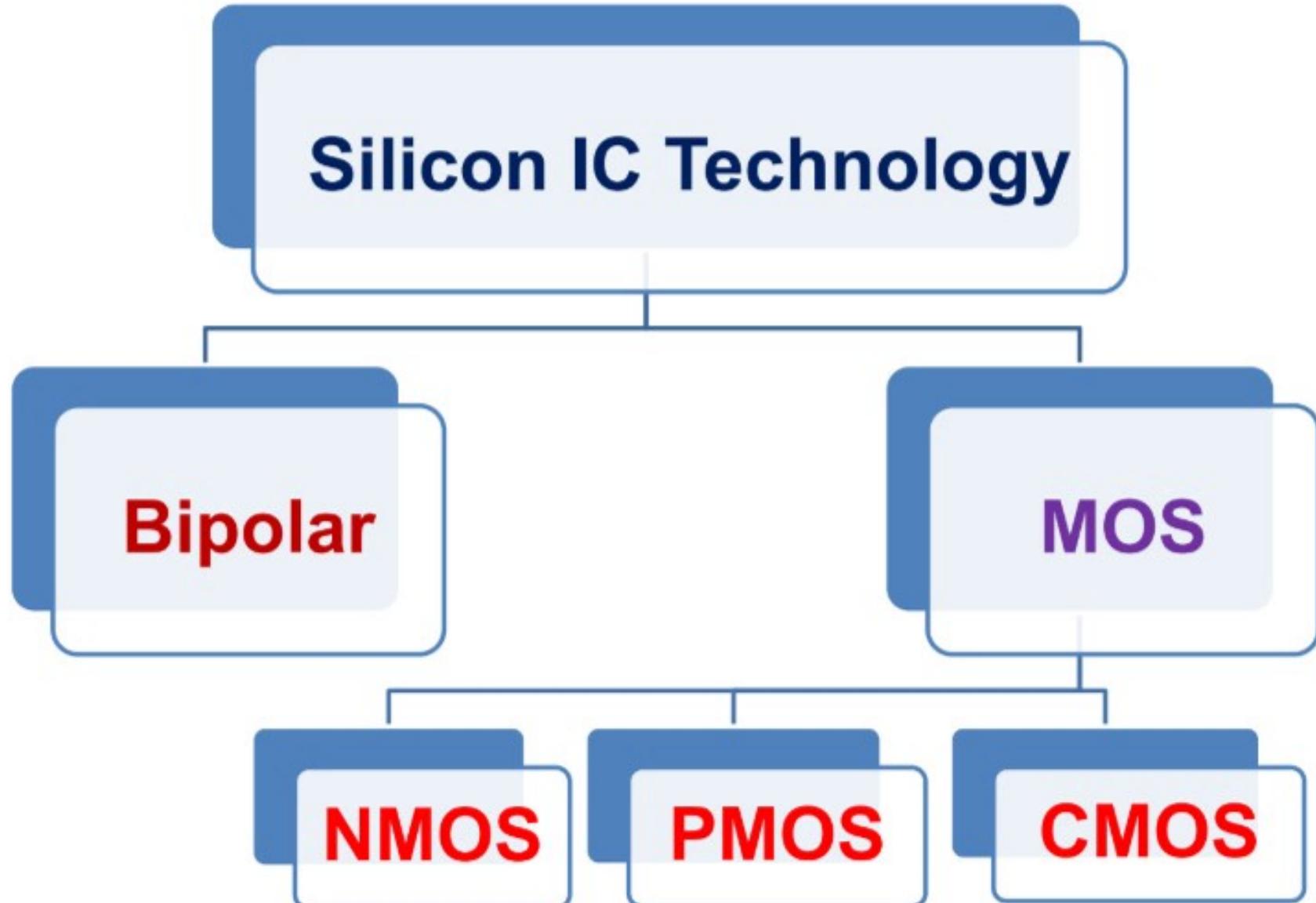


# Lumped representation of parasitic MOSFET Capacitance



# **1.3 Technology Comparison**

# Technology Trend



# Comparison between technology trends

IPNSD  
2022

BJT Technology	MOS Technology
Low Input Impedance	High Input Impedance
High Power Dissipation	Low Power Dissipation
Low Noise Margin	High Noise Margin
Limitations in Scaling	Can be scaled down easily
Low packaging Density	High packaging Density

Thank  
you!

