

Module 3

MOS Circuit Design Styles

3.1 Static: Static CMOS, Pass transistor, Transmission gate, Pseudo NMOS design styles.

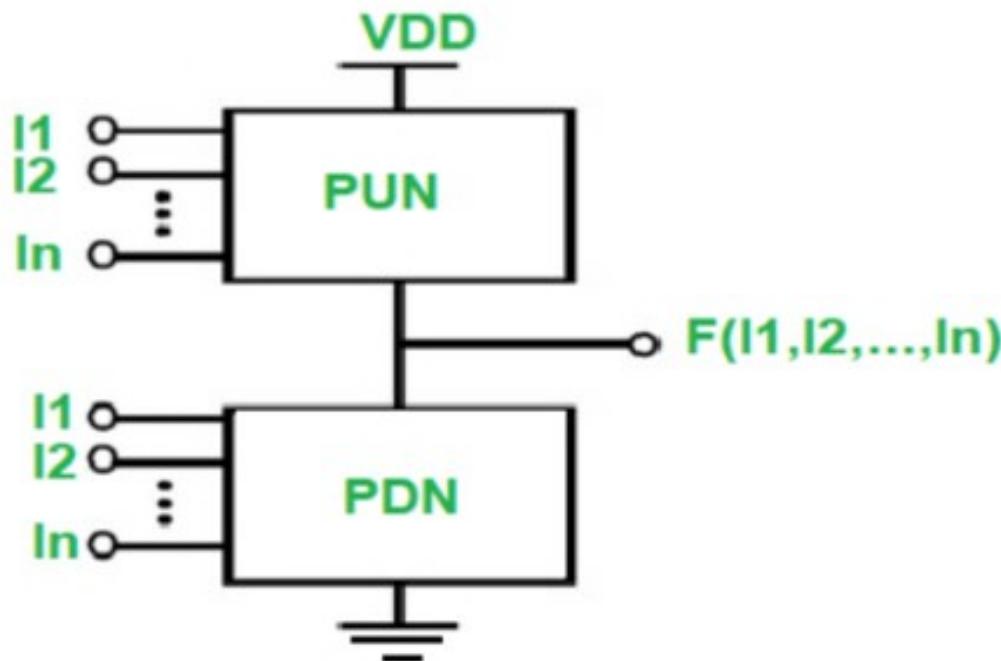
3.2 Dynamic: C²MOS, Dynamic, Domino, NORA and Zipper design styles.

3.3 Complex Boolean function realization using various design styles

3.1 Static CMOS Design

What is Static Design ?

- It implies that, except during a switching time, each gate output is connected to either V_{DD} or V_{SS} via Low resistance path.
- It consists of two networks , Pull-up (PUN) and Pull-down (PDN).
- PDN consists of N-MOS and produces strong Zero while PUN consists of P-MOS and produces strong One.



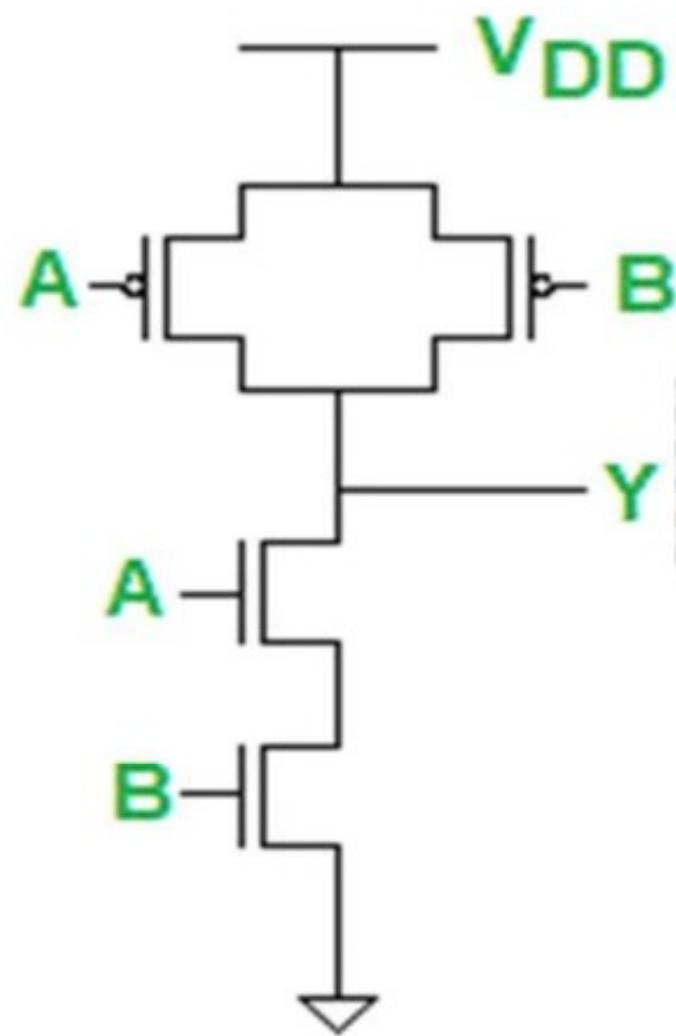
Rules of constricting PUN and PDN

- PDN is constructed by N-MOS and PUN is by P-MOS.
- N-MOS switches are closed when logic 1 is applied and P-MOS switches are closed when logic 0 is applied.
- Series connection of switches corresponds to AND & Parallel connection corresponds to OR operation.
- PUN & PDN are Dual of each other (ie. Series connection in PDN corresponds to parallel connection in PUN).
- Always built Driver circuit (ie PDN) first and then load network (ie. PUN). [which is the compliment of PDN]
- The given function should always be in complement form

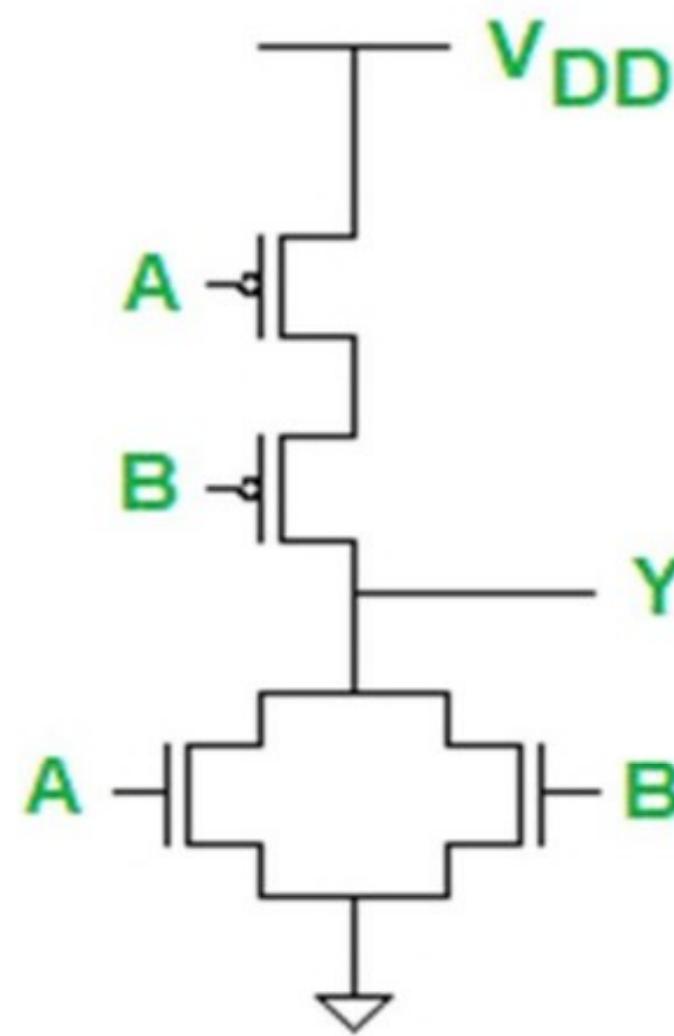
given for should always be
in complement form

CMOS NAND & NOR gate

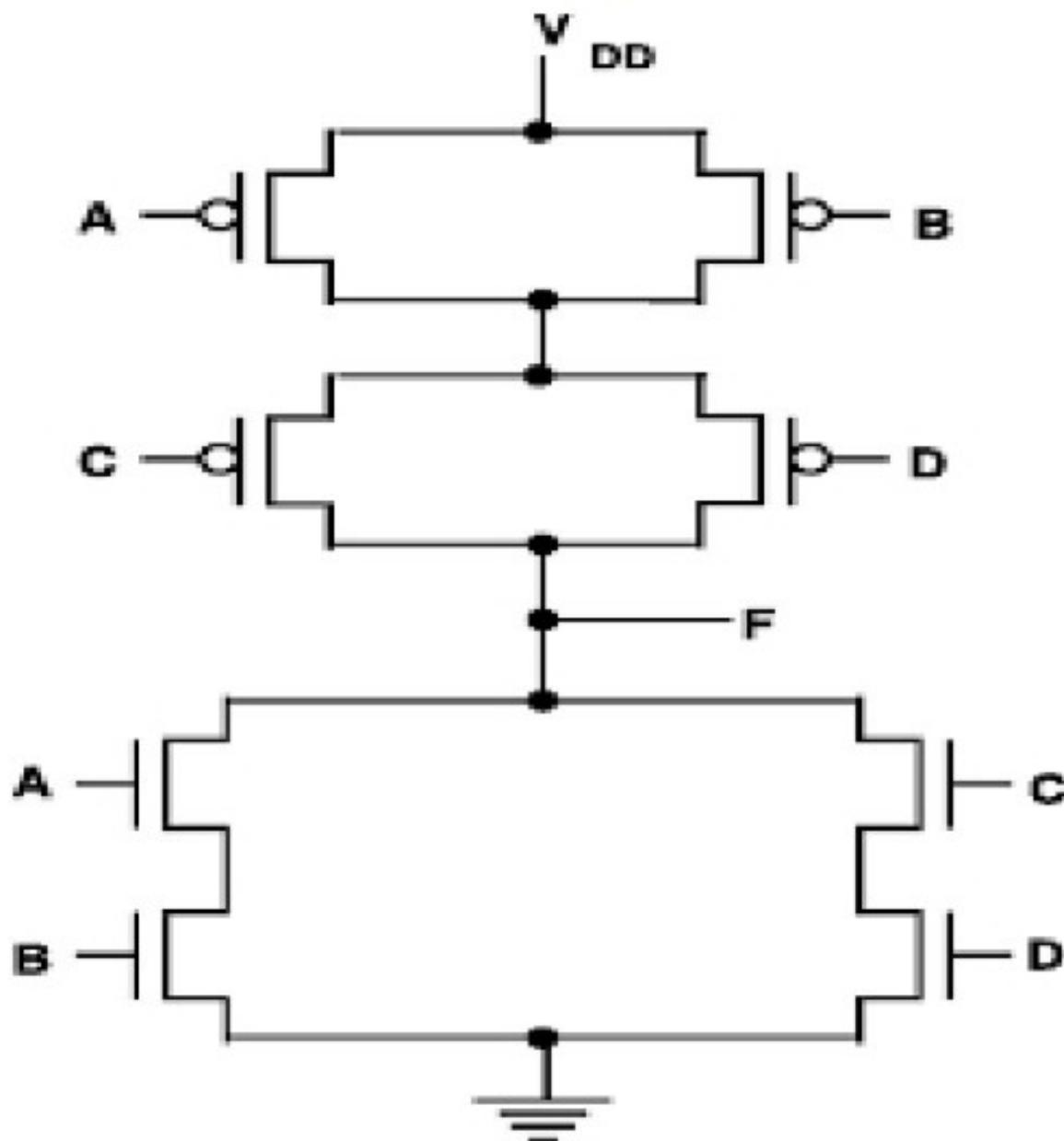
$$Y = \overline{A \cdot B}$$



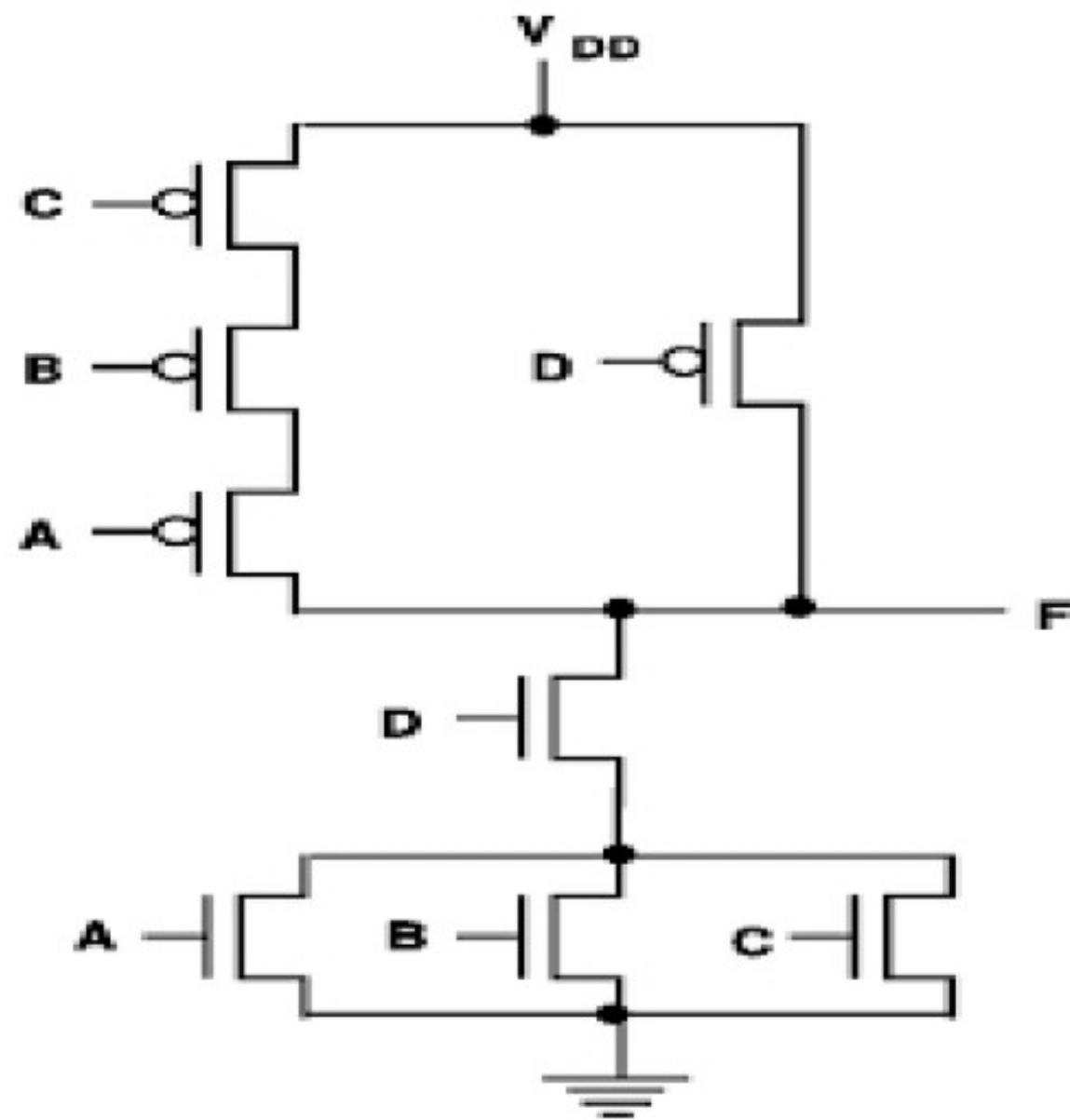
$$Y = \overline{A+B}$$



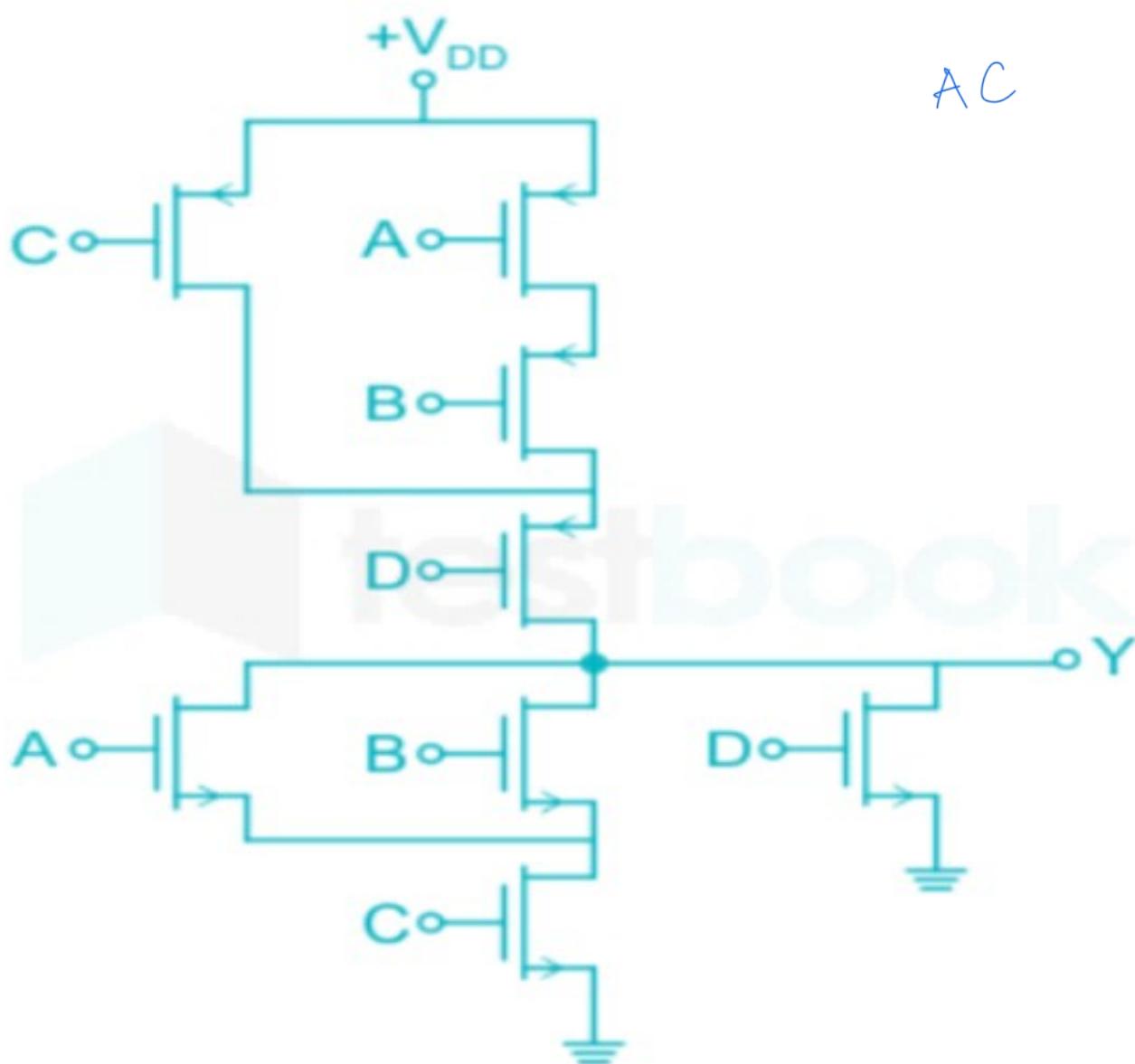
Q.1 Construct $F = \overline{AB} + \overline{CD}$ using Static CMOS design style



Q.2 Construct $F = \overline{(A+B+C)} \cdot D$ using Static CMOS design style



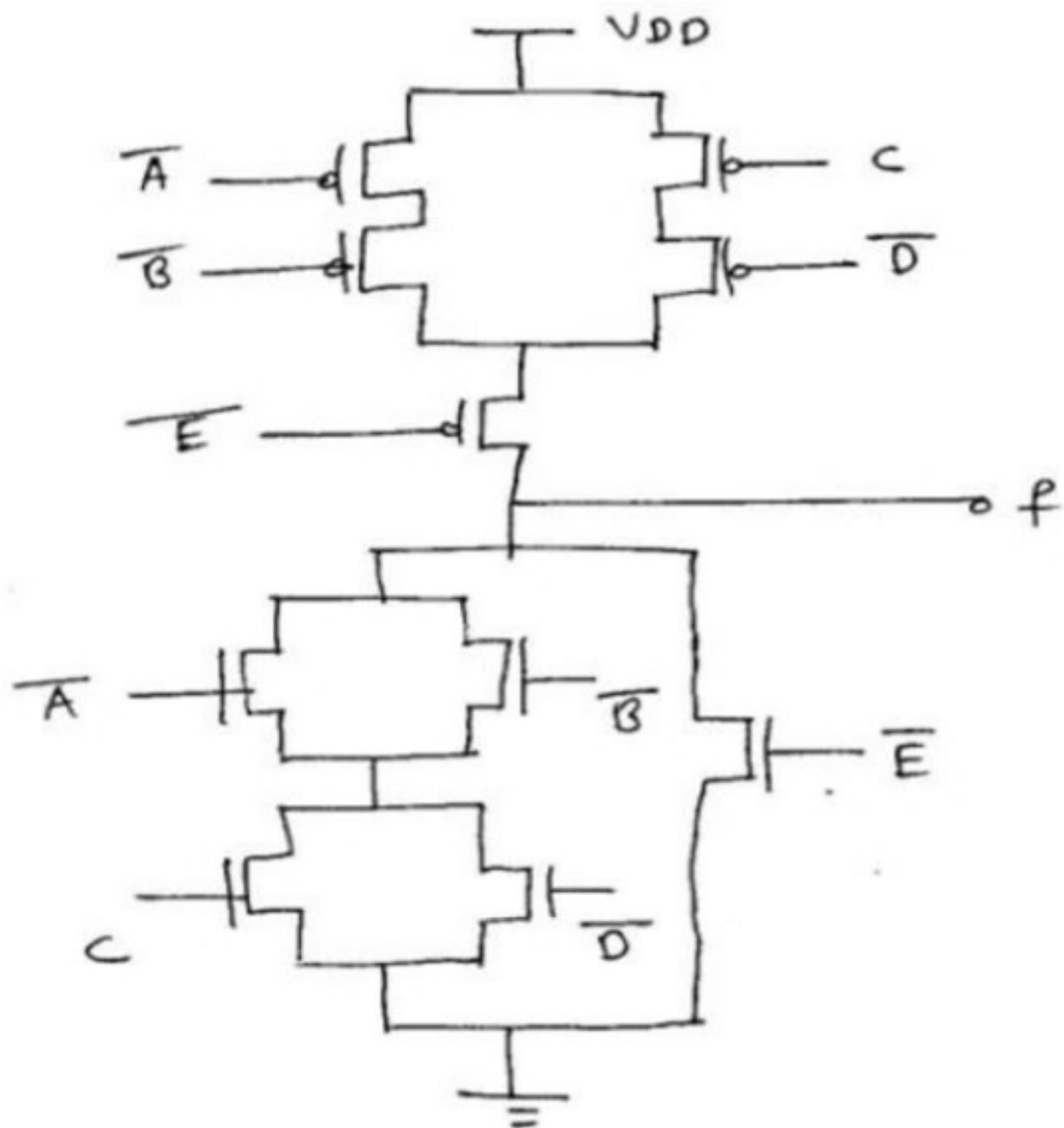
Q.3 Construct $F = \overline{(A+B)}C + D$ using Static CMOS design style



Q.4 Construct $F = (AB + \overline{CD})E$ using Static CMOS design style

The given function is not in complement form, hence take double inversion of it,

$$\begin{aligned}\overline{\overline{f}} &= \overline{(AB + \overline{CD}) \cdot E} \\ &= \overline{(AB + \overline{CD})} + \overline{E} \\ &= \overline{(AB)}(\overline{\overline{CD}}) + \overline{E} \\ &= (\overline{A} + \overline{B})(C + \overline{D}) + \overline{E}\end{aligned}$$



Q.5 Construct 2:1 MUX using static CMOS logic

2: 2

Boolean function of 2:1 mux is,

$$y = \overline{S} D_0 + S D_1$$

$$y = \overline{S} D_0$$

→ Take Complement on both sides

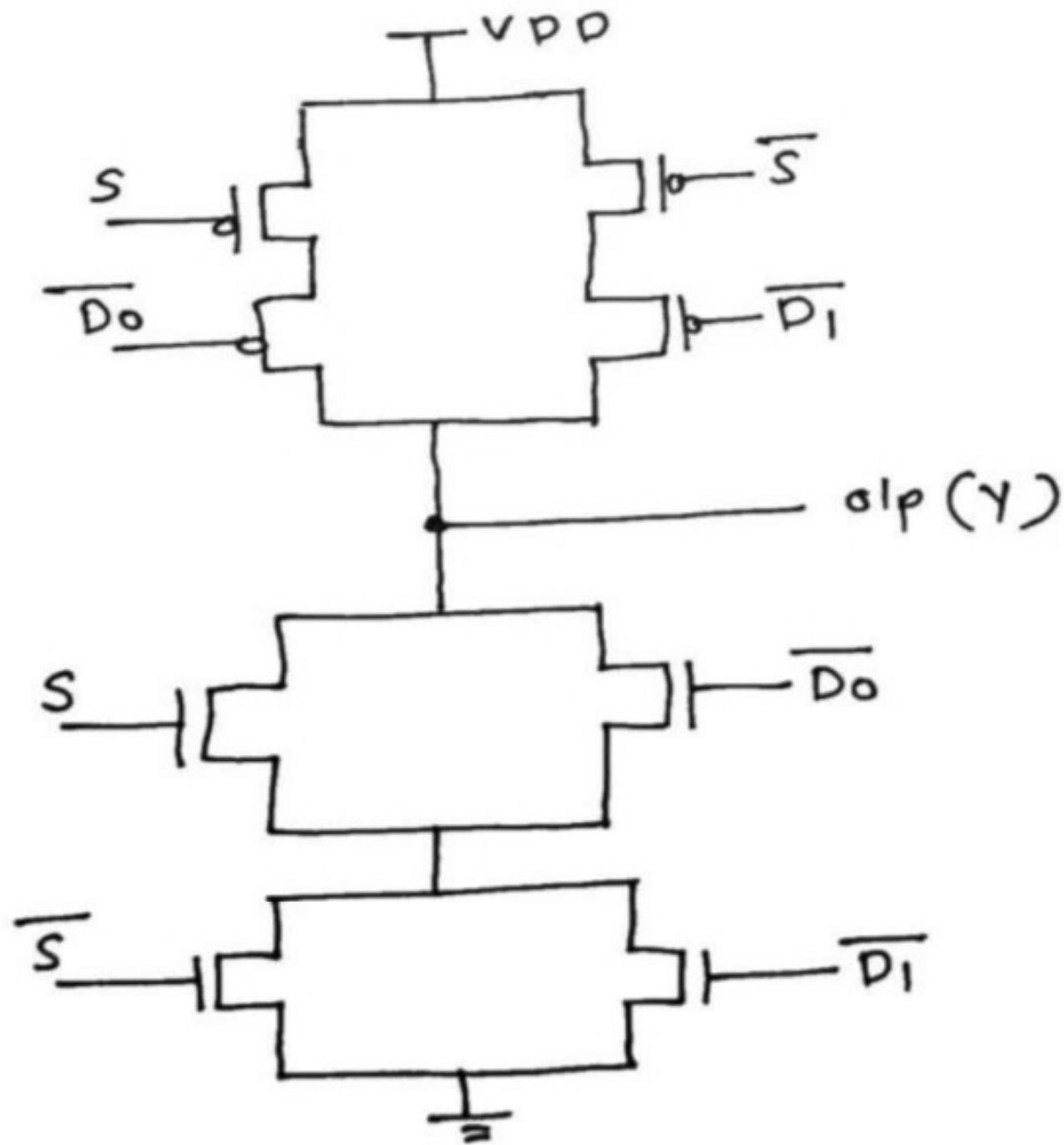
$$\overline{y} = \overline{(\overline{S} D_0) + (S D_1)}$$

$$(\overline{S} + \overline{D}_0) \cdot (\overline{S} + \overline{D}_1)$$

$$= \overline{(\overline{S} D_0) \cdot (\overline{S} D_1)}$$

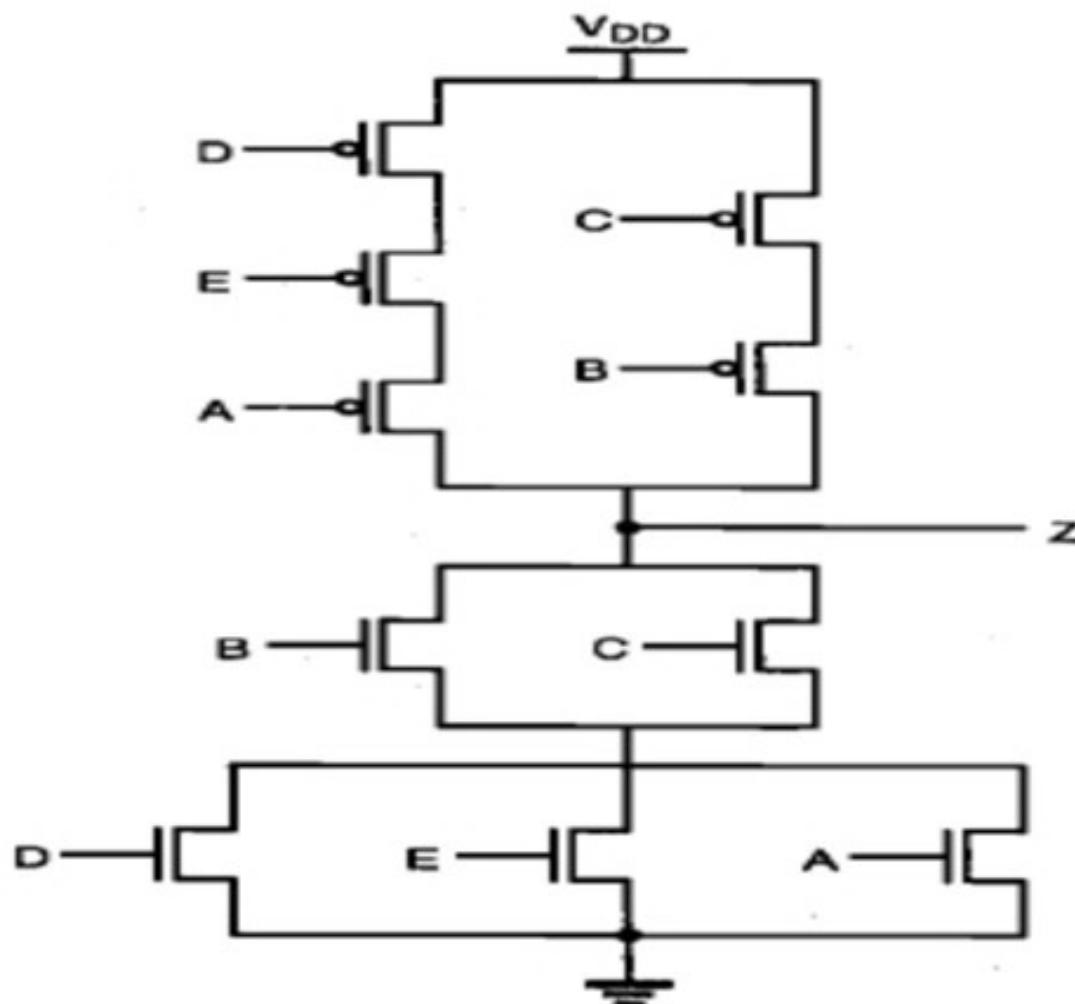
$$= \overline{(\overline{S} + \overline{D}_0) \cdot (\overline{S} + \overline{D}_1)}$$

$$y = \overline{(S + \overline{D}_0) \cdot (S + \overline{D}_1)}$$



Q.5 Draw an equivalent CMOS inverter circuit for the following static CMOS logic. Assume $(W/L) = 15$ for all PMOS and $(W/L) = 10$ for all NMOS for the expression given below.

$$Z = \overline{(D+E+A)(B+C)}$$



For Series connected MOSFETs

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \dots$$

$$\frac{1}{\left(\frac{W}{L}\right)_{eq}} = \frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} + \dots$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_1} + \frac{1}{\left(\frac{W}{L}\right)_2} + \dots}$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\sum_1^K \frac{1}{\left(\frac{W}{L}\right)}}$$

For unequal (W/L) ratio

$$\left(\frac{W}{L}\right)_{eq} = \frac{W}{nL}$$

For equal (W/L) ratio

For Parallel connected MOSFETs

$$C_{eq} = C_1 + C_2$$

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_1 + \left(\frac{W}{L}\right)_2 + \dots$$

$$\left(\frac{W}{L}\right)_{eq} = \sum_1^K \left(\frac{W}{L}\right)$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{nW}{L}$$

Driver n-MOSFETs (A,E,D) with same (W/L) ratio ie . 10 are connected in parallel,

$$\left(\frac{W}{L}\right)_{eq} = \frac{nW}{L}$$

$$\left(\frac{W}{L}\right)_{eq} = 3 \times 10 = 30$$

Similarly, Driver n-MOSFETs (B,C) with same (W/L) ratio ie . 10 are connected in parallel,

$$\left(\frac{W}{L}\right)_{eq} = 2 \times 10 = 20$$

Load p-MOSFETs (A,E,D) with same (W/L) ratio ie . 15 are connected in series,

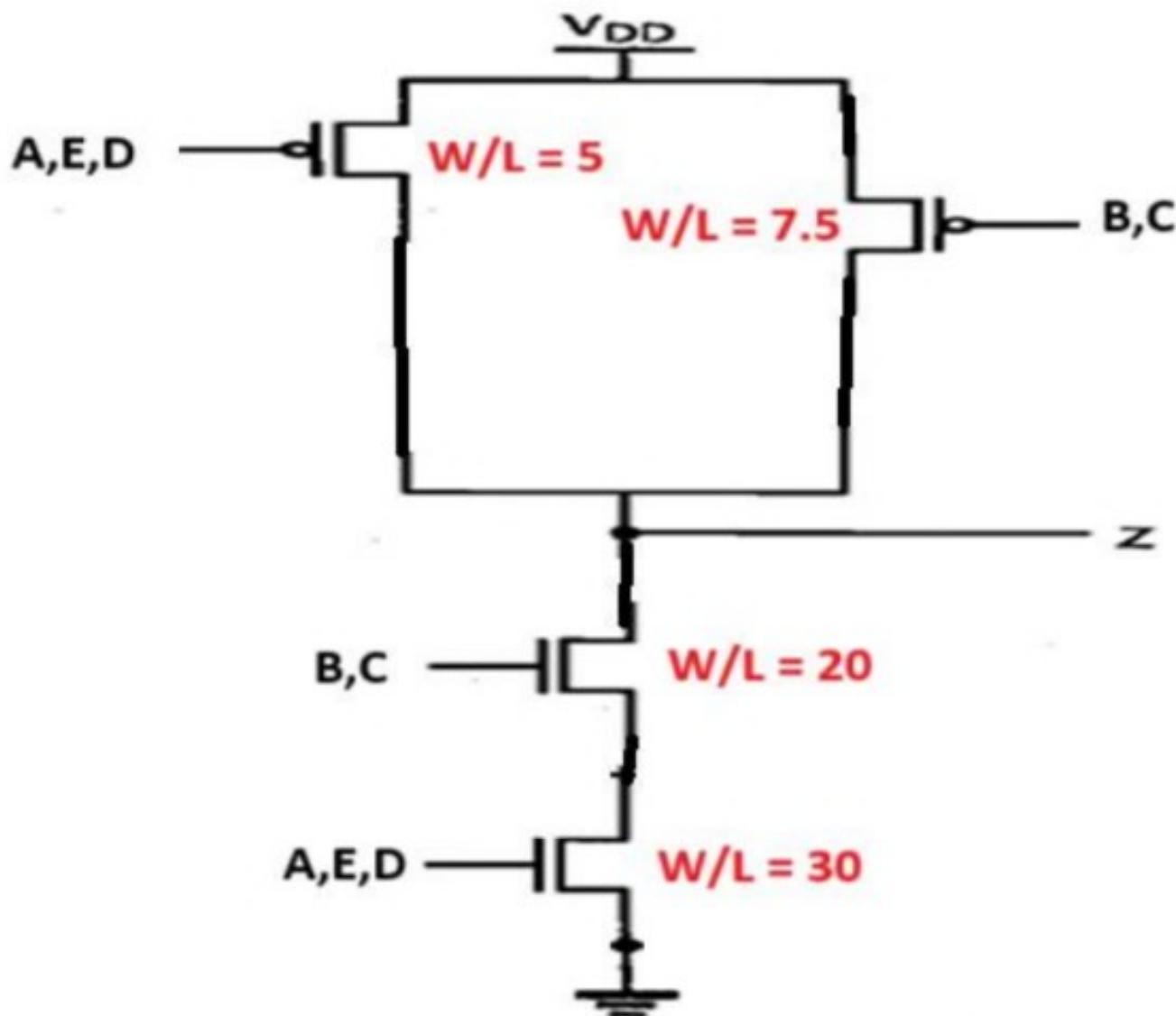
$$\left(\frac{W}{L}\right)_{eq} = \frac{W}{nL}$$

$$\left(\frac{W}{L}\right)_{A,E,D} = \frac{15}{3} = 5$$

Similarly, Load p-MOSFETs (B,C) with same (W/L) ratio ie . 15 are connected in series,

$$\left(\frac{W}{L}\right)_{B,C} = \frac{15}{2} = 7.5$$

The new schematic with this (W/L) ratio is given below,



Now, Driver n-MOSFETs (A,E,D) and (B,C) with different (W/L) ratio ie . 30 & 20 respectively are connected in series,

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\sum_1^K \frac{1}{\left(\frac{W}{L}\right)}}$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{\left(\frac{W}{L}\right)_{A,E,D}} + \frac{1}{\left(\frac{W}{L}\right)_{B,C}}}$$

$$\left(\frac{W}{L}\right)_{eq} = \frac{1}{\frac{1}{30} + \frac{1}{20}}$$

$$\left(\frac{W}{L}\right)_{eq} = 12$$

Now, Load p-MOSFETs (A,E,D) and (B,C) with different (W/L) ratio ie 5 & 7.5 respectively are connected in parallel,

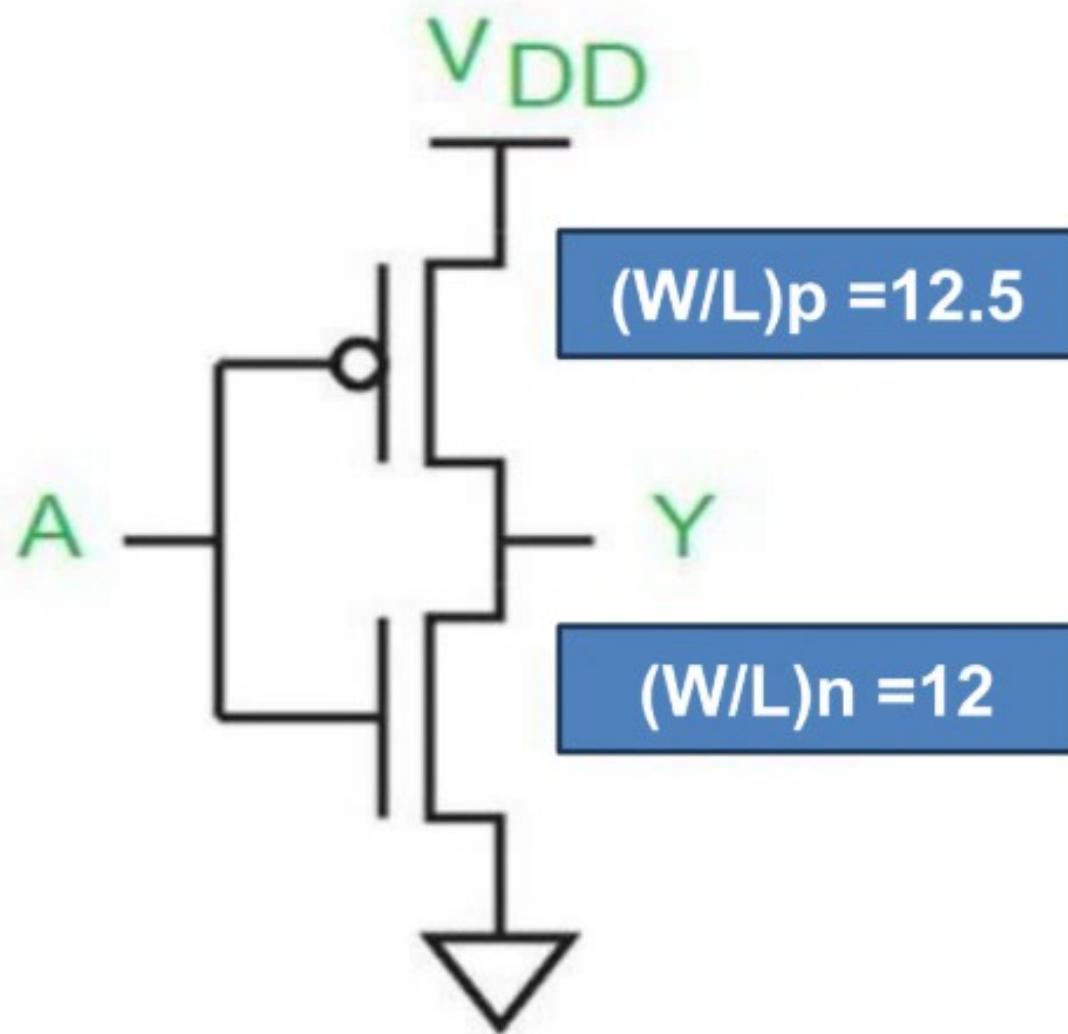
$$\left(\frac{W}{L}\right)_{eq} = \sum_1^K \left(\frac{W}{L}\right)$$

$$\left(\frac{W}{L}\right)_{eq} = \left(\frac{W}{L}\right)_{A,E,D} + \left(\frac{W}{L}\right)_{B,C}$$

$$\left(\frac{W}{L}\right)_{eq} = 5 + 7.5$$

$$\boxed{\left(\frac{W}{L}\right)_{eq} = 12.5}$$

Thus, the equivalent inverter circuit is as shown below

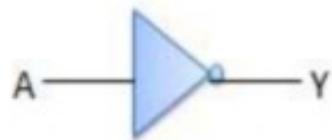


Pass-transistor Logic

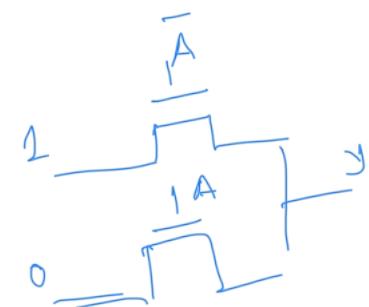
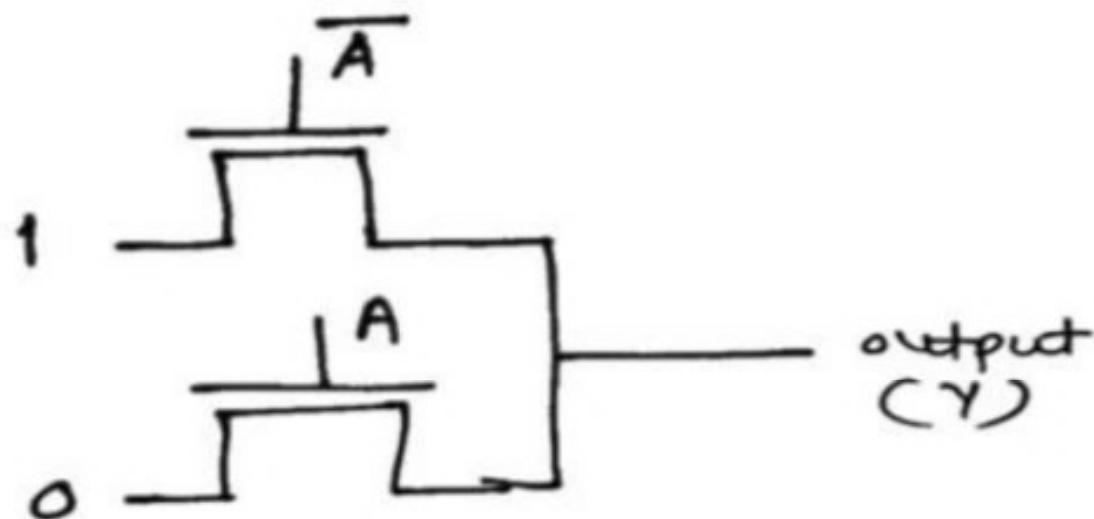
- In this logic, i/p passes to the o/p when transistor is ON.
- It utilize N-MOS transistors only to implement the logic.
- In this logic, the primary inputs drive the Gate terminal and Source-Drain terminals, unlike the static CMOS logic in which primary inputs are applied to the Gate terminal and supply voltage is applied to the Source & Drain terminals.
- Thus, the power dissipation of pass-transistor logic is negligible.

primary i/p drive the gate & S-D terminal
CMOS → i/p → gate & supply voltage → SD
power dissipation of pass
transistor logic is negligible

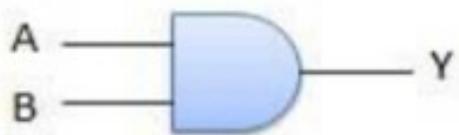
NOT-gate



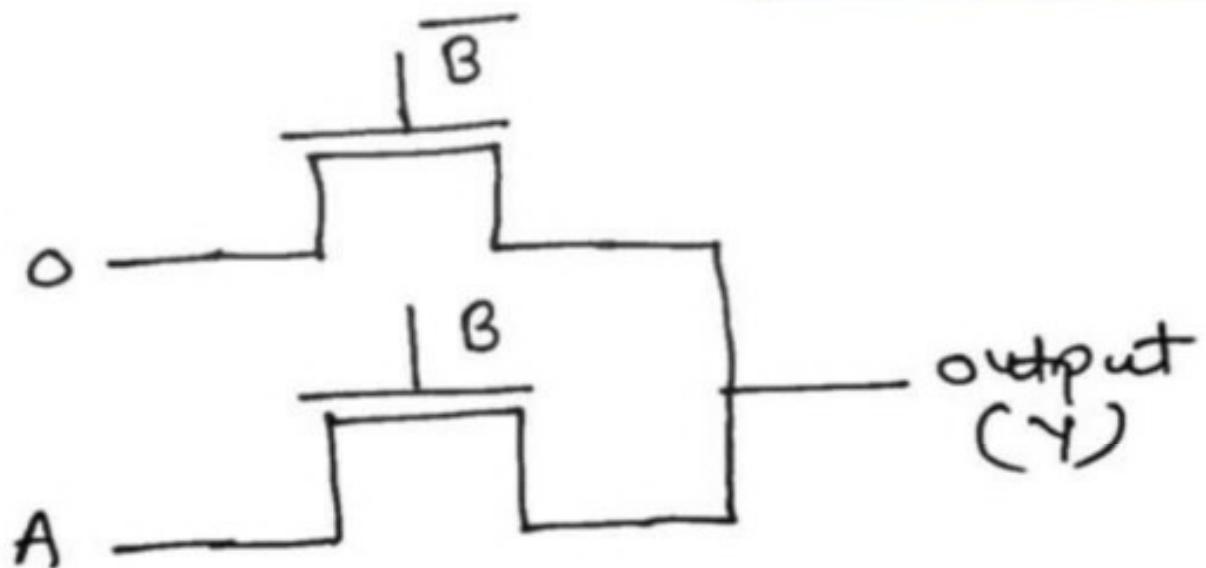
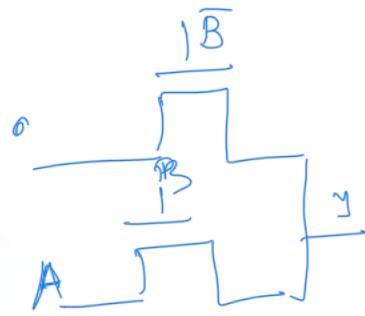
Inputs	Output
A	Y
0	1
1	0



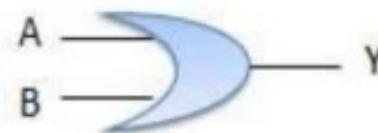
AND-gate



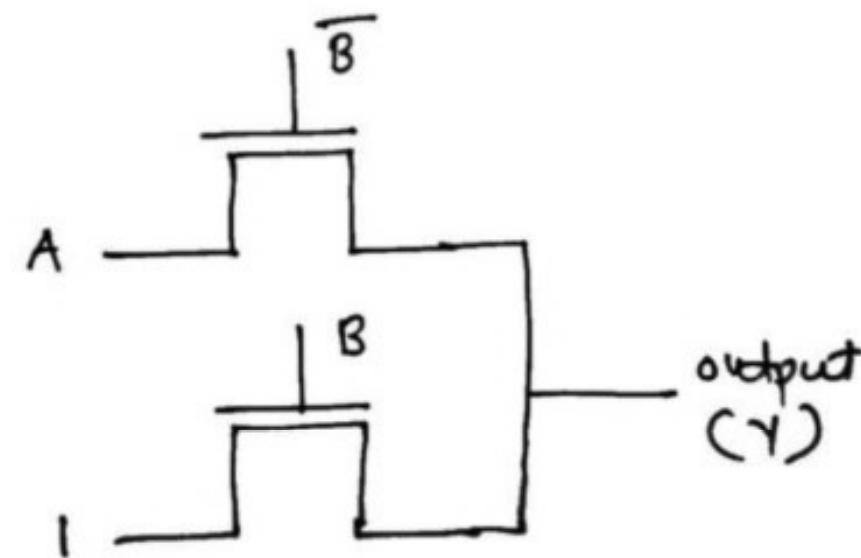
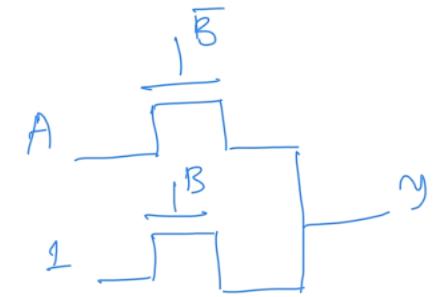
Inputs		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



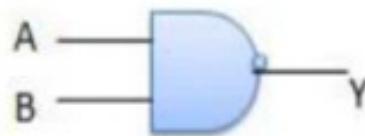
OR-gate



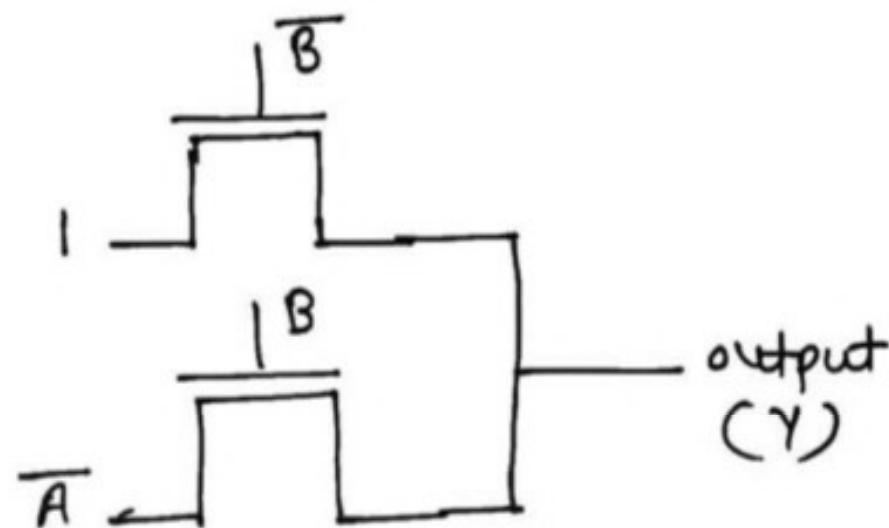
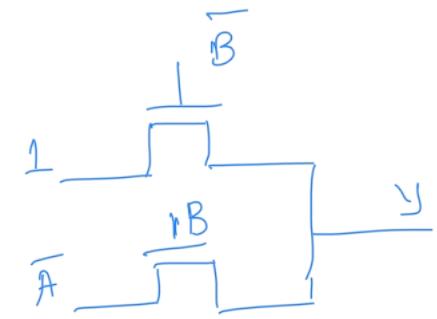
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



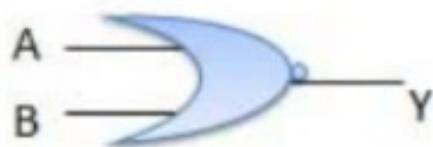
NAND-gate



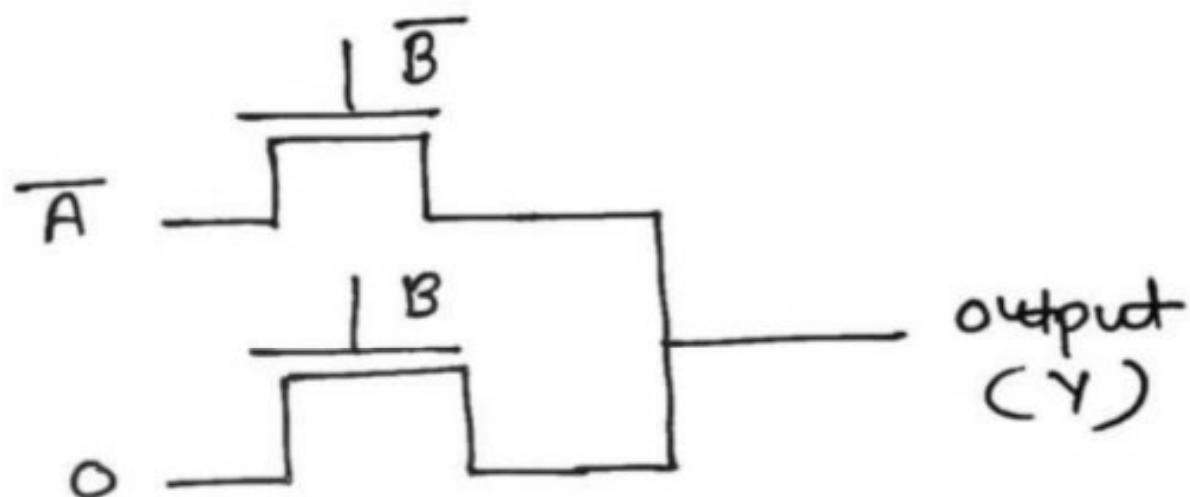
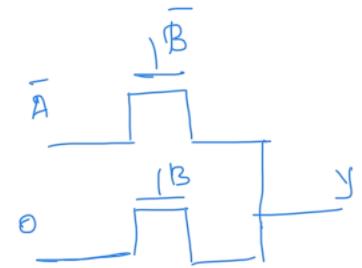
Inputs		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



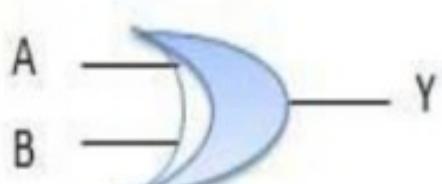
NOR-gate



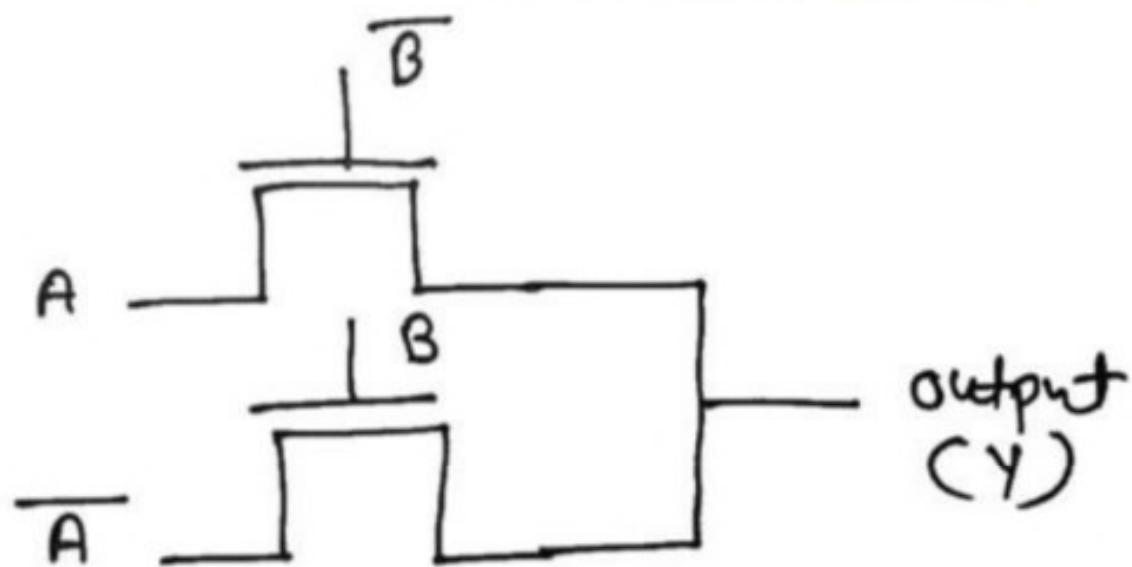
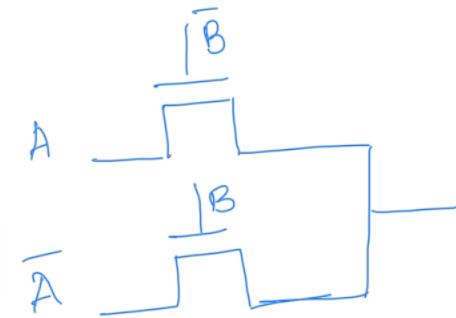
Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



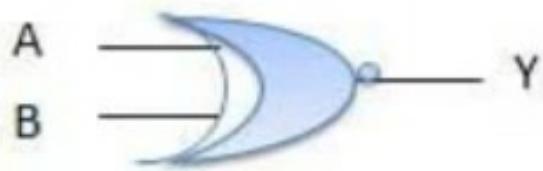
XOR-gate



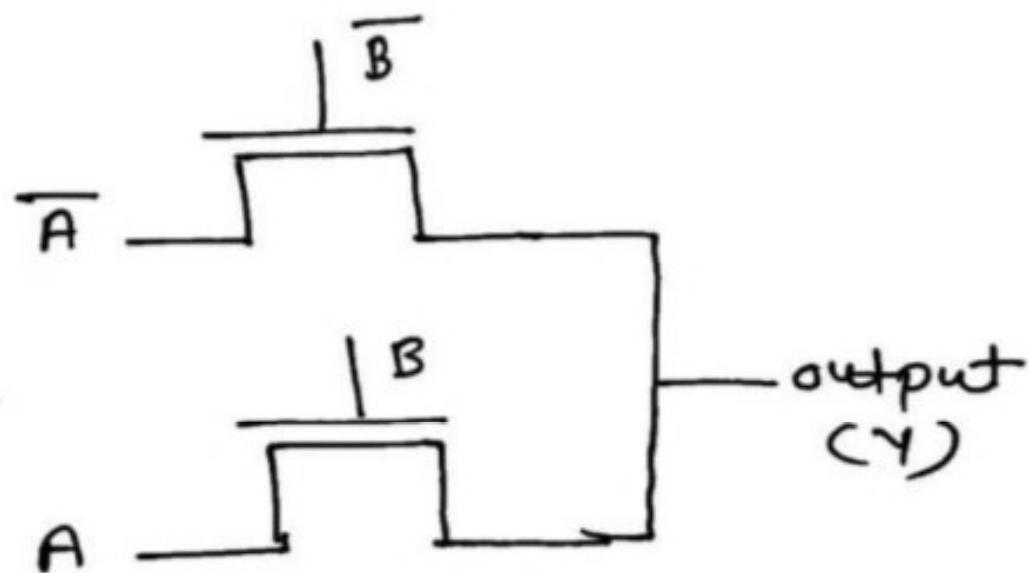
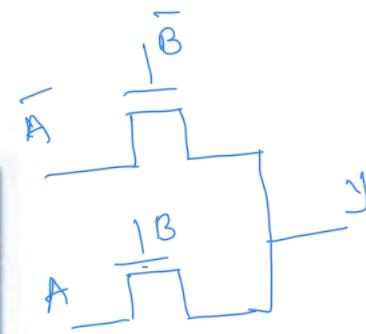
Inputs		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



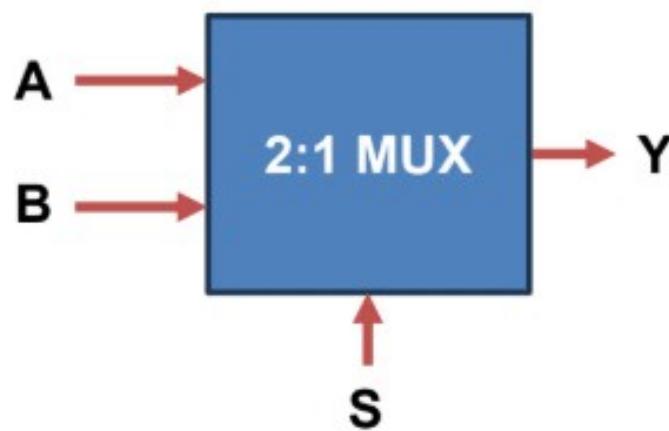
XNOR-gate



Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

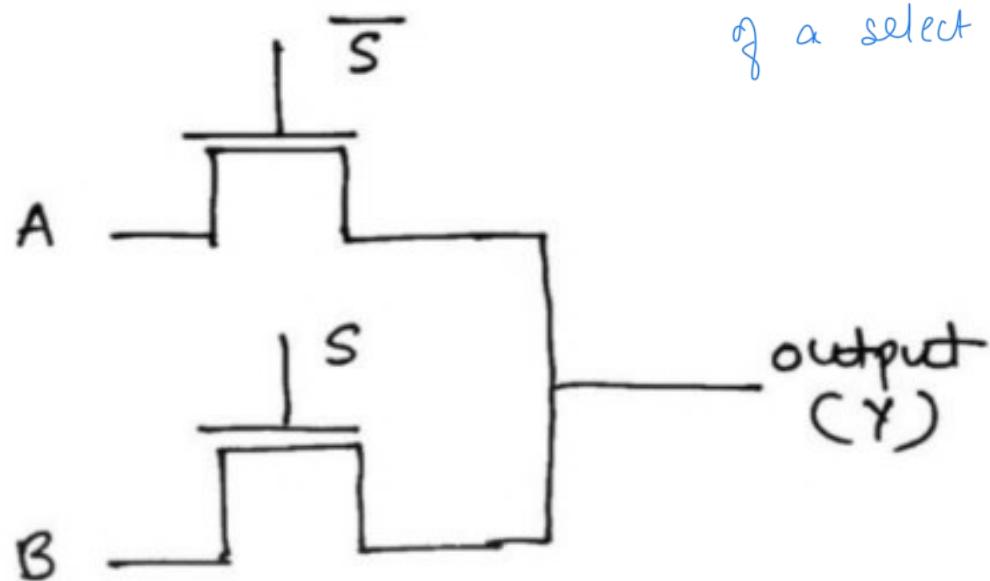


2:1 MUX



S	Y
0	A
1	B

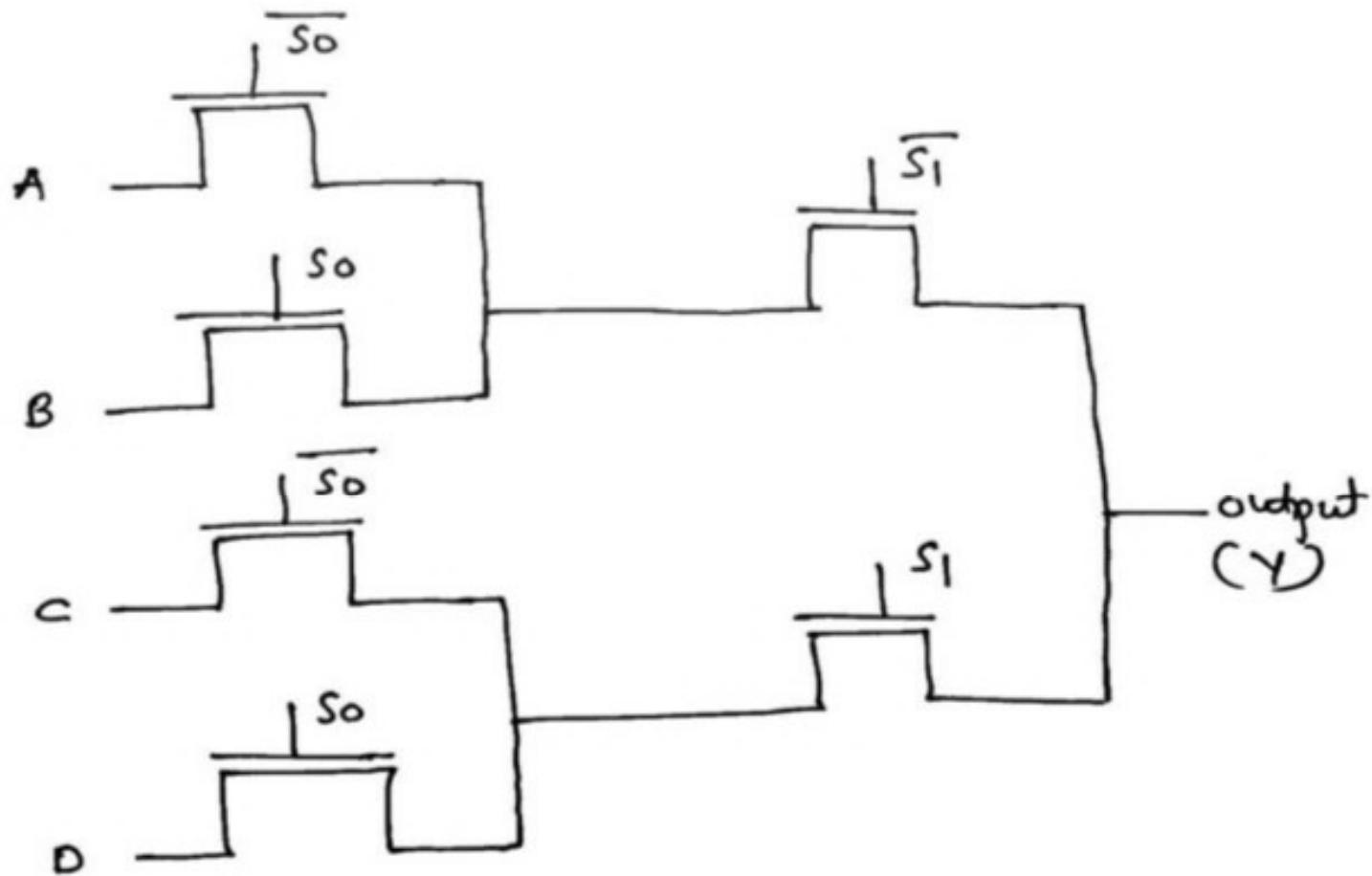
- combinational ckt that selects one of the two data signals and directs it to the output, based on the state of a select line



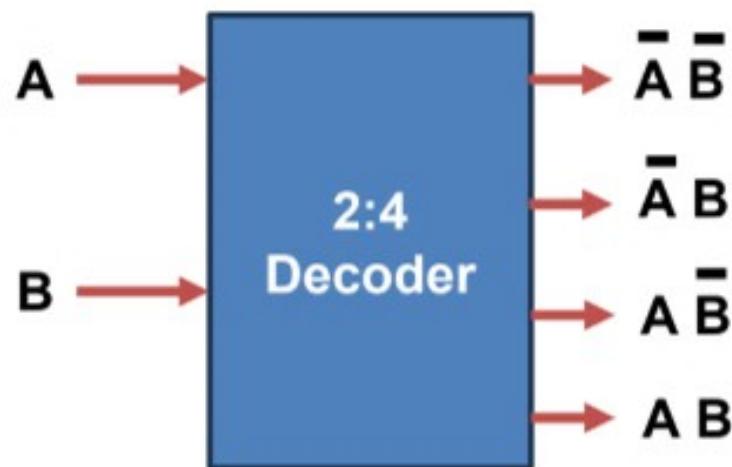
4:1 MUX



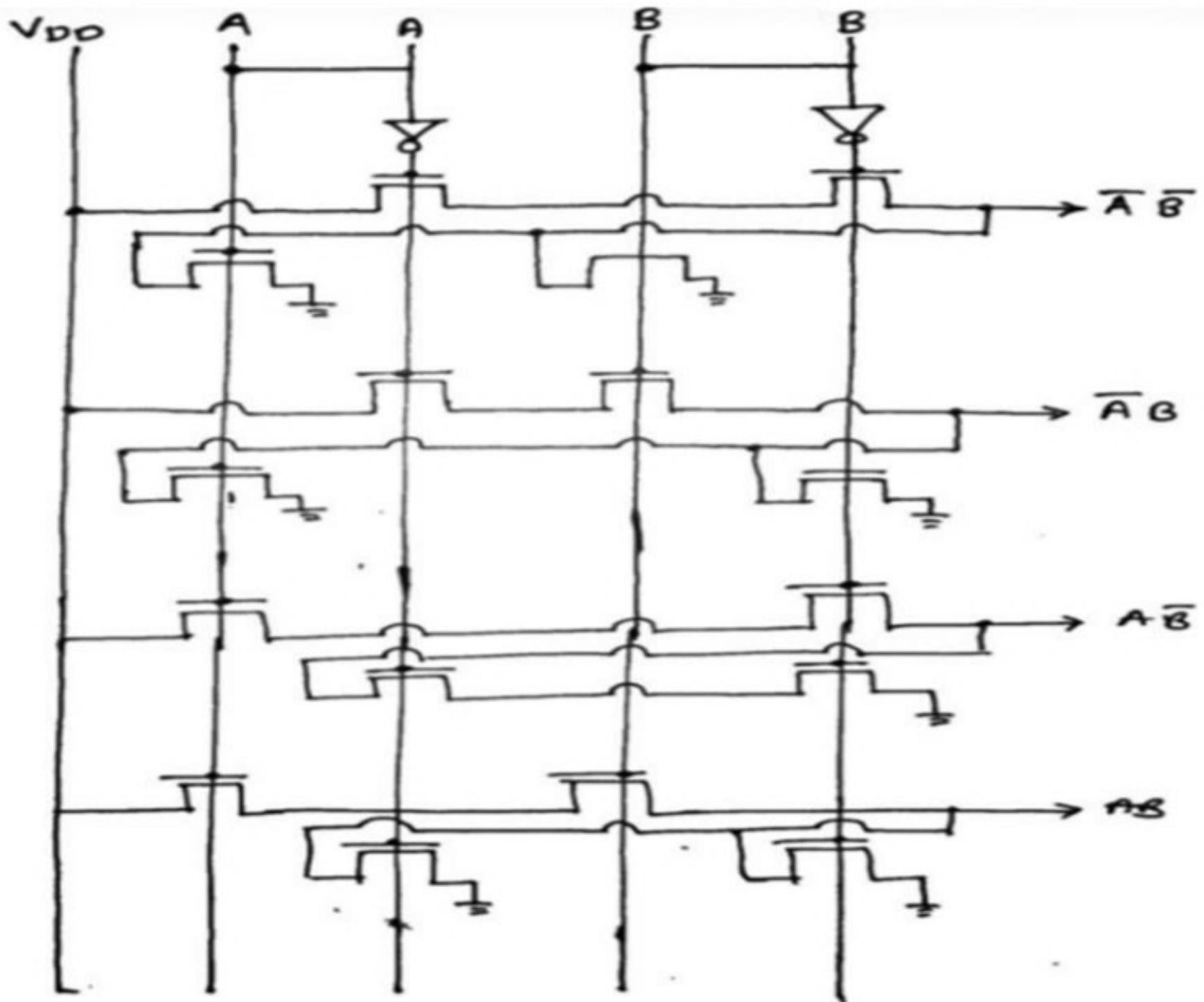
S_1	S_0	Y
0	0	A
0	1	B
1	0	C
1	1	D



2:4 Decoder



A	B	Y
0	0	$\bar{A}\bar{B}$
0	1	$\bar{A}B$
1	0	$A\bar{B}$
1	1	AB



Advantages of Pass transistor Logic

- Simple circuit
- Speed is faster
- Complex circuit can be realized using small number of transistors hence required less area.

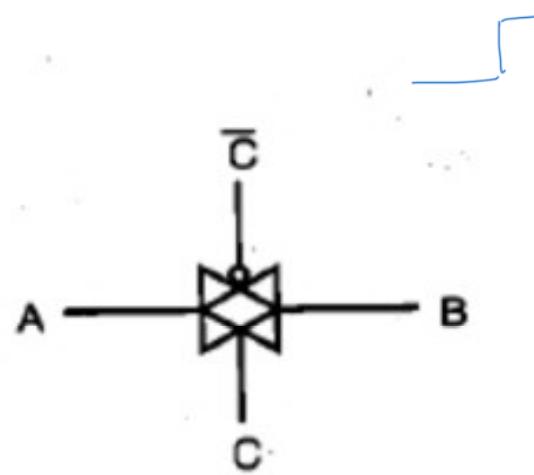
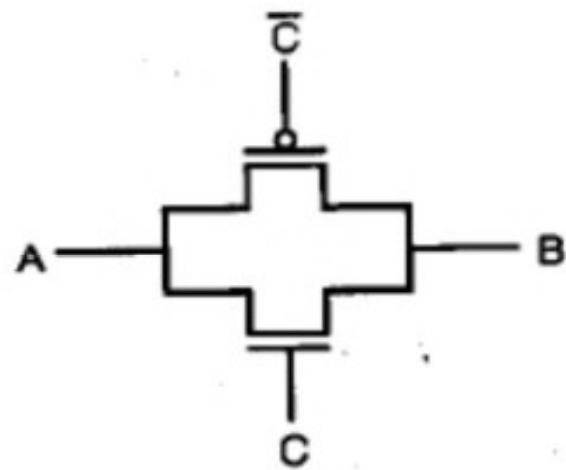
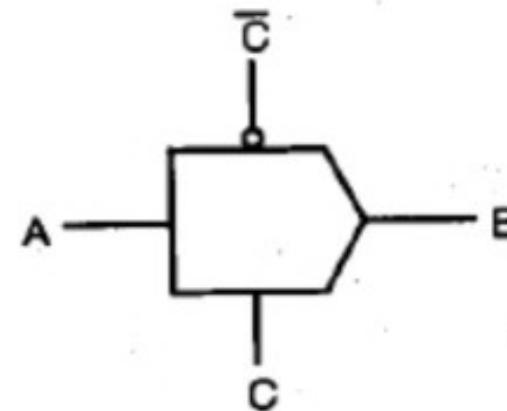
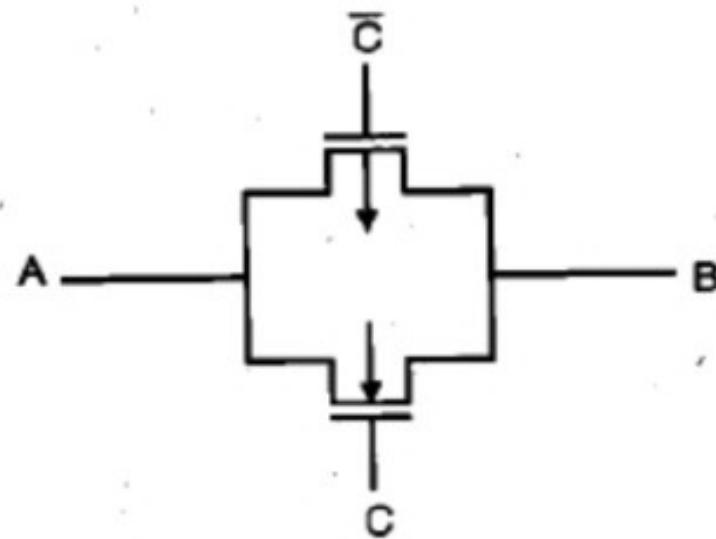
Disadvantages of Pass transistor Logic

- As NMOS transistor is good passer of Zero and poor passer of High voltage (ie V_{dd})
- So, Pass transistor can drive o/p voltage upto ($V_{dd} - V_{T,n}$)
- If this transistor is drive by another transistor then o/p voltage will be ($V_{dd} - V_{T,n} - V_{T,n}$) and after some stage it will be enter in cut-off region because $V_{GS} < V_{T,n}$
- To overcome this problem, Transmission gate is used.

Transmission gate

- N-MOS transistor can pass strong logic 0 but can not pass strong logic 1 , while P-MOS transistor can pass strong logic 1 but can not pass strong logic 0.
- For n-MOS
 $V_{in} = 0, V_{out} = 0 \quad \& \quad V_{in} = 1, V_{out} = V_{DD} - V_{T,n}$
- For p-MOS
 $V_{in} = 0, V_{out} = |V_{T,p}| \quad \& \quad V_{in} = 1, V_{out} = 0$
- Thus, by connecting them together in parallel , the full voltage range from 0 to V_{dd} can be transmitted.
- Such a switch acts as a voltage controlled switch where the control signal is applied to the gate of N-MOS transistor and complement to the gate of P-MOS transistor.

Four different representations of the CMOS transmission gate (TG).

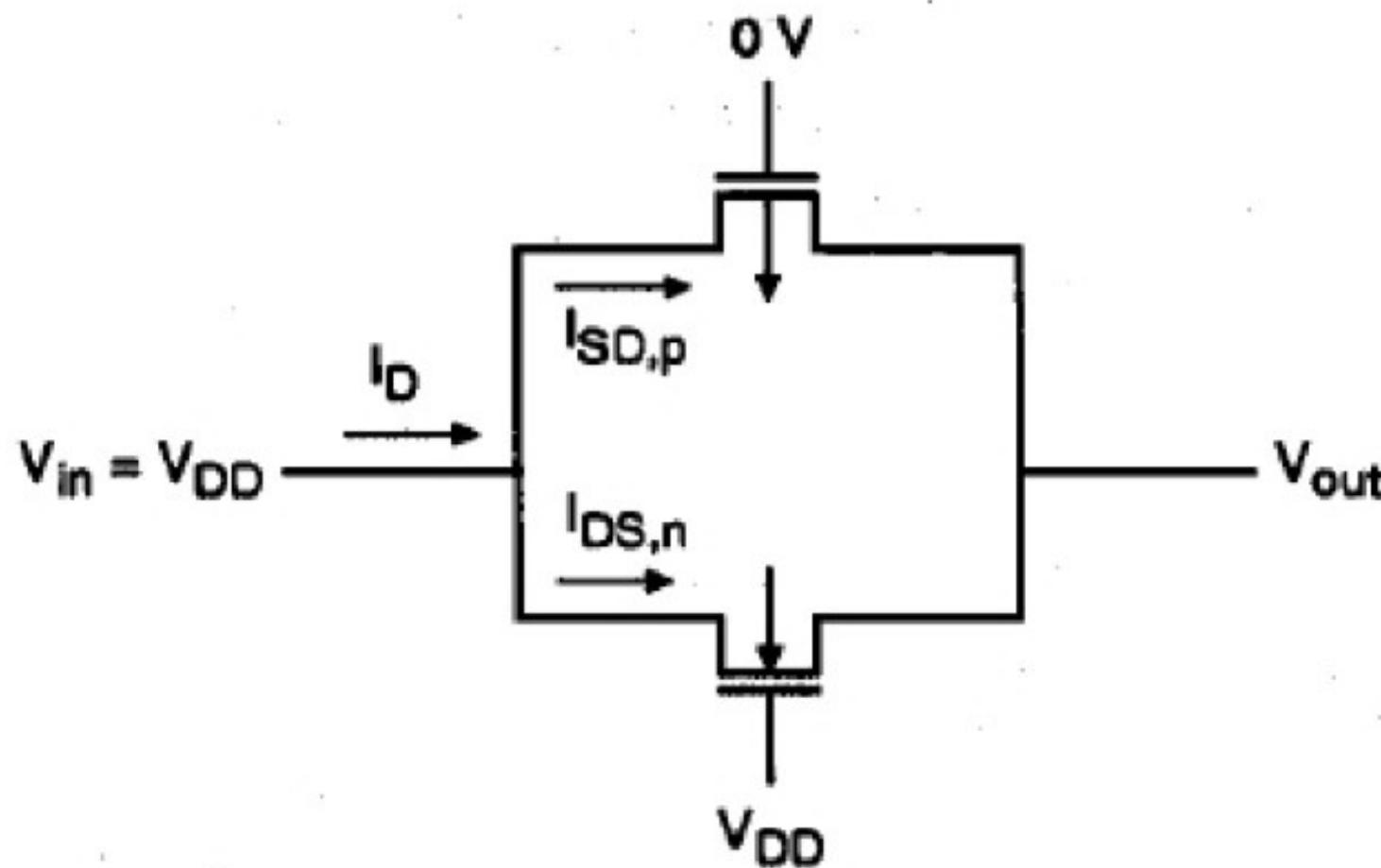


Working Principle of Transmission gate

- When control signal 'C' is high, both N-MOS & P-MOS transistors becomes 'ON' & forming an electrical path between the left & right side (ie. low impedance path).
- On the other hand, when control signal 'C' is low, both the MOSFETs are 'OFF' and switch is open (ie high impedance state).

DC analysis of CMOS Transmission Gate

- Let us consider the following bias condition,



\Rightarrow The total current flowing through the transmission gate is

$$I_D = I_{DS,n} + I_{SD,p}$$

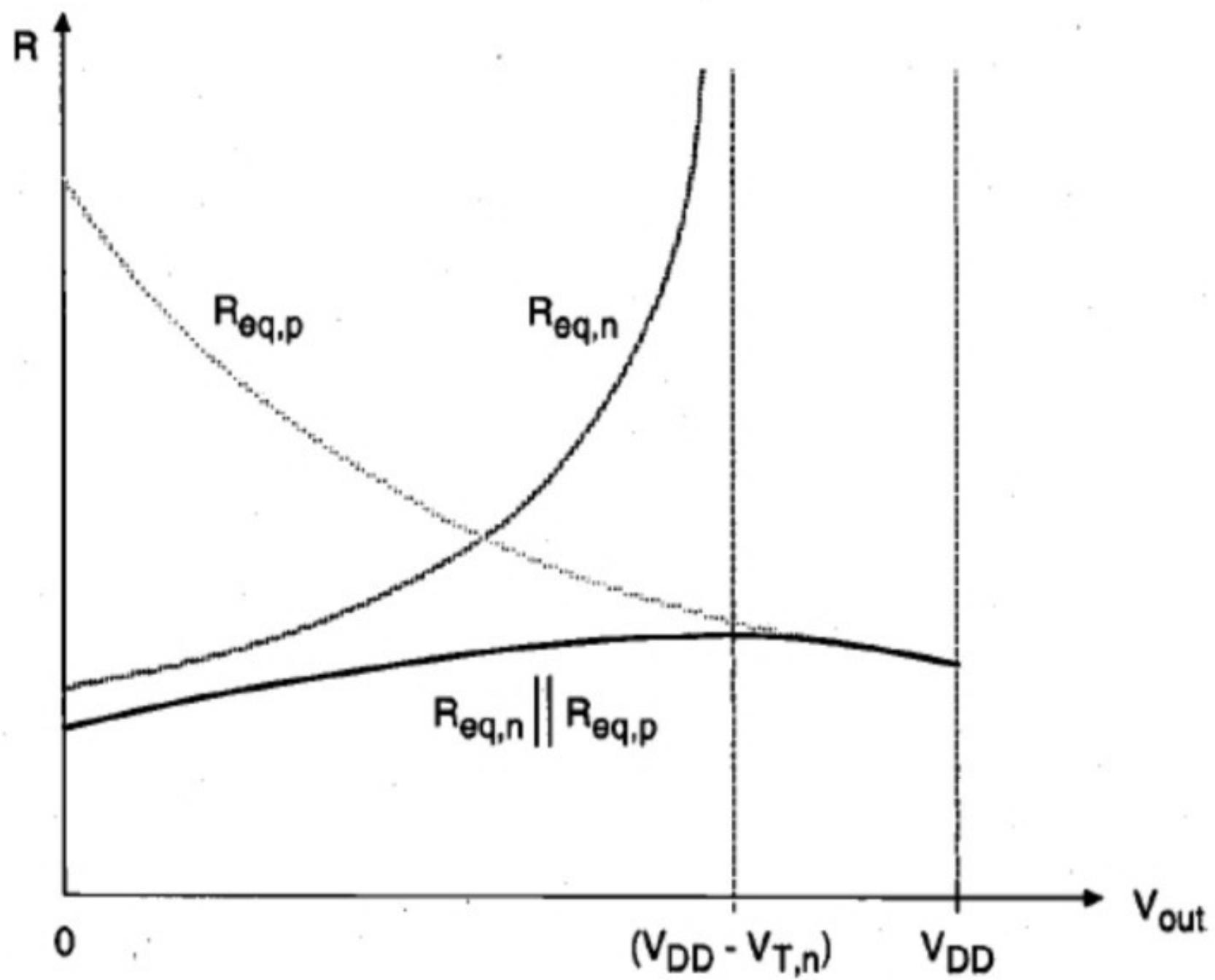
So, the equivalent resistance for each xtor is,

$$R_{eq,n} = \frac{V_{DD} - V_{out}}{I_{DS,n}}$$

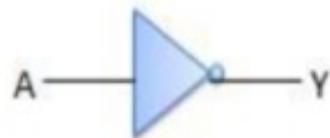
$$\& R_{eq,p} = \frac{V_{DD} - V_{out}}{I_{SD,p}}$$

& total equi. resistance of the CMOS TG will then

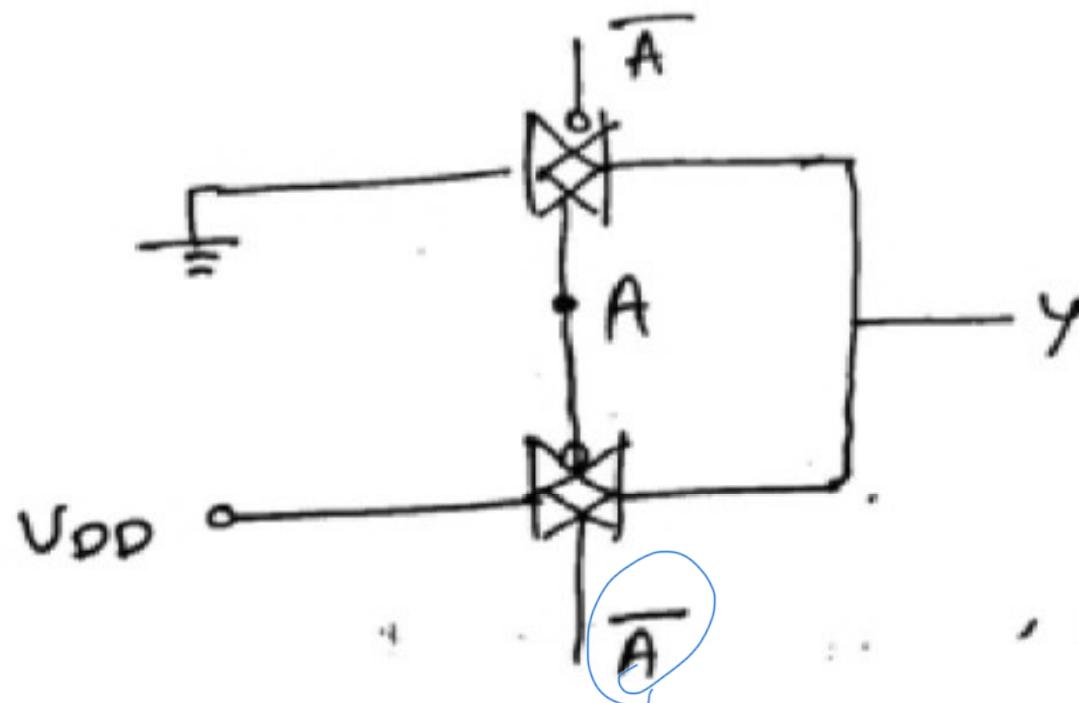
be then
$$R_{eq(T.G.)} = R_{eq(n)} || R_{eq(p)}$$



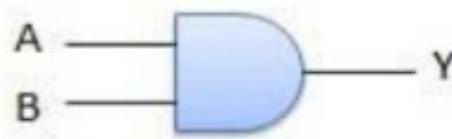
NOT-gate



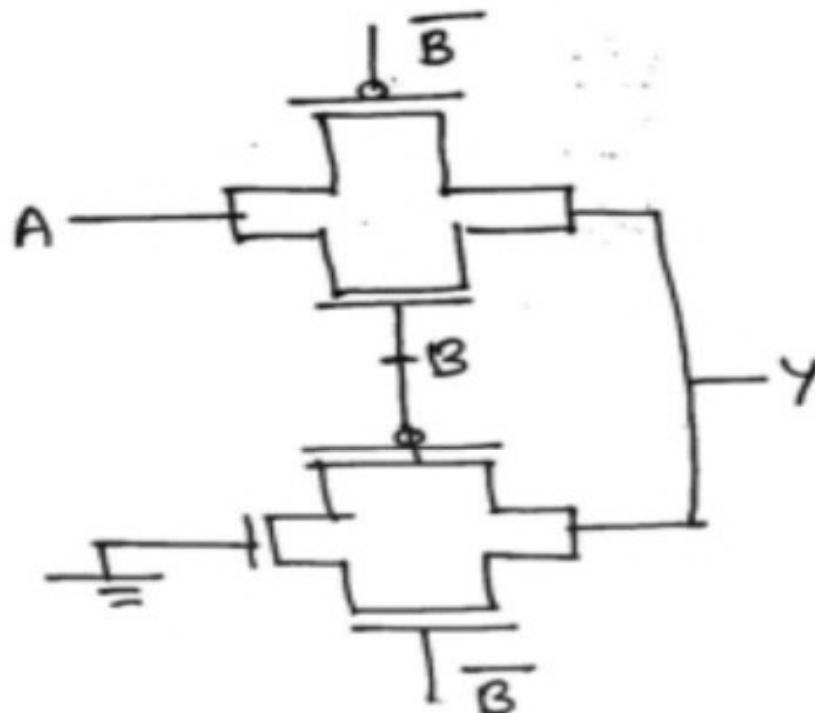
Inputs	Output
A	B
0	1
1	0



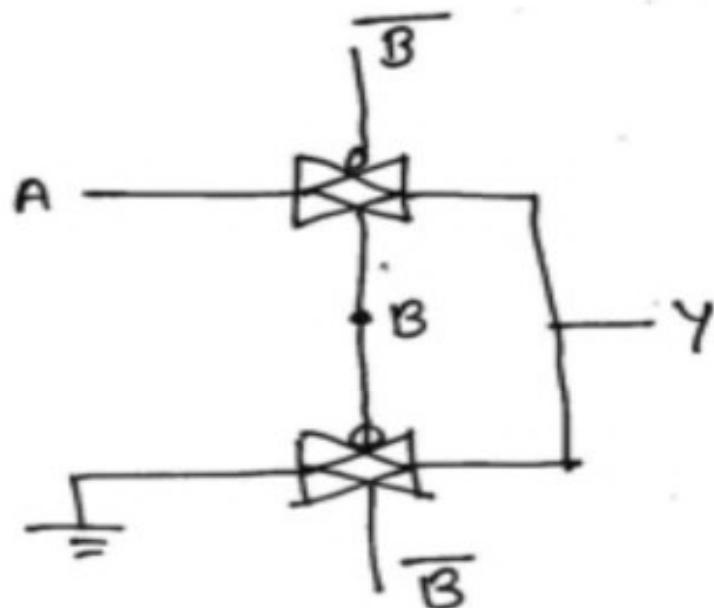
AND-gate



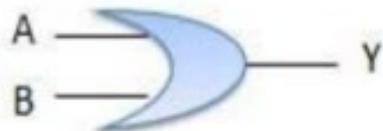
Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



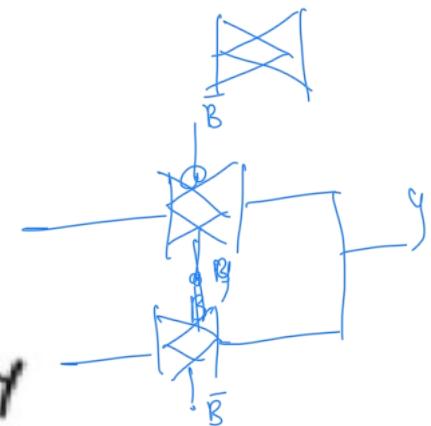
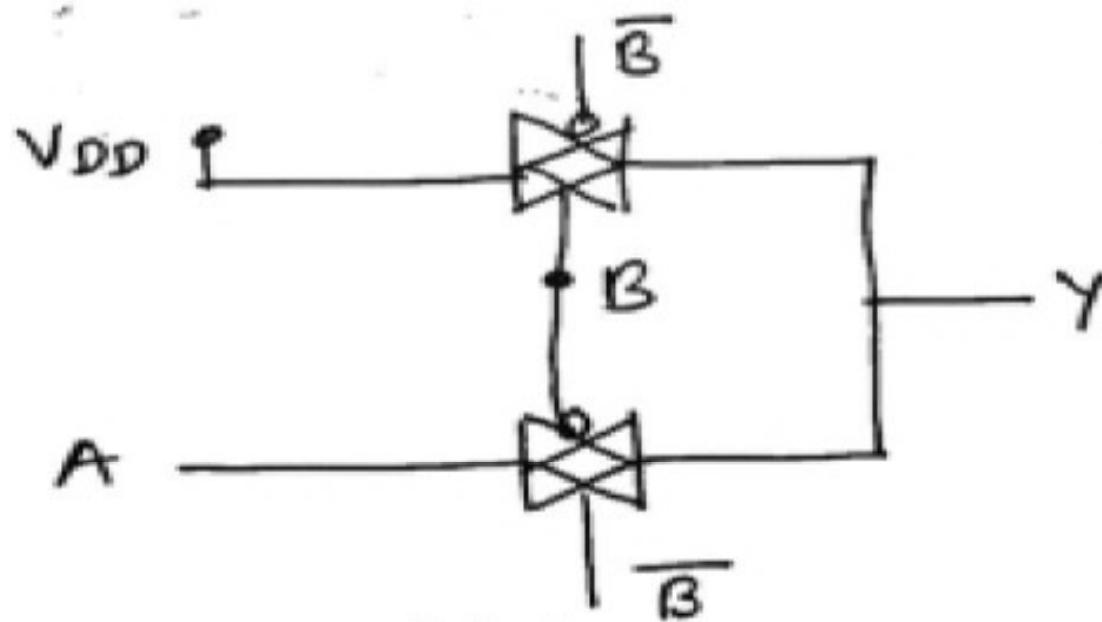
OR



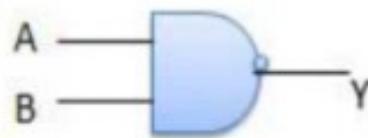
OR-gate



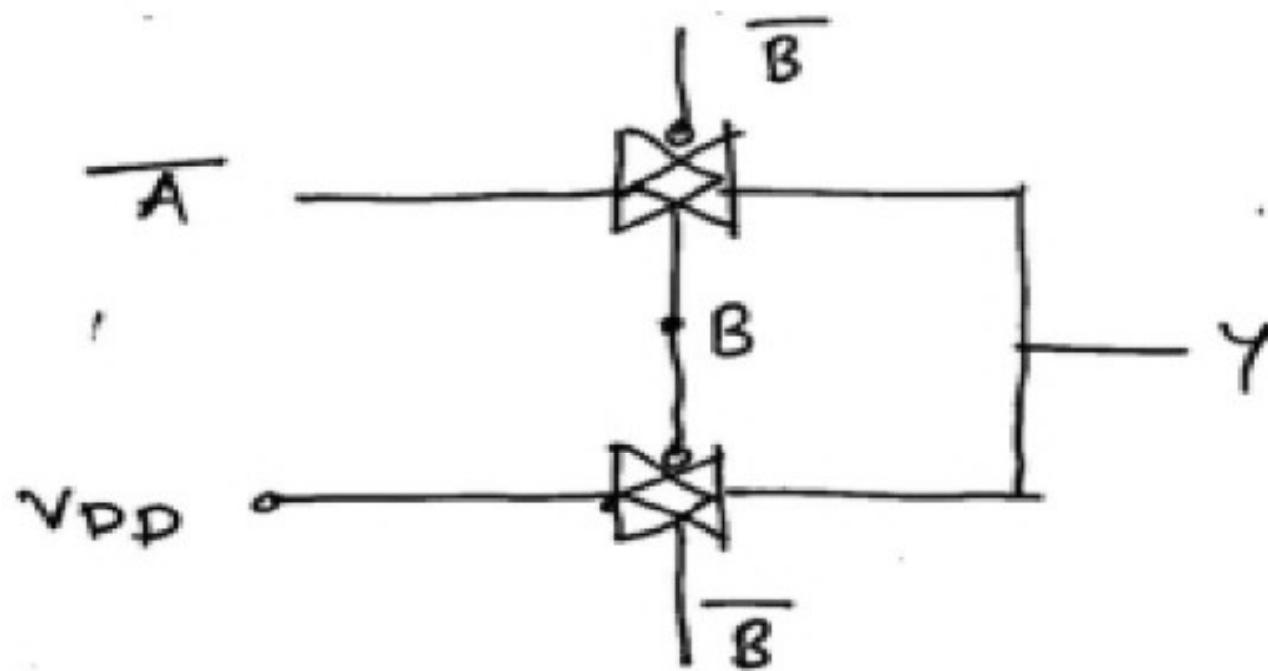
Inputs		Output
A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1



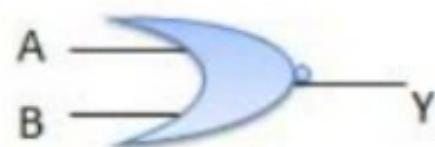
NAND-gate



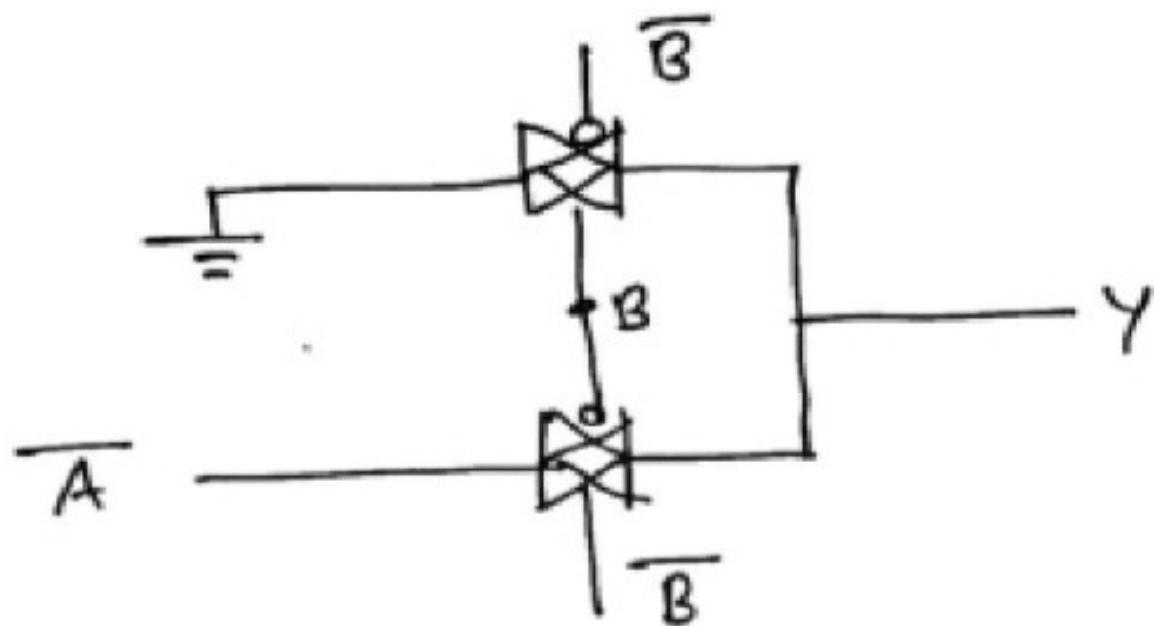
Inputs		Output
A	B	\overline{AB}
0	0	1
0	1	1
1	0	1
1	1	0



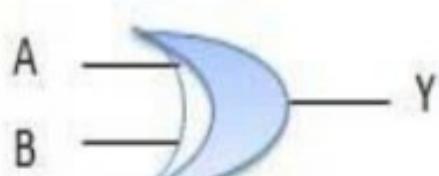
NOR-gate



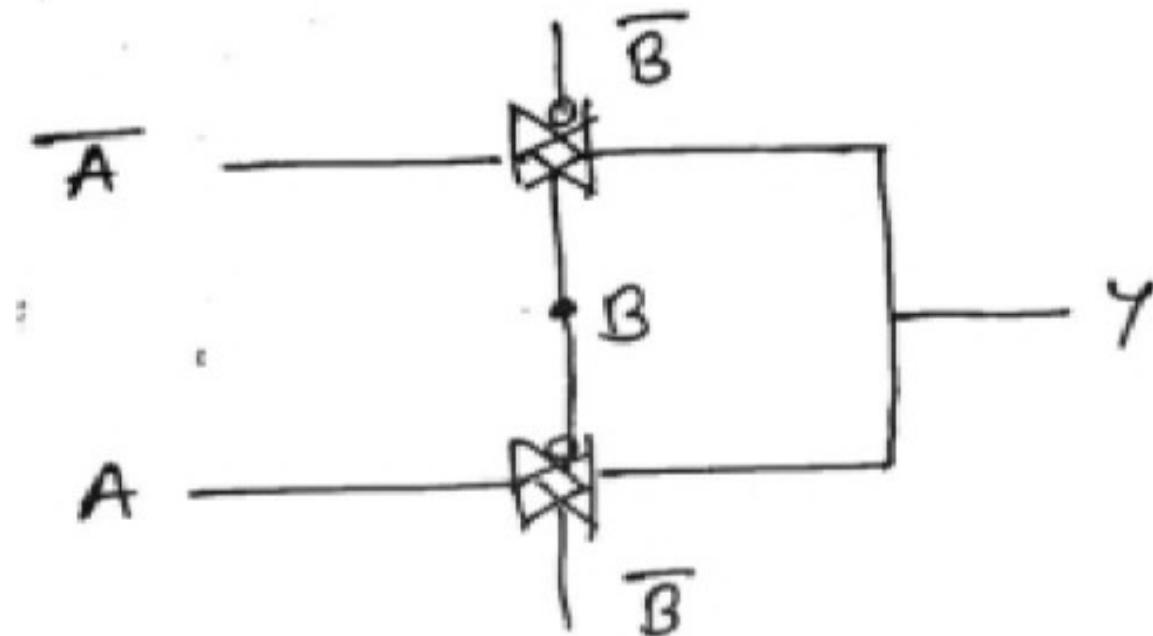
Inputs		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



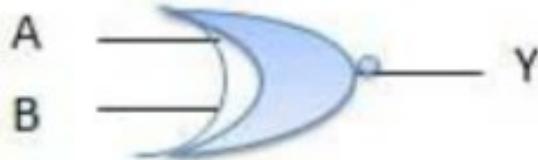
XOR-gate



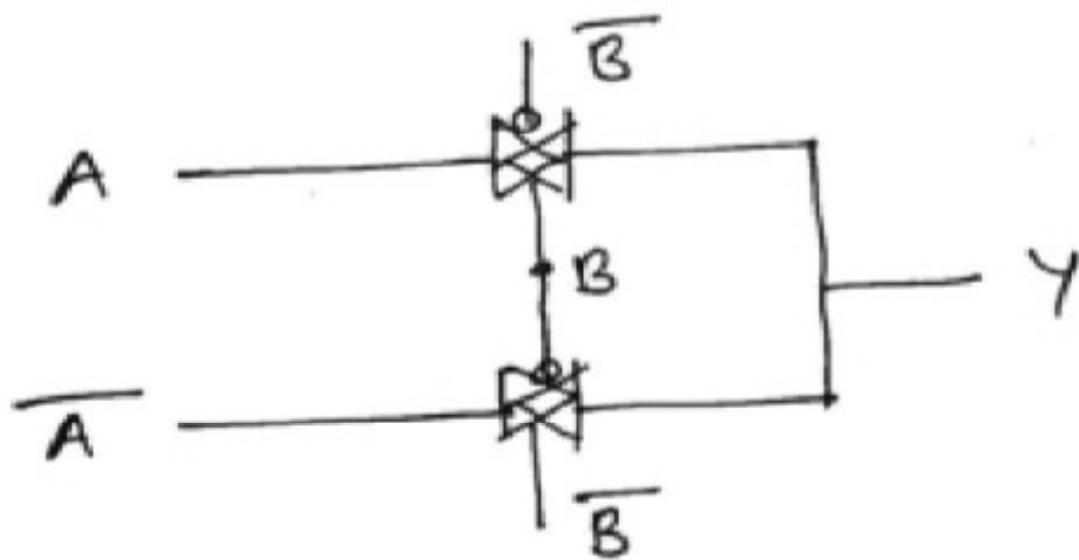
Inputs		Output
A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	0



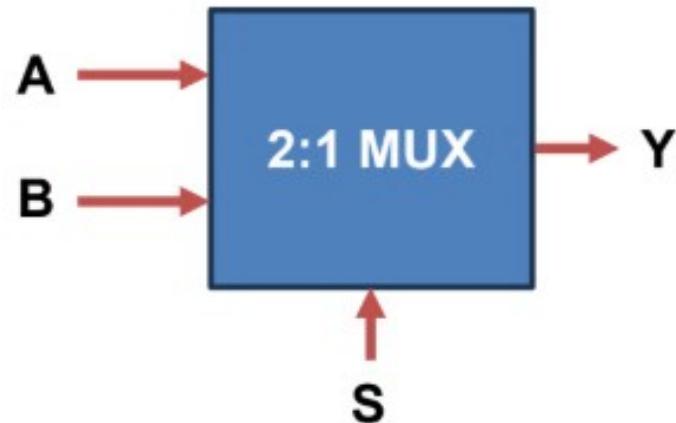
XNOR-gate



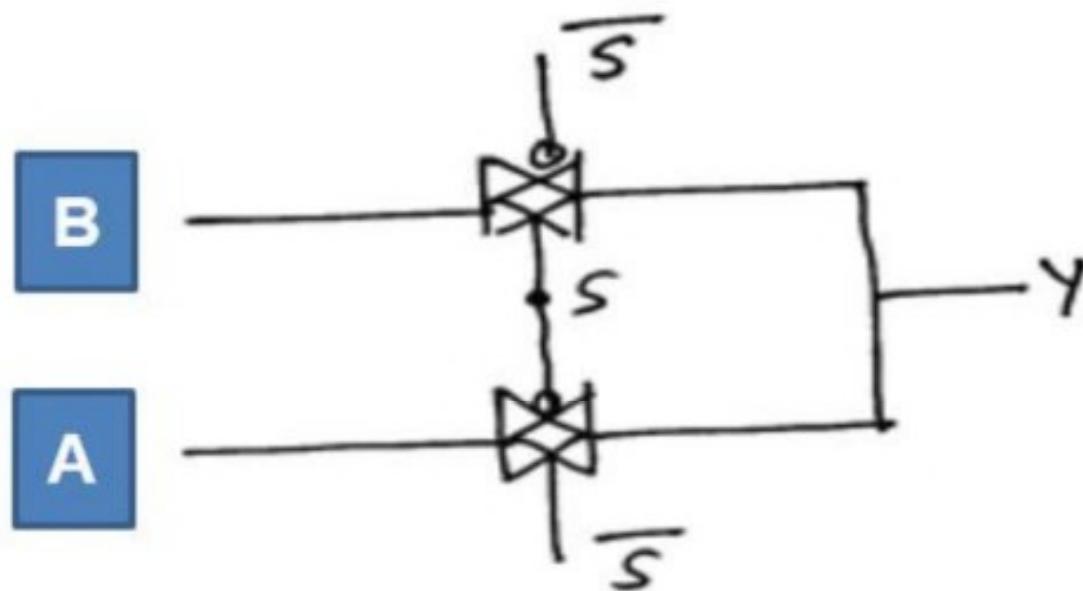
Inputs		Output
A	B	$A \oplus B$
0	0	1
0	1	0
1	0	0
1	1	1



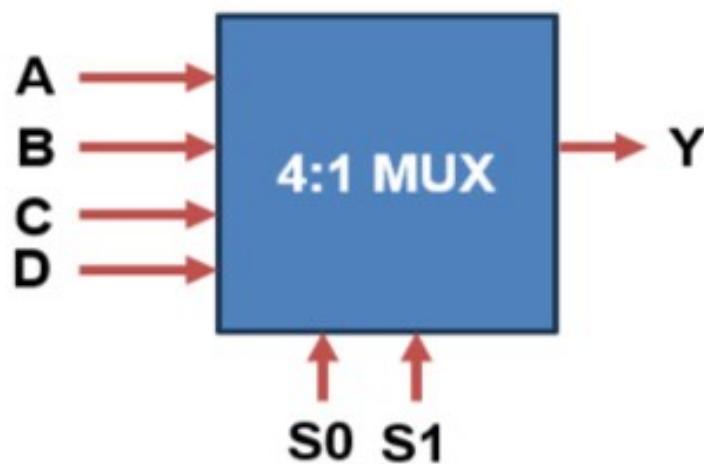
2:1 MUX



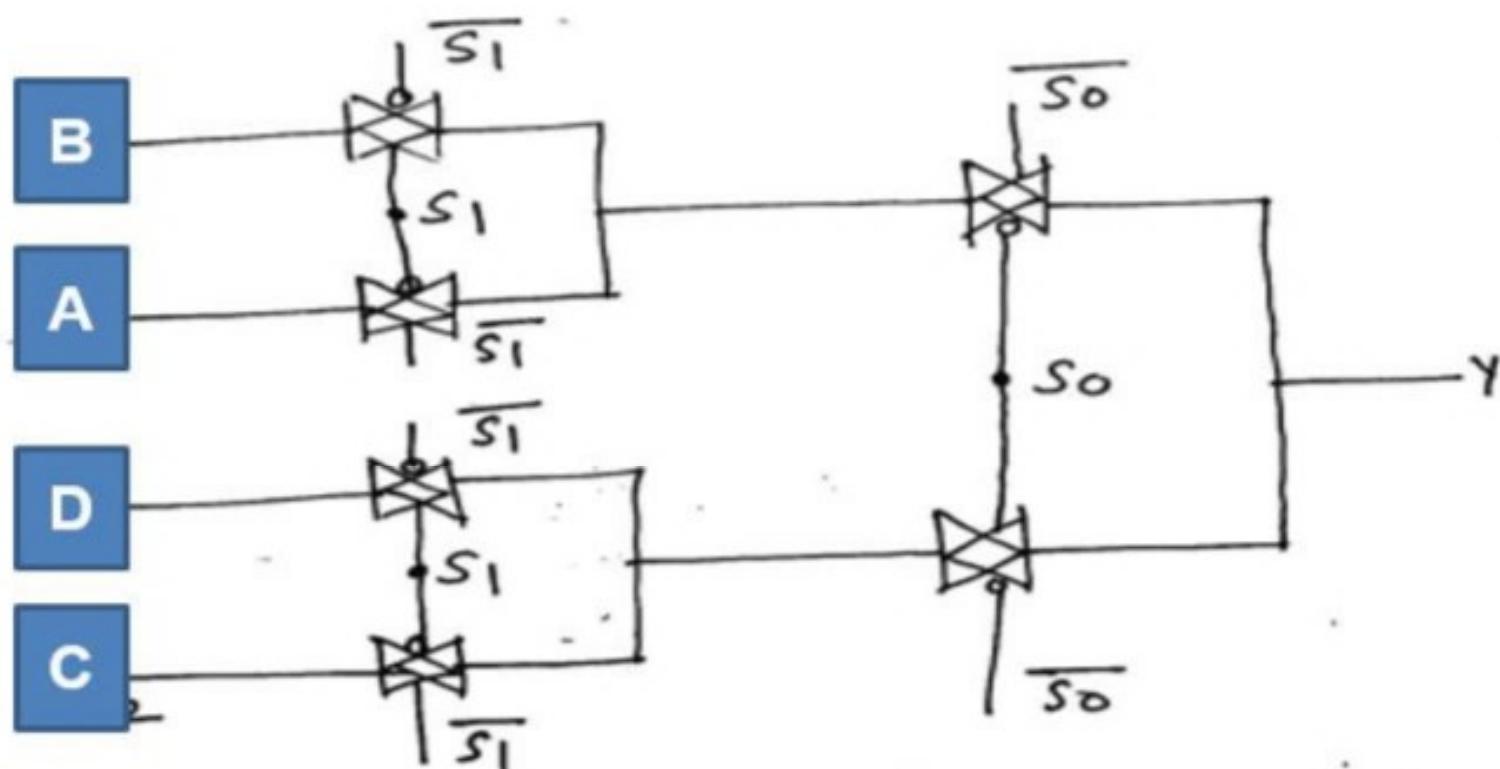
S	Y
0	A
1	B



4:1 MUX



S_1	S_0	Y
0	0	A
0	1	B
1	0	C
1	1	D



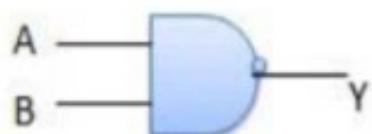
Pseudo n-MOS

pseudo
pmos → grounded gate

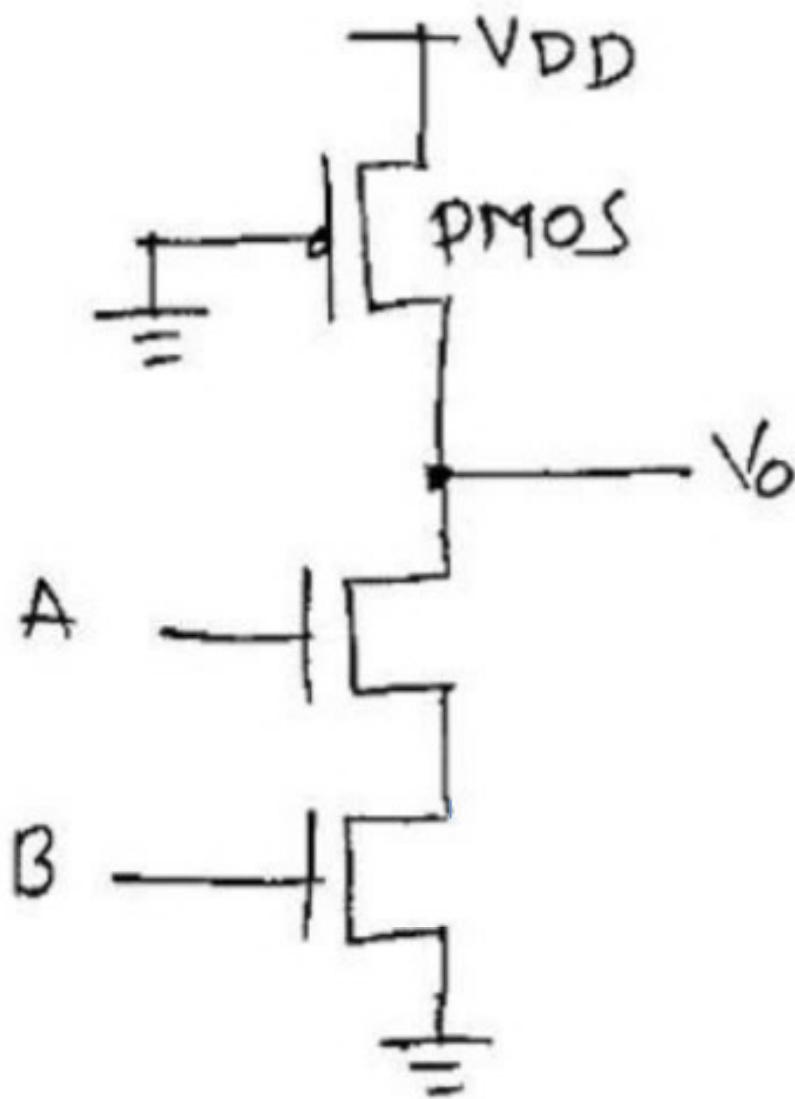
- This technique uses single p-MOS transistor with grounded gate at the load side.
- Because of grounded Gate of p-MOS transistor it is always in ON state.
- The logical inputs are applied to n-MOS logic circuit.
- The given function should be in complement form to construct the n-MOS logic circuit.

NAND-gate

$$Y = \overline{A \cdot B}$$



Inputs		Output
A	B	\overline{AB}
0	0	1
0	1	1
1	0	1
1	1	0

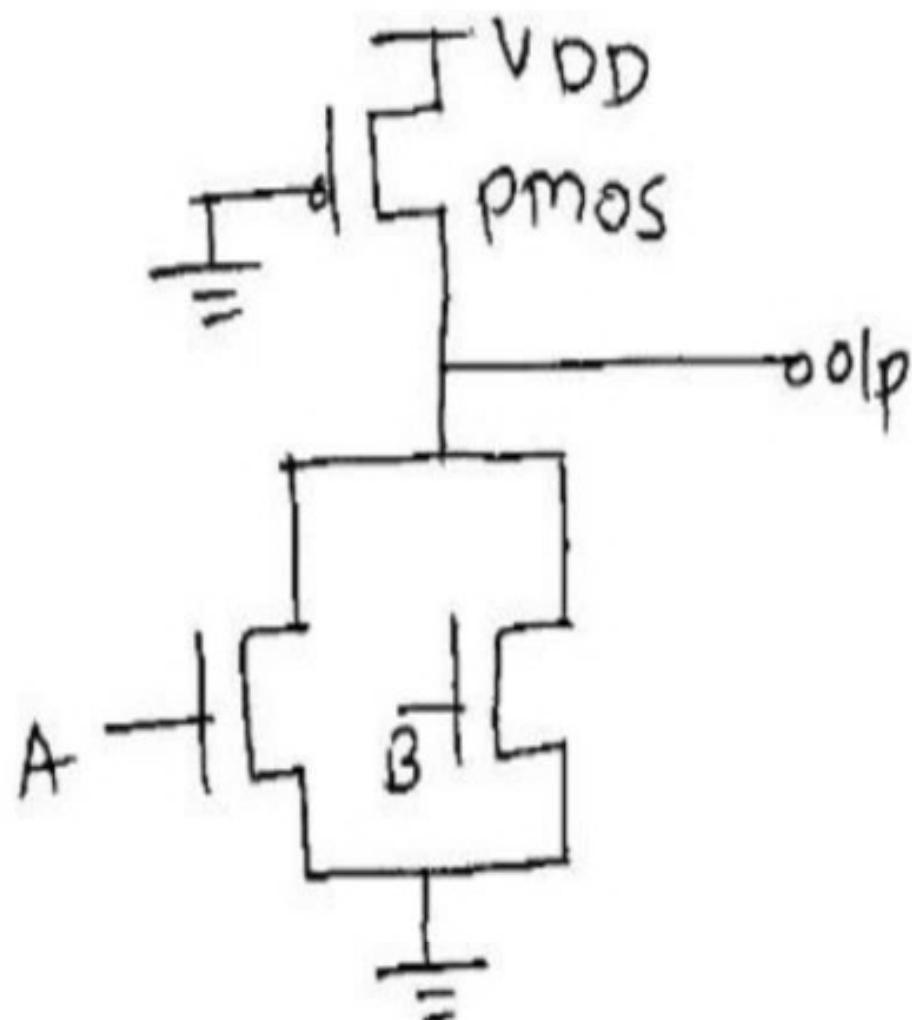


NOR-gate

$$Y = \overline{A+B}$$



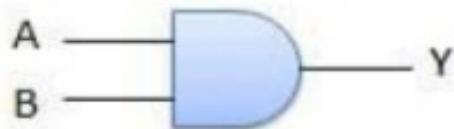
Inputs		Output
A	B	$\overline{A+B}$
0	0	1
0	1	0
1	0	0
1	1	0



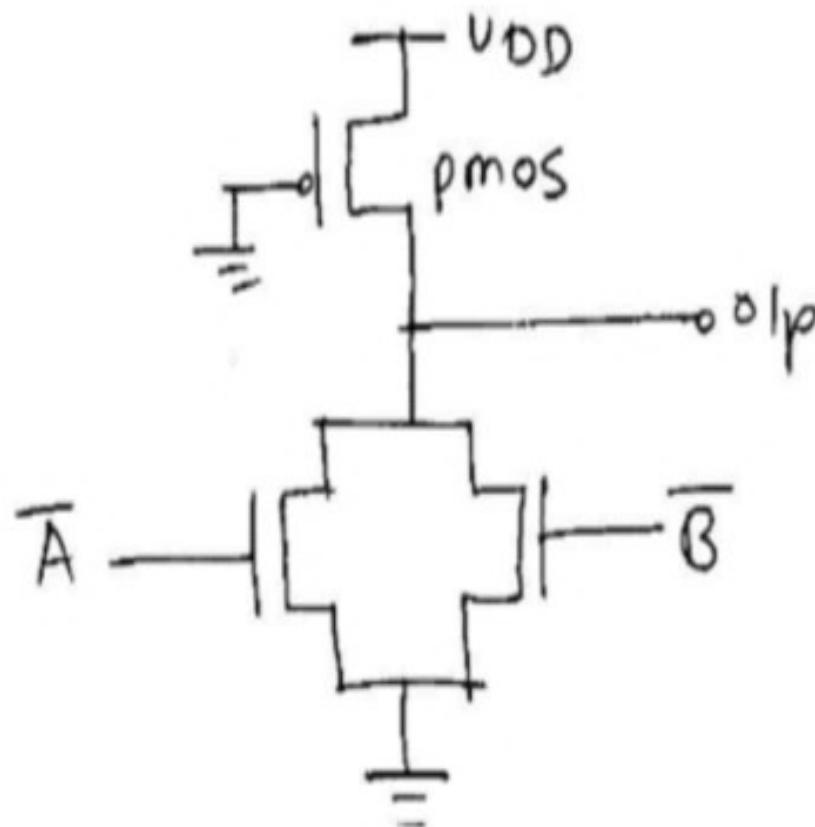
AND-gate

$$Y = A \cdot B$$

$$f = \overline{\overline{A \cdot B}} = \overline{\overline{A} + \overline{B}}$$



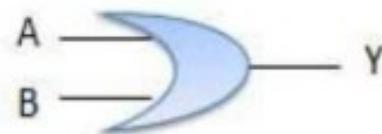
Inputs		Output
A	B	AB
0	0	0
0	1	0
1	0	0
1	1	1



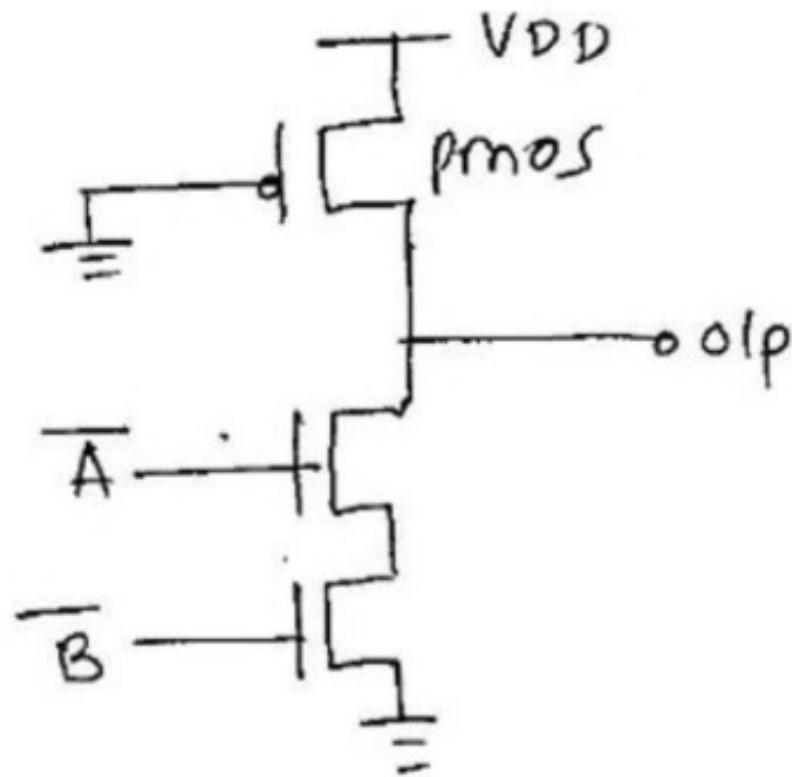
OR-gate

$$Y = A+B$$

$$f = \overline{(A+B)} = \overline{\overline{A} \cdot \overline{B}}$$

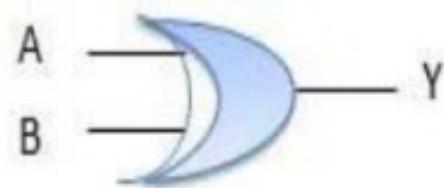


Inputs		Output
A	B	$A + B$
0	0	0
0	1	1
1	0	1
1	1	1



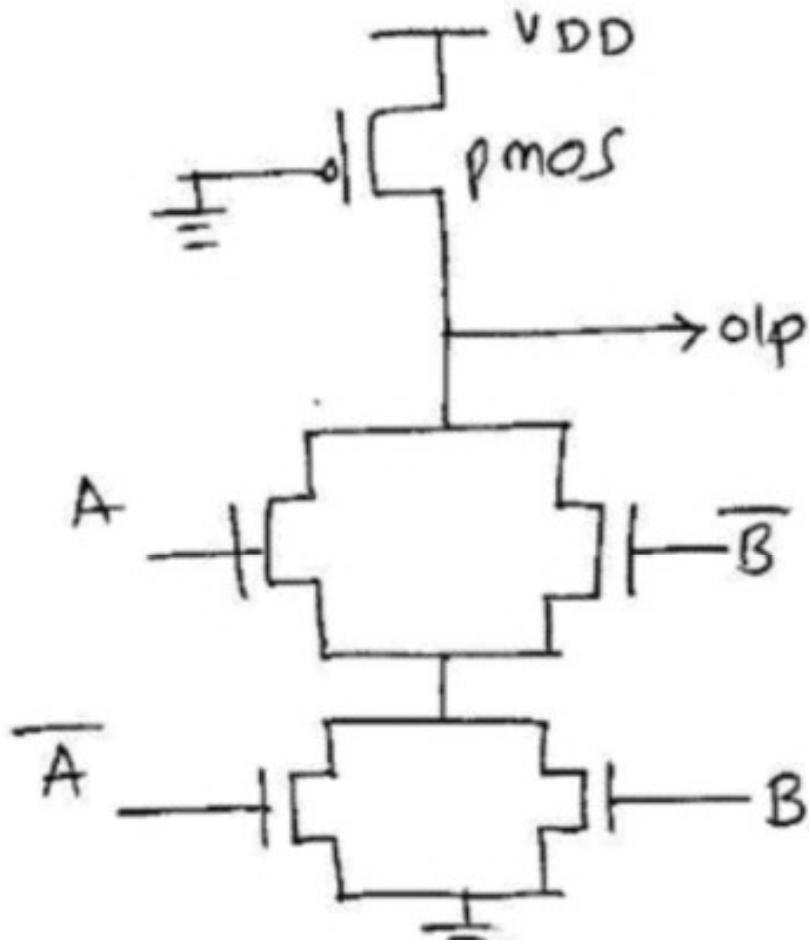
XOR-gate

$$f = A \oplus B$$



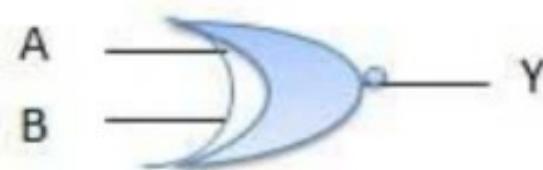
Inputs		Output
A	B	$A \oplus B$
0	0	0
0	1	1
1	0	1
1	1	0

$$\begin{aligned} f &= (\overline{\overline{A}B + A\overline{B}}) \\ &= \overline{(\overline{\overline{A}B}) \cdot (\overline{A}\overline{B})} \\ &= \overline{(A+\overline{B}) \cdot (\overline{A}+B)} \end{aligned}$$



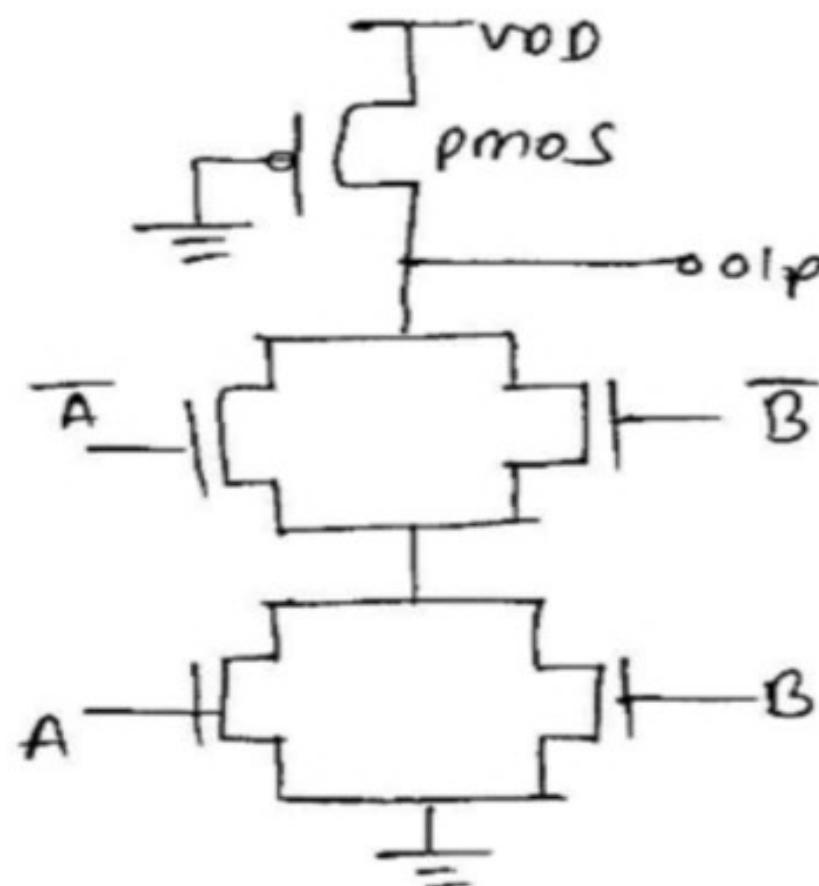
XNOR-gate

$$f = A \oplus B$$



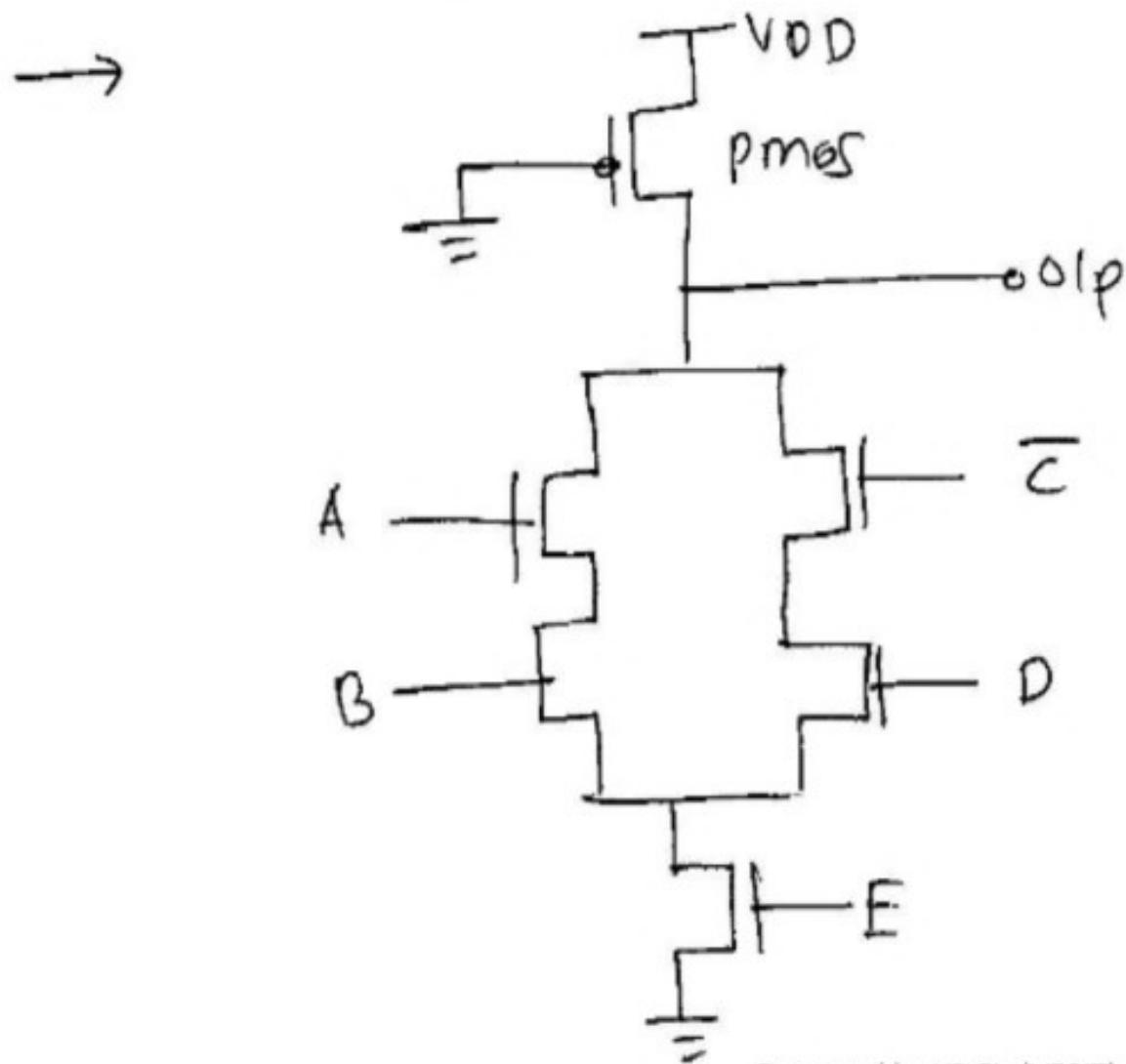
Inputs		Output
A	B	$A \oplus B$
0	0	1
0	1	0
1	0	0
1	1	1

$$\begin{aligned}
 f &= (\overline{AB} + \overline{\bar{A} \cdot \bar{B}}) \\
 &= \overline{(\overline{AB}) \cdot (\overline{\bar{A} \cdot \bar{B}})} \\
 &= \overline{(\overline{A} + \overline{B}) \cdot (\overline{\bar{A}} + \overline{\bar{B}})} \\
 &= \overline{(\overline{A} + \overline{B}) \cdot (A + B)}
 \end{aligned}$$

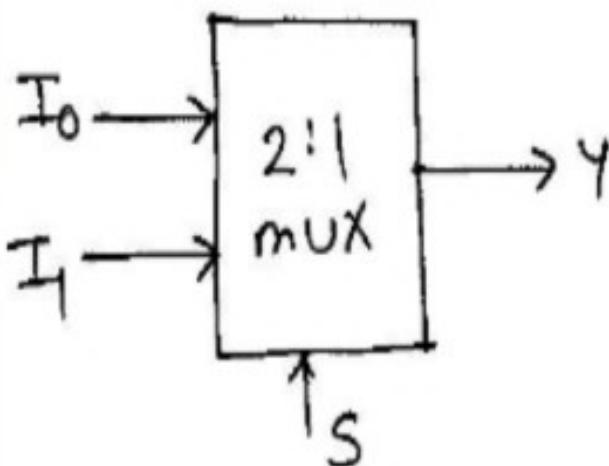


Q9) Realize the following function using pseudo n-mos logic

$$f = \overline{(A \cdot B + \overline{C} \cdot D)} E$$



eq 2:1 mux

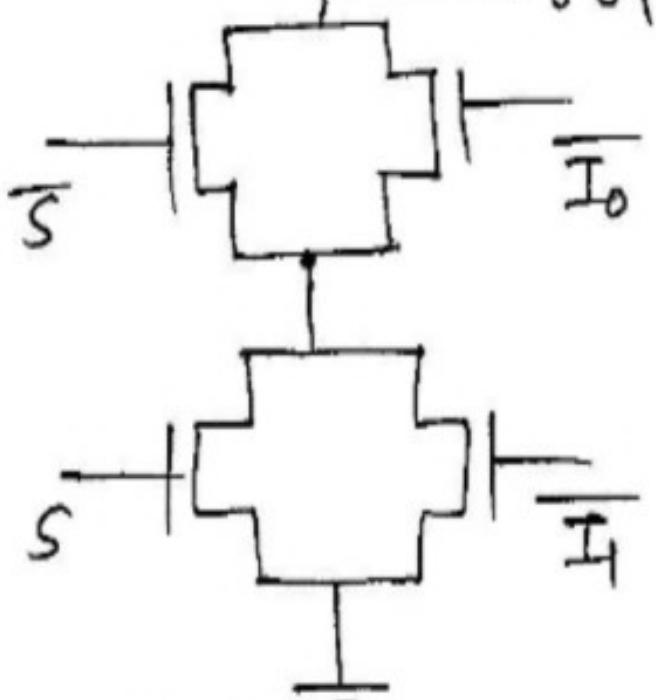


$$\text{As, } Y = SI_0 + \bar{S}I_1$$

Take Double Inversion,

$$\bar{Y} = (\overline{SI_0 + \bar{S}I_1}) = (\overline{\bar{S}I_0}) \cdot (\overline{\bar{S}I_1})$$

$$\bar{Y} = \overline{(\bar{S}+I_0)(S+\bar{I}_1)} = \overline{(\bar{S}+I_0)} \cdot \overline{(S+\bar{I}_1)}$$



When

$$S=1, Y=I_0$$

$$S=0, Y=I_1$$

\therefore we can express as,

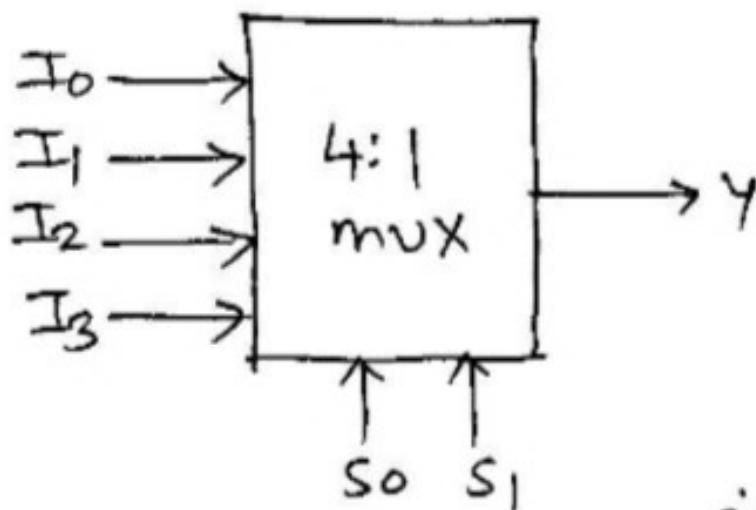
$$Y = SI_0 + \bar{S}I_1$$

$$S=0, Y=I_0$$

$$S=0, Y=I_1$$

$$Y = SI_0 + \bar{S}I_1$$

(e9)

4:1 muxTruth-table

S_0	S_1	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

$$\therefore Y = I_0 \overline{S_0} \overline{S_1} + I_1 \overline{S_0} S_1 + I_2 S_0 \overline{S_1} + I_3 S_0 S_1$$

Note → Take double complement of this eqn $+ I_3 S_0 S_1$

$$\begin{aligned}\therefore \overline{\overline{Y}} &= \overline{(I_0 \overline{S_0} \overline{S_1}) + (I_1 \overline{S_0} S_1) + (I_2 S_0 \overline{S_1}) + (I_3 S_0 S_1)} \\ &= \overline{(I_0 \overline{S_0} \overline{S_1})} \cdot \overline{(I_1 \overline{S_0} S_1)} \cdot \overline{(I_2 S_0 \overline{S_1})} \cdot \overline{(I_3 S_0 S_1)} \\ &= \overline{(\overline{I_0} + S_0 + S_1)} \cdot \overline{(\overline{I_1} + S_0 + \overline{S_1})} \cdot \overline{(\overline{I_2} + \overline{S_0} + S_1)} \cdot \overline{(\overline{I_3} + \overline{S_0} + \overline{S_1})}\end{aligned}$$

⇒ Draw schematic of above eqn.

Advantages of Pseudo n-MOS

- We require $(N+1)$ transistor to implement complex boolean function, where N = number of n-MOS transistor and '1' = number of p-MOS transistor.
- Hence , Less chip area is required.

Disadvantages of Pseudo n-MOS

- As p-MOS transistor is always ON , hence static power dissipation loss is more as compared to static CMOS logic.
static power dissipation loss is more

3.2 Dynamic CMOS Design

C²MOS Logic Circuit

Refer Class Notebook for this topic

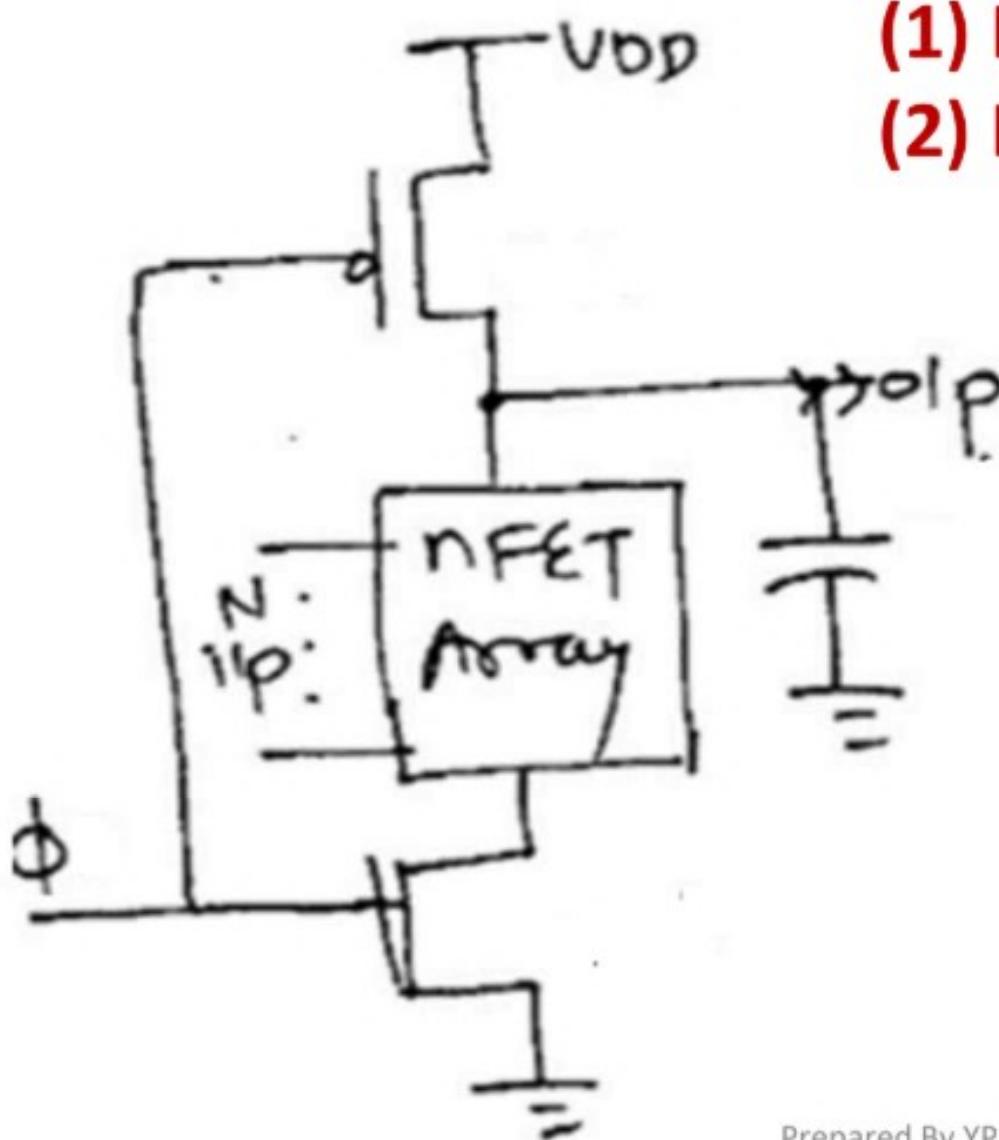
Dynamic Logic Circuit

- It uses clock , thus it enables the synchronization of various circuit blocks.
- It allows construction of sequential circuit also.
- It uses $(N+1)$ transistors , hence less chip area is required compare to static CMOS logic.
- It often dissipates less dynamic power than static logic circuits as parasitic capacitance smaller.

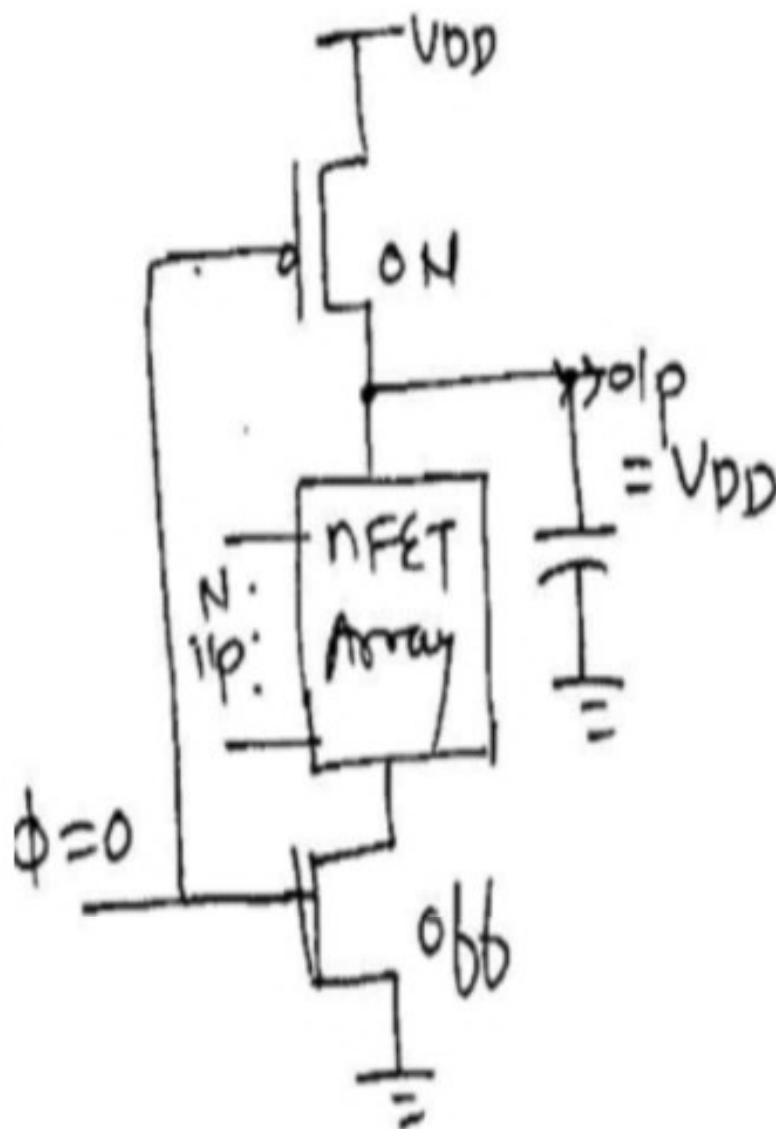
Structure of Dynamic Logic Circuit

➤ The operation of circuit involves two phases,

- (1) Precharge ($\phi = 0$)
- (2) Evaluation ($\phi = 1$)



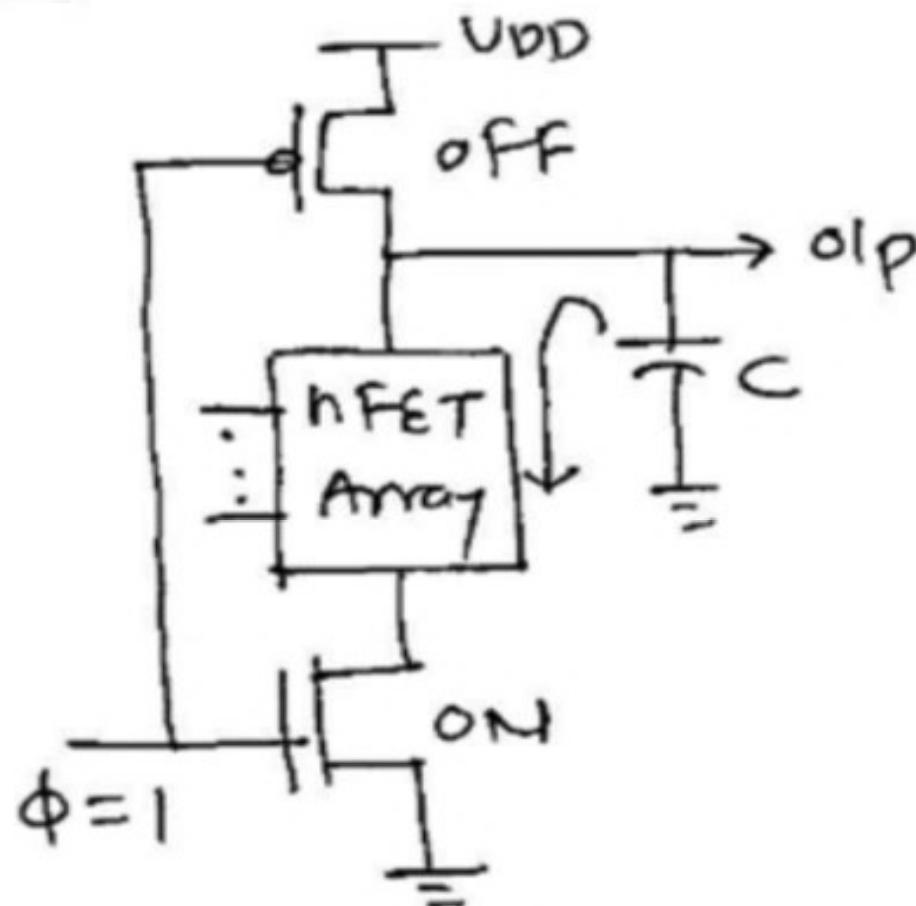
(1) Precharge phase



- During this phase, clk value is low ($\phi = 0$), making p-MOS transistor ON & n-MOS transistor OFF.
- Since p-MOS transistor is ON It drives the o/p node voltage to V_{dd} by charging the o/p capacitor and hence called as Precharge phase.

(2) Evaluation phase

- During this phase, clk value is low ($\phi = 1$) , making n-MOS transistor ON & p-MOS transistor OFF.
- The inputs are actually evaluated during this phase.
- Depending upon the combination of applied inputs , the nFET arrays are either ON or OFF.



Case 1 :- When n-FET array is closed

- If n-FET array is closed then capacitor C gets discharged path to the ground , hence the o/p voltage is zero.

Case 2 :- When n-FET array is open

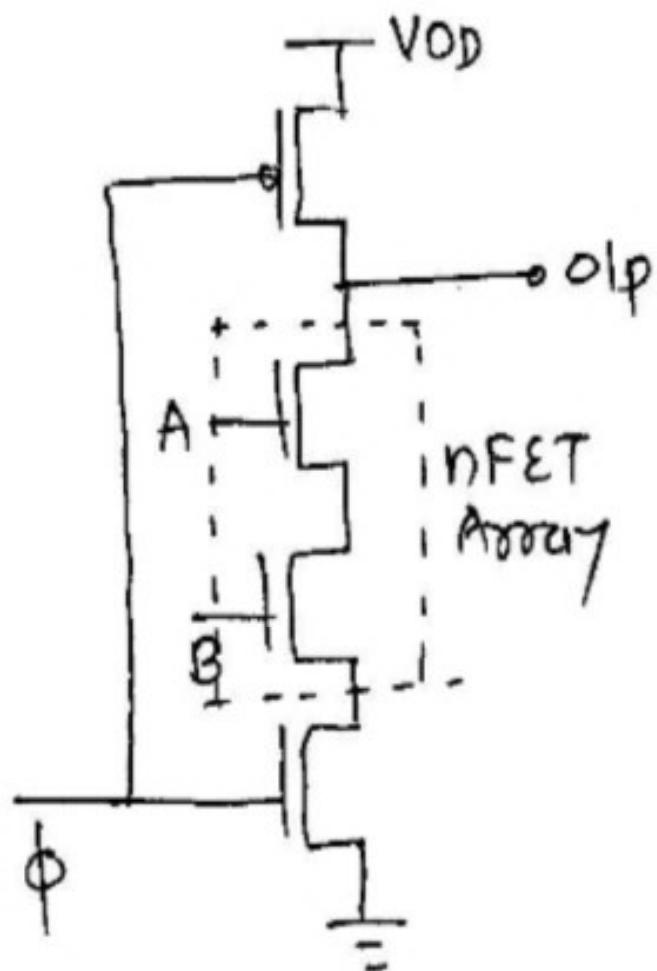
- If n-FET array is open, then capacitor C does not get any discharge path to the ground , hence o/p voltage retained at the high value.

⑨ Realize 2 iip NAND gate using Dynamic Logic
 & 2 iip NOR gate



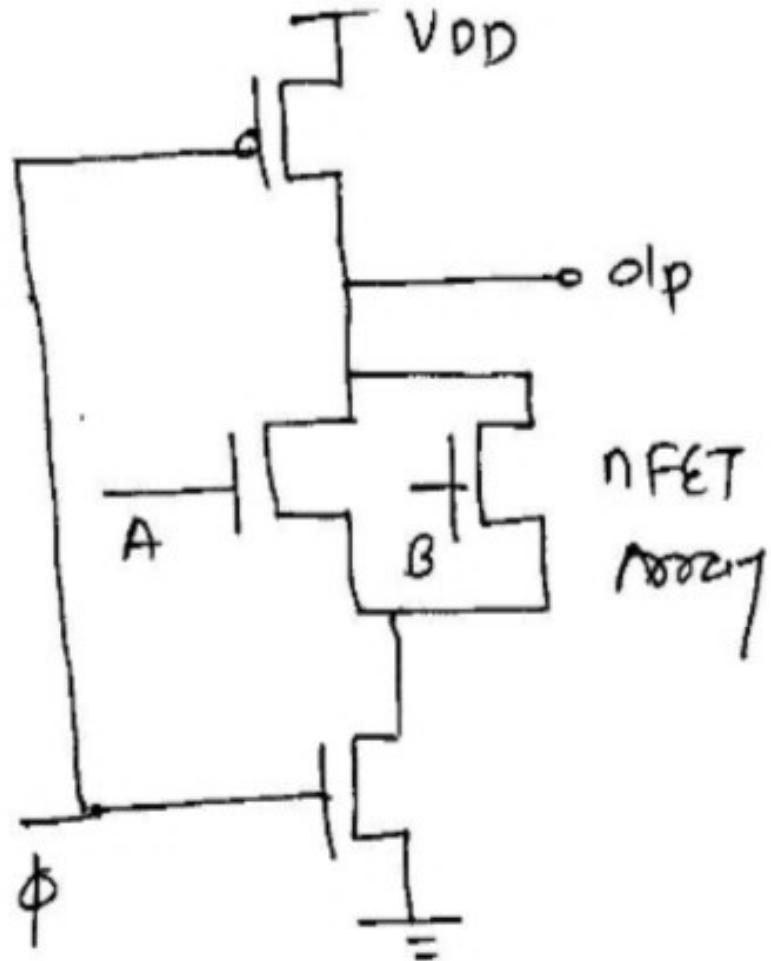
NAND gate

$$Y = \overline{AB}$$



NOR gate

$$Y = \overline{A+B}$$



③ AND gate $y = AB$
 Take double complement
 $\therefore y = \overline{\overline{AB}}$
 $y = \overline{\overline{A} + \overline{B}}$

④ OR Gate $y = A + B$
 $\bar{y} = (\overline{\overline{A} + \overline{B}})$
 $= \overline{(\overline{A} \cdot \overline{B})}$

Implement above functn. in nFET Array

⑤ XOR Gate
 $f = \overline{AB} + \overline{A}\overline{B}$
 $f = (\overline{A}\overline{B} + \overline{A}\overline{B})$
 $= (\overline{\overline{AB}}) \cdot (\overline{\overline{AB}})$
 $f = \overline{(\overline{A} + B) \cdot (\overline{A} + \overline{B})}$

⑥ XNOR Gate
 $f = AB + \overline{AB}$
 $= (\overline{AB} + \overline{AB})$
 $= \overline{(\overline{AB}) \cdot (\overline{\overline{AB}})}$
 $f = \overline{(\overline{A} + \overline{B}) \cdot (A + B)}$

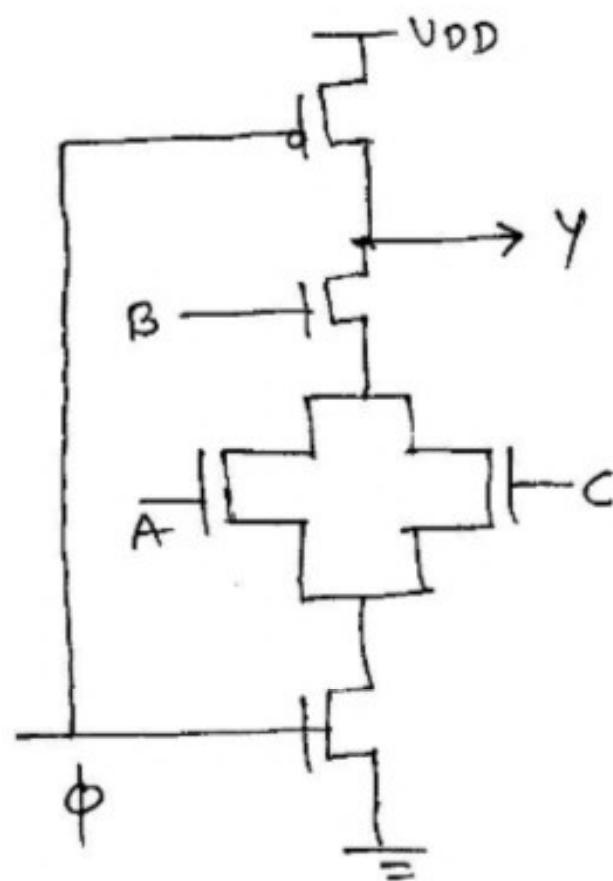
Note Implement above functions in nFET Array.

Improve
 \Rightarrow Implementation of 2:1 mux & 4:1 mux, pls refer
pseudo nmos logic
 \rightarrow nFET array logic is same.
Prepared by S. A. M. J. T.

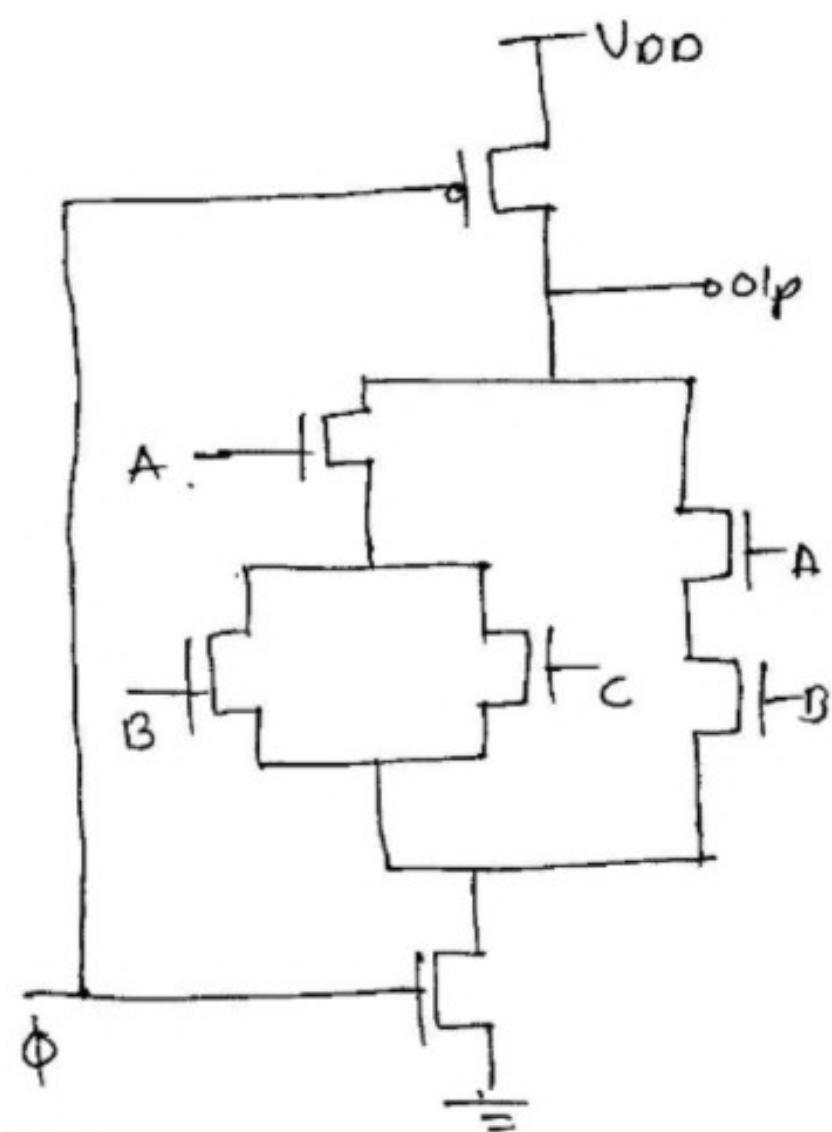
Q9) Implement the following funcn using dynamic logic

① $Y = \overline{AB + BC}$

Soln $\rightarrow Y = \overline{B(A+C)}$



② $Y = \overline{AB + A(B+C)}$

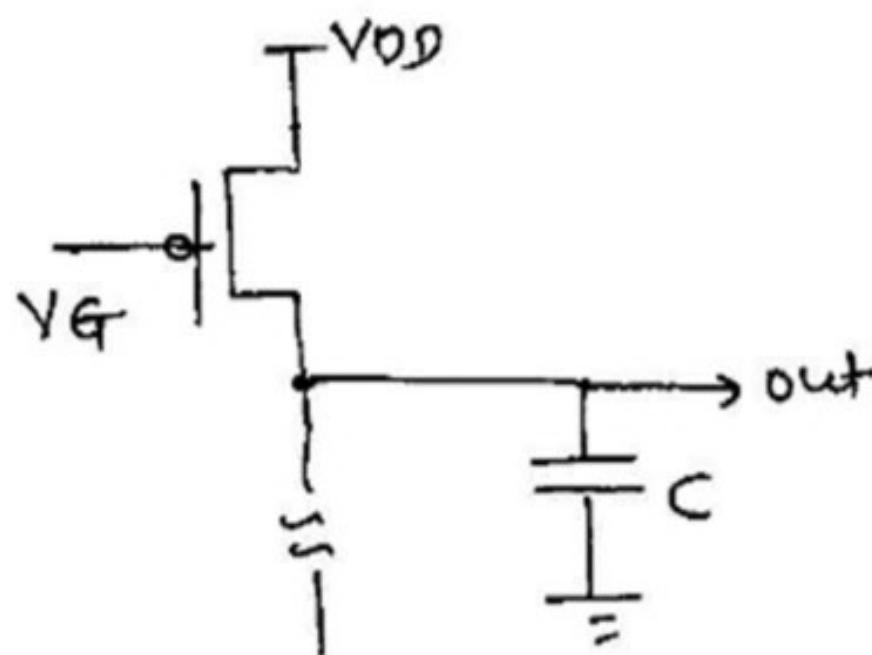


Disadvantages of Dynamic CMOS

(1) Charge Leakage :-

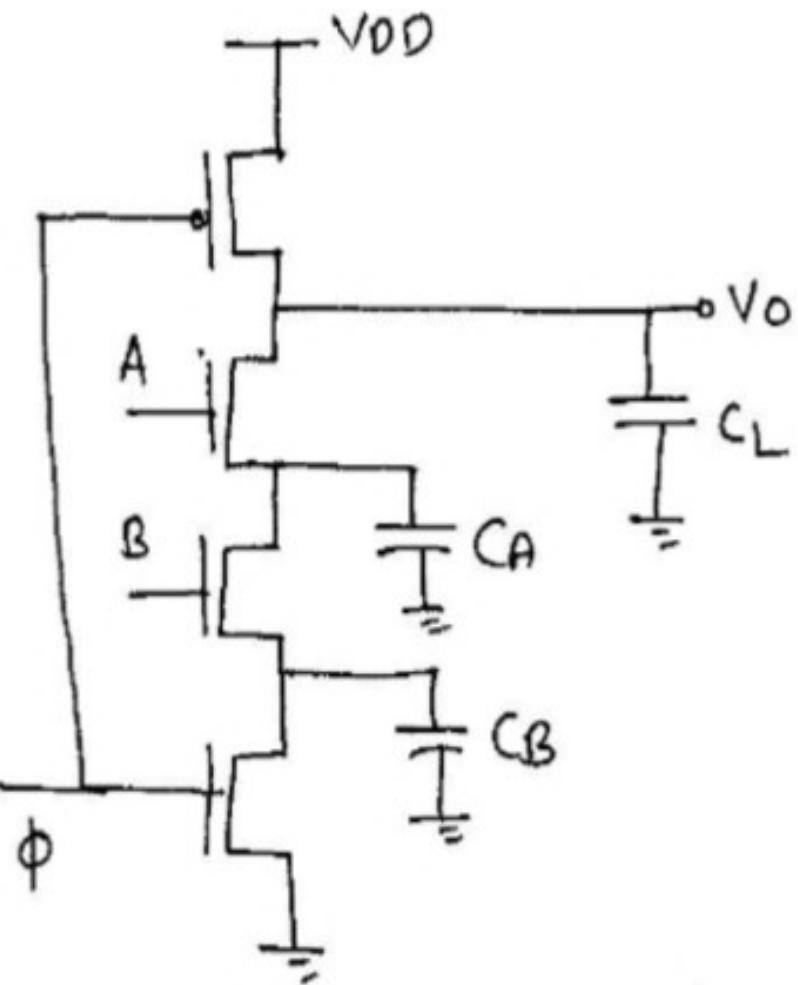
- MOSFET becomes open circuit when $V_{GS} < V_{T,n}$ and ideally no current flows through it & capacitor holds the charge.

- But, practically small current always flows through it which causes the voltage across capacitor to reduce.



(2) Charge Sharing :-

- This problem is due to the Parasitic capacitance inherently associated with the MOSFETs.

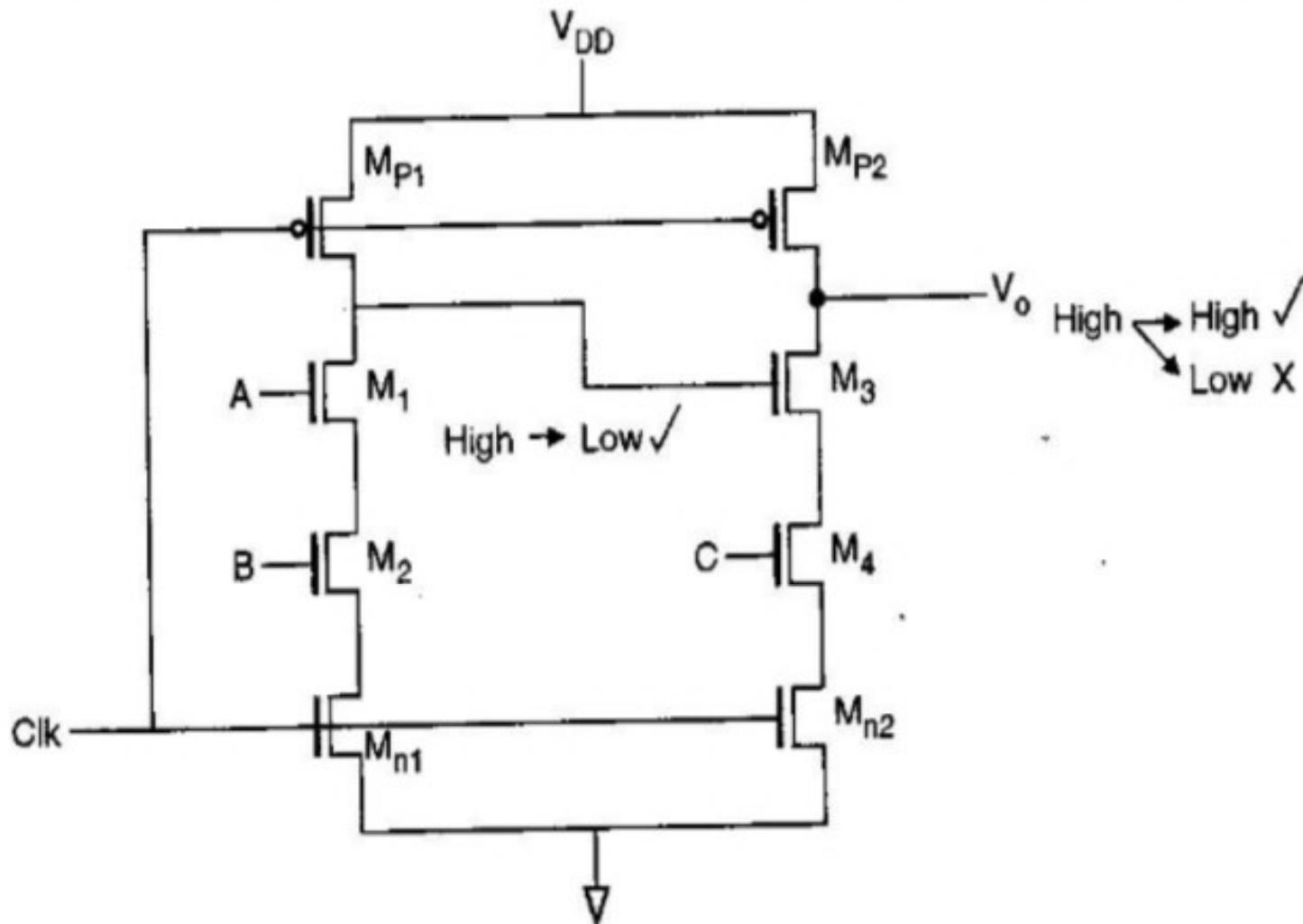


- Thus, the o/p voltage is shared among the capacitors.
- As shown in fig, assume that during Precharge phase the capacitor C_L is charged to V_{dd} .
- Let, during the Evaluation phase $A=1$ and $B=0$, thus n-FET array is off & o/p remains high.

But, as MOSFET 'A' is ON due to $i/p = 1$, capacitor C_A & C_L appears in parallel, thus o/p voltage $V_o = C_L V_{dd} / (C_A + C_L)$ is reduced. This leads to wrong state and called as Charge sharing problem.

(3) Race Problem:-

- It is the timing problem that comes into picture during Cascading dynamic logic gates. (ie o/p of the 1st stage is serving as i/p to the next stage.)
- Following fig. shows race problem in dynamic logic

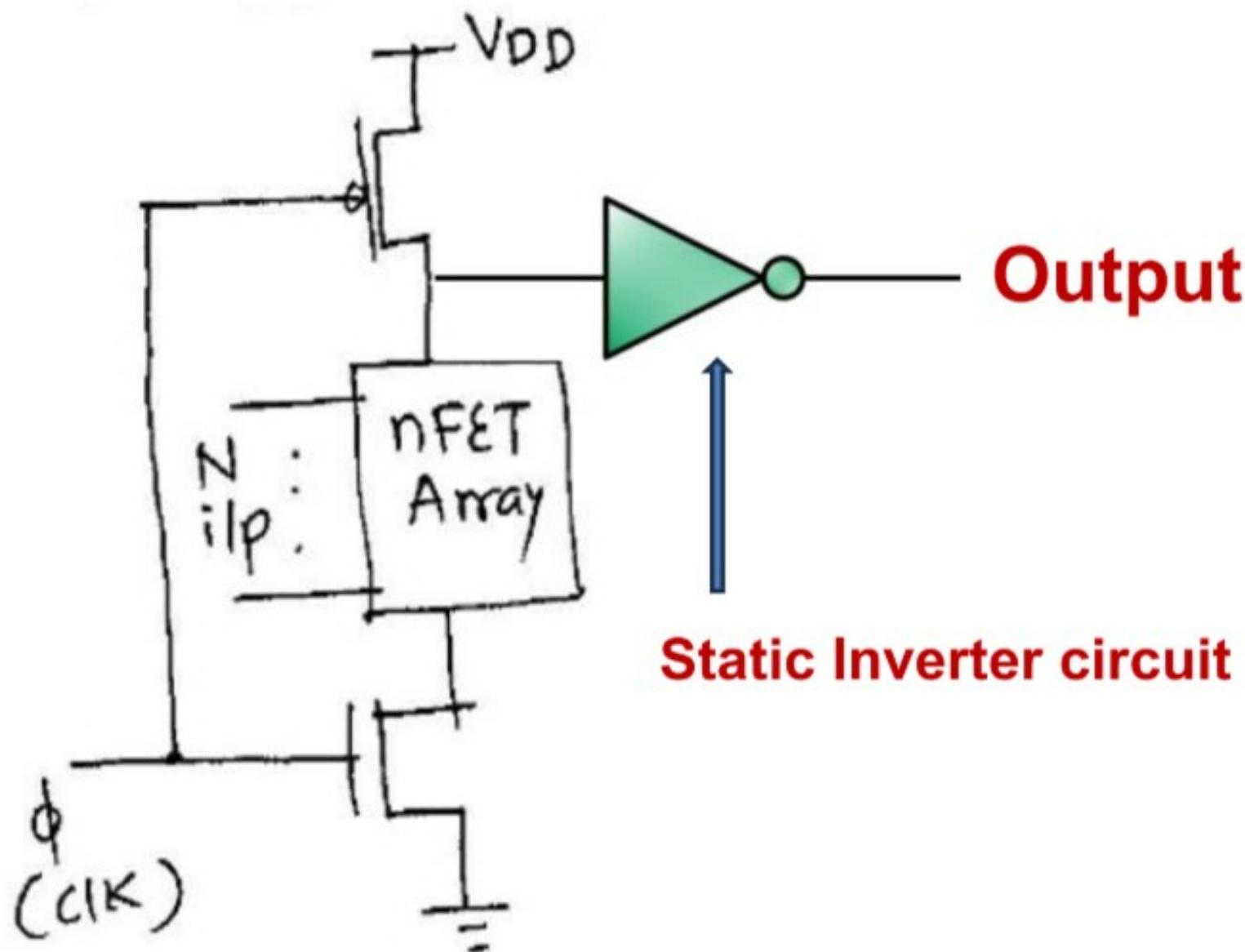


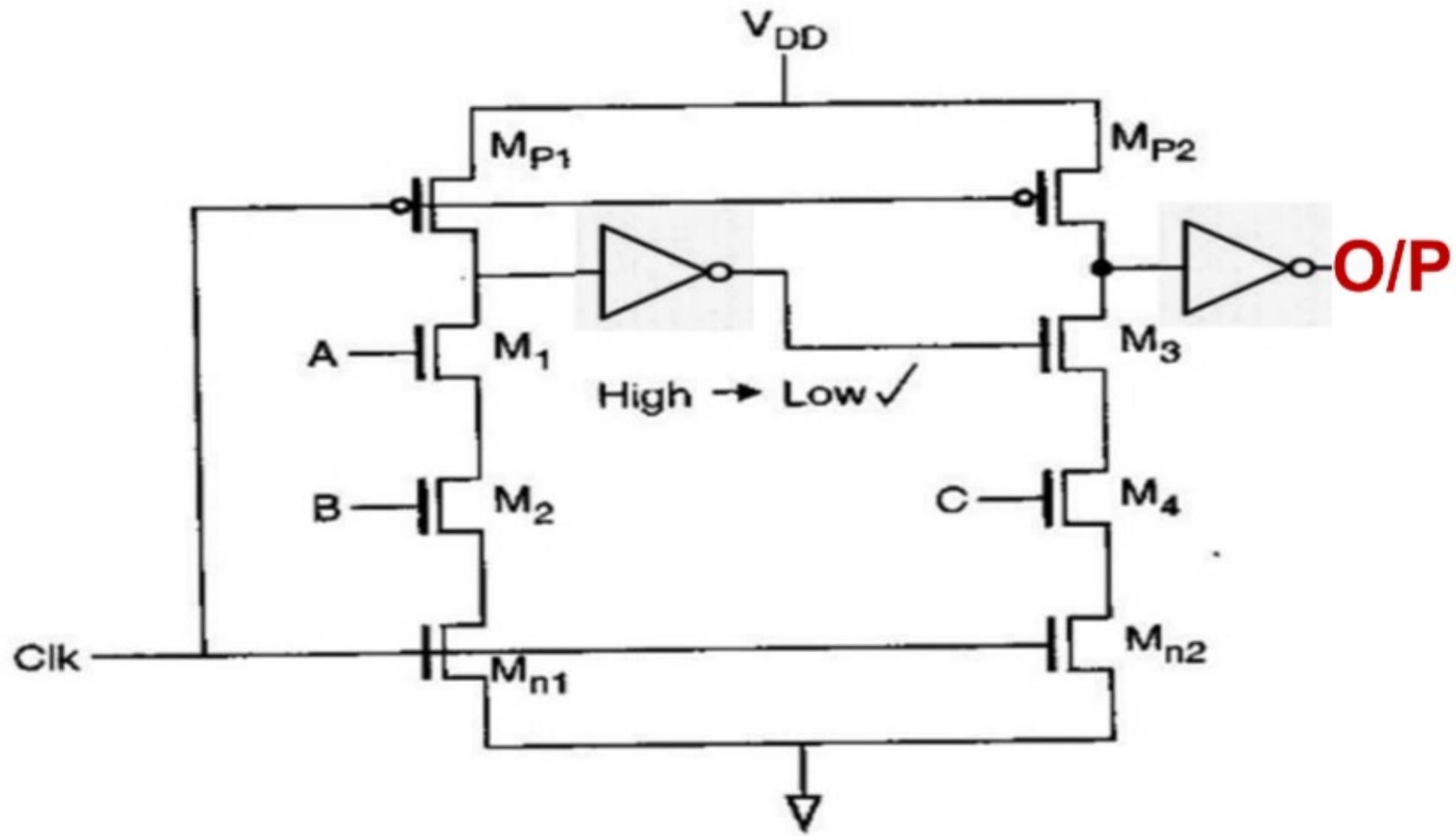
- When clk is low (ie Precharge phase) , the o/p of both the stages are Precharge to Vdd.
- During, the evaluation phase, inputs A,B & C all are high. Therefore , during the evaluation period, since A and B are high will drive the o/p of first stage to low value. Now o/p of first stage is going to i/p to second stage transistor M3, so o/p of M3 is supposed to be logic high.
- However if the propagation delay of the first stage is long, at the very beginning of the evaluation period, the o/p of second stage accidentally switched to low, as the i/p connecting from the o/p of first stage can not turn low instantaneously because of propagation delay.
- As a result an enormous state is produced at the o/p of the second stage. Once the o/p is pulled low, during this logic evaluation period , it can not be pulled high again.
- To overcome the race problem , connect an inverter at the o/p the all stages & resulting circuit is called as Domino logic circuit.

Domino Chain Reaction



Domino Logic Circuit



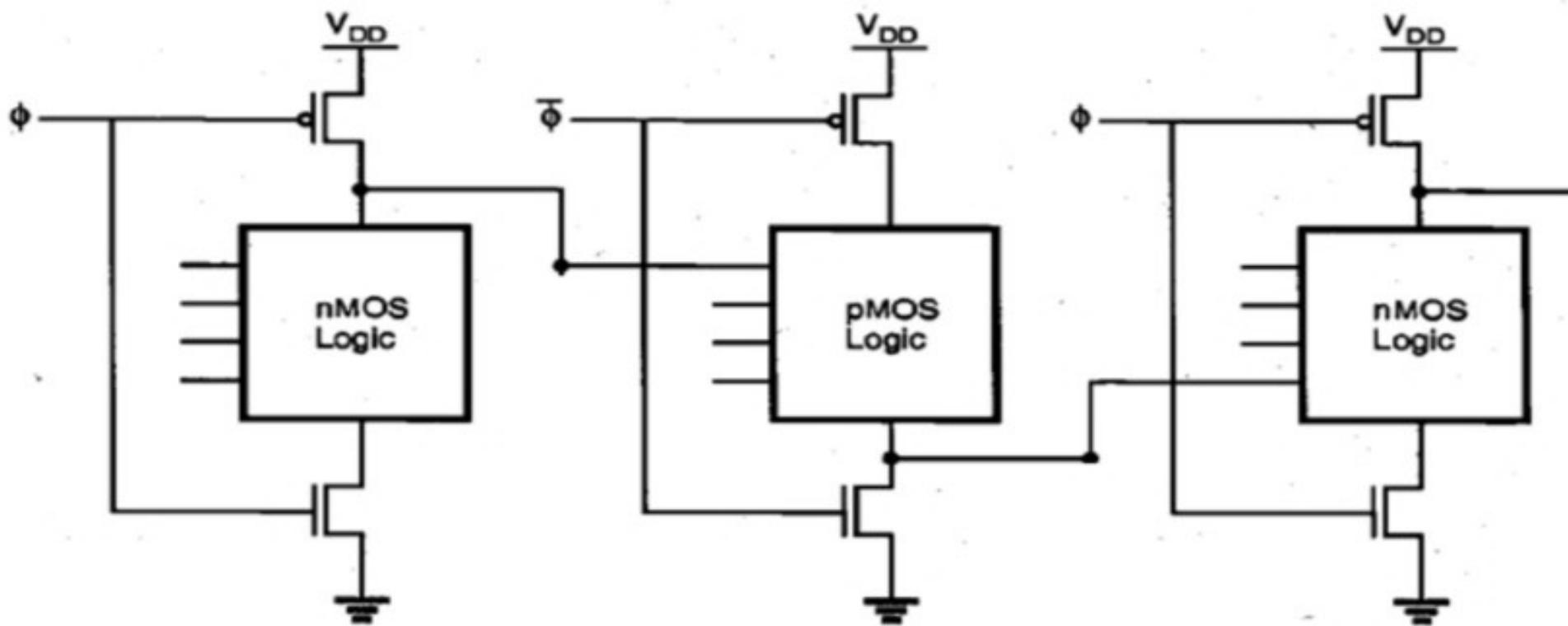


Disadvantage :-

- We get delayed output of the circuit.
- Need of static inverter increases the chip area.

NORA (No Race) / NP Domino Logic

It consists of alternate connection of n-MOS and p-MOS transistors as shown below.

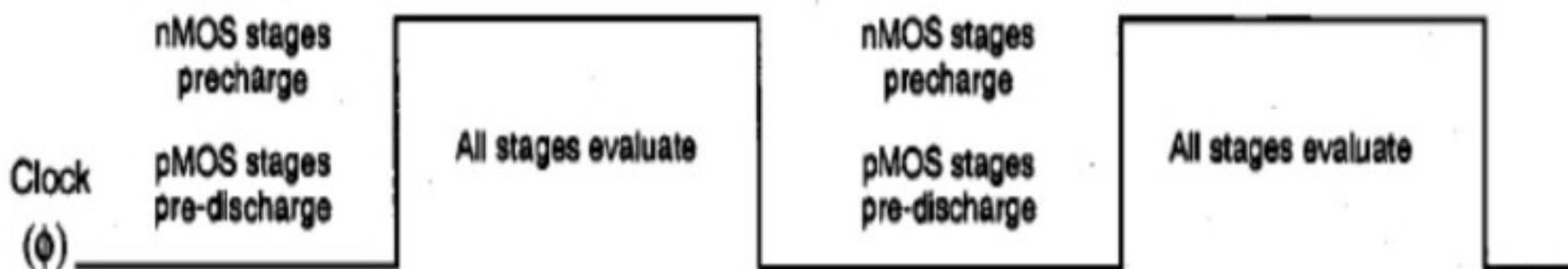


As shown in figure, the precharge and evaluate timing of nMOS logic stage is accomplished by clock signal ' Φ ' while pMOS logic stages are controlled by $\bar{\Phi}$.

Operation –

- When $\Phi=0$, the output nodes of nMOS logic blocks are precharge to VDD through pMOS precharge transistor, whereas the output nodes of pMOS logic blocks are precharged to 0V through the nMOS discharge transistor, driven by Φ .
- When $\Phi=1$, all cascaded nMOS and pMOS logic stages evaluate one after the other.

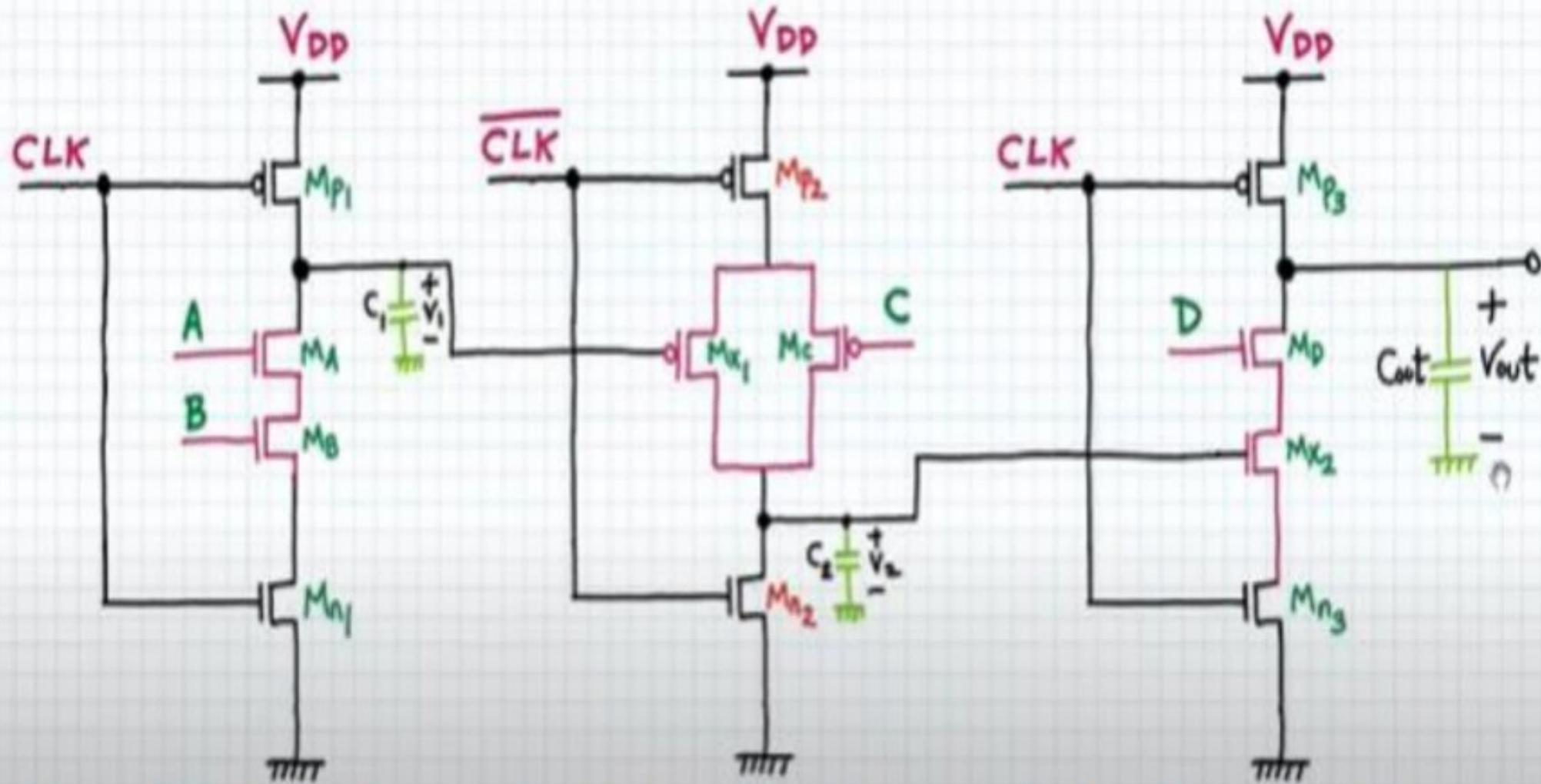
Following fig. shows scheduling of precharge and evaluation phases.



Implement $Y = \overline{A+B} \cdot C + D \cdot E$ using NORA logic

Refer Class Notebook

Implement $Y = \overline{(A \cdot B)} \cdot C \cdot D$ using NORA logic



NMOS Dynamic Logic

PMOS Dynamic Logic

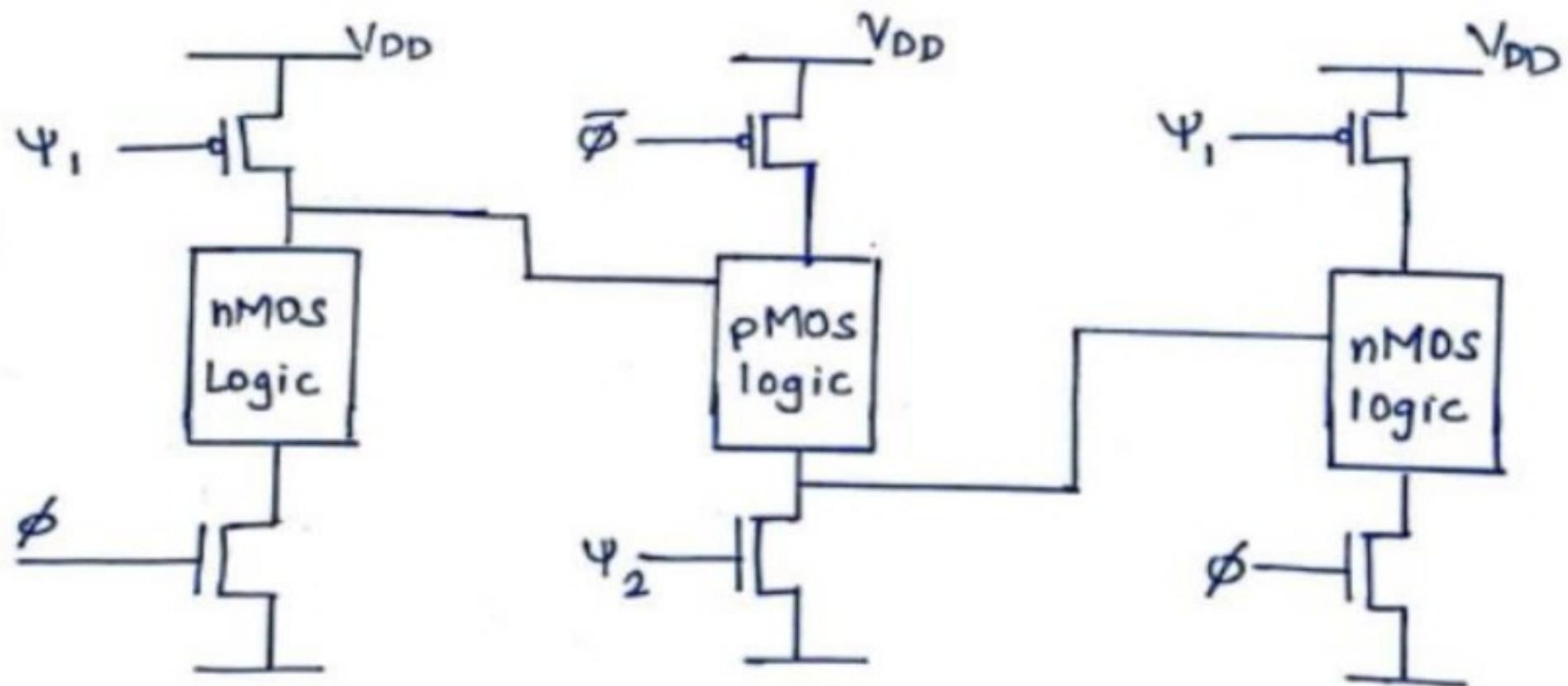
NMOS Dynamic Logic

Disadvantages of NORA Logic

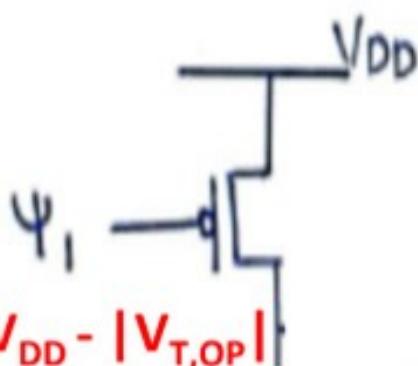
- Charge sharing and charge leakage.
- Hence to overcome this problem, Zipper logic is used.

Zipper Logic

- Zipper logic is a scheme for improving charge leakage and charge sharing problems.
- It is identical to NORA logic except the clock signals.
- It receives a slightly different clock signals for the pre-charge (discharge) transistors and for pull down (pull up) transistors.
- Clock signals which drive pMOS precharge and nMOS discharge transistors, allow the transistors to remain in weak conduction or in cutoff during evaluate phase, thus compensating for charge sharing and charge leakage problems.
- pMOS pre-charge transistors gates are held at $V_{dd} - |V_{tp}|$
- nMOS pre-charge transistors gates are held at V_{tn} above GND.

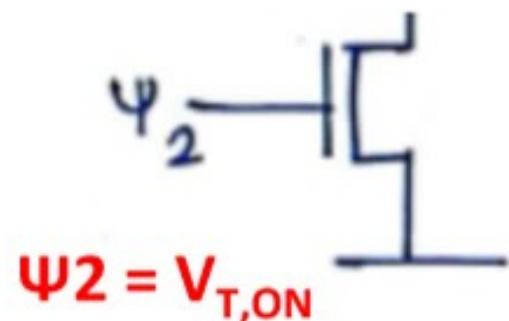


- Zipper CMOS logic generates 4 different clock signals.
- Ψ_1 & Ψ_2 used for pre-recharge / pre-discharge phase.
- ϕ & ϕ' used during evaluation phase.
- When $\phi=0$, $\phi' = V_{DD}$; $\Psi_1 = 0$, $\Psi_2 = V_{DD}$
- When $\phi=V_{DD}$, $\phi' = 0$; $\Psi_1 = V_{DD} - |V_{T,OP}|$, $\Psi_2 = V_{T,ON}$



$$\begin{aligned}V_{GS} &= V_G - V_S \\&= V_{DD} - |V_{T,OP}| - V_{DD} \\V_{GS} &= |V_{T,OP}|\end{aligned}$$

(ie. PMOS is near cut-off ie. Weak conduction)



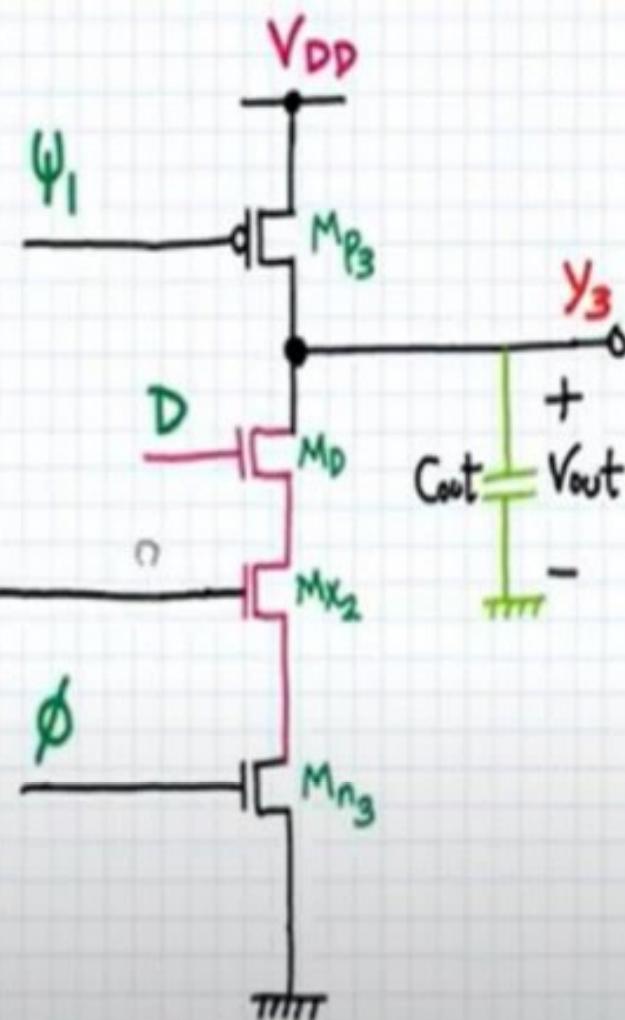
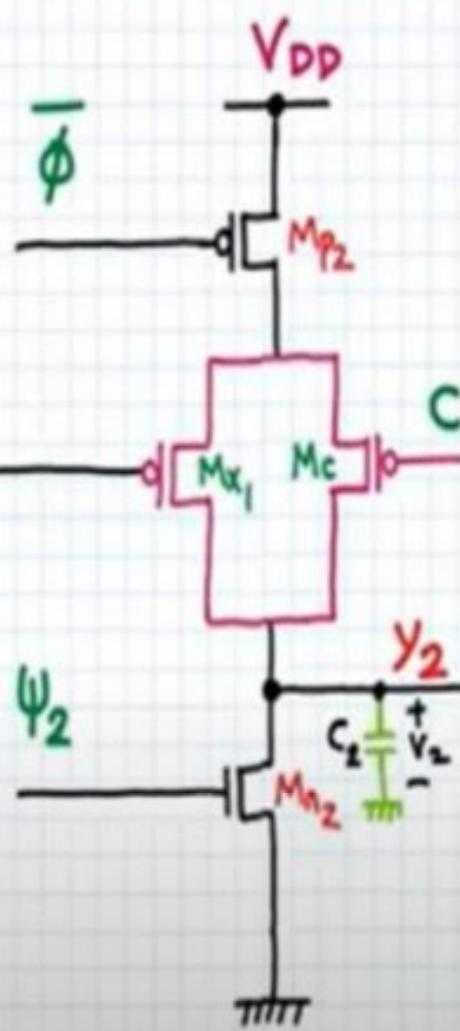
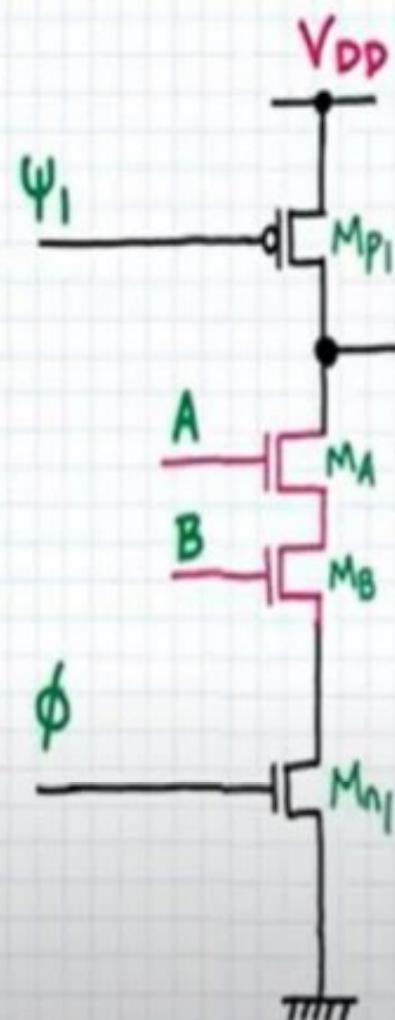
$$\begin{aligned}V_{GS} &= V_G - V_S \\&= V_{T,ON} - 0 \\V_{GS} &= V_{T,ON}\end{aligned}$$

(ie. NMOS is near cut-off ie. Weak conduction)

This shows that None of the transistor is completely in OFF state

Zipper Logic

Implement $Y = (\bar{A} \cdot B) \cdot C \cdot D$ using Zipper logic



Thank
you!

