Module 5:-
Semiconductor Memories

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5.1 SRAM: 6T SRAM operation, design strategy, read/write circuits, sense amplifier.

5.2 DRAM: 1T DRAM, operation modes, leakage currents, refresh operation, physical design.

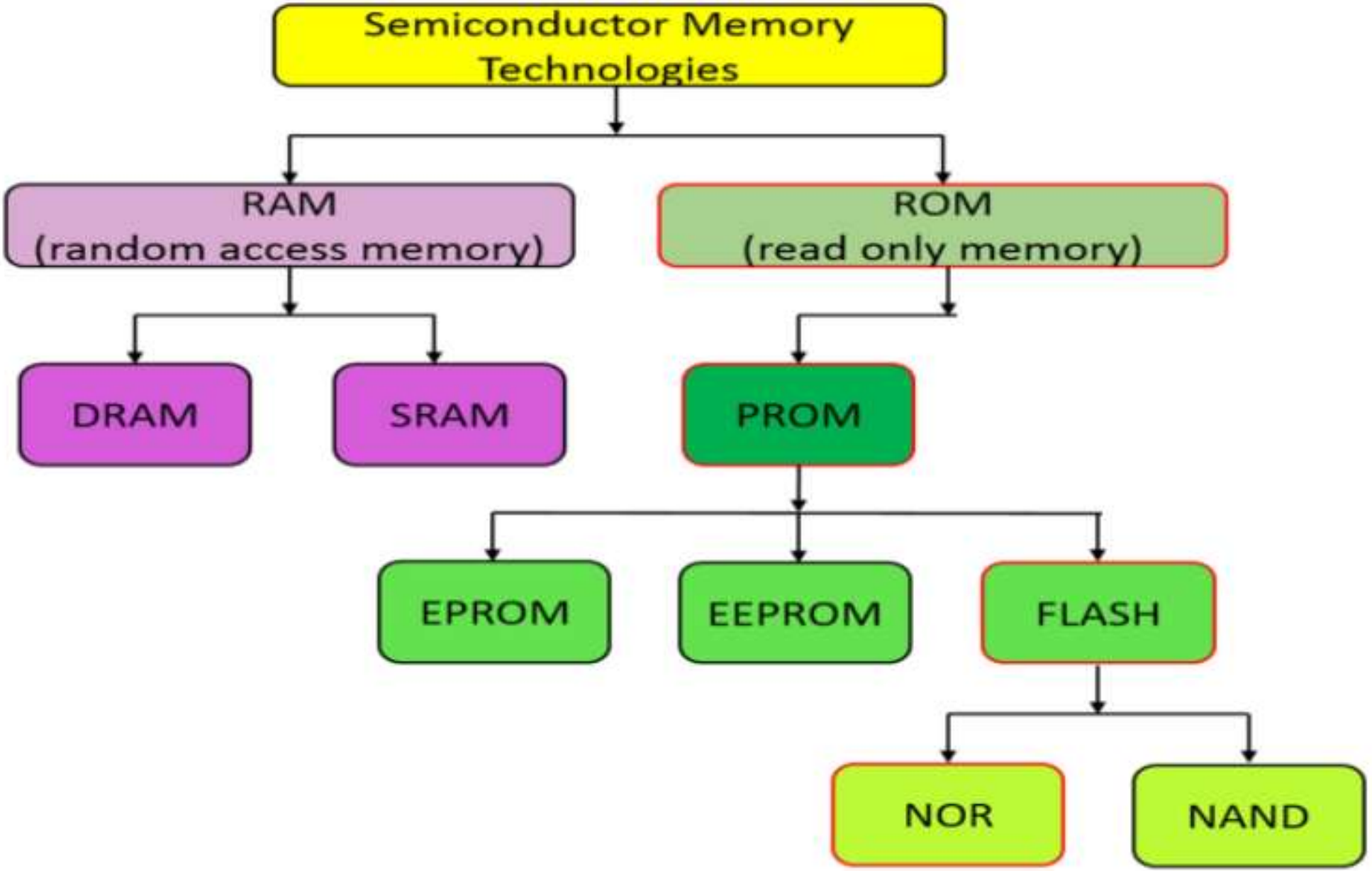
5.3 ROM Array: NAND and NOR based ROM array.

5.4 Flash Memory: F-N tunnelling

Semiconductor Memory

- Semiconductor memory array capable of storing large quantities of digital information are essential to all digital systems.
- The amount of memory required in a particular system depends on the type of application , but in general the number of transistors required for data storage is much larger than the number of transistors used for logical operations & other purpose.
- The maximum realizable data storage capacity of single chip semiconductor memory arrays approximately doubles every two years.
- Designing compact memories with high storage capacity , low power consumption & high access speed are the impinging issues in the memory design.

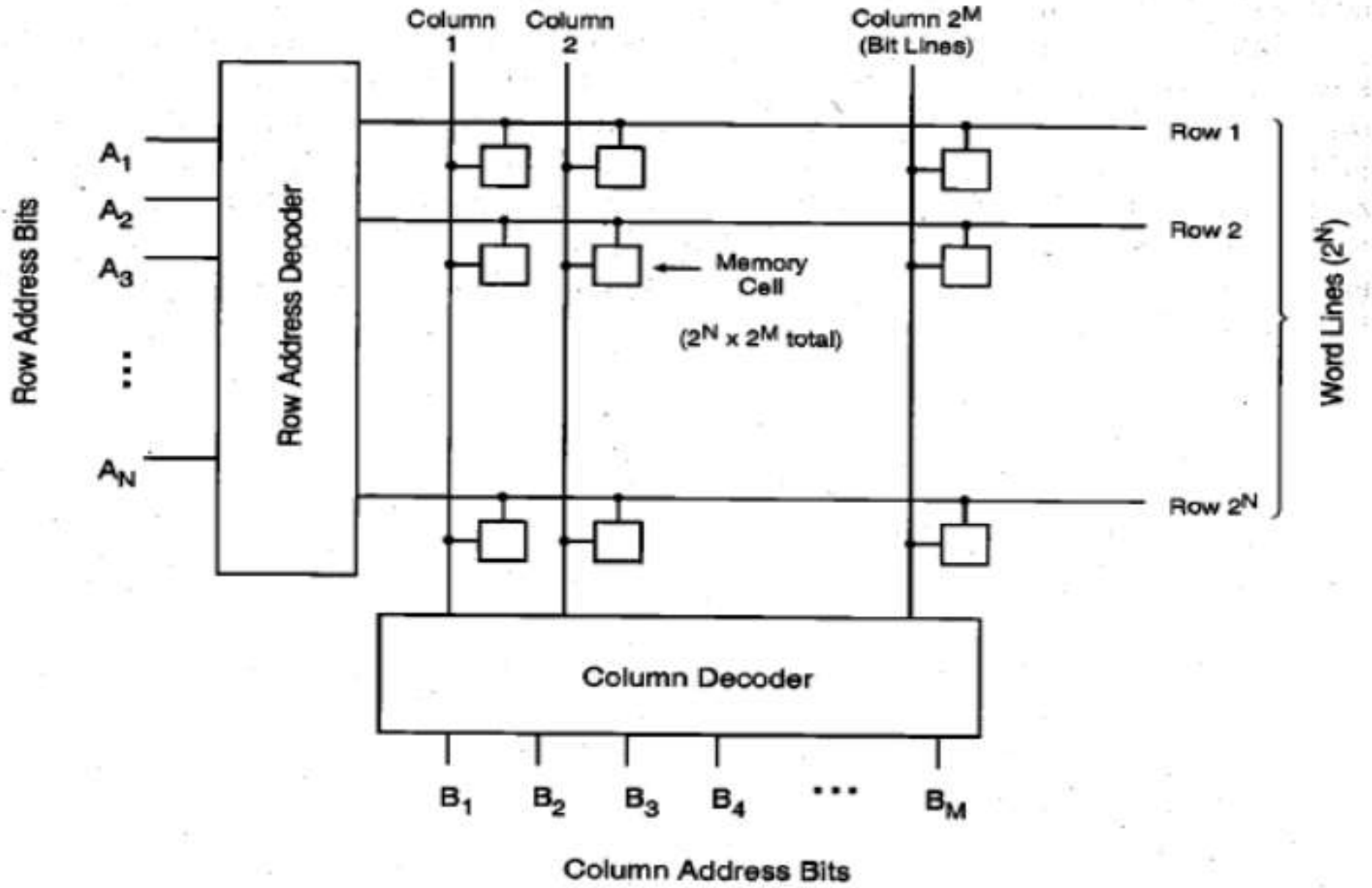
Classification of Semiconductor Memory

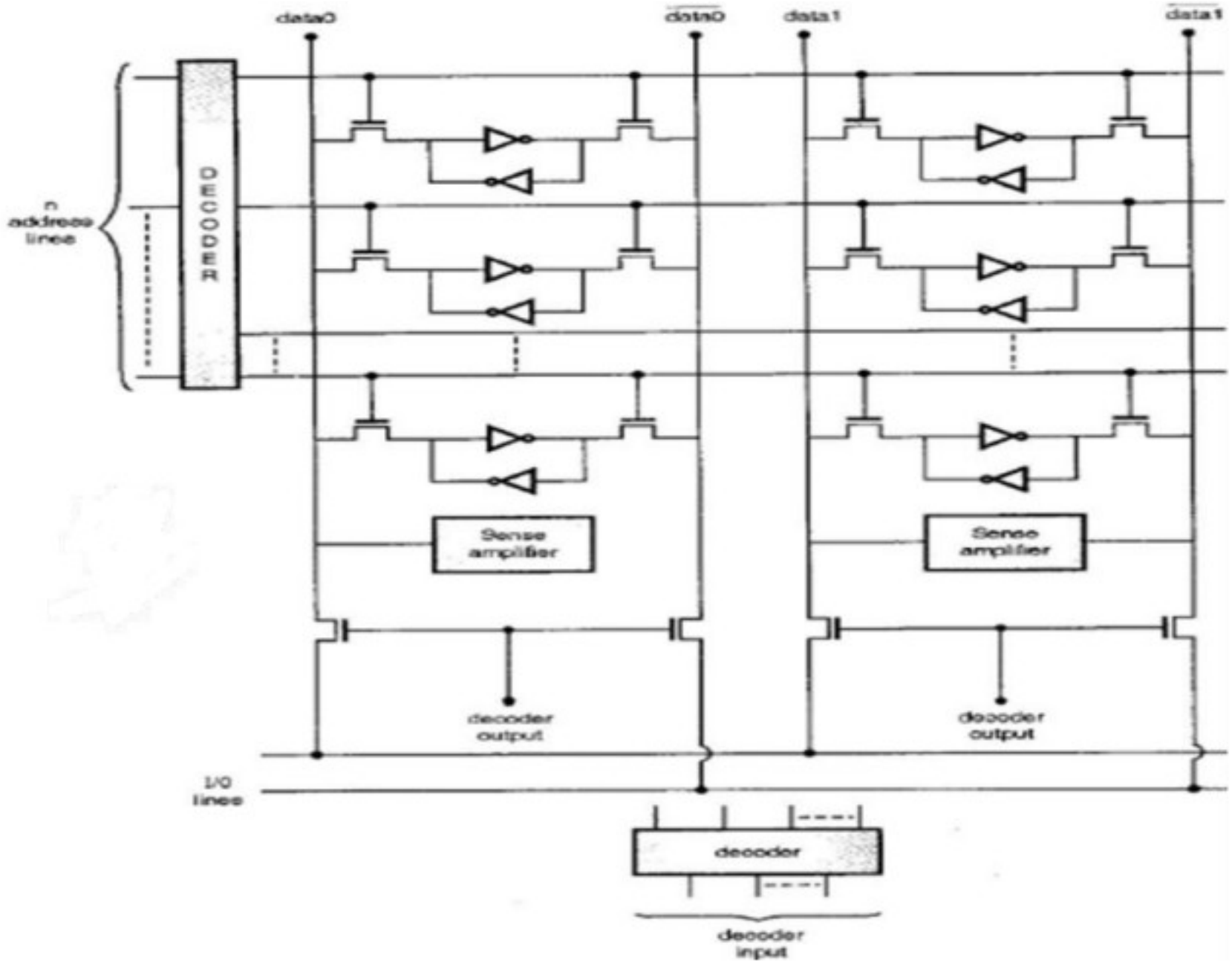


Difference between RAM and ROM

RAM	ROM
Read and Write memory	Read only memory
It is Volatile memory ie. If power is off then RAM will loose the stored data.	It is non-volatile memory ie. If power is off then also ROM can retain the data.
Some types of RAM (Dynamic) requires Refresh operation	It does not require the Refresh operation

RAM array organization



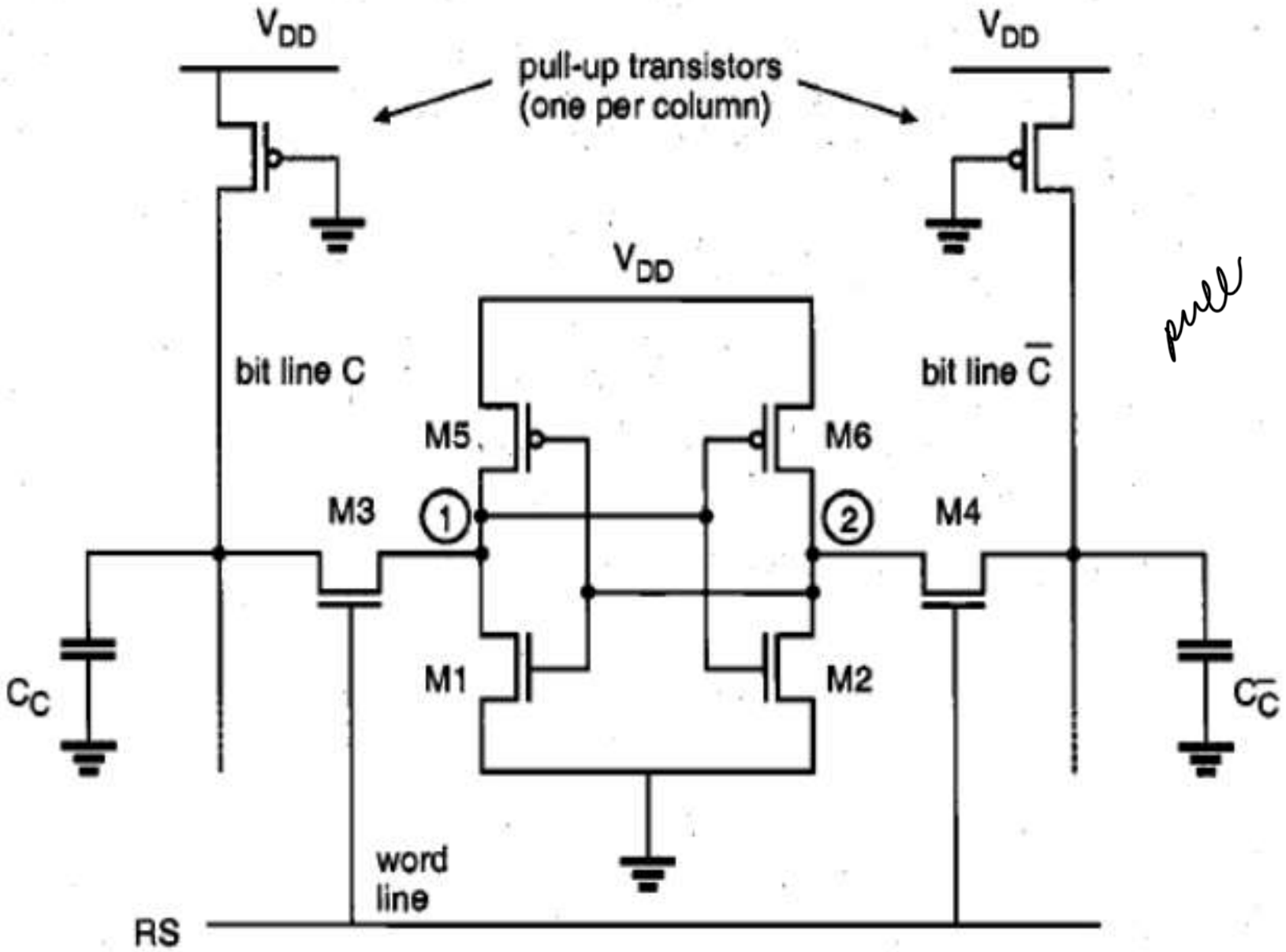

data0
data0
data1
data1
n address lines
DECODER
Sense amplifier
Sense amplifier
decoder output
decoder output
I/O lines
decoder
decoder input

- As shown in fig, it consist of individual memory cells arranged in an array of horizontal rows and vertical columns.
- Each cell is capable of storing one bit of binary information.
- It has 2^N rows called as word lines & 2^M columns called as bit lines. Thus total number of memory cells in this array is 2^N X 2^M.
- The memory cell at each junction consist of two inverters connected back to back with feedback & two pass transistors acting as a access transistor.
- To access a particular memory cell, the corresponding word line & corresponding bit line must be activated according to the address coming from both the decoders.
- Once memory cell or group of memory cell is selected a data read or write operation is performed on the selected single or multiple bits on a particular row.
- Sense amplifiers are used to sense the information stored in the memory cell during the read operation & then based on that it drives the data lines to full signal range once sensed.
- Differential amplifier could use as a sense amplifier.

Static RAM

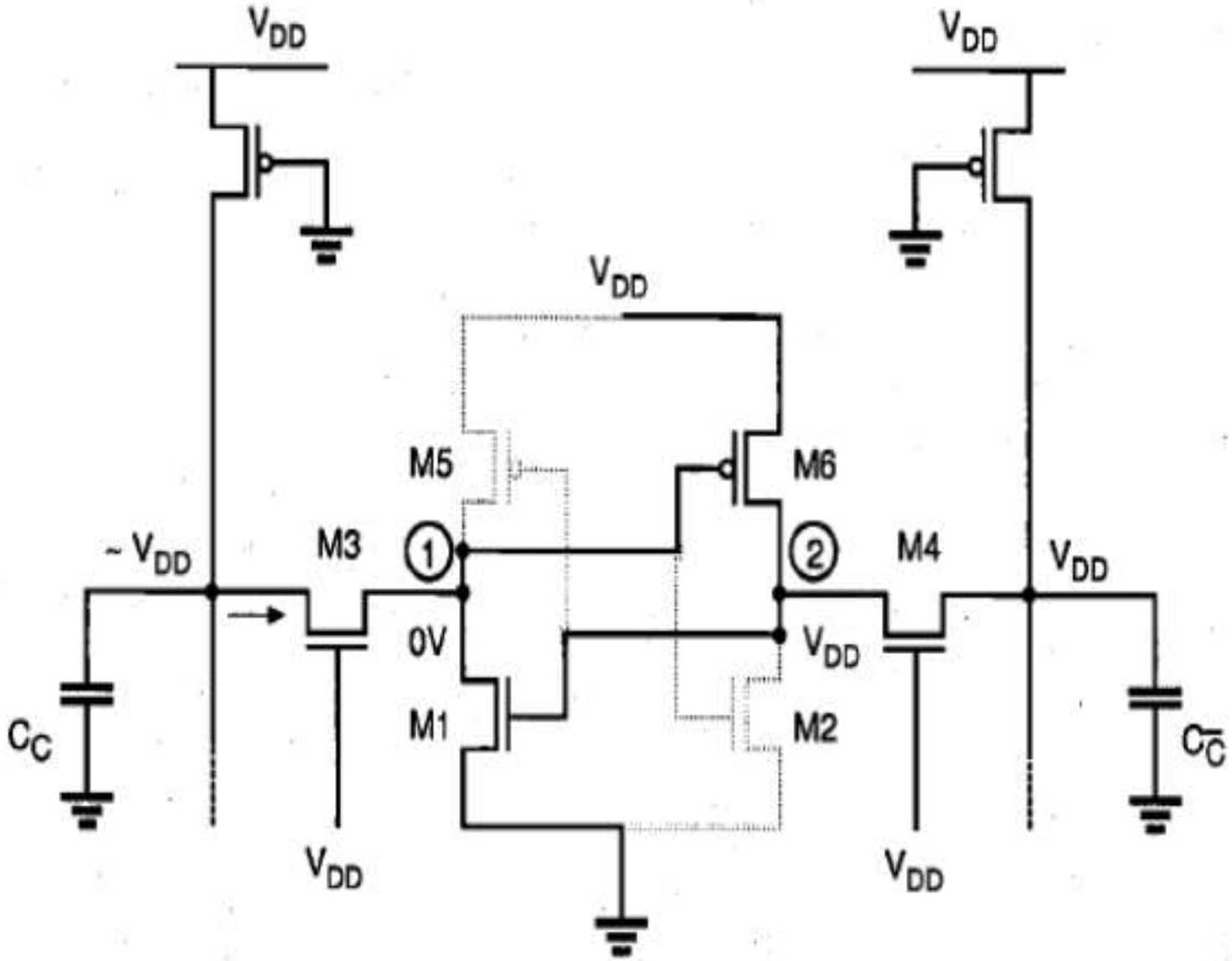
- It stores the information depends on the state of transistor as long as power supply voltage is provided, without any need for periodic refresh operation.
- Static RAM cell consist of two cross coupled inverters which simply acts as a Latch circuit with two stable states.
- It also consist of two complementary access transistors M3 and M4.
- The access transistors are turn ON whenever a word line (Row) is activated for Read or Write operation, connecting the cell to the complementary bit-line columns.

Static RAM cell topology



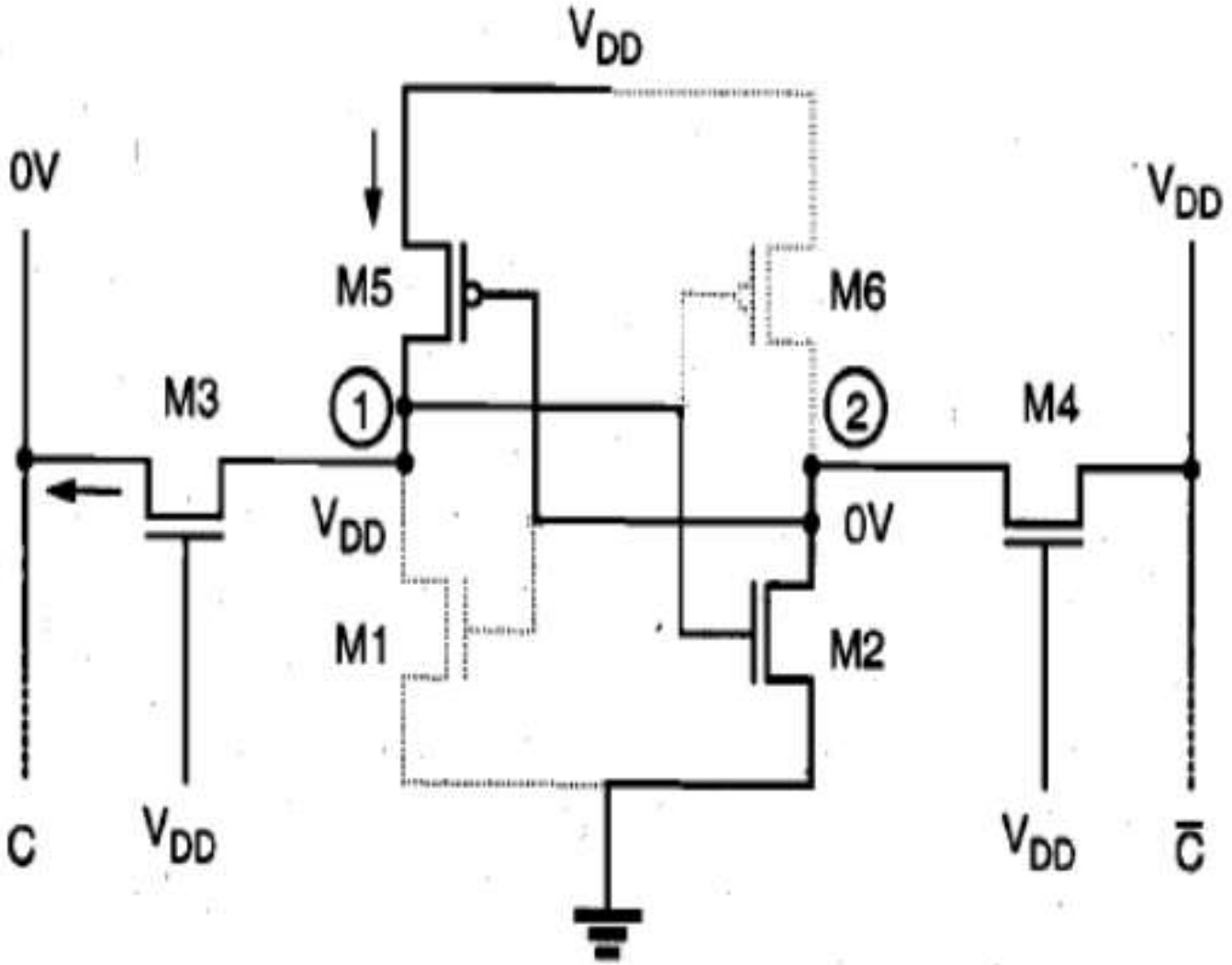
pull

Data Read operation



- Assume that logic 0 is stored in the cell, ie V1=0 v and V2=Vdd , hence transistor M1 & M6 operates in linear mode and transistor M2 & M5 remains OFF.
- Thus, internal node voltages are V1=0V and V2=Vdd before the cell Access transistor M3 & M4 are turned ON.
- After the access transistor M3 & M4 turned ON by Row selection circuitry, the voltage level of column C' will not show any significant variation.
- On the other half of the cell,M3 & M1 will conduct a non zero current and voltage level of column C will begin to drop slightly.

Data Write operation



- Consider we have to write Zero, into the cell assuming that logic 1 is stored in SRAM cell initially.
- Transistor M2 & M5 are in linear mode while transistor M1 & M6 are turned OFF.
- Thus, the internal node voltages are V1=Vdd & V2=0 V before the access transistor M3 & M4 are turned ON.
- The column voltage Vc is forced to logic 0 level by the data write circuitry, thus Vc is approximately Zero volt.
- Once the access transistor M3 & M4 are turned ON by the Row selection circuitry, we expect that the node voltage V2 remains below the threshold voltage of M1 , and is insufficient to turn on M1 transistor.
- To change the stored information ie.to force V1 to 0 V and V2 to Vdd, the node voltage V1 must be reduced below the threshold voltage of M2 so that M2 turns OFF first & this will guarantee that M1 subsequently turn ON, changing the stored information.

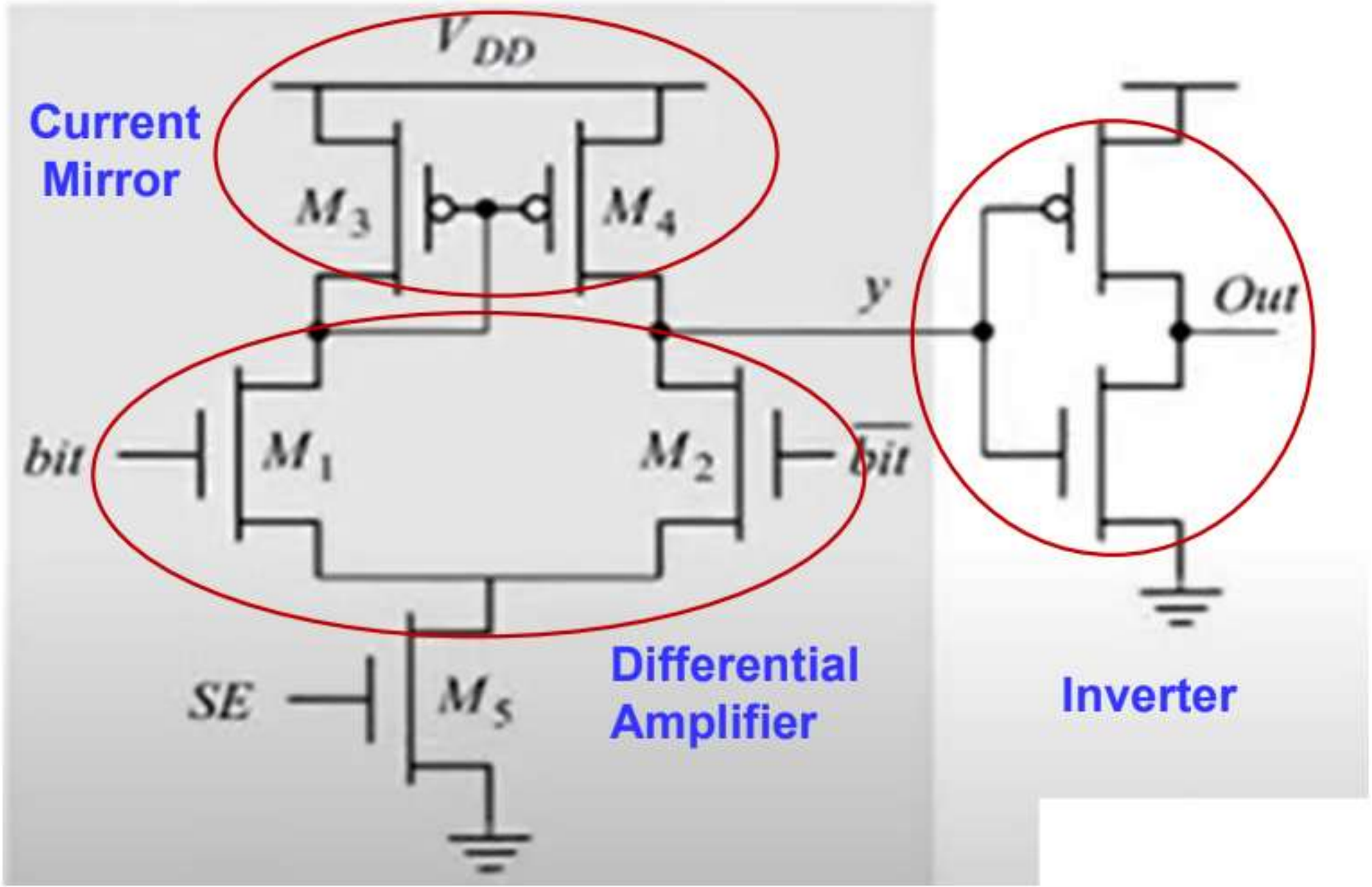
Sense Amplifier

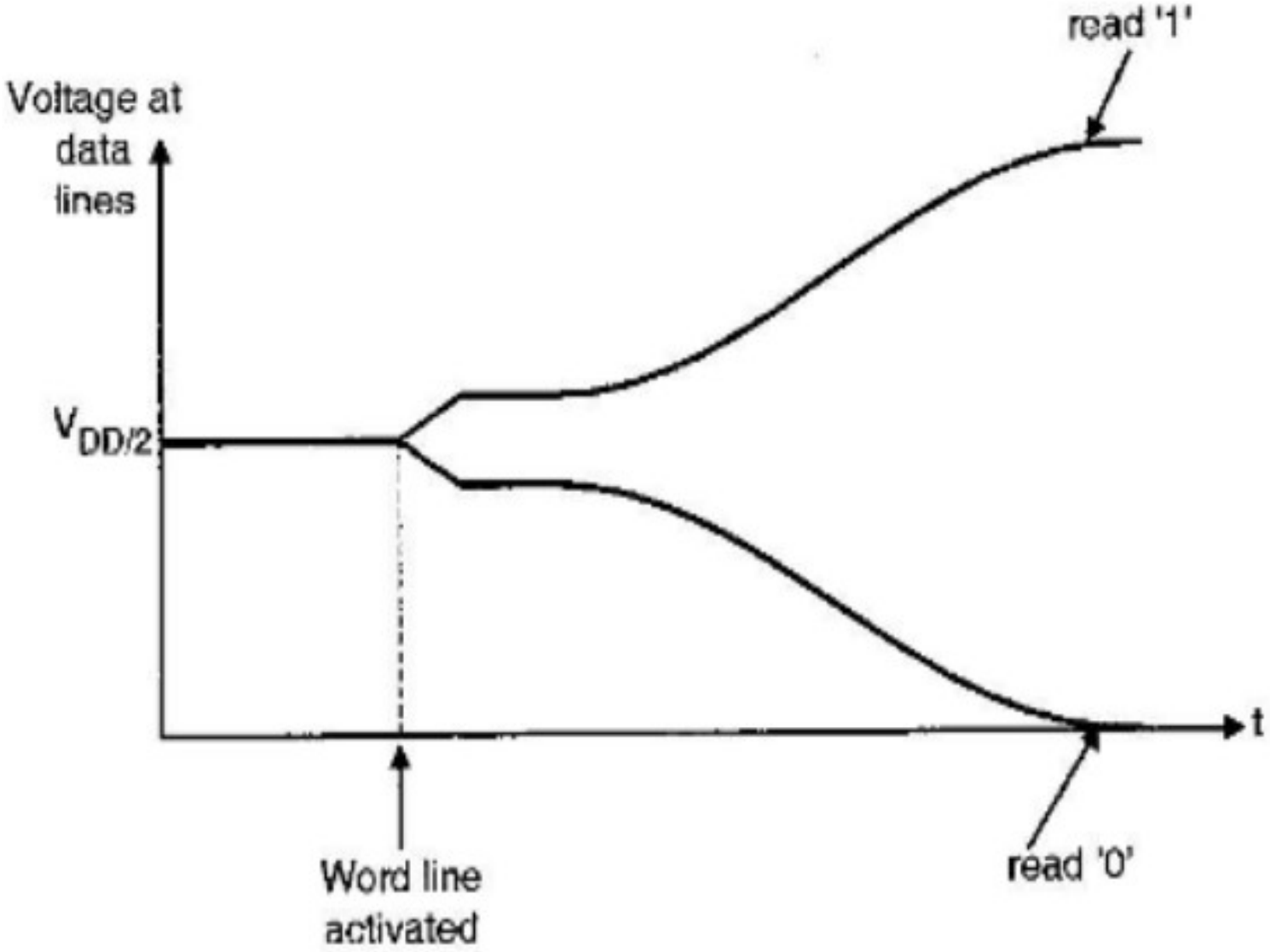
- A sense amplifier is used to sense the information stored in the memory cell during the read operation.

- Its role is to sense the low power signals from a bit line / data line that represents a data bit (1 or 0) stored in a memory cell, and amplify the small voltage swing to recognizable logic levels so the data can be interpreted properly by logic outside the memory.

- Differential amplifier is used as a Sense amplifier.

Sense Amplifier using Differential amplifier



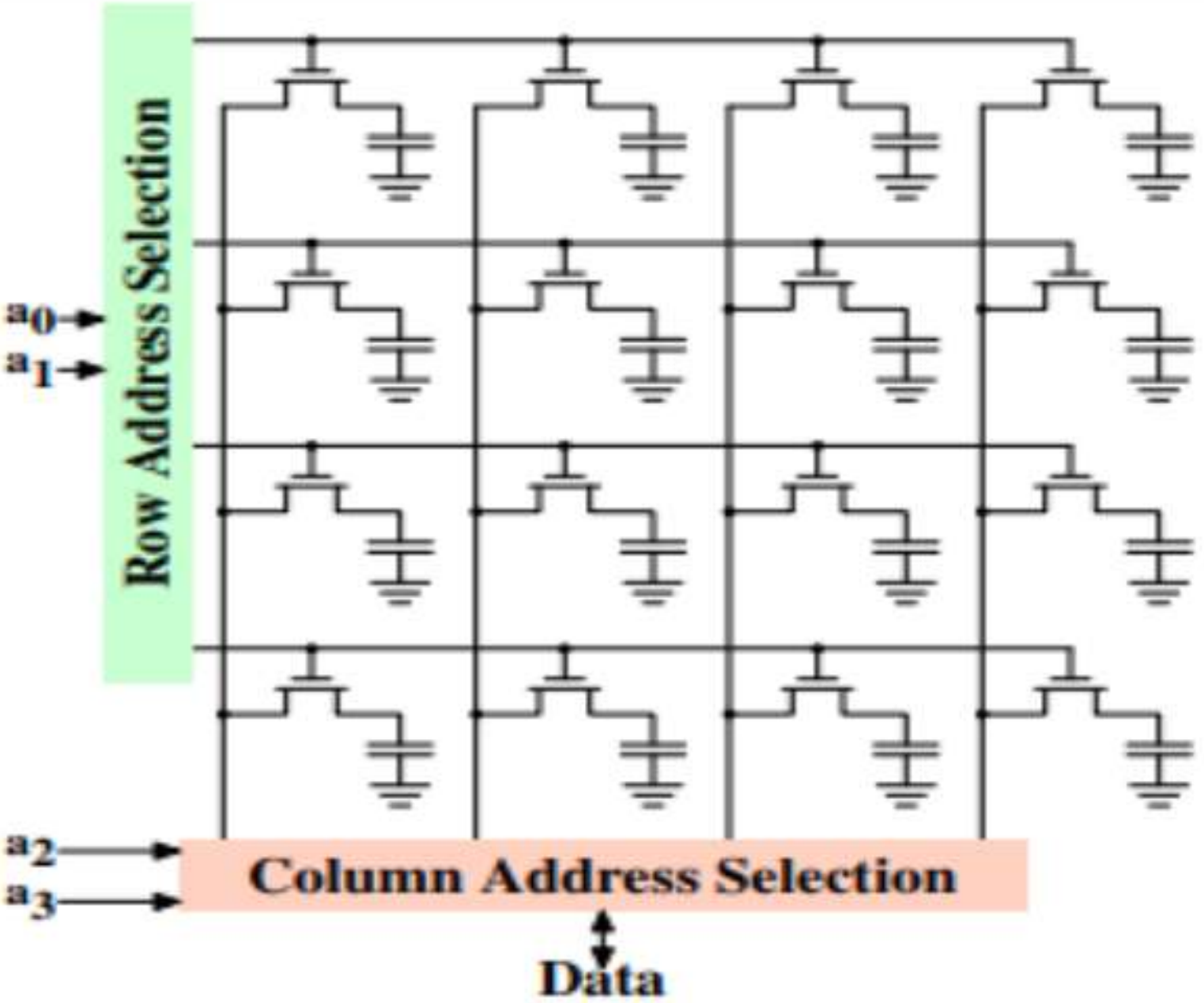


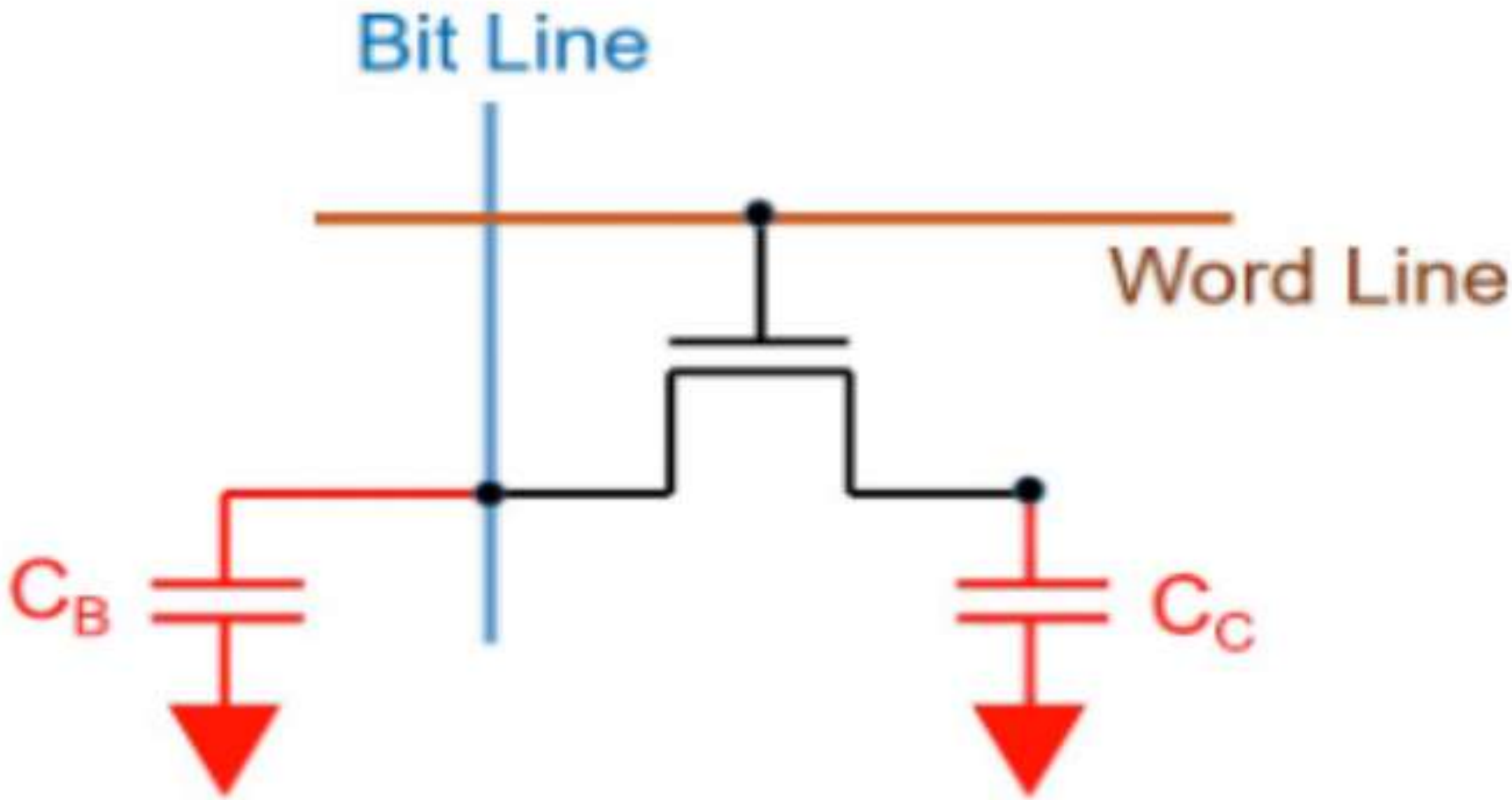
Waveforms of data lines

Dynamic RAM

- It stores the information depends on the charge in Capacitor.
- It does not require continuous power supply but the charge in capacitor must be refreshed after a particular interval of time.

1-T DRAM Cell

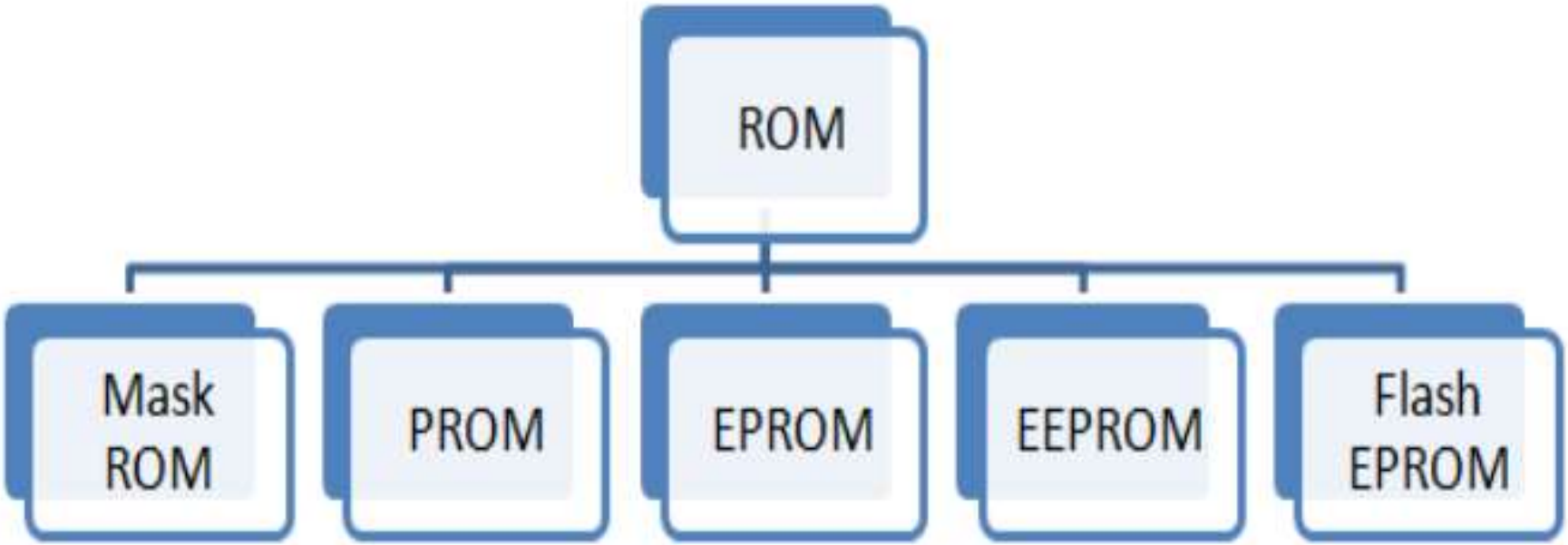

Row Address Selection
a0
a1
a2
a3
Column Address Selection
Data


Bit Line
Word Line
C_B
C_C

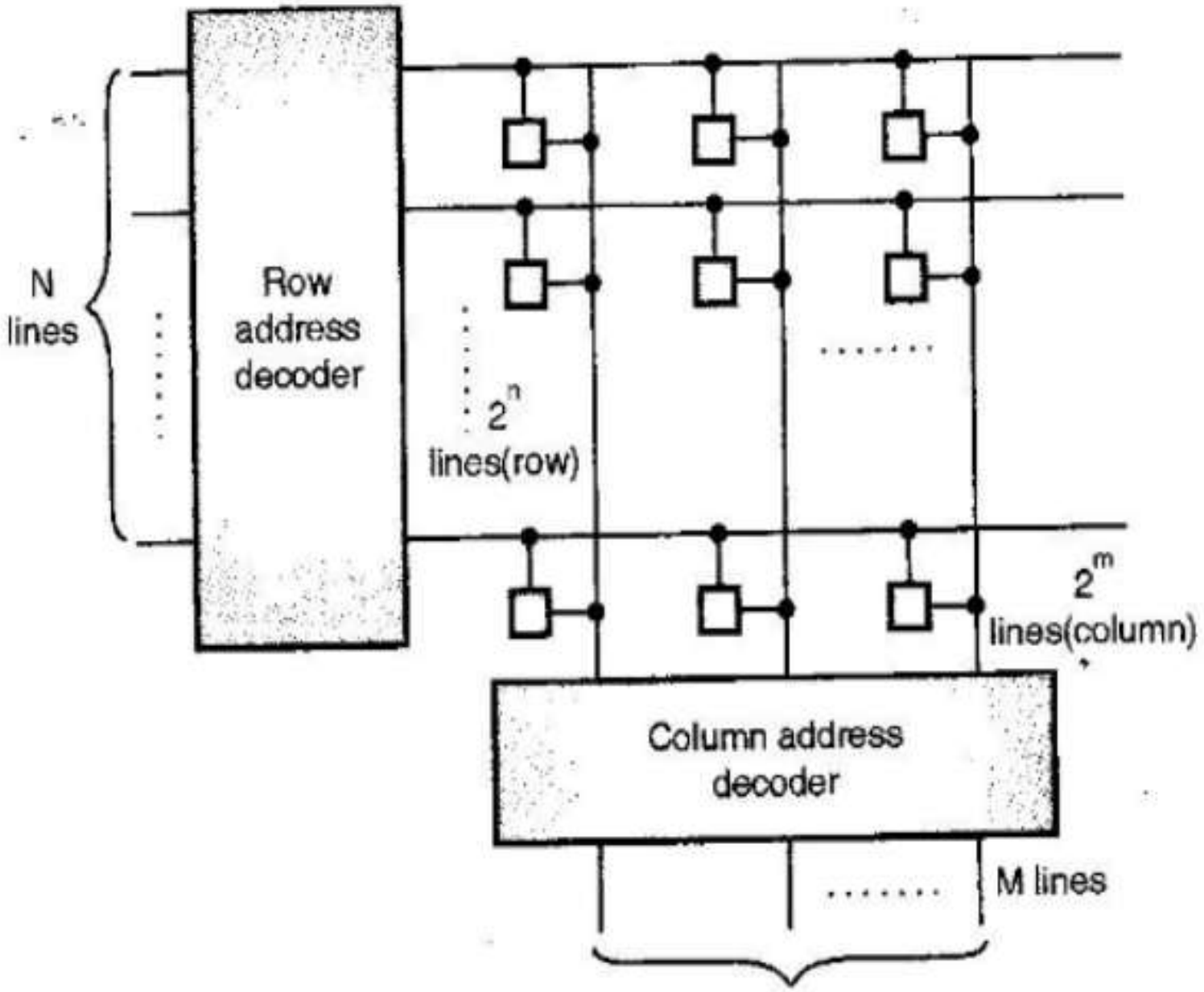
Difference between SRAM and DRAM

SRAM	DRAM
It retains the stored data as long as power supply is ON	It loses the stored data even though the power supply is ON
It uses latch circuit to store the data , hence does not require refresh operation	It stores the data in the form of charge on capacitor , which leaks away in very short time , hence require Refresh operation
Packaging density is small as 6 transistors used	Packaging density is large as 1 transistor and capacitor is used
Higher speed	Lower speed
Low power consumption	High power consumption
Expensive	Inexpensive
Used for Cache memory	Used for Main memory

Read Only Memory (ROM)

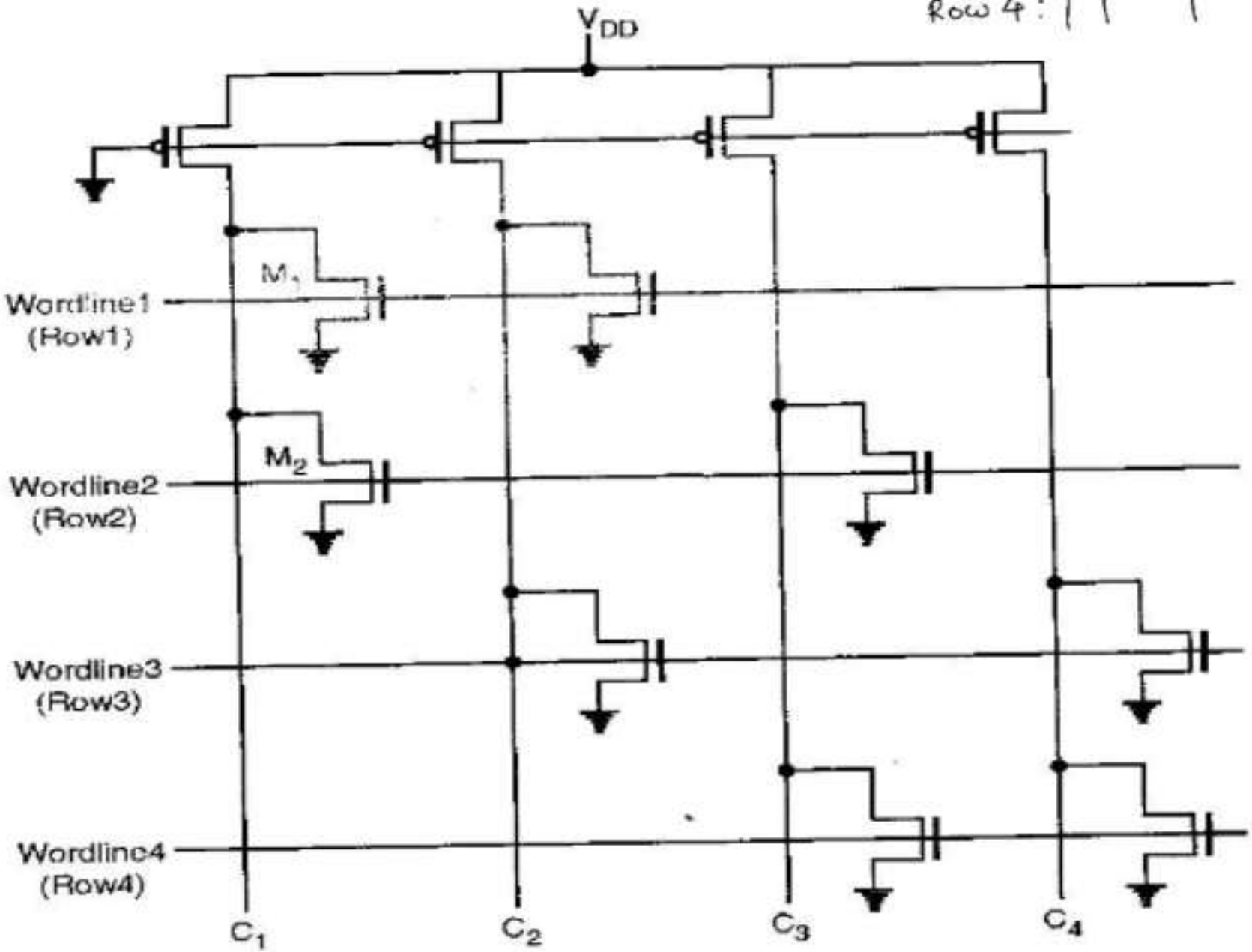


ROM Structure



NOR based ROM Array

	C_1	C_2	C_3	C_4
Row 1 :	0	0	1	1
Row 2 :	0	1	0	1
Row 3 :	1	0	1	0
Row 4 :	1	1	0	0

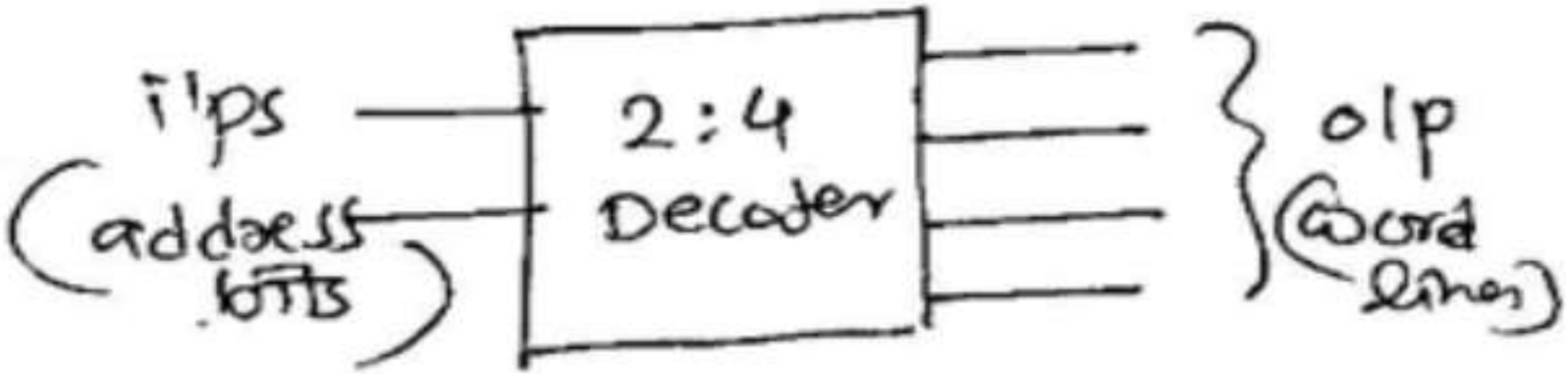


➢ **Following table shows the data stored in this memory**

	C_1	C_2	C_3	C_4
Row 1 :	0	0	1	1
Row 2 :	0	1	0	1
Row 3 :	1	0	1	0
Row 4 :	1	1	0	0

ROW Decoder for NOR based ROM Array

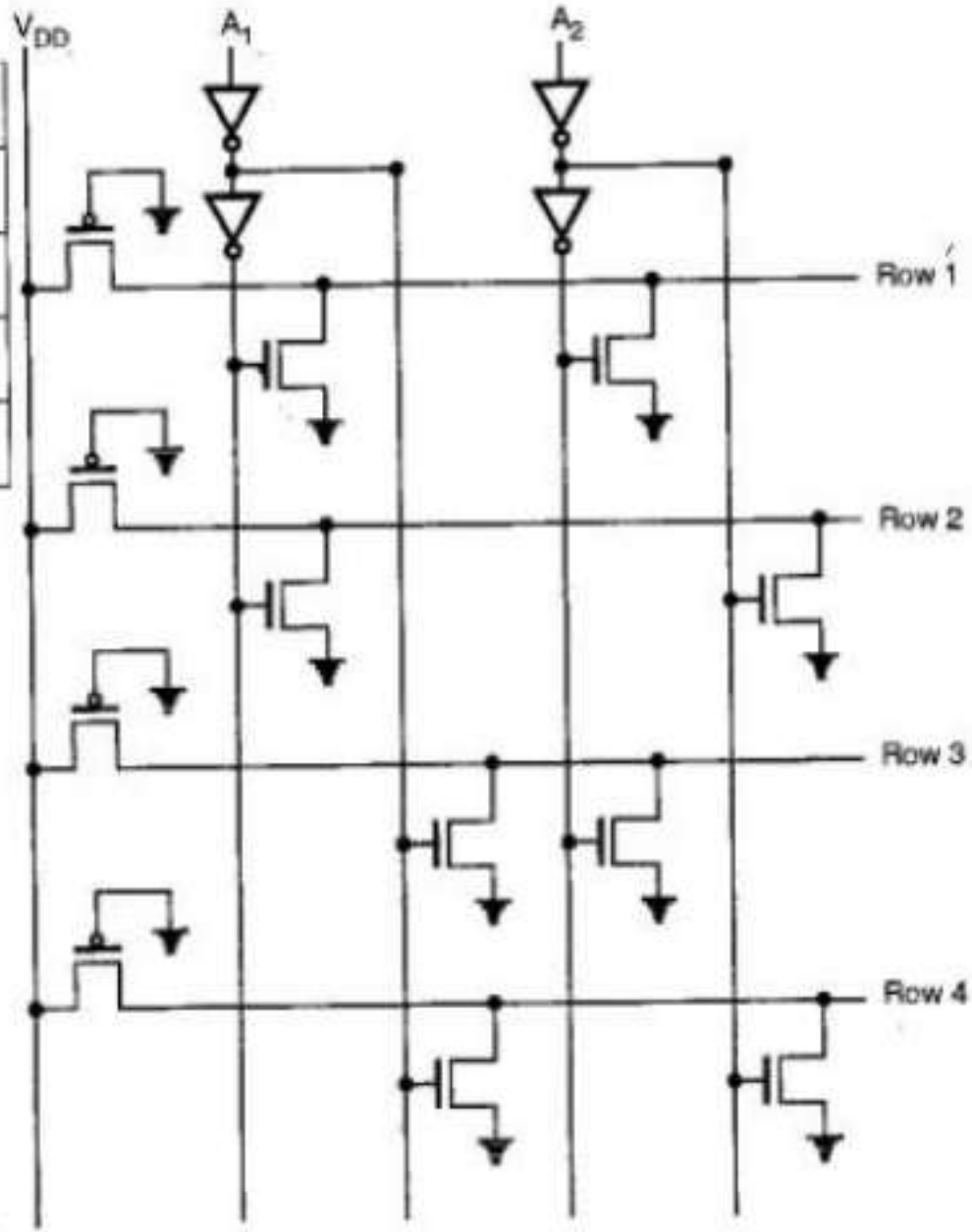
- Purpose of Row decoder is to select on the 2^N word lines by raising its voltage to high voltage



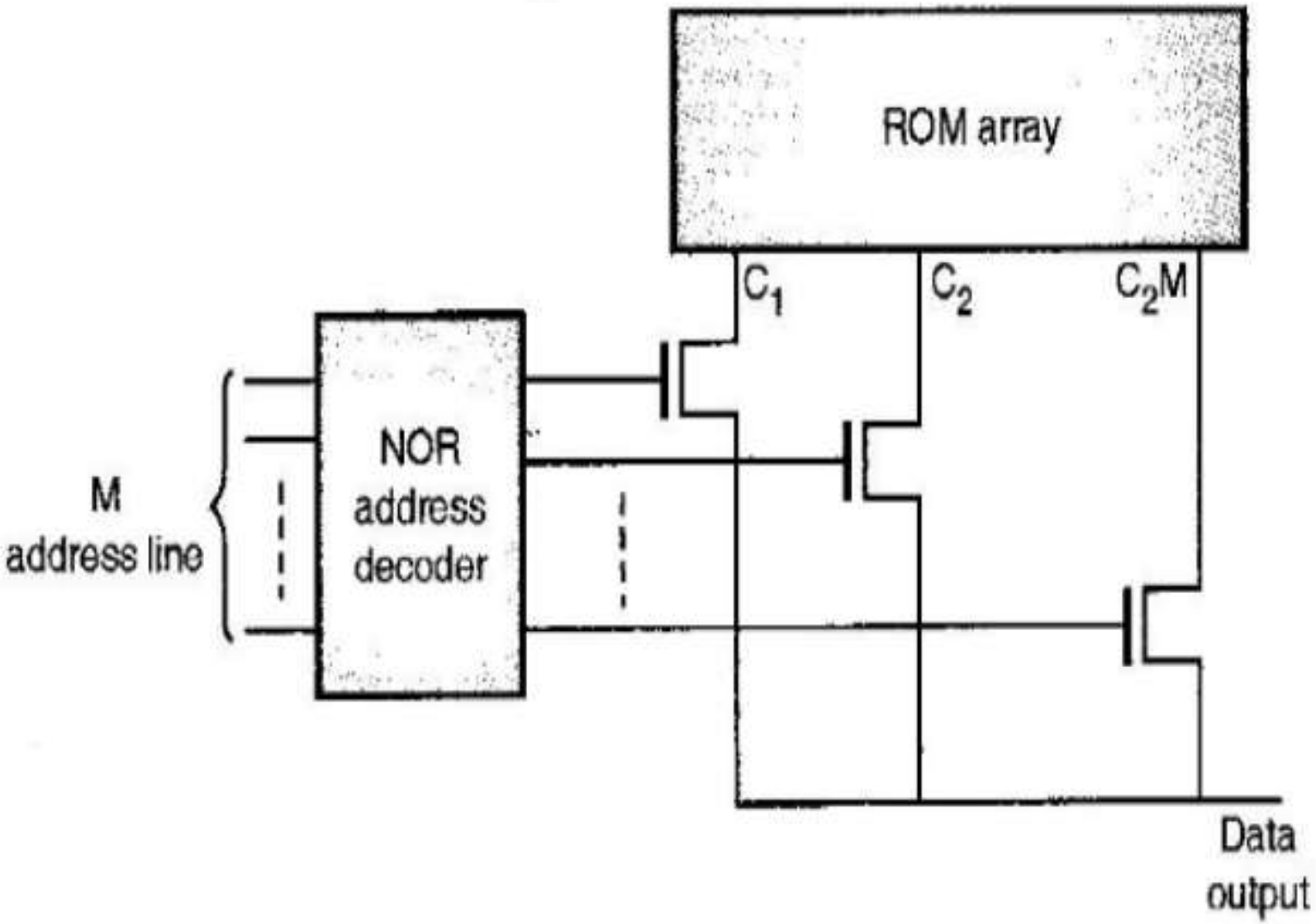
2:4 Decoder Circuit

Truth table

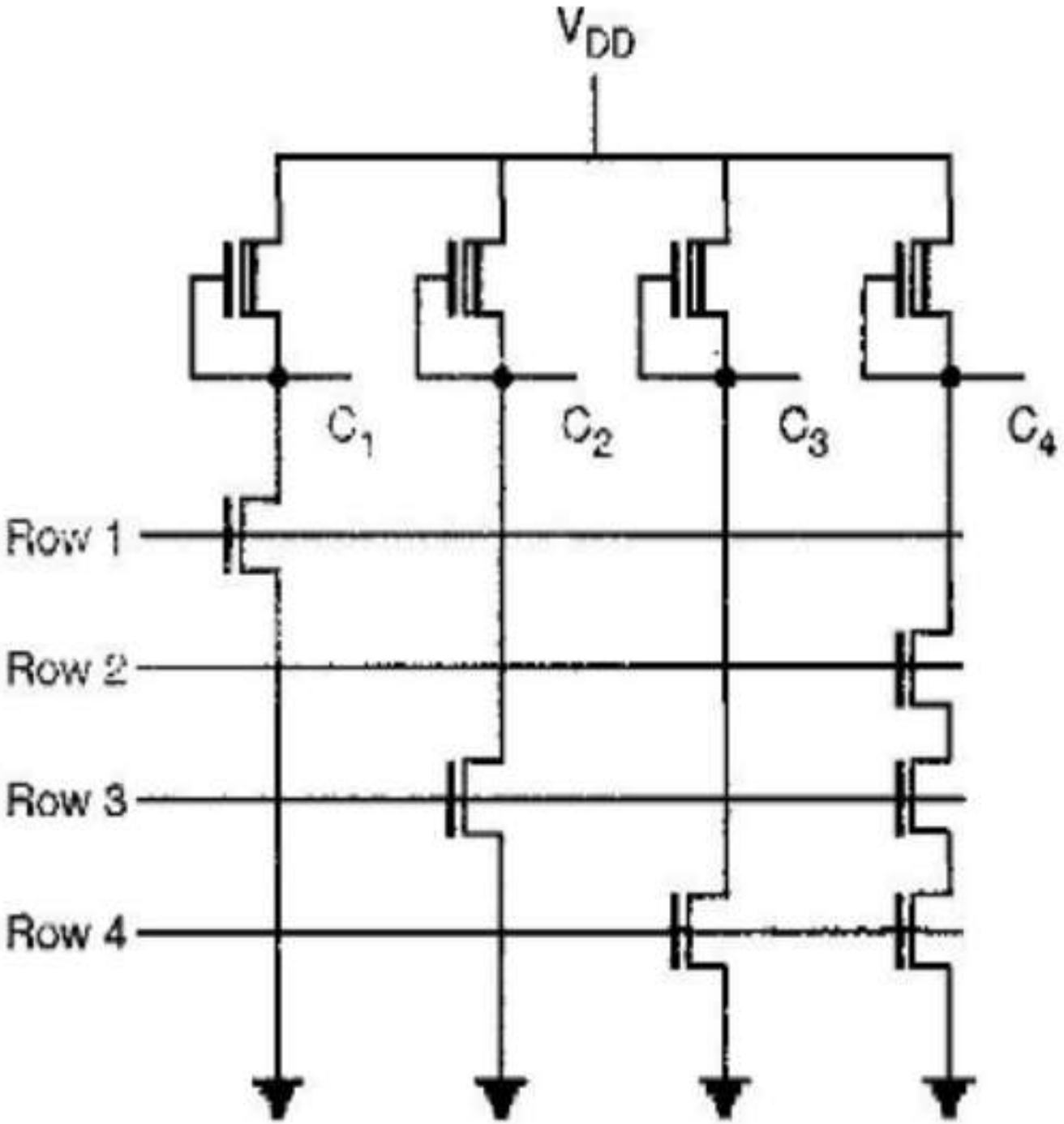
A_1	A_2	R_{ow1}	R_{ow2}	R_{ow3}	R_{ow4}
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1



Column Decoder for NOR based ROM Array



NAND based ROM Array

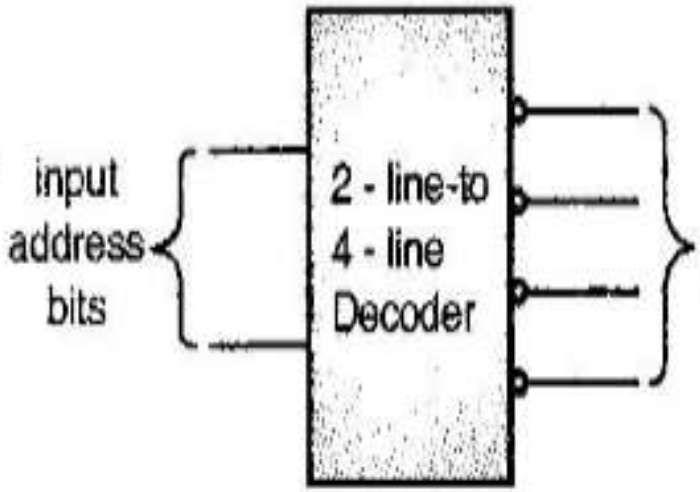


	C_1	C_2	C_3	C_4
ROW1 :	1	0	0	0
ROW2 :	0	0	0	1
ROW 3:	0	1	0	1
ROW4 :	0	0	1	1

➢ **Following table shows the data stored in this memory**

	C_1	C_2	C_3	C_4
ROW1 :	1	0	0	0
ROW2 :	0	0	0	1
ROW3 :	0	1	0	1
ROW4 :	0	0	1	1

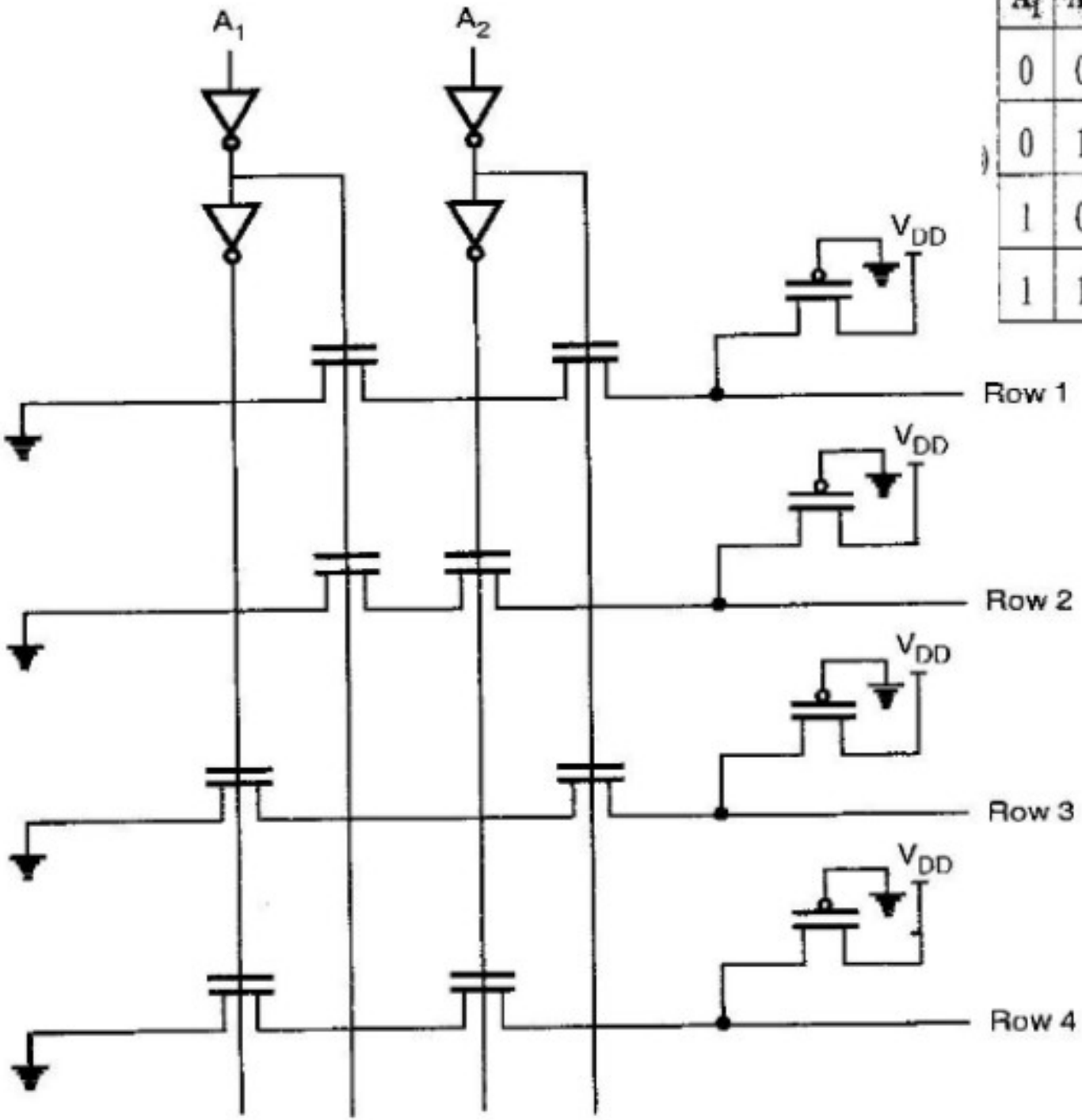
ROW Decoder for NAND based ROM Array



(a)

A_1	A_2	Row 1	Row 2	Row 3	Row 4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

(b)



A_1	A_2	Row 1	Row 2	Row 3	Row 4
0	0	0	1	1	1
0	1	1	0	1	1
1	0	1	1	0	1
1	1	1	1	1	0

Non-Volatile Memory

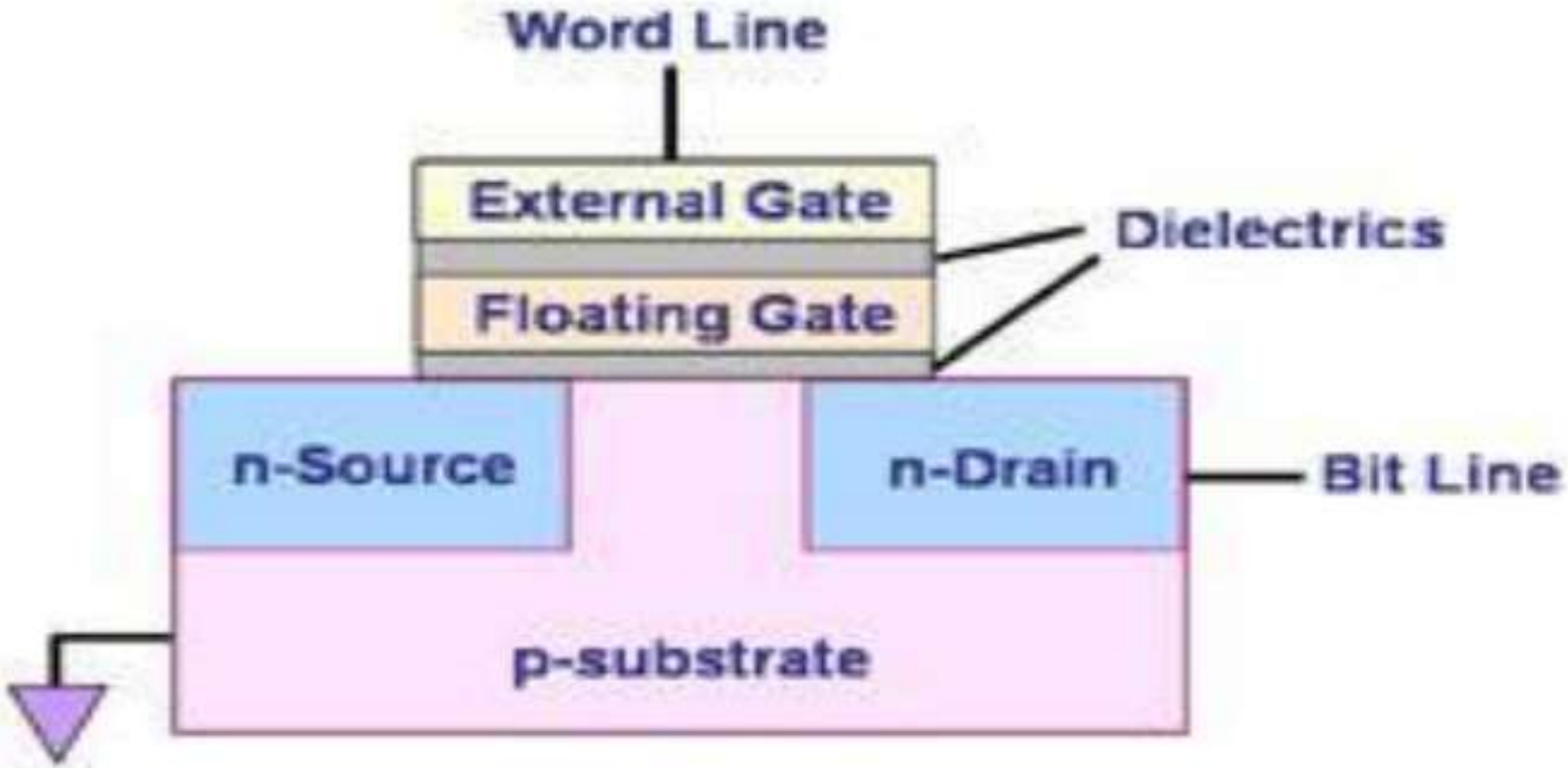
- It retain stored information even after power is removed.

- Examples of non-volatile memory include flash memory, read-only memory (ROM), ferroelectric RAM, hard disk drives, floppy disks, and magnetic tape, optical discs etc.

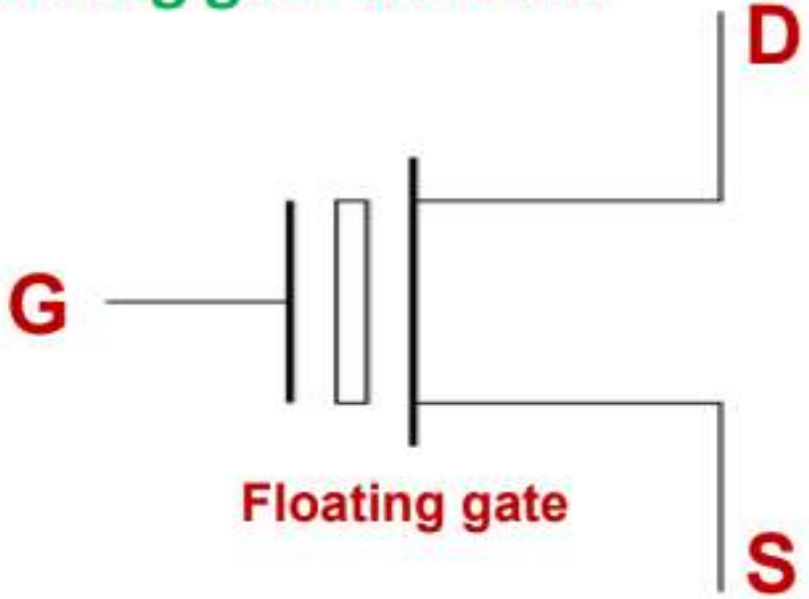
Flash Memory

- Flash memory is a low-cost, high-density, non-volatile storage chip that can be electrically erased and reprogrammed.
- In a flash memory, a whole block of memory cells can be erased in a single action, or in a 'flash'.
- It retain the data for 10 years (approx.)
- Number of write/erase cycles = 10^5
- Used in Digital camera,USB,Solid State Disk (SSD)
- Flash memory can be either NOR-Flash or NAND-Flash.

- A basic flash memory cell consists of a MOSFET that was modified to include an isolated inner gate between its external gate and the silicon as shown in Figure.
- This inner gate is known as a 'floating gate', which is the data-storing element of the memory cell and external gate is 'Control gate'.



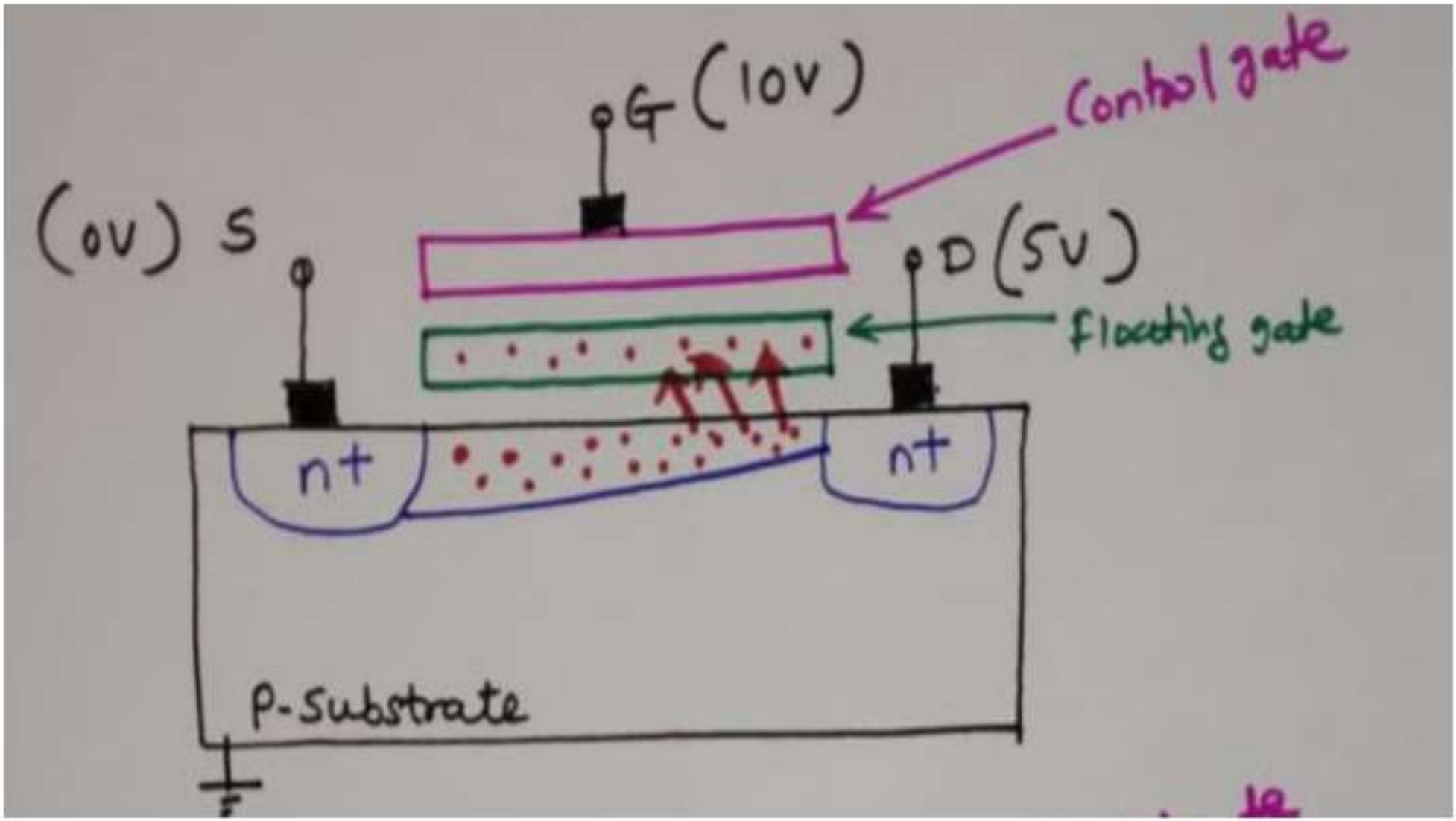
- Data is stored in a flash memory cell in the form of electrical charge accumulated inside the floating gate.
- The amount of charge stored in the floating gate depends on the voltage applied to the external gate of the memory cell that controls the flow of charge into or out of the floating gate.
- Logic 1 means floating gate is empty
- Logic 0 means floating gate is full of electrons.
- Symbol of floating gate MOSFET



Programming Operation of Flash Memory

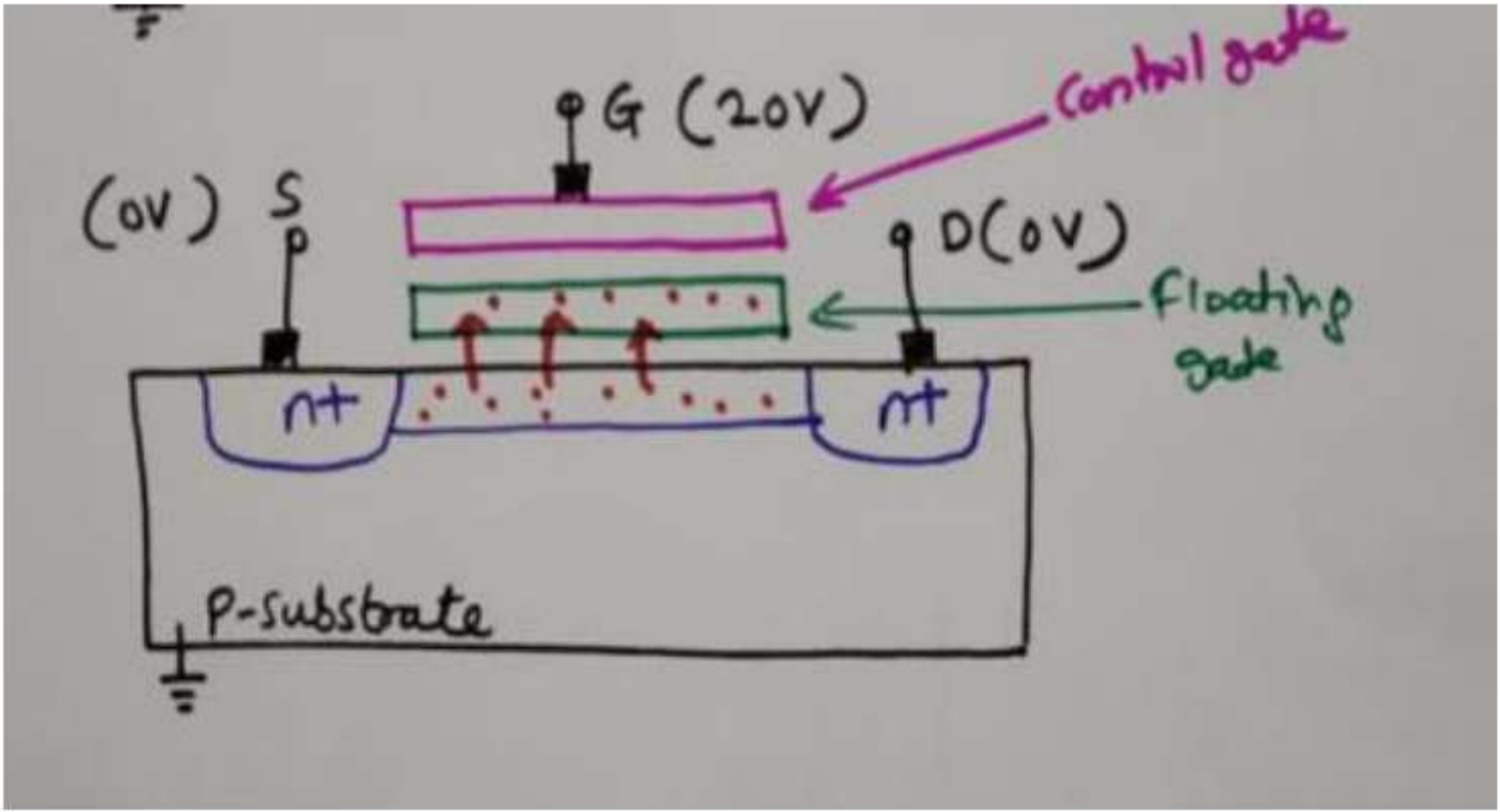
(1) Channel Hot Electron method (CHE)

- When sufficient drain voltage is applied at the drain terminal of MOSFET, electrons present in the channel gets attracted towards the drain terminal.
- At the same time, if higher Gate voltage is applied at the Gate terminal of the MOSFET then due to the higher gate voltage the electrons are penetrated through the floating gate and they remain there unless removed.
- This method by which electrons are penetrated into the floating gate is called as Tunneling effect.
- In this method, Source voltage = 0V , Drain voltage = 5V and Gate voltage =10V applied.


G (10V)
Control gate
(0V) S
D (5V)
floating gate
n+
n+
P-substrate

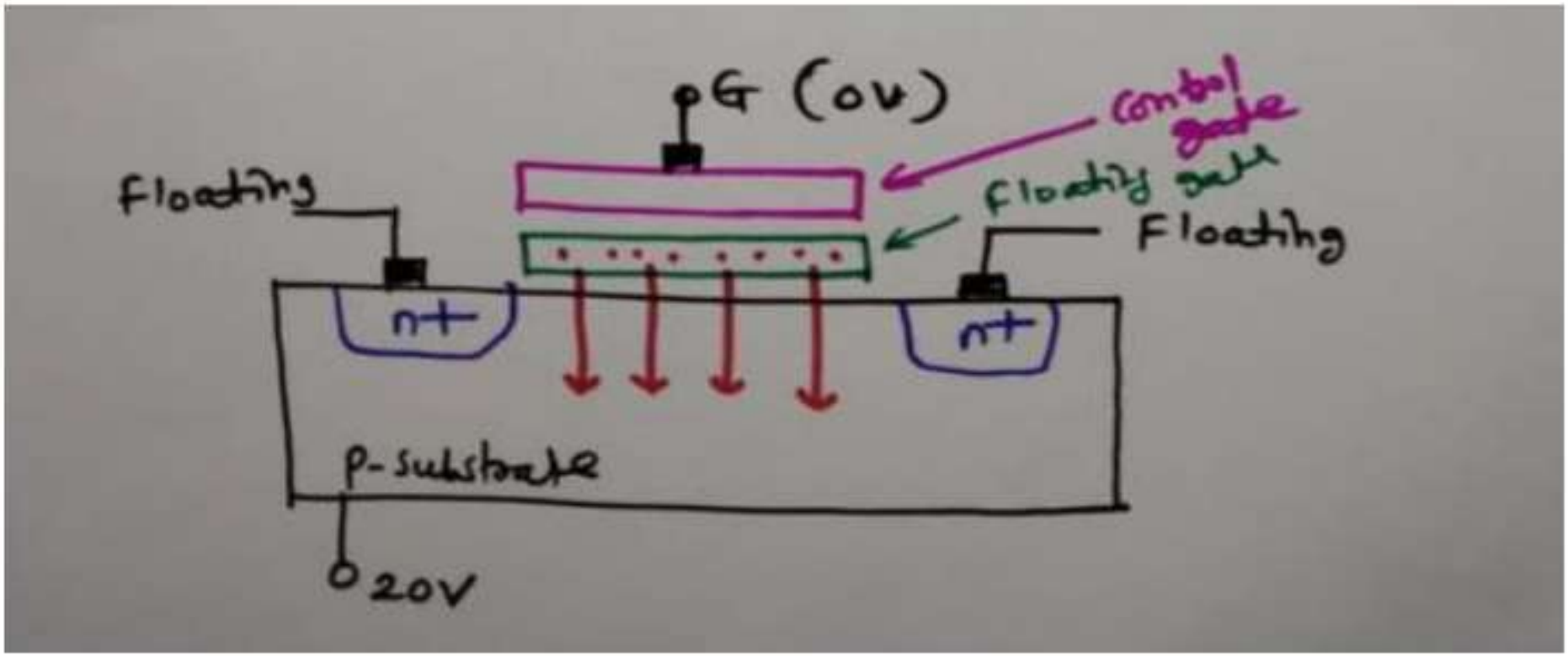
(2) Fowler–Nordheim Tunnelling method (FN)

- In this method Source voltage and Drain voltage are kept at 0 V.
- Large Gate voltage about 20 V is applied due to which, the electrons are penetrated through the floating gate and they remain there unless removed.
- This is efficient method for flash programming.


G (20V)
Control gate
(0V) S
D(0V)
Floating gate
n+
n+
P-substrate

Erase Operation of Flash Memory

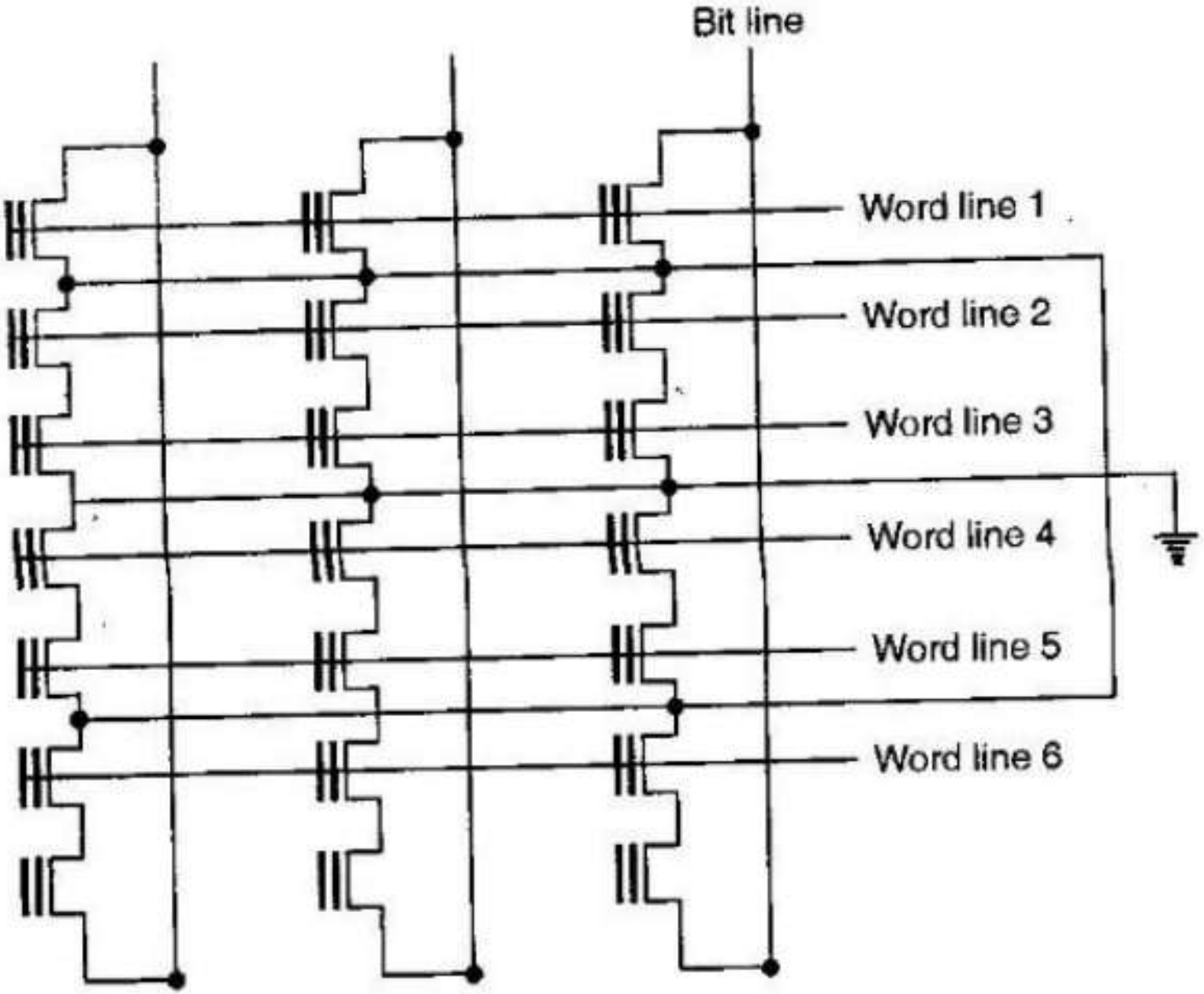
- During erase operation Source and Drain terminals are kept floating
- No Gate voltage is applied.
- Large body voltage (approx. 20 V) is applied due to which electrons present in the floating gate is attracted towards the body terminal due to such high positive voltage.



NOR type of Flash Memory

- It consist of floating gate transistor having its one end connected to the ground and other end connected to the bit line.
- The control gate is connected to word line.
- This type of memory is called as NOR flash because it acts like a NOR gate in which if any one of the word line is brought high, the corresponding stage transistor pulls the output line low.

NOR Flash Memory Array



Programming of NOR Flash

- A single level NOR flash cells are logically equivalent binary "1" value which is there default state. Thus, NOR gate can be programed to logic "0" as follows,
- Apply a high voltage to control gate of selected device (approx. 10 -15V).
- This turns the channel ON allowing electrons to flow from source to drain.
- If this current is high, hot electrons are generated and injected into the floating gate through insulating layer.
- Thus,threshod voltage of device is shifted to higher value.

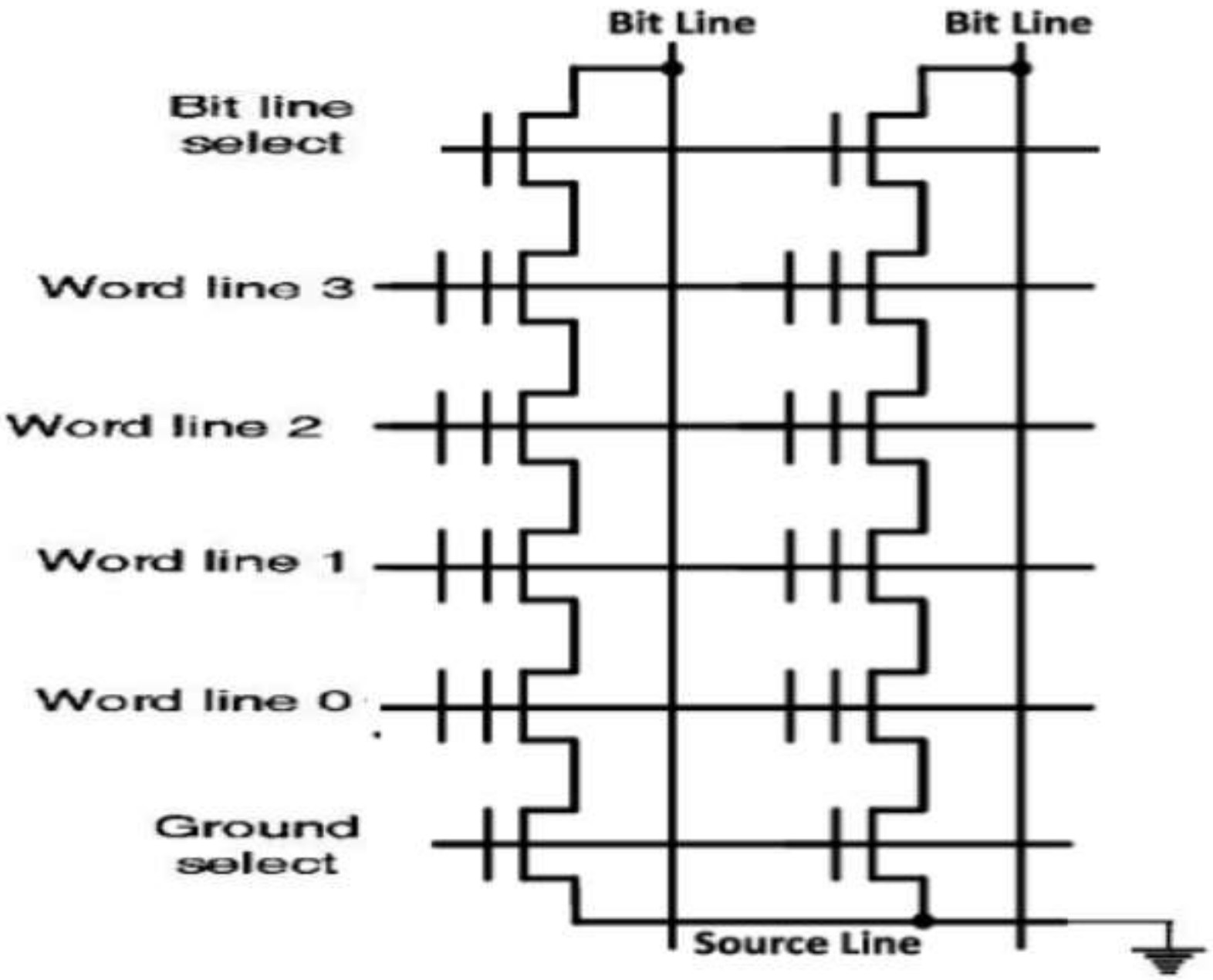
Erasing of NOR Flash

- A large voltage (approx. 20 V) is applied at the bulk terminal of the MOSFET.
- Because of which , electrons present in the floating gate are pulled in the substrate again.
- This causes the floating gate devoid of charge.

NAND type of Flash Memory

- It consist of floating gate transistors that are connected in series.
- In this arrangement the bit line is pulled low only of all the word lines are pulled high, which is similar to the NAND gate behavior, hence called as NAND flash.
- As all the cells are connected in series, therefore they can not be programmed individually.
- It uses a tunnel injection and tunnel release for writing and erase respectively.
- It is more denser than NOR flash memory and ideal for high capacity data storage.

NAND Flash Memory Array



	DRAM	SRAM	FLASH
Advantage	Cheap	Fast	Save data when power is off
Disadvantage	Comparatively slow & loses data when power supply is off	Cost is 4 times more than DRAM & & loses data when power supply is off	Data saving process is slow and consumes lot of power

https://youtu.be/r2KaVfSH884?si=6ZU5M-MV94_6wOny


Thank
you!