

# **Module 2**

# **MOSFET Inverters**

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## **Module 2:- MOSFET Inverters**

- 2.1 Introduction to MOS inverters: Active and passive load nMOS inverters, CMOS inverter and their comparison.**
- 2.2 Static Analysis of Resistive nMOS and CMOS Inverters: Calculation of critical voltages and noise margins.**
- 2.3 Analysis & Design of symmetric CMOS inverter.**
- 2.4 Analysis of CMOS inverter: Calculation of rise time, fall time and propagation delay.**

## **2.1 Introduction to MOS Inverters**

# MOSFET Inverter

- An Inverter is most fundamental logic gate that performs a Boolean operation on single i/p variable.

digital logic ckt which produces output that is logical complement of the input.

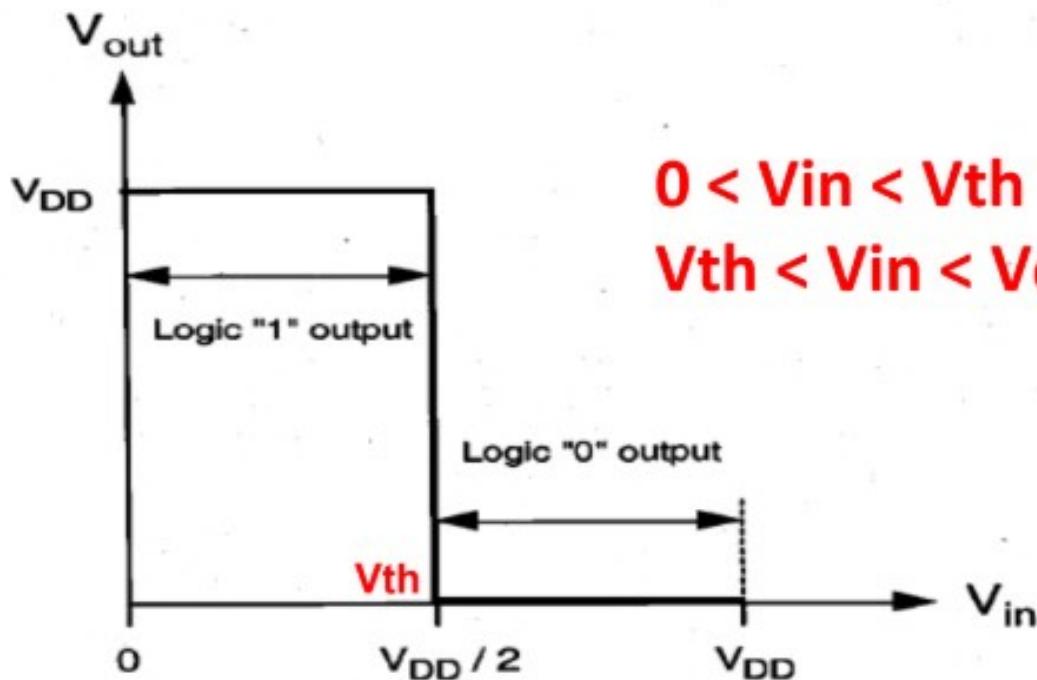
- Logic symbol and truth table is ,

i/p	o/p
1	0
0	1



Input	Output
1	0
0	1

- Following fig. shows voltage transfer characteristics ( VTC) of an ideal inverter circuit,



$0 < V_{in} < V_{th}$  = Output is 1  
 $V_{th} < V_{in} < V_{dd}$  = Output is 0

$$V_{DD}/2$$

$$0 < V_{in} < V_{th} = \text{output} = 1$$

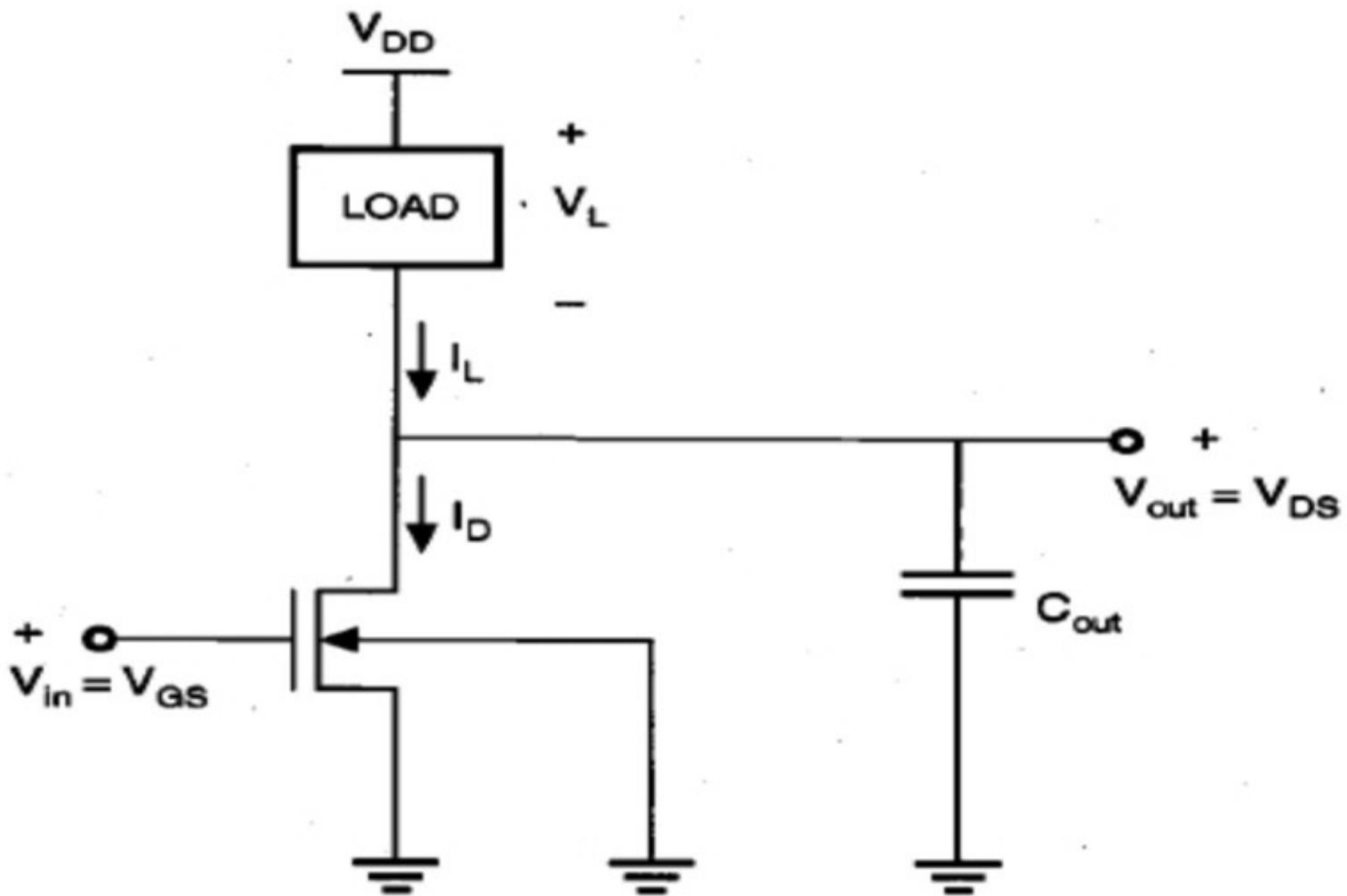
$$V_{th} < V_{in} < V_{dd} = \text{output} = 0$$

- The voltage  $V_{th}$  is called threshold voltage & from any i/p voltage between 0 to  $V_{th}$  ( ie.  $V_{dd}/2$  ), the o/p voltage is equal to  $V_{dd}$  (ie Logic 1)
- The o/p switches from  $V_{dd}$  to 0 when  $V_{in}=V_{th}$
- For any i/p voltage between  $V_{th}$  &  $V_{dd}$  , the o/p voltage is equal to 0 ( ie logic 0 )

$$V_{in} = V_m$$

$$\begin{aligned} V_{dd} = \\ \underline{\text{logic 1}} \end{aligned}$$

# Generalized NMOS Inverter

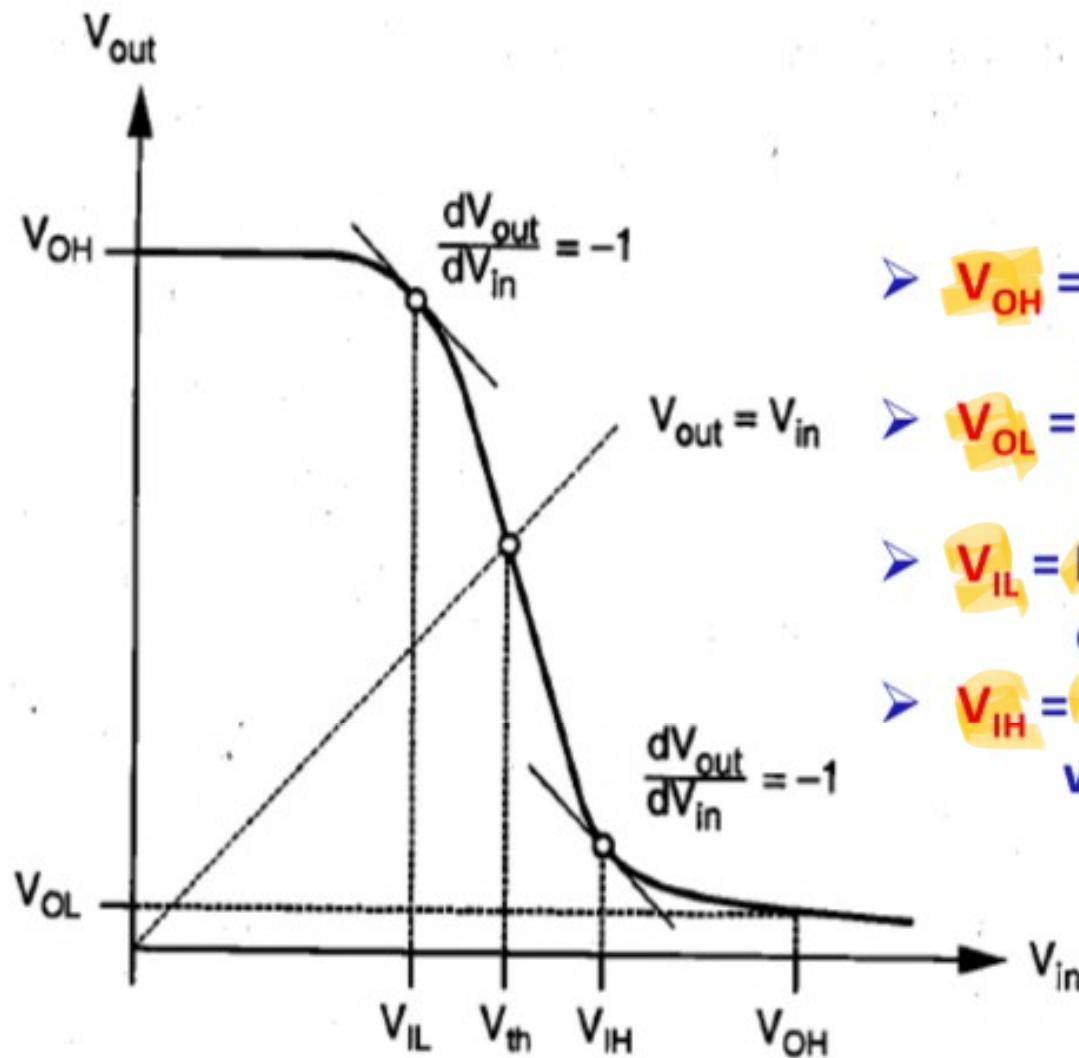


$$V_{in} = V_{GS}$$
$$V_{out} = V_{DS}$$

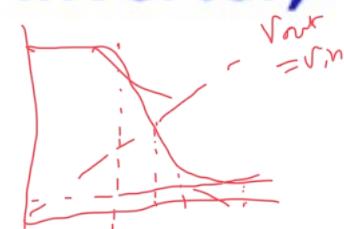
- As shown in fig,  $V_{in}=V_{GS}$  and  $V_{out} = V_{DS}$
- The source and substrate terminals of NMOS transistor is called as Driver transistor and connected to ground potential ( ie  $V_{SB} = 0$ )  
 $V_{SB} = 0$   
ss → DT.  
↓  
GND.
- The load is two terminal circuit , with current ( $I_L$ ) & Voltage ( $V_L$ )
- The o/p of an inverter circuit is connected to i/p of another MOS inverter , which can be represented by Lumped capacitor.

# Voltage Transfer Characteristics (VTC)

- VTC describes  $V_{out}$  as a function of  $V_{in}$  under the DC conditions.
- Following fig. shows generalized VTC for NMOS inverter,

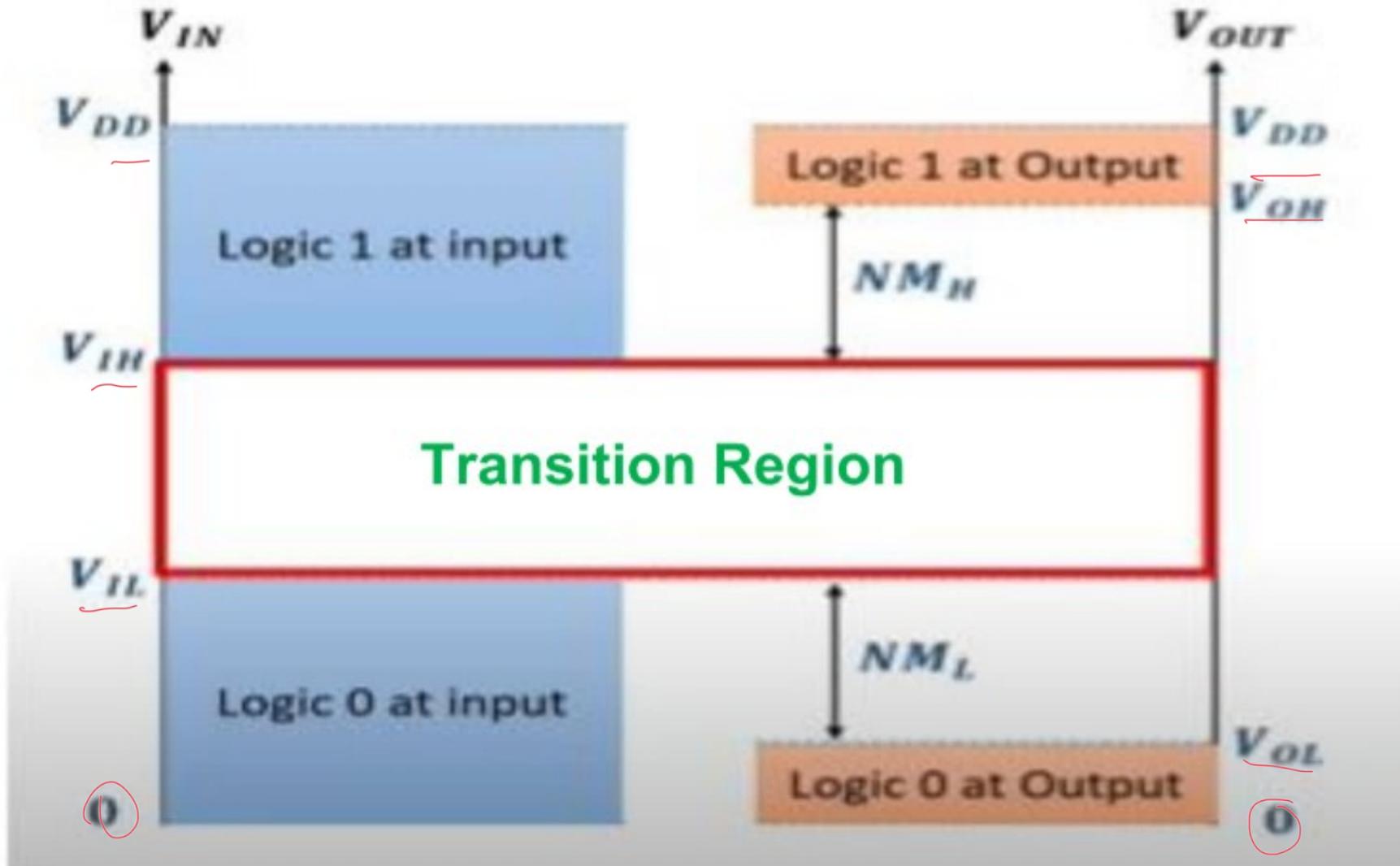


- $V_{OH}$  = Maximum o/p voltage when o/p level is logic 1
- $V_{OL}$  = Minimum o/p voltage when o/p level is logic 0
- $V_{IL}$  = Maximum input voltage which can be interpreted as logic 0
- $V_{IH}$  = Minimum input voltage which can be interpreted as logic 1



max o/p volt when o/p level is logic 1  
min o/p logic 0

- For a very low input voltage levels the o/p voltage  $V_{out} = V_{OH}$  in which NMOS is off and does not conduct any current.
- As  $V_{in}$  increases, the NMOS is ON & starts conducting a certain drain current and o/p voltage start decreasing and reaches to zero.
- As shown in curve , we get two critical voltage points where the slope of characteristics ie.  $dv_{out}/dV_{in} = -1$
- The smaller i/p voltage value which satisfy the above condition is called i/p low voltage ( $V_{IL}$ ) and larger i/p voltage satisfying this condition is called as i/p high voltage ( $V_{IH}$ ).
- As the i/p voltage is further increased , the o/p voltage continues to drop and reaches o/p low voltage ( $V_{OL}$ ). o/p continues to drop → reaches o/p low voltage
- The point on curve , where  $V_{in}=V_{out}$  is called as inverter Threshold voltage (  $V_{TH}$  ) V\_{in}=V\_{out} → inverter V\_{in}



- The voltage range between  $V_{IL}$  and  $V_{IH}$ , corresponding to i/p voltage values that may not be processed correctly as logic 0 or logic 1 i/p by inverter is called as **Transition region**.

## Noise margin

- It explains upto what extent, IC allows Noise in transmission of logic 0 and logic 1.
- It is defined as ,” The amount by which the signal exceeds the threshold for proper “0” or “1”.
- Two Noise margins are defined as Noise margin for low signal level ( $N_{ML}$ ) and for high signal level ( $N_{MH}$ )

$$N_{ML} = V_{IL} - V_{OL}$$
$$N_{MH} = V_{OH} - V_{IH}$$

➤ Under the steady state condition,

$$V_{out} = f(V_{in})$$

if now i/p voltage is affected by noise then

$$V_{out} = f(V_{in} + \Delta V_{noise})$$

➤ By using 1<sup>st</sup> order Taylor's series expansion and by neglecting higher order terms ,

$$V_{out}' = f(V_{in}) + (dV_{out} / dV_{in}) \Delta V_{noise}$$

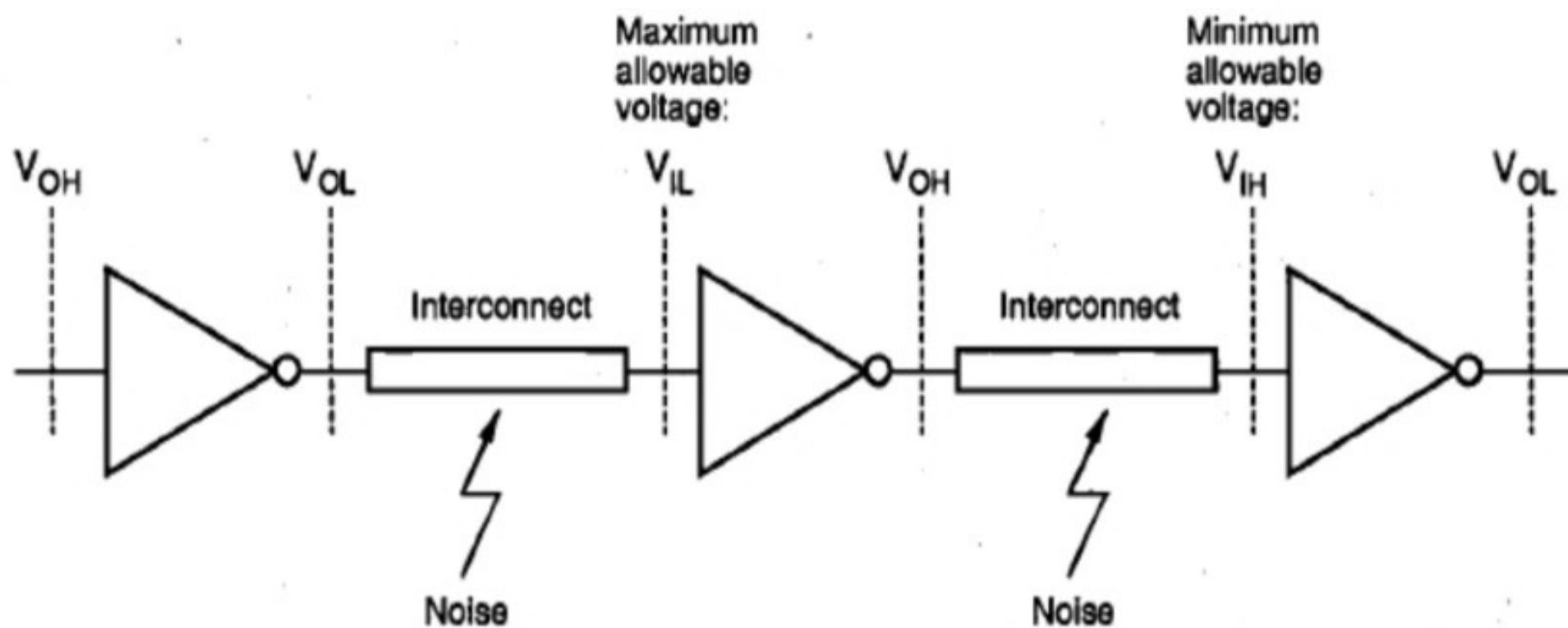
➤ In general ,

Perturbed o/p = Nominal o/p + Gain X External perturbation

$$\text{Perturbed o/p} = \text{Nominal o/p} + \text{Gain} \times \text{External perturbation}$$

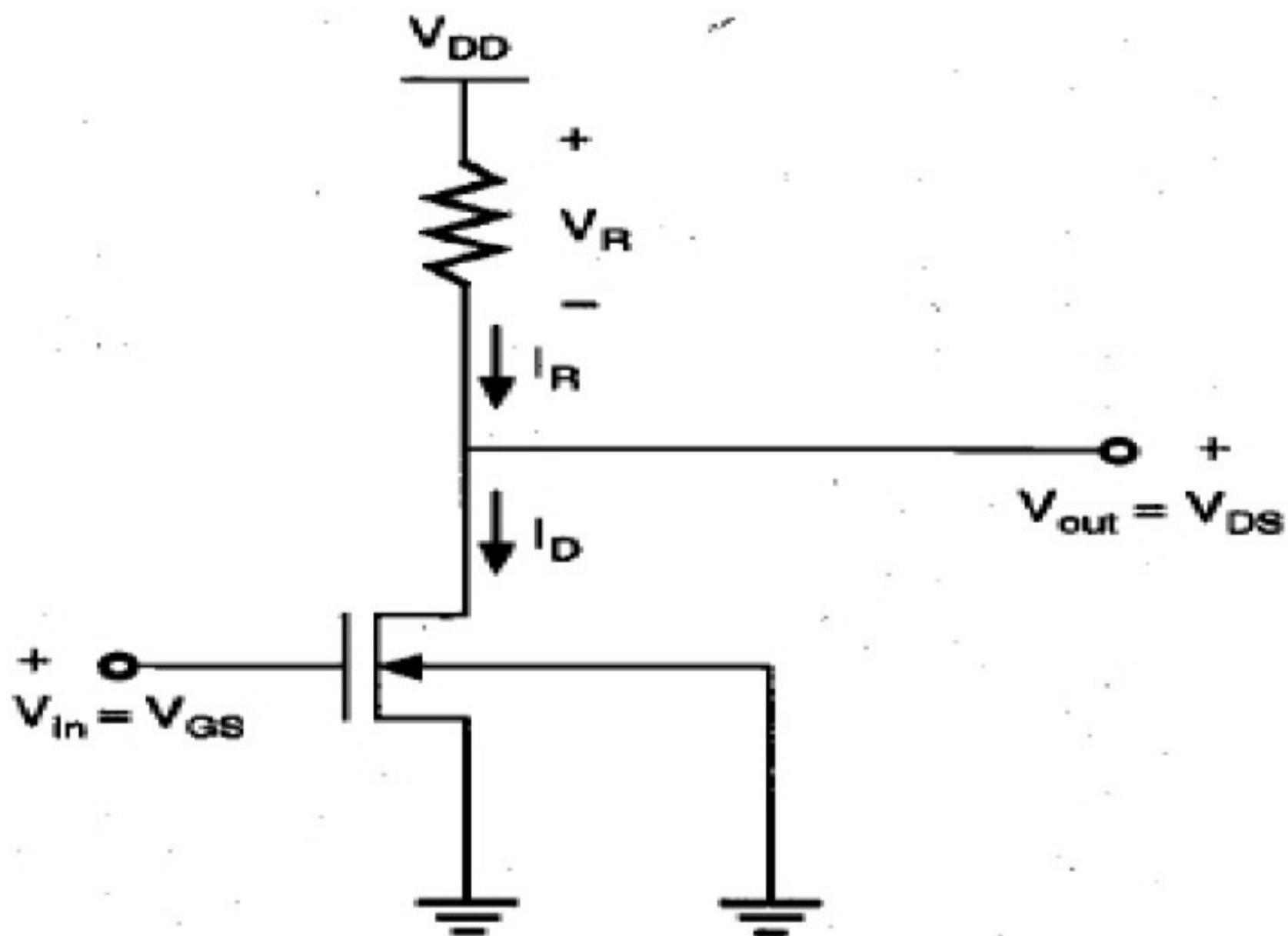
## Noise Immunity

- To understand the effect of noise on the circuit reliability , let us consider the following circuit,



- Assume all inverters are identical & let i/p voltage of the first inverter is equal to  $V_{OH}$  ( logic 1) thus, the o/p is equal to  $V_{OL}$  ( logic 0).
- Now, this o/p signal is being transmitted to the next inverter i/p via an interconnect, which could be metal or polysilicon line connecting the two gates, these on-chip interconnects are generally prone to signal noise, the o/p signal of the first inverter will be perturbed during the transmission. Consequently, the voltage level at the i/p of second inverter will be either larger or smaller than  $V_{OL}$ .
- If the i/p voltage of second inverter is smaller than  $V_{OL}$ , then this signal will be interpreted correctly as logic 0 i/p by second inverter, on the other hand , if the i/p voltage becomes larger than  $V_{OL}$  as a result of noise then it may not be interpreted correctly by the inverter and similarly for the third inverter.

# Resistive load Inverter



NMOS  $\rightarrow$  driver  
 $R_L = \text{Load}$   
 $V_{SB} = 0$

- In which N-mos xtor acts as driver & load is  $R_L$ .
- As shown,  $I_D = I_R$ , in DC state (steady) opern.  
also,  $V_{SB} = 0$
- To simplify the calculations, channel-length modulation effect (ie.  $\lambda$ ) is neglected in this analysis.

Working :-

- If the i/p voltage smaller than threshold volt. ( $V_{TO}$ ) is applied, the xtor is in cutoff region & does not conduct any drain current.

$$\therefore I_R = I_D = 0$$

i/p  $< V_{TO} \rightarrow$  cutoff region.  
 $\rightarrow$  no drain current  
 $I_R = I_D = 0$   
 $V_D$  across  $R_L = 0$ ,

& voltage drop across  $R_L = 0$ , thus, total VDD voltage will appear at the o/p  $\therefore V_{out} = V_{DD}$  (ie. i/p = 0)  
 $= V_{OS}$  (ie. o/p = 1)

→ If  $i_{lp}$  voltage is increased beyond ' $V_{TO}$ ', the driver starts conducting a non-zero drain current, but in this case MOSFET is initially in saturation because initially as,  $V_{out} = V_{DS} = V_{DD}$  which is larger than  $(V_{in} - V_{TO})$ ,

Thus, in saturation drain current is given by,

$$I_D = I_R = \frac{K_n}{2} (V_{in} - V_{TO})^2 \quad I_D = I_R = \frac{K_n}{2} (V_{in} - V_{TO})^2$$

→ Now, with increasing  $i_{lp}$  voltage, the drain current of driver  $x_{tar}$  also increases & o/p voltage  $V_{out}$  starts to drop. Eventually, for  $i_{lp}$  voltage larger than  $(V_{out} + V_{TO})$ ,  $x_{tar}$  enters into a linear mode. & Current is,

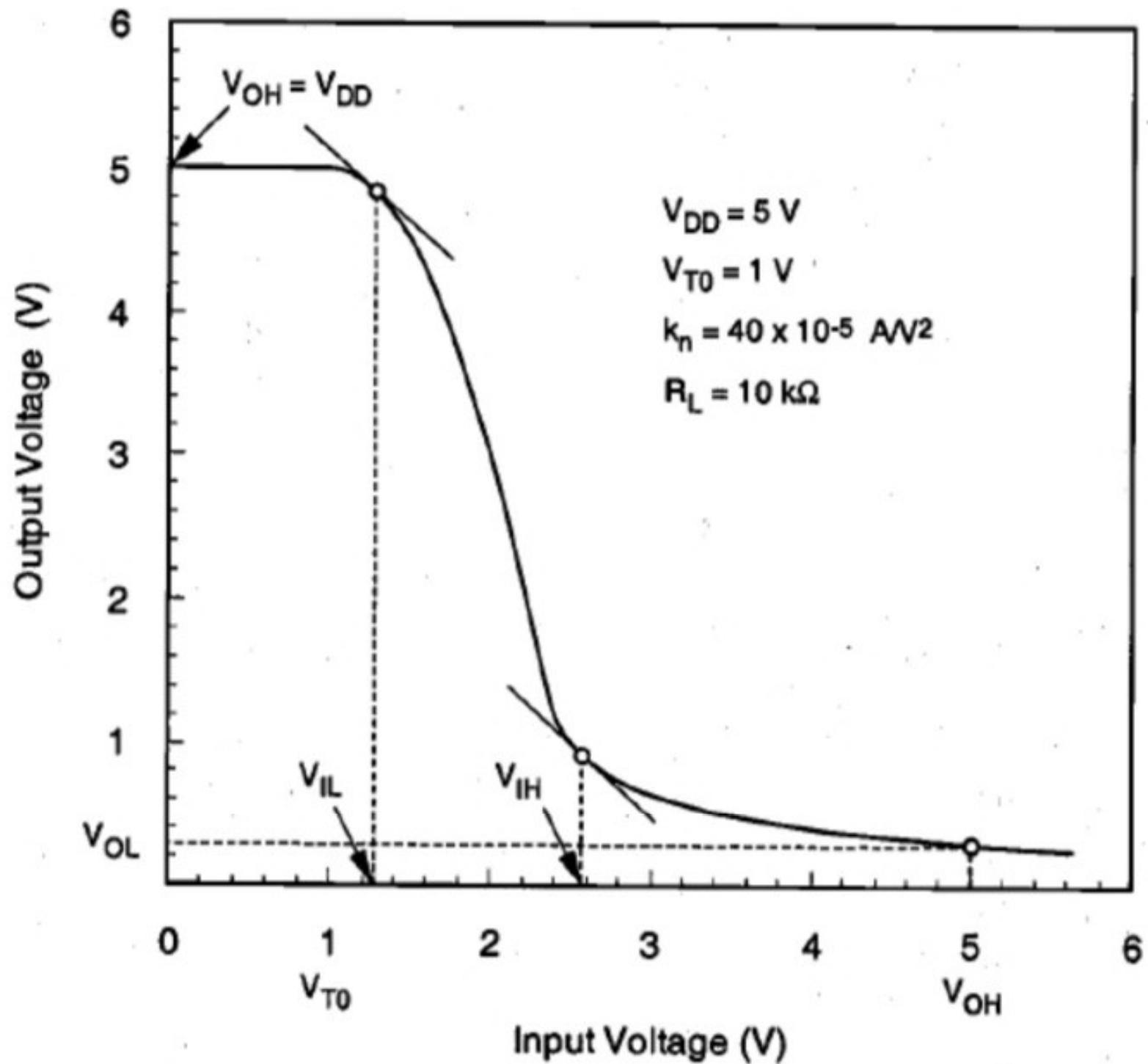
$$I_D = I_R = \frac{K_n}{2} \left[ 2(V_{in} - V_{TO}) \cdot V_{out} - V_{out}^2 \right]$$

→ Various operating regions of xtor is listed as,

I <sub>lp</sub> voltage Range	Operating mode
$V_{in} < V_{TO}$	Cut-off
$V_{TO} \leq V_{in} < V_{out} + V_{TO}$	Saturation
$V_{in} \geq V_{out} + V_{TO}$	Linear

$$\begin{aligned}V_{in} &< V_{TO} \leftarrow \\V_{in} &< V_{out} + V_{TO}\end{aligned}$$

→ following fig. shows VTC of R-load inverter ckt.



# ① Calculation of $V_{OH}$

→ From the outer loop of CKT, o/p voltage is given by,

$$V_{out} = V_{DD} - R_L \cdot I_R \quad \rightarrow ①$$

When the o/p voltage is low i.e.  $V_{in} < V_{TO}$ , the xtr is cut-off & current is zero. i.e.  $I_R = I_0 = 0$

∴ we can write from eqn ①

$$V_{out} = V_{OH} = V_{DD}$$

## ② Calculation of $V_{OL}$

→ To calculate ' $V_{OL}$ ' we assume that 'ilp' voltage =  $V_{OH}$   
ie.  $V_m = V_{OH} = V_{DD}$

As,  $V_m - V_{TO} > V_{out}$  the xtr operates in linear mode

$$\text{& from eqn } ① \quad I_R = \frac{V_{DD} - V_{out}}{R_L} \quad \rightarrow ②$$

$$\text{As } I_R = I_D$$

$$\frac{V_{DD} - V_{OL}}{R_L} = \frac{k_n}{2} \left[ 2(V_{DD} - V_{TO}) \cdot V_{OL} - V_{OL}^2 \right]$$

After Simplifying eqn we get,

$$V_{OL}^2 - 2 \cdot \left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right) \cdot V_{OL} + \frac{2}{KnRL} \cdot V_{DD} = 0$$

This is quadratic eqn where,

$$a=1, b= -2 \left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right), c = \frac{2 \cdot V_{DD}}{KnRL}$$

whose soln for  $V_{OL}$  is,

$$V_{OL} = \frac{+2 \left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right) \pm \sqrt{\left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right)^2 - 4 \left( \frac{2 \cdot V_{DD}}{KnRL} \right)}}{2}$$

→ As the value of  $V_{OL}$  must be b/w 0 &  $V_{DD}$  hence  
we can write,

$$V_{OL} = \left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right) - \sqrt{\left( V_{DD} - V_{TO} + \frac{1}{KnRL} \right)^2 - \frac{2 \cdot V_{DD}}{KnRL}}$$

### ③ Calculation of $V_{IL}$

- By def<sup>n</sup> of  $V_{IL}$ , which is smaller of the two s/p voltage values @ which  $\frac{dV_{out}}{dV_m} = -1$
- from the VTC curve it is seen that, when the s/p is equal to  $V_{IL}$ , the o/p voltage ( $V_{out}$ ) is slightly smaller than  $V_{OH}$ . Consequently  $V_{out} > V_m - V_{TO}$  & xtor operates in saturation mode.

$$\text{As, } I_R = I_D$$

$$\frac{V_{DD} - V_{out}}{R_L} = \frac{k_n}{2} (V_m - V_{TO})^2 \quad \longrightarrow ①$$

Dibb. above eqn w.r.t.  $V_m$  we get,

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_m} = \frac{k_n}{2} \cdot 2(V_m - V_{TO}) \quad \left\{ \begin{array}{l} V_{DD}, R_L, V_{TO} \\ \text{constants} \end{array} \right\}$$

but  $\frac{dV_{out}}{dV_m} = -1$

$$\therefore \text{we get, } \frac{1}{R_L} = K_n(V_{in} - V_{TO})$$

but @ slope = -1,  $V_{in} = V_{IL}$  put in above eqn,

$$\therefore \frac{1}{R_L} = K_n(V_{IL} - V_{TO})$$

Simplify we get, 
$$V_{IL} = V_{TO} + \frac{1}{K_n R_L} \longrightarrow ②$$

& value of o/p voltage when  $V_{in} = V_{IL}$  can be found by  
putting eqn ② in eqn ①

we get 
$$V_{out}(V_{in}=V_{IL}) = V_{DD} - \frac{1}{2K_n R_L}$$

#### ④ Calculation of $V_{IH}$ :-

→ As shown on VTC curve,  $V_{IH}$  is the larger of the two voltage points at which Slop,  $\frac{dV_{out}}{dV_{in}} = -1$

→ It is seen from graph that, when ilp voltage =  $V_{IH}$ , the olp voltage  $V_{out}$  is slightly larger than olp low voltage ' $V_{OL}$ '. ie.  $V_{out} < V_{in} - V_{TO}$  & xtr operates in the linear Region.

$$\text{As, } I_R = I_D$$

$$\therefore \frac{V_{OD} - V_{out}}{R_L} = \frac{K_n}{2} \left[ 2(V_{in} - V_{TO}) \cdot V_{out} - V_{out}^2 \right] \rightarrow ①$$

Diff. above eqn w.r.t. ' $V_{in}$ ', we get

$$-\frac{1}{R_L} \cdot \frac{dV_{out}}{dV_{in}} = \frac{K_n}{2} \left[ 2(V_{in} - V_{TO}) \cdot \frac{dV_{out}}{dV_{in}} + 2V_{out} - 2V_{out} \cdot \frac{dV_{out}}{dV_{in}} \right]$$

put  $\frac{dV_{out}}{dV_{in}} = -1$  at  $V_m = V_{IH}$  in above eqn

$$-\frac{1}{R_L}(-1) = Kn \left[ (V_{IH} - V_{TO})(-1) + V_{out} - V_{out}(-1) \right]$$

$$\frac{1}{R_L} = Kn \left[ -(V_{IH} - V_{TO}) + 2V_{out} \right]$$

After simplifying we get,

$$V_{IH} = V_{TO} + 2V_{out} - \frac{1}{KnR_L} \rightarrow ③$$

Thus, we get two algebraic eqn, i.e. eqn ① & ③, for two unknowns  $V_{IH}$  &  $V_{out}$ . To determine them, put eqn ③ in eqn ①,

directly, we get  $V_{out}(V_{in}=V_{IH}) = \sqrt{\frac{2}{3} \cdot \frac{V_{DD}}{KnR_L}}$

put this eqn in ③

we get,

$$V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{KnR_L}} - \frac{1}{KnR_L}$$

Imp → Thus, four critical voltage points  $V_{OH}$ ,  $V_{OL}$ ,  $V_{IH}$ ,  $V_{IL}$  can be used to find Noise Margin,  $NML$  &  $NMH$ . of R-load Inverter CKT.

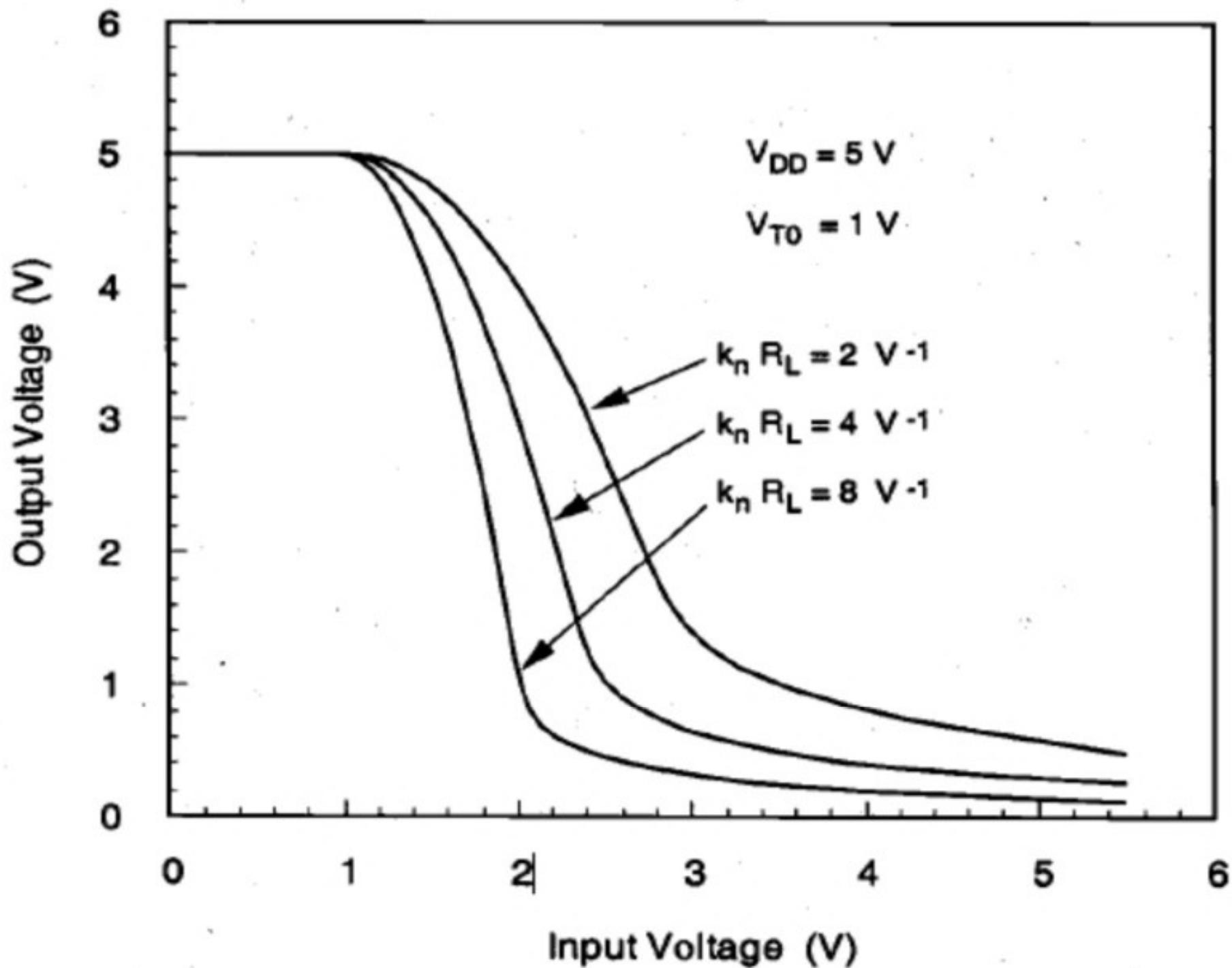
Imp → from all these eqn, it is seen that term ( $K_n R_L$ ) is only the design parameter.

→ following graph shows the VTC of R-Load, for different values of ( $K_n R_L$ ).

→ It is seen from VTC, that, Large value of  $K_n R_L$  approaches the ideal inverter slope.

→ But its value involve other Trade-off with the Area & power consumption of the CKT.

# VTC Curve of R-Load



## # Power Consumption & chip-area #

→ The Avg. DC power of R-load inverter CKT is found by considering two cases,

**Case-I**  $V_{in} = V_{OL}(\text{Low}) \rightarrow$  In this case, driver xtar is in cut-off, hence no current flows in the CKT  
 $\therefore I_D = I_R = 0$  & DC power dissipation = 0

**Case-II**  $V_{in} = V_{OH}(\text{High}) \rightarrow$  In this case, both xtar & load conducts a current, since o/p voltage in this case is  $V_{OL}$   
the current drawn from the power supply is, case is  $V_{in}$

$$I_D = I_R = \frac{V_{DD} - V_{OL}}{R_L}$$

$$I_D = I_R = \frac{V_{DD} - V_{OL}}{R_L}$$

→ Assuming that o/p voltage is low during 50% of the open time & high during remaining 50% time.

Then, the avg. DC power consumption of the inverter is,

$$P_{avg(DC)} = \frac{ON + OFF}{2} = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$$

$$P_{avg(DC)} = \frac{V_{DD}}{2} \cdot \frac{V_{DD} - V_{OL}}{R_L}$$

Chip Area → The chip area occupied by the R-load inverter ckt depends on two parameters

①  $(\frac{W}{L})$  ratio of the Driver xtor. ①  $(\frac{W}{L}) \rightarrow x_{tor}$

② The value of 'RL'

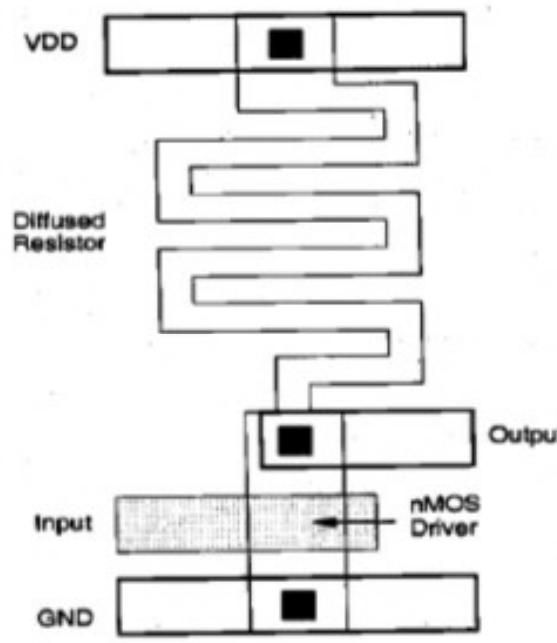
②  $R_L$

① diffused Resistor @ polysilicon resistor

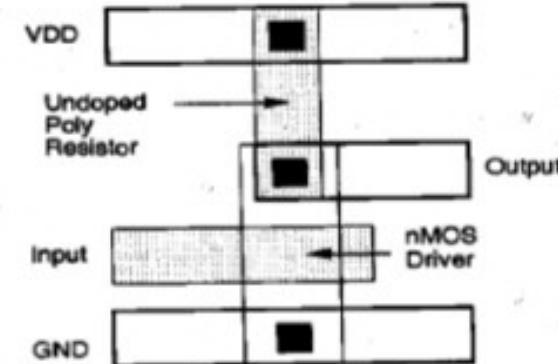
→ There are two methods of Resistor fabricating

① Diffused Resistor & ② Polysilicon Resistor.

→ fig. shows the area taken by both tech.



(a)



(b)

④ Consider a resistive load inverter ckt with  $V_{DD} = 5V$ ,  
 $K_n = 20 \mu A/V^2$ ;  $V_{TO} = 0.8V$ ;  $R_L = 200K\Omega$  &  $\frac{W}{L} = 2$ .  
 calculate the critical voltages ( $V_{OH}$ ,  $V_{OL}$ ,  $V_{IL}$ ,  $V_{IH}$ ) on  
 the VTC & find the noise margin of the ckt.

Soln → The Driver ckt is NMOS, whose Transconductance ( $K_n$ )  
 is given as,

$$K_n = K_n \left( \frac{W}{L} \right) = 20 \times 2 = 40 \mu A/V^2$$

$$\left[ \Omega = \frac{V}{A} \right]$$

$$\therefore K_n R_L = 40 \times 10^6 \frac{A}{V^2} \times 200 \times 10^3 \frac{V}{A}$$

$$\therefore K_n R_L = 8 V^1$$

$$\boxed{\textcircled{1} \quad V_{OH} = V_{DD} = 5V}$$

$$\textcircled{2} \quad V_{OL} = V_{DD} - V_{TO} + \frac{1}{KnR_L} - \sqrt{\left(V_{DD} - V_{TO} + \frac{1}{KnR_L}\right)^2 - \frac{2V_{DD}}{KnR_L}}$$

$$= 5 - 0.8 + \frac{1}{8} - \sqrt{(5 - 0.8 + \frac{1}{8})^2 - \frac{2 \times 5}{8}}$$

$\therefore \boxed{V_{OL} = 0.147 \text{ V}}$

$$\textcircled{3} \quad V_{IL} = V_{TO} + \frac{1}{KnR_L} = 0.8 + \frac{1}{8}$$

$\therefore \boxed{V_{IL} = 0.925 \text{ V}}$

$$\textcircled{4} \quad V_{IH} = V_{TO} + \sqrt{\frac{8}{3} \cdot \frac{V_{DD}}{KnR_L} - \frac{1}{KnR_L}}$$

$$= 0.8 + \sqrt{\frac{8}{3} \cdot \frac{5}{8}} - \frac{1}{8}$$

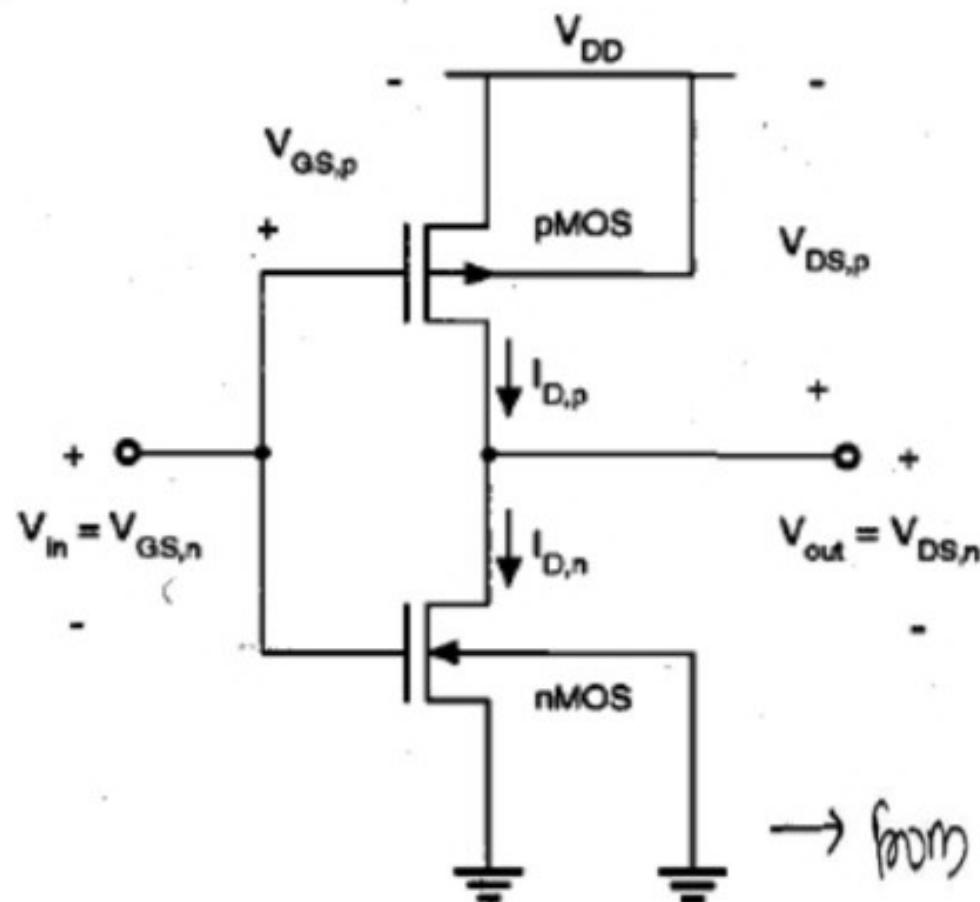
$\boxed{V_{IH} = 1.97 \text{ V}}$

$\Rightarrow$  Now, Noise Margin  $NM_L = V_{IL} - V_{OL} = 0.93 - 0.147$   
 $\qquad\qquad\qquad \underline{\underline{0.78 \text{ V}}}$

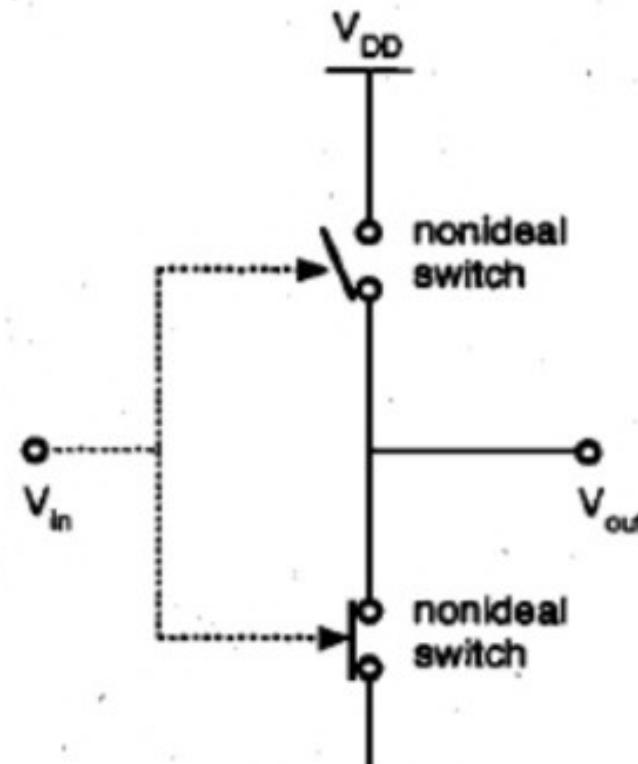
 $NM_H = V_{OH} - V_{IH} = 5 - 1.97 \approx \underline{\underline{3.03 \text{ V}}}$

# CMOS Inverter

➤ Following fig. shows CMOS Inverter which consist of an enhancement NMOS & PMOS structure acting as driver & load respectively.



(a)



→ from the CKT,  $V_{GS,n} = V_{in}$  &  $V_{DS,n} = V_{out}$

& also,  $V_{GS,p} = V_{in} - V_{DD}$  &  $V_{DS,p} = V_{out} - V_{DD}$

$$V_{GS,n} = V_{in}$$
$$V_{DS,n} = V_{out}$$

- As shown in fig, the input voltage is connected to the gate terminals of both the nmos & p-mos xtor, thus both the xtors driven directly by ilp signal 'Vin'.
- The substrate of N+mos xtor is connected to the ground, while substrate of p-mos xtor is to 'VDD' in order to reverse bias the source & drain junction.
- from the CKT,  $V_{GS,n} = Vin$  &  $V_{DS,n} = V_{out}$   
 & also,  $V_{GS,p} = Vin - V_{DD}$  &  $V_{DS,p} = V_{out} - V_{DD}$

$$V_{GS,n} = Vin \quad \& \quad V_{DS,n} = V_{out}$$

$$V_{GS,p} = Vin - V_{DD}$$

$$V_{DS,p} = V_{out} - V_{DD}$$

### Case-I

If  $V_{in} < V_{TO,n}$

i.e.  $V_{in} < \text{Threshold voltage of n-mos}$

$$V_{in} < V_{TO,n}$$

→ The n-mos xtor is cut-off & at the same time pmos xtor is ON, operating in linear region. Since, the drain current of both the xtor is zero,  
i.e.  $I_{D,n} = I_{D,p} = 0$

& output voltage  $V_{out} = V_{OH} = V_{DD}$

$$n\text{-mos} \rightarrow \text{cutoff}$$

$$p\text{-mos} \rightarrow \text{ON}$$

$$I_D = 0 \rightarrow V_{out} = V_{OH} = V_{DD}$$

### Case-II

If  $V_{in} > V_{DD} + V_{TO,p}$

$V_{in} > V_{DD} + V_{TO,p}$ , n-mos = ON  
pmos → cutoff,  $n\text{-mos} \rightarrow \text{ON}$   
 $V_{out} = V_{OL} = 0$

→ The pmos xtor is cut-off & n-mos xtor is ON operating in linear region.

& output voltage  $V_{out} = V_{OL} = 0$

$$V_{in} > V_{TO,n} \\ V_{DS,n} > V_{BS} - V_I$$

### Case-III

Both these xtors operates in saturation region if, for NMOS,  $V_{in} > V_{TO,n}$  & if following cond' satisfy,

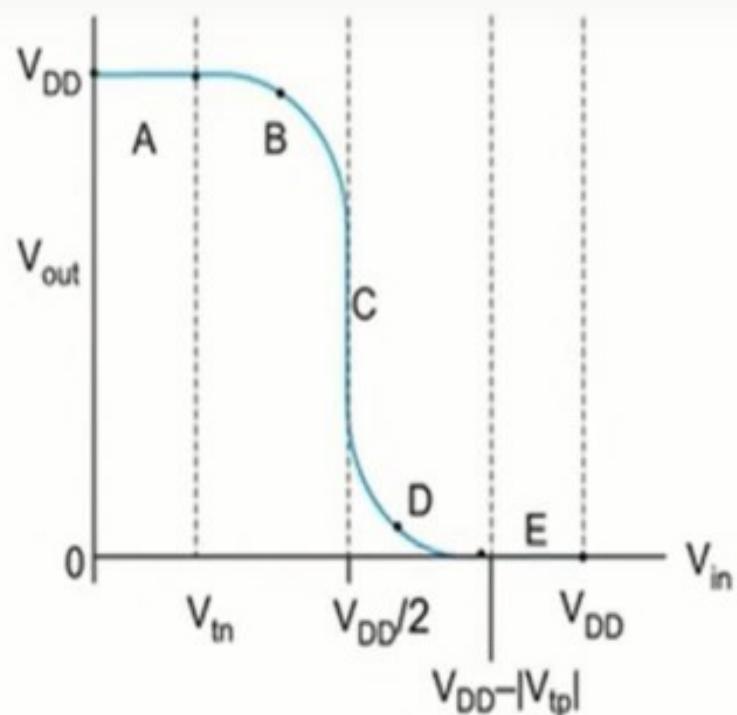
$$V_{DS,n} > V_{GS,n} - V_{TO,n}$$

i.e.  $V_{out} > V_{in} - V_{TO,n}$

& for pmos,  $V_{in} < (V_{DD} + V_{TO,p})$  & if following cond' satisfy,

$$V_{DS,p} \leq V_{GS,p} - V_{TO,p}$$

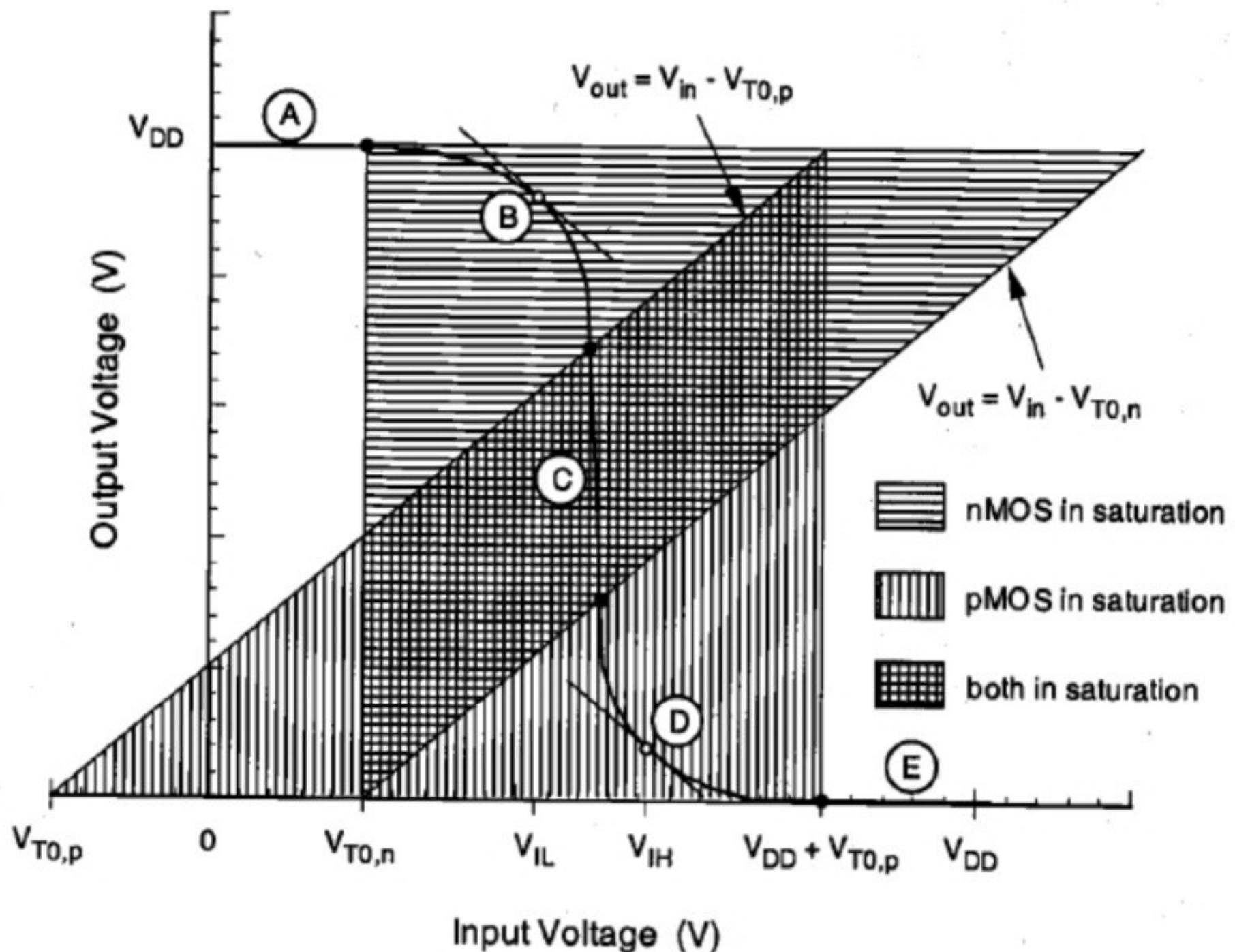
i.e.  $V_{out} \leq V_{in} - V_{TO,p}$



	Cutoff	Linear	Saturated
nMOS	$V_{gsn} < V_{tn}$	$V_{gsn} > V_{tn}$	$V_{gsn} > V_{tn}$
	$V_{in} < V_{tn}$	$V_{in} > V_{tn}$	$V_{in} > V_{tn}$
		$V_{dsn} < V_{gsn} - V_{tn}$	$V_{dsn} > V_{gsn} - V_{tn}$
		$V_{out} < V_{in} - V_{tn}$	$V_{out} > V_{in} - V_{tn}$
pMOS	$V_{gsp} > V_{tp}$	$V_{gsp} < V_{tp}$	$V_{gsp} < V_{tp}$
	$V_{in} > V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$	$V_{in} < V_{tp} + V_{DD}$
		$V_{dsp} > V_{gsp} - V_{tp}$	$V_{dsp} < V_{gsp} - V_{tp}$
		$V_{out} > V_{in} - V_{tp}$	$V_{out} < V_{in} - V_{tp}$

Region	Condition	p-device	n-device	Output
A	$0 \leq V_{in} < V_{tn}$	linear	cutoff	$V_{out} = V_{DD}$
B	$V_{tn} \leq V_{in} < V_{DD}/2$	linear	saturated	$V_{out} > V_{DD}/2$
C	$V_{in} = V_{DD}/2$	saturated	saturated	$V_{out}$ drops sharply
D	$V_{DD}/2 < V_{in} \leq V_{DD} -  V_{tp} $	saturated	linear	$V_{out} < V_{DD}/2$
E	$V_{in} > V_{DD} -  V_{tp} $	cutoff	linear	$V_{out} = 0$

# VTC Curve of CMOS Inverter



# # Calculation of the Critical voltage points on VTC #

$$\textcircled{1} \quad V_{OH} = V_{DD} \quad ; \quad \textcircled{2} \quad V_{OL} = 0$$

SKIP

## ③ Calculation of V<sub>IL</sub> :-

By the defn, slope of the VTC, ie.  $\frac{dv_{out}}{dV_{in}} = -1$

when  $V_{in} = V_{IL}$ . In this case, the n-mos xtrs operates in saturation while p-mos xtrs operates in linear region.  
(Refer table),

from  $I_{D,n} = I_{D,p}$  we get,

$$\frac{Kn}{2} (V_{GS,n} - V_{TO,n})^2 = \frac{Kp}{2} [2 \cdot (V_{GS,p} - V_{TO,p}) V_{DS,p} - V_{DS,p}^2]$$

As we have,  $V_{GS,n} = V_{in}$  ;  $V_{GS,p} = V_{in} - V_{DD}$  ;  $V_{DS,p} = V_{out} - V_{DD}$

put in above eqn we get,

$$\frac{Kn}{2} \cdot (V_{in} - V_{TO,n})^2 = \frac{Kp}{2} [2 \cdot (V_{in} - V_{DD} - V_{TO,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

$\Rightarrow$  Differentiate both sides w.r.t.  $V_m$ :

SKIP

$$\frac{K_n}{2} \cdot 2(V_{in} - V_{T0,n}) = \frac{K_p}{2} \left[ 2(V_m - V_{DD} - V_{T0,p}) \left( \frac{dV_{out}}{dV_m} \right) + (V_{out} - V_{DD}) - 2(V_{out} - V_{DD}) \left( \frac{dV_{out}}{dV_m} \right) \right]$$

$$K_n(V_m - V_{T0,n}) = K_p \left[ (V_m - V_{DD} - V_{T0,p}) \left( \frac{dV_{out}}{dV_m} \right) + (V_{out} - V_{DD}) - (V_{out} - V_{DD}) \cdot \left( \frac{dV_{out}}{dV_m} \right) \right]$$

put  $V_m = V_{IL}$  &  $\frac{dV_{out}}{dV_m} = -1$ , in above eqn

$$K_n(V_{IL} - V_{T0,n}) = K_p \left[ (V_{IL} - V_{DD} - V_{T0,p})(-1) + (V_{out} - V_{DD}) - (V_{out} - V_{DD})(-1) \right]$$

we get,

$$K_n(V_{IL} - V_{T0,n}) = K_p(2V_{out} - V_{IL} + V_{T0,p} - V_{DD})$$

It can be rearrange as,

$$V_{IL} = \frac{2V_{out} + V_{T0,p} - V_{DD} + K_n V_{T0,n}}{1 + K_p}$$

where,  $K_p = \frac{K_n}{K_p}$

#### ④ Calculation of $V_{IH}$

SKIP

→ When  $V_m = V_{IH}$ , NMOS operates in linear region & PMOS operates in saturation region.

→ AS,  $I_{D,n} = I_{D,p}$

$$\frac{K_n}{2} \cdot [2 \cdot (V_{GS,n} - V_{TO,n}) \cdot V_{DS,n} - V_{DS,n}^2] = \frac{K_p}{2} \cdot (V_{GS,p} - V_{TO,p})^2$$

put,  $V_{GS,n} = V_m$  ;  $V_{DS,n} = V_{out}$  ;  $V_{GS,p} = V_m - V_{DD}$

we get,

$$\frac{K_n}{2} \left[ 2(V_m - V_{TO,n}) \cdot V_{out} - V_{out}^2 \right] = \frac{K_p}{2} \cdot (V_m - V_{DD} - V_{TO,p})^2$$

Differentiate above eqn w.r.t ' $V_m$ '

$$\begin{aligned} \frac{K_n}{2} \left[ 2(V_m - V_{TO,n}) \left( \frac{dV_{out}}{dV_m} \right) + V_{out} - 2V_{out} \left( \frac{dV_{out}}{dV_m} \right) \right] \\ = \frac{K_p}{2} \cdot 2(V_m - V_{DD} - V_{TO,p}) \end{aligned}$$

$$\text{ie. } K_n \left[ (V_{in} - V_{TO,n}) \left( \frac{dv_{out}}{dV_{in}} \right) + V_{out} - V_{out} \left( \frac{dV_{out}}{dV_{in}} \right) \right] \\ = K_p (V_{in} - V_{DD} - V_{TO,p})$$

put  $V_{in} = V_{IH}$  &  $\frac{dV_{out}}{dV_{in}} = -1$  in above eqn

$$K_n \left[ (V_{IH} - V_{TO,n})(-1) + V_{out} - V_{out}(-1) \right] = K_p (V_{IH} - V_{DD} - V_{TO,p})$$

we get,

$$K_n (-V_{IH} + V_{TO,n} + 2V_{out}) = K_p (V_{IH} - V_{DD} - V_{TO,p})$$

Rearranging we get,

$$V_{IH} = \frac{V_{DD} + V_{TO,p} + K_p \cdot (2V_{out} + V_{TO,n})}{1 + K_p}$$

where,  $K_R = \frac{K_n}{K_p}$

⑤ Calculation of  $V_{th}$  (ie. Inverter Threshold voltage)

It is defined as,  $V_{th} = V_{in} = V_{out}$ , both transistors are Skip  
expected to be in saturation

As we have,  $I_{D,n} = I_{D,p}$

$$\therefore \frac{K_n}{2} (V_{GS,n} - V_{TO,n})^2 = \frac{K_p}{2} (V_{GS,p} - V_{TO,p})^2$$

Put  $V_{GS,n} = V_{in}$  &  $V_{GS,p} = V_{in} - V_{DD}$  in above eqn,

$$\frac{K_n}{2} (V_{in} - V_{TO,n})^2 = \frac{K_p}{2} (V_{in} - V_{DD} - V_{TO,p})^2$$

$$K_n (V_{in} - V_{TO,N})^2 = K_p (V_{in} - V_{DD} - V_{TO,P})^2$$

→ Taking sq. root on both sides

$$\sqrt{K_n} (V_{in} - V_{TO,n}) = \sqrt{K_p} (V_{in} - V_{DD} - V_{TO,p})$$

Rearrange this eqn we get,

$$V_{in} \left( 1 + \sqrt{\frac{K_p}{K_n}} \right) = V_{TO,n} + \sqrt{\frac{K_p}{K_n}} \cdot (V_{DD} + V_{TO,p})$$

- Thus, Inverter Threshold voltage,

$$V_{th} = V_{ih} = \frac{V_{TO,n} + \sqrt{\frac{1}{K_R}} (V_{DD} + V_{TO,p})}{1 + \sqrt{\frac{1}{K_R}}} \quad \cancel{=}$$

$$\text{where, } K_R = \frac{K_n}{K_p}$$

(eg) Consider a CMOS inverter CKT with the following parameters,  
 $V_{DD} = 3.3V$ ;  $V_{TO,n} = 0.6V$ ;  $V_{TO,p} = -0.7V$ ;  
 $K_n = 200 \mu A/V^2$ ;  $K_p = 80 \mu A/V^2$   
Calculate the noise margin of the CKT.

$$\rightarrow K_R = \frac{K_n}{K_p} = \frac{200 \mu A/V^2}{80 \mu A/V^2} = 2.5$$

$$\rightarrow \text{We have } V_{OH} = V_{DD} = 3.3V \\ V_{OL} = 0V$$

Now, To find  $V_{IL}$  we have,

$$V_{IL} = \frac{2V_{out} + V_{TO,p} - V_{DD} + K_R V_{TO,n}}{1+K_R}$$

$$= \frac{2V_{out} - 0.7 - 3.3 + (2.5)(0.6)}{1+2.5}$$

$$V_{IL} = 0.57 V_{out} - 0.71 \quad \longrightarrow \textcircled{1}$$

Now, To find 'V<sub>out</sub>' we have eqn.

$$\frac{K_n}{2} (V_{in} - V_{T0,n})^2 = \frac{K_p}{2} [2(V_{in} - V_{DD} - V_{T0,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2]$$

The above eqn can also be written as,

$$\left(\frac{K_n}{K_p}\right) (V_{in} - V_{T0,n})^2 = 2(V_{in} - V_{DD} - V_{T0,p})(V_{out} - V_{DD}) - (V_{out} - V_{DD})^2$$

but  $V_{in} = V_{IL} = 0.57V_{out} - 0.71$  from eqn ①

put in above eqn,

$$2.5(0.57V_{out} - 0.71 - 0.6)^2 = 2(0.57V_{out} - 0.71 - 3.3 + 0.7) \\ (V_{out} - 3.3) - (V_{out} - 3.3)^2$$

After simplifying, we get,

$$0.66V_{out}^2 + 0.05V_{out} - 6.65 = 0$$

Note → find the two values of this quadratic eqn & values of  $V_{out} > 0$  should be chosen

we get,  $V_{out} = 3.14V$  put in eqn ①  
 $\therefore V_{IL} = 0.57(3.14) - 0.71$ ,  $V_{IL} = 1.08V$

Now,  
 To calculate  $V_{IH}$  we have,

$$V_{IH} = \frac{V_{DD} + V_{TO,P} + K_R \cdot (2V_{out} + V_{TO,n})}{1 + K_R}$$

$$= \frac{3.3 - 0.7 + 2.5(2V_{out} + 0.6)}{1 + 2.5} = 1.43V_{out} + 1.17 \quad \rightarrow ②$$

Again, to find ' $V_{out}$ ' we have,

$$\frac{Kn}{2} [2(V_{in} - V_{TO,n}) \cdot V_{out} - V_{out}^2] = \frac{K_P}{2} (V_{in} - V_{DD} - V_{TO,P})^2$$

The above eqn can also be written as,

$$\left(\frac{K_n}{K_p}\right) \left[ 2(V_{IH} - V_{TO,n})V_{out} - V_{out}^2 \right] = (V_{IH} - V_{DD} - V_{TO,p})^2$$

$$(2.5) \left[ 2(1.43V_{out} + 1.17 - 0.6)V_{out} - V_{out}^2 \right] = (1.43V_{out} + 1.17 - 3.3 + 0.7)^2$$

After Simplifying we get,

$$2.61V_{out}^2 + 6.94V_{out} - 2.04 = 0$$

We get,  $V_{out} = 0.27\text{V}$  put in eqn ②

$$\therefore V_{IH} = 1.43(0.27) + 1.17 \quad \boxed{V_{IH} = 1.55\text{V}}$$

$$\therefore \text{Noise Margin, } NM_L = V_{IL} - V_{OL} = 1.08 - 0 = \underline{\underline{1.08\text{V}}}$$

$$\& NM_H = V_{OH} - V_{IH} = 3.3 - 1.55 = \underline{\underline{1.75\text{V}}}.$$

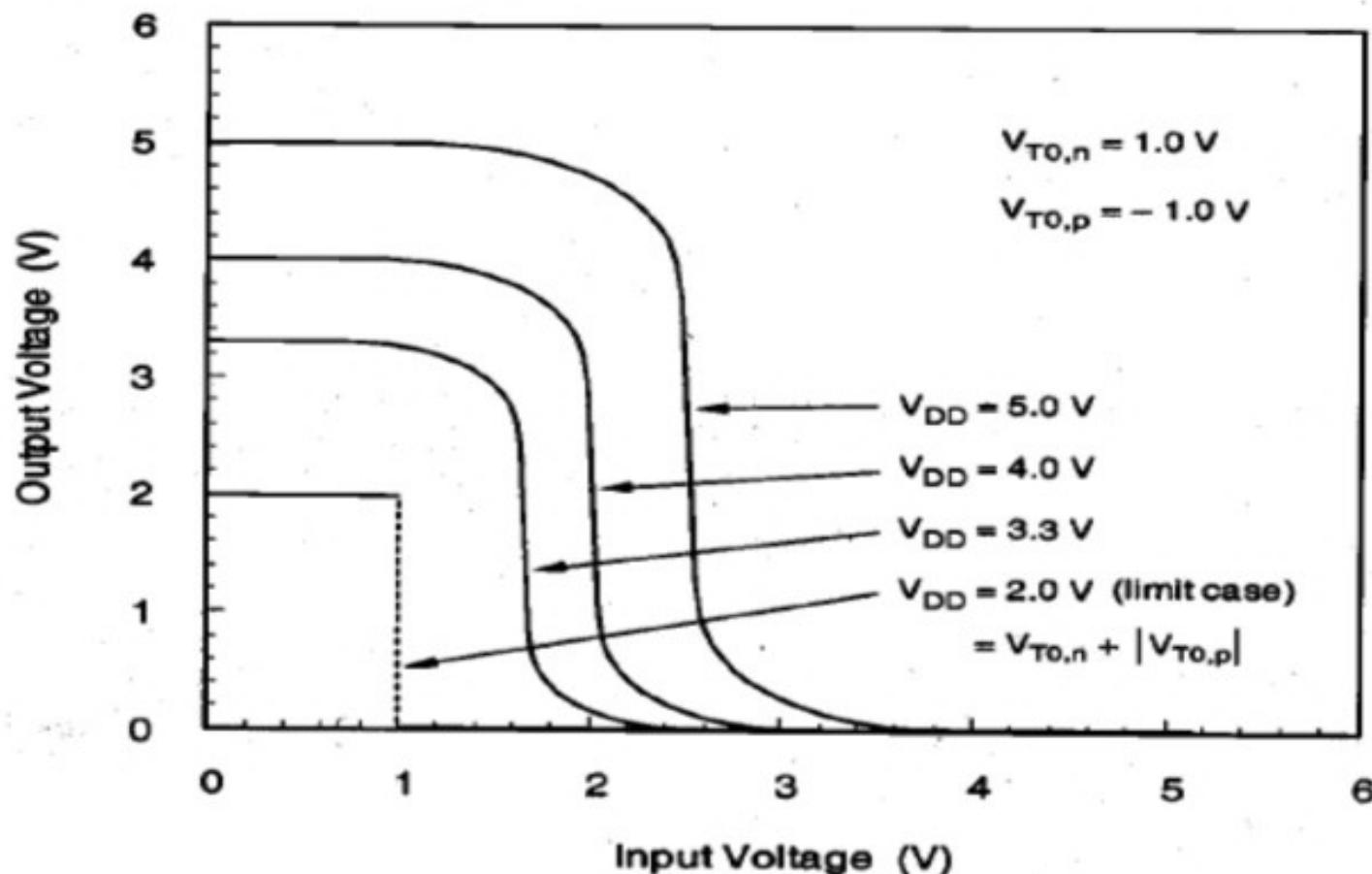
## Supply Voltage Scaling in CMOS Inverter

- The overall power dissipation of digital circuit is strong function of supply voltage  $V_{DD}$ .
- Thus, the variation of supply voltage should not affect the functionality of basic inverter circuit.
- CMOS inverter operates correctly with the following conditions,

$$V_{DD \ min} = V_{TO,N} + |V_{TO,P}|$$

- This means that correct inverter operation will be sustained if at least one of the transistor remain in conduction.

➤ Following fig. shows VTC of CMOS, obtained with different CMOS voltage levels.



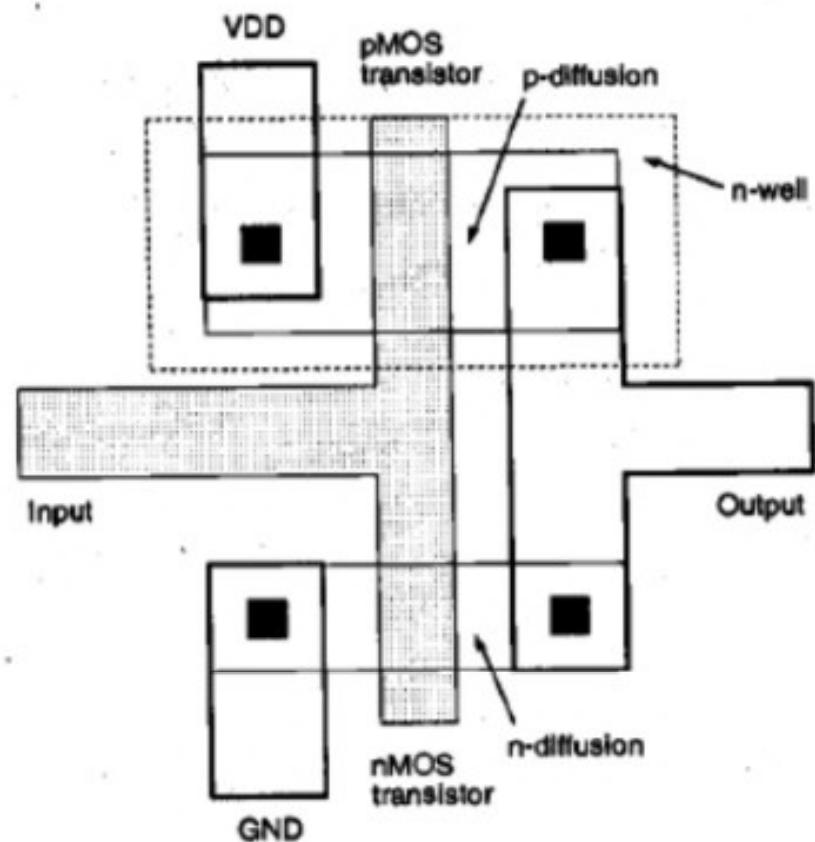
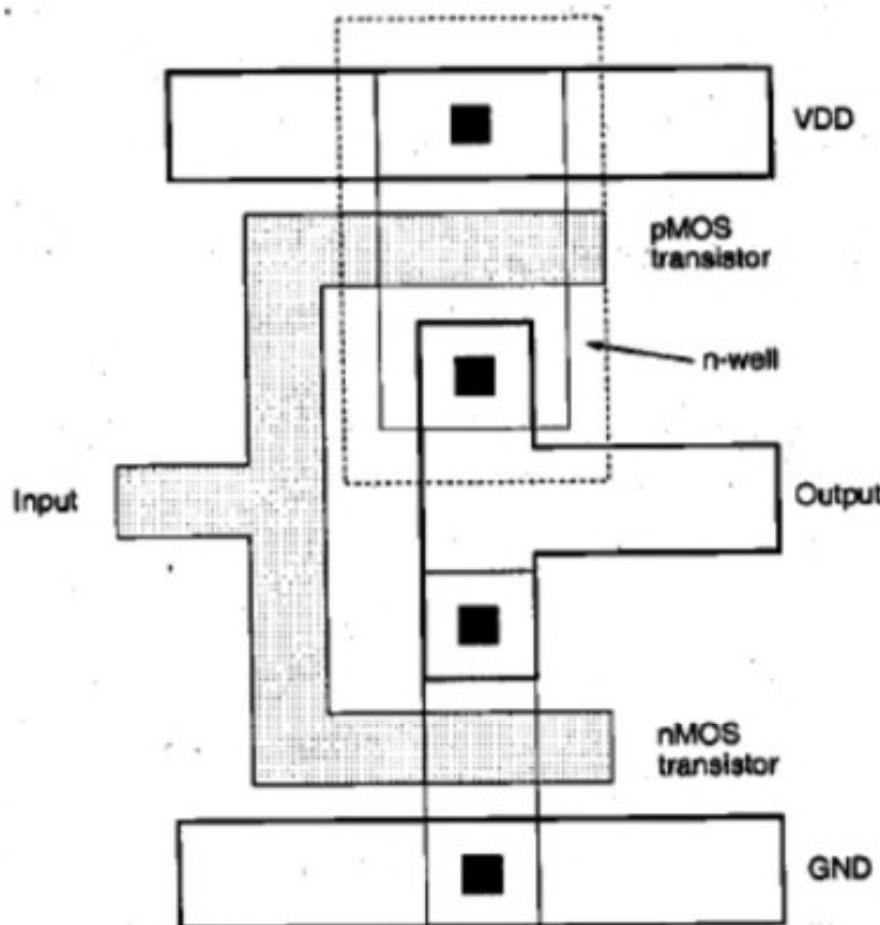
➤ From the graph, it is seen that, if the power supply voltage is reduced below the sum of two threshold voltages, the VTC contain a region in which none of the transistor is conducting.

## Power consumption in CMOS Inverter

- As the CMOS inverter does not draw a significant current from the power source in both of its steady state operating points ( ie  $V_{OH}$  &  $V_{OL}$  ) , the DC power dissipation of the circuit is almost negligible.
- Thus, in many applications where the low power consumption is preferred , CMOS inverter is preferred.

# Area considerations in CMOS Inverter

- The CMOS inverter does not occupy the significantly more Area , but complexity in the fabrication process.



# Comparison between R-load and CMOS Inverter

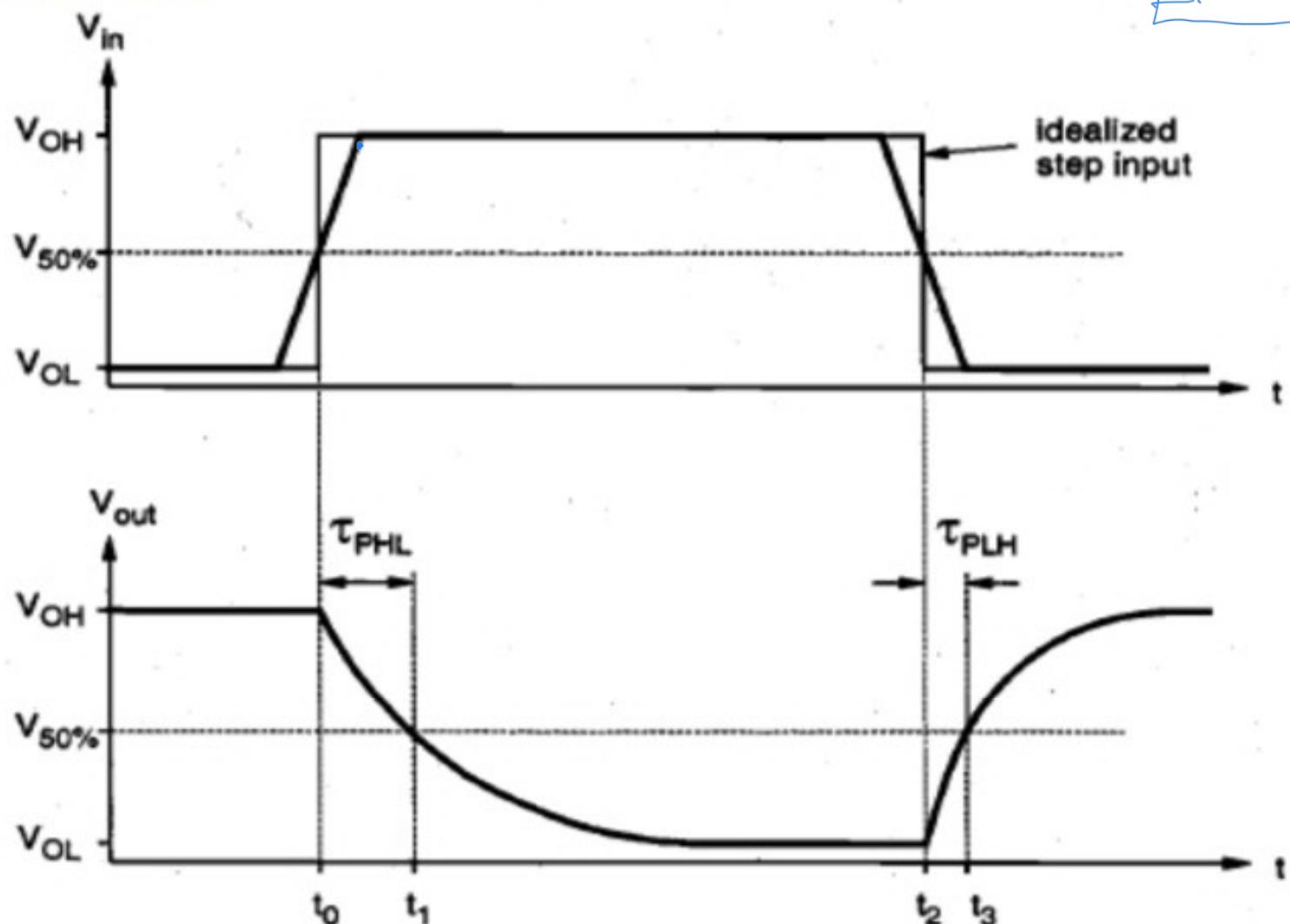
Parameters	Resistive load Inverter	CMOS Inverter
Chip area	More	Less
Power Dissipation	More	Less
Noise Margin	Less	More
Transition time	Slow	Fast
Diagram		

CA  
PD  
NM  
T  
D

# Switching Characteristics of CMOS Inverter

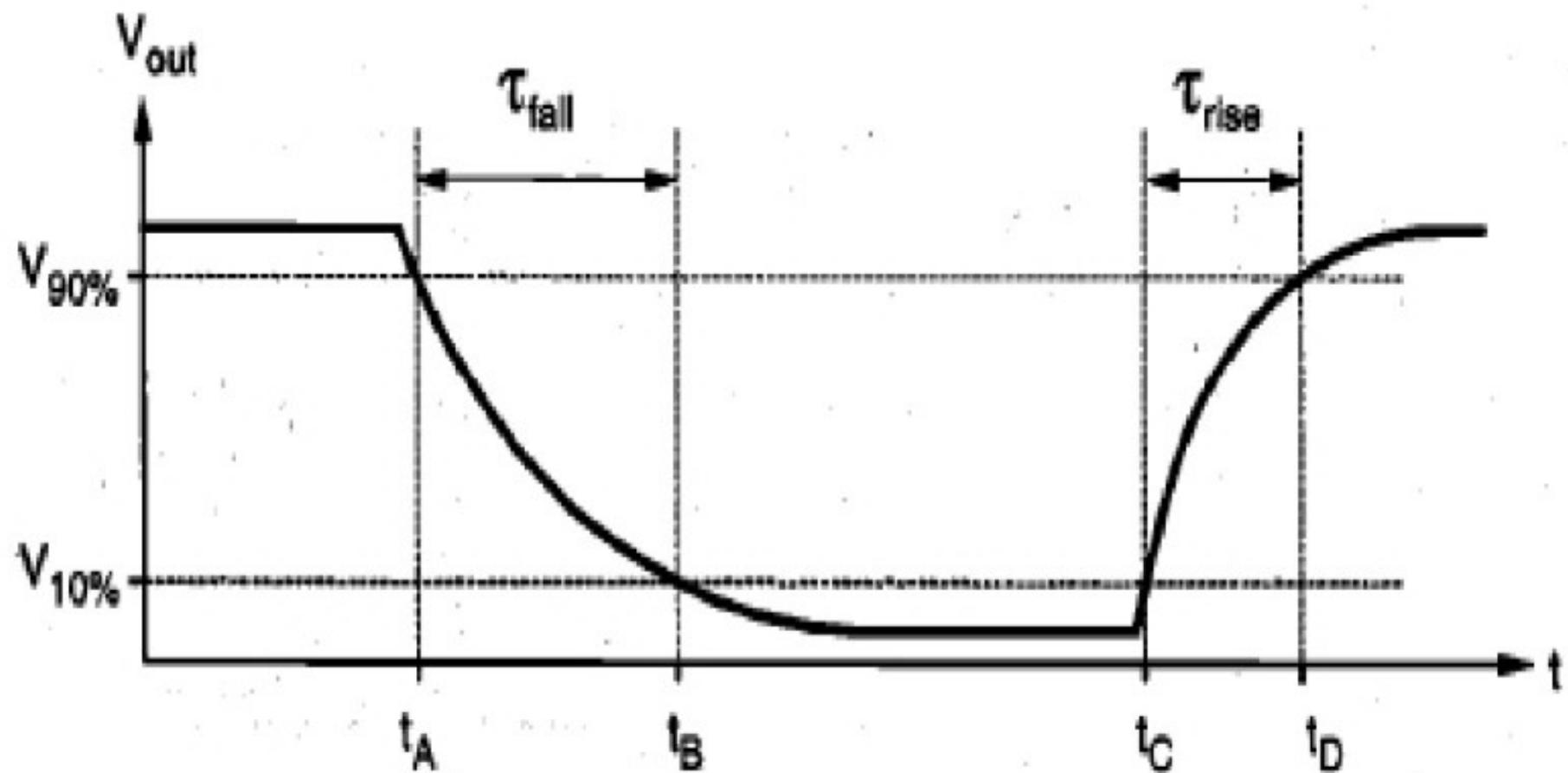
Dynamic Response

- Following fig. Shows input and output voltage waveform of an inverter



- Following fog. Shows input and output voltage waveform of an inverter,
- $T_{PHL}$  = Propagation delay during High to Low transition.
- It is defined as the time delay between the  $V_{50\%}$  transition of rising i/p voltage and the  $V_{50\%}$  transition of the falling output voltage.
- $T_{PLH}$  = Propagation delay during Low to High transition.
- It is defined as the time delay between the  $V_{50\%}$  transition of falling i/p voltage and the  $V_{50\%}$  transition of the rising output voltage.
- Where ,  $V_{50\%} = \frac{1}{2} (V_{OL} + V_{OH})$
- From fig,  $T_{PHL} = t_1 - t_0$  and  $T_{PLH} = t_3 - t_2$
- The average propagation delay of an inverter is  $(T_{PHL} + T_{PLH}) / 2$

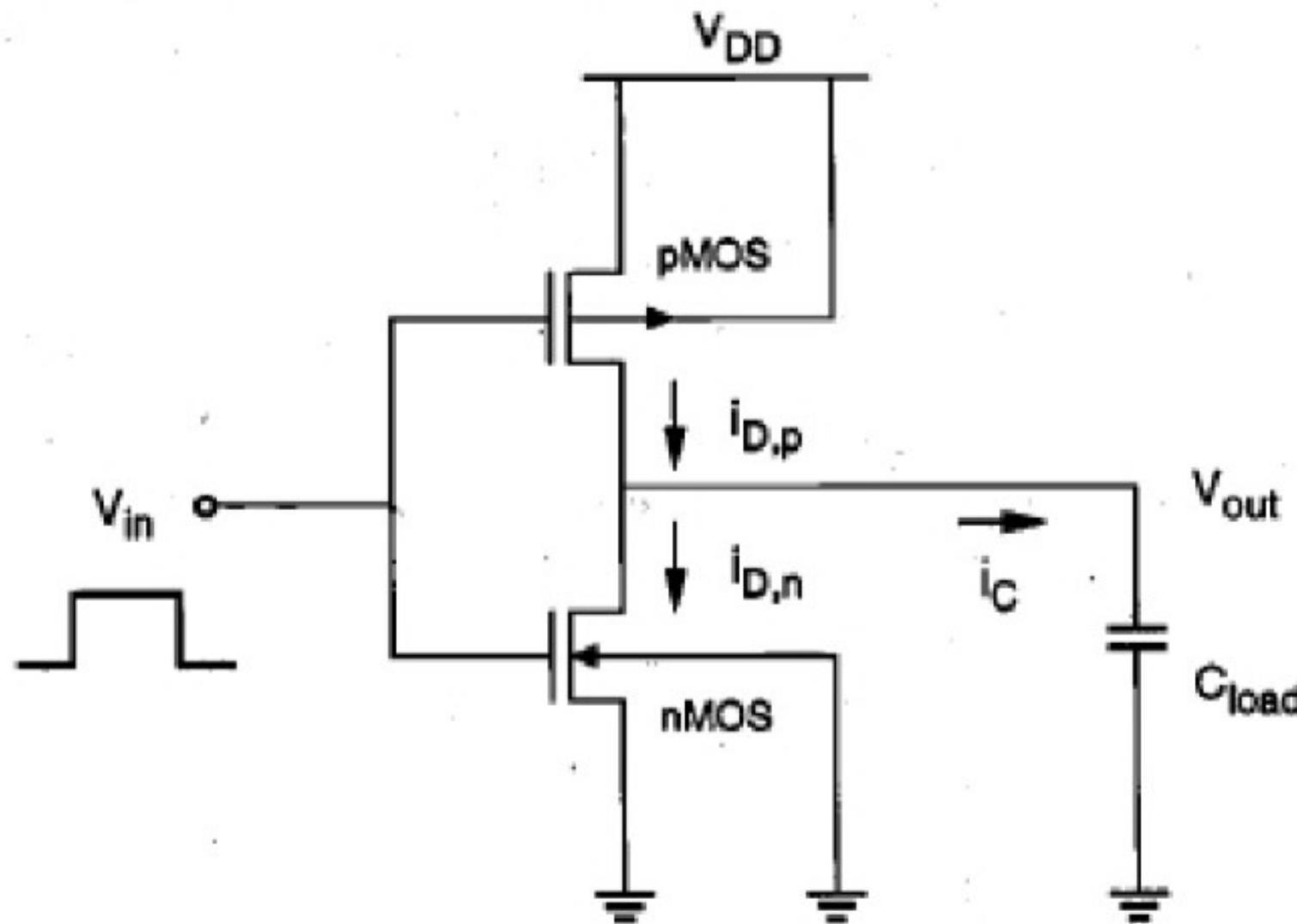
# Rise time and Fall time of CMOS Inverter



- **Rise time** :- It is defined as the time required for the output voltage to rise from  $V_{10\%}$  to  $V_{90\%}$  level.
- **Fall time** :- It is defined as the time required for the output voltage to drop from  $V_{90\%}$  to  $V_{10\%}$  level.

➤ Where ,  $V_{10\%} = V_{OL} + 0.1 (V_{OH} - V_{OL})$   
 $V_{90\%} = V_{OL} + 0.9 (V_{OH} - V_{OL})$

# Calculation of Delay time of CMOS Inverter



## # Calculation of Delay time #

→ Consider the following CMOS inverter ckt  
As shown, the capacitance current is function of the output voltage & is given by,

$$C_{\text{load}} \frac{dV_{\text{out}}}{dt} = i_C \quad \left[ \because i_C = C \frac{dV}{dt} \right]$$

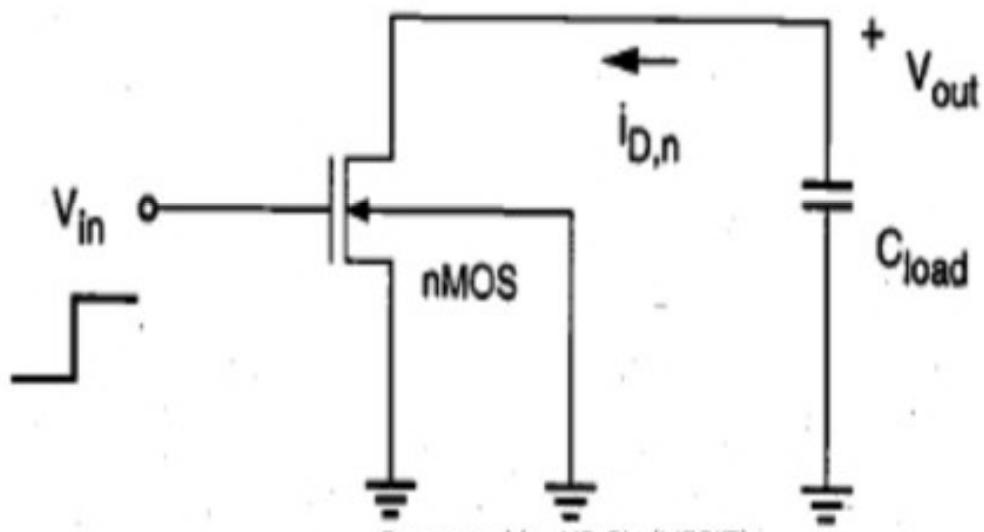
from Fig,  $i_{D,P} = i_{D,N} + i_C$   
 $\therefore i_C = i_{D,P} - i_{D,N}$  put in above eqn

$$C_{\text{load}} \frac{dV_{\text{out}}}{dt} = i_{D,P} - i_{D,N} \rightarrow ①$$

⇒ Let us consider the rising input case of CMOS Inverter,  
& assume, initially output voltage =  $V_{OH}$

So, when input voltage switches from low ( $V_{OL}$ ) to high ( $V_{OH}$ ) [ie.  $\sqcap$ ], the NMOS xitor is turned ON & it starts to discharge the load capacitance,

at the same time PMOS xitor is off  
ie.  $i_{D,P} \approx 0$



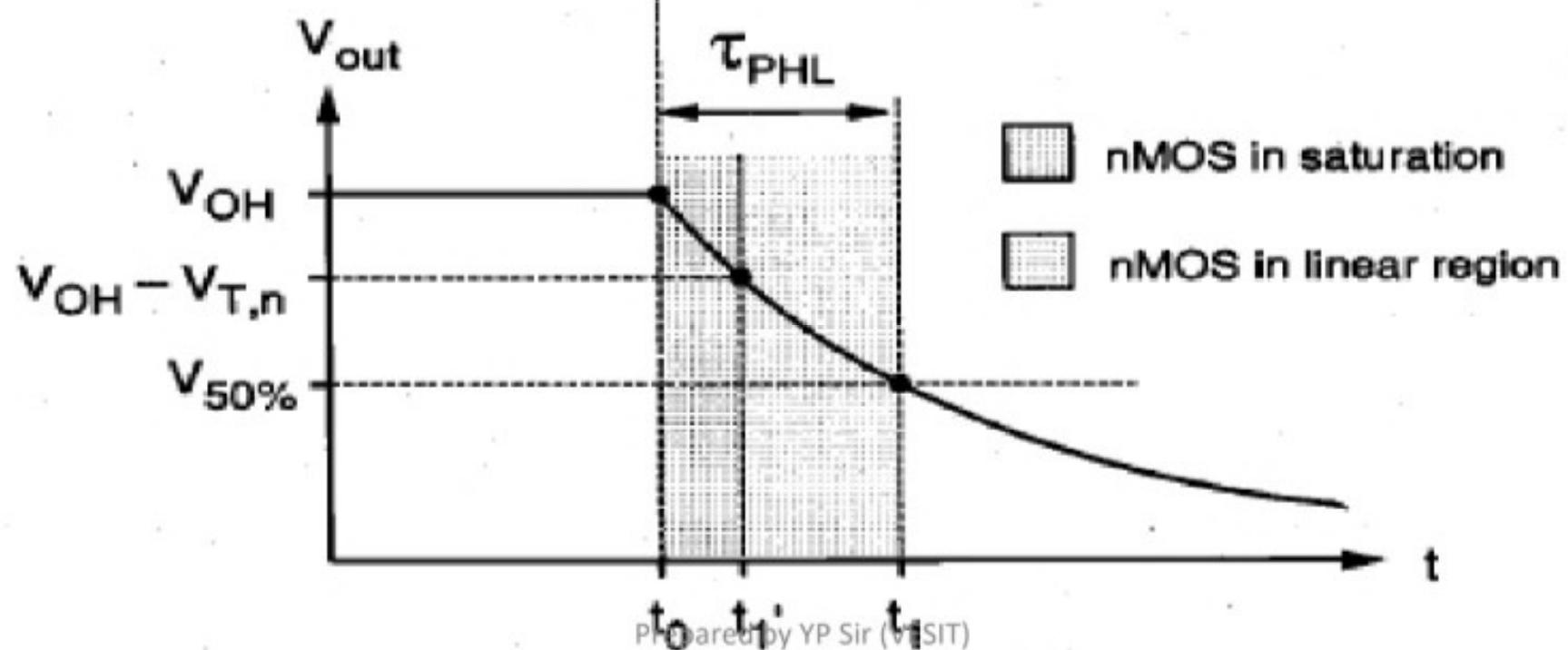
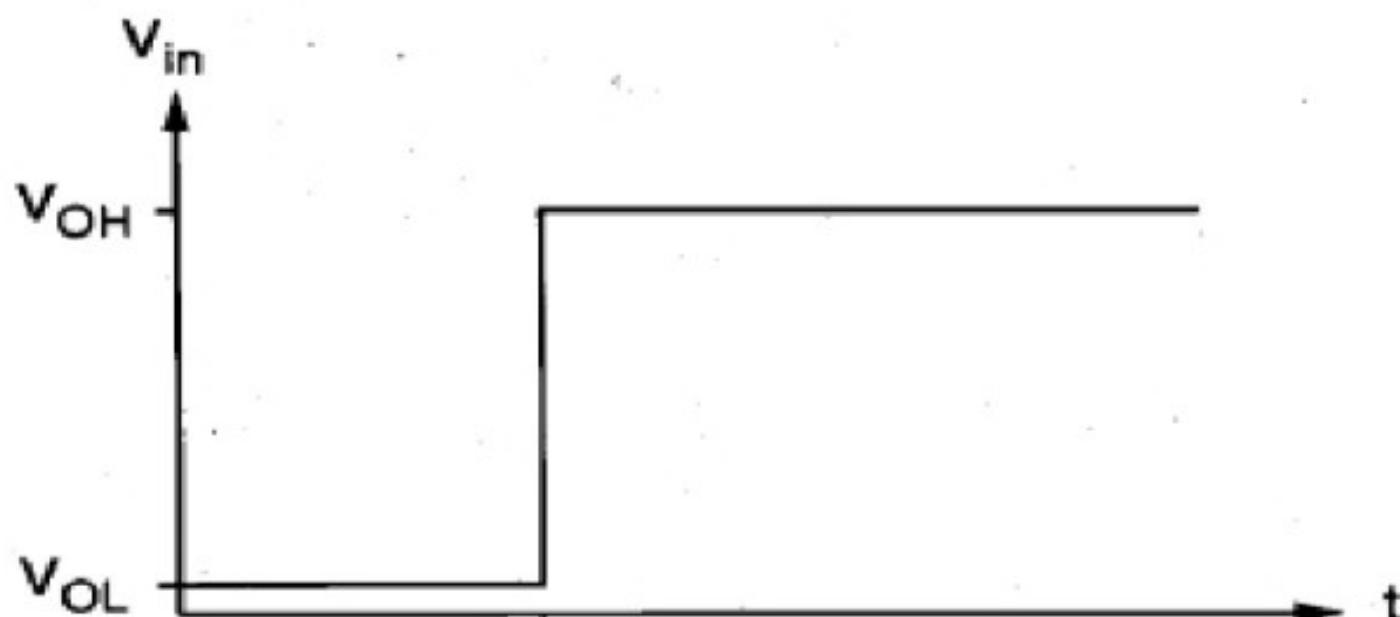
→ following fig. shows equivalent ckt of the CMOS inverter during High-to-low o/p transition.

Thus, eqn ① becomes as,

$$C_{load} \frac{dV_{out}}{dt} = -I_{D,n} \quad \rightarrow ②$$

→ Now, let us consider the ilp & olp voltage waveform during high-to-low x'ition.

⇒ As shown in wlf, when nmos x'tor starts conducting, it initially operates in saturation region, when the o/p voltage falls below  $(V_{DD} - V_{T,n})$  the nmos x'tor starts to conduct in the linear region.



**Case-I** NMOS is operating in saturation region.

$$\therefore i_{D,n} = \frac{K_n}{2} (V_{in} - V_{T,n})^2$$
$$= \frac{K_n}{2} (V_{OH} - V_{T,n})^2 \text{ for } V_{out} > V_{OH} - V_{T,n}$$

from eqn ②,  $dt = - \frac{C_{load}}{i_{D,n}} dV_{out}$

& its solution in the time interval between  $t_0$  &  $t_1$  can be found as,

$$\int_{t_0}^{t_1} dt = - C_{load} \int_{V_{out}=V_{OH}}^{V_{OH}-V_{T,n}} \left( \frac{1}{i_{D,n}} \right) dV_{out}$$

Put value of  $i_{D,n}$  in above eqn

$$= - C_{load} \int_{V_{out}=V_{OH}}^{V_{OH}-V_{T,n}} \left( \frac{1}{\frac{K_n}{2} (V_{OH} - V_{T,n})^2} \right) dV_{out}$$

$$\int_{t=0}^{t_1} dt = \frac{-2C_{load}}{K_n(V_{OH}-V_{T,n})^2} \int_{V_{OH}}^{V_{OH}-V_{T,n}} dV_{out}$$

$$[t]_{t_0}^{t_1} = \frac{-2C_{load}}{K_n(V_{OH}-V_{T,n})^2} [V]_{V_{OH}}^{V_{OH}-V_{T,n}}$$

$$\therefore t_1 - t_0 = \frac{-2C_{load}}{K_n(V_{OH}-V_{T,n})^2} [(V_{OH}-V_{T,n}) - (V_{OH})]$$

$$\therefore t_1 - t_0 = \frac{2C_{load}V_{T,n}}{K_n(V_{OH}-V_{T,n})^2} \longrightarrow ③$$

Case-2 Consider nMOS operating in Linear Region

$$\therefore i_{D,n} = \frac{Kn}{2} [2(V_{in} - V_{T,n})V_{out} - V_{out}^2]$$

$$= \frac{Kn}{2} [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2] \text{ for } V_{out} \leq V_{OH} - V_{T,n}$$

Thus, obtain the soln of eqn ② for interval  $t'$  to  $t_1$

i.e.  $\int_{t=t_1}^{t_1} dt = -C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{SOI}} \left( \frac{1}{i_{D,n}} \right) dV_{out}$

put value of  $i_{D,n}$  in above eqn

$$= -2C_{load} \int_{V_{OH}-V_{T,n}}^{V_{SOI}} \left( \frac{1}{Kn[2(V_{OH} - V_{T,n})V_{out} - V_{out}^2]} \right) dV_{out}$$

Solving the above integral yields,

$$[t]_{TH}^{t_1} = \frac{-2C_{load}}{k_n} \cdot \frac{1}{2(V_{OH} - V_{T,n})} \ln \left( \frac{V_{out}}{2(V_{OH} - V_{T,n}) - V_{out}} \right) \Bigg|_{V_{OH} - V_{T,n}}$$

$$t_1 - t_1' = \frac{C_{load}}{k_n (V_{OH} - V_{T,n})} \ln \left( \frac{2(V_{OH} - V_{T,n}) - V_{SOI.}}{V_{SOI.}} \right)$$

but  $V_{SOI.} = \frac{1}{2}(V_{OL} + V_{OH})$  put in above eqn

$$t_1 - t_1' = \frac{C_{load}}{k_n (V_{OH} - V_{T,n})} \ln \left[ \frac{2(V_{OH} - V_{T,n}) - \frac{1}{2}(V_{OL} + V_{OH})}{\frac{1}{2}(V_{OL} + V_{OH})} \right]$$

The above eqn can be further simplified as,

$$t_1 - t_1' = \frac{C_{load}}{k_n (V_{OH} - V_{T,n})} \ln \left[ \frac{\frac{4(V_{OH} - V_{T,n})}{V_{OH} + V_{OL}} - 1}{1} \right] \rightarrow ④$$

finally, propagation delay-time ( $\tau_{PHL}$ ) can be found by combining eqn ③ & ④

$$\therefore \tau_{PHL} = \frac{C_{load}}{k_n (V_{OH} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{OH} - V_{T,n}} + \ln \left( \frac{\frac{4(V_{OH} - V_{T,n})}{V_{OH} + V_{OL}} - 1}{1} \right) \right]$$

$$\therefore \tau_{PHL} = \frac{C_{load}}{K_n(V_{OH} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{OH} - V_{T,n}} + \ln \left( \frac{4(V_{OH} - V_{T,n})}{V_{OH} + V_{OL}} - 1 \right) \right]$$

for  $V_{OH} = VDD$  &  $V_{OL} = 0$ , the above eqn becomes as,

$$\boxed{\tau_{PHL} = \frac{C_{load}}{K_n(VDD - V_{T,n})} \left[ \frac{2V_{T,n}}{VDD - V_{T,n}} + \ln \left( \frac{4(VDD - V_{T,n})}{VDD} - 1 \right) \right]}$$

Similarly, The propagation delay time  $\tau_{PLH}$  can be found as,

$$\tau_{PLH} = \frac{C_{load}}{K_p(V_{DD} - |V_{T,P}|)} \left[ \frac{2|V_{T,P}|}{V_{DD} - |V_{T,P}|} + \ln \left( \frac{4(V_{DD} - |V_{T,P}|)}{V_{DD}} - 1 \right) \right]$$

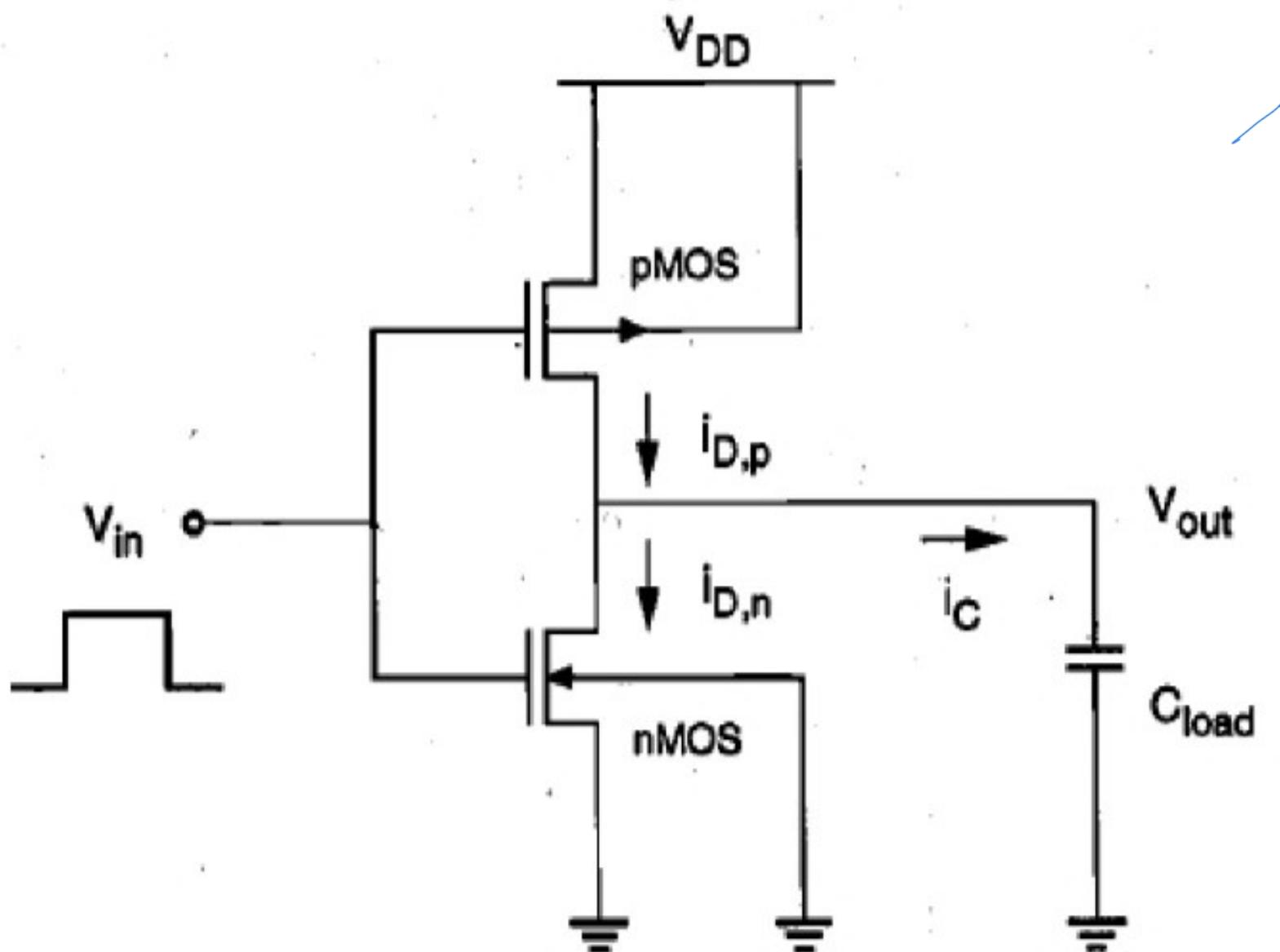
$\Rightarrow$  Comparing the delay expression of both,  
The sufficient cond'n for balanced propagation delay  
ie. for  $\tau_{PHL} = \tau_{PLH}$  in CMOS inverter are,

$$|V_{T,n}| = |V_{T,p}| \quad \& \quad K_n = K_p \quad \text{or} \quad \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

NM  
IT  
PD  
A&D

## Inverter design with Delay constraints

- The design procedure usually involves the design constraints such as Noise margin, Inversion threshold, Power dissipation, Area & Delay constraints.
- Thus, design process should involve the balancing of these requirements for optimum performance.
- In order to satisfy certain timing requirements we need to determine the channel dimensions ( $w_n, w_p$ ) of nMOS and pMOS transistor.



→ As shown in fig., the load capacitance of the inverter is also a function of x<sub>tar</sub> size

C<sub>load</sub> consists of intrinsic components (parasitic drain capacitance which depends on x<sub>tar</sub> dimension) & extrinsic components (ie. interconnect / wiring capacitance etc - which are usually independent of x<sub>tar</sub> dimension of inverter)

→ Let us consider that, C<sub>load</sub> is the function of extrinsic components only, thus,  $\left(\frac{W_n}{L_n}\right)$  of nmos x<sub>tar</sub> &  $\left(\frac{W_p}{L_p}\right)$  of pmos x<sub>tar</sub> is as given below,

$$\left(\frac{W_n}{L_n}\right) = \frac{C_{load}}{\tau_{PLH} M_n C_{ox} (V_{DD} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left( \frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

&

$$\left(\frac{W_p}{L_p}\right) = \frac{C_{load}}{\tau_{PLH} M_p C_{ox} (V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

- In most cases, the xbar size found from delay requirements must also meet other design criteria such as N.M. & Inversion Threshold.
- In all cases, the xbar dimension should be chosen so that all delay times remain below the required target value.

(e.g) Design a CMOS Inverter by determining the width  $w_n$  &  $w_p$  of the nmos & pmos xbar to meet the following performance specifications

$V_{TH} = 1.5V$  for  $V_{DD} = 3V$ ,  $T_{PHL} \leq 0.2ns$ ;  $T_{PLH} \leq 0.15ns$   
 A falling delay of  $0.35\text{ nsec}$  for an op transition from  $2V$  to  $0.5V$  by assuming  $C_{load} = 300\text{ fF}$ . for an ide.

The device parameters are,

$$m_{nCOX} = 120 \mu\text{A/V}^2 ; m_{pCOX} = 60 \mu\text{A/V}^2 ;$$

$$L = 0.6 \mu\text{m} \text{ for both Nmos & Pmos} ;$$

$$V_{TO,N} = 0.8V ; V_{TO,P} = -1.0V ; W_{min} = 1.2 \mu\text{m}$$

Sol<sup>n</sup>

Calculate the ( $\frac{W}{L}$ ) ratios of the nMOS & pMOS xtors

As we have,

$$\left( \frac{W_n}{L_n} \right) = \frac{C_{load}}{T_p H L M_n C_{ox} (V_{DD} - V_{T,n})} \left[ \frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left( \frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right]$$

$$= \frac{300 \times 10^{-15}}{0.2 \times 10^9 \times 120 \times 10^{-6} \times (3 - 0.8)} \left[ \frac{2 \times 0.8}{3 - 0.8} + \ln \left( \frac{4(3 - 0.8)}{3} - 1 \right) \right]$$

$$\boxed{\left( \frac{W_n}{L_n} \right) = 7.9} \quad \longrightarrow \quad ①$$

also,

$$\left( \frac{W_p}{L_p} \right) = \frac{C_{load}}{T_p L H M_p C_{ox} (V_{DD} - |V_{T,p}|)} \left[ \frac{2|V_{T,p}|}{V_{DD} - |V_{T,p}|} + \ln \left( \frac{4(V_{DD} - |V_{T,p}|)}{V_{DD}} - 1 \right) \right]$$

$$= \frac{300 \times 10^{-15}}{0.15 \times 10^9 \times 60 \times 10^{-6} (3 - 1)} \left[ \frac{2 \times 1}{(3 - 1)} + \ln \left( \frac{4(3 - 1)}{3} - 1 \right) \right]$$

$$\boxed{\left( \frac{W_p}{L_p} \right) = 25.2} \quad \longrightarrow \quad ②$$

Thank  
you!

