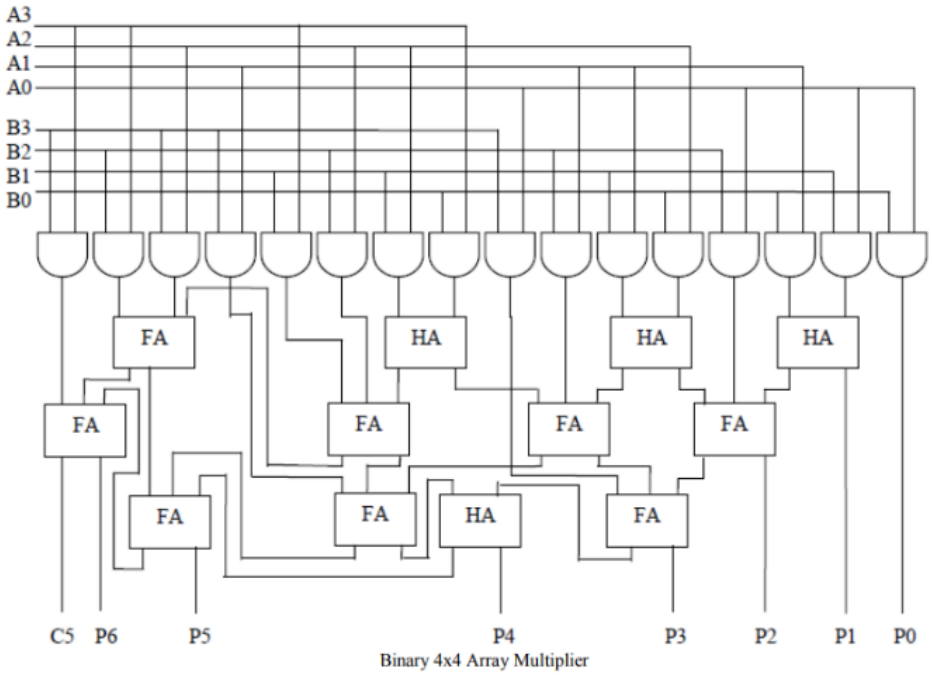
VLSI PROJECT - REPORT

Binary 4x4 Multiplier



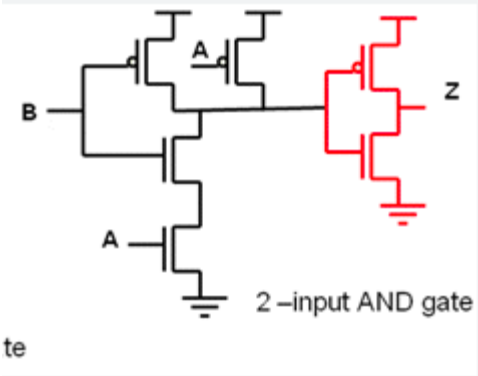
Binary 4x4 Array Multiplier

SUB-CIRCUITS USED TO MAKE MULTIPLIER:

- AND GATE
- HALF ADDER
- FULL ADDER

i. AND GATE:

CMOS DESIGN:



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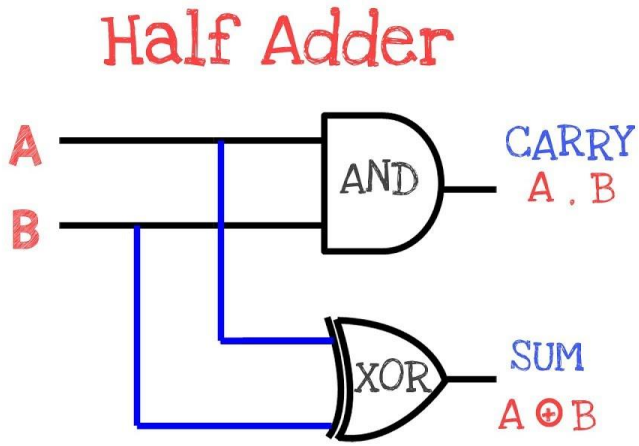
ii. HALF ADDER:

GATE LEVEL DESIGN:

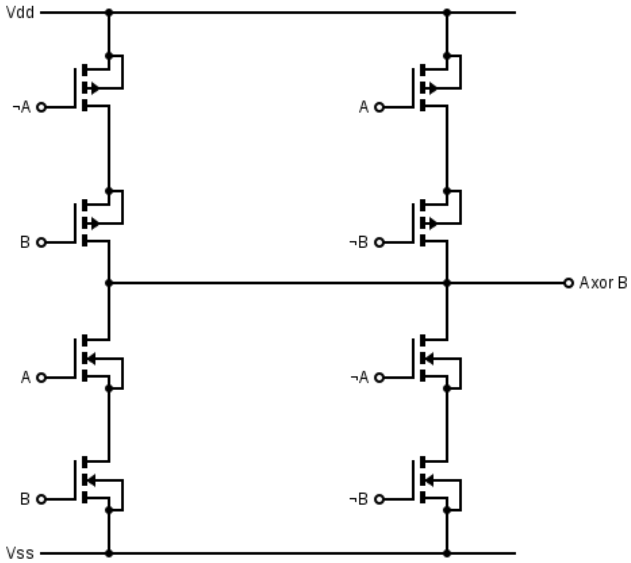


SUB CIRCUITS USED:

- XOR
- AND

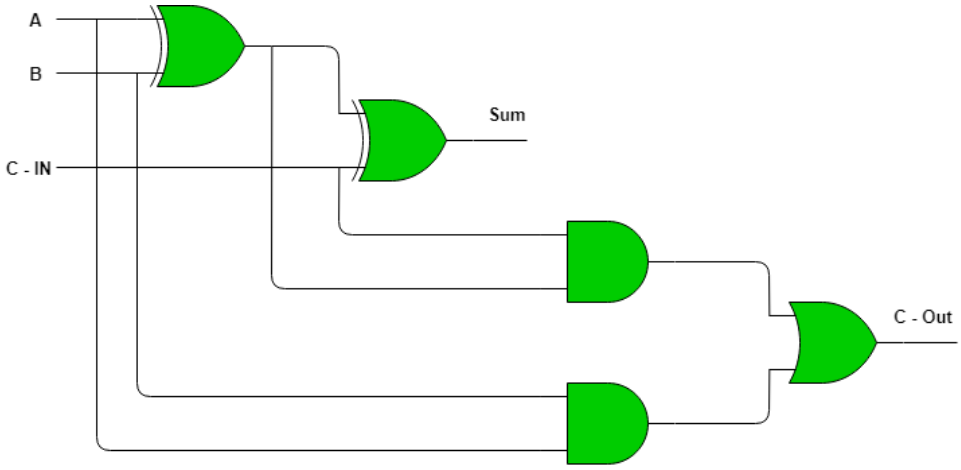
XOR:

CMOS DESIGN:



iii. FULL ADDER:

GATE LEVEL DESIGN:

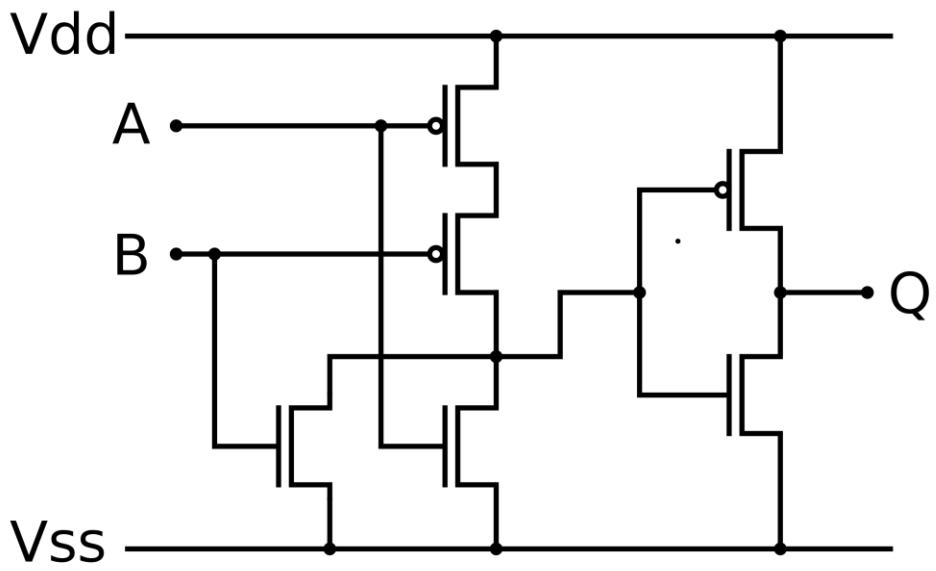


SUB CIRCUITS USED:

- HALF ADDER
- XOR

- AND
- OR

CMOS DESIGN OF OR GATE:



PRE AND POST LAYOUT RESULTS:

Pre layout results implies results of propagation delays and leakage power by the ngspice design of circuit.

The ngspice code to calculate power is stored in a file called “circuit.cir” and the code to calculate propagation delays is “circuitPROPDELAY.cir”, power for different inputs is stored in “power.txt” and the propagation delays of 50 paths are stored in “delay.txt” in a decreasing sorted order, all in the folder “ngspice”

MAGIC IS USED FOR THE LAYOUT OF THE MULTIPLIER.

MAGIC FILE NAME: “final.mag”

Post layout results implies results of propagation delays and leakage power by the spice file extracted from magic design of circuit.

The spice code to calculate power is stored in a file called “final.spice” and the code to calculate propagation delays is “finalpropdelay.spice”, power for different inputs is stored in “power.txt” and the propagation delays of 50 paths are stored in “delay.txt” in a decreasing sorted order, all in the folder “Magic”

RESULTS:

Leakage Current:

We see that the power in post layout design is slightly lesser I.e of the order 5*10^-10 or 6*10^-10 than the leakage power in the pre layout design which is of the order 7*10^-10 or 8*10^-10

Propagation Delays:

The propagation delays in the pre layout design are lesser than the ones in the post layout design by 100 times.

The pre layout design has delays of the order 10^-10 and 10^-9 and post layout design has delays of the order 10^-7 and 10^-8.

Maximum Propagation Delays:

Pre-Layout: 6.89035E-09

Post-Layout: 5.88815E-07

VERILOG:

The subcircuits used in this are the half_adder.v and full_adder.v to make the circuit multiplier.v with the test bench multiplier_tb.v and the gtk wave file is multiplier_tb.vcd

Output truth table is stored in the file “output.txt”

We see that the output truth table matches the expected result for all combinations of inputs.

COMMANDS TO RUN THE FILES:

☺ To Run ngspice for power calculation(Pre-Layout)

python3 main.py

☺ To run ngspice for propagation delay calculation:

-*ngspice circuitPROPDELAY.cir*

☺ To run Magic file:

- *magic -T SCN6M_DEEP.09.tech27 final.mag*

☺ To run the spice file extracted from Magic for power calculation

-python3 main.py

☺ To run spice file extracted from magic for propagation delay calculation

-ngspice finalpropdelay.spice

☺ To run the verilog file to verify the results

-*python3 main.py*