DIGITAL VLSI DESIGN

PROJECT-1
LEAKAGE CURRENT ESTIMATION

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- ANUSHKA AGRAWAL (2021102023) : Analysying and code for leakage current estimation and circuit netlist creation
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Introduction

Leakage current, a common occurrence in MOSFETs, creates challenges in digital circuit design. Even when MOSFETs are supposed to be off, tiny currents still flow, wasting power and potentially causing reliability issues. Estimating these currents is essential for making circuits more efficient and long-lasting. This report focuses on presenting a method to estimate leakage currents in larger circuits. By understanding and predicting these currents, designers can make better choices, improving the efficiency and reliability of electronic systems.

LEAKAGE CURRENT ESTIMATION IN SINGLE MOSFET (Stage-1)

PROCEDURE

In this section, we focus on estimating leakage current in a single MOSFET, both NMOS and PMOS. The calculations are conducted across various width-to-length (W/L) ratios and supply voltage settings. The derived leakage currents encompass the flow through gate, drain, source, and body terminals.

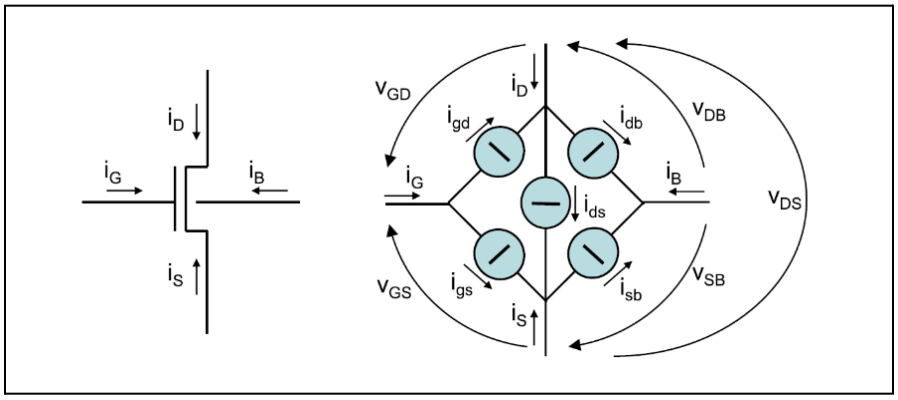


Fig 1: leakage currents in a single mosfet across different terminals

Analyzing leakage current individually through each terminal aids in extrapolating to larger circuits, particularly those employing 2-input gates such as NAND and NOR gates.

Throughout the calculations, it becomes apparent that body leakage current consistently remains significantly smaller than the other three leakage currents. Additionally, as the supply voltage increases, so does the leakage current. Similarly, increasing the W/L ratio of the MOSFET causes an increase in leakage current.

RESULTS

1. Changing the width so that we change the W/L ratio, and estimate the voltages at each node. We have shown results for the following W/L ratios: 1, 2, 4, 6, 8. Along with the change in the W/L ratio, we have shown the results for different values of Vdd values ranging from 0.5 to 1.1 with a step size of 0.5.

   Results (shown only a few, NMOS OFF):

   a. W/L = 1, Vdd ranges from 0.05 to 0.25

```
Width, V_alim, V(drain), V(gate), V(source), V(body), I(Vd), I(Vg), I(Vs), I(Vb)
4.5E-08, 0.05, 0, 0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
4.5E-08, 0.1, 0, 0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
4.5E-08, 0.15, 0, 0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
4.5E-08, 0.2, 0, 0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
4.5E-08, 0.25, 0, 0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
```

   b. W/L = 2, Vdd ranges from 0.05 to 0.25

Width	V_alim	V(drain)	V(gate)	V(source)	V(body)	I(Vd)	I(Vg)	I(Vs)	I(Vb)
9E-08	0.05	0	0	0	0	-1.48632E-20	2.00953E-19	-1.48632E-20	-1.71227E-19
9E-08	0.1	0	0	0	0	-1.48632E-20	2.00953E-19	-1.48632E-20	-1.71227E-19
9E-08	0.15	0	0	0	0	-1.48632E-20	2.00953E-19	-1.48632E-20	-1.71227E-19
9E-08	0.2	0	0	0	0	-1.48632E-20	2.00953E-19	-1.48632E-20	-1.71227E-19
9E-08	0.25	0	0	0	0	-1.48632E-20	2.00953E-19	-1.48632E-20	-1.71227E-19

c. W/L = 6, Vdd ranges from 0.05 to 0.25

Width	V_alim	V(drain)	V(gate)	V(source)	V(body)	I(Vd)	I(Vg)	I(Vs)	I(Vb)
2.7E-07	0.05	0	0	0	0	-4.83055E-20	6.53098E-19	-4.83055E-20	-5.56487E-19
2.7E-07	0.1	0	0	0	0	-4.83055E-20	6.53098E-19	-4.83055E-20	-5.56487E-19
2.7E-07	0.15	0	0	0	0	-4.83055E-20	6.53098E-19	-4.83055E-20	-5.56487E-19
2.7E-07	0.2	0	0	0	0	-4.83055E-20	6.53098E-19	-4.83055E-20	-5.56487E-19
2.7E-07	0.25	0	0	0	0	-4.83055E-20	6.53098E-19	-4.83055E-20	-5.56487E-19

Note: The results were presented in the 1st eval of this project, for all the combinations of NMOS_on, NMOS_off, PMOS_on, PMOS_off.

Cloud link with this results for all the above mentioned states: https://iiitaphyd-my.sharepoint.com/:f:/g/personal/arya_marda_students_iiit_ac_in/EsGj8rLAHzBCiZYZ_yDHsqIBStm68TWvNZYpXnMQcPMbuQ?e=eWgmB9

2. The next results that we present are where we have varied the Source voltage and drain Voltage from 0 to 1.1 with a step size of 0.5, and the gate voltage is either 0 or 1.1v. Remember the W/L ratio is constant in this case.

The altering code snippet:

```
while vtestg le maxi
  alter Vg = vtestg
  let Vtests=0
  while Vtests le maxi
    alter Vs = Vtests
    let Vtestd=0
    while Vtestd le maxi
      alter Vd = Vtestd
      dc TEMP 85 85 10
      echo "$&V(drain), $&V(gate), $&V(source), $&I(Vd), $&I(Vg), $&I(Vs), $&I(Vb)" >> nmos1.csv
      let Vtestd = Vtestd + 0.05
    end
    let Vtests = Vtests + 0.05
  end
  let vtestg = vtestg + 1.1
end
```

Results (shown only a few, for nmos):

```
V(drain), V(gate), V(source), I(Vd), I(Vg), I(Vs), I(Vb)
0, 0, 0, -6.50266E-21, 8.7917E-20, -6.50266E-21, -7.49117E-20
0.05, 0, 0, -2.69535E-09, 5.10764E-12, 2.69023E-09, 8.02146E-15
0.1, 0, 0, -3.47378E-09, 1.39085E-11, 3.45986E-09, 9.60963E-15
0.15, 0, 0, -3.99514E-09, 2.7367E-11, 3.96776E-09, 9.92509E-15
0.2, 0, 0, -4.52327E-09, 4.66315E-11, 4.47663E-09, 9.98899E-15
0.25, 0, 0, -5.09847E-09, 7.30653E-11, 5.0254E-09, 1.00034E-14
0.3, 0, 0, -5.73642E-09, 1.08281E-10, 5.62813E-09, 1.00085E-14
0.35, 0, 0, -6.44847E-09, 1.54182E-10, 6.29427E-09, 1.0012E-14
0.4, 0, 0, -7.24539E-09, 2.13007E-10, 7.03237E-09, 1.00158E-14
```

We use these results for the calculation of leakage currents of nand, nor and not gates for all input combinations (00,01,10,11 for nand, nor and 0,1 for not) in stage-2. Nmos results are stored in nmos.csv and pmos results in pmos.csv.

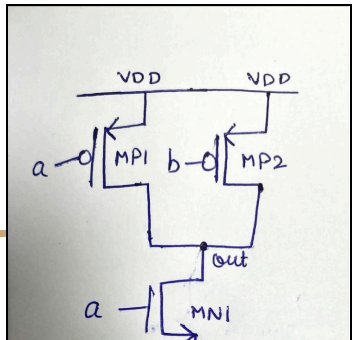
Cloud link with this results for both NMOS and PMOS:
https://iiitaphyd-my.sharepoint.com/:f:/g/personal/arya_marda_students_iiit_ac_in/Ej_vjphJbihKuaTyfsnb1pkBiheVPvy2zJdtV9IcRZEx8Q?e=A49Evh

LEAKAGE CURRENT ESTIMATION FOR TWO INPUT GATES (NAND,NOR) and Inverter: (Stage-2)

PROCEDURE

In this phase, we transition to analyzing 2-input gates, specifically NAND and NOR gates, and Inverter utilizing the insights gained from the previous stage.

For the NAND gate, we configure two NMOS transistors in series for the pull-down section and two PMOS transistors in parallel for the pull-up section. By considering all possible input combinations, we



compute the voltages at each terminal for each transistor. Now, from stage-1, we have the current values across all terminals of both pmos and nmos for different values of gate, source and drain voltages. So now, for each mosfet of the nand, we obtain the drain, gate and source voltages, then for this obtained combination of drain, gate,source voltages, we map them and we obtain the current across drain, gate source and body for each of these mosfets from the nmos.csv and pmos.csv file we generated in stage-1.

Note: For any mosfet, I(drain) + I(gate) = I(source) + I(body). This implies that :

I(drain) - I(source) = I(body) - I(gate) and

I(source) - I(drain) = I(gate) - I(body)

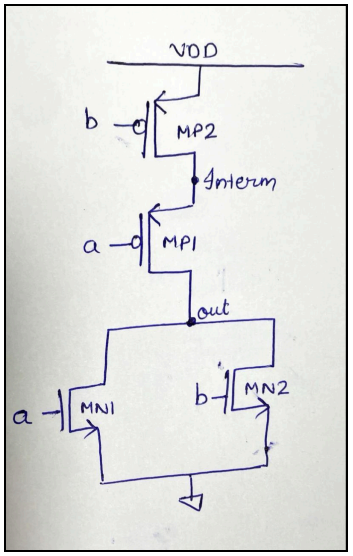
These equations have been used in many places where we want to calculate leakage of the supply current across a mosfet by doing I(source) - I(drain) but instead we do I(gate) - I(body) for ease of calculation.

Once we get the current flowing through each terminal, to determine the leakage current through the gate, we individually analyze each input combination.

1. Input Combination 1: a = 0, b = 0
   Both the PMOS are in ON state and NMOS are in off state. Therefore, the total leakage current for this input combination:
   I_leakage = 2*(I_drain(MP1) - I_source(MP1)) + 2*(I_body(MP1)) +I_drain(MN1)
   = 2*(I_gate(MP1) - I_body(MP1)) + 2*(I_body(MP1)) + I_drain(MN1)
2. Input Combination 2: a= 0, b = 1
   One of PMOS is off and NMOS_1 is off. The total leakage for this input combination:
   I_leakage = (I_drain(MP1) - I_source(MP1)) + I_drain(MN1) + I_gate(MN2)
   = (I_gate(MP1) - I_body(MP1)) + I_drain(MN1) + I_gate(MN2)
3. Input Combination 3: a= 1, b= 0
   One of PMOS is again off and NMOS_2 is off. Therefore, the total leakage for this input combination:
   I_leakage = (I_source(MN1) - I_drain(MN1)) + (I_drain(MP2) - I_source(MP2)) +
   I_drain(MN2) + I_body(MP2) + I_gate(MN1)
   = (I_body(MN1) - I_gate(MN1)) + (I_gate(MP2) - I_body(MP2)) +
   I_drain(MN2) + I_body(MP2) + I_gate(MN1)

4. Input Combination 4: a = 1, b = 1
   Both PMOS are off, and NMOS are in ON state. Therefore, the total leakage current for this input combination:
   I_leakage = 2*(I_source(MP1)) + 2*(I_body(MP1)) + 2*(I_gate(MP1)) + 2*(I_gate(MN1))

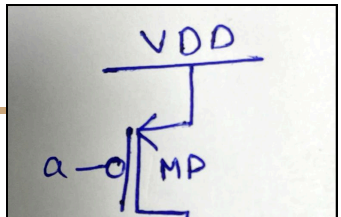
Similarly, for the NOR gate, we reverse the configuration, employing two PMOS transistors in series for the pull-up section and two NMOS transistors in parallel for the pull-down section. By assessing all input combinations, we determine the current passing through all the terminals in similar fashion as done for NAND gates.



Once we get the current flowing through each terminal, to determine the leakage current through the gate, we individually analyze each input combination.

1. Input Combination 1: a = 0, b = 0
   Both the PMOS are in ON state and NMOS are in off state.
   Therefore, the total leakage current for this input combination:
   I_leakage = 2*(I_drain(MN1)) + I_body(MP1) + I_body(MP2) + (I_drain(MP2) - I_source(MP2)) + (I_drain(MP1) - I_source(MP1))
   = 2*(I_drain(MN1)) + I_body(MP1) + I_body(MP2) + (I_gate(MP2) - I_body(MP2)) + (I_gate(MP1) - I_body(MP1))
2. Input Combination 2: a= 0, b = 1
   One of NMOS is off and PMOS_2 is off. The total leakage for this input combination:
   I_leakage = I_gate(MP2) + I_source(MP2) + I_gate(MN2) + I_body(MP1)
3. Input Combination 3: a= 1, b= 0
   One of NMOS is again off and PMOS_1 is off. Therefore, the total leakage for this input combination:
   I_leakage = (I_drain(MP2) - I_source(MP2)) + I_gate(MN1) + I_body(MP2) + I_gate(MP1) + I_source(MP1)
4. Input Combination 4: a = 1, b = 1
   Both PMOS are off, and NMOS are in ON state. Therefore, the total leakage current for this input combination:
   I_leakage = I_source(MP2) + I_gate(MP1) + I_gate(MP2) + 2*(I_gate(MN1))

Similarly, for NOT gate, we get the leakage current for both input values.



1. Input a = 0

   Leakage current = (I_drain(MP) - I_source(MP)) + I_drain(MN) + I_body(MP)

   = (I_gate(MP) - I_body(MP)) + I_drain(MN) + I_body(MP)

2. Input a = 1

   Leakage current = I_gate(MP) + I_gate(MN) + I_source(MP)

To validate these leakage current estimations, we construct the complete circuit for the NAND, NOR and NOT gate and measure and add the current flowing through the supply node and input nodes which are ON. This accumulated current is the actual leakage current flowing through any of the gate.

ACTUAL LEAKAGE CURRENT CALCULATION FOR VERIFICATION:

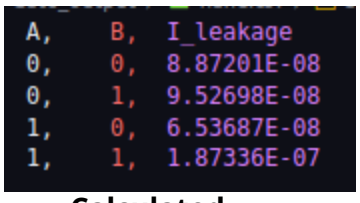
Input: A =0 B=0	Leakage Current = I(Vdd)
Input: A =0 B=1	Leakage Current = I(Vdd) + I(B)
Input: A =1 B=0	Leakage Current = I(Vdd) + I(A)
Input: A =1 B=1	Leakage Current = I(Vdd) + I(A) + I(B)

By employing this methodology, we aim to ensure the accuracy of our leakage current estimations for 2-input gates and validate their applicability in larger circuit designs.

RESULTS:

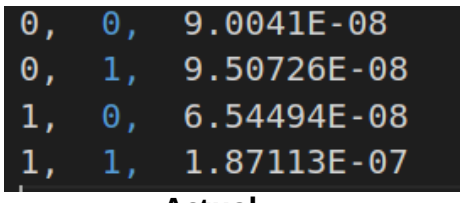
The leakage current calculated using the methodology described above for each gate and each input combination:

1. **NAND Gate:**



A,	B,	I_leakage
0,	0,	8.87201E-08
0,	1,	9.52698E-08
1,	0,	6.53687E-08
1,	1,	1.87336E-07

Calculated

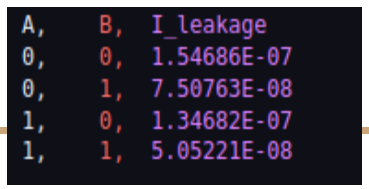


0,	0,	9.0041E-08
0,	1,	9.50726E-08
1,	0,	6.54494E-08
1,	1,	1.87113E-07

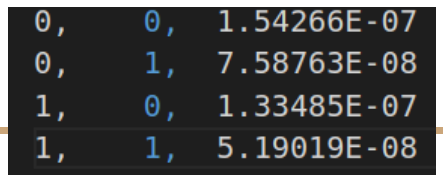
Actual

Avg Error : 0.478

2. **NOR Gate:**



A,	B,	I_leakage
0,	0,	1.54686E-07
0,	1,	7.50763E-08
1,	0,	1.34682E-07
1,	1,	5.05221E-08

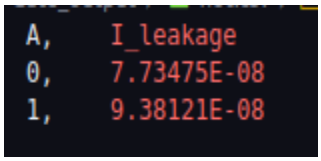


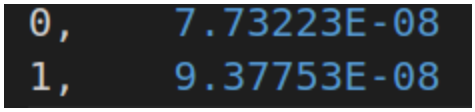
0,	0,	1.54266E-07
0,	1,	7.58763E-08
1,	0,	1.33485E-07
1,	1,	5.19019E-08

Avg Error: 2.4395

Calculated **Actual**

3. **NOT Gate:**





Avg Error: 0.0718

Calculated **Actual**

LEAKAGE CURRENT ESTIMATION ISCAS 74182 CIRCUITS

PROCEDURE

In the third stage, our focus shifts to estimating the leakage current through the ISCAS 74182 circuit, a complex construction comprising 9 input nodes and 5 output nodes. The circuit diagram provided serves as our blueprint for analysis.

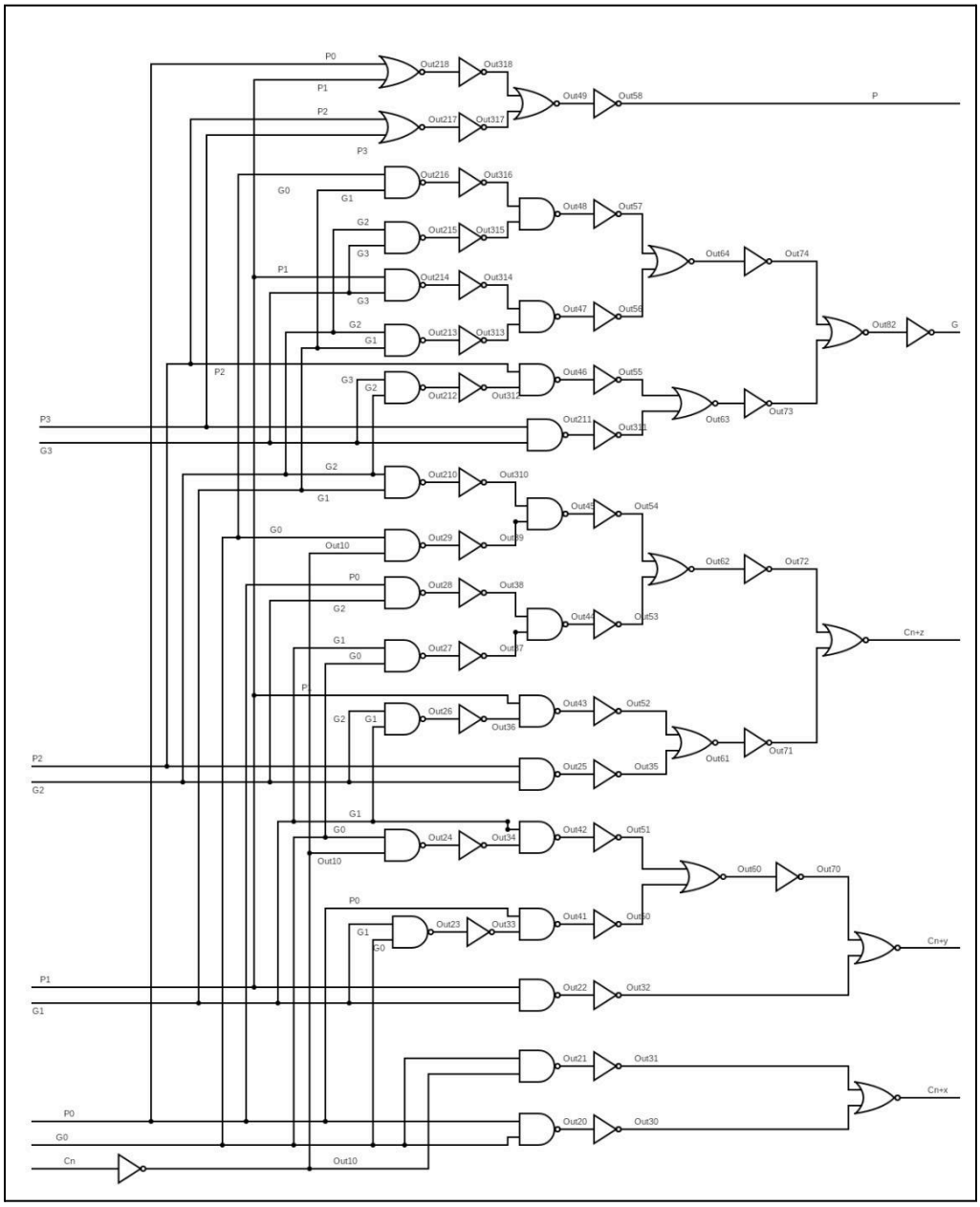


Fig 2: circuiti diagram for ISCAS 74182

1. ESTIMATING THE LEAKAGE CURRENT

To estimate the leakage current in the entire circuit, we employ a systematic approach by breaking down the circuit into its constituent gates: NAND, NOR, and NOT gates. Leveraging the methodology developed in the second stage, we calculate the leakage current flowing through each gate individually and then aggregate these values to obtain the final result.

Our methodology involves the following steps:

- **Gate-Level Analysis**: For a given input combination, we determine the input and output voltages for each gate in the circuit.
- **Leakage Current Calculation for Each Gate**: Using the input voltage of each gate, we utilize the matrices generated in the second stage to compute the leakage current specific to that gate. This process involves applying the established methodology for estimating leakage current in 2-input gates, adapted to the configuration of each gate type (NAND, NOR, or NOT).
- **Aggregation of Leakage Currents**: Once we have calculated the leakage current through each individual gate, we sum these values to obtain the total leakage current through the entire circuit.

By applying this methodology, we effectively assess the impact of leakage current at the gate level and aggregate these contributions to determine the overall leakage behavior of the circuit. This comprehensive approach ensures accurate estimation of leakage current and provides valuable insights for optimizing power efficiency and reliability in complex circuit designs.

2. CALCULATING THE ACTUAL LEAKAGE CURRENT

To verify the accuracy of our estimated leakage current through the entire circuit, we undertake a practical approach. We construct the complete circuit and for a given input combination we measure the leakage current flowing through the input nodes which are in ON state and the supply node for a given input combination. This gives us the actual leakage current for the whole circuit for a given input combination.We compare the measured actual leakage current with the leakage current values estimated through our methodology. Any discrepancies between the two sets of values are noted and analyzed.

Leakage Current = I(Vdd) + $\sum$ I(Input_K == 1)

RESULTS

For a given input combination, we compute the input and output voltages of each gate in the circuit and store it in outputs.csv file. One we get this, we calculate the total estimated

leakage current using the script cal_current_mos.py (it calculate the leakage current for each gate individually and sums them up). To verify the result, we calculate the actual leakage current, by summing up the current flowing through supply node, and input node which are ON.

For input combination P0 = 0, P1 = 0, P2 = 0, P3 = 0, G0 = 0, G1 = 0, G2 = 0, G3 = 0, Cnt = 0
The estimated leakage current we get is: `7.2711392000000009e-06`

The actual leakage current we get is: `7.89093e-06`

Error percentage = 7.95%

CALCULATING LEAKAGE CURRENT FOR ALL THE POSSIBLE COMBINATIONS.

We have a python script 'input.py' which callculates the leakage current from both methods, calculate the error and prints to a csv file: 'Errro.csv' for all the possible input combinations.

Results:

```
Combination, leakage_current_cir, leakage_current_mos, error
000000000,7.89093e-06, 7.2711392000000009e-06, 0.7854470892530928
000000001,8.21631e-06, 6.9747999000000065e-06, 1.511031229347473
000000010,7.76655e-06, 6.9162588000000008e-06, 1.094811982154227
000000011,9.07207e-06, 6.619237800000005e-06, 2.7037183355066654
000000100,8.0329e-06, 6.886079800000007e-06, 1.4276540228310988
000000101,7.70157e-06, 6.797359700000006e-06, 1.1740597047095518
000000110,7.90852e-06, 6.5311994000000065e-06, 1.74156555208812
000000111,8.55733e-06, 6.441797600000005e-06, 2.472187469689723
```

```
Max Error: 8.397625191614658
Min Error: 0.7854470892530928
Average Error: 5.0093619012631265
```

Drive Link:
https://iiitaphyd-my.sharepoint.com/:x:/g/personal/arya_marda_students_iiit_ac_in/EeIahbgpT_REsMnJu1pWxBIBrnEg6WfLk1HYWmeRHEYzHA?e=W9wgqq