

EE314 Digital Circuits Laboratory

Experiment 1 Preliminary

1)

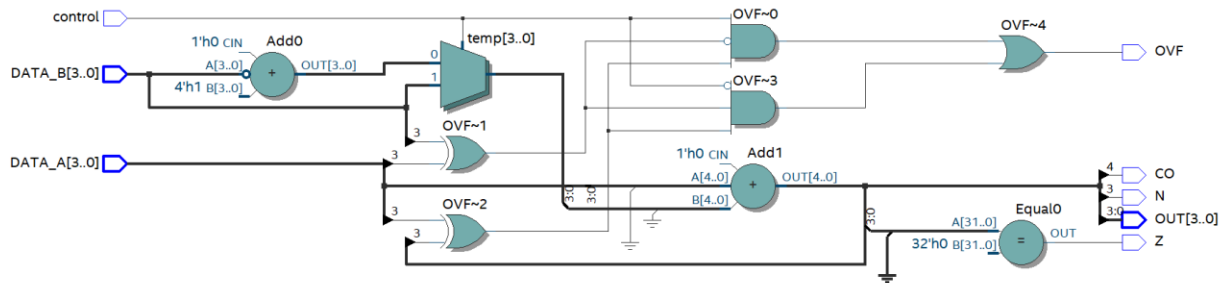


Figure 1: RTL Schematic of Arithmetic Unit

```

Windows PowerShell x Anaconda Prompt (anaconda) x + v - □ x
-5 0 ADD 0xb 0xb 0 0 0 0 1 1 0 0
0 -7 SUB 0x7 0x7 0 0 0 1 0 0 0 0
5 -4 SUB 0x9 0x9 0 0 0 1 1 0 0 0
4 -2 ADD 0x2 0x2 1 1 0 0 0 0 0 0
-1 4 ADD 0x3 0x3 1 1 0 0 0 0 0 0
-5 2 SUB 0x9 0x9 1 1 0 0 0 1 0 0
-6 6 ADD 0x0 0x0 1 1 0 0 0 0 0 1
-6 -2 SUB 0xc 0xc 0 0 0 0 1 1 0 0
3 -7 SUB 0xa 0xa 0 0 1 1 1 1 0 0
4 7 SUB 0xd 0xd 0 0 0 0 1 1 0 0

51000.00ns INFO cocotb.regression arithmetic_unit_test passed
51000.00ns INFO cocotb.regression
*****
** TEST STATUS SIM TIME (ns) REAL TIM
*****
** AU_test.arithmetic_unit_test PASS 51000.00
*****
** TESTS=1 PASS=1 FAIL=0 SKIP=0 51000.00
*****
make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP1/Experiment1Materialsv2-20250317/AUTest/Tests'
(base) D:\METU-EE\EE-Sem-6\EE314\EXP1\Experiment1Materialsv2-20250317\AUTest\Tests>

```

Figure 2: Test Results for Arithmetic Unit

2)

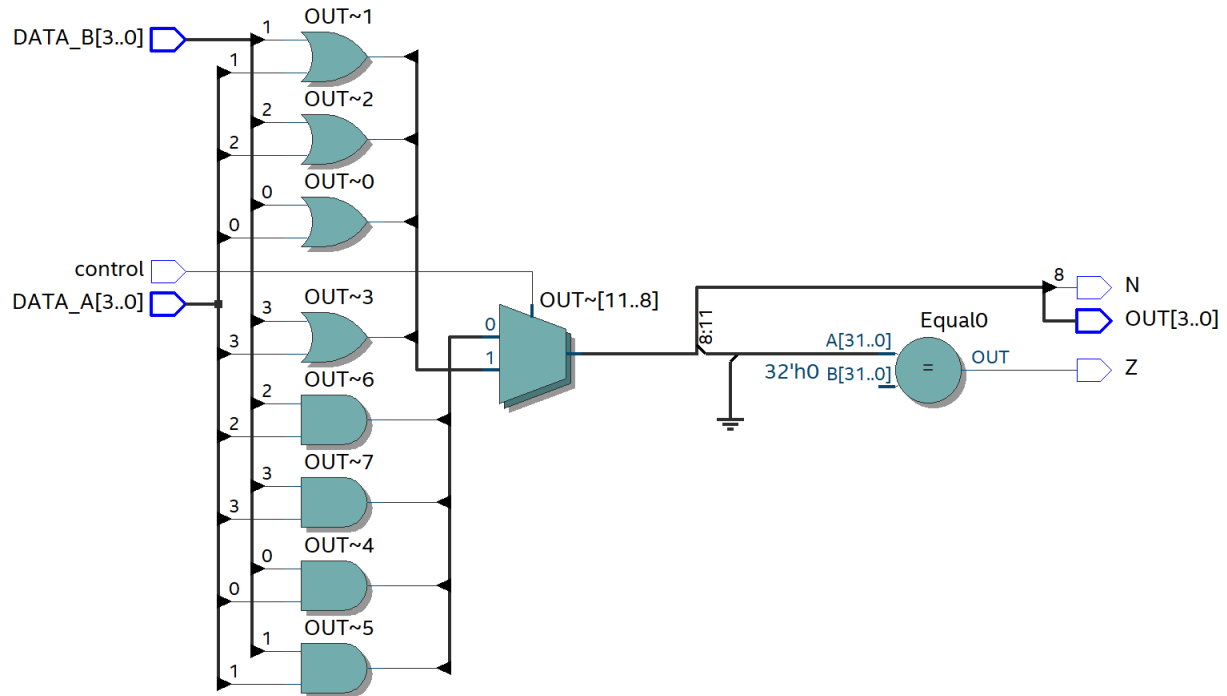


Figure 3: RTL Schematic for Logic Unit

```

Windows PowerShell  x  Anaconda Prompt (anaconda)  x  +  v
-7  -1  OR  0xf  0xf  1  1  0  0
-3  -3  OR  0xd  0xd  1  1  0  0
-8  -6  AND  0x0  0x0  0  0  1  1
0  -2  OR  0x2  0x2  0  0  0  0
3  -2  AND  0x2  0x2  0  0  0  0
0  -5  OR  0xb  0xb  1  1  0  0
-1  -6  AND  0x6  0x6  0  0  0  0
7  -3  OR  0x7  0x7  0  0  0  0
-6  -6  AND  0xa  0xa  1  1  0  0
-2  -8  OR  0xe  0xe  1  1  0  0

51000.00ns INFO cocotb.regression logic_unit_test passed
51000.00ns INFO cocotb.regression
*****
** TEST STATUS SIM TIME (ns) REAL TIM
*****
** LU_test.logic_unit_test PASS 51000.00
*****
** TESTS=1 PASS=1 FAIL=0 SKIP=0 51000.00
*****
make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP1/Experiment1Materialsv2-20250317/LUTest/Tests'
(base) D:\METU-EE\EE-Sem-6\EE314\EXP1\Experiment1Materialsv2-20250317\LUTest\Tests>

```

Figure 4: Test Results for Logic Unit

[illegible]

```

Windows PowerShell x Anaconda Prompt (anaconda. x + - □ x
4 0 OR 0x4 0x4 0 0 0 0 0 0 0 0 0 0
-5 -7 AND 0x9 0x9 0 0 0 0 0 0 0 0 0 0
7 -7 OR 0xf 0xf 0 0 0 0 0 0 0 0 0 0
2 -6 ADD 0xc 0xc 0 0 0 0 0 0 0 0 0 0
-4 -5 SUB 0x1 0x1 1 1 0 0 0 0 0 0 0 0
-4 4 OR 0xc 0xc 0 0 0 0 0 0 0 0 0 0
-5 1 OR 0xb 0xb 0 0 0 0 0 0 0 0 0 0
7 1 SUB 0x6 0x6 1 1 0 0 0 0 0 0 0 0
1 5 AND 0x1 0x1 0 0 0 0 0 0 0 0 0 0
5 4 ADD 0x9 0x9 0 0 1 1 0 0 1 1 0 0

51000.00ns INFO cocotb.regression alu_test passed
51000.00ns INFO cocotb.regression
*****

** TEST STATUS SIM TIME (ns) REAL TIM

*****

** ALU_test.alu_test PASS 51000.00

*****

** TESTS=1 PASS=1 FAIL=0 SKIP=0 51000.00

*****

make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP1/Experiment1Materialsv2-20250317/ALUTest/Tests'

(base) D:\METU-EE\EE-Sem-6\EE314\EXP1\Experiment1Materialsv2-20250317\ALUTest\Tests>

```

Figure 6: Test Results for ALU