

## EE314 Digital Circuits Laboratory

## Experiment 3 Preliminary

1)

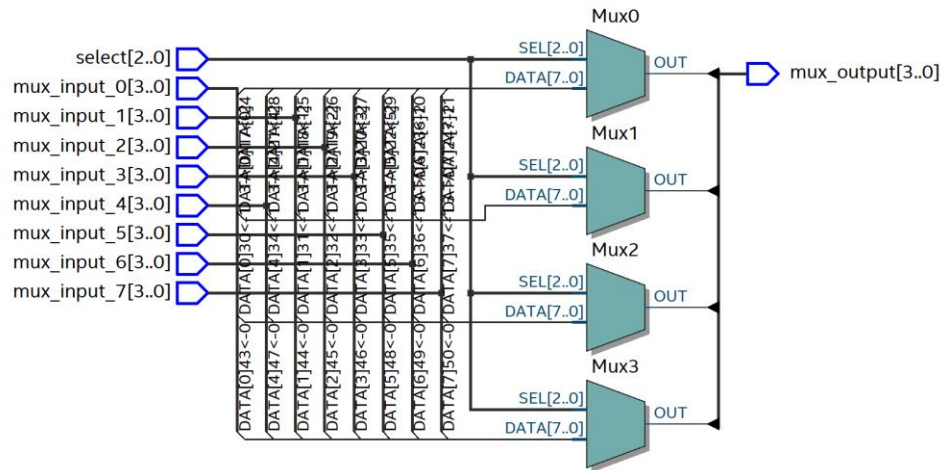


Figure 1: RTL Schematic for MUXx.v

2)

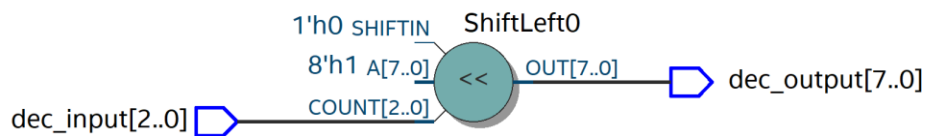


Figure 2: RTL Schematic for Decoder.v

3)

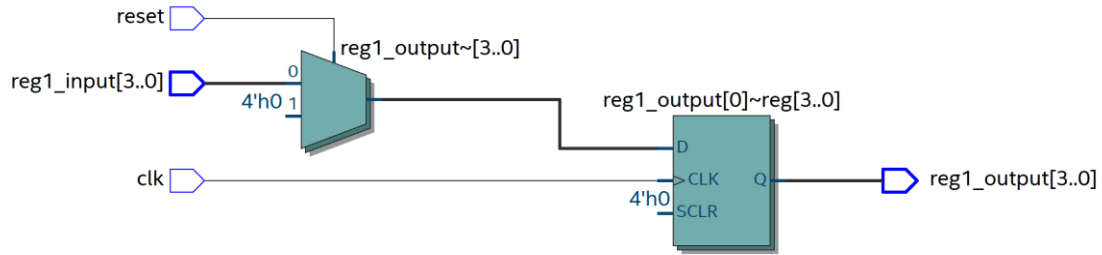


Figure 3: RTL Schematic for Reg1.v

4)

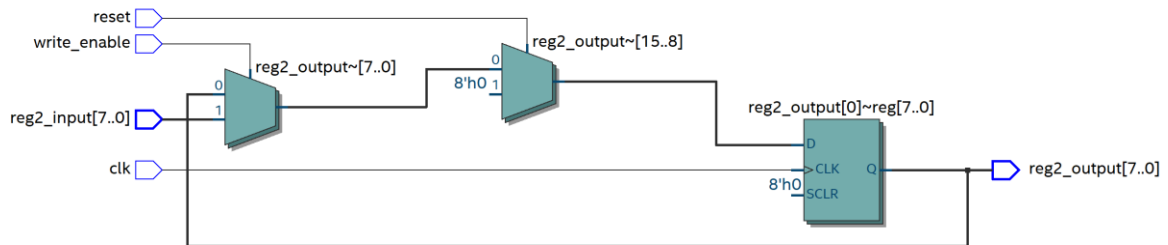


Figure 4: RTL Schematic for Reg2.v

5)

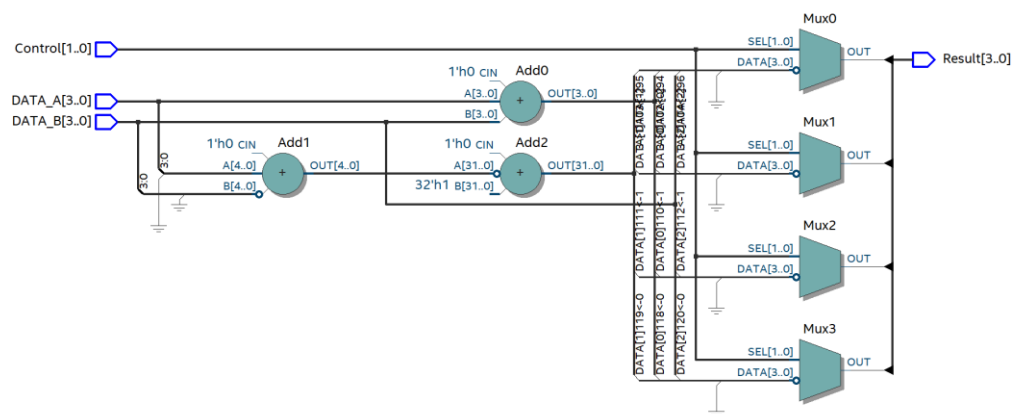


Figure 5: RTL Schematic for ALU.v

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85000.00ns INFO cocotb.ALU PASS: Control=0b11, A=7'h7, B=11'hb | Result: 0'h0
86000.00ns INFO cocotb.ALU PASS: Control=0b11, A=4'h4, B=4'h4 | Result: 0'h0
87000.00ns INFO cocotb.ALU PASS: Control=0b11, A=6'h6, B=8'h8 | Result: 0'h0
88000.00ns INFO cocotb.ALU PASS: Control=0b11, A=8'h8, B=6'h6 | Result: 0'h0
89000.00ns INFO cocotb.ALU PASS: Control=0b11, A=9'h9, B=5'h5 | Result: 0'h0
90000.00ns INFO cocotb.regression test_alu_width_variations passed
90000.00ns INFO cocotb.regression
*****
** TEST STATUS SIM TIME
*****
(ns) REAL TIME (s) RATIO (ns/s) **
*****
** test_alu.test_alu_width_variations PASS 90000
*****
** TESTS=1 PASS=1 FAIL=0 SKIP=0 90000
*****
make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP3/ALUTest/Tests'
(base) D:\METU-EE\EE-Sem-6\EE314\EXP3\ALUTest\Tests>

```

Figure 6: Testbench Results for ALU.v

6)

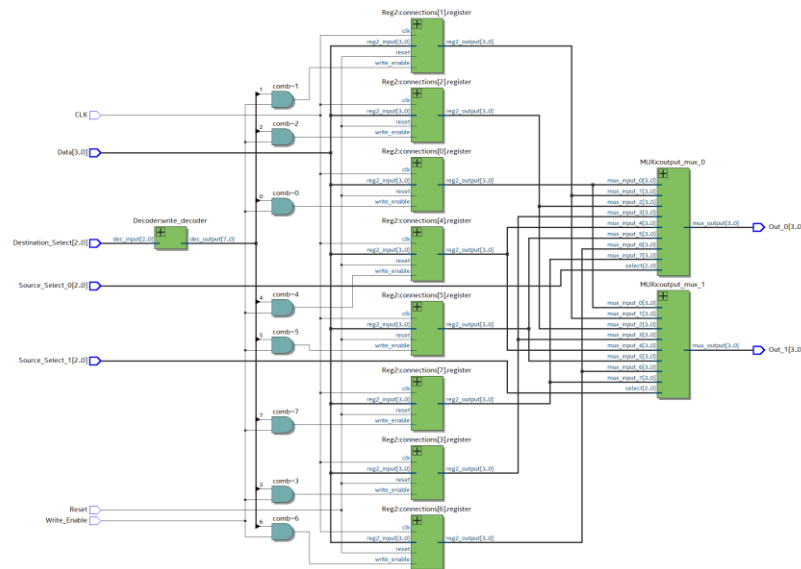


Figure 7: RTL Schematic for Register\_File.v

```

not detect Python virtual environment. Using system-wide Python interpreter
--ns INFO      gpi                ..\gpi\GpiCommon.cpp:101 in gpi_print_registered_impl      VPI
registered
0.00ns INFO      cocotb                Running on Icarus Verilog version 12.0 (devel)
0.00ns INFO      cocotb                Running tests with cocotb v1.9.2 from C:\Users\ASUS\AppData\Roam
ing\Python\Python312\site-packages\cocotb
0.00ns INFO      cocotb                Seeding Python random module with 1746369959
0.00ns INFO      cocotb.regression      Found test Register_File test test_register_file
0.00ns INFO      cocotb.regression      running test_register_file (1/1)
Testbench for the Register_File module.
All tests passed successfully with W = 4 bits!
test_register_file passed
*****
** TEST                                STATUS  SIM TIME (ns)
*****
REAL TIME (s)  RATIO (ns/s) **
*****
0.05  19567661.41 **
*****
2.00  464948.29 **
*****
make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP3/Experiment3Materials-20250502/RegisterFileTest/Tests'
(base) D:\METU-EE\EE-Sem-6\EE314\EXP3\Experiment3Materials-20250502\RegisterFileTest\Tests>

```

Figure 8: Testbench Results for Register\_File.v