

EE314 EXP4 Preliminary

1)

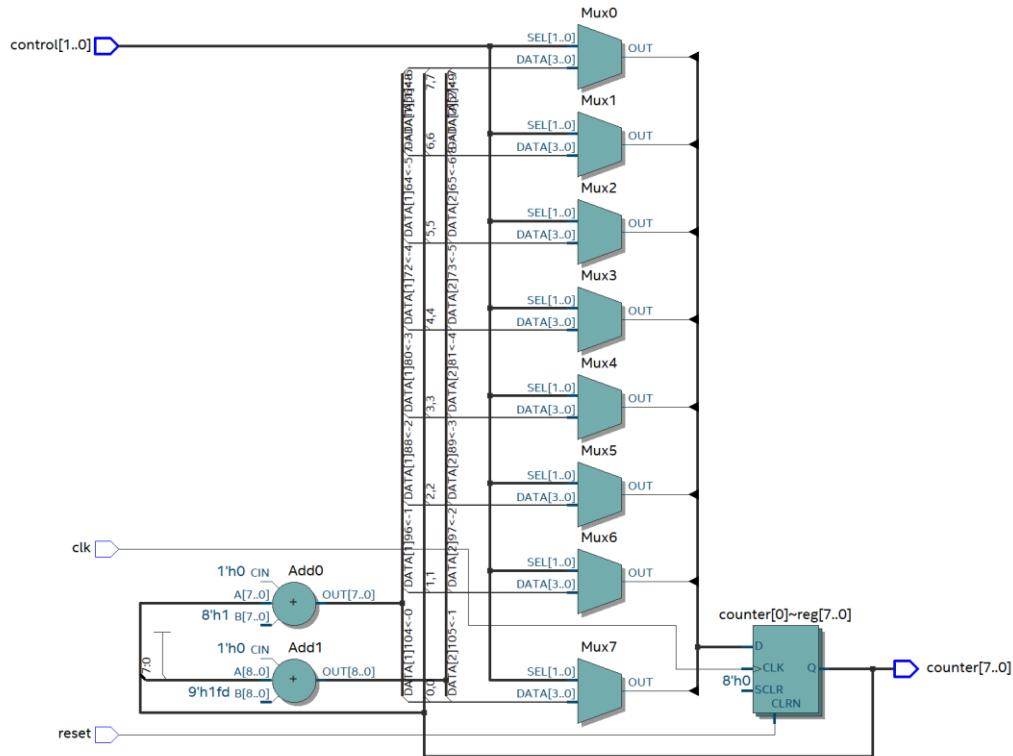


Figure 1: RTL Schematic for Counter.v

2)

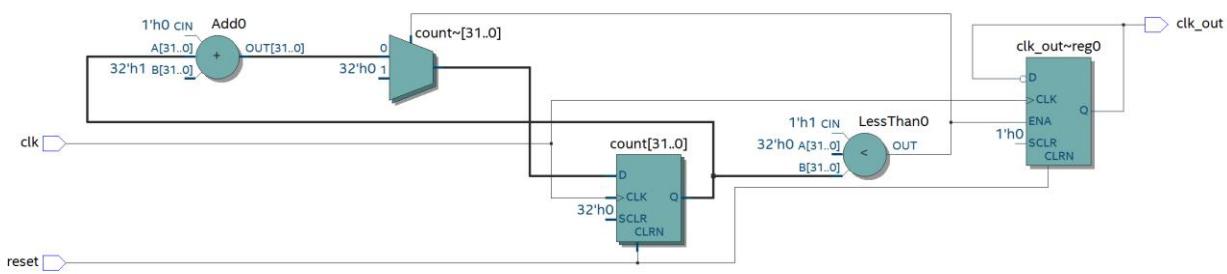


Figure 2: RTL Schematic for Clock_Divider.v

3)

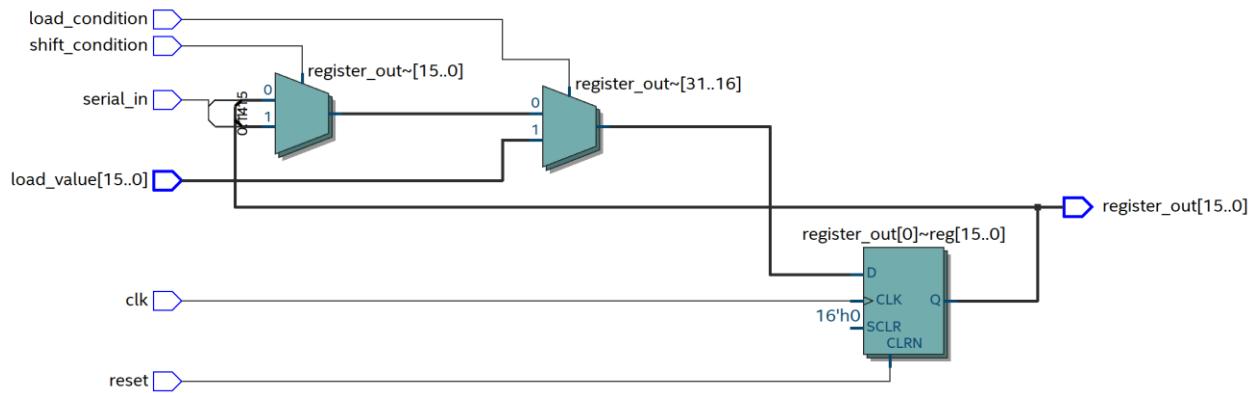


Figure 3: RTL Schematic for Shift_Register.v

4)

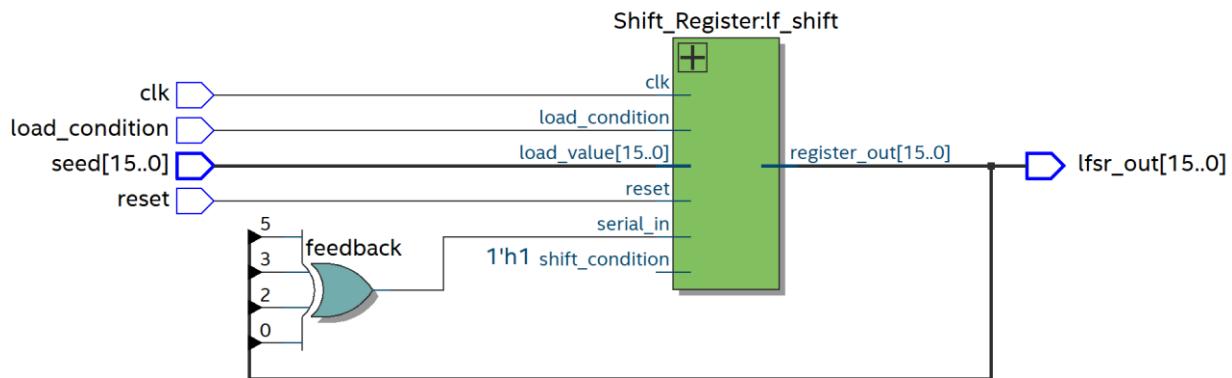


Figure 4: RTL Schematic for LFSR.v

5)

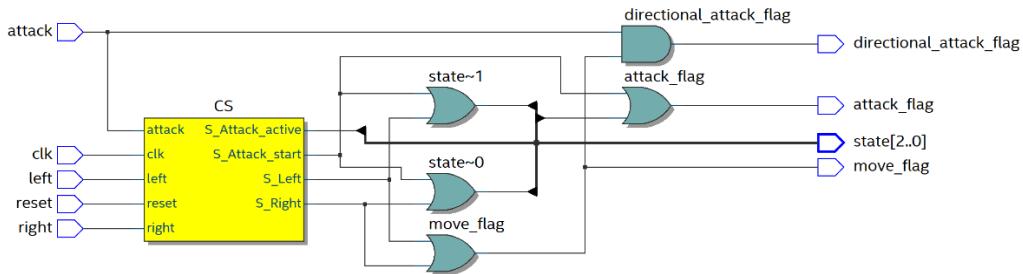


Figure 5: RTL Schematic for Small_Game.v

```

registered
  0.00ns INFO    cocotb
  0.00ns INFO    cocotb
  0.00ns INFO    cocotb
  0.00ns INFO    cocotb.regression
  0.00ns INFO    cocotb.regression
Passed Transition to Left
Passed Transition to IDLE
Passed Transition to Right
  41000.00ns INFO    cocotb.Small_Game
  42000.00ns INFO    cocotb.regression
  42000.00ns INFO    cocotb.regression
*****
TIME (s)  RATIO (ns/s) **
*****
  0.00      inf  **
*****
  0.16    265241.24  **
*****
make[1]: Leaving directory '/d/METU-EE/EE-Sem-6/EE314/EXP4/Exp4_Tests/Small_Game/Tests'

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Running on Icarus Verilog version 12.0 (devel)
 Running tests with cocotb v1.9.2 from C:\Users\ASUS\AppData\Roam
 Seeding Python random module with 1747592923
 Found test Small_Game_test.Small_Game_test
 running Small_Game_test (1/1)

All tests passed successfully!
 Small_Game_test **passed**

** TEST	STATUS	SIM TIME (ns)	REAL
** Small_Game_test.Small_Game_test	PASS	42000.00	

** TESTS=1 PASS=1 FAIL=0 SKIP=0 42000.00

Figure 6: Test Results for Small_Game.v