Electronics
Section 03

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Fayoum Center & Assiut Center

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Nodal Analysis

Steps to Determine Node Voltages:

1. Select a node as the reference node. Assign voltages v_1, $v_2, \ldots, v_{n-1}$ to the remaining $n - 1$ nodes. The voltages are referenced with respect to the reference node.
2. Apply KCL to each of the $n - 1$ nonreference nodes. Use Ohm's law to express the branch currents in terms of node voltages.
3. Solve the resulting simultaneous equations to obtain the unknown node voltages.

Current flows from a higher potential to a lower potential in a resistor.

We can express this principle as

$$\boxed{i = \frac{v_{\text{higher}} - v_{\text{lower}}}{R}}$$

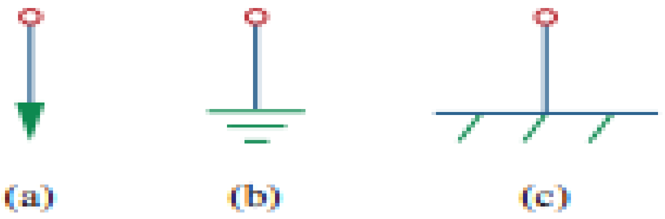


Figure
Common symbols for indicating a reference node, (a) common ground, (b) ground, (c) chassis ground.

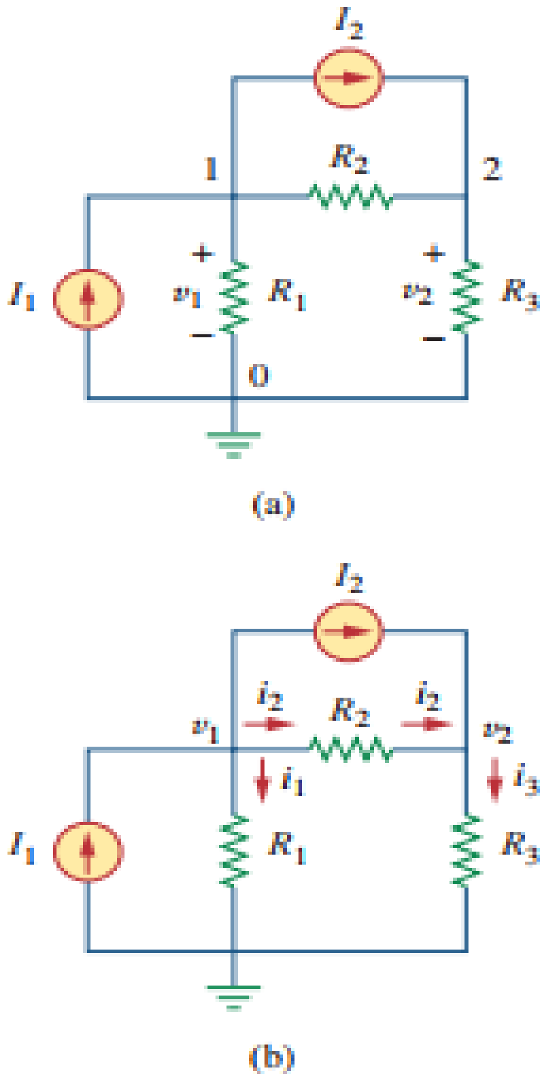


Figure
Typical circuit for nodal analysis.

Mesh Analysis

A **mesh** is a loop which does not contain any other loops within it.

Steps to Determine Mesh Currents:

1. Assign mesh currents $i_1, i_2, \ldots, i_n$ to the n meshes.
2. Apply KVL to each of the n meshes. Use Ohm's law to express the voltages in terms of the mesh currents.
3. Solve the resulting n simultaneous equations to get the mesh currents.

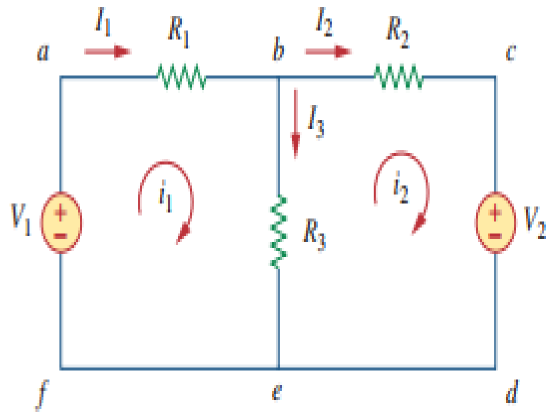


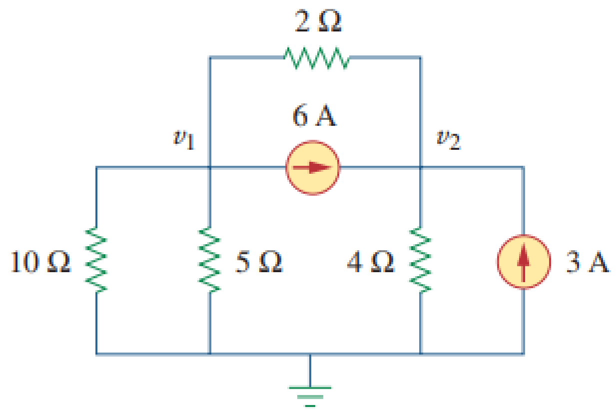
Figure
A circuit with two meshes.

Nodal Versus Mesh Analysis

The first factor is the nature of the particular network. Networks that contain many series-connected elements, voltage sources, or supermeshes are more suitable for mesh analysis, whereas networks with parallel-connected elements, current sources, or supernodes are more suitable for nodal analysis. Also, a circuit with fewer nodes than meshes is better analyzed using nodal analysis, while a circuit with fewer meshes than nodes is better analyzed using mesh analysis. The key is to select the method that results in the smaller number of equations.

The second factor is the information required. If node voltages are required, it may be expedient to apply nodal analysis. If branch or mesh currents are required, it may be better to use mesh analysis.

Q1. For the circuit in Fig. , obtain v_1 and v_2.



Solution

At node 1,

$$\frac{-v_1}{10} - \frac{v_1}{5} = 6 + \frac{v_1 - v_2}{2} \longrightarrow 60 = -8v_1 + 5v_2 \qquad (1)$$

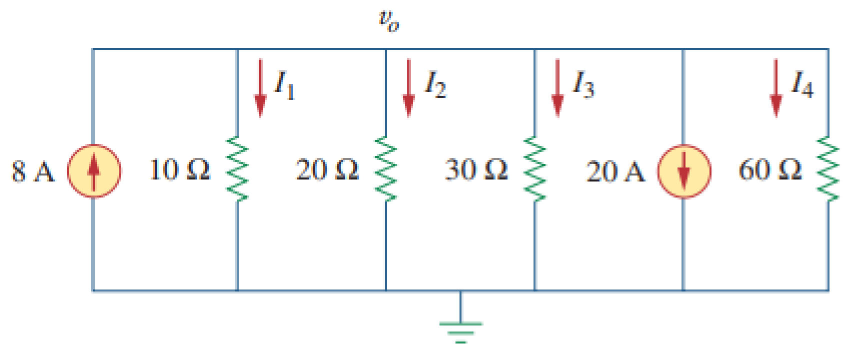
At node 2,

$$\frac{v_2}{4} = 3 + 6 + \frac{v_1 - v_2}{2} \longrightarrow 36 = -2v_1 + 3v_2 \qquad (2)$$

Solving (1) and (2),

$$v_1 = \mathbf{0\ V},\ v_2 = \mathbf{12\ V}$$

Q2. Find the currents I_1 through I_4 and the voltage v_o in the circuit of Fig.



Solution

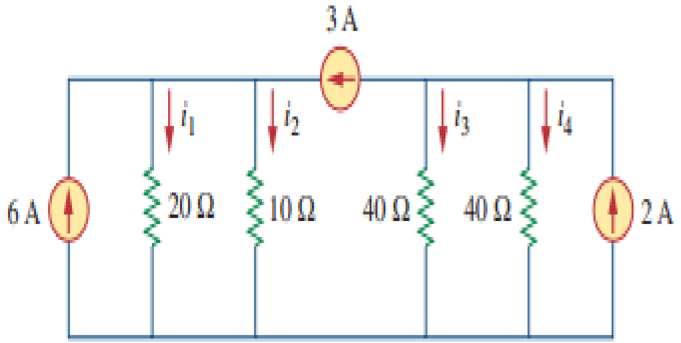
Applying KCL to the upper node,

$$-8+\frac{v_0}{10}+\frac{v_o}{20}+\frac{v_o}{30}+20+\frac{v_0}{60}=0 \text{ or } v_0=\mathbf{-60\ V}$$

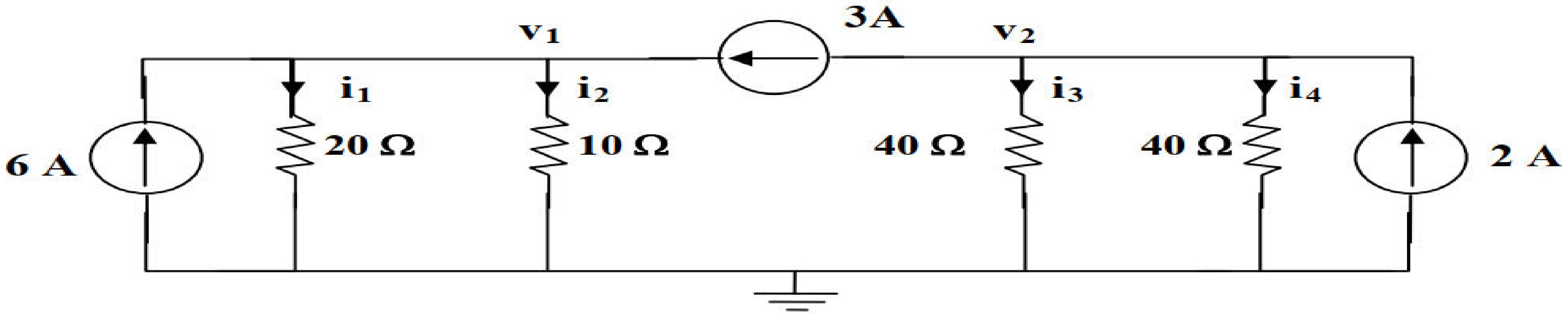
$$i_1=\frac{v_0}{10}=\mathbf{-6\ A}\ ,\ i_2=\frac{v_0}{20}=\mathbf{-3\ A},$$

$$i_3=\frac{v_0}{30}=\mathbf{-2\ A},\ i_4=\frac{v_0}{60}=\mathbf{-1\ A}.$$

Q3. Given the circuit in Fig. , calculate the currents i_1 through i_4.



Solution



At node 1,

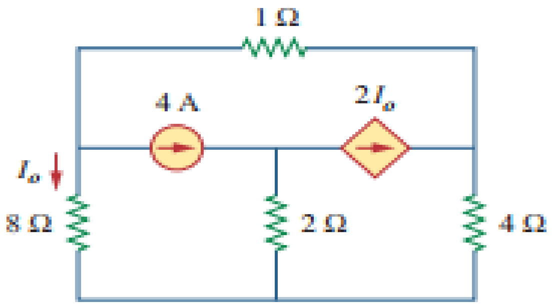
$$-6 - 3 + v_1/(20) + v_1/(10) = 0 \text{ or } v_1 = 9(200/30) = 60 \text{ V}$$

At node 2,

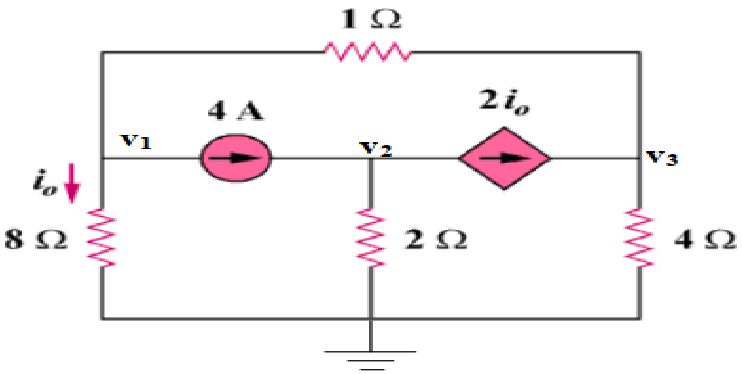
$$3 - 2 + v_2/(40) + v_2/40 = 0 \text{ or } v_2 = -1(1600/80) = -20 \text{ V}$$

$$i_1 = v_1/(20) = \mathbf{3\ A},\ i_2 = v_1/(10) = \mathbf{6\ A},$$
$$i_3 = v_2/(40) = \mathbf{-500\ mA},\ i_4 = v_2/(40) = \mathbf{-500\ mA}.$$

Q4. Find I_o in the circuit of Fig.



Solution



At node 1. $[(v_1-0)/8] + [(v_1-v_3)/1] + 4 = 0$

At node 2. $-4 + [(v_2-0)/2] + 2i_o = 0$

At node 3. $-2i_o + [(v_3-0)/4] + [(v_3-v_1)/1] = 0$

Finally, we need a constraint equation, $i_o = v_1/8$

This produces,

$$1.125v_1 - v_3 = 4 \quad (1)$$

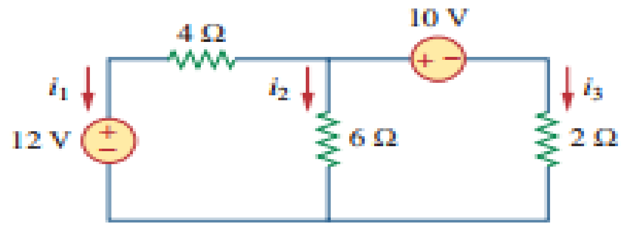
$$0.25v_1 + 0.5v_2 = 4 \quad (2)$$

$$-1.25v_1 + 1.25v_3 = 0 \text{ or } v_1 = v_3 \quad (3)$$

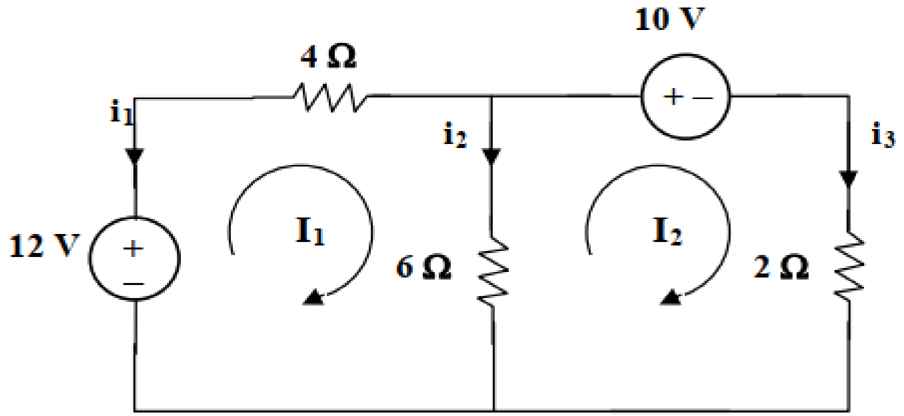
Substituting (3) into (1) we get $(1.125-1)v_1 = 4$ or $v_1 = 4/0.125 = 32$ volts. This leads to,

$i_o = 32/8 =$ **4 amps**.

Q5. Use mesh analysis to obtain i_1, i_2, and i_3 in the circuit in Fig. :



Solution



Applying mesh analysis gives,

$$10I_1 - 6I_2 = 12 \text{ and } -6I_1 + 8I_2 = -10$$

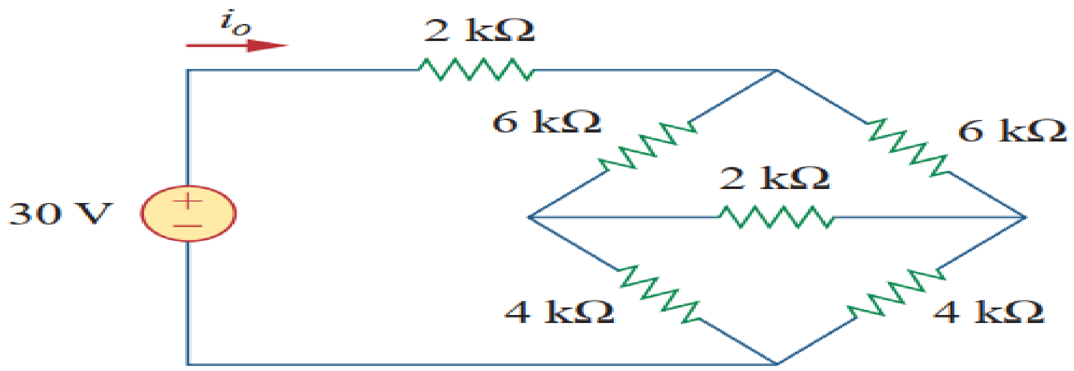
or

$$\begin{bmatrix} 6 \\ -5 \end{bmatrix} = \begin{bmatrix} 5 & -3 \\ -3 & 4 \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} 6 \\ -5 \end{bmatrix} \text{ or } \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \frac{\begin{bmatrix} 4 & 3 \\ 3 & 5 \end{bmatrix}}{11} \begin{bmatrix} 6 \\ -5 \end{bmatrix}$$

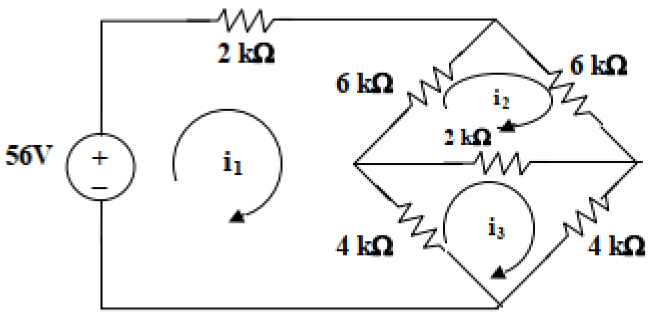
$$I_1 = (24–15)/11 = 0.8182 \text{ and } I_2 = (18–25)/11 = –0.6364$$

$i_1 = –I_1 = $ **–818.2 mA**; $i_2 = I_1 – I_2 = 0.8182+0.6364 = $ **1.4546 A**; and $i_3 = I_2 = $ **–636.4 mA**.

Q6. For the bridge network in Fig. , find i_o using mesh analysis.



Solution



Assume all currents are in mA and apply mesh analysis for mesh 1.

$$-56 + 12i_1 - 6i_2 - 4i_3 = 0 \text{ or } 6i_1 - 3i_2 - 2i_3 = 28 \quad (1)$$

for mesh 2,

$$-6i_1 + 14i_2 - 2i_3 = 0 \text{ or } -3i_1 + 7i_2 - i_3 = 0 \quad (2)$$

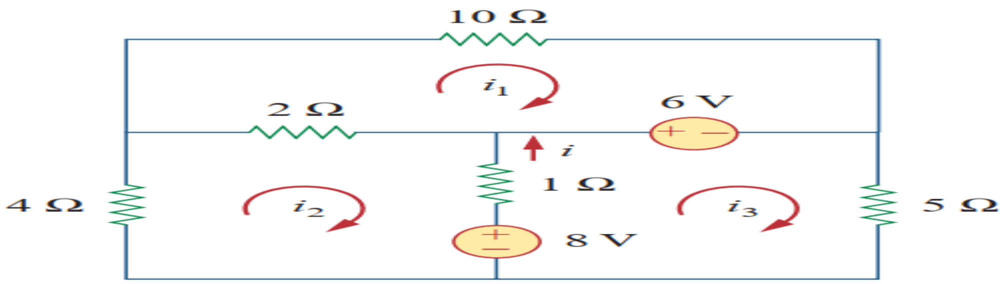
for mesh 3,

$$-4i_1 - 2i_2 + 10i_3 = 0 \text{ or } -2i_1 - i_2 + 5i_3 = 0 \quad (3)$$

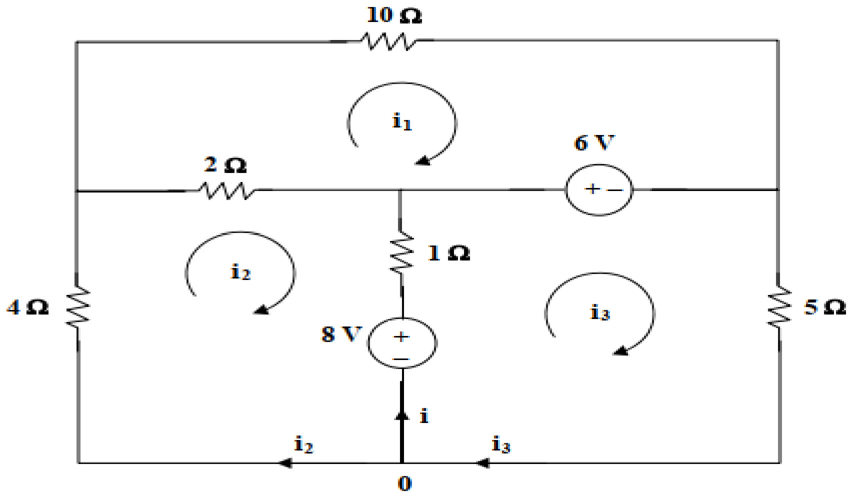
Solving (1), (2), and (3) using MATLAB, we obtain,

$$\boldsymbol{i_o = i_1 = 8 \text{ mA}}.$$

Q7. Apply mesh analysis to find i in Fig.



Solution



For loop 1,

$$6 = 12i_1 - 2i_2 \longrightarrow 3 = 6i_1 - i_2 \qquad (1)$$

For loop 2,

$$-8 = -2i_1 + 7i_2 - i_3 \qquad (2)$$

For loop 3,

$$-8 + 6 + 6i_3 - i_2 = 0 \longrightarrow 2 = -i_2 + 6i_3 \qquad (3)$$

We put (1), (2), and (3) in matrix form,

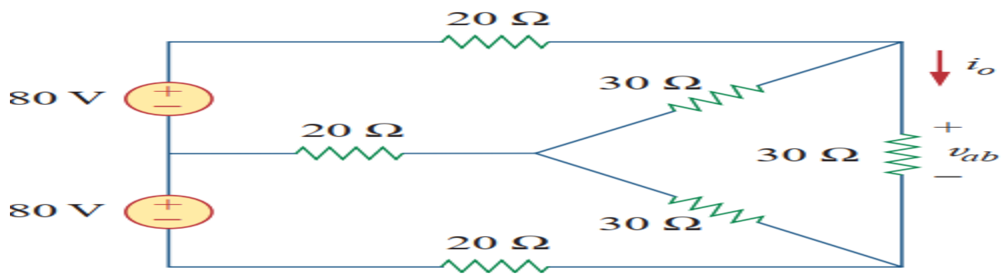
$$\begin{bmatrix} 6 & -1 & 0 \\ 2 & -7 & 1 \\ 0 & -1 & 6 \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \end{bmatrix} = \begin{bmatrix} 3 \\ 8 \\ 2 \end{bmatrix}$$

$$\Delta = \begin{vmatrix} 6 & -1 & 0 \\ 2 & -7 & 1 \\ 0 & -1 & 6 \end{vmatrix} = -234, \quad \Delta_2 = \begin{vmatrix} 6 & 3 & 0 \\ 2 & 8 & 1 \\ 0 & 2 & 6 \end{vmatrix} = 240$$

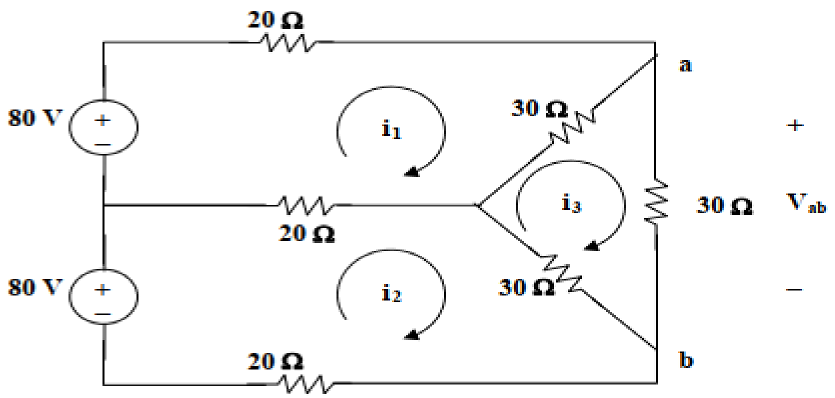
$$\Delta_3 = \begin{vmatrix} 6 & -1 & 3 \\ 2 & -7 & 8 \\ 0 & -1 & 2 \end{vmatrix} = -38$$

At node 0, $i + i_2 = i_3$ or $i = i_3 - i_2 = \dfrac{\Delta_3 - \Delta_2}{\Delta} = \dfrac{-38 - 240}{-234} =$ **1.188 A**

Q8. Use mesh analysis to find v_{ab} and i_o in the circuit of Fig. . . . . .



Solution



For loop 1,

$80 = 70i_1 - 20i_2 - 30i_3 \longrightarrow 8 = 7i_1 - 2i_2 - 3i_3$ (1)

For loop 2,

$80 = 70i_2 - 20i_1 - 30i_3 \longrightarrow 8 = -2i_1 + 7i_2 - 3i_3$ (2)

For loop 3,

$0 = -30i_1 - 30i_2 + 90i_3 \longrightarrow 0 = i_1 + i_2 - 3i_3$
(3)

Solving (1) to (3), we obtain $i_3 = 16/9$

$I_o = i_3 = 16/9 =$ **1.7778 A**

$V_{ab} = 30i_3 =$ **53.33 V**.

MCQ

(1) At node 1 in the circuit of Fig. ' , applying KCL gives:

(a) $2 + \frac{12 - v_1}{3} = \frac{v_1}{6} + \frac{v_1 - v_2}{4}$

(b) $2 + \frac{v_1 - 12}{3} = \frac{v_1}{6} + \frac{v_2 - v_1}{4}$

(c) $2 + \frac{12 - v_1}{3} = \frac{0 - v_1}{6} + \frac{v_1 - v_2}{4}$

(d) $2 + \frac{v_1 - 12}{3} = \frac{0 - v_1}{6} + \frac{v_2 - v_1}{4}$

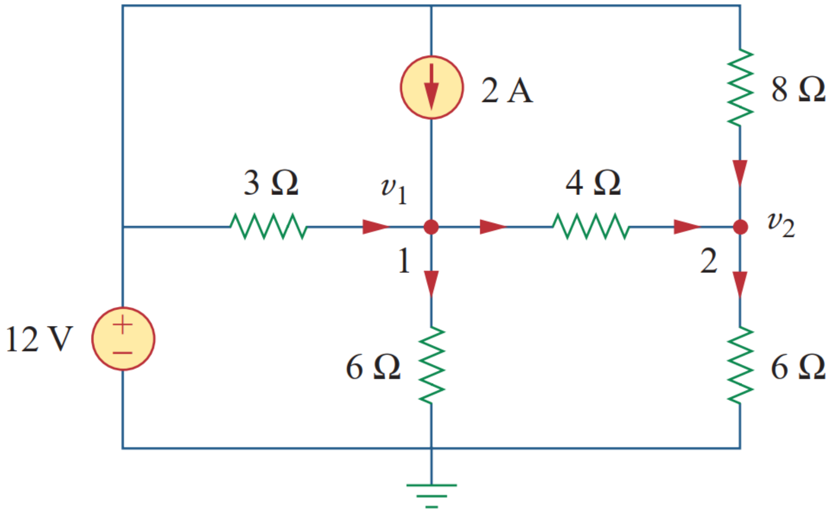
(2) In the circuit of Fig. : , applying KCL at node 2 gives:

(a) $\frac{v_2 - v_1}{4} + \frac{v_2}{8} = \frac{v_2}{6}$

(b) $\frac{v_1 - v_2}{4} + \frac{v_2}{8} = \frac{v_2}{6}$

(c) $\frac{v_1 - v_2}{4} + \frac{12 - v_2}{8} = \frac{v_2}{6}$

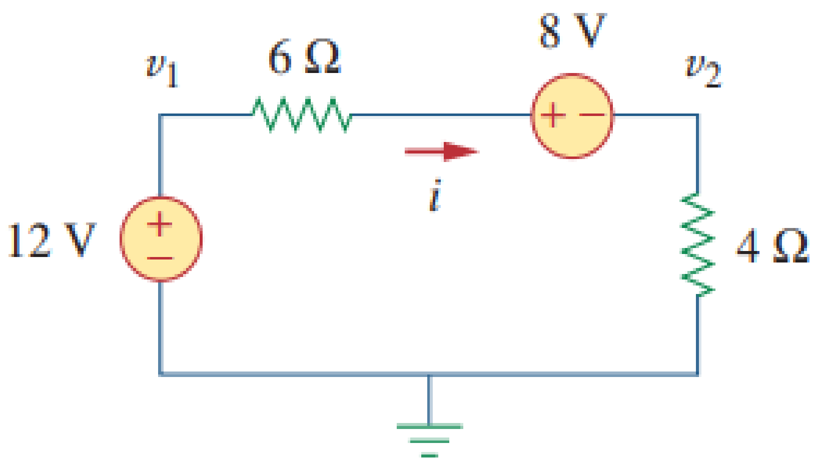
(d) $\frac{v_2 - v_1}{4} + \frac{v_2 - 12}{8} = \frac{v_2}{6}$



(3) For the circuit in Fig , v_1 and v_2 are related as:

(a) $v_1 = 6i + 8 + v_2$ (b) $v_1 = 6i - 8 + v_2$

(c) $v_1 = -6i + 8 + v_2$ (d) $v_1 = -6i - 8 + v_2$



(4) The current i in the circuit of Fig. is:

(a) -2.667 A (b) -0.667 A

(c) 0.667 A (d) 2.667 A

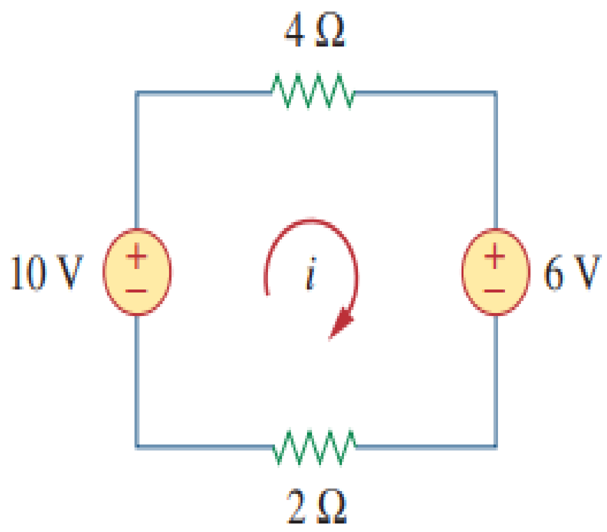
(5) The loop equation for the circuit in Fig. is:

(a) $-10 + 4i + 6 + 2i = 0$

(b) $10 + 4i + 6 + 2i = 0$

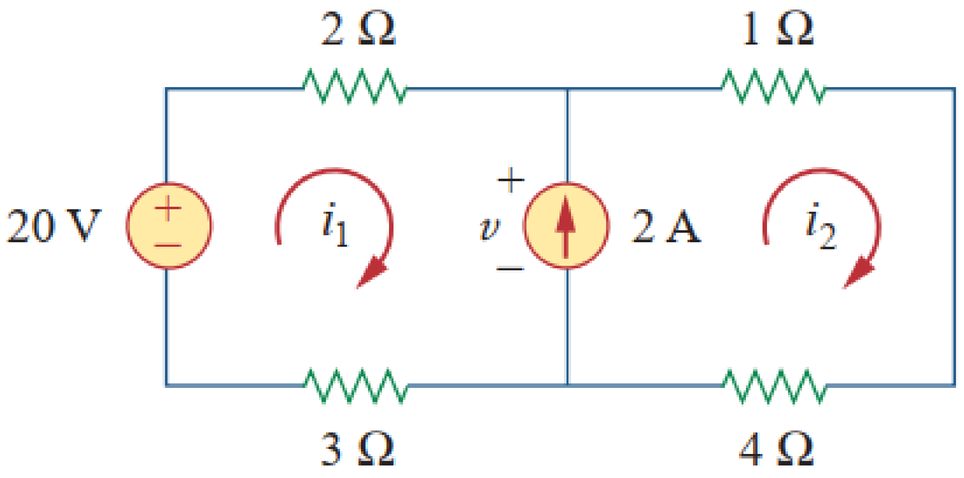
(c) $10 + 4i - 6 + 2i = 0$

(d) $-10 + 4i - 6 + 2i = 0$



(6) The voltage v across the current source in the circuit i_1 =1A of Fig. 3.49 is:

(a) 20 V (b) 15 V (c) 10 V (d) 5 V



(7) The *PSpice* part name for a current-controlled voltage source is:

(a) EX (b) FX (c) HX (d) GX

(8) Which of the following statements are not true of the pseudocomponent IPROBE:

(a) It must be connected in series.

(b) It plots the branch current.

(c) It displays the current through the branch in which it is connected.

(d) It can be used to display voltage by connecting it in parallel.

(e) It is used only for dc analysis.

(f) It does not correspond to a particular circuit element.