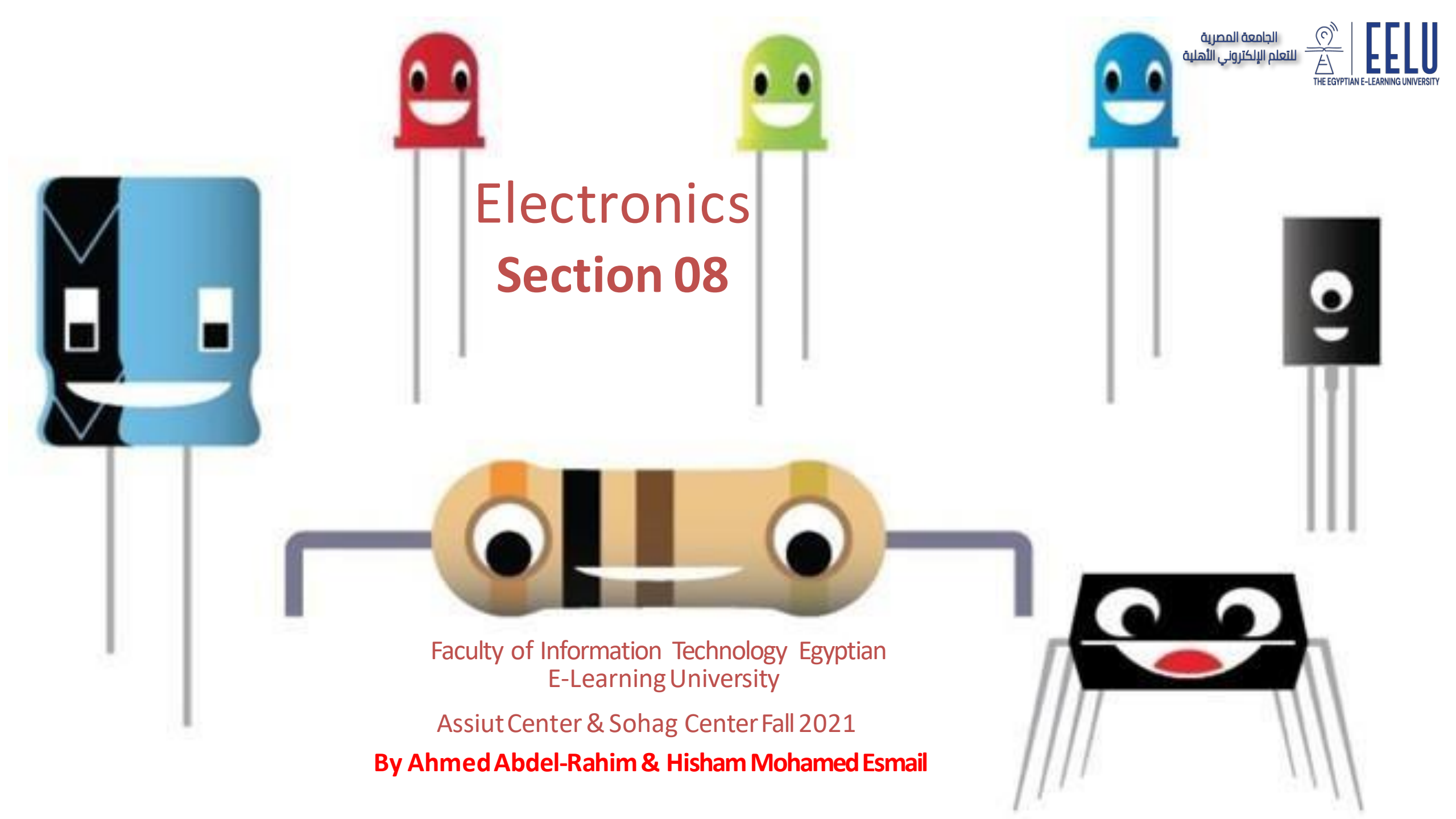


# Electronics

## Section 08

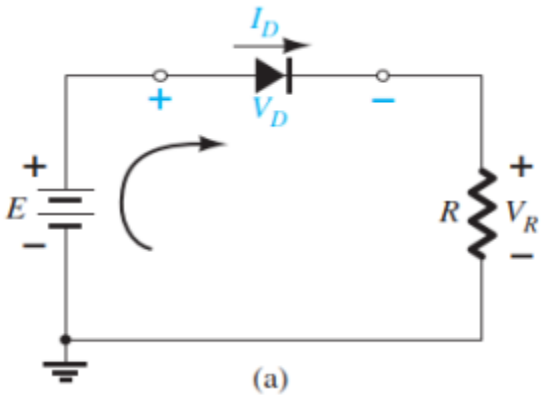
Faculty of Information Technology Egyptian E-Learning University

Assiut Center & Sohag Center Fall 2021

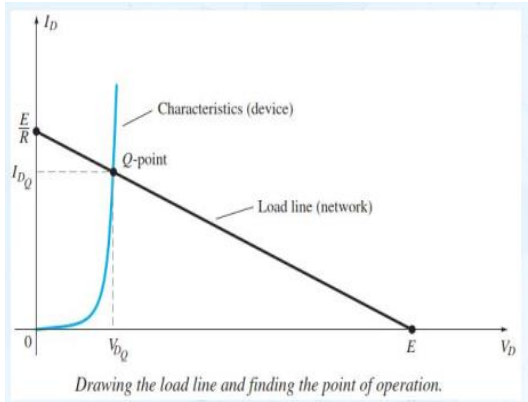
**By Ahmed Abdel-Rahim & Hisham Mohamed Esmail**

# Diode Applications

## 1.LOAD-LINE ANALYSIS




(a)




*Drawing the load line and finding the point of operation.*

$$+E - V_D - V_R = 0$$

$$E = V_D + I_D R$$

$$I_D = \frac{E}{R}\bigg|_{V_D=0\,\text{V}}$$

$$V_D = E\big|_{I_D=0\,\text{A}}$$

## 2. SERIES DIODE CONFIGURATIONS

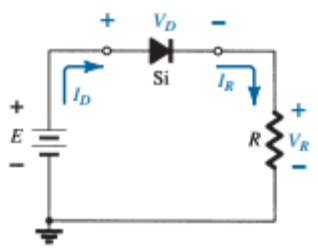
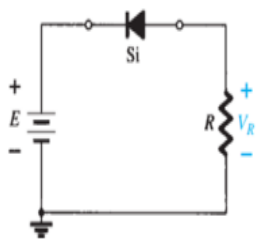
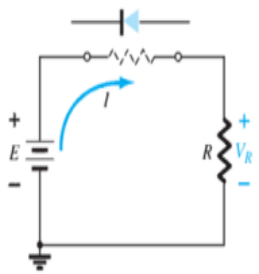


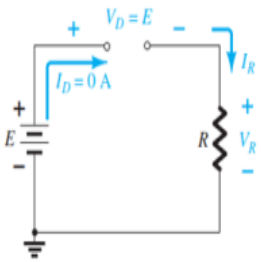

**FIG. 8**
*Series diode configuration.*




*Reversing the diode*




*Determining the state of the diode*



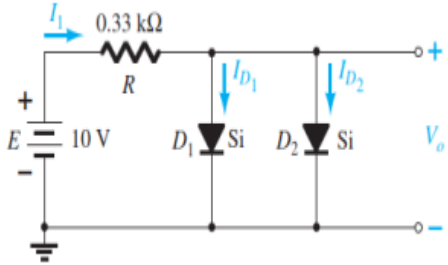

*Substituting the equivalent model for the "off" diode*

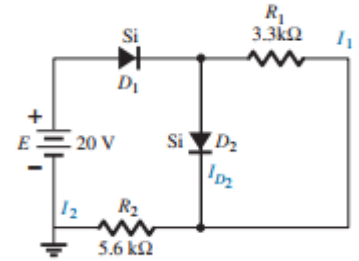
$$V_D = V_K$$

$$V_R = E - V_K$$

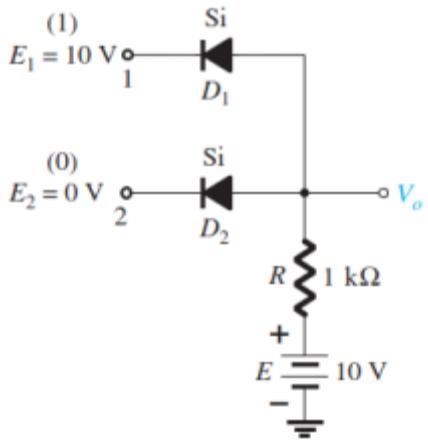
$$I_D = I_R = \frac{V_R}{R}$$

## 3.PARALLEL AND SERIES–PARALLEL CONFIGURATIONS

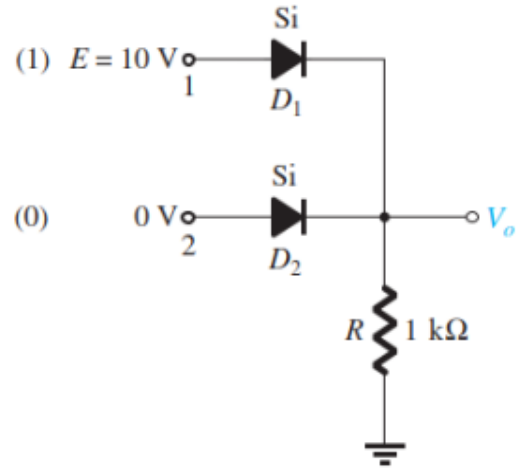



## 4.AND/OR GATES




*Positive logic AND gate.*




*Positive logic OR gate.*

## 5.Half-WAVE RECTIFICATION

$V_{dc} = 0.318\,V_m$ half-wave

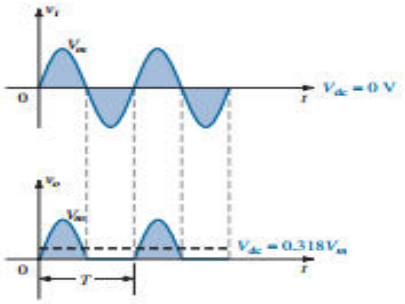
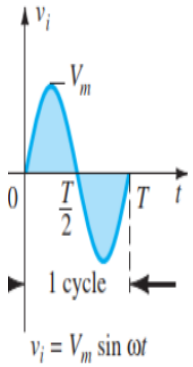
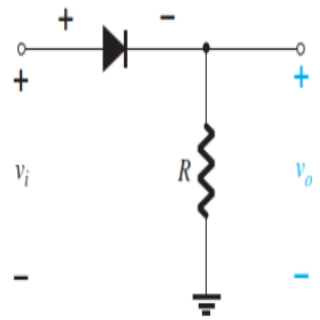


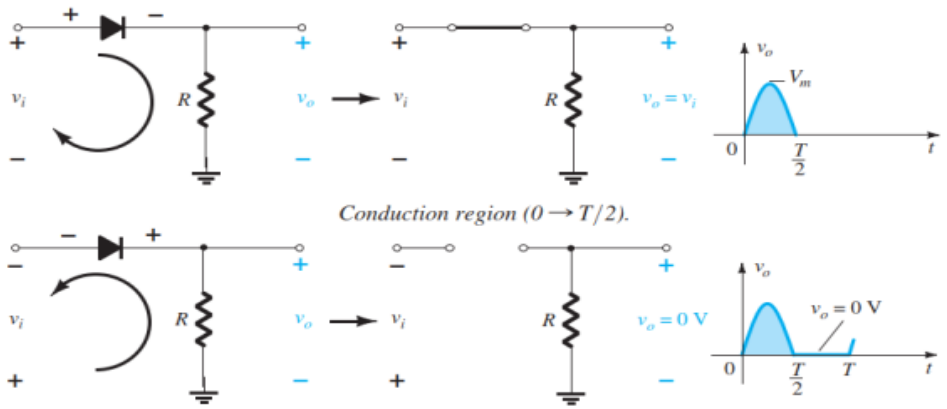

FIG.
*Half-wave rectified signal.*




$v_i = V_m \sin \omega t$




*Half-wave rectifier.*



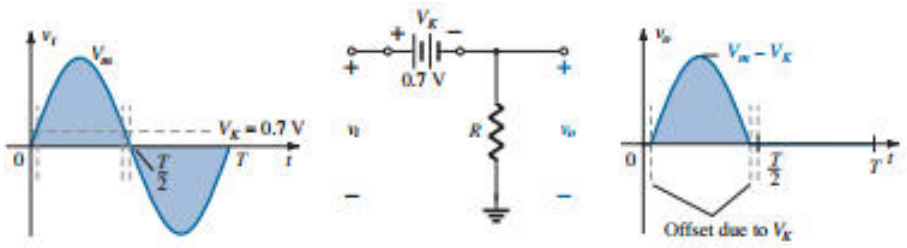




FIG.
*Effect of $V_K$ on half-wave rectified signal.*

$V_{dc} \cong 0.318(V_m - V_K)$

## 6.FULL-WAVE RECTIFICATION

$V_{dc} = 0.636\,V_m$ full-wave

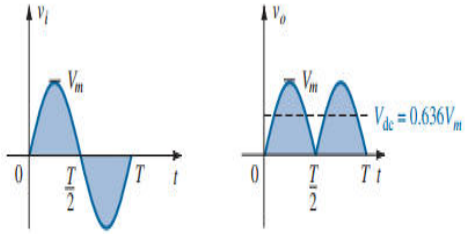
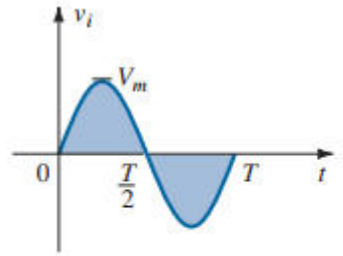



FIG.
*Input and output waveforms for a full-wave rectifier.*



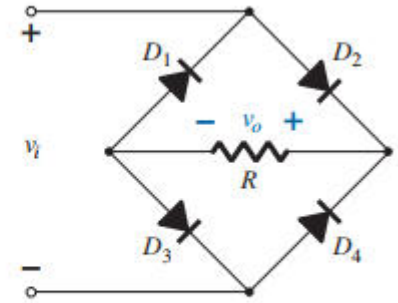




FIG.
*Full-wave bridge rectifier.*

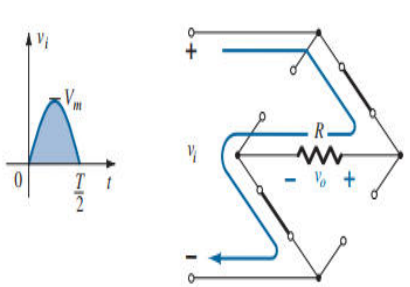



FIG.
*Conduction path for the positive region of $v_i$.*

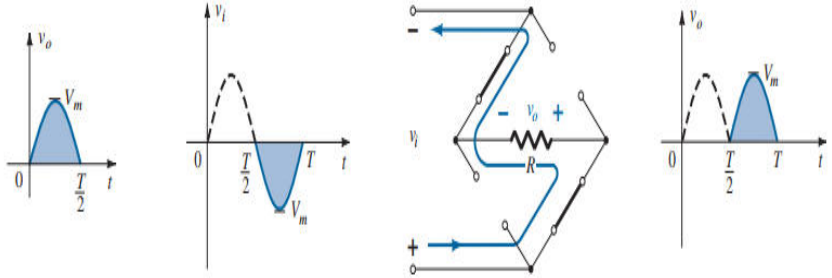
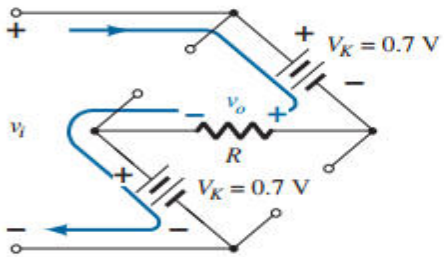



FIG.
*Conduction path for the negative region of $v_i$.*



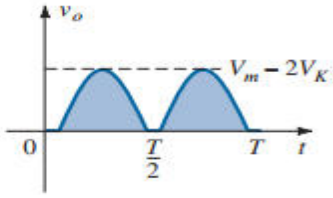



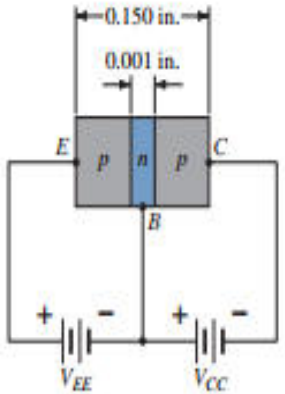

FIG.
*Determining $V_{o_{max}}$ for silicon diodes in the bridge configuration.*

$V_{dc} \cong 0.636(V_m - 2V_K)$

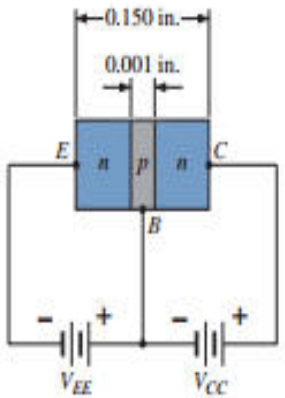
# Bipolar Junction Transistors (BJT)

## Transistor Construction

**FIG.**
*The first transistor. (Courtesy of AT&T Archives and History Center.)*




(a)




(b)

**FIG.**
*Types of transistors: (a) pnp; (b) npn.*

## Transistor Operation

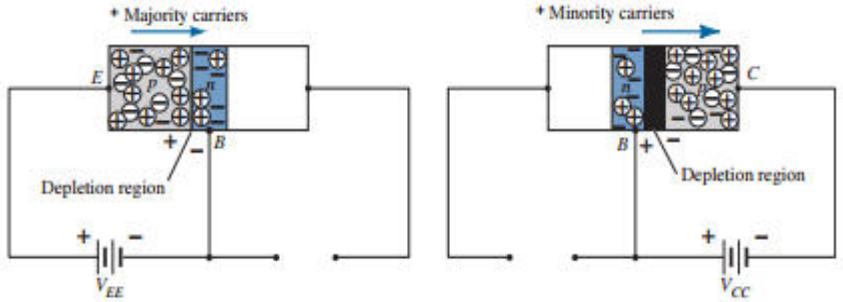



**FIG.**
*Biasing a transistor: (a) forward-bias; (b) reverse-bias.*

***One p–n junction of a transistor is reverse-biased, whereas the other is forward biased.***

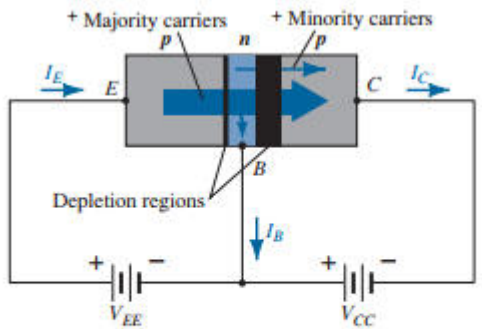
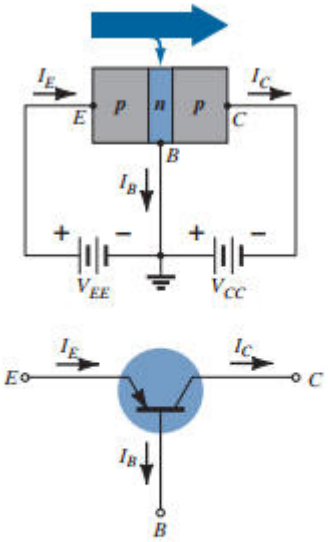


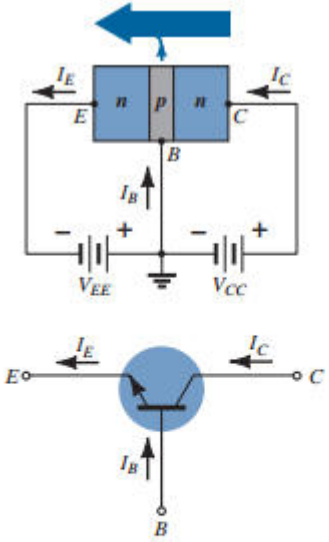

**FIG.**
*Majority and minority carrier flow of a pnp transistor.*

$$I_E = I_C + I_B$$

$$I_C = I_{C_{majority}} + I_{CO_{minority}}$$



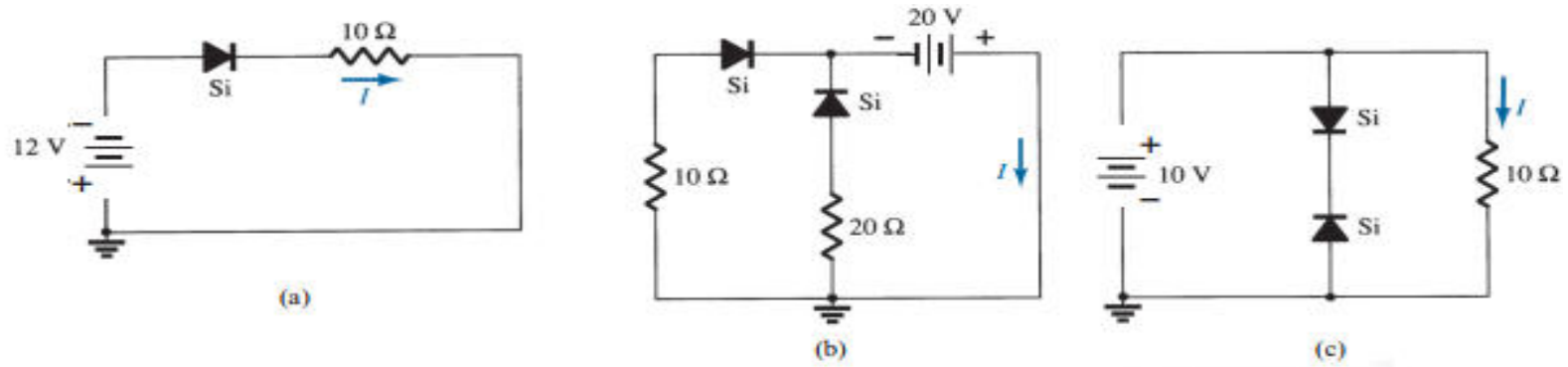

(a)




(b)

**FIG.**
*Notation and symbols used with the common-base configuration: (a) pnp transistor; (b) npn transistor.*

**Q1. Determine the current I for each of the configurations of Figure. using the approximate equivalent model for the diode.**




## Solution

(a) $I = \mathbf{0\ mA}$; diode reverse-biased.

(b) $V_{20\Omega} = 20\ \text{V} - 0.7\ \text{V} = 19.3\ \text{V}$ (Kirchhoff's voltage law)

$$I(20\ \Omega) = \frac{19.3\ \text{V}}{20\ \Omega} = 0.965\ \text{A}$$

$$V(10\ \Omega) = 20\ \text{V} - 0.7\ \text{V} = 19.3\ \text{V}$$

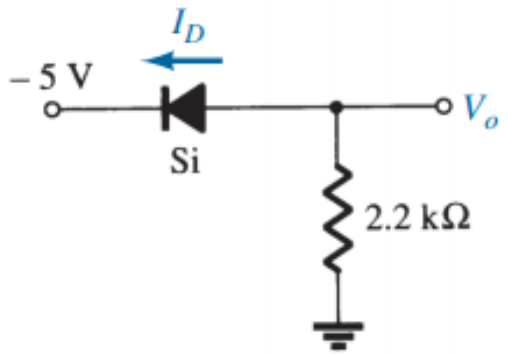
$$I(10\ \Omega) = \frac{19.3\ \text{V}}{10\ \Omega} = 1.93\ \text{A}$$

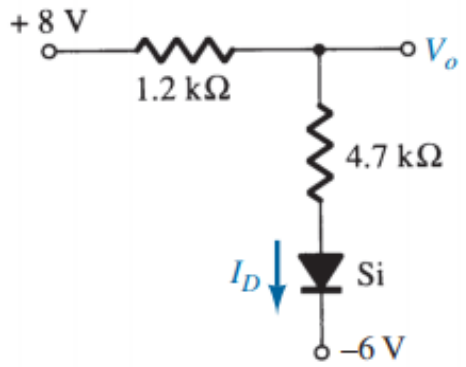
$$I = I(10\ \Omega) + I(20\ \Omega)$$

$$= \mathbf{2.895\ A}$$

(c) $I = \dfrac{10\ \text{V}}{10\ \Omega} = \mathbf{1\ A}$; center branch open

## Q2. Determine $V_o$ and $I_D$ for the networks of Figure.




### Solution

(a) Diode forward-biased,

Kirchhoff's voltage law (CW): $-5\text{ V} + 0.7\text{ V} - V_o = 0$

$$V_o = \mathbf{-4.3\text{ V}}$$

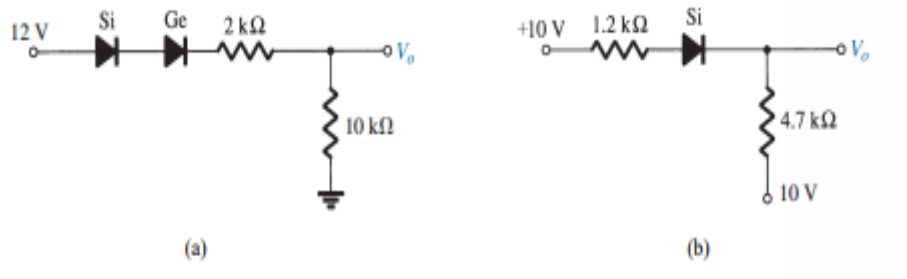
$$I_R = I_D = \frac{|V_o|}{R} = \frac{4.3\text{ V}}{2.2\text{ k}\Omega} = \mathbf{1.955\text{ mA}}$$

(b) Diode forward-biased,

$$I_D = \frac{8\text{ V} + 6\text{ V} - 0.7\text{ V}}{1.2\text{ k}\Omega + 4.7\text{ k}\Omega} = \mathbf{2.25\text{ mA}}$$

$$V_o = 8\text{ V} - (2.25\text{ mA})(1.2\text{ k}\Omega) = \mathbf{5.3\text{ V}}$$

## Q3. Determine the level of $V_o$ for each network of Figure.

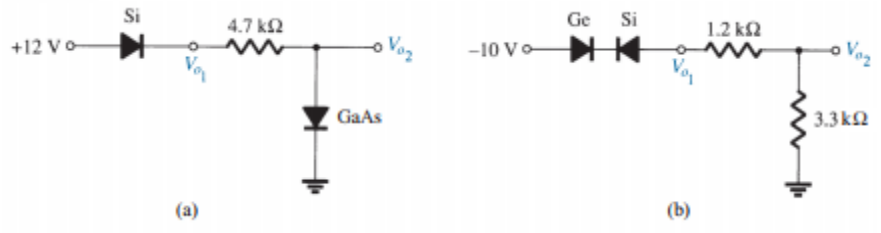



## Solution

(a) $V_o = \dfrac{10\,\text{k}\Omega(12\,\text{V} - 0.7\,\text{V} - 0.3\,\text{V})}{2\,\text{k}\Omega + 10\,\text{k}\Omega} = \mathbf{9.17\ V}$

(b) $V_o = \mathbf{10\ V}$

## Q4. Determine $V_{o1}$ and $V_{o2}$ for the networks of Figure.




## Solution

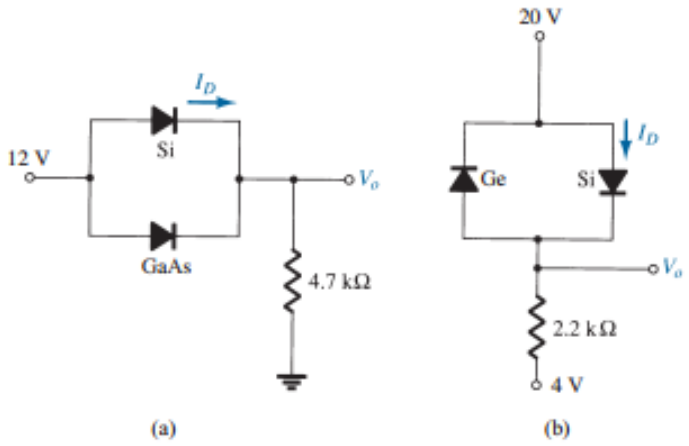
(a) $V_{o_1} = 12\,\text{V} - 0.7\,\text{V} = \mathbf{11.3\ V}$

$V_{o_2} = \mathbf{1.2\ V}$

(b) $V_{o_1} = \mathbf{0\ V}$

$V_{o_2} = \mathbf{0\ V}$

## Q5. Determine $V_o$ and $I_D$ for the networks of Figure.




## Solution

(a) Both diodes forward-biased
Si diode turns on first and locks in 0.7 V drop.

$$I_R = \frac{12\text{ V} - 0.7\text{ V}}{4.7\text{ k}\Omega} = 2.4\text{ mA}$$

$$I_D = I_R = \mathbf{2.4\text{ mA}}$$

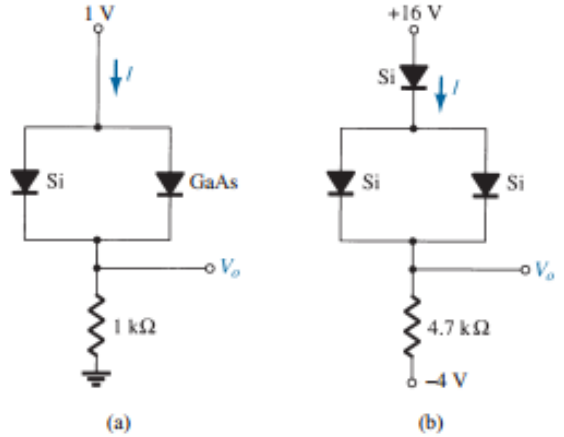
$$V_o = 12\text{ V} - 0.7\text{ V} = \mathbf{11.3\text{ V}}$$

(b) Right diode forward-biased:

$$I_D = \frac{20\text{ V} + 4\text{ V} - 0.7\text{ V}}{2.2\text{ k}\Omega} = \mathbf{10.59\text{ mA}}$$

$$V_o = 20\text{ V} - 0.7\text{ V} = \mathbf{19.3\text{ V}}$$

## Q6. Determine $V_o$ and $I_D$ for the networks of Figure.




## Solution

(a) Si diode "on" preventing GaAs diode from turning "on":

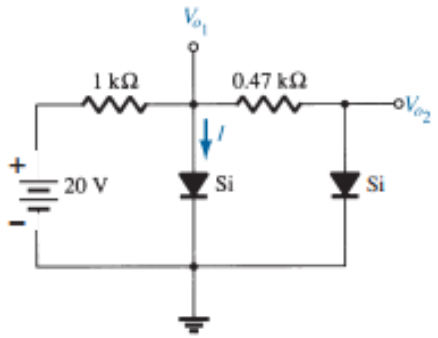
$$I = \frac{1\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \frac{0.3\text{ V}}{1\text{ k}\Omega} = \mathbf{0.3\text{ mA}}$$

$$V_o = 1\text{ V} - 0.7\text{ V} = \mathbf{0.3\text{ V}}$$

(b) $$I = \frac{16\text{ V} - 0.7\text{ V} - 0.7\text{ V} + 4\text{ V}}{4.7\text{ k}\Omega} = \frac{18.6\text{ V}}{4.7\text{ k}\Omega} = \mathbf{3.96\text{ mA}}$$

$$V_o = 16\text{ V} - 0.7\text{ V} - 0.7\text{ V} = \mathbf{14.6\text{ V}}$$

## Q7. Determine $Vo_1$, $Vo_2$, and $_I$ for the network of Figure.




## Solution

Both diodes forward-biased:

$V_{o_1} = \mathbf{0.7\ V}$, $V_{o_2} = \mathbf{0.7\ V}$

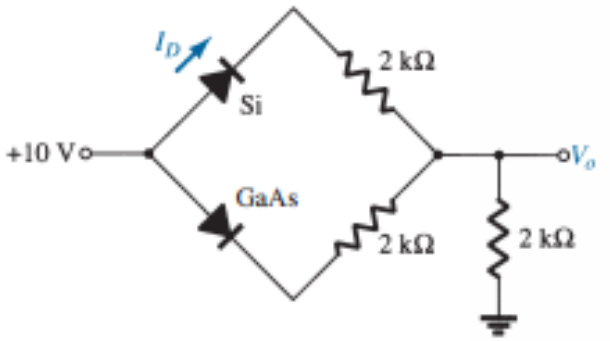
$$I_{1\,k\Omega} = \frac{20\ V - 0.7\ V}{1\ k\Omega} = \frac{19.3\ V}{1\ k\Omega} = 19.3\ mA$$

$I_{0.47\,k\Omega} = 0\ mA$

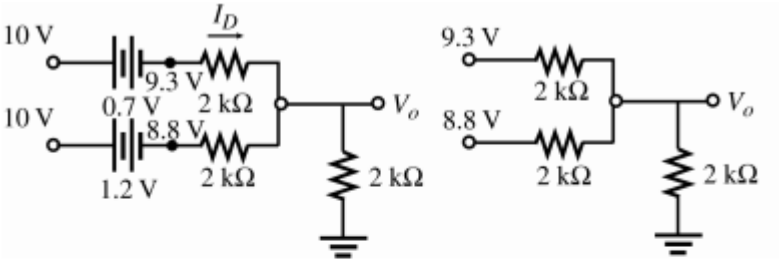
$I = I_{1\,k\Omega} - I_{0.47\,k\Omega} = 19.3\ mA - 0\ mA$

$= \mathbf{19.3\ mA}$

## Q8. Determine $V_o$ and $I_D$ for the network of Figure.




## Solution



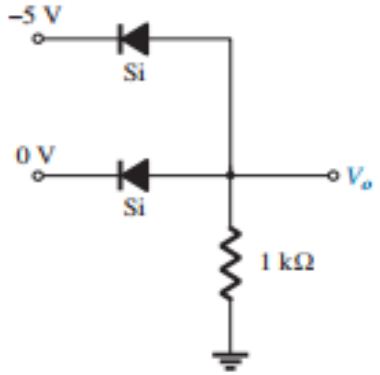

Superposition: $V_{o_1}(9.3\ V) = \dfrac{1\ k\Omega(9.3\ V)}{1\ k\Omega + 2\ k\Omega} = 3.1\ V$

$$V_{o_2}(8.8\ V) = \frac{16\ k\Omega(8.8\ V)}{1\ k\Omega + 2\ k\Omega} = 2.93\ V$$

$V_o = V_{o_1} + V_{o_2} = \mathbf{6.03\ V}$

$$I_D = \frac{9.3\ V - 6.03\ V}{2\ k\Omega} = \mathbf{1.635\ mA}$$

## Q9. Determine $V_o$ for the negative logic OR gate of Figure.

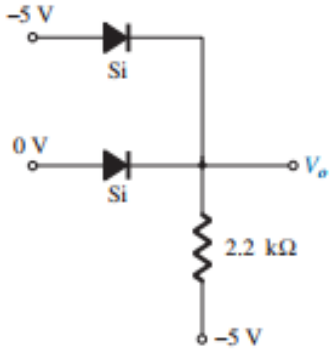



### Solution

The Si diode with −5 V at the cathode is "on" while the other is "off". The result is

$V_o = -5\text{ V} + 0.7\text{ V} = \mathbf{-4.3\text{ V}}$

## Q10. Determine $V_o$ for the negative logic AND gate of Figure.



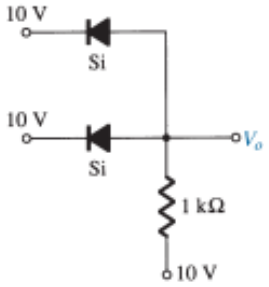

### Solution

0 V at one terminal is "more positive" than −5 V at the other input terminal. Therefore assume lower diode "on" and upper diode "off".
The result:

$V_o = 0\text{ V} - 0.7\text{ V} = \mathbf{-0.7\text{ V}}$

The result supports the above assumptions.

## Q11. Determine the level of $V_o$ for the gate of Figure.



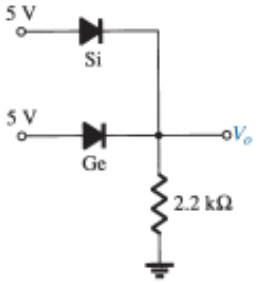

### Solution

Since all the system terminals are at 10 V the required difference of 0.7 V across either diode cannot be established. Therefore, both diodes are "off" and

$V_o = \mathbf{+10\text{ V}}$

as established by 10 V supply connected to 1 kΩ resistor.

## Q12. Determine Vo for the configuration of Figure.



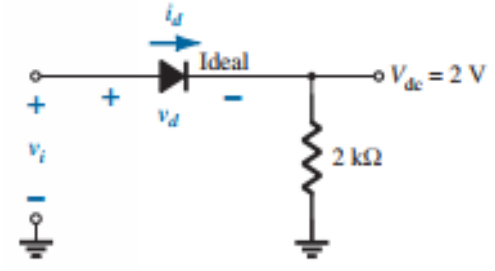

### Solution

The Si diode requires more terminal voltage than the Ge diode to turn "on". Therefore, with 5 V at both input terminals, assume Si diode "off" and Ge diode "on".

The result: $V_o = 5\text{ V} - 0.3\text{ V} = \mathbf{4.7\text{ V}}$

The result supports the above assumptions.

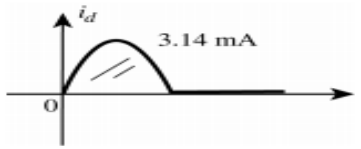
**Q13.** Assuming an ideal diode, sketch $v_i$, $v_d$, and $i_d$ for the half-wave rectifier of Figure. The input is a sinusoidal waveform with a frequency of 60 Hz. Determine the profit value of $v_i$ from the given dc level.




## Solution

$$V_{dc} = 0.318\ V_m \Rightarrow V_m = \frac{V_{dc}}{0.318} = \frac{2\text{ V}}{0.318} = \mathbf{6.28\ V}$$


$$I_m = \frac{V_m}{R} = \frac{6.28\text{ V}}{2\text{ k}\Omega} = \mathbf{3.14\ mA}$$



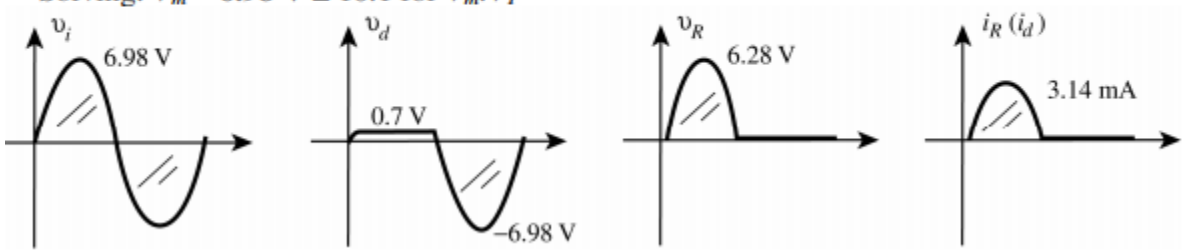

**Q14.** Repeat Problem 13 with a silicon diode ($V_K = 0.7$ V).

## Solution

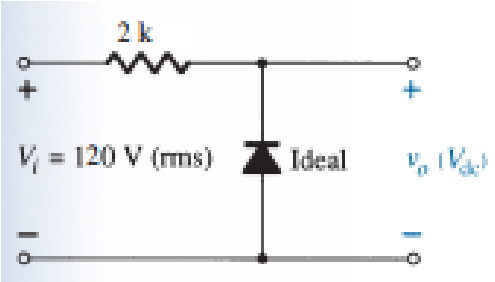
Using $V_{dc} \cong 0.318(V_m - V_T)$

$2\text{ V} = 0.318(V_m - 0.7\text{ V})$

Solving: $V_m = \mathbf{6.98\ V} \cong 10{:}1$ for $V_m{:}V_T$



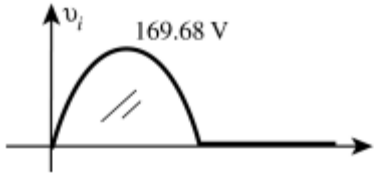
## Q15. For the network of Figure, sketch $v_o$ and determine $V_{dc}$.



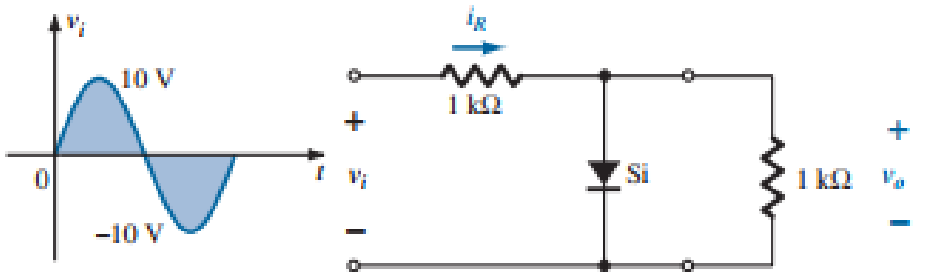

## Solution

$V_m = \sqrt{2}\,(120\text{ V}) = 169.68\text{ V}$

$V_{dc} = 0.318V_m = 0.318(169.68\text{ V}) = \mathbf{53.96\text{ V}}$




## Q16. For the network of Figure, sketch $v_o$ and $i_R$.




## Solution

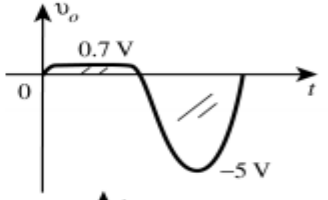
Diode will conduct when $v_o = 0.7$ V; that is,

$$v_o = 0.7\text{ V} = \frac{1\text{ k}\Omega(v_i)}{1\text{ k}\Omega + 1\text{ k}\Omega}$$

Solving: $v_i = \mathbf{1.4\text{ V}}$

For $v_i \geq 1.4$ V Si diode is "on" and $v_o = \mathbf{0.7\text{ V}}$.
For $v_i < 1.4$ V Si diode is open and level of $v_o$ is determined by voltage divider rule:

$$v_o = \frac{1\text{ k}\Omega(v_i)}{1\text{ k}\Omega + 1\text{ k}\Omega} = 0.5\,v_i$$




For $v_i = -10$ V:

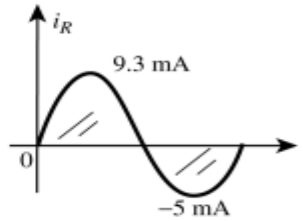
$v_o = 0.5(-10\text{ V})$

$= \mathbf{-5\text{ V}}$

When $v_o = 0.7$ V, $v_{R_{max}} = v_{i_{max}} - 0.7\text{ V}$

$= 10\text{ V} - 0.7\text{ V} = 9.3\text{ V}$

$$I_{R_{max}} = \frac{9.3\text{ V}}{1\text{ k}\Omega} = 9.3\text{ mA}$$




$$I_{max}(\text{reverse}) = \frac{10\text{ V}}{1\text{ k}\Omega + 1\text{ k}\Omega} = \mathbf{0.5\text{ mA}}$$

**Q17.** A full-wave bridge rectifier with a 120-V rms sinusoidal input has a load resistor of 1 kΩ.

a. If silicon diodes are employed, what is the dc voltage available at the load?

b. Determine the required PIV rating of each diode.

c. Find the maximum current through each diode during conduction.

d. What is the required power rating of each diode?

## Solution

(a) $V_m = \sqrt{2}\,(120\text{ V}) = 169.7\text{ V}$

$V_{L_m} = V_{i_m} - 2V_D$

$= 169.7\text{ V} - 2(0.7\text{ V}) = 169.7\text{ V} - 1.4\text{ V}$

$= 168.3\text{ V}$

$V_{dc} = 0.636(168.3\text{ V}) = \mathbf{107.04\text{ V}}$

(b) $\text{PIV} = V_m(\text{load}) + V_D = 168.3\text{ V} + 0.7\text{ V} = \mathbf{169\text{ V}}$

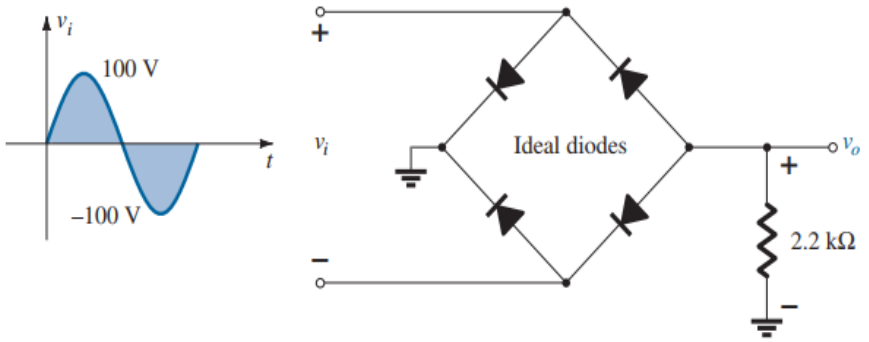
(c) $I_D(\text{max}) = \dfrac{V_{L_m}}{R_L} = \dfrac{168.3\text{ V}}{1\text{ k}\Omega} = \mathbf{168.3\text{ mA}}$

(d) $P_{max} = V_D I_D = (0.7\text{ V})I_{max}$

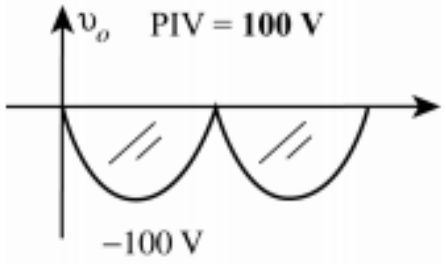
$= (0.7\text{ V})(168.3\text{ mA})$

$= \mathbf{117.81\text{ mW}}$

**Q18.** Draw Determine $V_0$ and the required PIV for the configuration of Figure. In addition, determine the maximum current through each diode.




## Solution




$I_{max} = \dfrac{100\text{ V}}{2.2\text{ k}\Omega} = \mathbf{45.45\text{ mA}}$

**Q19. What is the major difference between a bipolar and a unipolar device?**

A bipolar transistor utilizes holes and electrons in the injection or charge flow process, while unipolar devices utilize either electrons or holes, but not both, in the charge flow process.

**Q20. How must the two transistor junctions be biased for proper transistor amplifier operation?**

Forward- and reverse-biased.

**Q21. What is the source of the leakage current in a transistor?**

The leakage current $I_{co}$ is the minority carrier current in the collector.

**Q22. Which of the transistor currents is always the largest? Which is always the smallest? Which two currents are relatively close in magnitude?**

$I_E$ the largest
$I_B$ the smallest
$I_C \cong I_E$

**Q23. If the emitter current of a transistor is 8 mA and $I_B$ is 1/100 of $I_C$, determine the levels of $I_C$ and $I_B$.**

**Solution**

$$I_B = \frac{1}{100} I_C \Rightarrow I_C = 100 I_B$$

$$I_E = I_C + I_B = 100 I_B + I_B = 101 I_B$$

$$I_B = \frac{I_E}{101} = \frac{8\text{ mA}}{101} = \mathbf{79.21\ \mu A}$$

$$I_C = 100 I_B = 100(79.21\ \mu\text{A}) = \mathbf{7.921\ mA}$$