جامعة بيرزيت

BIRZEIT UNIVERSITY

لن يستطيعوا كسر إرادتنا، كلنا غزة

OUR WILL IS UNBREAKABLE... WE ARE ALL GAZA

Faculty of Engineering and Technology

Department of Electrical and Computer Engineering

ENCS 2110

EXP 8 Pre-Lab: Introduction to QUARTUSII Software

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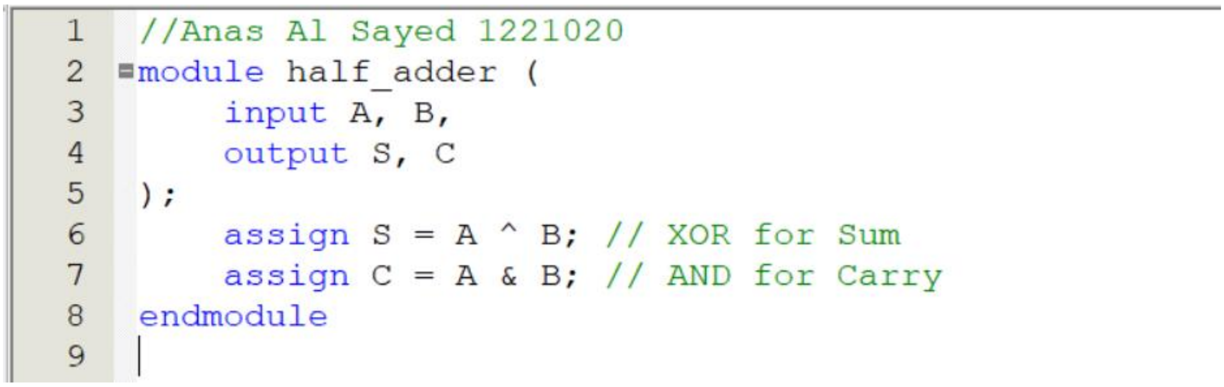
Section: 10

Instructor: Hanya Radwan

✓ **Half Adder (Data Flow)**

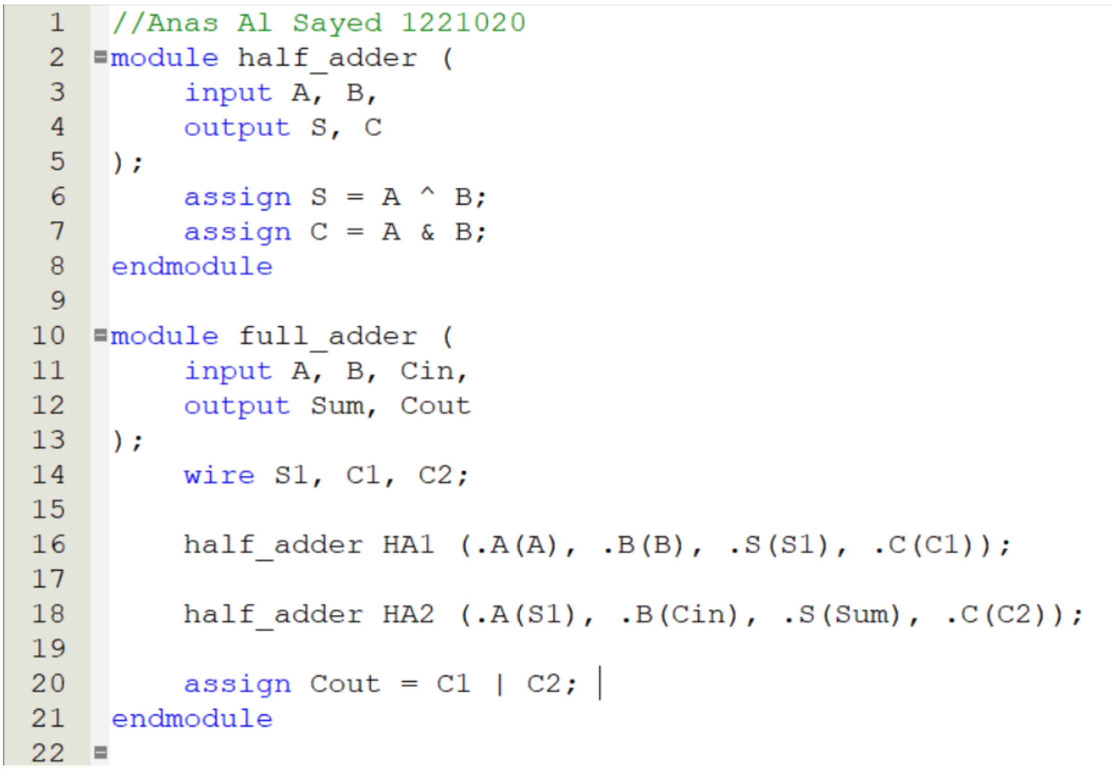
A **Half Adder** adds two bits and produces a **Sum (S)** and **Carry (C)**.



```
//Anas Al Sayed 1221020
module half_adder (
    input A, B,
    output S, C
);
    assign S = A ^ B; // XOR for Sum
    assign C = A & B; // AND for Carry
endmodule

```

✓ **Full Adder using Half Adder (Structural)**

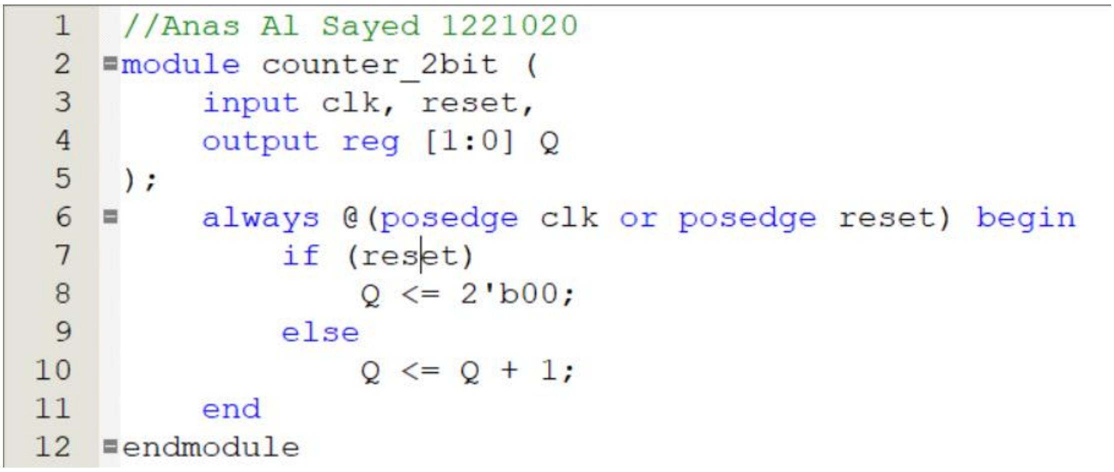
A Full Adder consists of two Half Adders and an OR gate.



```
//Anas Al Sayed 1221020
module half_adder (
    input A, B,
    output S, C
);
    assign S = A ^ B;
    assign C = A & B;
endmodule

module full_adder (
    input A, B, Cin,
    output Sum, Cout
);
    wire S1, C1, C2;

    half_adder HA1 (.A(A), .B(B), .S(S1), .C(C1));

    half_adder HA2 (.A(S1), .B(Cin), .S(Sum), .C(C2));

    assign Cout = C1 | C2;
endmodule

```

✓ **2-bit Counter (Behavioral)**

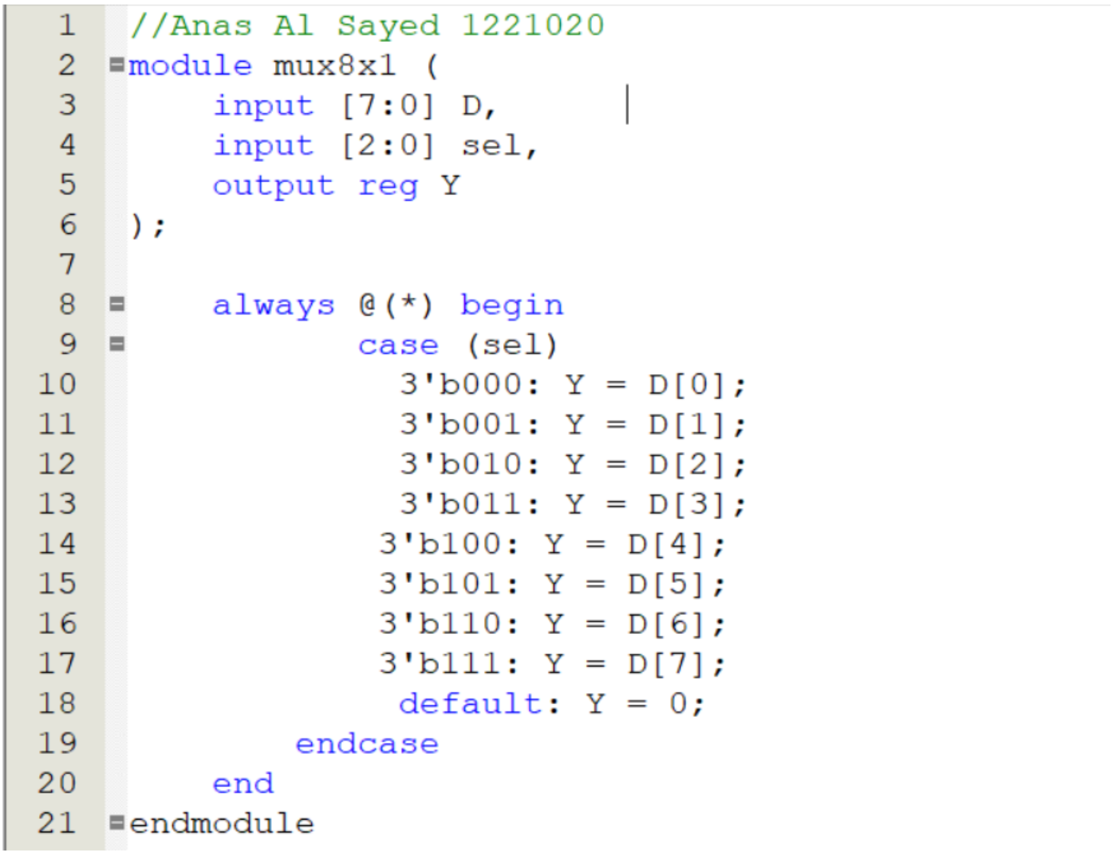
A 2-bit counter counts from 00 to 11 (0 to 3 in decimal).



```verilog
//Anas Al Sayed 1221020
module counter_2bit (
    input clk, reset,
    output reg [1:0] Q
);
    always @(posedge clk or posedge reset) begin
        if (reset)
            Q <= 2'b00;
        else
            Q <= Q + 1;
    end
endmodule
```

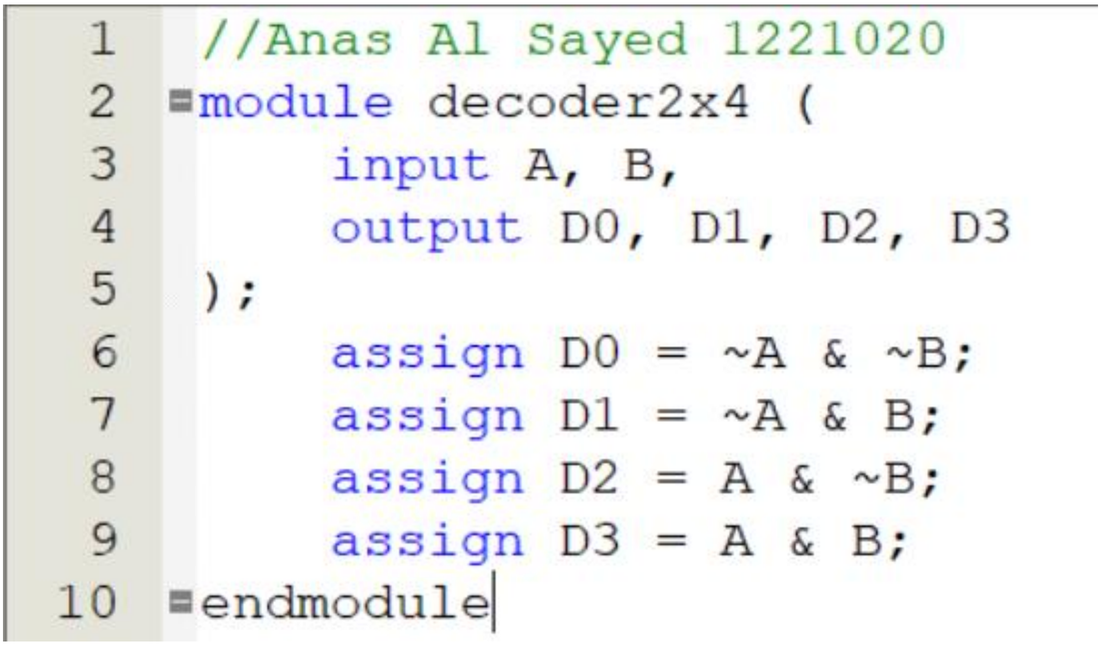
✓ **8-to-1 Multiplexer (Behavioral)**

An 8x1 MUX selects one of 8 inputs based on a 3-bit select line.



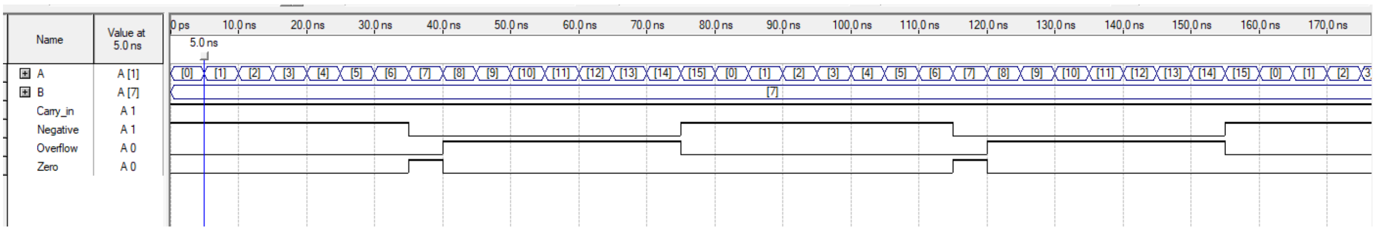
```verilog
//Anas Al Sayed 1221020
module mux8x1 (
    input [7:0] D,
    input [2:0] sel,
    output reg Y
);

    always @(*) begin
           case (sel)
             3'b000: Y = D[0];
             3'b001: Y = D[1];
             3'b010: Y = D[2];
             3'b011: Y = D[3];
            3'b100: Y = D[4];
            3'b101: Y = D[5];
            3'b110: Y = D[6];
            3'b111: Y = D[7];
             default: Y = 0;
        endcase
    end
endmodule
```

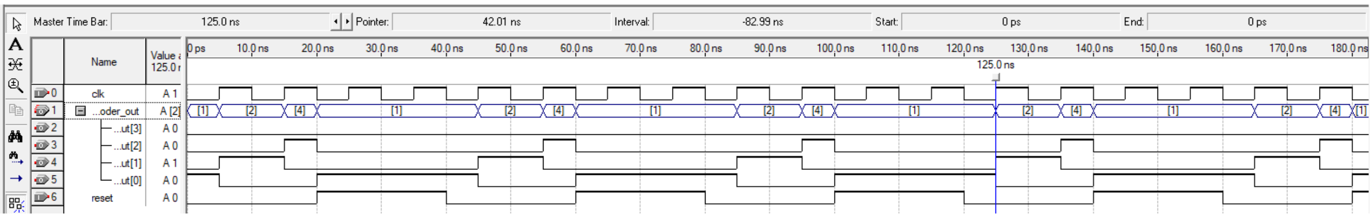
✓ **2x4 Decoder using Basic Gates (Structural)**
A 2x4 decoder takes 2 inputs and produces 4 outputs.



```verilog
//Anas Al Sayed 1221020
module decoder2x4 (
    input A, B,
    output D0, D1, D2, D3
);
    assign D0 = ~A & ~B;
    assign D1 = ~A & B;
    assign D2 = A & ~B;
    assign D3 = A & B;
endmodule
```

✓ **The waveform for the above parts.**

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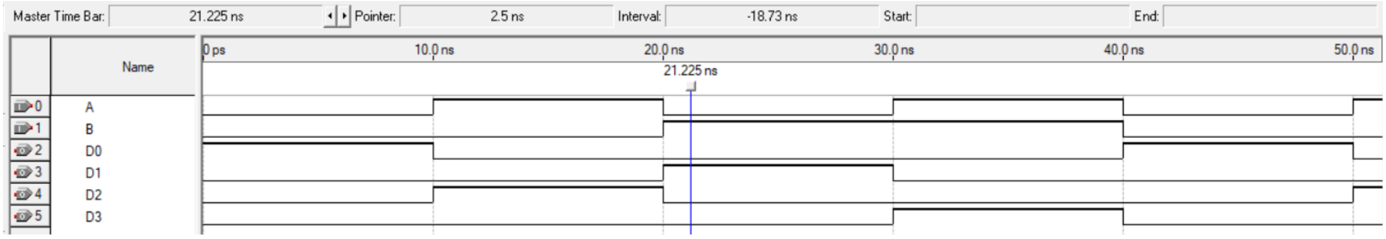
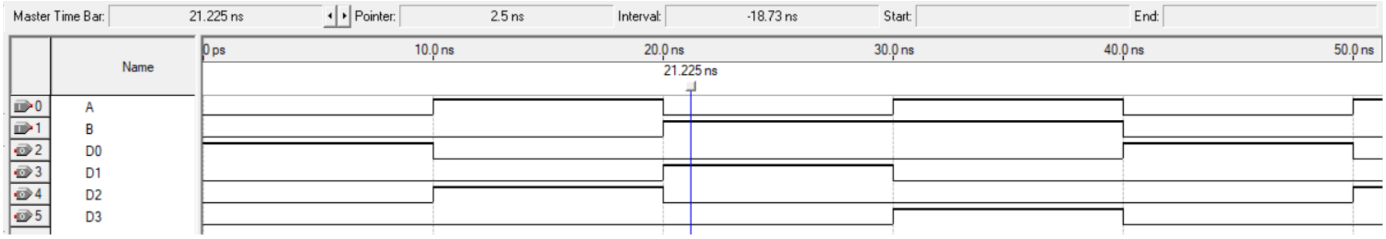

Master Time Bar: 21.225 ns Pointer: 2.5 ns Interval: -18.73 ns Start: End:


Master Time Bar: 21.225 ns Pointer: 2.5 ns Interval: -18.73 ns Start: End: