
**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

**ENCS 2110**

# EXP 5 Post-Lab: Sequential Logic Circuits

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✓ **Although latches are useful for storing binary information, they are rarely used in sequential circuit design, why?**

***Latches*** *are* ***level-triggered*** *devices, meaning they continuously respond to input changes as long as the enable* ***(****or clock****)*** *signal is active. This can cause timing issues like glitches or race conditions, especially in complex circuits.*
*In contrast****,*** ***flip-flops*** *are edge-triggered, meaning they only respond to inputs at the moment of a* ***clock edge*** *(rising or falling), making them more predictable and stable in synchronous designs.*

✓ **What is the disadvantage of the RS flip flop?**

*The* ***RS flip-flop (****Set-Reset flip-flop****)*** *has an undefined state when both Set* ***(S)*** *and Reset* ***(****R****)*** *inputs are high* ***(****1****)*** *at the same time.*
*In this condition, the outputs* ***Q*** *and* ***Q'*** *both go low, violating their expected behavior of being complements of each other.*

- *This creates uncertainty and can lead to circuit malfunction, which is why this condition must always be avoided.*

✓ **What is the difference between "synchronous" and "ripple" counters?**

***Synchronous counters:***
*All* ***flip-flops*** *are triggered by the same clock signal simultaneously. This results in faster and more predictable behavior, making them ideal for high-speed applications.*

***Ripple counters*** ***(****also called asynchronous counters****)****:*
*The clock* ***input*** *is given only to the* ***first flip-flop****, and the* ***output*** *of each* ***flip-flop*** *triggers the next one. This creates a* ***ripple*** *effect, causing propagation delays as the signal moves through each* ***flip-flop****.*

- *So,* ***synchronous*** *= faster and accurate.*
- ***Ripple*** *= simpler but slower due to delay.*