

**Faculty of Engineering and Technology**

**Department of Electrical and Computer Engineering**

**ENCS 2110**

**EXP 1 Post-Lab: Combinational Logic Circuits**

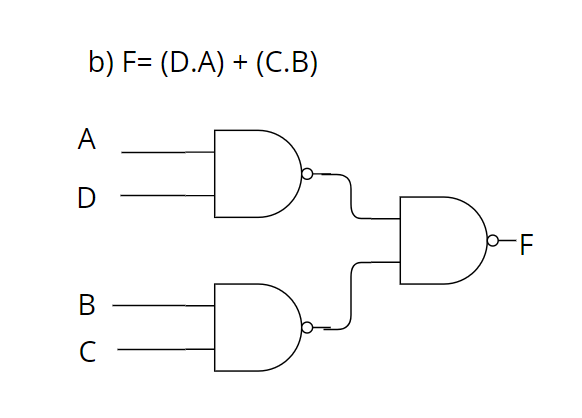
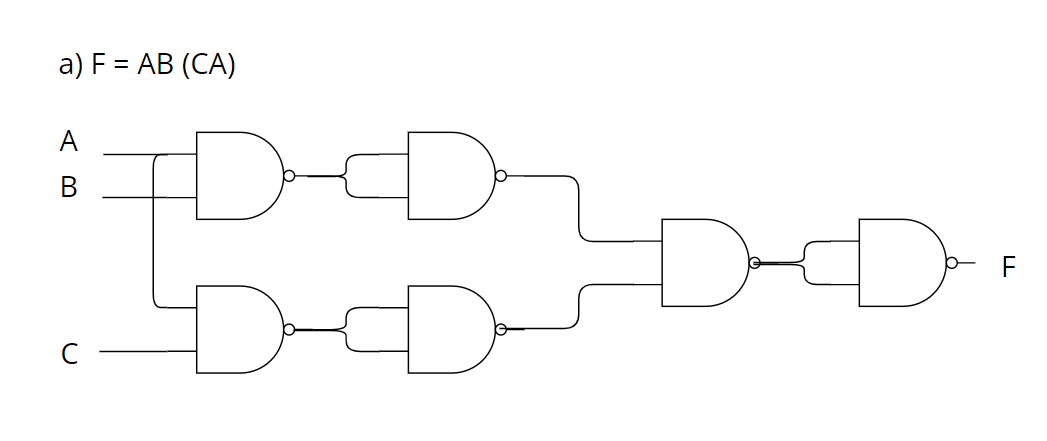
**Student’s name:** Anas Al Sayed

**Student’s No.:** 1221020

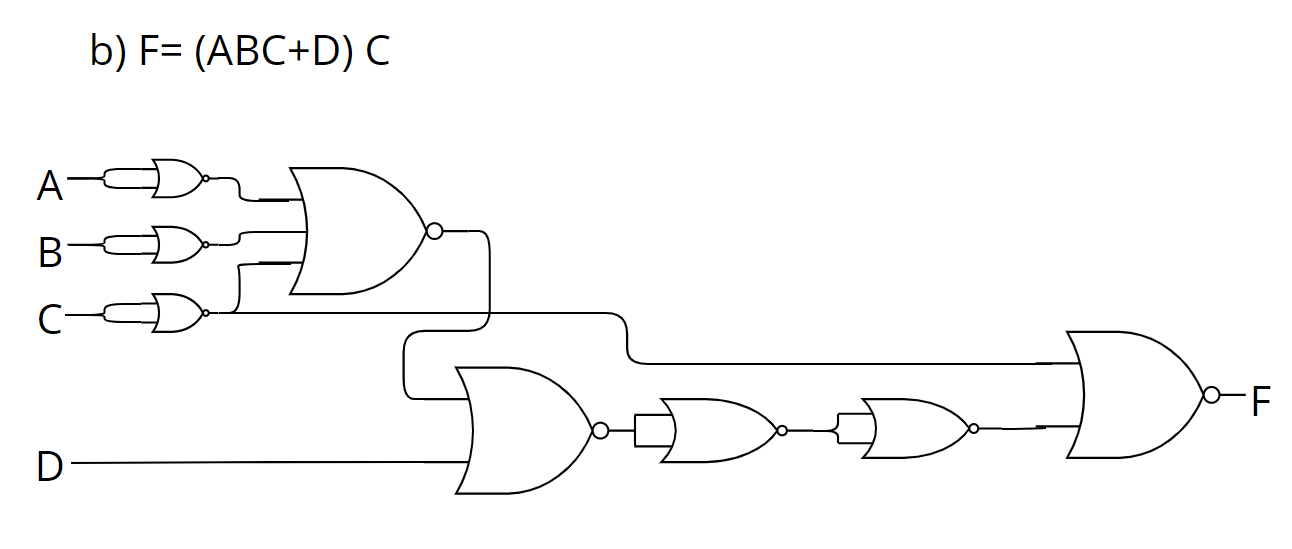
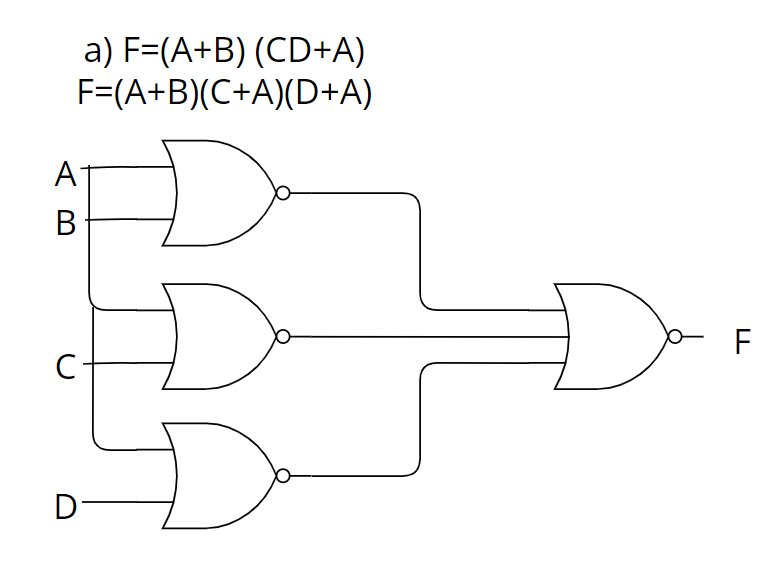
**Section:** 10

**Instructor:** Hanya Radwan

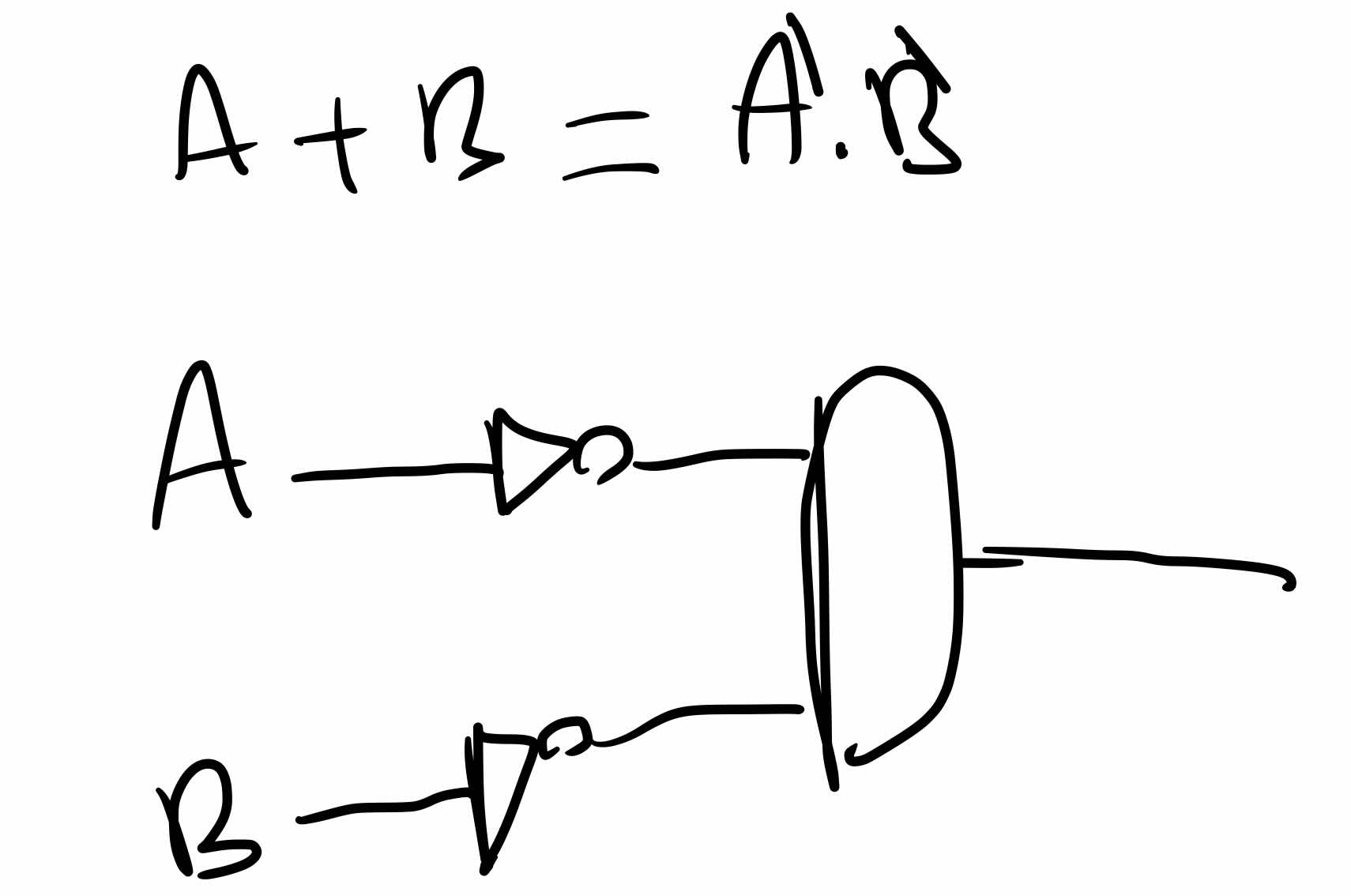
* **Draw the logic diagram showing the implementation of the following Boolean equation using “NAND” gates**



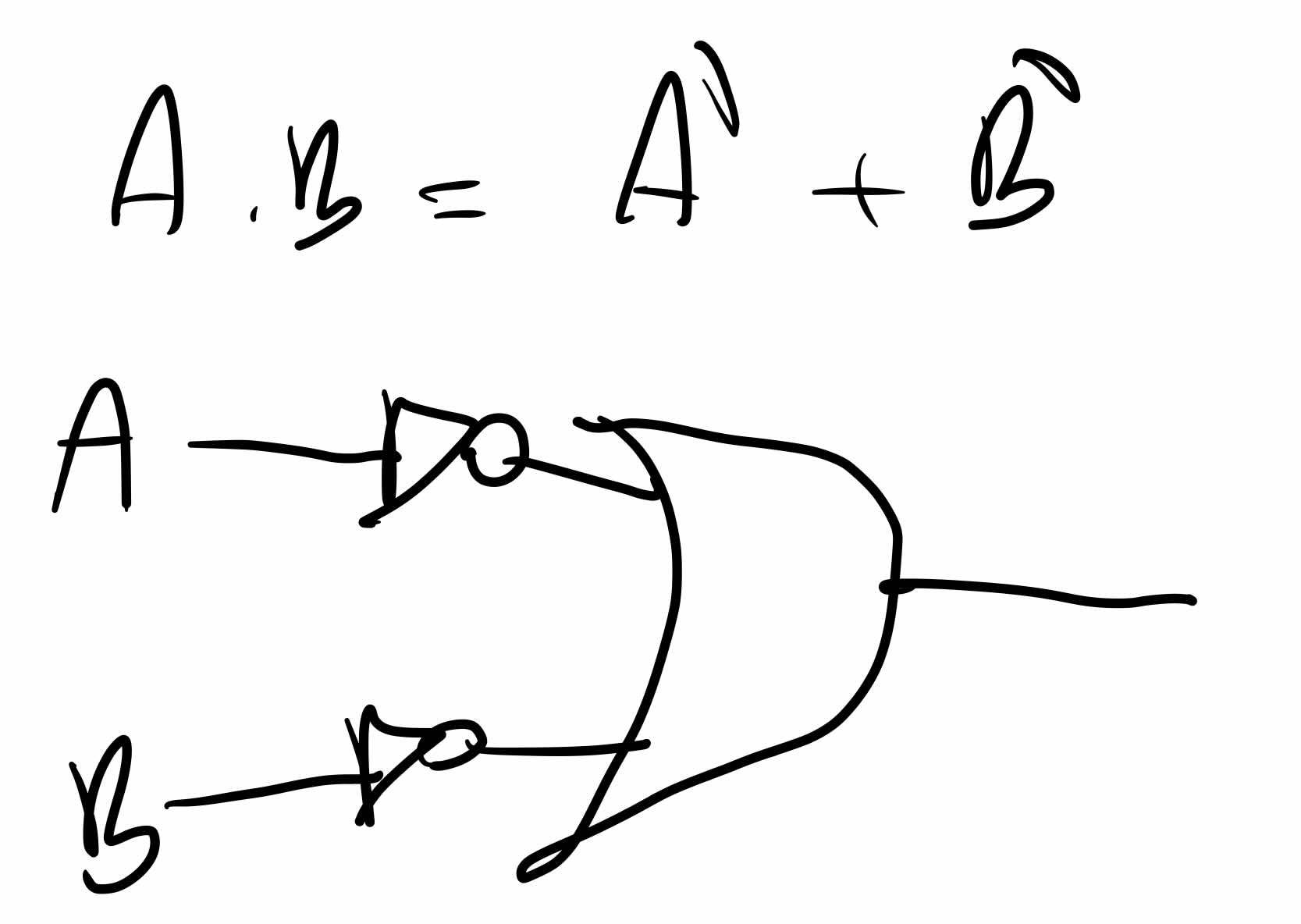
* **Draw the logic diagram of the following Boolean equations using NOR gates.**



* **Implement the OR operation using AND, NOT gate. Draw the logic diagram and write the Boolean equation.**



* **Implement the AND gate using OR, NOT gate. Draw the logic diagram and write the Boolean equation.**



* **Prove that the equality operation F1 =AB+A’B’ is the inverse of exclusive OR operation F2=AB’+A’B (use Demerger’s theorem).**

F1 = AB+A’B’

F1`=(A`+B`)(A+B)

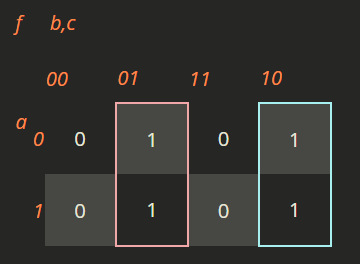
=A`A+A`B+B`A+B`B

=0+A`B+AB`+0

=AB` + A`B = F2

* **Show how is it possible to reduce Boolean expressions using the Karnaugh map:**

1. F1 = A’B’C + ABC’ + A’BC’ + AB’C



* ***F1 = B'C + BC'***

1. F2=A’D+A’C+BD+AB’D’



* ***F2 = A'D + A'C + AB'D' + BD***