Lab Project 2: Modeling, Simulation and Implementation of 4-bit Multiplier
University of Windsor
Department of Electrical and Computer Engineering
06-88-330: Digital Logic Design II, Fall 2016
Instructor: Dr. Mohammed Khalid
Due date: Wednesday, November 9, 2016

Using VHDL language, ALTERA Quartus II software and ALTERA DE2-115 board, you should design, simulate and implement a "4-bit Binary Multiplier" based on hardware friendly, modified shift and add algorithm. The detailed operation of this multiplier is described in Chapter 5 of the class notes that are posted online. Please refer to Figures 5.13 to 5.16. You have to create the VHDL model for the ASM chart for the 4-bit multiplier given in Figure 5-16. You have to then simulate the VHDL model using **given data sets (all of them)**. You must display the following signals in the simulation results timing diagram: *clk, Start, Reset, State, BC, C, PPS, MPD* and *MPR and Done*. The timing diagrams for the simulation results should be equivalent to the solution of Problem 5.5 posted on the course web site that is given as a table. You must also synthesize the VHDL model, download to FPGA and test your multiplier on the FPGA board. Use a push button on the DE2-115 FPGA to provide the *clk* input to the multiplier. The *A, B, Start* and *Reset* inputs should be controlled by toggle switches on the DE2-115 board. You must display the Done output on an LED and the result (product) as a **three digit decimal value on three seven segment displays on the FPGA board. You also need to show coded states on other LEDs.**

Hints:
- Declare libraries. Review how FSM VHDL model is implemented in VHDL class notes slides.
- Based on your VHDL coding style, you may face a situation where the model works in the simulator but not on FPGA. To resolve this problem, carefully review the suggestions provided in the document "Hints about VHDL modeling of State Machines…". This is posted on the course web site in the Lab Resources section.
- Name of entity must match project name, declare ports of black box within entity, Architecture is where you should declare signals, write processes using sensitivity list, and assign signals to corresponding ports.
- In the VHDL model, you will need to keep track of the states in the ASM chart (S0, S1, S2, S3) using two LEDs (00,01,10,11).
- The push button on the DE2-115 board is already debounced by circuit on the board.
- Read the DE2-115 manual to figure out what I/O pins you need to use for this Project.
- It is highly recommended that each group writes at least some of the VHDL code BEFORE coming to the lab. This will save significant amount of their time.

Data Sets:
A=0011, B=0010;
A=1011, B=0011;
A=0101, B=0111;
A=1110, B=1000;
A=1111, B=1111;

Marking:
GAs will check the results of simulation and functionality of design on the DE2-115 boards. Part marks will be given for all aspects.
35 percent for working simulation
35 percent for working implementation
30 percent individual oral questions
Do not share your VHDL code with any person other than your group member(s). Any copying of VHDL code from other groups or from the Internet will result in zero points for one or both parties (those who copy and those who allow their code to be copied). More severe penalties may also apply. You can discuss this lab project with GAs during GA office hours. Late submissions will be penalized. No late submissions will be accepted after one week from the due date.