Lab Project 1
University of Windsor
Department of Electrical and Computer Engineering
06-88-330: Digital Logic Design II, Fall 2016
Instructor: Dr. Mohammed Khalid
Due date: Wednesday, October 19, 2016

Using VHDL language, ALTERA Quartus II software and ALTERA DE2-115 board, you should design, simulate and implement a "2-Digit up/down BCD seconds counter with reset button" circuit. The counter value must be automatically incremented/decremented once every second (slow down the clock to 1 Hz). The up counting or down counting is determined by the status of a push button on DE2-115 board (e.g. PUSHBUTTON[0]). If the push button is pressed, the counter should count down and vice versa. In the up counting mode, if the counter reaches "59", the counter should go to "00" upon the next count. Similarly, in the down counting mode, when the counter reaches "00", it should go back to "59" upon the next count. The output of this circuit must be displayed in BCD digit format on the 7-segment display unit of DE2-115 board (SEVEN SEGMENT Display). Use two of the digits on 7-segment to display the counter value. The Reset will be determined by the other push button (e.g. PUSHBUTTON[1]). If the push button is pressed the counter should stop and the 7-segment display should reset to display "00". When button is released, the counter will start counting. In this design you have to utilize the onboard oscillator as the source for clock signal (refer to "DE2-115 Board User Manual" to learn more about this signal).

Hints:
-This is a sequential logic circuit, where you must keep track of what state you are in.
-Declare libraries.
-Name of entity must match project name, declare ports of black box within entity, Architecture is where you should declare signals, write processes using sensitivity list, and assign signals to corresponding ports.
-You need to divide down the clock frequency from 50 MHz to 1 Hz. The VHDL code that divides the clock will be provided to you. You need to integrate it into your own code.
-The push button on the DE2-115 board is already de-bounced by circuit on the board.
-Read the DE2-115 manual to figure out what I/O pins you need to use for this Project.
-It is highly recommended that each group writes at least some of the VHDL code BEFORE coming to the lab. This will save significant amount of their time.

Marking:
GAs will check the results of simulation and functionality of design on the DE2 boards. Part marks will be given for all aspects.
35 percent for working simulation
35 percent for working implementation
30 percent individual oral questions
Note that you must send the GAs your VHDL code before asking GAs to grade your simulation and implementation. Late submissions will not be accepted.