AL422 Data Sheets

(Revision V1.1)

Amendments (Since April 2, 1999)

05-13-99 DC/AC characteristics (including current consumption) updated.

07-02-99 Pinout diagram (5.0) and DC external load (7.4) modified.

08-03-99 Description about TST pin added in sections 6.0 & 8.1.

09-02-99 8.3.2 rewritten.

10-26-99 Capacitance provided in the AC characteristics section.

12-15-99 Remove TST pin restriction.

01-18-01

1. Revised section “8.3.2 Read Enable during Reset Cycles” to “8.3.2 The Proper Manipulation of FIFO Access”.
2. Add section “8.3.3 Single Field Write with Multiple Read Operation”
3. Add section “8.3.4 One Field Delay Line (The Old Data Read)”

AL422 3M-Bits FIFO Field Memory

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1.0 Description

The AL422 consists of 3M-bits of DRAM, and is configured as 393,216 words x 8 bit FIFO (first in first out). The interface is very user-friendly since all complicated DRAM operations are already managed by the internal DRAM controller.

Current sources of similar memory (field memory) in the market provide limited memory size which is only enough for holding one TV field, but not enough to hold a whole PC video frame which normally contains 640x480 or 720x480 bytes. The AverLogic AL422 provides 50% more memory to support high resolution for digital PC graphics or video applications. The 50% increase in speed also expands the range of applications.

2.0 Features

- 384K (393,216) x 8 bits FIFO organization
- Support VGA, CCIR, NTSC, PAL and HDTV resolutions
- Independent read/write operations (different I/O data rates acceptable)
- High speed asynchronous serial access
- Read/write cycle time: 20ns
- Access time: 15ns
- Output enable control (data skipping)
- Self refresh
- 5V or 3.3V power supply
- Standard 28-pin SOP package

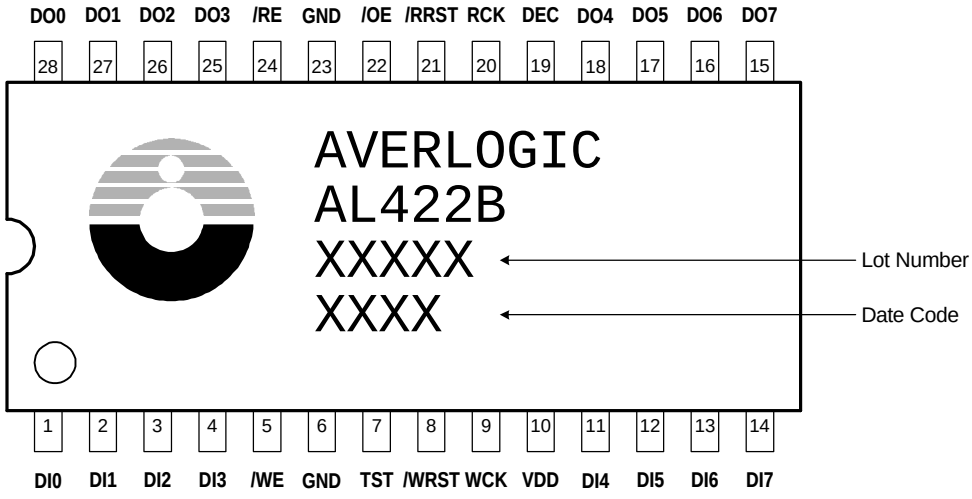
3.0 Applications

- Multimedia systems
- Video capture systems
- Video editing systems
- Scan rate converters
- TV's picture in picture feature
- Time base correction (TBC)
- Frame synchronizer
- Digital video camera
- Buffer for communications systems

4.0 Ordering Information

Part number	Package	Power Supply	Status
AL422B	28-pin plastic SOP	+5/+3.3 volt	Shipping
AL422V5	28-pin plastic SOP	+5 volt	Replaced by AL422B
AL422V3	28-pin plastic SOP	+3.3 volt	Replaced by AL422B

5.0 Pinout Diagram



AL422-04 422B pinout diagram

6.0 Pin Description

Pin name	Pin #	I/O type	Function
DI0~DI7	1~4, 11~14	input	Data input
WCK	9	Input	Write clock
/WE	5	Input (active low)	Write enable
/WRST	8	Input (active low)	Write reset
DO0~DO7	15~18, 25~28	Output (tristate)	Data output
RCK	20	Input	Read clock
/RE	24	Input (active low)	Read enable
/RRST	21	Input (active low)	Read reset
/OE	22	Input (active low)	Output enable
TST	7	Input	Test pin (pulled-down)*
VDD	10		5V or 3.3V
DEC/VDD	19		Decoupling cap input
GND	6, 23		Ground

7.0 Electrical Characteristics

7.1 Absolute Maximum Ratings

Parameter		Ratings		Unit
		3.3V application	5V application	
V_{DD}	Supply Voltage	-1.0 ~ +4.5	-1.0 ~ +7.0	V
V_P	Pin Voltage	-1.0 ~ +5.5	-1.0 ~ V_{DD} +0.5	V
I_O	Output Current	-20 ~ +20	-20 ~ +20	mA
T_{AMB}	Ambient Op. Temperature	0 ~ +70	0 ~ +70	°C
T_{stg}	Storage temperature	-55 ~ +125	-55 ~ +125	°C

7.2 Recommended Operating Conditions

Parameter		3.3V application		5V application		Unit
		Min	Max	Min	Max	
V_{DD}	Supply Voltage	+3.0	+3.6	+4.5	+5.25	V
V_{IH}	High Level Input Voltage	+2.0	+5.5	+3.0	V_{DD} +0.5	V
V_{IL}	Low Level Input Voltage	-1.0	+0.8	-1.0	+0.8	V

7.3 DC Characteristics

(V_{DD} =5V or 3.3V, Vss=0V. T_{AMB} = 0 to 70°C)

Parameter		3.3V application			5V application			Unit
		Min	Typ	Max	Min	Typ	Max	
I_{DD}	Operating Current @20MHz	-	33	-	-	50	-	mA
I_{DD}	Operating Current @30MHz	-	45	-	-	66	-	mA
I_{DD}	Operating Current @40MHz	-	57	-	-	82	-	mA
I_{DD}	Operating Current @50MHz	-	68	-	-	97	-	mA
I_{DDS}	Standby Current	-	7	-	-	12	-	mA
V_{OH}	Hi-level Output Voltage	0.7V_{DD}	-	V_{DD}	+3.0	-	V_{DD}	V
V_{OL}	Lo-level Output Voltage	-	-	+0.4	-	-	+0.4	V
I_{LI}	Input Leakage Current	-10	-	+10	-10	-	+10	µA
I_{LO}	Output Leakage Current	-10	-	+10	-10	-	+10	µA

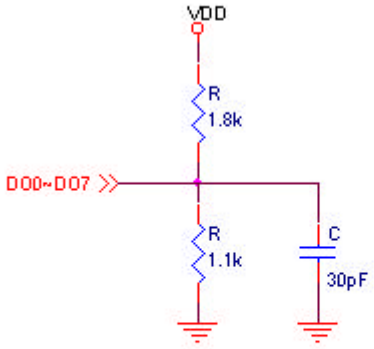
7.4 AC Characteristics

(V_{DD} =5V or 3.3V, Vss=0V, T_{AMB} = 0 to 70°C)

Parameter		3.3V application		5V application		Unit
		Min	Max	Min	Max	
T_{WC}	WCK Cycle Time	20	1000	20	1000	ns
T_{WPH}	WCK High Pulse Width	7	-	7	-	ns
T_{WPL}	WCK Low Pulse Width	7	-	7	-	ns
T_{RC}	RCK Cycle Time	20	1000	20	1000	ns
T_{RPH}	RCK High Pulse Width	7	-	7	-	ns
T_{RPL}	RCK Low Pulse Width	7	-	7	-	ns
T_{AC}	Access Time	-	15	-	15	ns
T_{OH}	Output Hold Time	4	-	4	-	ns
T_{HZ}	Output High-Z Setup Time	3	15	4	15	ns
T_{LZ}	Output Low-Z Setup Time	3	15	4	15	ns
T_{WRS}	/WRST Setup Time	5	-	6	-	ns
T_{WRH}	/WRST Hold Time	2	-	3	-	ns
T_{RRS}	/RRST Setup Time	5	-	6	-	ns
T_{RRH}	/RRST Hold Time	2	-	3	-	ns
T_{DS}	Input Data Setup Time	5	-	6	-	ns
T_{DH}	Input Data Hold Time	2	-	3	-	ns
T_{WES}	/WE Setup Time	5	-	6	-	ns
T_{WEH}	/WE Hold Time	2	-	3	-	ns
T_{WPW}	/WE Pulse Width	10	-	10	-	ns
T_{RES}	/RE Setup Time	5	-	6	-	ns
T_{REH}	/RE Hold Time	2	-	3	-	ns
T_{RPW}	/RE Pulse Width	10	-	10	-	ns
T_{OES}	/OE Setup Time	5	-	6	-	ns
T_{OEH}	/OE Hold Time	2	-	3	-	ns
T_{OPW}	/OE Pulse Width	10	-	10	-	ns
T_{TR}	Transition Time	2	20	3	20	ns
C_I	Input Capacitance	-	7	-	7	pF
C_O	Output Capacitance	-	7	-	7	pF

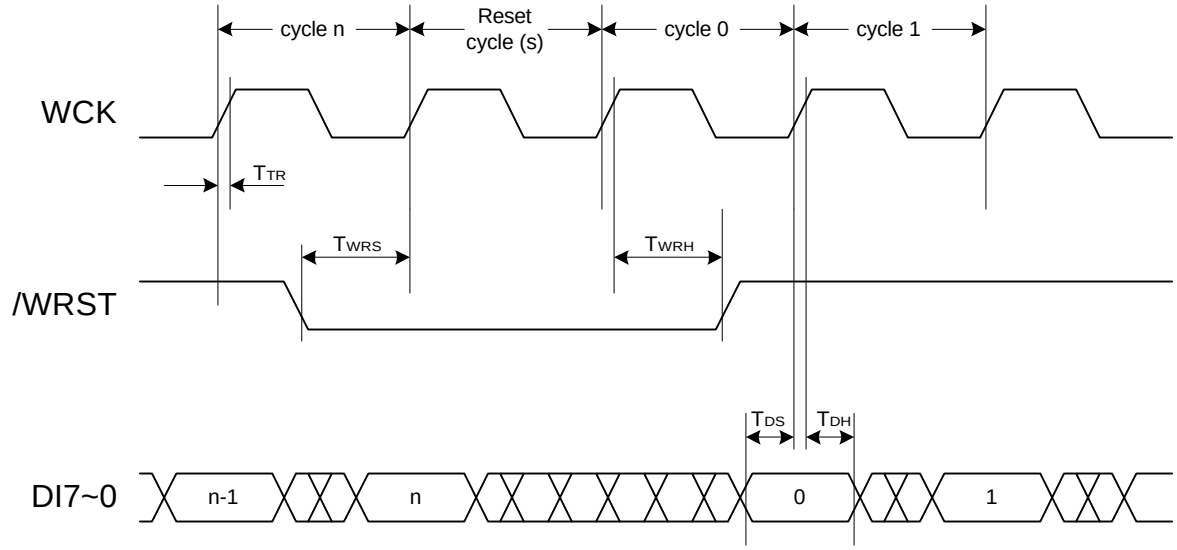
- Input voltage levels are defined as VIH=3.0V and VIL=0.4V.
- The read address needs to be at least 128 cycles after the write address.

DO external load:



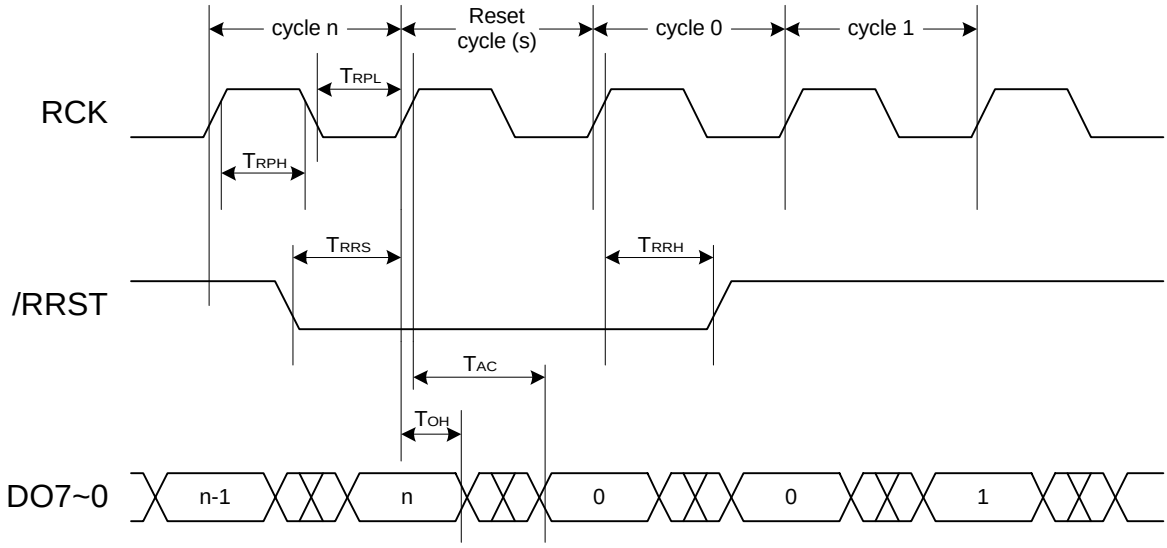
AL422-17 AL422 external load

7.5 Timing Diagrams



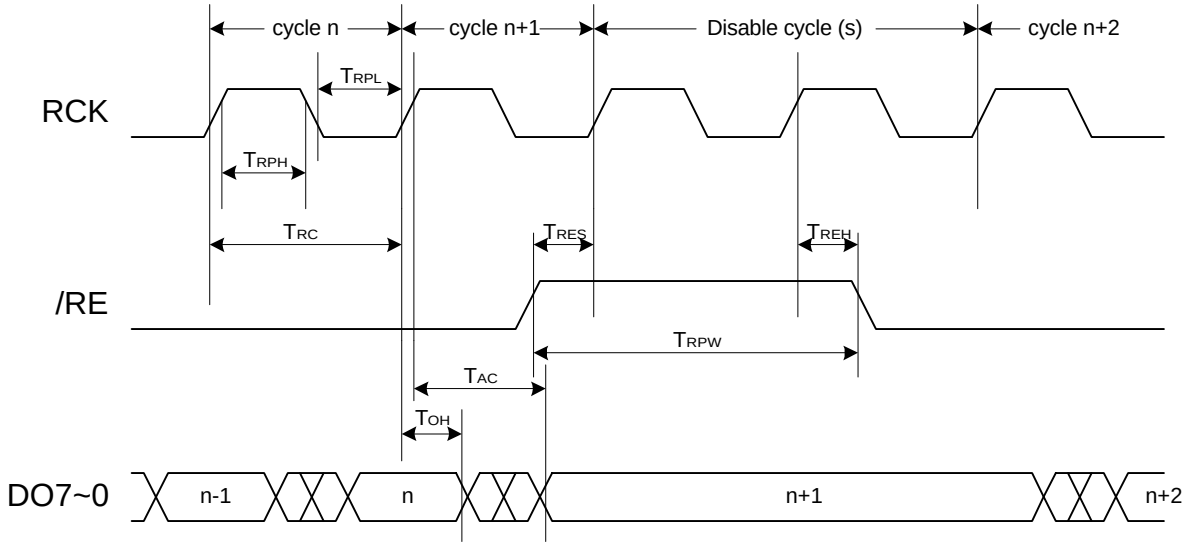
/WE = "L"

AL422-05 Write Cycle Timing (Write Reset)



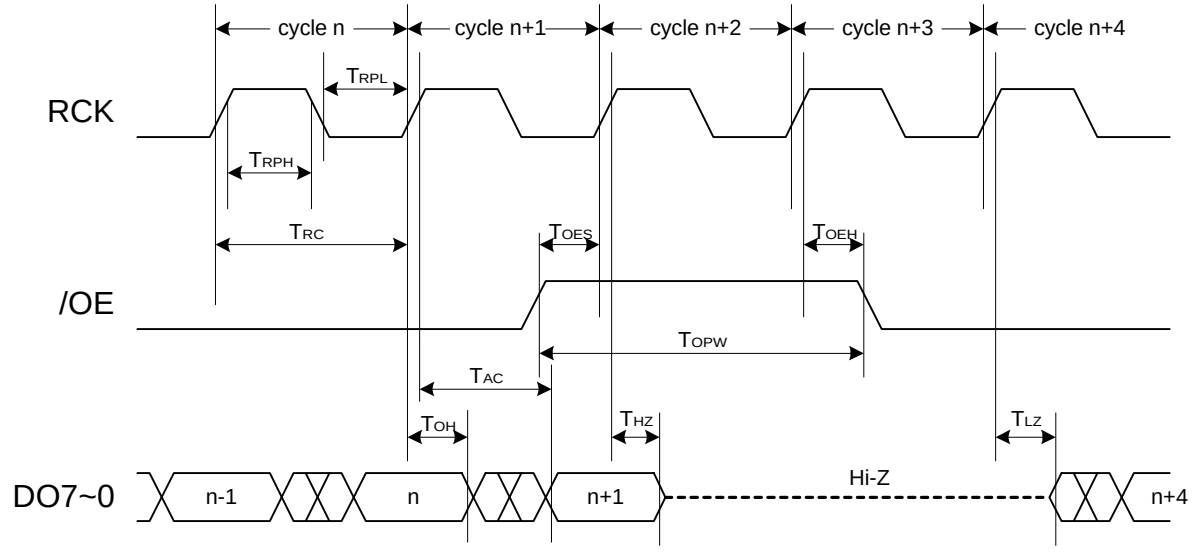
/RE = /OE = "L"

AL422-07 Read Cycle Timing (Read Reset)



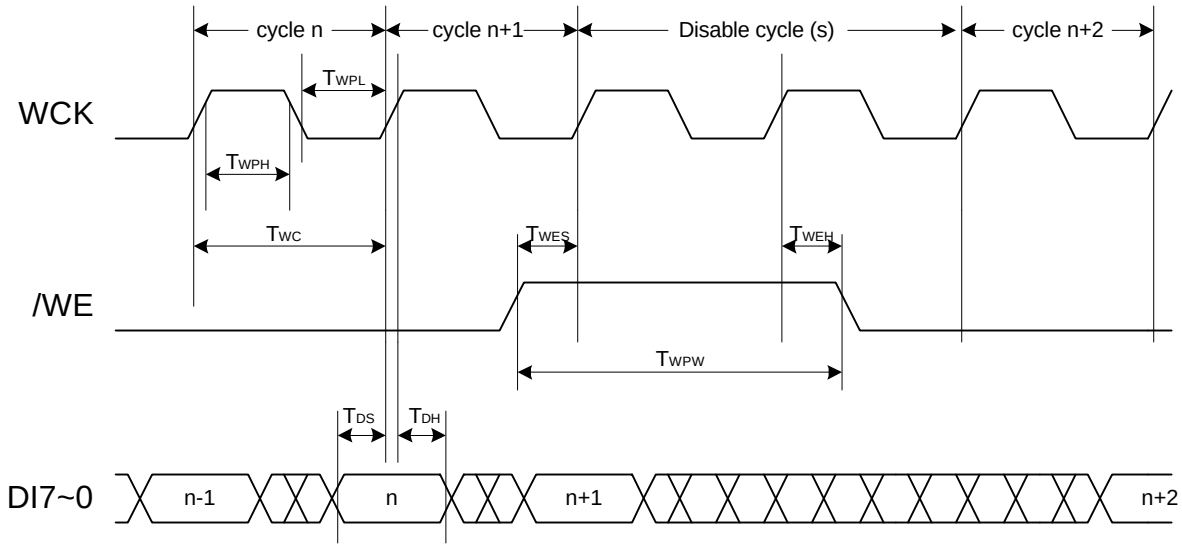
/OE = "L"

AL422-08 Read Cycle Timing (Read Enable)

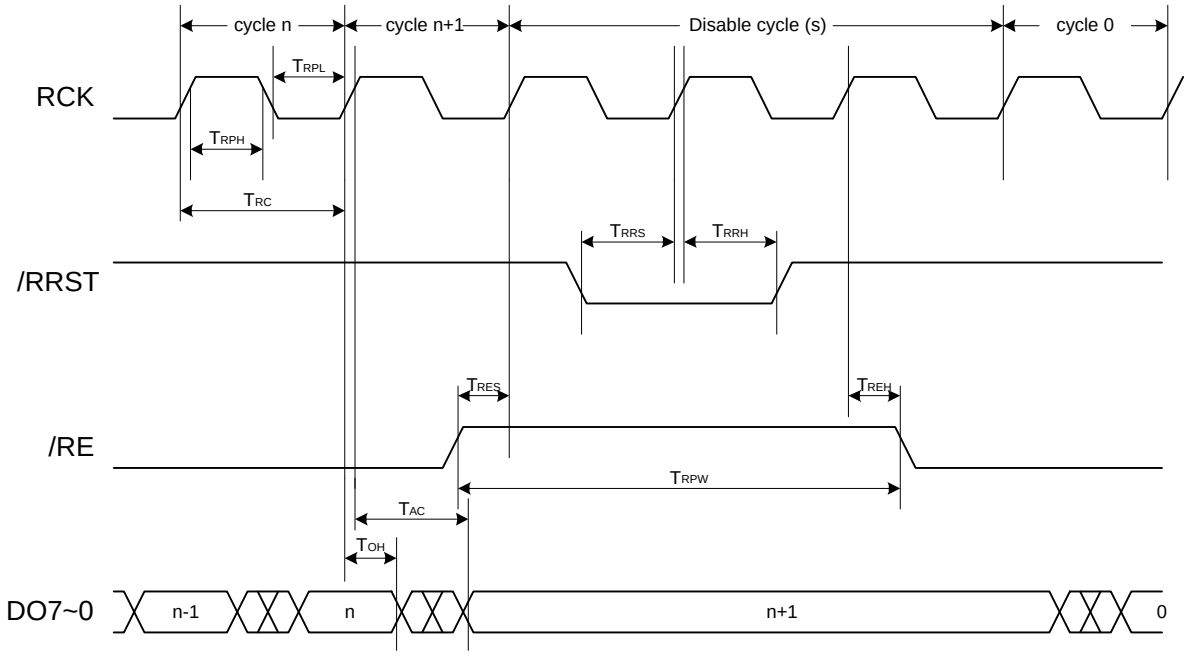


/RE = "L"

AL422-09 Read Cycle Timing (Output Enable)

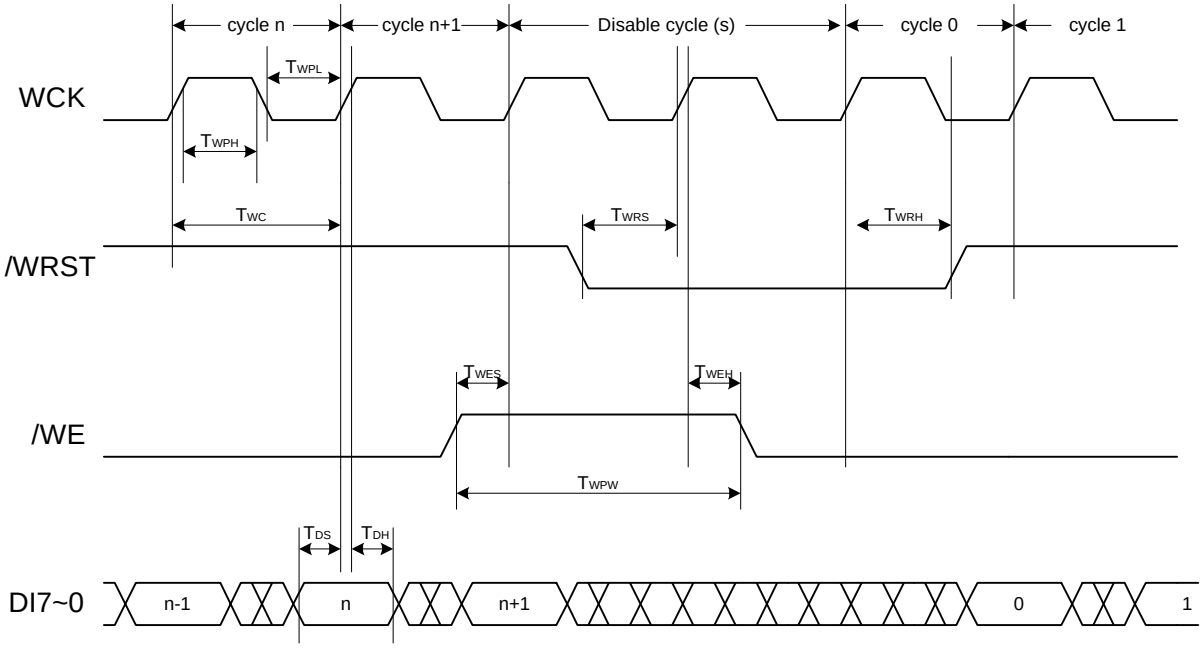


AL422-06 Write Cycle Timing (Write Enable)



/OE = "L"

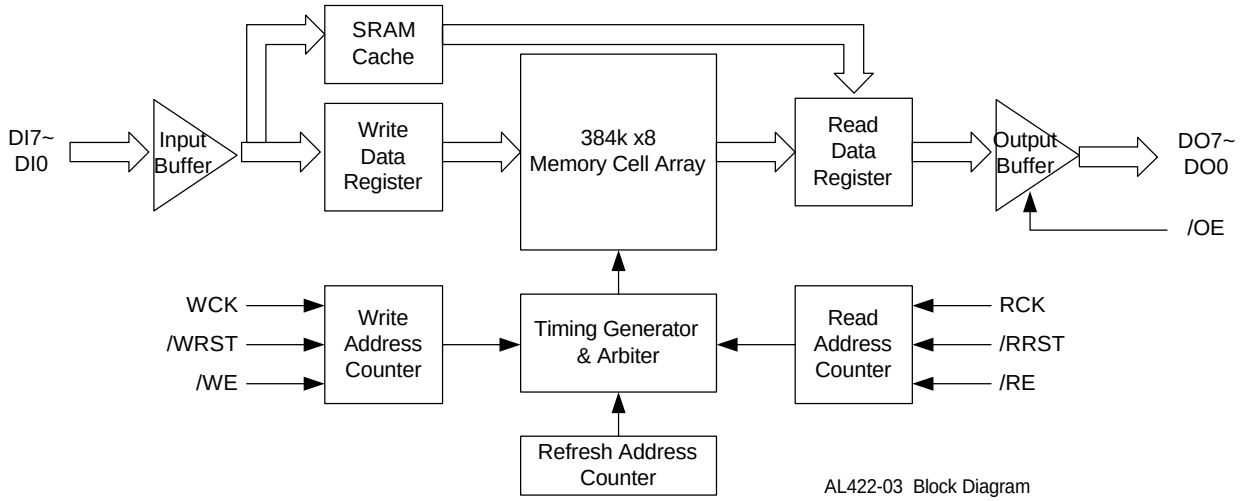
AL422-14 Read Cycle Timing (RE, RRST)



AL422-15 Write Cycle Timing (WE, WRST)

8.0 Functional Description

The AL422 is a video frame buffer consisting of DRAM that works like a FIFO which is long enough to hold up to 819x480 bytes of picture information and fast enough to operate at 50MHz. The functional block diagram is as follows:



AL422-03 Block Diagram

The I/O pinouts and functions are described as follows:

DI7~DI0 Data Input: Data is input on the rising edge of the cycle of WCK when /WE is pulled low (enabled).

DO7~DO0 Data Output: Data output is synchronized with the RCK clock. Data is obtained at the rising edge of the RCK clock when /RE is pulled low. The access time is defined from the rising edge of the RCK cycle.

WCK Write Clock Input: The write data input is synchronized with this clock. Write data is input at the rising edge of the WCK cycle when /WE is pulled low (enabled). The internal write address pointer is incremented automatically with this clock input.

RCK Read Clock Input: The read data output is synchronized with this clock. Read data output at the rising edge of the RCK cycle when /OE is pulled low (enabled). The internal read address pointer is incremented with this clock input.

/WE Write Enable Input: /WE controls the enabling/disabling of the data input. When /WE is pulled low, input data is acquired at the rising edge of the WCK cycle. When /WE is pulled high, the

memory does not accept data input. The write address pointer is stopped at the current position. /WE signal is fetched at the rising edge of the WCK cycle.

/RE Read Enable Input: /RE controls the operation of the data output. When /RE is pulled low, output data is provided at the rising edge of the RCK cycle and the internal read address is incremented automatically. /RE signal is fetched at the rising edge of the RCK cycle.

/OE Output Enable Input: /OE controls the enabling/disabling of the data output. When /OE is pulled low, output data is provided at the rising edge of the RCK cycle. When /OE is pulled high, data output is disabled and the output pins remain at high impedance status. /OE signal is fetched at the rising edge of RCK cycle.

/WRST Write Reset Input: This reset signal initializes the write address to 0, and is fetched at the rising edge of the WCK input cycle.

/RRST Write Reset Input: This reset signal initializes the read address to 0, and is fetched at the rising edge of the RCK input cycle.

TST Test Pin: For testing purpose only. It should be pulled low for normal applications.

DEC: Decoupling cap pin, should be connected to a 1μF or 2.2μF capacitor to ground for 5V application. For 3.3V application, the DEC pin can be simply connected to the 3.3V power with regular 0.1μF bypass capacitor.

8.1 Memory Operation

Initialization

Apply /WRST and /RRST 0.1ms after power on, then follow the following instructions for normal operation.

Reset Operation

The reset signal can be given at any time regardless of the /WE, /RE and /OE status, however, they still need to meet the setup time and hold time requirements with reference to the clock input. When the reset signal is provided during disabled cycles, the reset operation is not executed until cycles are enabled again. When /WRST signal is pulled low, the data input address will be set to 0 and the data in the Input Buffer will be flushed into memory cell array. When /RRST signal is pulled low, the data output address will be set to 0 and pre-fetch the data from memory cell array to Output Buffer.

Write Operation

Data input DI7~DI0 is written into the write register at the WCK input when /WE is pulled low. The write data should meet the setup time and hold time requirements with reference to the WCK input cycle.

Write operation is prohibited when /WE is pulled high, and the write address pointer is stopped at the current position. The write address starts from there when the /WE is pulled low again. The /WE signal needs to meet the setup time and hold time requirements with reference to the WCK input cycle.

Read Operation

Data output DO7~DO0 is written into the read register at the RCK input when both /RE and /OE are pulled low. The output data is ready after T_{AC} (access time) from the rising edge of the RCK input cycle.

The read address pointer is stopped at the current position when /RE is pulled high, and starts there when /RE is pulled low again.

/OE needs to be pulled low for read operations. When /OE is pulled high, the data outputs will be at high impedance stage. The read address pointer still increases synchronously with RCK regardless of the /OE status. The /RE and /OE signals need to meet the setup time and hold time requirements with reference to the RCK input cycle.

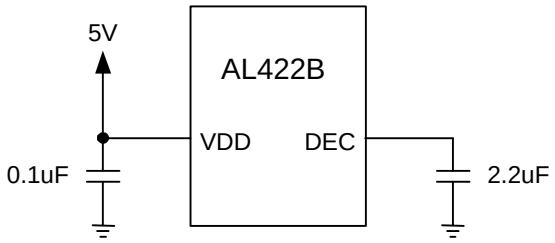
When the new data is read, the read address should be between 128 to 393,247 cycles after the write address, otherwise the output may not be new data.

8.2 5V and 3.3V applications

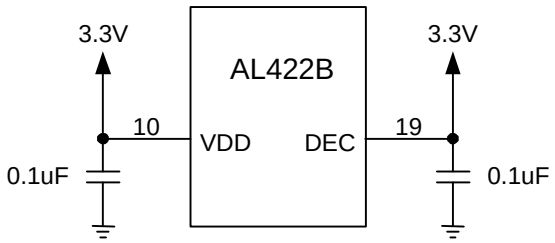
The AL422 can accept either 3.3V or 5V power with slightly different external configuration. The internal voltage regulator can convert 5V power to 3.3V for the embedded DRAM and logic circuitry when 5V power is applied to VDD pin (#10) only and leave the DEC pin (#19) decoupled by a capacitor of 1μF or 2.2μF to ground. The regulator can also be bypassed when 3.3V power is applied to both VDD and DEC pins. In either case the AL422 is 5V or 3.3V I/O tolerant. The 3.3V configuration consumes less power and is free from noise interference from the voltage regulator so may be more ideal for high-speed applications.

Please note that using the AL422B with 5V configuration can directly replace the previous AL422V5; using it with 3.3V configuration can directly replace the previous AL422V3. No additional modification is required.

The 5V configuration (direct replacement of the previous AL422V5) is as follows:



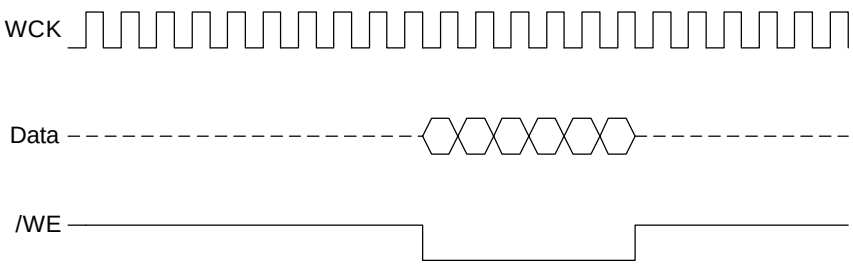
The 3.3V configuration (direct replacement of the previous AL422V3) is as follows:



8.3 Application Notes

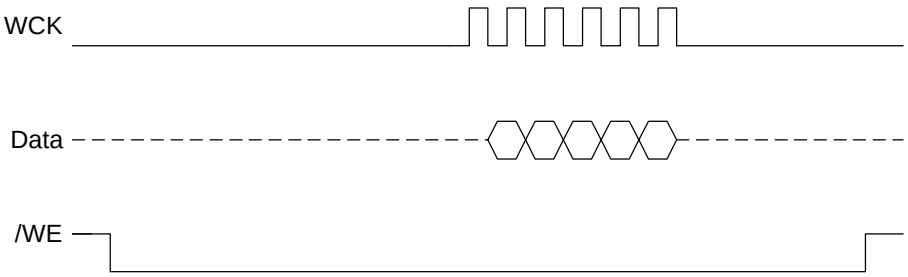
8.3.1 Irregular Read/Write

It is recommended that the WCK and RCK are kept running at least 1MHz at all times. The faster one of WCK and RCK is used as the DRAM refresh timing clock and has to be kept free running. When irregular FIFO I/O control is needed, keep the clock free running and use /WE or /RE to control the I/O as follows:



AL422-17 Slow Write - Correct

The following drawing shows irregular clock and should be avoided:



AL422-16 Slow Write - Incorrect

8.3.2 The Proper Manipulation of FIFO Access

The FIFO memory is designed to allow easy field delay, time-base conversion, and other types of signal processing. To ensure the expectant data can be read out from the AL422 FIFO, the proper manipulation on the AL422 FIFO memory is highly recommended

1. The read address should be between 128 to 393,247 cycles after the write address to read the current field data. (The restriction is indicated in the “Read Operation” Section).

2. The proper FIFO access must make sure after read reset, the read operation will either read all the old data (last field data) until next read reset, or follow the constraint 1 above to read newly update data. In any 2 read resets interval, the FIFO access can not read old data (the field data are written before last write reset), and stop for a period then read the newly update data (even at that time, write counter is ahead of read counter by more than 128 cycles).

If the FIFO memory manipulations violate the above conditions, some amount of consecutive unexpected data (old data) will be read at the FIFO data bus.

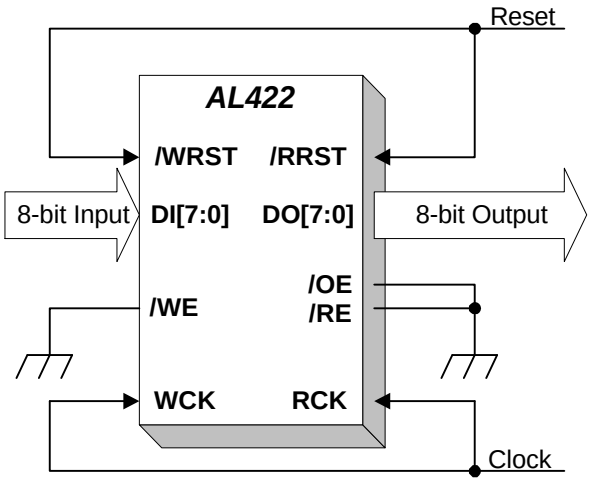
8.3.3 Single Field Write with Multiple Read Operation

It is one of the functions for FIFO memory that can buffer a field data and do multiple times of fields read access. In some applications, such as still image capturing, require one field write and multiple field data read operations. In order not to violate the 128 cycles of write to read delay latency rule, the write address (pointer) needs to be reset to 0 for the coming multiple read operations so that FIFO can provide the expectant data at DO bus.

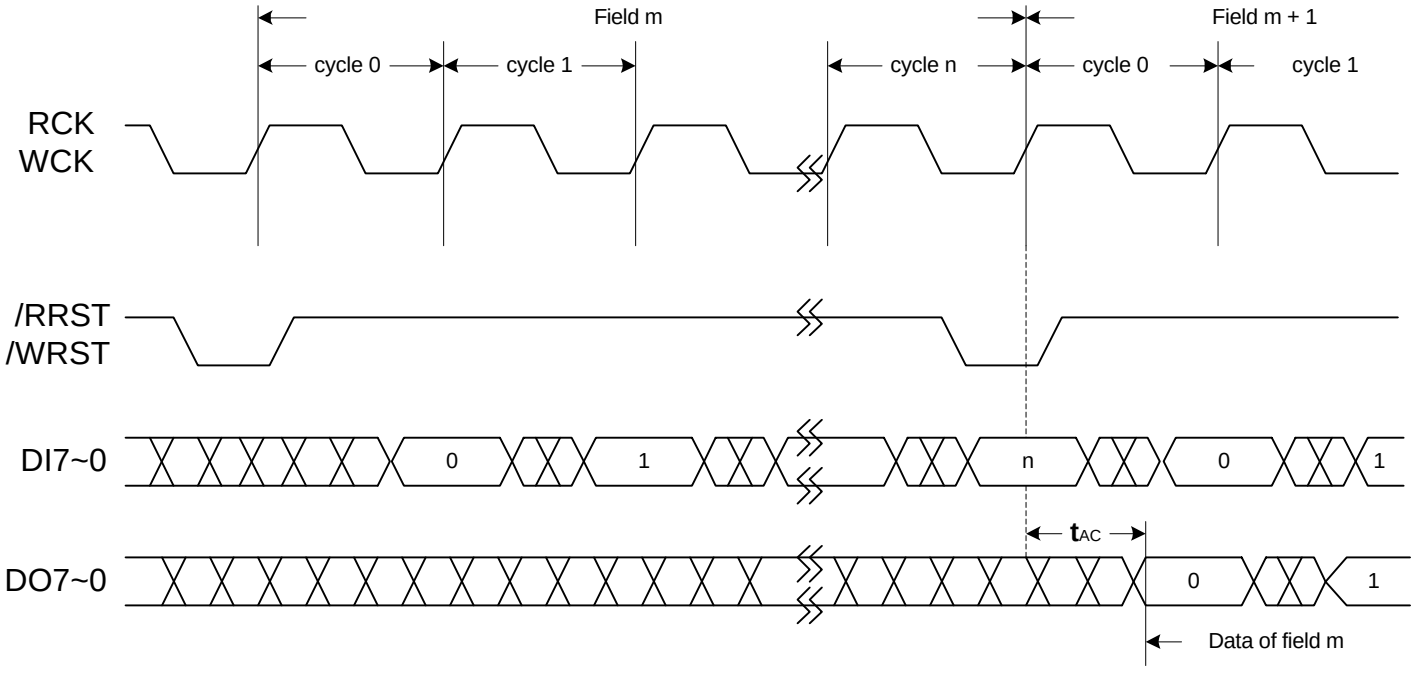
8.3.4 One Field Delay Line (The Old Data Read)

As the design shown in diagram by applying the reset every 1-field cycle (with the common signal for /WRST and /RRST) and a constant read/write operation (with all /WE, /RE and /OE are tied to ground), “1 field delay line” timing is shown in timing chart below. When the difference between the

write address and the read address is 0 (the read address and the write address are the same), the old field data are read as shown in the timing chart.



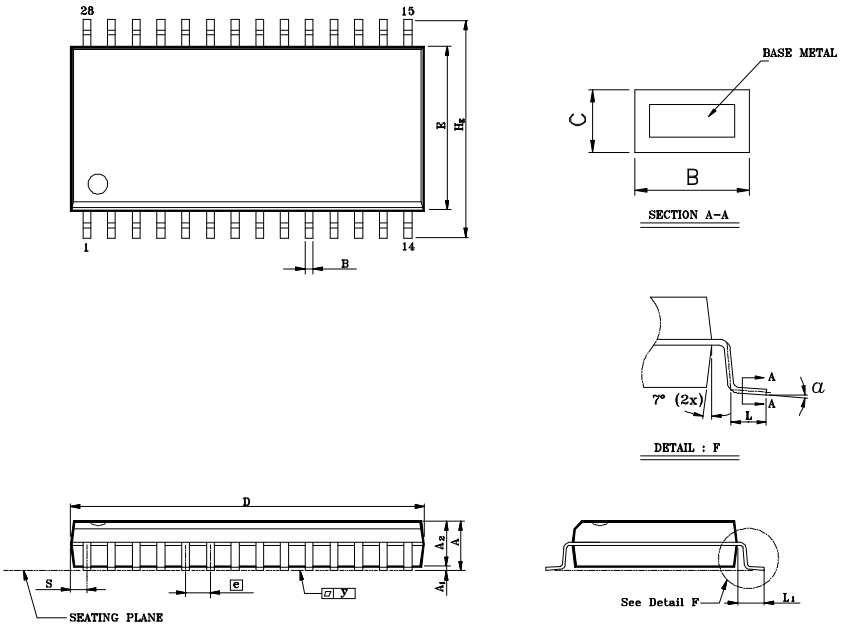
AL422 1 Field Delay Line Diagram



AL422-08 1 Field Delay Line Timing Diagram

9.0 Mechanical Drawing

28 PIN PLASTIC SOP:



Symbol	Dimension in inch			Dimension in mm		
	Min	Nom	Max	Min	Nom	Max
A	—	—	0.112	—	—	2.85
A_1	0.004	—	—	0.10	—	—
A_2	0.093	0.098	0.103	2.36	2.49	2.62
B	0.014	0.016	0.020	0.36	0.41	0.51
C	0.008	0.010	0.012	0.20	0.25	0.30
D	—	0.713	0.728	—	18.11	18.49
E	0.326	0.331	0.336	8.28	8.41	8.53
e	0.044	0.050	0.056	1.12	1.27	1.42
H	0.453	0.465	0.477	11.51	11.81	12.12
L	0.028	0.036	0.044	0.71	0.91	1.12
L_1	0.059	0.067	0.075	1.50	1.70	1.91
S	—	—	0.047	—	—	1.19
y	—	—	0.004	—	—	0.10
α	0°	—	8°	0°	—	8°

Note:
1. Dimension D Max. & s include mold flash or tie bar burrs
2. Dimension b does not include dambar protrusion/intrusion.
3. Dimension D & E include mold mismatch and determined at the mold parting line
4. Controlling dimension: Inch
5. General appearance spec should be based on final visual inspection spec.

REV NO	DESCRIPTION	DATE
B	1. Revise symbol letter per JEDEC definition. 2. Tighten tolerance of followine dimensions. Dimension / Was / Now C / 0.014" / 0.012" D / 0.733" / 0.728" α / 10° / 8°	Apr,07
B	1. Update form. 2. The effective decimal 0.xx instead of 0.xxx in the metric system.	Mar,22

TITLE: 28LD SOP (330 mil BODY) PACKAGE OUTLINE			
L/F MATERIAL: A194 F.H.		JEDEC CODE NO	MO-059
		ELAJ CODE NO	———
APPR.		DWG NO.	S028-SW2
R&D		REV NO.	C
Q.M		SCALE	
CHK.		DATE	June, 30, 98
DEN.		SHT NO.	1/1
AVERLOGIC TECHNOLOGIES, INC.			

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