Digital Logic Design

2-Bit Calculator

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Contents

Addition

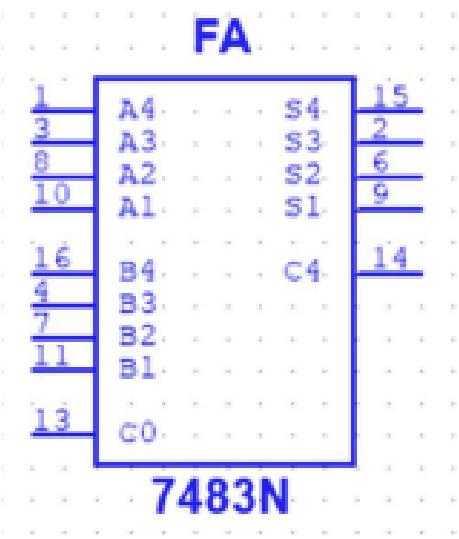
Truth Table:

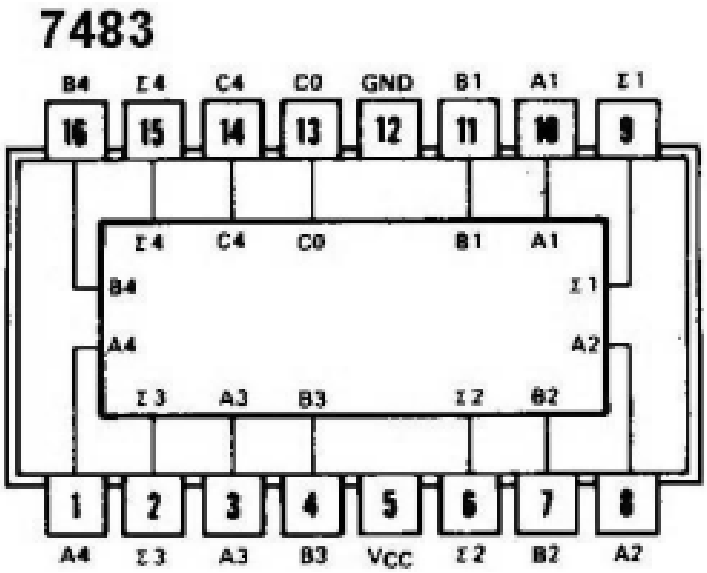
INPUTS						OUTPUTS				
A			B							
A1	A0	A_Dec.	B1	B0	B_Dec.	∑3	∑2	∑1	∑0	∑ Decimal
0	0	0	0	0	0	0	0	0	0	0
0	0		0	1	1	0	0	0	1	1
0	0		1	0	2	0	0	1	0	2
0	0		1	1	3	0	0	1	1	3
0	1	1	0	0	0	0	0	0	1	1
0	1		0	1	1	0	0	1	0	2
0	1		1	0	2	0	0	1	1	3
0	1		1	1	3	0	1	0	0	4
1	0	2	0	0	0	0	0	1	0	2
1	0		0	1	1	0	0	1	1	3
1	0		1	0	2	0	1	0	0	4
1	0		1	1	3	0	1	0	1	5
1	1	3	0	0	0	0	0	1	1	3
1	1		0	1	1	0	1	0	0	4
1	1		1	0	2	0	1	0	1	5
1	1		1	1	3	0	1	1	0	6

How it works:

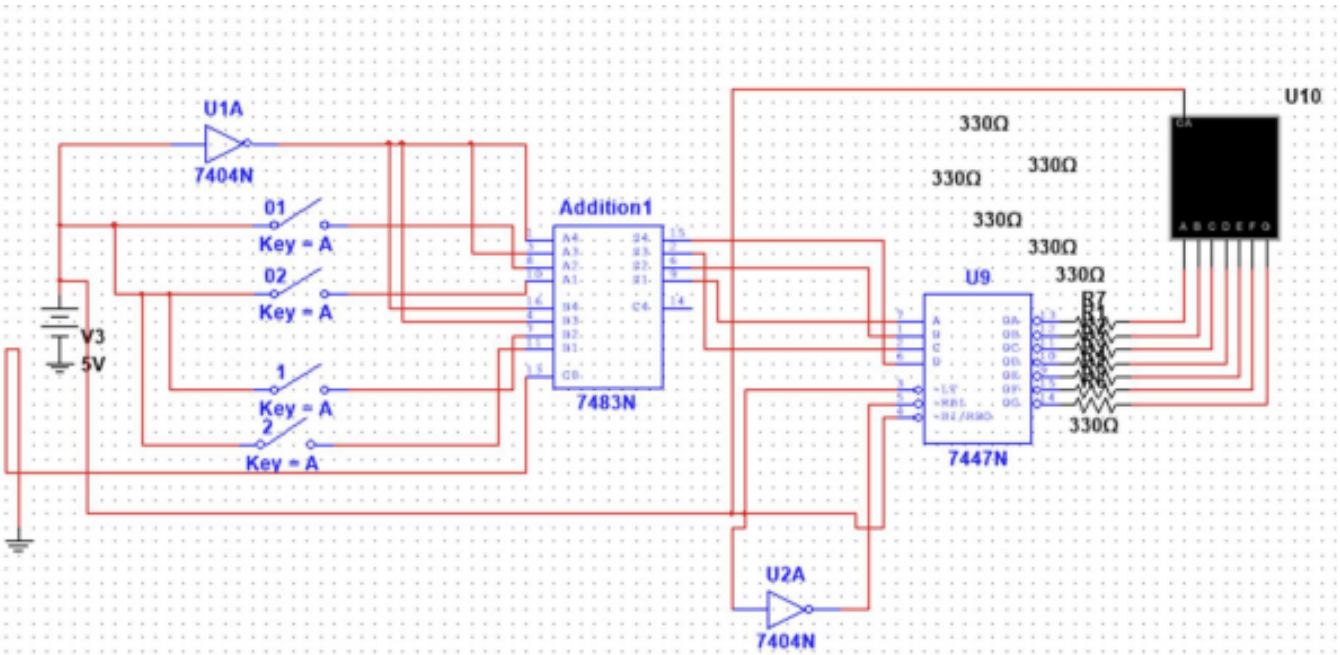
The addition operation was implemented using a full adder IC, the full adder IC facilitated the building of this operation as it has the built-in function of adding numbers in a single IC. The IC consists of a 4-bits parallel binary adder where the inputs of the IC are A1, A2, A3 and A4 for the number ‘A’ and B1, B2, B3 and B4 for the number ‘B’.

Full-Adder Diagram:





Circuit:



Subtraction

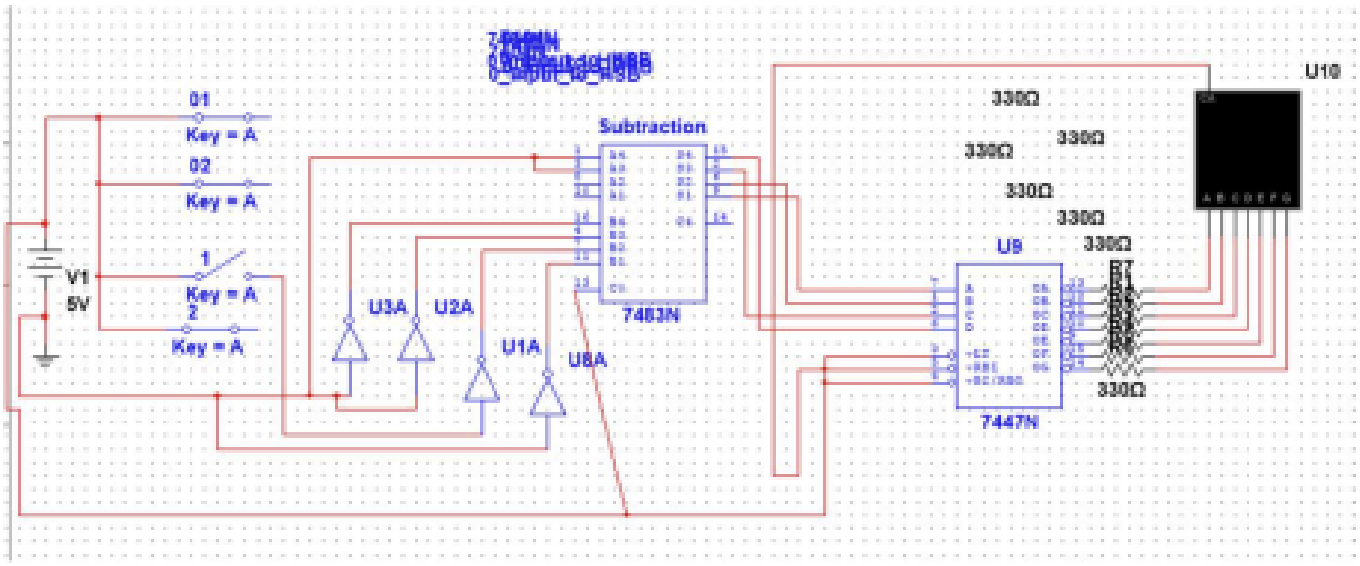
Truth Table:

INPUTS						OUTPUTS				
A			B							
A1	A0	A_Dec.	B1	B0	B_Dec.	D3	D2	D1	D0	D_Decimal
0	0	0	0	0	0	0	0	0	0	0
0	0		0	1	1	X	X	X	X	X
0	0		1	0	2	X	X	X	X	X
0	0		1	1	3	X	X	X	X	X
0	1	1	0	0	0	0	0	0	1	1
0	1		0	1	1	0	0	0	0	0
0	1		1	0	2	X	X	X	X	X
0	1		1	1	3	X	X	X	X	X
1	0	2	0	0	0	0	0	1	0	2
1	0		0	1	1	0	0	0	1	1
1	0		1	0	2	0	0	0	0	0
1	0		1	1	3	X	X	X	X	X
1	1	3	0	0	0	0	0	1	1	3
1	1		0	1	1	0	0	1	0	2
1	1		1	0	2	0	0	0	1	1
1	1		1	1	3	0	0	0	0	0

How it works:

The subtraction operation is very simple as it only occurs under one condition, when A is greater than or equal B; logical output is produced. It was also implemented using a 7483 full adder IC. However there have been some differences between the addition and subtraction operations. Firstly, the carry in in the subtraction always has a high signal unlike the addition that has a low carry in, moreover every binary bit in the number ‘B’ passes through a 7404 NOT gate to get the two’s complement of the number so that the operation later preforms as the addition of the bits of number ‘A’ and the two’s complement of the number ‘B’.

Circuit:



Multiplication

Truth Table:

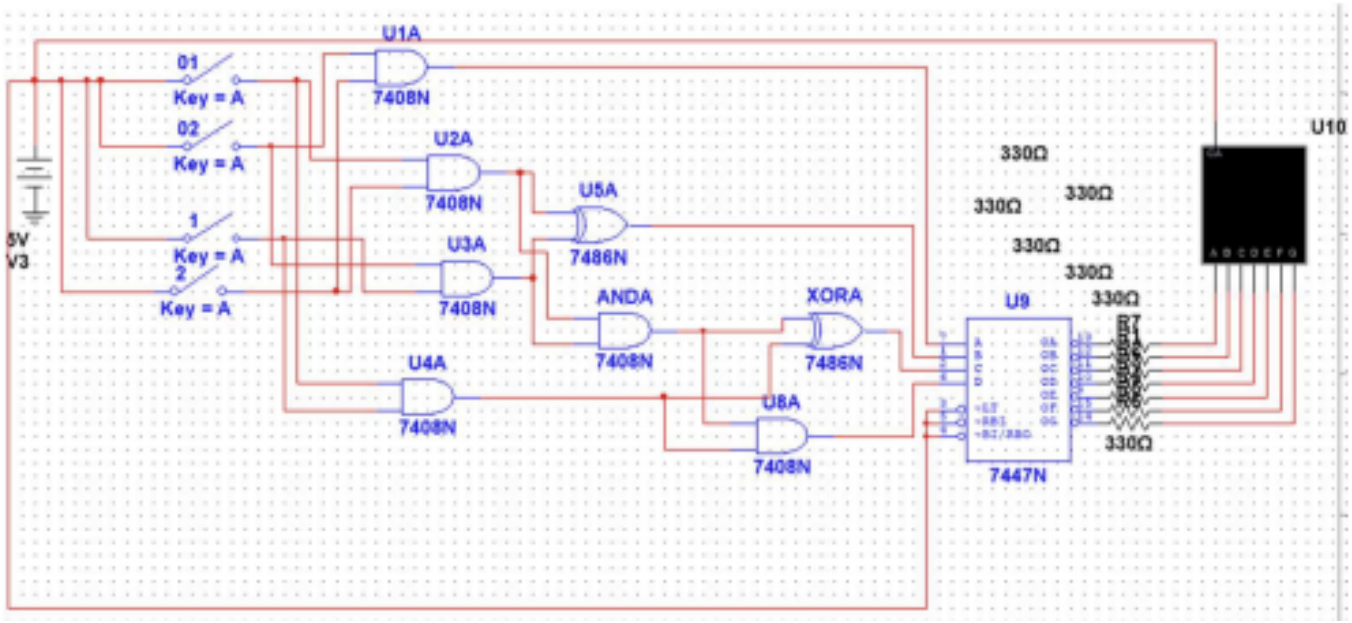
INPUTS						OUTPUTS				
A			B							
A1	A0	A_Dec.	B1	B0	B_Dec.	P3	P2	P1	P0	P Decimal
0	0	0	0	0	0	0	0	0	0	0
0	0		0	1	1	0	0	0	0	0
0	0		1	0	2	0	0	0	0	0
0	0		1	1	3	0	0	0	0	0
0	1	1	0	0	0	0	0	0	0	0
0	1		0	1	1	0	0	0	1	1
0	1		1	0	2	0	0	1	0	2
0	1		1	1	3	0	0	1	1	3
1	0	2	0	0	0	0	0	0	0	0
1	0		0	1	1	0	0	1	0	2
1	0		1	0	2	0	1	0	0	4
1	0		1	1	3	0	1	1	0	6
1	1	3	0	0	0	0	0	0	0	0
1	1		0	1	1	0	0	1	1	3
1	1		1	0	2	0	1	1	0	6
1	1		1	1	3	1	0	0	1	9

How it works:

As for the multiplication operation, it was carried normally using basic AND, OR and XOR gates. A*B was calculated manually using simple multiplication rules to produce the simplified expression to be implemented.

- **P0=A0B0 "A0 AND B0"**
- **P1=A1B0+A0B1 "(A1 AND B0) PLUS (A0 AND B1)"**
- **P2=A1B1+C1 "(A1 AND B1) PLUS C1"**
- **P3= C2 "C2 as it is"**

Circuit:



Power

Truth Table:

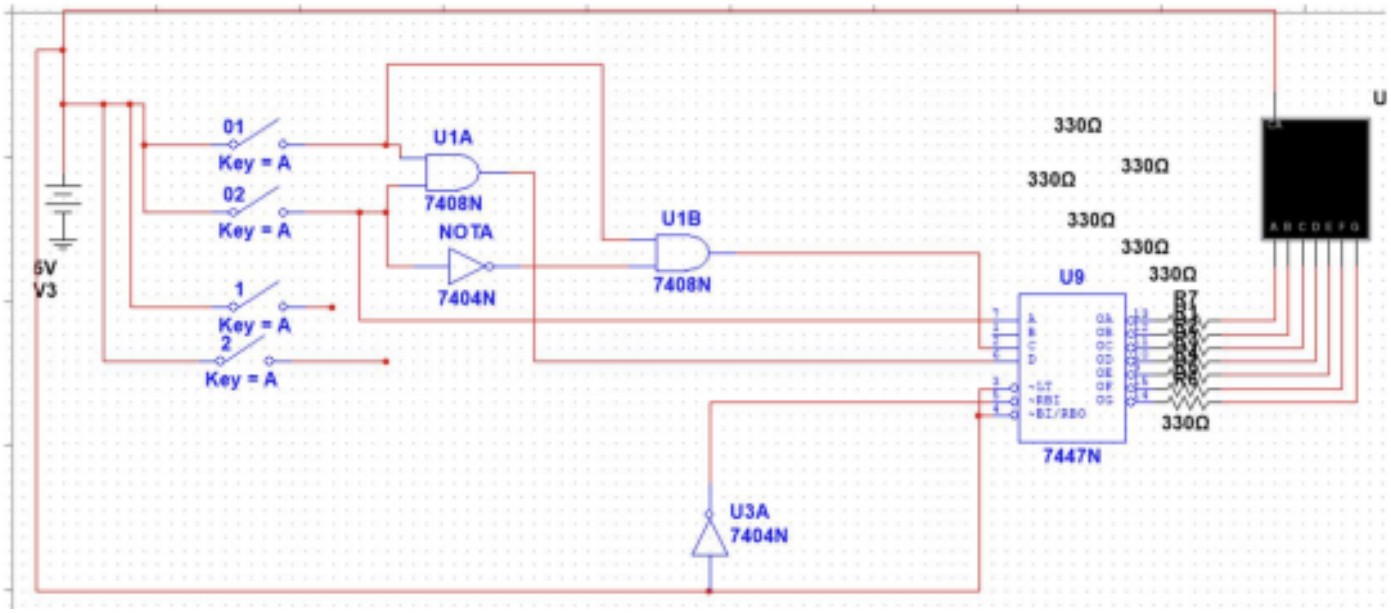
INPUTS			OUTPUTS				
A							
A1	A0	A_Dec.	S3	S2	S1	S0	S Decimal
0	0	0	0	0	0	0	0
0	1	1	0	0	0	1	1
1	0	2	0	1	0	0	4
1	1	3	1	0	0	1	9

How it works:

The procedure of squaring a number A depends only on the bits of A therefor the bits of number B has no interaction with the implementation of the circuit. There are only four possible values of the operation:

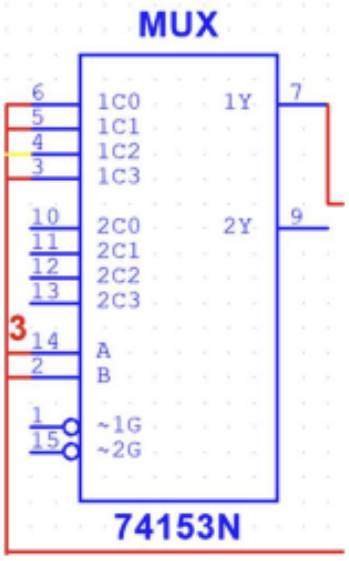
The circuit is completely done by AND and NOT gates after extracting the Sum of Products terms from the truth table then simplifying them using Karnaugh map. The truth table for the operation of squaring the number 'A' is also very useful to facilitate the understanding of the operation as well as fining out the SOP as well as simplifying the expressions using the K-map.

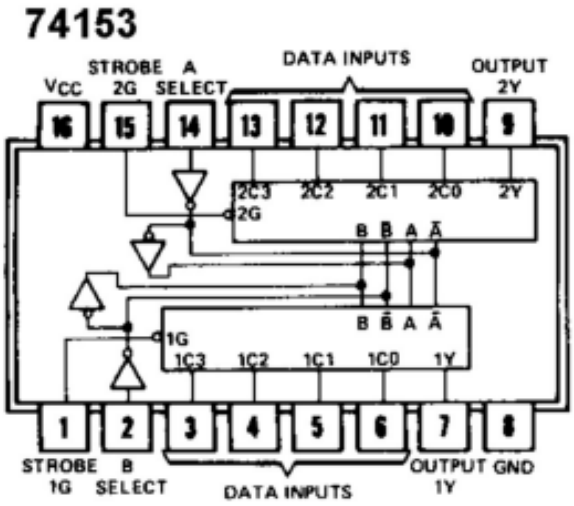
Circuit:



MUX

Circuit:





Truth Table:

Input Selection Lines		Outputs			
S1	S0	MUX 4	MUX 3	MUX 2	MUX 1
0	0	∑3	∑2	∑1	∑0
0	1	P3	P2	P1	P0
1	0	S3	S2	S1	S0
1	1	D3	D2	D1	D0

7-Segment

How it works:

The four outputs from the multiplexers, 1 output from each, are connected to a 7447 decoder to decode the binary numbers to decimal ones on the 7-segment display. The 7447 decoder receives 4 inputs in the A, B, C and D pins. The OA to OG pins are connected to the 7 segment display as inputs to it.

Circuit: