# CMOS FABRICATION TECHNOLOGY

## Introduction

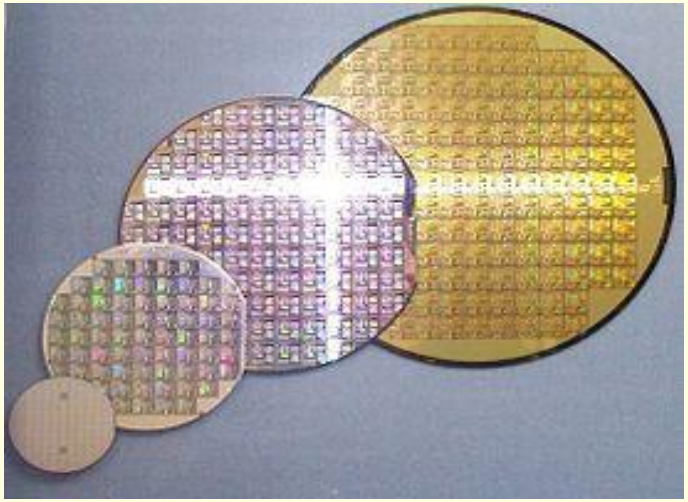
# CMOS Fabrication Technology

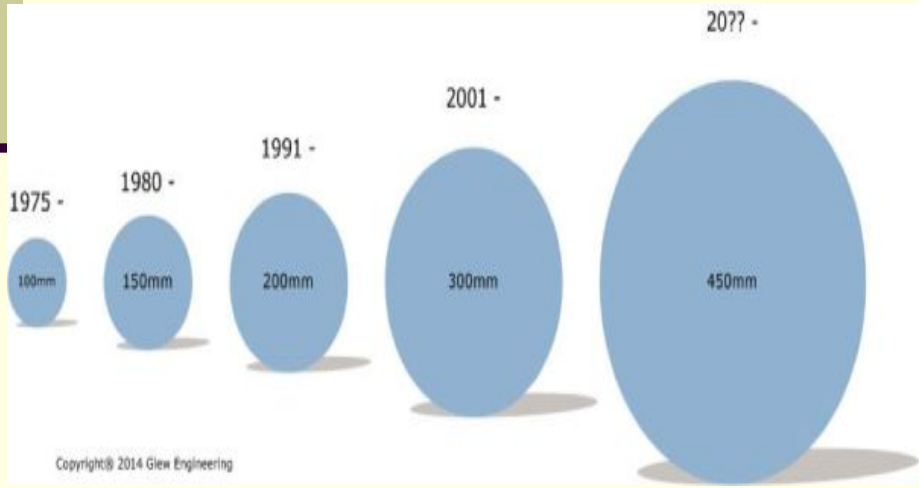
- A basic N-well CMOS Process
- The P-well Process
- Twin –tub Process
- Silicon On Insulator(SOI)

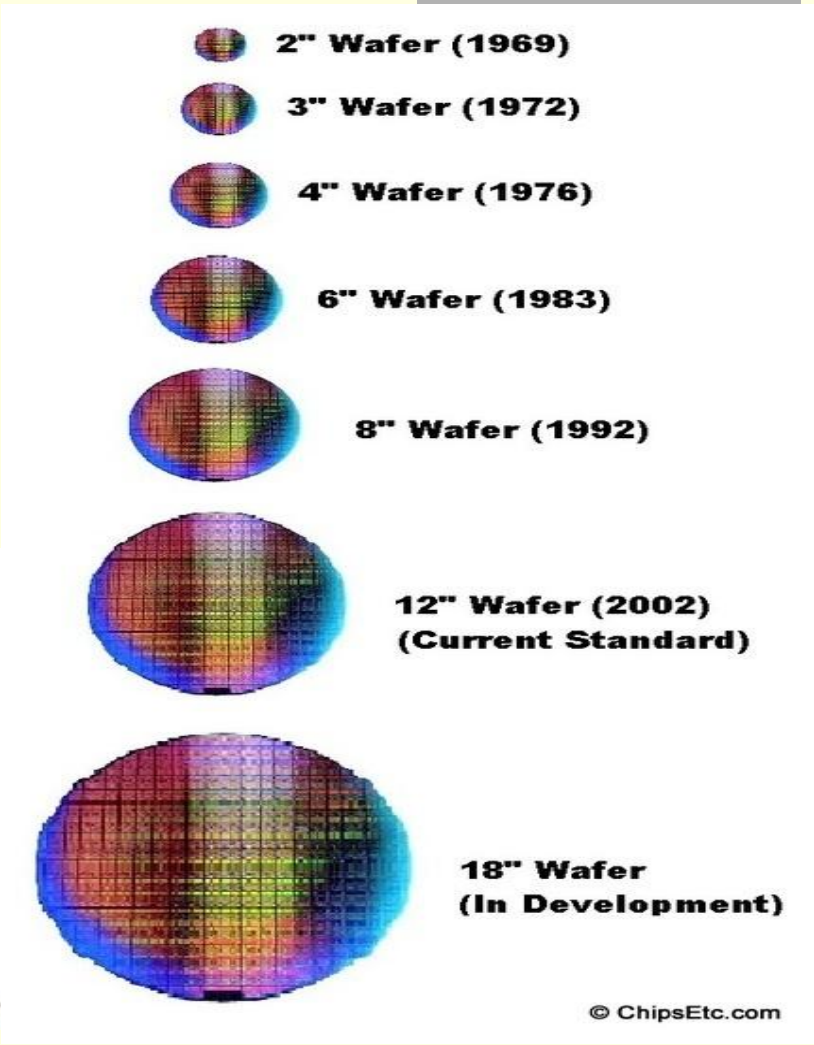
# CMOS Fabrication Process

- CMOS transistors are fabricated on silicon wafer
- Wafers diameters (200-300 mm)
- Lithography process similar to printing press
- On each step, different materials are deposited, or patterned or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

# WAFERS SELECTION

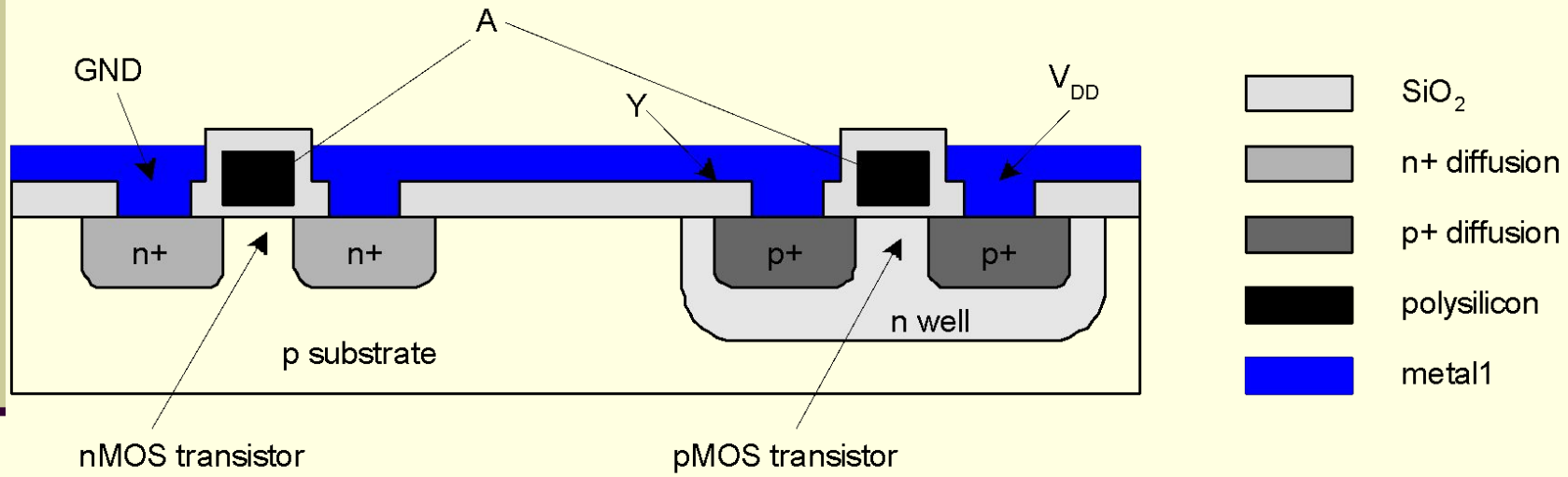




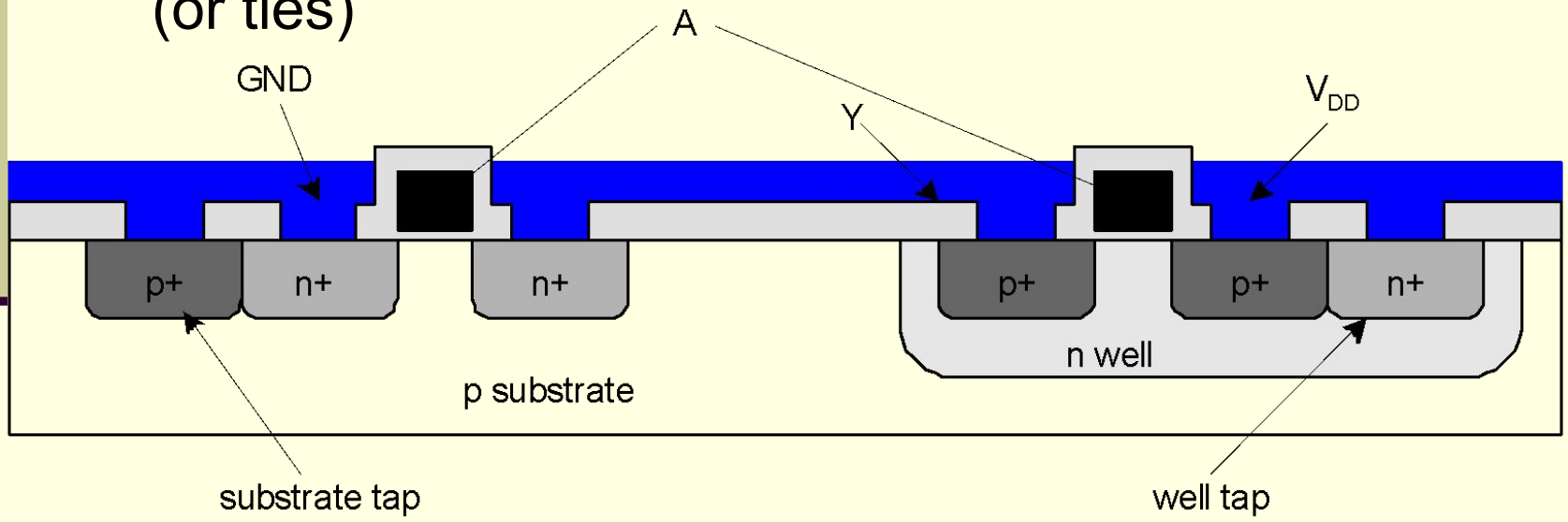
# Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires to make an n-well for body of pMOS transistors



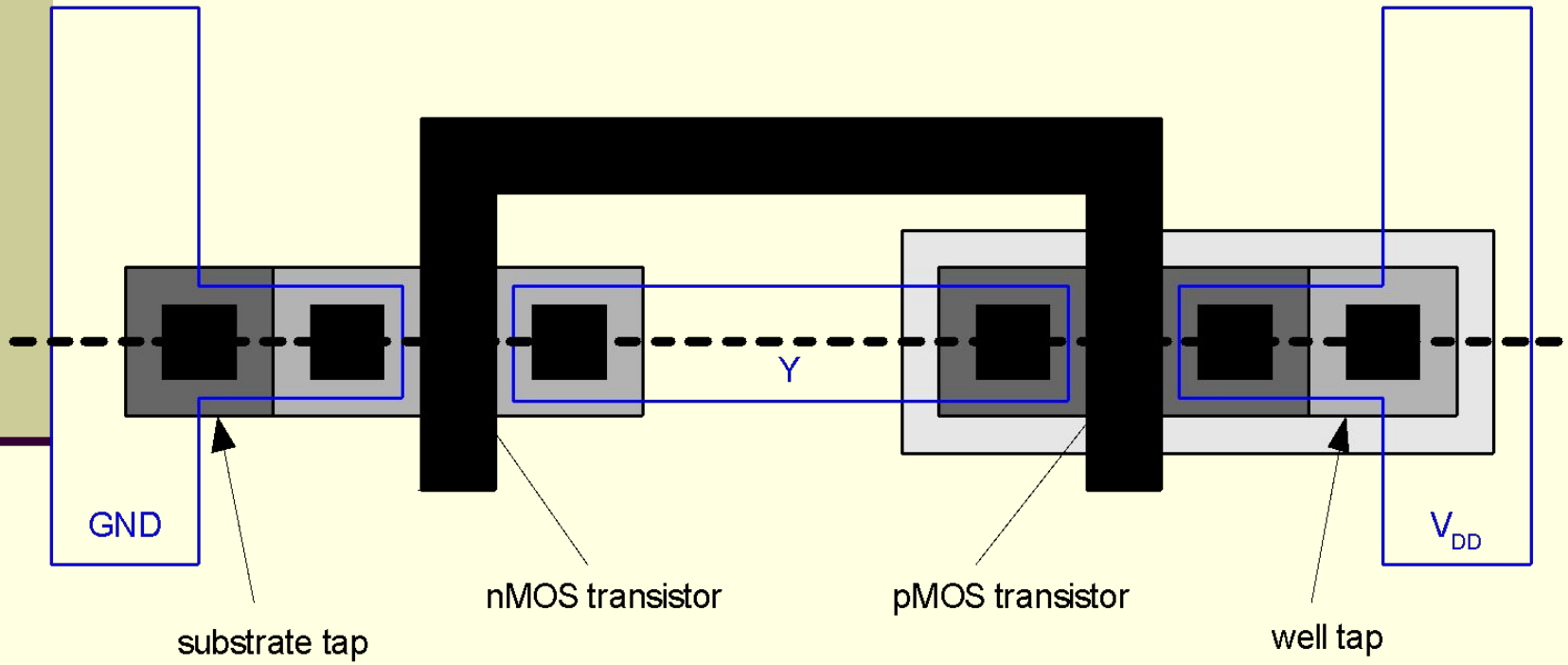
# Well and Substrate Taps

- Substrate must be tied to GND and n-well to $V_{DD}$
- Metal to lightly-doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts/taps (or ties)



# Inverter Mask Set

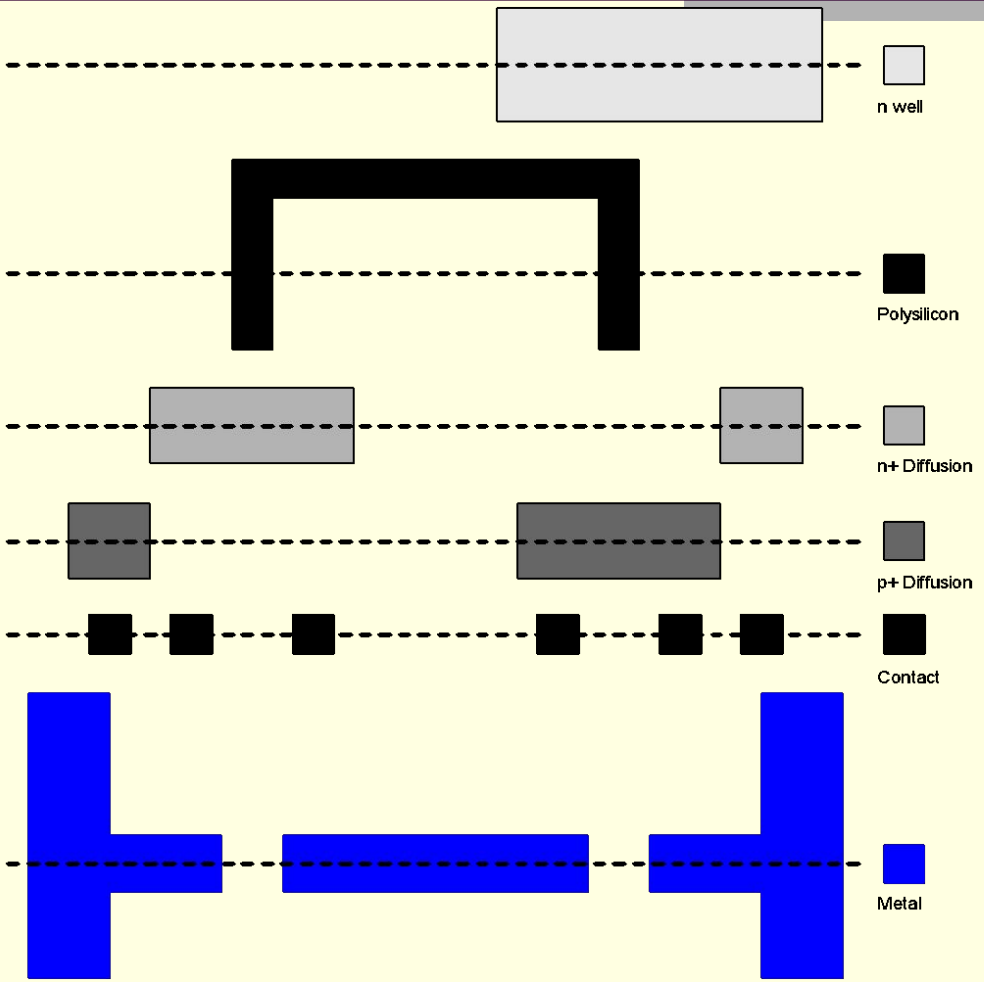
- Top view
- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



# Detailed Mask Views

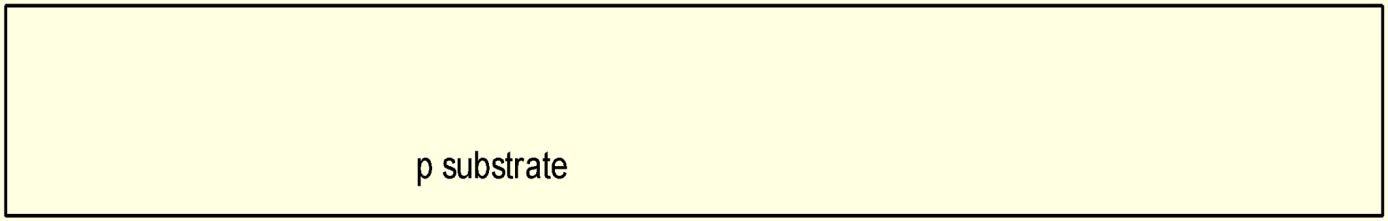
- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal

**In reality >40 masks may be needed**



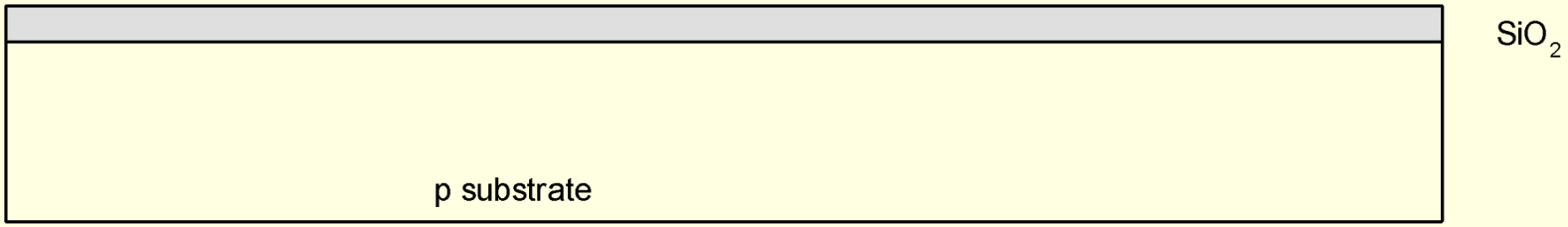
# Fabrication Steps

- Start with blank wafer (typically p-type where NMOS is created)
- Build inverter from the bottom up
- First step will be to form the n-well (where PMOS would reside)
  - Cover wafer with protective layer of $SiO_2$ (oxide)
  - Remove oxide layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer to form n-well
  - Strip off $SiO_2$



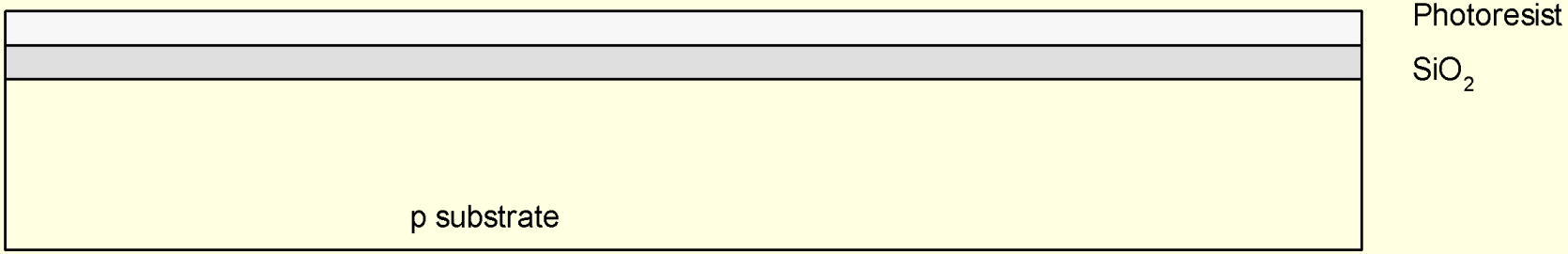
# Oxidation

- Grow $SiO_2$ on top of Si wafer
  - 900 – 1200 C with $H_2O$ or $O_2$ in oxidation furnace



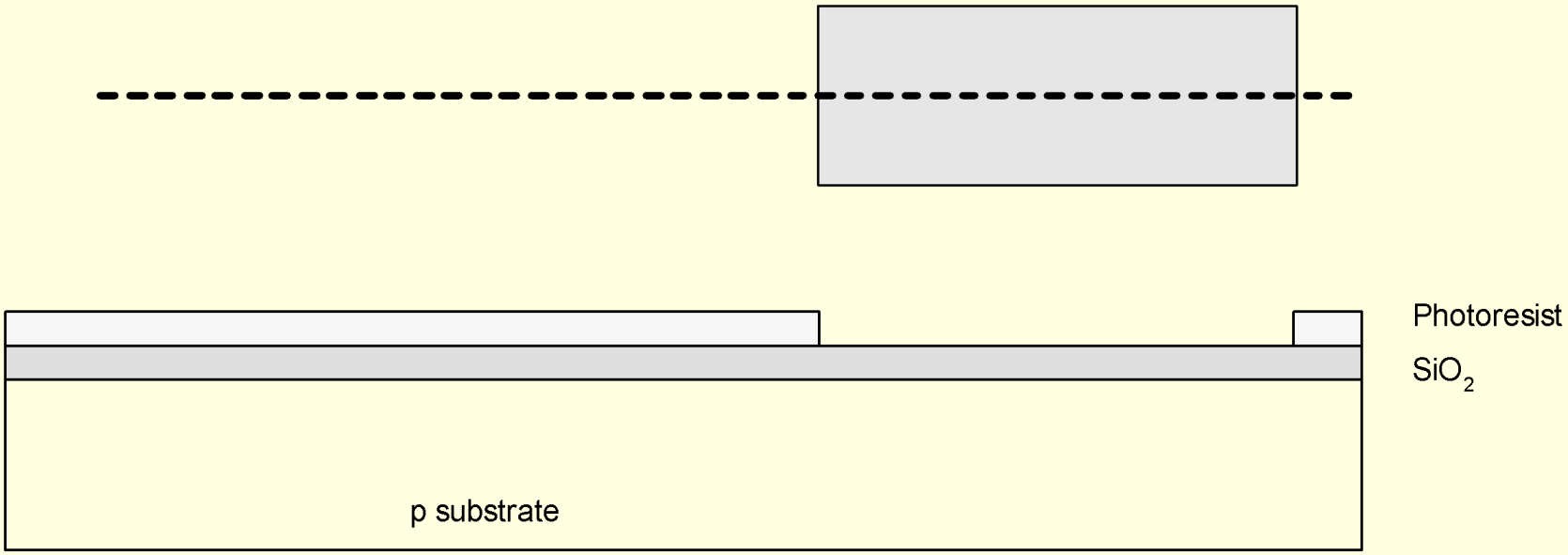
# Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Property changes where exposed to light
- Two types of photoresists (positive or negative)
  - Positive resists can be removed if exposed to UV light
  - Negative resists cannot be removed if exposed to UV light



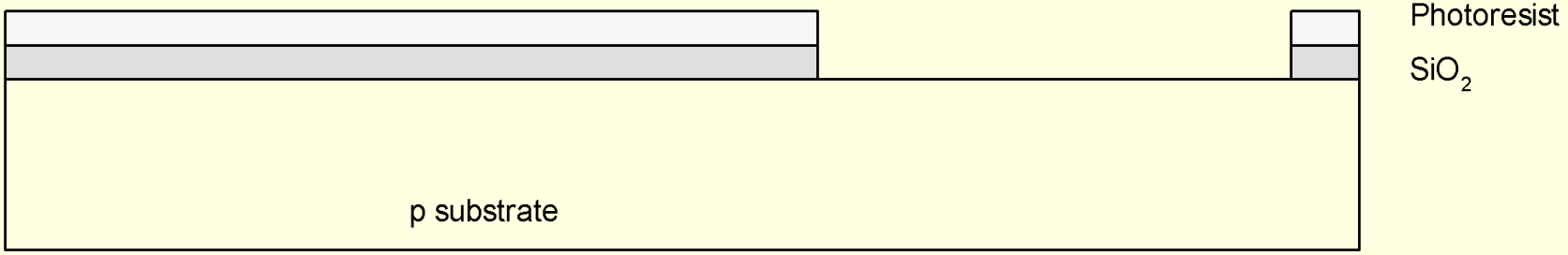
# Lithography

- Expose photoresist to Ultra-violate (UV) light through the n-well mask
- Strip off exposed photoresist with chemicals



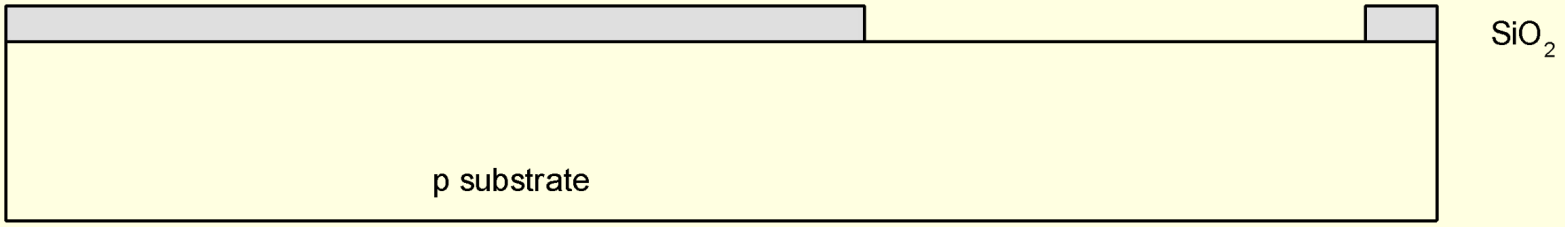
# Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!!
- Only attacks oxide where resist has been exposed
- N-well pattern is transferred from the mask to silicon-di-oxide surface; creates an opening to the silicon surface



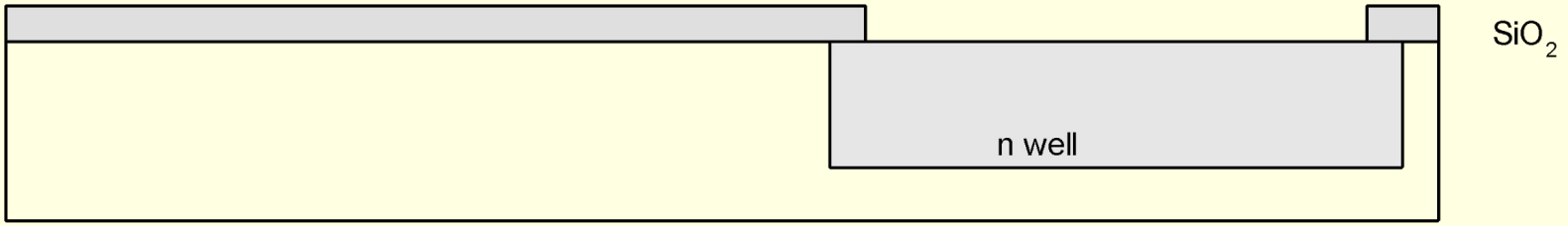
# Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn't melt in next step



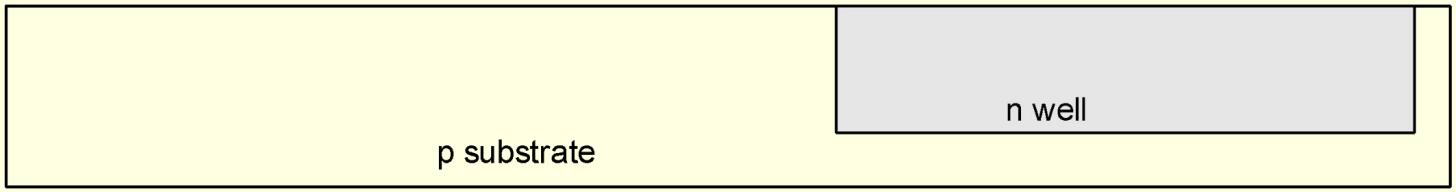
# n-well

- n-well is formed with diffusion or ion implantation
- Diffusion
  - Place wafer in furnace with arsenic-rich gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implanatation
  - Blast wafer with beam of As ions
  - Ions blocked by $SiO_2$, only enter exposed Si
- $SiO_2$ shields (or masks) areas which remain p-type



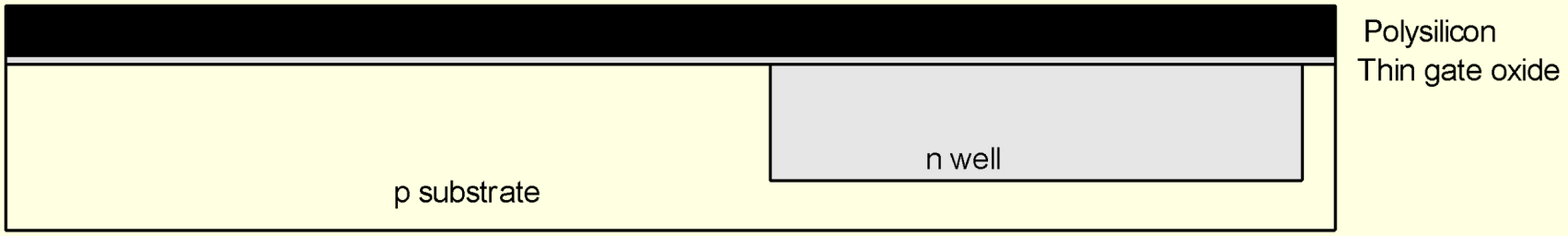
# Strip Oxide

- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps



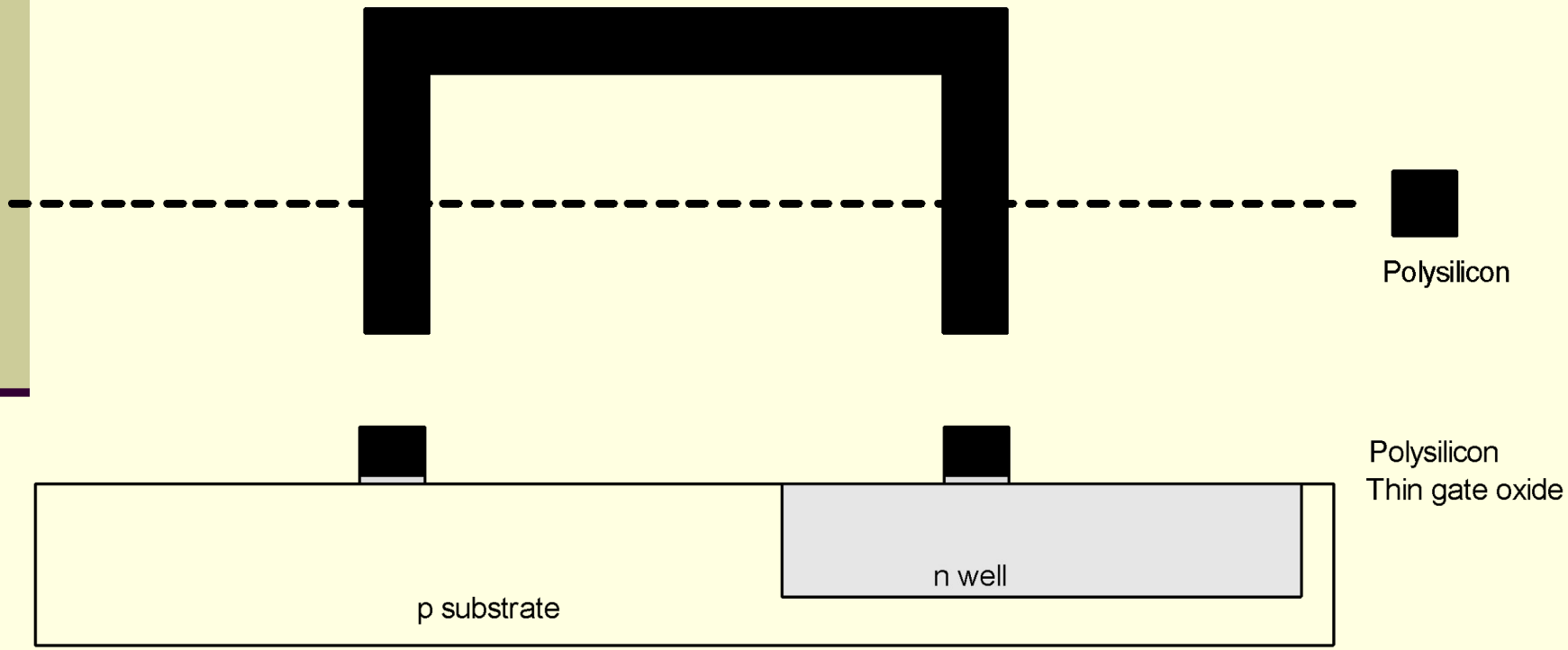
# Polysilicon
## (self-aligned gate technology)

- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of silicon layer
  - Place wafer in furnace with Silane gas ($SiH_4$)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor



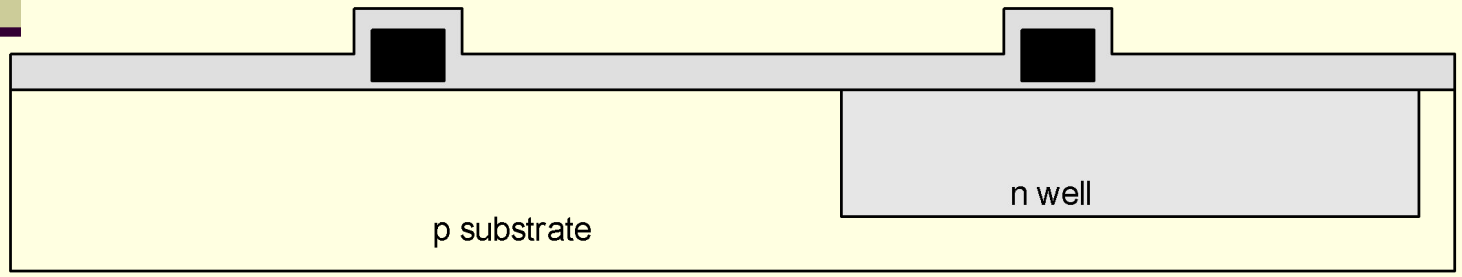
# Polysilicon Patterning

- Use same lithography process discussed earlier to pattern polysilicon



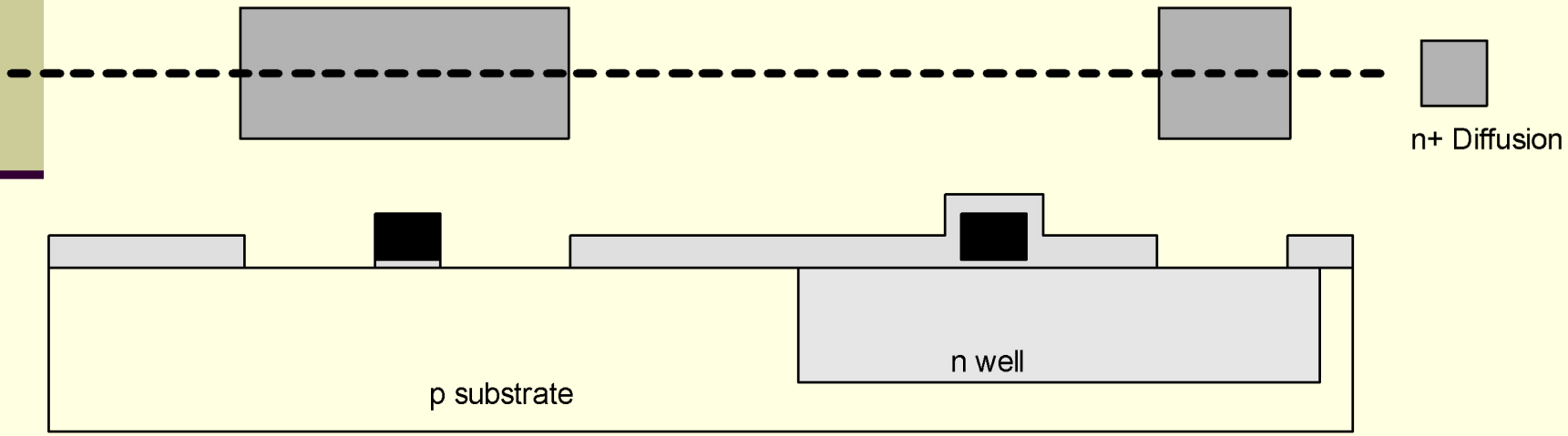
# Self-Aligned Process

- Use gate-oxide/polysilicon and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact



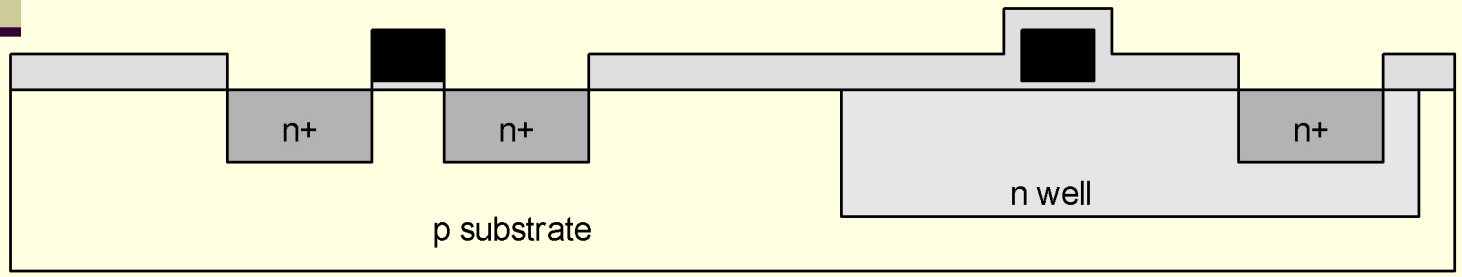
# N-diffusion/implantation

- Pattern oxide and form n+ regions
- *Self-aligned process* where gate blocks n-dopants
- Polysilicon is better than metal for self-aligned gates because it doesn't melt during later processing



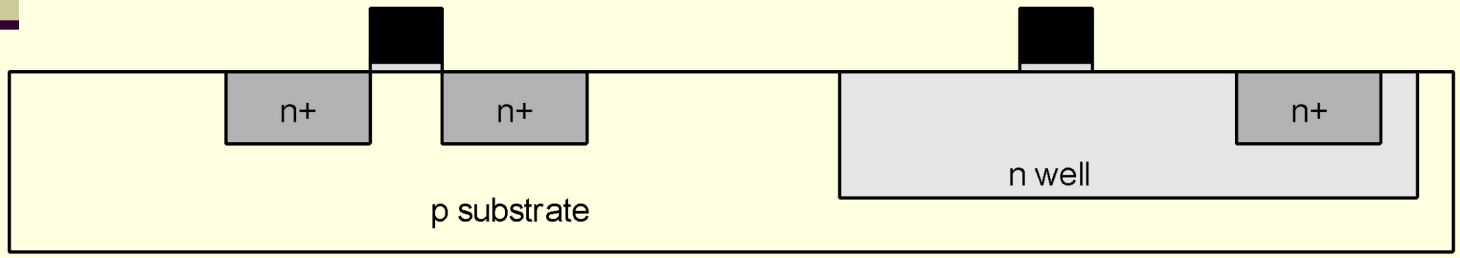
# N-diffusion/implantation cont.

- Historically dopants were diffused
- Usually high energy ion-implantation used today
- But n+ regions are still called diffusion



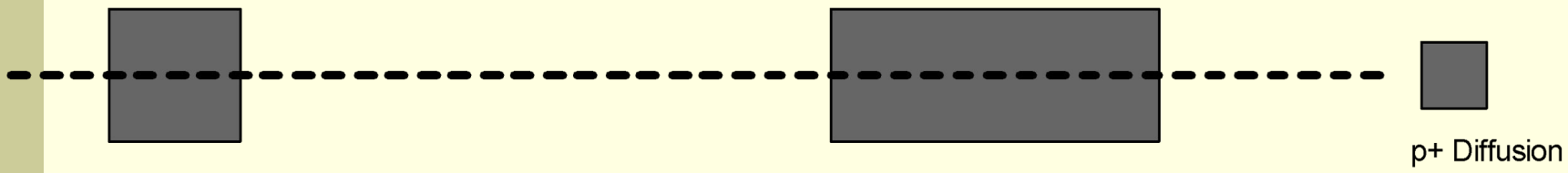
# N-diffusion cont.

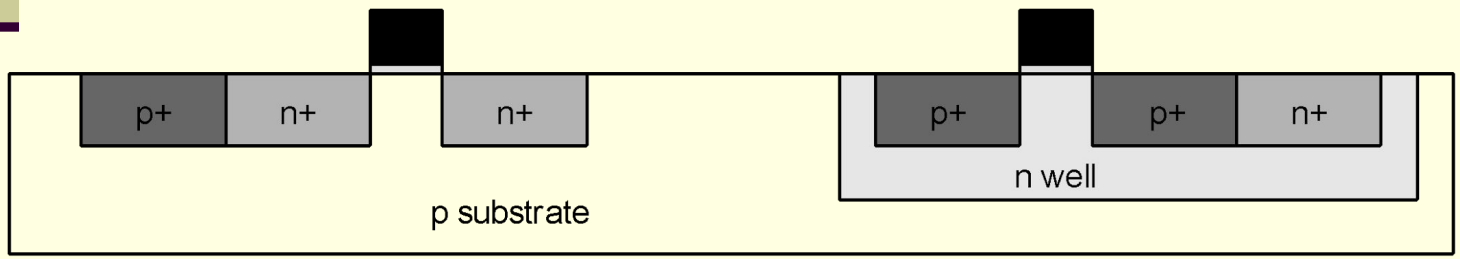
- Strip off oxide to complete patterning step



# P-Diffusion/implantation

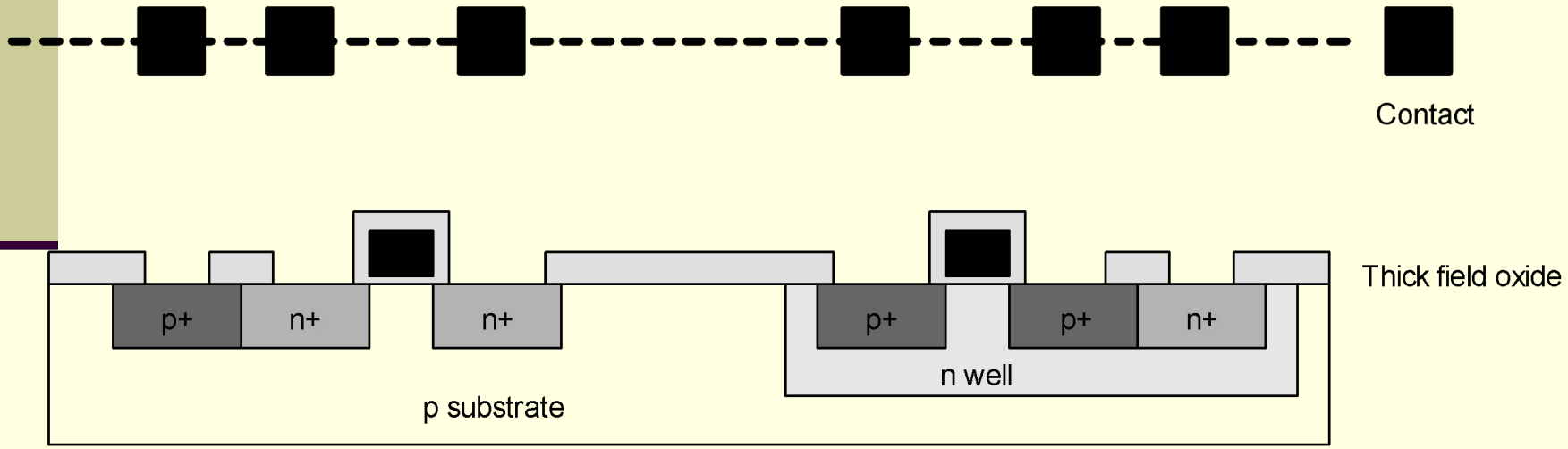
- Similar set of steps form p+ “diffusion” regions for PMOS source and drain and substrate contact



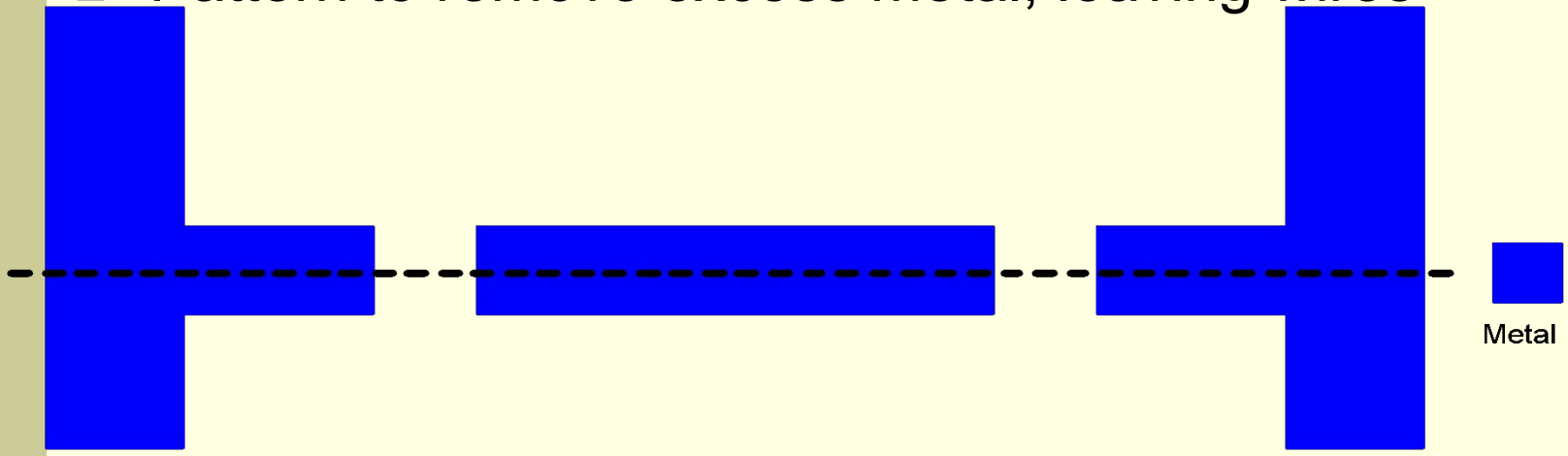
# Contacts

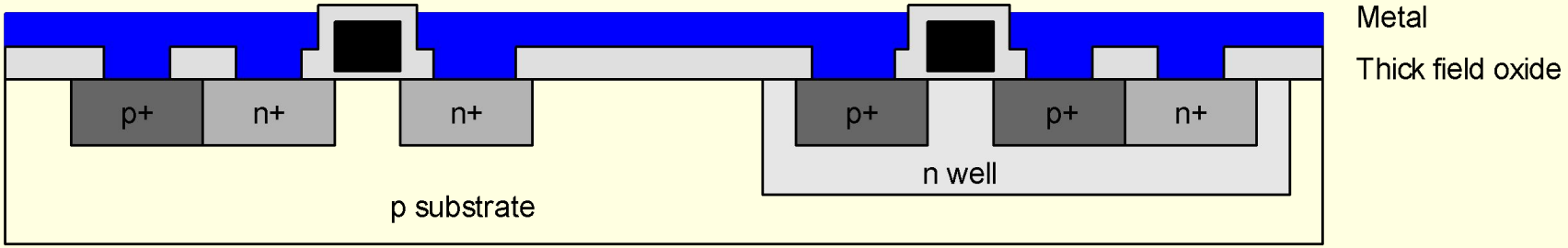
- Now we need to wire together the devices
- Cover chip with thick field oxide (FO)
- Etch oxide where contact cuts are needed



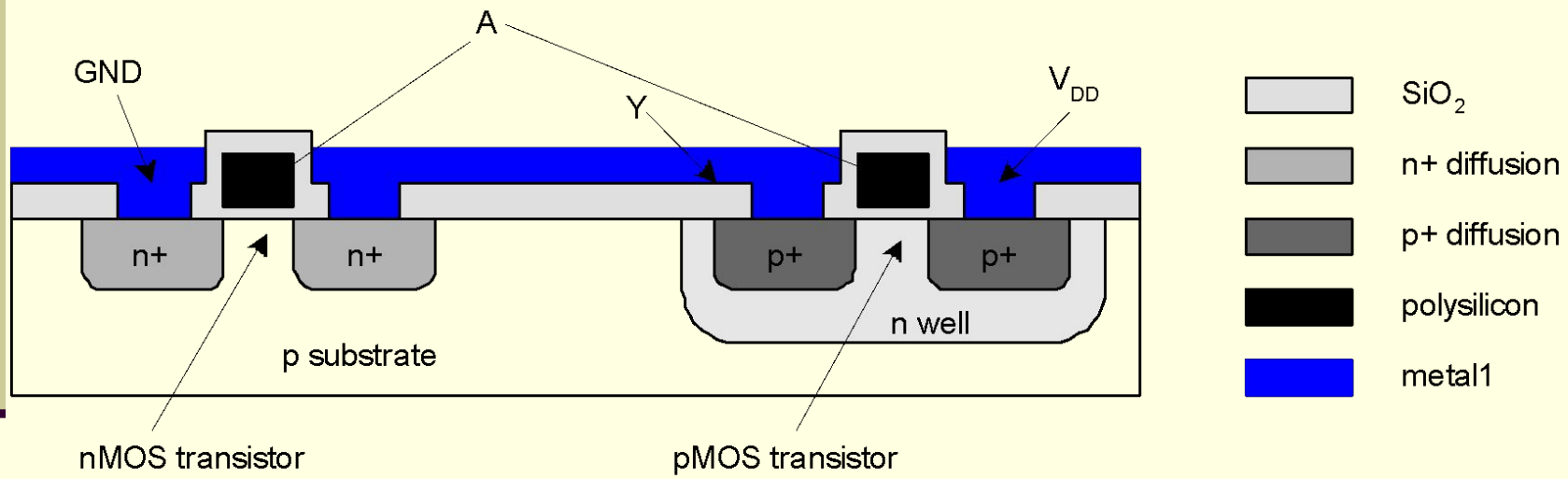
# Metalization

- Sputter on aluminum over whole wafer
- Copper is used in newer technology
- Pattern to remove excess metal, leaving wires



# Inverter Fabrication Cross-section



# THANK YOU