SPI (Serial peripheral Interleve) MOST = SOI serial date in marke always initiates tronsaction. SCIK most spi SPI MOSZ Mayter masq 2 SCIK -> serial de clode mosz -> mouter out slave in MISO > Master in slave out 55 -> slave relear (chip select, active low) Muske musi mosz slave miso m450 552 553. musz slave mzso mos, slave om zpu 55

Advantages / pisaduantages. >Full duplex more pinsthan UARTHER Higher speed thom short distance vs. RS485/RSE3Z UART + 12 C Lots of variants > unbiquitous CPOL -> clock polarity CPHA -> clocic phene. CPOL = 0 epol = 1 22 CPHA= 4 Cycle X 2 X 3 X 4 XS M230 2X1X2X3 X4X mast 2 X 1 X 2 X 3 X 4 X CPHA=O & & D cycle XIXXXXXXXX MZSO X. 1 XZXX 3 X 7 X CX MOSIXIXLX3X4X5X

Key fectures of SPI:-1 Full-Duplex communication SPI supports simultaneous data tronsmission and reception. 2] master slave architecture: -SPI supp There is typically one marker device and one or more slave 3] four wire interface · MOSI Cmayter out Storve In) carries datafrom the meriter to the slave · MISO (Mey tex in slave out) coories data from the slave to the mester · SCHK (sepicel dk) · SS (slewe select) 1000 Used by marker to select which slave occince to Communicate with. # How SPZ works! 17 initialization master configures the clock polarity (cPO2) and clock phase (CPHA) settings. It also determines the dove brequery. 27 Octa Trunsfer. · The meester pulls the ss line low to release slave. * The marker 'generaly clockep led on the selle line. · Date is shifted out of he most line bom master and into me slave, while date from the slave is shilled out of he meso line and into master.

Slave date Trumition Diagram Fim 55×=1 TOLE 65-50 55 n =1 64,0 Read - du cotife ss-n = 62 Reed dwa is 60 write add la mouth Mago port mos Zer been lig =1 Read-addr Reversed RAM 88 CHK_LMD fug=0 Reed.

