Weekly Status Report

Name of the Engineer: Anas Khan

Working at Client Place: No **Name of Client: BB Training Centre**

Working in-house: No **Reporting to: Mr. Ajay Sagdeo/Dr. Praveen**

Duration: 12 FEB to 16 Feb 2024 **Number of hours Invested/week: 40 h/w**

Date	Duration	Description of work	Outcomes
12 February 2024	10 am to 1 pm	Introduction to the Counters and Timing diagrams.	Understood the Counters and Timing diagrams concepts.
	2 pm to 5 pm	Synchronous Counters- Twisted Ring Counter, Ring Counter. Asynchronous Counters- Ripple Counter.	Understood Synchronous Counters and Asynchronous Counters. .
	5 pm to 6:30 pm	Practice on Counter Design.	Done practice on Counter Design Questions.
13 February 2024	10 am to 1 pm	Introduction to Shift Registers and their Configurations.	Understood the concept of Shift Registers and their configurations.
	2 pm to 5 pm	MOD-n up/down counter design.	Able to design MOD-n up/down counters design.
	5 pm to 6:30 pm	Finite State Machine. Sequence Detector- Moore and Mealy.	Able to design FSM.
14 February 2024	10 am to 1 pm	Static Timing Analysis, Metastability, State Machine Minimisation.	In-depth understanding of Timing Analysis.
	1 pm to 5 pm	State Encoding methods, iterative pattern recognition, data path, control path.	Able to design iterative pattern recognizer circuits.
	5 pm to 6:30 pm	Algorithmic state machine, elements, and chart.	Able to draw ASM chart for Mealy and Moore.

15 February 2024	10 am to 1 pm	Asynchronous Circuit Design-with and without latch.	Able to implement Asynchronous Circuit Design.
	2 pm to 3 pm	Merger Graph/Compatibility Graph, incompletely specified machine.	Understood the Concept in detail.
	3 pm to 6:30 pm	Practice Question Bank on ASM, ISM.	Got additional knowledge on MSI Blocks.

Date	Duration	Description of work	Outcomes
16 February 2024	10 am to 1 pm	Memory Design and Expansion.	Understood Design approach.
	2 pm to 5 pm	PLD classification, CPLD, FPGA, LUT. Introduction to ASIC and ASSP	In-depth understanding of concepts and applications of ASSP, ASIC, and FPGA.
	5 pm to 6:30 pm	Practice Memory Design and Duty Cycle.	Done practice in Conversions.