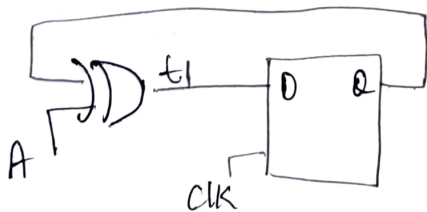
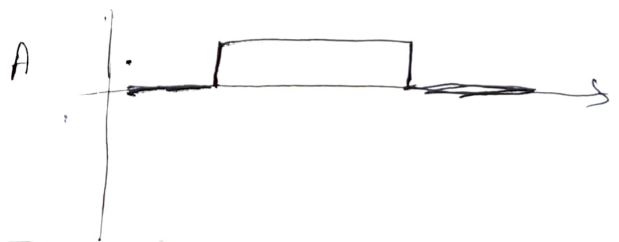
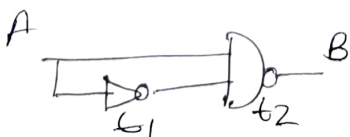


- Q) Tell me about yourself
- Q) So what is Serdes? How do you convert parallel data into serial data? [~~about~~ It was related to Project]
- Q) Max Questions
- Q) Do you know about LDO? explain with block diagram
- Q) Follow up question on Feedbacks $\begin{cases} \text{Negative} \\ \text{Positive} \end{cases}$
- Q) Where do you get reference voltage - BGR
- Q) What is difference between BGR & LDO
- Q) Explain how BGR maintains 1.21V despite PVT variation
[as I mentioned this was follow up question]
- Q) Do you know verilog & system verilog? what are Blocking & Non blocking assignments.
- Q) He gave CKT diagram & asked to write verilog code

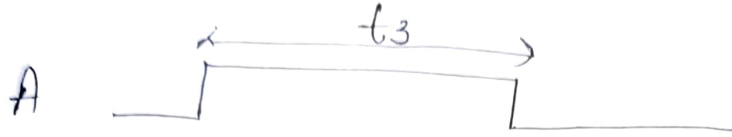


- Q) He gave an CKT diagram which has Propagation delays t_1 & t_2 and asked to write output waveform



c) follow up question

what if $(t_3 < t_1)$ then draw output waveform.



d) what is interdelay & intradelay?

e) what will be v_{out} .

