7th February 2025

SESSION 4 MEETING MINUTES

INTRODUCTION

1. Understanding RTL and why is it important?
2. If we have RTL why do we use Verilog or SystemVerilog?
3. Recap of STA (Static Timing Analysis), and discussed Setup and Hold Time.

ASSIGNMENT

1. Digital clock assignment to be continued.
2. To start implementation using Verilog.

DISCUSSION

1. Abstraction Layers and Modeling Types:

Abstraction Layers:

1. SVRNM (System Verilog Real Number Model)
2. Wreal (Wire Real)
3. Electrical
4. Schematics (Note: Schematics are not models but actual circuit representations)

Modeling Types:

- SVRNM: Uses an **EE package and EE net**, which relies on Ohm's Law. It can handle voltage and resistance calculations but does not calculate current since that requires a circuit. The limitation is that it lacks an **inout** connection.
- Wreal: Used in simulations but is computationally expensive. It can be used as **inout** but has limitations, such as multiple drivers not being supported. **Schematics are used in Wreal modeling.** Uses VAMS language.
- Electrical (AMS Model): A more accurate analog behavioral model using **VAMS language.** It provides true analog behavior and enables circuit-level verification. This model is not used quite often.

2. UPF, Inout Wires, and Analog Behavior:

- UPF (Unified Power Format): Used to simulate power intent in designs.
- Inout Wires: Capable of connecting circuits to wires, depending on wire direction. **All analog/electrical signals are inout**, though **SVRNM does not support this.**

- **Wreal in Inouts:** Wreal can be used for inout connections but doesn't support multiple drivers.

3. Verification Flow Discussion:

1. **Specs:** Define system requirements.
2. **Vplans (Test Plans, Methodology, Coverage, Testbench):** Framework to validate the design based on specs. Importance of Vplans?
3. **Modeling:** Creating design models using given specs.
4. **DMS (Top-Level Connectivity with Model):** Ensures testbench and connectivity issues are addressed before moving to AMS.
5. **AMS (Analog Mixed-Signal Verification):** Converts specific models into schematics for actual verification.
6. **Coverage & Regression:** Ensures all features are tested and functioning as required.

DOUBTS:

1. *Why can't current be modelled in SVRNM?*

CONCLUSION

This meeting provided a comprehensive understanding of different modeling types, emphasizing their significance in verification. Also explored the role of SVRNM, Wreal, and Electrical models in circuit design and discussed the verification flow from specifications to final validation. Understood the importance of Vplans before the start of a project. Next session will begin with a quick recap of the previous meetings(ASIC flow, Full Custom flow).