Novel approach for accelerating Mixed Signal Verification through System Verilog and Analog assertions

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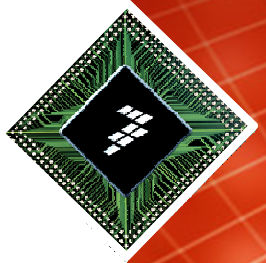

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Challenges

- Large number of configurations & programming options for most AIP blocks
- No formal Equivalence check for VAMS & SPICE models
- Non-Overlapping Verification cycles
- Huge time on AMS simulation
- Simple Verilog-AMS Drivers/Monitors used to automate AMS Verification
- Large effort that goes into developing VAMS Components

Verilog vs VAMS

VAMS has following additional Advantages:

- Notion of Current and Voltages in digital simulation
- More construct than verilog

VAMS vs Digital Simulation

In VAMS

- No randomization
- Very low interaction with other high level languages like C.

In Digital

- No notion of Electrical Interface
- No voltage domain checking is possible as only 0 and 1 are level

Current Solutions

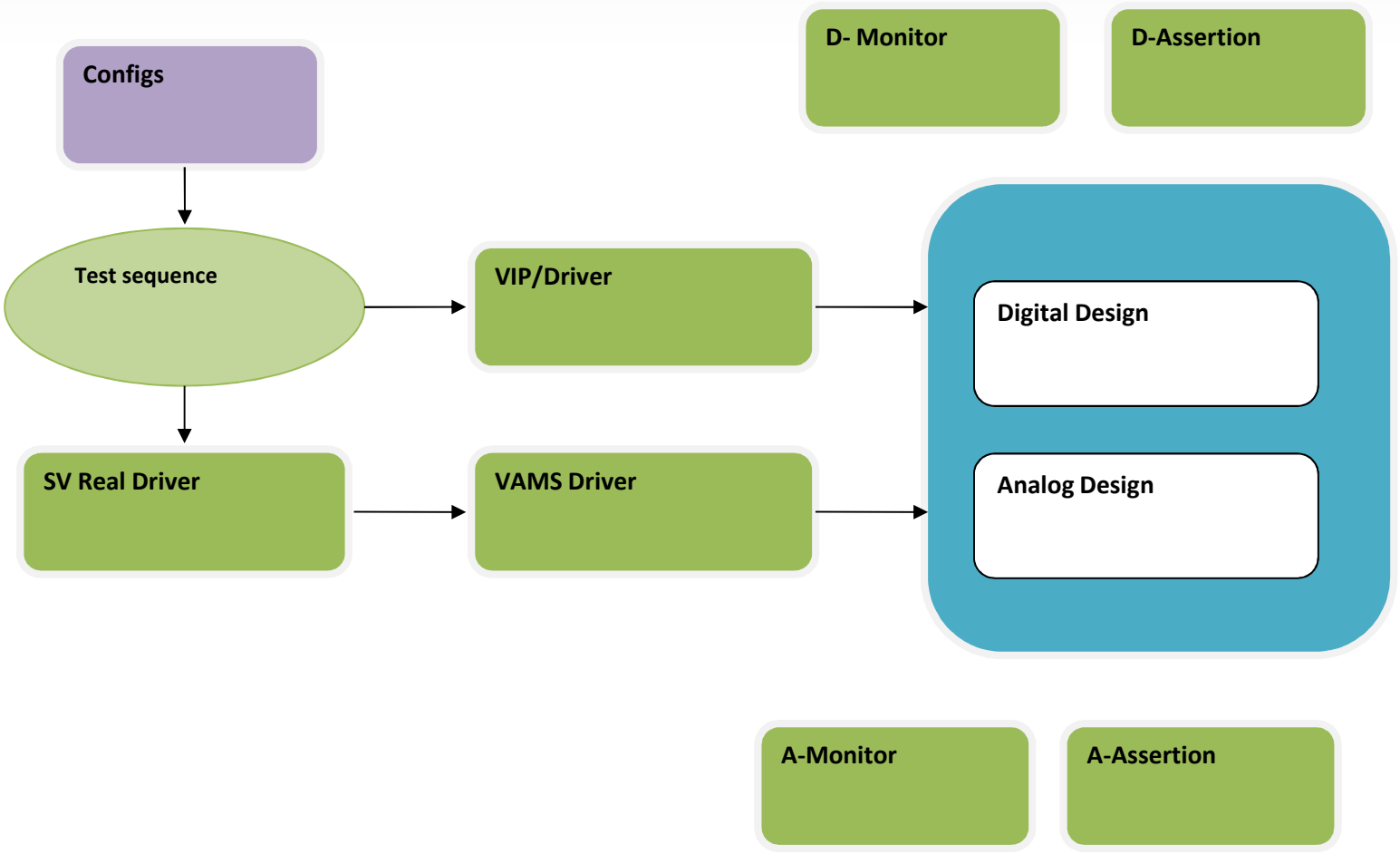
Spice Simulation to check analog behavior but has inherent problems

- Comes very late in design cycle
- Long run time
- Very less feature can be verified
- No overlap with Digital verification so lead to change in digital logic at very end

Our Solution

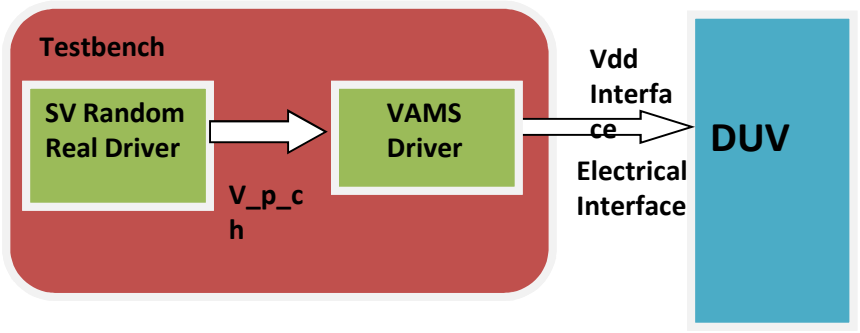
- **SV-Real and VAMS**
  - Data generation in SV domain
  - Simplified VAMS for Test bench purpose
  - Random and Coverage driven Verification
  - Re-usable Test bench
  - High performance accurate models for VAMS at RTL

Mix Signal Testbench Architecture



SV Real Vs VAMS interactions

```
//Function to generate Random Real number
  function real genRealRandom( int minRange , int maxRange , int divFac );
    real RandRealout;  //generated real number
    int NumRange;

    NumRange= $urandom_range ( (minRange*divFac), (maxRange*divFac))  ;

    RandRealout = $itor(NumRange)/$itor(divFac);

    return(RandRealout);

  endfunction
```

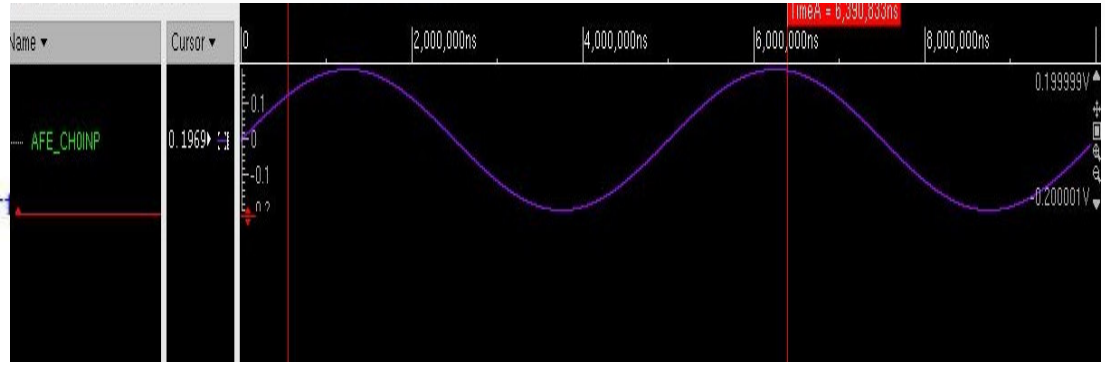


SV Testbench : Electrical Interface with DUV

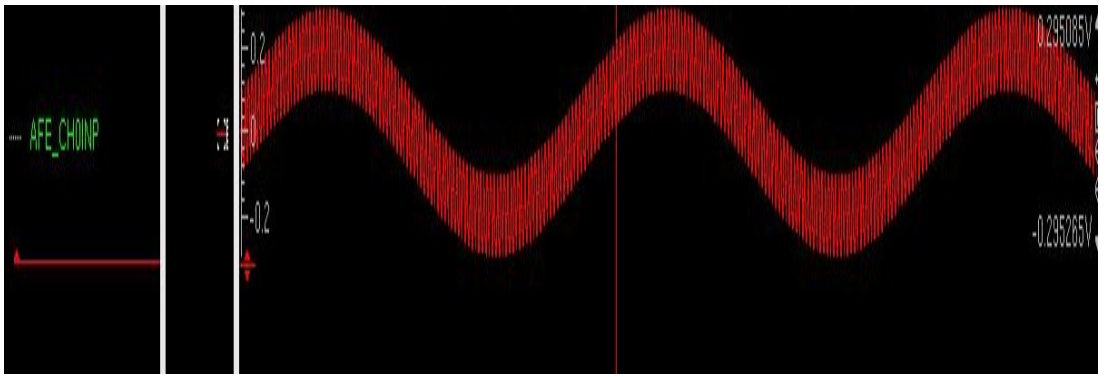
```
module Vsrc_switch(V_out,gnd_node);
input gnd_node;


output V_out;  // Electrical Output going to connect to [
electrical V_out,V_src;
electrical gnd_node;
.
.
.

  analog
  begin
    if(drv_en)
       V(V_src,V_out) <+ V_x_on;                    // vol
    else
      I(V_src,V_out) <+ V(V_src,V_out) / R_off;    // curr

     V(V_src,gnd_node) <+ transition(V_reg,10p,t_rise);
  end

 task set_V;
   input V_in; // Real output from SV Driver
   real V_in;
   begin
     V_reg = V_in;
   end
.
```

Data and Noise generation

```
// --- task to generate sine wave using DPI
// --- randomize amplitude( amp ),
// --- theta , DC Offset (offest) is
// --- provided through System Verilog Real
// --- Number Randomization
// --- Sine Wave is Driven through Vams interf

task Sine_wave(input real theta ,
               input real amp ,
               input real offset);
ams_if.V_p_ch <= (offset + amp*math_pkg::sin(theta));
endtask
```

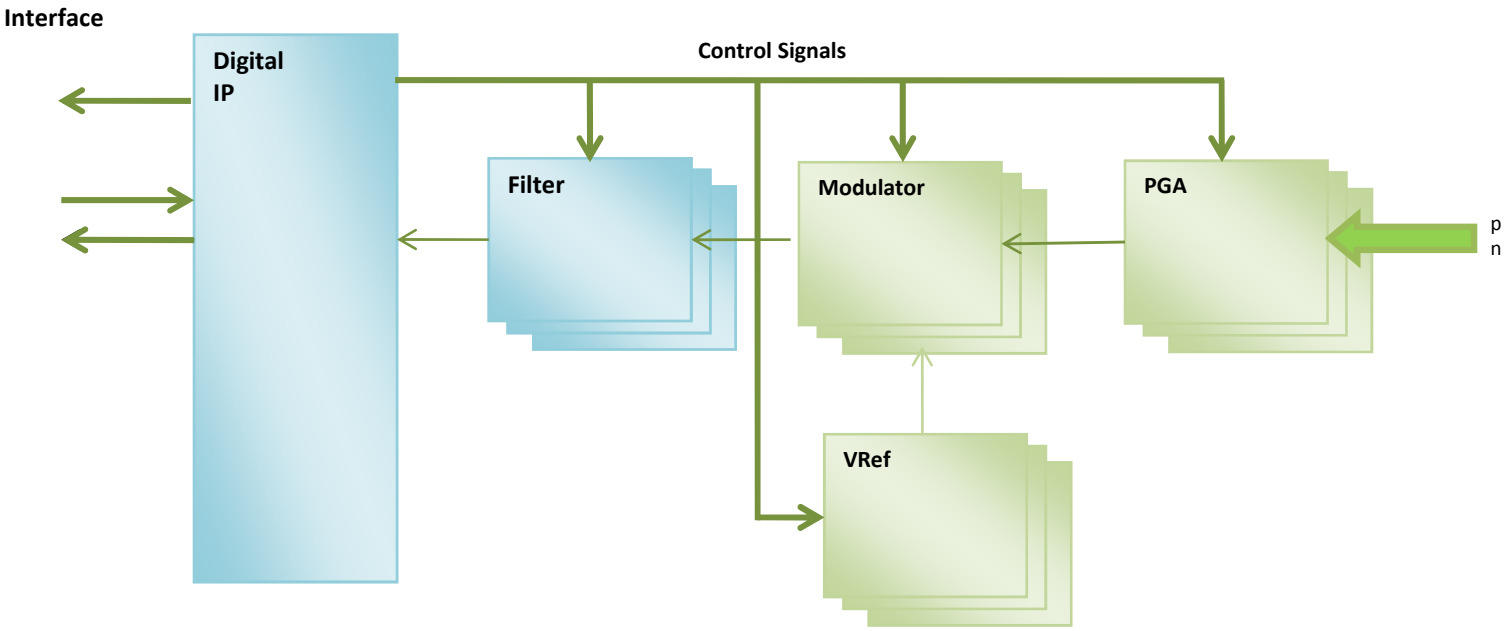



```
task White_noise( ref  real noise );
 integer temp;
 real theta;
   while(1)begin
   theta = 2*3.14159*200000*time_s;
     noise =0.1*math_pkg::sin(theta);
     ams_if.Noise <= noise;
    @(posedge ams_if.ipg_clk);
   end
endtask
```

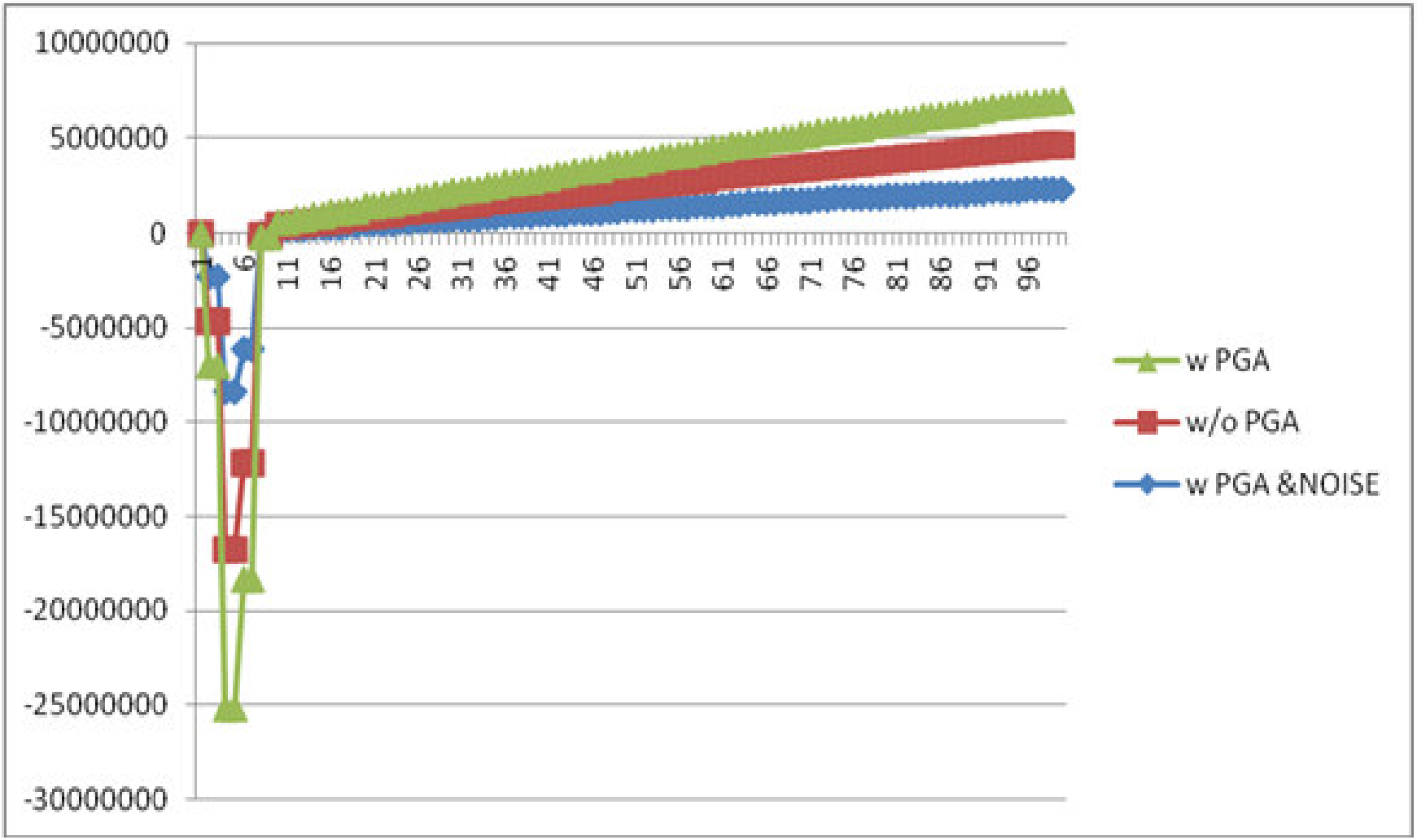


Case Study

- The functionality requirement from analog models
  - Voltage measurement in both differential and common mode.
  - Variable programmable sampling rates
  - Run time Configurable analog gain
  - User selectable reference voltage source.



Output with unfiltered Noise(>40 Mhz)

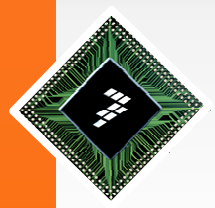


Results

S.No.	Functionality	AMS *Simulation	Proposed Method	Benefits of Proposed Method
1.	Single run individual block (ADC, Low Pass Filter, Gain Amplifier, Power Connectivity, Sampling precision check)	>3-6hrs	~30 mins	1. Development Cycle time is reduced 2. More features can be verified in given time frame
2.	Single test Combined blocks (ADC, Low Pass Filter, Gain Amplifier, Power Connectivity, Sampling precision check)	~24hrs	~1hr	
3.	Randomization	No	Yes	Robust Verification
4.	Configurable accuracy at signal sampling time	No	Yes	Speed up simulation

Conclusion

- Multiple IP Features to be verified
- Exhaustive coverage needed
- Across corner Cz. Needed
- Simulation Speed very important
- Moderately Accurate VAMS Model
- Approach : VAMS Based RNM Simulation with SV-VAMS approach



THANK YOU

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