Unit 3.

# Differential Amplifiers.

The differential amplifier operation has become the dominant choice in today's high performance analog and mixed-signal circuits.

· The analysis and design of cmos differential amplifiers.

· We will analyze both the large-signal & small signal behavior.

· The study of differential pairs with diode-connected and current source loads as well as differential cascode stages.

We will also introduce the concept of common-mode rejection & formulae it for differential amplifiers.

## Single-Ended and differential operation

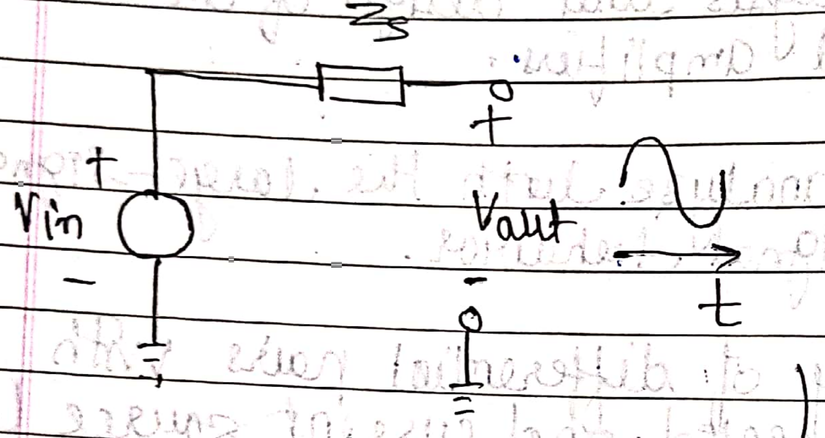
A single ended signal is defined as one that is measured w.r.t a fixed potential, usually the ground.

· A differential signal is defined as one that is measured betn two nodes that have equal and opposite signal excursions around a fixed potential.

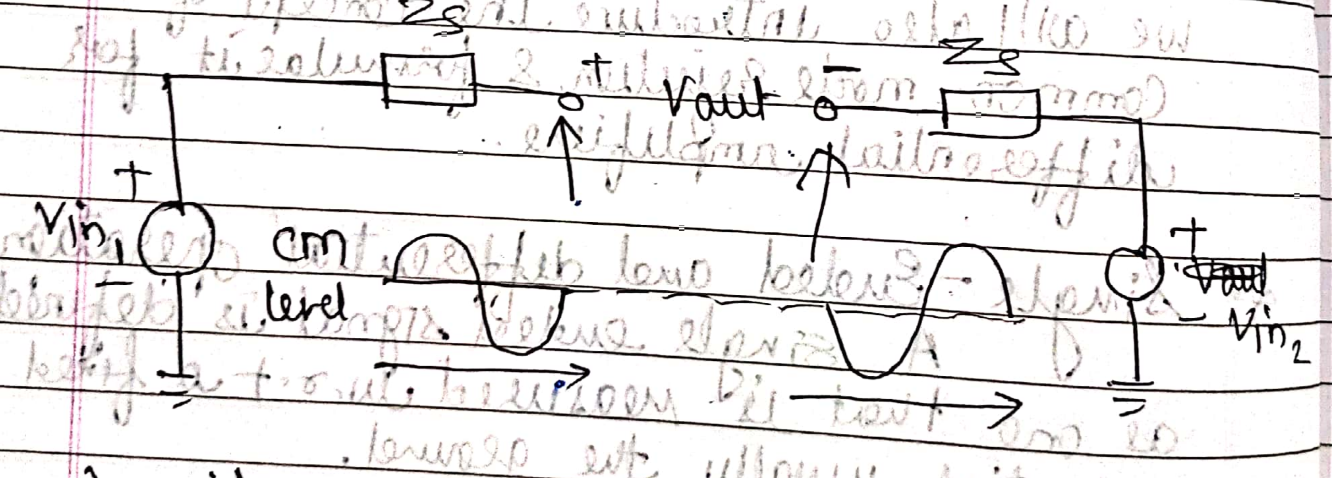
· In the strict sense, the two nodes must also exhibit equal impedances to that Potential.

As shown in fig 4. two types of signals conceptually

The "center" potential in differential signaling is called the "common-mode" (CM) level.




a) Single ended




b) differential signals

# * Basic differential pair

The dc transfer characteristics of a source-coupled pair.

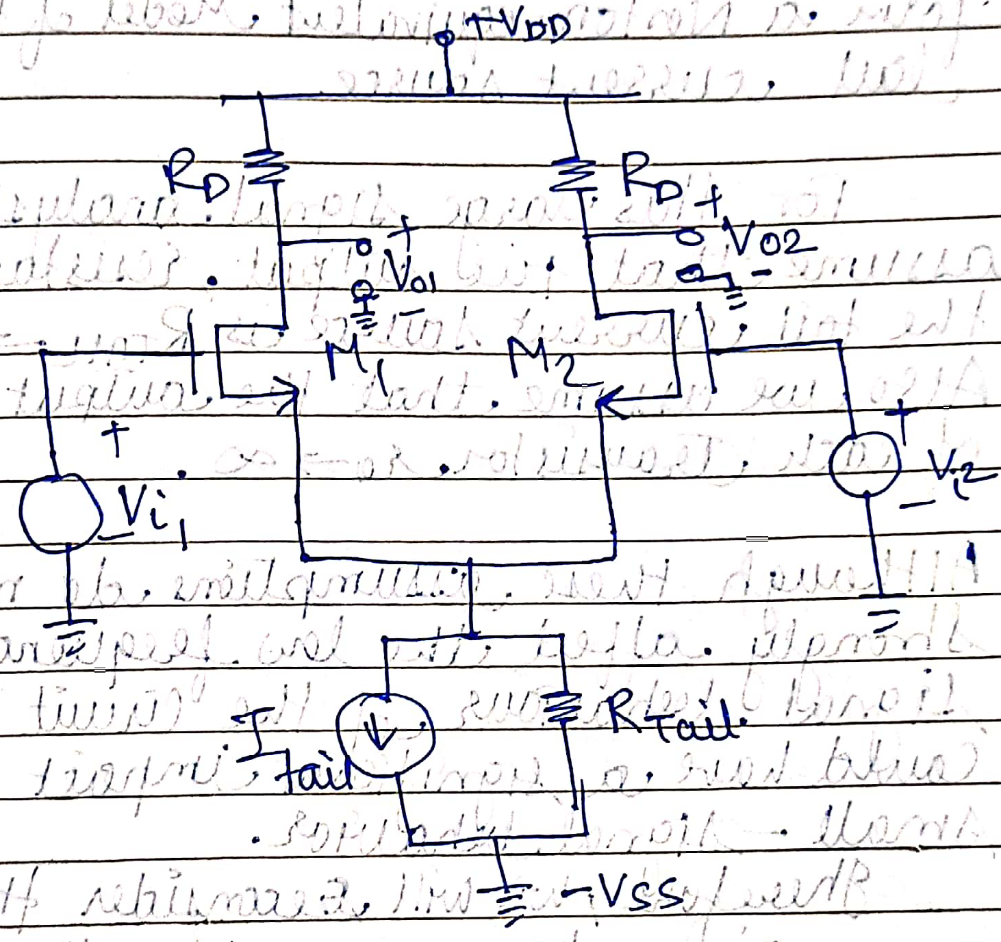



fig. n-channel MOSFET source coupled pair.

Consider the n-channel MOS transistor source coupled pair as shown in above fig.

The following analysis applies equally well to a corresponding p-channel source - coupled pair with appropriate sign changes.
In monolithic form, a transistor current source, called a tail current source, is

is usually connected to sources of $M_1$ & $M_2$, In that case $I_{TAIL}$ and $R_{TAIL}$ together form a Norton-equivalent Model of the tail current source.

For this large signal analysis, we assume that the output resistance of the tail current source is $R_{TAIL} \to \infty$. Also we assume that the output resistance of each Transistor $r_o \to \infty$.

Although these assumptions do not strongly affect the low frequency large signal behaviour of the circuit, they could have a significant impact on the small-signal behavior.

Therefore, we will reconsider these assumptions when we analyze the circuit from a small signal standpoint.

from KVL ~~around~~ around the input loop,

$$V_{i1} - V_{gs1} + V_{g2} - V_{i2} = 0 \quad -(1)$$

Transistor operates in non-saturation

$$V_{i1} \leq V_{DD} \;\&\; V_{i2} \leq V_{DD}$$

$$V_{gs1} = V_t + \sqrt{\frac{2 I_{d1}}{k'(W/L)}} \quad -(2)$$

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$$V_{gs2} = V_t + \sqrt{\frac{2I_{d2}}{k'(W/L)}} \quad —(3)$$

Substitute (2) & (3) into (1)

$$V_{id} = V_{i1} - V_{i2} = \frac{\sqrt{I_{d1}} - \sqrt{I_{d2}}}{\sqrt{\frac{k'}{2}\frac{W}{L}}} \quad —(4)$$

from KCL at the source $M_1$ & $M_2$

$$I_{d1} + I_{d2} = I_{TAIL} \quad —(5)$$

$$I_{d2} = I_{d1} - I_{TAIL}$$

Solving eq (5) for $I_{d2}$, substituting into (4)

$$x = \frac{-b \pm \sqrt{b^2-4ac}}{2a}$$

$$I_{d1} = \frac{I_{TAIL}}{2} \pm \frac{k'}{4}\frac{W}{L}V_{id}\sqrt{\frac{4I_{TAIL}}{k'(W/L)} - V_{id}^2} \quad —(6)$$

Since $I_{d1} > I_{TAIL}/2$ when $V_{id} > 0$, therefore − term can't be possible.

$$I_{d1} = \frac{I_{TAIL}}{2} + \frac{k'}{4}\frac{W}{L}V_{id}\sqrt{\frac{4I_{TAIL}}{k'(W/L)} - V_{id}^2} \quad —(7)$$

Substituting (6) into (5)

$$I_{d2} = \frac{I_{TAIL}}{2} - \frac{k'}{4}\frac{W}{L}V_{id}\sqrt{\frac{4I_{TAIL}}{k'(W/L)} - V_{id}^2} \quad —(8)$$

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eqn (7) & (8) are valid when both transistors operate in the active or saturation region.

We assume that neither transistor operates in the triode region.

When $M_1$ turns off, $I_{d_1} = 0$

$$I_{d_2} = I_{TAIL}$$

On other hand,

$I_{d_1} = I_{TAIL}$ & $I_{d_2} = 0$ when $M_2$ turns off.

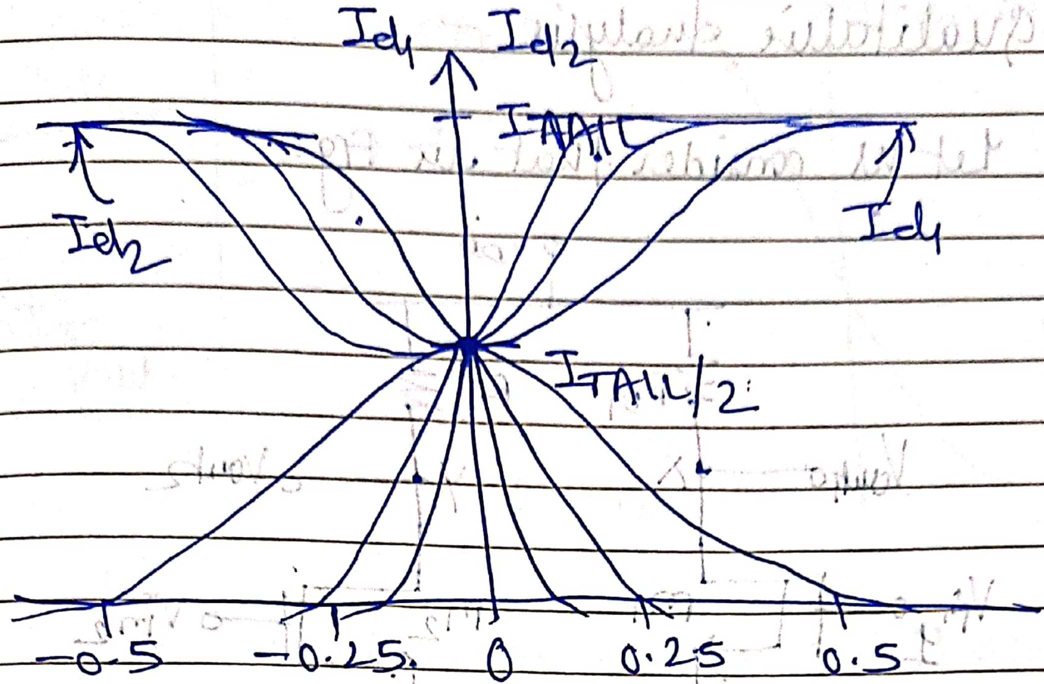
Substitute these values in eqn (4)

$$|V_{id}| \leq \sqrt{\frac{2 I_{TAIL}}{k'(W/L)}}$$

Since $I_{d_1} = I_{d_2} = I_{TAIL}/2$ when $V_{id} = 0$

$$|V_{id}| \leq \sqrt{2}\left(\sqrt{\frac{2 I_{d_1}}{k'(W/L)}}\right)\Bigg|_{V_{id}=0}$$

$$= \sqrt{2}\,(V_{ov})\Big|_{V_{id}=0}$$




dc transfer characteristics of the MOS source coupled pair.

(overdrive) $V_{OV} = V_{GS} - V_t$ determined when $V_{id} = 0$.

For differential o/p voltages

$V_{od} = V_{o1} - V_{o2} = V_{DD} - I_{d_1} R_D - V_{DD} + I_{d_2} R_D$

Since $\Delta I_d = 0$ when $V_{id} = 0$.

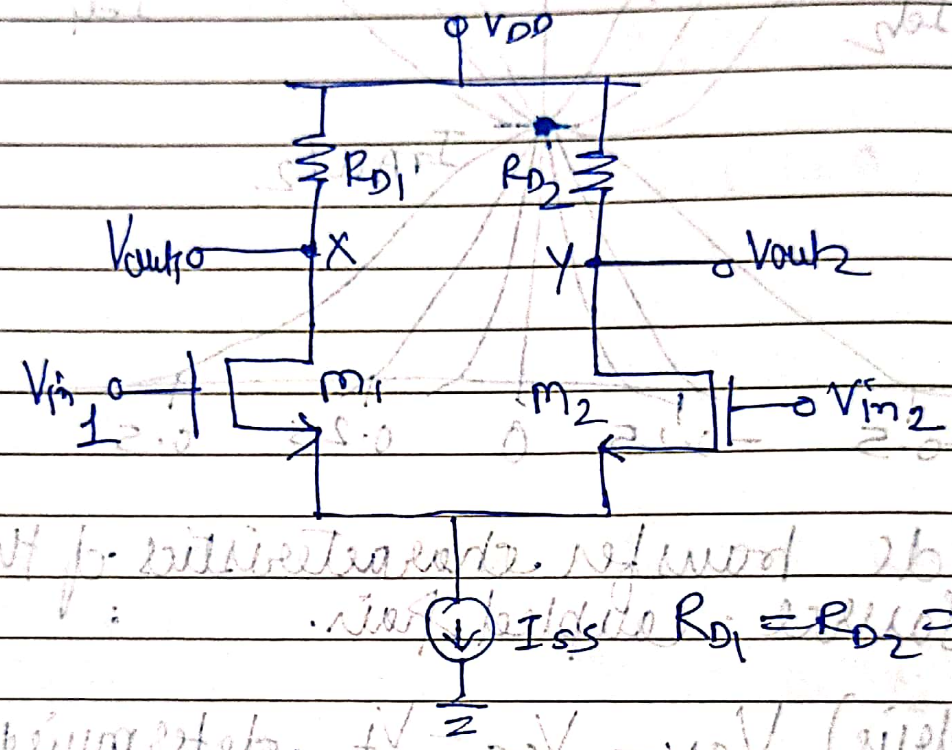
$V_{od} = 0$ when $V_{id} = 0$.

If $M_1$ & $M_2$ are identical & if identical resistors are connected to the drains of $M_1$ & $M_2$.

This property allows direct coupling of cascade MOS differential pairs as in bipolar case.

## Qualitative Analysis:-

Let us consider that in Fig.




$R_{D1} = R_{D2} = R_D$

Basic differential pair

$V_{in1} - V_{in2}$ varies from $-\infty$ to $\infty$

If $V_{in1}$ is much more negative than $V_{in2}$, $M_1$ is off, $M_2$ is on, & $I_{D2} = I_{SS}$

Thus $V_{out1} = V_{DD}$ and $V_{out2} = V_{DD} - R_D I_{SS}$

As $V_{in1}$ is brought closer to $V_{in2}$, $M_1$ gradually turns on, drawing a fraction of $I_{SS}$ from $R_{D1}$ & hence lowering $V_{out1}$.

Since $I_{D1} + I_{D2} = I_{SS}$, the drain current of $M_2$ decreases & $V_{out2}$ rises.

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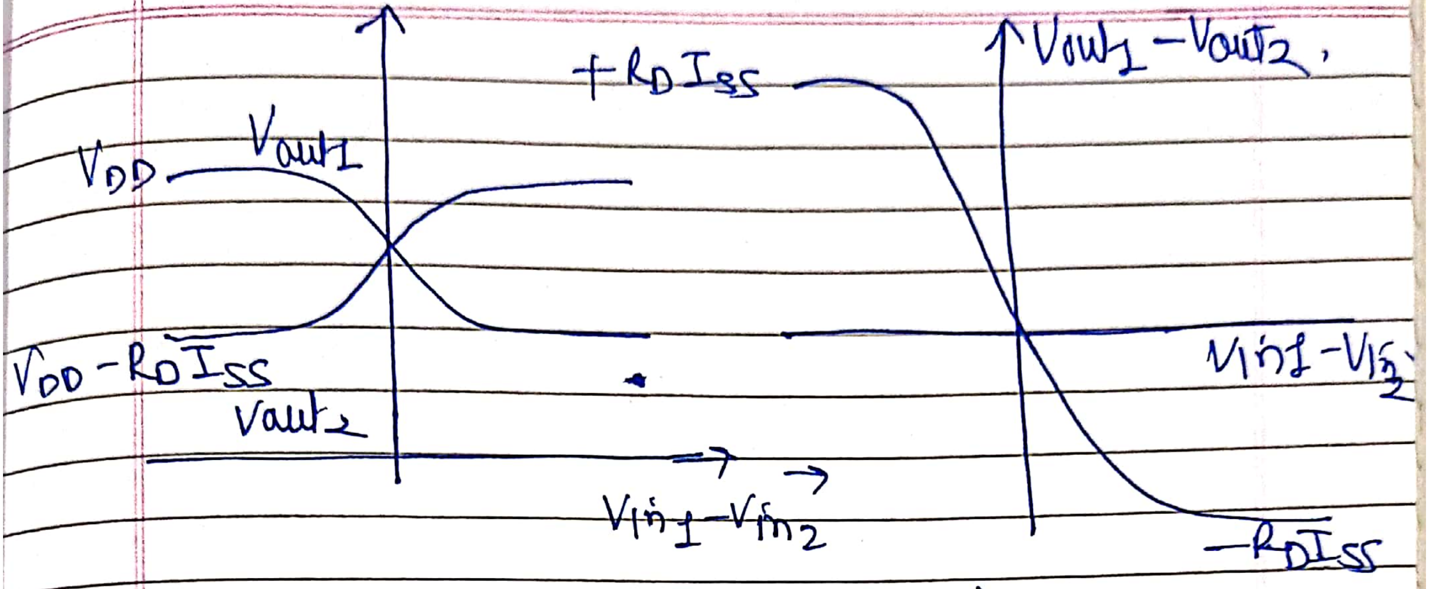


a) b)

I/P-O/P characteristics of a differential pair