

Figure 6.2 First-stage CMOS inverter with lumped output load capacitance.

6.2 Delay-Time Definitions

Before we begin the derivation of delay expressions, we will present some commonly used delay time definitions. The input and output voltage waveforms of a typical inverter circuit are shown in Fig. 6.3. The propagation delay times τ_{PHL} and τ_{PLH} determine the input-to-output signal delay during the high-to-low and low-to-high transitions of the output, respectively. By definition, τ_{PHL} is the time delay between the $V_{50\%}$ -transition of the *rising* input voltage and the $V_{50\%}$ -transition of the *falling* output voltage. Similarly, τ_{PLH} is defined as the time delay between the $V_{50\%}$ -transition of the *falling* input voltage and the $V_{50\%}$ -transition of the *rising* output voltage.

To simplify the analysis and the derivation of delay expressions, the input voltage waveform is usually assumed to be an ideal step pulse with zero rise and fall times. Under this assumption, τ_{PHL} becomes the time required for the output voltage to fall from V_{OH} to the $V_{50\%}$ level, and τ_{PLH} becomes the time required for the output voltage to rise from V_{OL} to the $V_{50\%}$ level. The voltage point $V_{50\%}$ is defined as follows.

$$V_{50\%} = V_{OL} + \frac{1}{2}(V_{OH} - V_{OL}) = \frac{1}{2}(V_{OL} + V_{OH}) \quad (6.2)$$

Thus, the propagation delay times τ_{PHL} and τ_{PLH} are found from Fig. 6.3 as

$$\begin{aligned} \tau_{PHL} &= t_1 - t_0 \\ \tau_{PLH} &= t_3 - t_2 \end{aligned} \quad (6.3)$$

The average propagation delay τ_P of the inverter characterizes the average time required for the input signal to propagate through the inverter.

$$\tau_P = \frac{\tau_{PHL} + \tau_{PLH}}{2} \quad (6.4)$$

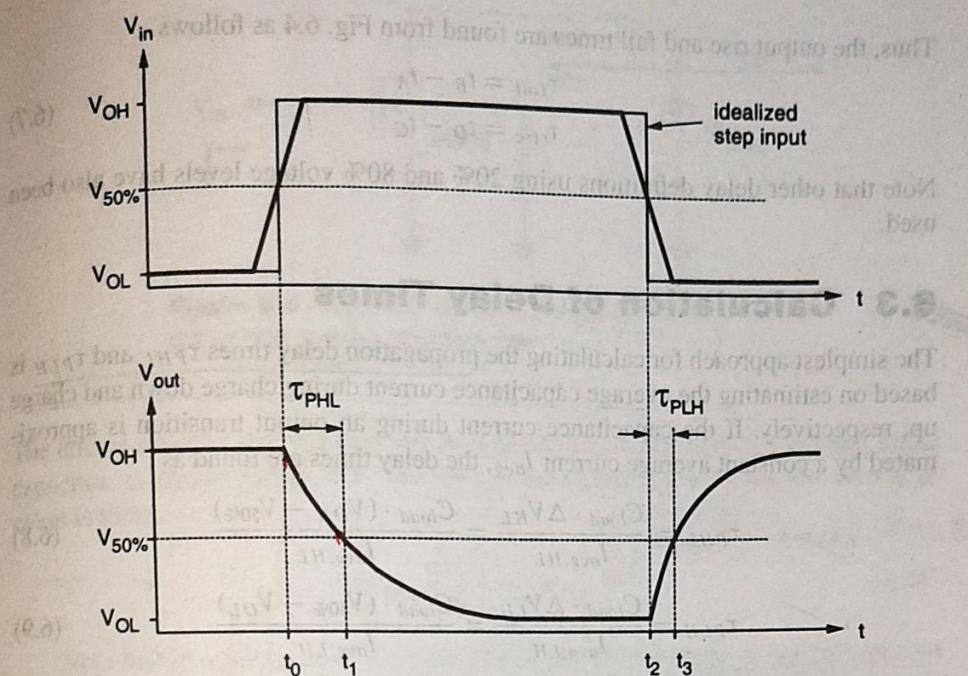


Figure 6.3 Input and output voltage waveforms of a typical inverter, and the definitions of propagation delay times. The input voltage waveform is idealized as a step pulse for simplicity.

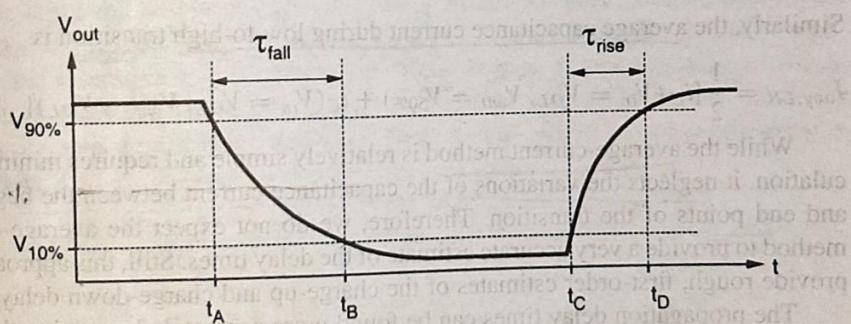


Figure 6.4 Output voltage rise and fall times.

→ We will refer to Fig. 6.4 for the definition of output voltage rise and fall times. The rise time τ_{rise} is defined here as the time required for the output voltage to rise from the $V_{10\%}$ level to $V_{90\%}$ level. Similarly, the fall time τ_{fall} is defined here as the time required for the output voltage to drop from the $V_{90\%}$ level to $V_{10\%}$ level. The voltage levels $V_{10\%}$ and $V_{90\%}$ are defined as

$$V_{10\%} = V_{OL} + 0.1 \cdot (V_{OH} - V_{OL}) \quad (6.5)$$

$$V_{90\%} = V_{OL} + 0.9 \cdot (V_{OH} - V_{OL}) \quad (6.6)$$

Thus, the output rise and fall times are found from Fig. 6.4 as follows.

$$\tau_{fall} = t_B - t_A \quad (6.7)$$

$$\tau_{rise} = t_D - t_C$$

Note that other delay definitions using 20% and 80% voltage levels have also been used.

6.3 Calculation of Delay Times

The simplest approach for calculating the propagation delay times τ_{PHL} and τ_{PLH} is based on estimating the average capacitance current during charge down and charge up, respectively. If the capacitance current during an output transition is approximated by a constant average current I_{avg} , the delay times are found as

$$\checkmark \quad \tau_{PHL} = \frac{C_{load} \cdot \Delta V_{HL}}{I_{avg,HL}} = \frac{C_{load} \cdot (V_{OH} - V_{50\%})}{I_{avg,HL}} \quad (6.8)$$

$$\checkmark \quad \tau_{PLH} = \frac{C_{load} \cdot \Delta V_{LH}}{I_{avg,LH}} = \frac{C_{load} \cdot (V_{50\%} - V_{OL})}{I_{avg,LH}} \quad (6.9)$$

Note that the average current during high-to-low transition can be calculated by using the current values at the beginning and the end of the transition.

$$I_{avg,HL} = \frac{1}{2} [i_C(V_{in} = V_{OH}, V_{out} = V_{OH}) + i_C(V_{in} = V_{OH}, V_{out} = V_{50\%})] \quad (6.10)$$

Similarly, the average capacitance current during low-to-high transition is

$$I_{avg,LH} = \frac{1}{2} [i_C(V_{in} = V_{OL}, V_{out} = V_{50\%}) + i_C(V_{in} = V_{OL}, V_{out} = V_{OL})] \quad (6.11)$$

While the average-current method is relatively simple and requires minimal calculation, it neglects the variations of the capacitance current between the beginning and end points of the transition. Therefore, we do not expect the average-current method to provide a very accurate estimate of the delay times. Still, this approach can provide rough, first-order estimates of the charge-up and charge-down delay times.

The propagation delay times can be found more accurately by solving the state equation of the output node in the time domain. The differential equation associated with the output node is given below. Note that the capacitance current is also a function of the output voltage.

$$C_{load} \frac{dV_{out}}{dt} = i_C = i_{D,p} - i_{D,n} \quad (6.12)$$

First, we consider the rising-input case for a CMOS inverter. Initially, the output voltage is assumed to be equal to V_{OL} . When the input voltage switches from low (V_{OL}) to high (V_{OH}), the nMOS transistor is turned on and it starts to discharge the load capacitance. At the same time, the pMOS transistor is switched off; thus,

$$i_{D,p} \approx 0 \quad (6.13)$$

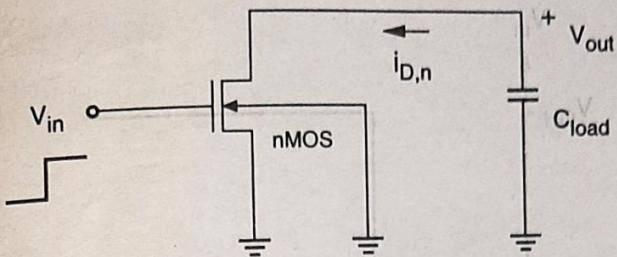


Figure 6.5 Equivalent circuit of the CMOS inverter during high-to-low output transition.

The circuit given in Fig. 6.2 can now be reduced to a single nMOS transistor and a capacitor, as shown in Fig. 6.5. The differential equation describing the discharge event is then

$$C_{load} \frac{dV_{out}}{dt} = -i_{D,n} \quad (6.14)$$

*to calculate
charge-down time*

Note that in other types of inverter circuits, such as the resistive-load inverter or the depletion-load inverter, the load device continues to conduct a nonzero current when the input is switched from low to high. However, the load current is usually negligible in comparison to the driver current. Therefore, (6.14) can be used to calculate the charge-down time not only in CMOS inverters, but also in almost all common types of inverter circuits.

The input and output voltage waveforms during this high-to-low transition are illustrated in Fig. 6.6. When the nMOS transistor starts conducting, it initially operates in the saturation region. When the output voltage falls below $(V_{DD} - V_{T,n})$, the nMOS transistor starts to conduct in the linear region. These two operating regions are also shown in Fig. 6.6. First, consider the nMOS transistor operating in saturation.

$$i_{D,n} = \frac{k_n}{2} (V_{in} - V_{T,n})^2$$

$$= \frac{k_n}{2} (V_{OH} - V_{T,n})^2, \quad \text{for } V_{OH} - V_{T,n} < V_{out} \leq V_{OH} \quad (6.15)$$

Since the saturation current is practically independent of the output voltage (neglecting channel-length modulation), the solution of (6.14) in the time interval between t_0 and t'_1 can be found as

$$\int_{t=t_0}^{t=t'_1} dt = -C_{load} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} \left(\frac{1}{i_{D,n}} \right) dV_{out}$$

$$= -\frac{2C_{load}}{k_n(V_{OH} - V_{T,n})^2} \int_{V_{out}=V_{OH}}^{V_{out}=V_{OH}-V_{T,n}} dV_{out} \quad (6.16)$$

$$-\frac{C_{load}}{i_{D,n}} dV_{out} = dt$$

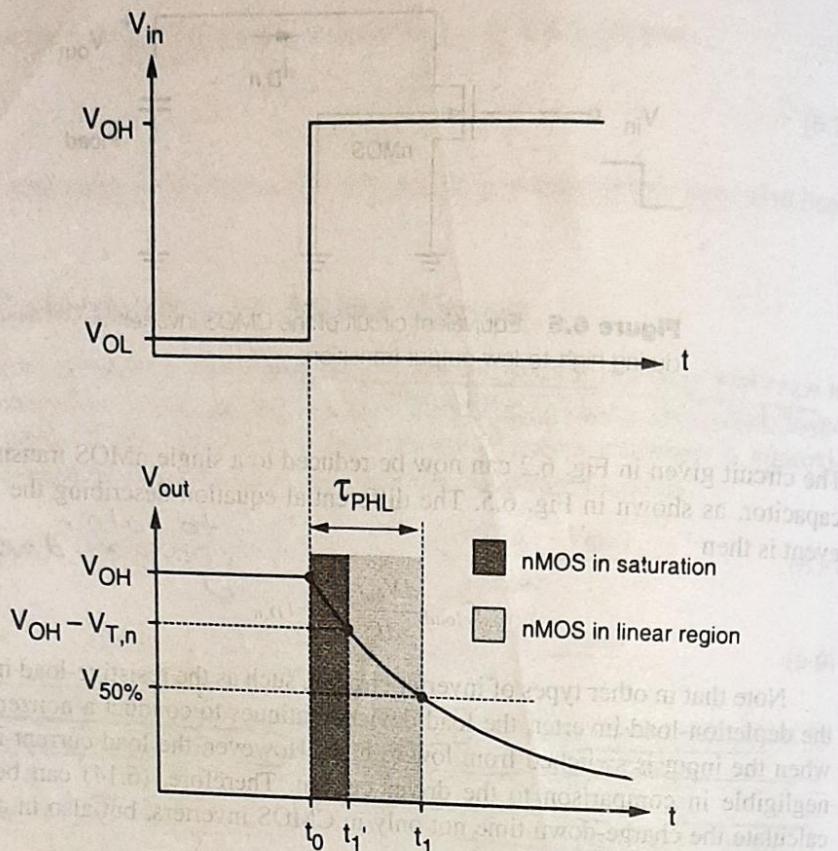


Figure 6.6 Input and output voltage waveforms during high-to-low transition.

Evaluating this simple integral yields

$$t'_1 - t_0 = \frac{2C_{load}V_{T,n}}{k_n(V_{OH} - V_{T,n})^2} \quad (6.17)$$

At $t = t'_1$, the output voltage will be equal to $(V_{DD} - V_{T,n})$ and the transistor will be at the saturation-linear region boundary. Next, consider the nMOS transistor operating in the linear region.

$$\begin{aligned} i_{D,n} &= \frac{k_n}{2} [2(V_{in} - V_{T,n})V_{out} - V_{out}^2] \\ &= \frac{k_n}{2} [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2], \quad \text{for } V_{out} \leq V_{OH} - V_{T,n} \end{aligned} \quad (6.18)$$

The solution of (6.14) in the time interval between t'_1 and t_1 can be found as

$$\begin{aligned} \int_{t=t'_1}^{t=t_1} dt &= -C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{i_{D,n}} \right) dV_{out} \\ &= -2 C_{load} \int_{V_{out}=V_{OH}-V_{T,n}}^{V_{out}=V_{50\%}} \left(\frac{1}{k_n [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2]} \right) dV_{out} \end{aligned} \quad (6.19)$$

$\frac{1}{V_{out} - (2V_{OH} - V_{T,n})}$

Evaluating this integral yields

$$t_1 - t'_1 = -\frac{2C_{load}}{k_n} \frac{1}{2(V_{OH} - V_{T,n})} \ln \left(\frac{V_{out}}{2(V_{OH} - V_{T,n}) - V_{out}} \right) \Big|_{V_{out}=V_{50\%}}^{V_{out}=V_{OH}-V_{T,n}} \quad (6.20)$$

$$\underline{t_1 - t'_1 = \frac{C_{load}}{k_n(V_{OH} - V_{T,n})} \ln \left(\frac{2(V_{OH} - V_{T,n}) - V_{50\%}}{V_{50\%}} \right)} \quad (6.21)$$

Finally, the propagation delay time for high-to-low output transition (τ_{PHL}) can be found by combining (6.17) and (6.21):

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{OH} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{OH} - V_{T,n}} + \ln \left(\frac{4(V_{OH} - V_{T,n})}{V_{OH} + V_{OL}} - 1 \right) \right] \quad (6.22a)$$

For $V_{OH} = V_{DD}$ and $V_{OL} = 0$, as is the case for the CMOS inverter, (6.22a) becomes:

$$\tau_{PHL} = \frac{C_{load}}{k_n(V_{DD} - V_{T,n})} \left[\frac{2V_{T,n}}{V_{DD} - V_{T,n}} + \ln \left(\frac{4(V_{DD} - V_{T,n})}{V_{DD}} - 1 \right) \right] \quad (6.22b)$$

Consider the CMOS inverter circuit shown in Fig. 6.2, with $V_{DD} = 3.3$ V. The $I-V$ characteristics of the nMOS transistor are specified as follows: when $V_{GS} = 3.3$ V, the drain current reaches its saturation level $I_{sat} = 2$ mA for $V_{DS} \geq 2.5$ V. Assume that the input signal applied to the gate is a step pulse that switches instantaneously from 0 V to 3.3 V. Using the data above, calculate the delay time necessary for the output to fall from its initial value of 3.3 V to 1.65 V, assuming an output load capacitance of 300 fF.

For the solution, consider the simplified pull-down circuit shown in Fig. 6.5. We will assume that the nMOS transistor operates in saturation from $t = 0$ to $t = t'_1 = t_{sat}$, and that it will operate in the linear region from $t = t'_1 = t_{sat}$ to $t = t_2 = t_{delay}$. We can also deduce from the $I-V$ characteristics that $V_{T,n} = 0.8$ V, since the nMOS transistor enters saturation when $V_{DS} \geq V_{GS} - V_{T,n}$. The voltage V_{GS} is equal to 3.3 V for $t \geq 0$.

The current equation for the saturation region can be written as

$$C \frac{dV_{out}}{dt} = -I_D = -I_{sat} = -\frac{1}{2} k_n (V_{OH} - V_{T,n})^2$$

We can calculate the amount of time in which the nMOS transistor operates in saturation (t_{sat}), by integrating this equation.

$$\int_{t=0}^{t=t_{sat}} dt = - \int_{V_{out}=3.3}^{V_{out}=2.5} \frac{C}{I_D} dV_{out}$$

$$t_{sat} = \frac{V_{T,n} C}{I_{sat}} = \frac{0.8 \text{ V} \cdot 300 \text{ fF}}{2 \text{ mA}} = 120 \text{ [ps]}$$

The transconductance k_n of the nMOS transistor can be found as follows:

$$k_n = \frac{2I_{sat}}{(V_{OH} - V_{T,n})^2} = \frac{2 \times 2 \times 10^{-3}}{(3.3 - 0.8)^2} = 0.640 \times 10^{-3} [\text{A/V}^2]$$

Now, the current equation for the linear operating region is

$$C \frac{dV_{out}}{dt} = -I_D = -\frac{1}{2} k_n [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2]$$

Integrating this differential equation between the two voltage boundary conditions yields the time in which the nMOS transistor operates in the linear region during this transition.

$$\begin{aligned} \int_{t=t_{sat}}^{t=t_{delay}} dt &= -2C \int_{V_{out}=2.5}^{V_{out}=1.65} \frac{dV_{out}}{k_n [2(V_{OH} - V_{T,n})V_{out} - V_{out}^2]} \\ t_{delay} - t_{sat} &= -\frac{C}{k_n (V_{OH} - V_{T,n})} \ln \left(\frac{V_{out}}{2(V_{OH} - V_{T,n}) - V_{out}} \right) \Big|_{V_{out}=2.5}^{V_{out}=1.65} \\ &= \frac{C}{k_n (V_{OH} - V_{T,n})} \\ &\quad \times \left[\ln \left(\frac{2(V_{OH} - V_{T,n}) - V_{1.65}}{V_{1.65}} \right) - \ln \left(\frac{2(V_{OH} - V_{T,n}) - V_{2.5}}{V_{2.5}} \right) \right] \\ &= \frac{0.3 \times 10^{-12}}{0.640 \times 10^{-3} (3.3 - 0.8)} \left[\ln \left(\frac{5 - 1.65}{1.65} \right) - \ln \left(\frac{5 - 2.5}{2.5} \right) \right] \\ &= 133 [\text{ps}] \end{aligned}$$

Thus, the total delay time is found to be

$$t_{delay} = 120 + 133 = 253 [\text{ps}]$$

Note that t_{delay} corresponds to the propagation delay time τ_{PHL} for falling output.

The average-current method presented earlier in this Section can also be used to estimate the propagation delay times as well as the rise and fall times of inverter circuits. This simple approach can in some cases produce fairly accurate first-order results, as presented in the following example.

EXAMPLE 6.2

For the CMOS inverter shown in Fig. 6.2 with a power supply voltage of $V_{DD} = 5 \text{ V}$, determine the fall time τ_{fall} , which is defined as the time elapsed between the time point at which $V_{out} = V_{90\%} = 4.5 \text{ V}$ and the time point at which $V_{out} = V_{10\%} = 0.5 \text{ V}$. Use both the average-current method and the differential equation method for

calculating τ_{fall} . The output load capacitance is 1 pF. The nMOS transistor parameters are given as

$$\mu_n C_{ox} = 20 \mu\text{A/V}^2$$

$$(W/L)_n = 10$$

$$V_{T,n} = 1.0 \text{ V}$$

Using a simple expression similar to (6.10), we can determine the average capacitor current during the charge-down event described earlier.

$$\begin{aligned} I_{avg} &= \frac{1}{2}[I(V_{in} = 5 \text{ V}, V_{out} = 4.5 \text{ V}) + I(V_{in} = 5 \text{ V}, V_{out} = 0.5 \text{ V})] \\ &= \frac{1}{2} \left[\frac{1}{2} k_n (V_{in} - V_{T,n})^2 + \frac{1}{2} k_n (2(V_{in} - V_{T,n})V_{out} - V_{out}^2) \right] \\ &= \frac{1}{2} \cdot \frac{1}{2} \cdot 20 \times 10^{-6} \cdot 10[(5 - 1)^2 + (2(5 - 1)0.5 - 0.5^2)] = 0.9875 \text{ [mA]} \end{aligned}$$

The fall time is then found as

$$\tau_{fall} = \frac{C \cdot \Delta V}{I_{avg}} = \frac{1 \times 10^{-12}(4.5 - 0.5)}{0.9875 \times 10^{-3}} = 4.05 \times 10^{-9} \text{ [s]} = 4.05 \text{ [ns]}$$

Now, we will recalculate the fall time using the differential equation approach. The nMOS transistor operates in the saturation region for $4.0 \text{ V} \leq V_{out} \leq 4.5 \text{ V}$. Writing the current equation for the saturation region, we obtain

$$C \frac{dV_{out}}{dt} = -\frac{1}{2} k_n (V_{in} - V_{T,n})^2, \quad \text{where } k_n = \mu_n C_{ox} \left(\frac{W}{L} \right)_n$$

$$\frac{dV_{out}}{dt} = \frac{-20 \times 10^{-6} \cdot 10 \cdot (5 - 1)^2}{2 \cdot 1 \times 10^{-12}} = -1.6 \times 10^9 \text{ [V/s]}$$

Integrating this simple expression yields the time during which the nMOS transistor operates in saturation.

$$\int_{t=0}^{t=t_{sat}} dt = -\frac{1}{1.6 \times 10^9} \int_{V_{out}=4.5}^{V_{out}=4} dV_{out}$$

$$t_{sat} = \frac{0.5}{1.6 \times 10^9} = 0.3125 \times 10^{-9} \text{ [s]} = 0.3125 \text{ [ns]}$$

The nMOS transistor operates in the linear region for $0.5 \text{ V} \leq V_{out} \leq 4.0 \text{ V}$. The current equation for this operating region is written as follows:

$$C \frac{dV_{out}}{dt} = -\frac{1}{2} k_n [2(V_{in} - V_{T,n})V_{out} - V_{out}^2]$$

Derivation for Fall Time (t_f)

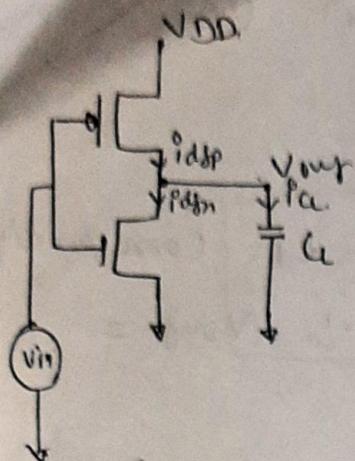
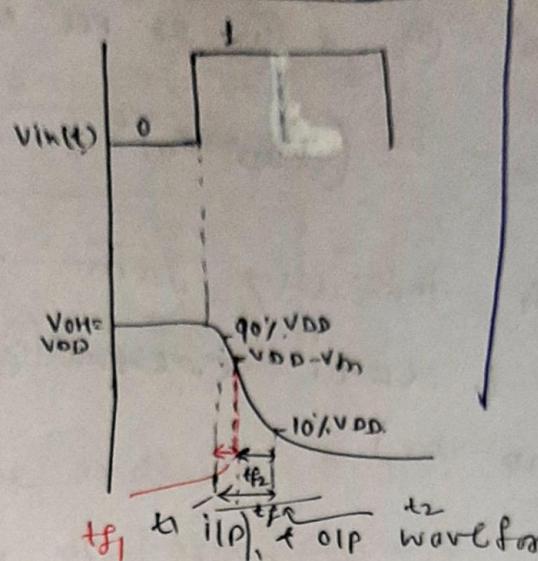


Fig: 1 common inverter



$$\therefore \text{Total falltime} = t_f = t_{f1} + t_{f2}$$

from Fig 2 t_{f1} = period during which the capacitor voltage V_{out} drops from $0.9V_{DD}$ to $V_{DD} - V_m$

t_{f2} = period during which the capacitor voltage V_{out} drops from $V_{DD} - V_m$ to $0.1V_{DD}$

$$-i_{Dp} + i_{Cl} + i_{DSn} = 0$$

$$\therefore \underline{i_{Dp} = 0}$$

$$\therefore \underline{i_{Cl} = -i_{DSn}} \quad \text{--- (1)}$$

$$i_{Cl} = C \frac{dV_{out}}{dt} \quad \text{--- (2)}$$

from $90\%V_{DD} \rightarrow V_{DD} - V_m$ nmos work in saturation

$$\therefore i_{DSn}(\text{sat}) = \frac{L \mu n}{2} (V_{GSn} - V_m)^2 \quad \text{--- (3)}$$

$$\therefore V_{GSn} = V_{in} = V_{DD}$$

$$\therefore i_{DSn}(\text{sat}) = \frac{L \mu n}{2} (V_{DD} - V_m)^2 \quad \text{--- (4)}$$

equating eqn ② & ④ as per eqn ①

$$C_L \cdot \frac{dV_{out}}{dt} = -\frac{k_n}{2} (V_{DD} - V_{thn})^2$$

to determine t_{f1} integrating from $t=t_1$ corresponding to $V_{out} = 0.9V_{DD}$ to $t=t_1$ corresponding to $V_{out} = (V_{DD} - V_{thn})$

$$\therefore C_L \cdot \frac{dV_{out}}{dt} = -\frac{k_n}{2} (V_{DD} - V_{thn})^2$$

$$\therefore dt = -\frac{2 \cdot C_L \cdot dV_{out}}{k_n (V_{DD} - V_{thn})^2} \quad \text{--- (5)}$$

integrating both the sides of eqn ⑤

$$\int_{t=t_1}^{t_1} dt = - \int_{V_{DD}-V_{thn}}^{0.9V_{DD}} \frac{2 \cdot C_L \cdot dV_{out}}{k_n \cdot (V_{DD} - V_{thn})^2}$$

$$V_{out} = 0.9V_{DD}$$

interchanging the limits of integration

$$t_{f1} = \frac{2 \cdot C_L}{k_n (V_{DD} - V_{thn})^2} \int_{V_{DD}-V_{thn}}^{0.9V_{DD}} dV_{out} = \frac{2 \cdot C_L}{k_n (V_{DD} - V_{thn})^2} \left[V_{out} \right]_{V_{DD}-V_{thn}}^{0.9V_{DD}}$$
$$= \frac{2 \cdot C_L}{k_n (V_{DD} - V_{thn})^2} [0.9V_{DD} - V_{DD} + V_{thn}]$$

$$t_{f1} = \frac{2 \cdot C_L (V_{thn} - 0.1V_{DD})}{k_n (V_{DD} - V_{thn})} \quad \text{--- (6)}$$

$$1. \quad t_{f1} = 3.6975 \text{ ns}$$

- taking V_{DD} common from N^r & n^r from P_{H,S}

$$= \frac{2 \cdot C_L V_{DD} \left(\frac{V_m}{V_{DD}} - 0.1 \right)}{V_{DD} V_{DD} (1 - V_m/V_{DD})^2}$$

$$J_{f1} = \frac{2 \cdot C_L (n - 0.1)}{V_{DD} (1 - n)^2} \quad \text{--- (7)}$$

$$n = \frac{V_m}{V_{DD}}$$

for t_{f2} the n-device begins to operate in the linear region, the discharge current is no longer constant. The time t_{f2} taken to discharge the capacitor voltage from (V_{DD} - V_m) to 0.1 V_{DD} can be obtained. (time from t_i to t_{f2})

$$i_C = -i_{dgm}(1_{in}) \quad \text{--- (8)}$$

$$\therefore C_L \frac{dv_{out}}{dt} = -\frac{k_n}{2} \left[2(V_{GS} - V_{dm}) \cdot V_{dsh} - V_{dgm}^2 \right]$$

$$C_L \frac{dv_{out}}{dt} = -\frac{k_n}{2} \left[2(V_{DD} - V_{dm}) \cdot V_{out} - V_{out}^2 \right]$$

$$dt = \frac{-C_L dV_{out}}{k_n [2(V_{DD} - V_{dm}) \cdot V_{out} - V_{out}^2]} \quad \text{--- (9)}$$

taking integration of both the sides of eqn (9)

$$\int_{t_i}^{t_2} dt = \int_{0.1V_{DD}}^{0.1V_{DD}} \frac{-2 \cdot C_L \cdot dV_{out}}{k_n [2(V_{DD} - V_{dm}) \cdot V_{out} - V_{out}^2]} \quad \text{--- (10)}$$

$$V_{out} = V_{DD} - V_m$$

$$= \frac{2 \cdot C_L}{k_n} \int_{0.1V_{DD}}^{V_{DD} - V_m} \frac{dV_{out}}{2(V_{DD} - V_m) \cdot V_{out} - V_{out}^2}$$

equating eqn ② & ④ as per eqn ①

$$C_L \cdot \frac{dV_{out}}{dt} = -\frac{k_n}{2} (V_{DD} - V_{in})^2$$

To determine t_{f_1} integrating from $t=t_1$ corresponding to $V_{out} = 0.9V_{DD}$ to $t=t_1$ corresponding to $V_{out} = (V_{DD} - V_{in})$

$$C_L \cdot \frac{dV_{out}}{dt} = -\frac{k_n}{2} (V_{DD} - V_{in})^2$$

$$dt = -\frac{2 C_L \cdot dV_{out}}{k_n (V_{DD} - V_{in})^2} \quad \text{--- (5)}$$

integrating both the sides of eqn (5)

$$\int_{t=t_1}^{t_1} dt = - \int_{V_{DD} - V_{in}}^{0.9V_{DD}} \frac{2 \cdot C_L \cdot dV_{out}}{k_n \cdot (V_{DD} - V_{in})^2}$$

$$V_{out} = 0.9V_{DD}$$

interchanging the limits of integration

$$+t_{f_1} = \frac{2 \cdot C_L}{k_n (V_{DD} - V_{in})} \int_{V_{DD} - V_{in}}^{0.9V_{DD}} dV_{out} = \frac{2 \cdot C_L}{k_n (V_{DD} - V_{in})^2} \left[V_{out} \right]_{V_{DD} - V_{in}}^{0.9V_{DD}}$$

$$= \frac{2 \cdot C_L}{k_n (V_{DD} - V_{in})^2} [0.9V_{DD} - V_{DD} + V_{in}]$$

$$+t_{f_1} = \frac{2 \cdot C_L (V_{in} - 0.1V_{DD})}{k_n (V_{DD} - V_{in})} \quad \text{--- (6)}$$

taking V_{DD} common from N^r & O^r from RHS

$$= \frac{2 \cdot C_L V_{DD} \left(\frac{V_m}{V_{DD}} - 0.1 \right)}{V_{DD} V_{DD} (1 - V_m/V_{DD})^2}$$

$$\boxed{t_f = \frac{2 \cdot C_L (n - 0.1)}{V_{DD} (1 - n)^2}} \quad - (7)$$

$$n = \frac{V_m}{V_{DD}}$$

for t_f , the n-device begins to operate in the linear region, the discharge current is no longer constant. The time t_f taken to discharge the capacitor voltage from $(V_{DD} - V_m)$ to $0.1 V_{DD}$ can be obtained. (time from $t_1 \rightarrow t_2$)

$$i_C = -i_{dgn}(1in) \quad - (8)$$

$$\therefore C_L \frac{dV_{out}}{dt} = -\frac{k_n}{2} \left[2(V_{GS} - V_m) \cdot V_{dsh} - V_{dsh}^2 \right]$$

$$C_L \frac{dV_{out}}{dt} = -\frac{k_n}{2} \left[2(V_{DD} - V_m) \cdot V_{out} - V_{out}^2 \right]$$

$$dt = \frac{-C_L dV_{out}}{k_n [2(V_{DD} - V_m) \cdot V_{out} - V_{out}^2]} \quad - (9)$$

taking integration of both the sides of eqn (9)

$$\int_{t_1}^{t_2} dt = \left\{ \begin{array}{l} -2 \cdot C_L \cdot dV_{out} \\ \hline k_n [2(V_{DD} - V_m) \cdot V_{out} - V_{out}^2] \end{array} \right\} \quad - (10)$$

$$V_{out} = V_{DD} - V_m$$

$$= \frac{2 \cdot C_L}{k_n} \int_{0.1 V_{DD}}^{V_{DD} - V_m} \frac{dV_{out}}{2(V_{DD} - V_m) \cdot V_{out} - V_{out}^2}$$

$$= \frac{2 \cdot C}{L_n} \left| \frac{V_{DD}-V_{IN}}{V_{DD} \left[2(V_{DD}-V_{IN}) - V_{OUT} \right]} \right|^2$$

$$= \frac{2 \cdot C}{L_n} \left\{ \frac{V_{DD}-V_{IN}}{V_{DD}} \left[\frac{A}{V_{OUT}} + \frac{B}{2(V_{DD}-V_{IN})-V_{OUT}} \right] \cdot V_{OUT} \right\}$$

= by Partial Fraction Expansion Method

$$\frac{1}{V_{OUT} \left(2(V_{DD}-V_{IN}) - V_{OUT} \right)} = \frac{A}{V_{OUT}} + \frac{B}{2(V_{DD}-V_{IN}) - V_{OUT}}$$

$$\therefore A \left(\frac{2(V_{DD}-V_{IN})}{V_{OUT}} \right) + B \cdot V_{OUT} = 1 \quad (1)$$

to calculate A put $V_{OUT}=0$ in equⁿ (1)

$$\therefore A = \frac{1}{2(V_{DD}-V_{IN})}$$

to calculate B put $V_{OUT} = 2(V_{DD}-V_{IN})$ in equⁿ (1)

$$\therefore B = \frac{1}{2(V_{DD}-V_{IN})}$$

$$= \frac{2 \cdot C}{L_n} \left| \frac{V_{DD}-V_{IN}}{V_{DD} \left[\frac{1}{V_{OUT}} + \frac{1}{2(V_{DD}-V_{IN})-V_{OUT}} \right]} \right|^2$$

$$= \frac{2 \cdot C}{2 \cdot (V_{DD}-V_{IN}) \cdot L_n} \left[\frac{V_{DD}-V_{IN}}{V_{DD}} \left(\frac{1}{V_{OUT}} + \frac{1}{2(V_{DD}-V_{IN})-V_{OUT}} \right) \right]^2$$

$$= \frac{C}{L_n \cdot (V_{DD}-V_{IN})} \left[\frac{V_{DD}-V_{IN}}{V_{DD}} \left(\frac{1}{V_{OUT}} - \frac{1}{V_{OUT}-2(V_{DD}-V_{IN})} \right) \right]^2$$

$$= \frac{2 \cdot C_L}{k_m \cdot (V_{DD} - V_{TH})} \left[\ln\left(\frac{V_{DD}}{V_{DD} - 2(V_{DD} - V_{TH})}\right) - \ln\left(\frac{V_{DD}}{V_{DD} - 2(V_{DD} - V_{TH})}\right) \right]$$

$$= \frac{2 \cdot C_L}{k_m \cdot (V_{DD} - V_{TH})} \left[\ln\left(\frac{V_{DD}}{\frac{V_{DD}}{V_{DD} - 2(V_{DD} - V_{TH})}}\right) \right] \frac{V_{DD} - V_{TH}}{0.1(V_{DD})}$$

$$= \frac{2 \cdot C_L}{k_m \cdot 2(V_{DD} - V_{TH})} \left[\ln\left(\frac{\frac{V_{DD} - V_{TH}}{(V_{DD} - V_{TH}) - 2(V_{DD} - V_{TH})}}{2(V_{DD} - V_{TH})}\right) - \ln\left(\frac{0.1V_{DD}}{0.1 - 2(V_{DD} - V_{TH})}\right) \right]$$

$$= \frac{C_L}{k_m \cdot (V_{DD} - V_{TH})} \left\{ \ln\left(\frac{(V_{DD} - V_{TH})}{-(V_{DD} - V_{TH})}\right) - \ln\left(\frac{0.1V_{DD}}{-1.9V_{DD} + 2V_{TH}}\right) \right\}$$

$$= \frac{C_L}{k_m \cdot (V_{DD} - V_{TH})} \left\{ \ln(-1) - \ln\left(\frac{0.1V_{DD}}{-1.9V_{DD} + 2V_{TH}}\right) \right\}$$

$$\ln(a) - \ln(b) = \ln(ab)$$

$$= \frac{C_L}{k_m \cdot (V_{DD} - V_{TH})} \ln\left(\frac{-1}{\frac{0.1V_{DD}}{-1.9V_{DD} + 2V_{TH}}}\right)$$

$$= \frac{C_L}{k_m \cdot (V_{DD} - V_{TH})} \ln\left(\frac{1.9V_{DD} - 2V_{TH}}{0.1V_{DD}}\right)$$

$$= \frac{C_L}{k_m \cdot (V_{DD} - V_{TH})} \ln\left(\frac{19V_{DD} - 20V_{TH}}{V_{DD}}\right)$$

$$= \frac{C_L}{k_m \cdot V_{DD} \left(\frac{1 - V_{TH}}{V_{DD}} \right)} \ln\left[\frac{V_{DD} \left(19 - 20 \frac{V_{TH}}{V_{DD}} \right)}{V_{DD}}\right] - (12)$$

at $n = \frac{V_{TH}}{V_{DD}}$ equⁿ (12) \Rightarrow

$$t_{f2} = \frac{C_L \ln(19 - 20n)}{k_m \cdot V_{DD} \left(1 - n \right)} - (13)$$

Adding eqn ⑦ + ⑬

$$t_f = t_{f1} + t_{f2}$$

$$t_f = \frac{2 C_L \cdot (n-0.1)}{VDD \cdot \ln(1-n)^2} + \frac{C_L \cdot \ln(1g-20n)}{\ln(n) \cdot VDD \cdot (1-n)}$$

by taking $\frac{2 \cdot C_L}{VDD \cdot \ln(1-n)}$ common

$$= \frac{2 \cdot C_L}{VDD \cdot \ln(n) \cdot (1-n)} \left[\frac{(n-0.1)}{(1-n)} + \frac{1}{2} \ln(1g-20n) \right]$$

$$\boxed{t_f = \frac{2 \cdot C_L}{k_n \cdot VDD \cdot (1-n)} \left[\frac{(n-0.1)}{1-n} + \frac{1}{2} \ln(1g-20n) \right]}$$

for CMOS inverter with $V_{DD} = 5V$, determine the fall time t_{fall} which is defined as the time elapsed between the time point at which $V_{out} = 90\% = 4.5V$ and the time point at which $V_{out} = V_{IOZ} = 0.5V$. Use both the average-current method and the differential eqn method for calculating t_{fall} . The op-amp load capacitance is $1PF$. The n-mos transistor parameters are given as;

$$dI_n/dV = 20mA/V^2$$

$$(W/L)_n = 10, \quad V_{dn} = 1.0V$$

$$\begin{aligned} I_{avg} &= \frac{1}{2} \left[I(V_{in}=5V, V_{out}=4.5V) + I(V_{in}=5V, V_{out}=0.5V) \right] \\ &= \frac{1}{2} \left[I_{sat} + I_{Un} \right] \\ &= \frac{1}{2} \left[\frac{k_n}{2} (V_{in}-V_{dn})^2 + \frac{k_n}{2} [2(V_{in}-V_{dn}) \cdot V_{out} - V_{out}^2] \right] \end{aligned}$$

$I_{avg} = 0.9875mA$

$$t_{fall} = \frac{C \cdot \Delta V}{I_{avg}} = \frac{1 \times 10^{-12} (4.5 - 0.5)}{0.9875 \times 10^{-3}} = 4.05ns.$$

$t_{fall} = 4.05ns$

Now, we will calculate the fall time using the differential equation approach. The n-mos transistor operates in the saturation region for $0 \leq V_{out} \leq 4.5V$.

$$C \frac{dv_{out}}{dt} = -\frac{k}{2} (v_{in} - v_m)^2$$

where $len = l_m \ln \frac{W}{L}$

$$\boxed{\frac{dv_{out}}{dt} = -1.6 \times 10^9 \text{ V/s}}$$

$$\int_{t=0}^{t_{sat}} dt = -\frac{1}{1.6 \times 10^9} \int_{V_{out}=4.5}^4 dv_{out}$$

$$\boxed{t_{sat} = 0.3125 \text{ ns}}$$

The n-mos transistor operates in the linear region for $0.5 \text{ V} \leq V_{out} \leq 4.0 \text{ V}$. The current equation for this operating region is written as follows:

$$\begin{aligned} C \frac{dv_{out}}{dt} &= -\frac{k}{2} [2(v_{in} - v_m) \cdot V_{out} - V_{out}^2] \\ &= -\frac{2C}{l_m} \int_{V_{out}=4}^{0.5} \frac{dv_{out}}{2(v_{in} - v_m) \frac{V_{out}}{V_{DD} - V_{out}} - V_{out}} \\ &= \frac{+2C}{(V_{DD} - v_m) l_m} \ln \left[\frac{V_{out}}{2(v_{in} - v_m) \frac{V_{out}}{V_{DD}} + V_{out}} \right]_{0.5}^{+} \\ &= \frac{1 \times 10^{-12}}{\frac{2.0 \times 10^{-6}}{l_m \ln \frac{W}{L}} \times 10 \times 4} \left\{ \ln \left[\frac{4}{2(5-1) \cdot 4 + 4} \right] - \ln \left[\frac{0.5}{2(5-0.5) \cdot 0.5 + 0.5} \right] \right\} \\ &= \frac{1 \times 10^{-12}}{2.0 \times 10^{-6} \times 80} \left[\ln \left(\frac{1}{18} \right) - \ln \left(\frac{0.5}{3.5} \right) \right] \\ &\approx \frac{1 \times 10^{-12}}{16.0 \times 10^{-12}} - 1.45 \left(1.945 \right) \\ &= 3.385 \times 10^{-9} = 3.385 \text{ ns.} \end{aligned}$$

$$\boxed{\therefore t_{all} = 3.6975 \text{ ns}}$$