VERILOG-AMS

LRM

INCLUDES CHAPTER 4,7 AND 10

10 COMPILER DIRECTIVES

WHAT ARE COMPILER DIRECTIVES?

- Special instructions in Verilog-AMS
- Begin with (`) accent grave
- Affect simulation and modeling across files
- Directives impact all files unless overridden
- Active from the point they appear until redefined

IMPORTANT COMPILER DIRECTIVE

- `default_discipline
- `default_transition
- `define and `undef
- `ifdef __VAMS_ENABLE__
- `ifdef __VAMS_COMPACT_MODELING__
- `begin_keywords and `end_keywords
- `__FILE__ and `__LINE__

`default_discipline

- Sets the default discipline for signals
- Applies to all signals without explicit discipline
- Can be redefined in the same file

```
`default_discipline ddiscrete
```

`default_transition

- Sets the default transition time
- Affects rise and fall times
- If omitted, the simulator decides transition time

```
`default_transition transition_time
```

`define and `undef

- `define creates a macro
- `undef removes a macro

__VAMS_ENABLE__

- Ensures compatibility between Verilog and Verilog-AMS
- Hides Verilog-AMS features unless enabled

```
`ifdef __VAMS_ENABLE__
        parameter integer del = 1 from [1:100];
`else
        parameter del = 1;
`endif
```

__VAMS_COMPACT_MODELING__

- Ensures compatibility between Verilog and Verilog-AMS
- Hides Verilog-AMS features unless enabled

```
ifdef __VAMS_COMPACT_MODELING__
        reff = ddx(iab, V(a));
        I(a,b) <+ white_noise(4.0*‘P_K*$temperature*reff, "thermal");
`elseif
        (analysis("noise"))$strobe("Noise not computed.");
`endif
```

`begin_keywords and `end_keywords

- Defines keyword set for parsing
- Ensures compatibility across Verilog versions

```
`begin_keywords "1364-2005"
module m2 (sin ...);
                input sin;
endmodule
`end_keywords
```

`__FILE__ and `__LINE__

`__FILE__ expands to the current filename

`__LINE__ expands to the current line number

Useful for debugging

```
$display("Internal error: null handle at %s, line %d.", `__FILE__, `__LINE__);
```

THANK YOU