8th January 2025

Session 1 meeting minutes

# Introduction

Brief introduction about career path, where analog mixed signal verification comes into the picture. Skills vs value provided.

# Assignment

1. Linux Assignment
   1. Provided a Linux assignment for familiarization with manipulating big files.
   2. Due on the 11th of January 2025.
2. SystemVerilog Assignment
   1. Provided a SV assignment based on the design of a digital clock, discussed the necessary features, including
      1. 6 7-segment display modules
      2. 24 Hour time
      3. The ability to set time, set an alarm, use the stopwatch and timer features
      4. Primary focus is ease of use
   2. Will touch base every 3-4 days with regards to the digital clock assignment.

# Flows

* + - 1. Types of flows: ASIC, Full custom, Semi-Custom, FPGA

1. Why is ASIC predominantly used, scope of career in FPGA, differences between full, semi and ASIC flows.
2. ASIC is a semi-custom flow
3. Each company has its own derivation of flow but relies on this structure as the backbone.
4. When do we choose which flow? What is the basis for the decision?
5. Started discussing an ASIC flow
   1. What are specs? Who decides these specifications? Where do they come from
   2. RTL design is NOT Verilog/system Verilog. Verilog or system Verilog can be used to write RTL, but only when the behaviour described is that of register transfer level.
   3. Why register transfer level? What does the register transfer level represent in an actual chip design.
   4. An analog design does not include RTL, it deals with schematics.
   5. Functional verification, NOT RTL verification follows RTL design.
      1. Difference between functional and RTL verification
6. Full custom Flow
   1. Injected into the discussion after a brief about functional verification
   2. Again discussed specs followed by schematic design
   3. Simulation is analogous to verification in ASIC flow.
   4. Followed by layout which includes
      1. DRC, LVS and PEX
         1. Discussed Design rule checks, similarities between PCB DRC and CMOS DRC. Why CMOS DRC is needed, how it is specified.
         2. Layout versus Schematic was touched upon
         3. Parasitic Extraction or PEX
            1. Why it is extracted post layout
            2. Represents RC delays caused by the interconnection and interference between different materials(metals, silicon, oxides etc.)
   5. Tapeout
      1. Etymology
      2. Graphical Data stream

# Conclusion

Discussed any questions with LVS, DRC, full custom flow

1. Topic of why SRAM is designed using ONLY full custom
   1. Comparison of SRAM design using FF vs manual transistor placement.
   2. Advantages of FF SRAM, disadvantages
   3. Custom tools by companies such as SanDisk for laying these SRAM blocks (Tiling tools)

Discussion will continue with functional verification (ASIC flow) from next week. Session will begin with a quick recap of the previous meeting.