17th January 2025

Session 2 meeting minutes

# Introduction

Began with previous assignments progress update

1. Linux Assignment
   1. As a continuation of the Linux assignment, we were to use internal GVIM commands to create the same functionality.
   2. Multiple methods such as loops in GVIM were discussed
   3. Then asked if anyone had used the ‘macro’ feature in GVIM, and if not to experiment with using macros to automate repetitive tasks without the need for scripting
2. Asked a question related to the previous week’s discussion, “Which flow would be used to design a fully analog chip?”
   1. Answer lies in the process of the ASIC flow, particularly the RTL design step. Since there is no RTL blocks, we cannot use the RTL design process to create an analog chip.

# Assignment

1. Continuation of digital clock assignment
2. Flow revision

# Discussion

1. Began with controllable parameters for designers, essentially W/L ratios.
2. How convergence issues during simulation of analog devices causes many issues, changes in timeline
3. What parameters do we control? Only W/L ratio, not PDK
4. What is a PDK (Process Development Kit)? What type of devices are contained within the PDK?
5. Discussed asking “why” as a habit, explained how to consistently ask why to arrive at the final solution, reasoning etc.
6. Continuation of previous week’s discussion, started with synthesis
   1. What synthesis does? A. Converts code to actual circuits. Provides a netlist file.
   2. What files does a synthesis process need? A. RTL, LIB files and design constraints
      1. RTL is obtained from previous steps, LIB files contain timing, electrical parameters etc, and are associated with the PDK used. SDC, or synopsys Design Constraint files contain parameters relating to the requirement of the synthesis process
7. Following synthesis, STA was discussed, termed as pre layout STA due to the repetition of STA afterwards
   1. What does STA do? A. Provides ability to verify Setup and Hold times, certain parameters based on requirements are set, and then the tool runs for those cases
   2. What files does a STA process need? The netlist file from synthesis, and the same SDC file and LIB file used during synthesis.
   3. Most commonly used tool is Synopsys PrimeTime.
8. GLS or Gate Level Simulation is done for those circuits that are asynchronous in nature. It can run parallel to STA (pre layout).
   1. This can help catch issues such as X-Propagation, where a mismatched or nearby signal can cause uncertainty and affect the proceeding block, which then propagates throughout the entire block/ design etc. X propagation is difficult to trace and can lead to non-functional behaviour.
9. Physical Design or PD
   1. Includes steps such as Floorplanning, placement, routing and Clock Tree synthesis (CTS)
   2. These can be thought of as similar to the building of a house, right from acquiring the land to ensuring that each room is accessible easily and timely.
   3. CTS ensures that the time required to arrive at the required block for multiple blocks is relatively equal/ proportional, to avoid clock mismatch.
   4. Placement involves the use of P-cells or parameterized cells
   5. Routing involves the use of different metals on different layers to ensure connection between blocks/devices, without creating false connections/other connection issues.
10. Post Layout STA
    1. While pre layout STA provides a rough value from which the circuit can be evaluated, post layout gives a much more accurate result as the layout has now introduced precise values associated with each of the wire runs, the distances between them, the layers used etc.
    2. This allows the tool to run mathematical expressions to extract the actual resistances and capacitances formed during layout.
    3. Post layout STA uses this PEX file to then run the STA again, returning a more accurate result, allowing better timing closure.
    4. Post Layout STA also allows an extracted simulation to be run if needed during the execution of the flow.
11. GDS-II
    1. Graphical Data Stream
    2. Representation of layout

# Conclusion

1. Discussed full semi-custom/ASIC flow
2. A question regarding the effect of temperature was brought up, and how we handle the change in processing due to heat and prolonged heat
   1. Most chips have thermal devices to detect excess heat
   2. BGR circuits are used to provide a temperature independent clock to all devices
   3. Built in Self Tests are included in chips to allow testing due to change in temperature etc.
   4. During simulation/verification we also analyse devices at different temperatures (corners) these usually align with the use case of the device.
3. Make asking why a habit