1. Which is the correct statement for `undef.

A) To define a constant value of varaiable

B) Removes the previously defined directive

C) To include new variable in port

D) B & C options

1. How many basic binary subtraction operations are possible?
2. 1
3. 2
4. 3
5. 4
6. Which of the following combinations cannot be combined into K-map groups?
7. diagonal
8. corners in the same column
9. corners in the same row
10. overlapping combinations
11. Which is not right statement for D-Flipflop?
12. data transfer can occur only at postive edge.
13. data transfer can occur at postive edge or negative edge
14. holds the data for both level.
15. What are the symbols used to represent digits in the binary number system?
16. 0,1,2
17. 0,1
18. 1,2
19. 0 through 8
20. Which loop statement is not used in verilog HD?
21. for loop
22. while loop
23. forever loop
24. foreach loop
25. Which of the following is correct for a D latch?
26. The output toggles if one of the inputs is held HIGH
27. Q output follows the input D when the enable is HIGH.
28. Only one of the inputs can be HIGH at a time.
29. The output complement follows the input when enabled.

8. Which is not the correct statement?

1. Transport delay is used for sequential modelling
2. Interial delay is used for combinational modelling
3. delay can be synthesized
4. delay can not be synthesized

9. Generate loop is used for \_\_\_\_\_\_\_\_\_.

1. To permits one or more variable declarations
2. For fix number of iteration
3. For A & B
4. none

10. How is a J-K flip-flop made to toggle?

1. J = 0, K = 0
2. J = 1, K = 0
3. J = 0, K = 1
4. J = 1, K = 1

11. If a =1 , assign y=(a==2'b11) then value of y will be

1. 1
2. 1'b0
3. 2'b11
4. None of above

12. The carry propagation can be expressed as \_\_\_\_\_\_\_\_.

1. Cp = AB
2. Cp = A + B
3. Cp = A^B
4. Cp = A-B

13. How many binary bits are necessary to represent 748 different numbers?

1. 9
2. 7
3. 10
4. 8

14. Verilog is case sensitive.

1. false
2. true

15. How many data select lines are required for selecting eight inputs?

1. 1
2. 2
3. 3

16. Verilog synthesizers treat the white space ‘ ‘ and carriage returns differently.

1. true
2. false

17. Give the decimal value of binary 10010.

1. (6)10
2. (9)10
3. (18)10
4. (20)10

18. Verilog may be written at the Behavioral, Structural, Gate, Switch, and Transistor levels.

1. true
2. false

19. Which loop is not used to execute fix number of iteration ?

1. for loop
2. forever loop
3. repeat
4. B & C options

20. An invalid condition in the operation of an active-HIGH input S-R latch occurs when \_\_\_\_\_\_\_\_.

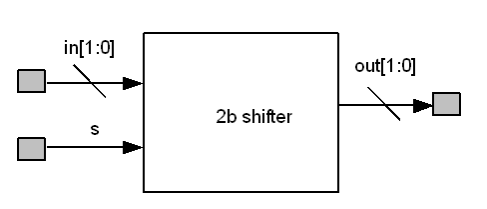
1. HIGHs are applied simultaneously to both inputs S and R
2. LOWs are applied simultaneously to both inputs S and R
3. a LOW is applied to the S input while a HIGH is applied to the R input
4. a HIGH is applied to the S input while a LOW is applied to the R input

Write Verilog code for below circuits.

**Exercise 1** – 2b shifter.

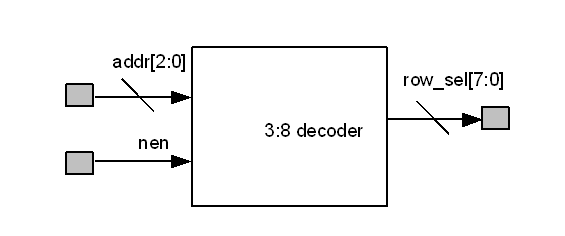
This is a 2bit shifter. This is a purely combinational logic block. The logic equations are:

* out[0] = s' ● in[0]
* out[1] = s' ● in[1] + s ● in[0]



**Ex 2** – 3:8 row decoder with enable.

This decoder has inputs addr[2:0] and an active low enable nen. It drives 8 active high output lines row\_sel[7:0], one of which is driven when nen is asserted.



**Ex 3** – 8b register with load and synchronous reset

This block implements an 8b wide register from DFFs. All flops are driven by a common clock and have a common reset rst. An input mux allows new data to be loaded into the register when ld is high; otherwise, the old data is recirculated.

