Course Title: Selected Topics in Wire line Transceiver Circuits

ELC611

ELC611 Course Outline/Topics

	Topics
1.	Introduction to serial/optical communications
2.	Wire line transceivers circuits
3.	Optical transceivers circuits
4.	Introduction to phase locked loops
5.	Phase locked loop top level analysis
6.	Phase locked loop building blocks (Phase detectors, Voltage controlled oscillators, Frequency dividers)
7.	Phase locked loop noise analysis
8.	Crystal oscillator circuit
9.	Clock and data recovery (system & circuit level design)

Detailted Course Outline – Part I

- Introduction to Serial/optical Communications
  - Applications
  - Basic Concepts Review
- Wire line Transceivers
  - Transmitter architectures and building blocks
  - Receivers architectures and building blocks
- Optical Transceivers
  - Trans-impedance Amplifiers (TIAs)
  - Limiting Amplifiers
- Clock and data recovery
  - CDR system level analysis & design
    - PLL, DLL, Phase interpolator based CDRs, & all digital CDRs
  - CDR building blocks

Course Details – Part I &II

- Instructors: Dr. Mohamed Youssef, Dr. Mohamed Salah Mobarak
- **Contact info**: youssef@ieee.org
- Mark Distribution: 4 projects (total=50), & final (50)

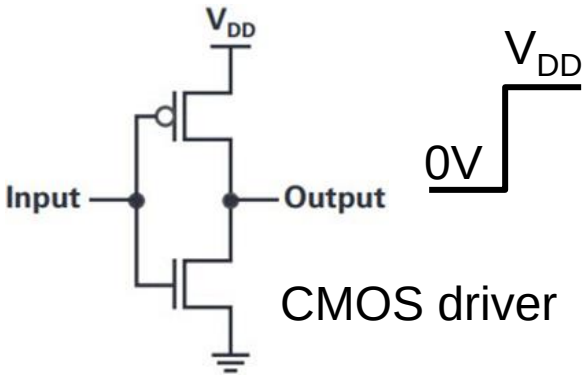
Course Main Textbooks/References (Part I)

- Design of Integrated Circuits for Optical Communications, by Behzad Razavi
- Broadband Circuits for Optical Fiber Communication, by Eduard Sackinger
- CMOS Circuit Design, Layout, and simulation, by R. Jacob Baker
- Selected Papers

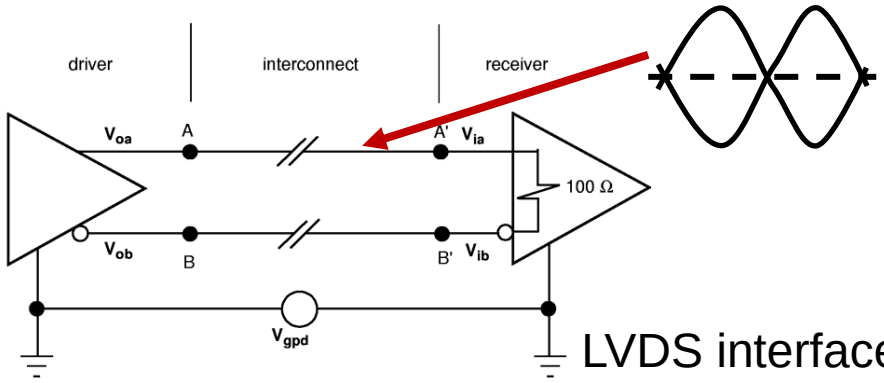
Brief History of Serial Interfaces

- **CMOS** interfaces used by standards such as **SPI** (serial peripheral interface) are adequate for applications up ~10-200Mbps
  - A CMOS driver can typically drive multiple CMOS receivers (due to the high impedance nature)
  - Advantages: low static current
  - transient current is why other technologies are used for output drivers beyond 200 Mbps.
- **LVDS** (low voltage differential signaling) offers advantages over CMOS technology.
  - It operates with a low voltage differential signal rather than single ended.
  - lower voltage swing → faster switching time & reduces EMI (electromagnetic interference) concerns.
  - LVDS also offers common-mode rejection (noise immunity).

CMOS vs. LVDS vs. Clock Less Interface (CDR)



CMOS driver

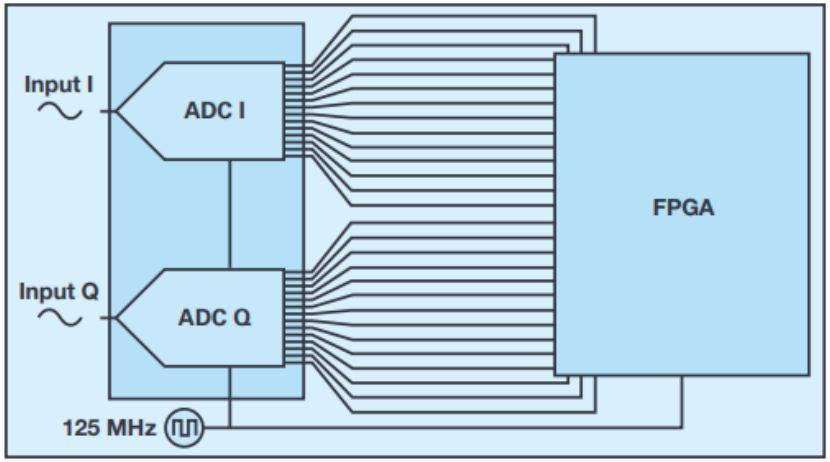


LVDS interface

	CMOS	LVDS	Clock Less (CDR)
Max data rate per lane	<200Mbps	<1Gbps	Reaches 40Gbps
Signal type	Single-ended	Differential	
Immune to noise	No	Yes	
Signal swing	0 to V_{DD} (~1.8V depends on supply)	Typically, 400mVp differential (varies according to standard)	
Termination	Typically, high impedance	100Ω differential	
Clock sent with data	Yes	Yes	No
Immune to clock skew	No	No	Yes

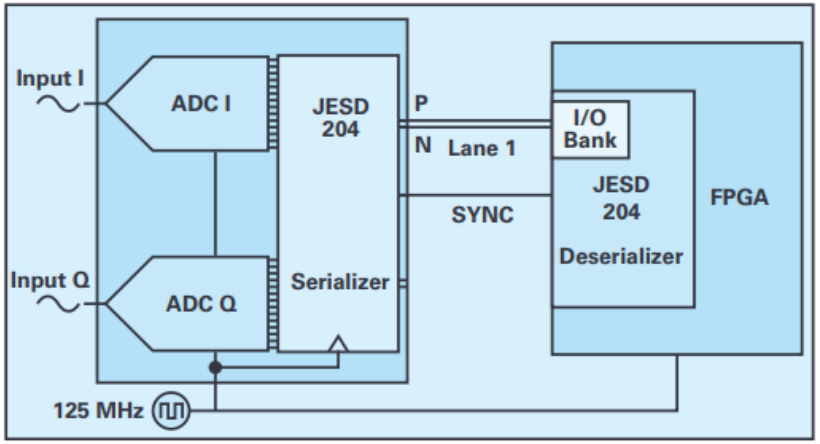
Ex: CMOS vs. LVDS vs. JESD204

ADC with Conventional Parallel CMOS/LVDS Outputs



- Must Have Same Trace Lengths (28)
- High Complexity Routing Due to BGA
- Higher/Lower Converter Resolution Requires Total Hardware Redesign

ADC with One Serial Jedec Link

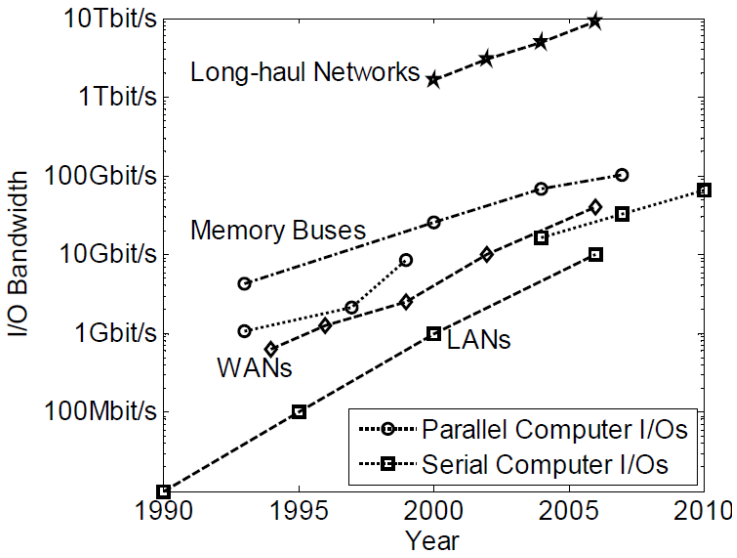


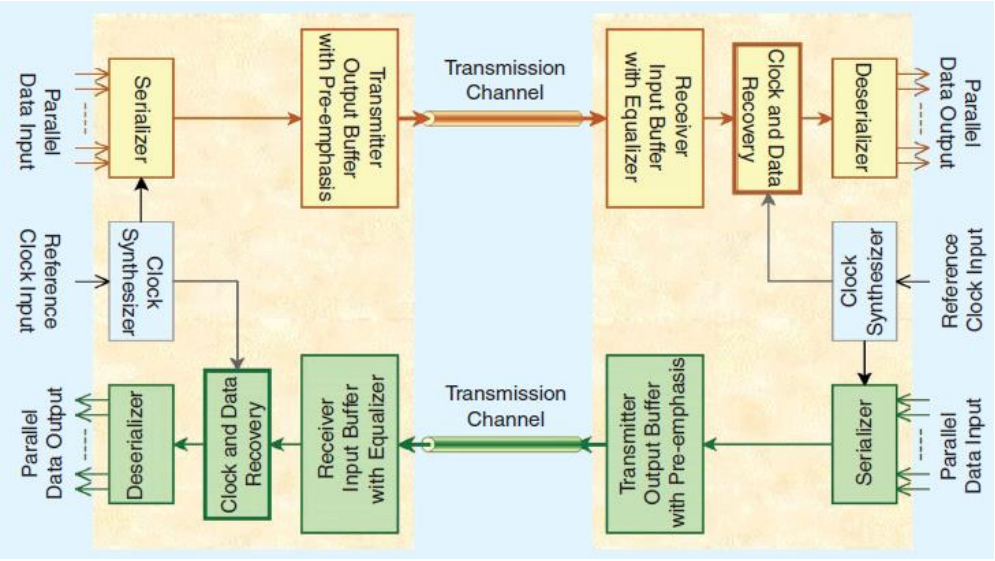
- Reduced Number of Traces (4)
- Very Low Complexity Routing
- Simplified Synchronization Protocol
- Migration to ADC with Higher/Lower Resolution without Hardware Modification, Only New Configuration File for the FPGA

- Motivation for JESD204 is to standardize an interface that reduces the number of digital I/Os between data converters and FGPAs/SoC using a scalable high speed serial interface
- Systems requiring wide bandwidth multichannel converters that are sensitive to latency across lanes won't be able to effectively use LVDS or parallel CMOS

"JESD204B vs. Serial LVDS Interface Considerations for Wideband Data Converter Applications" by George Diniz

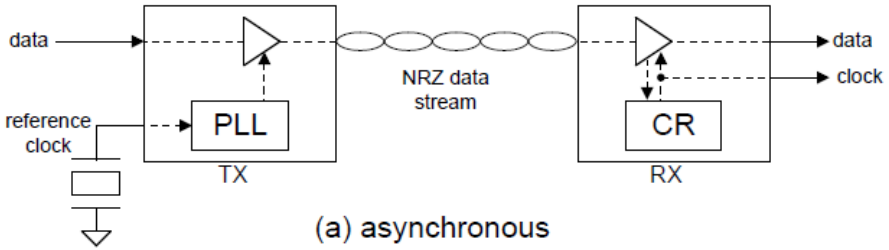
Introduction Serial Interfaces



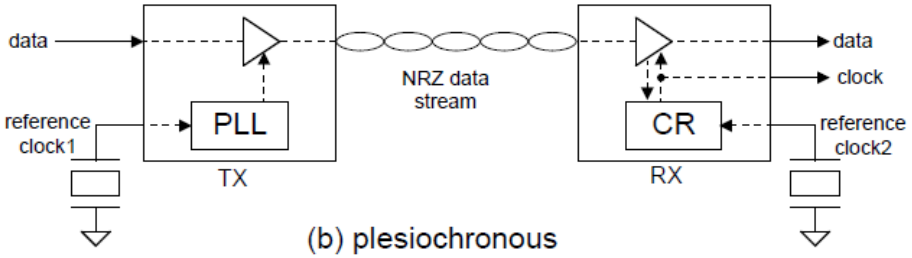


- Serial standards such as: JESD204,*10G Ethernet*, *SATA, PCI Express,* USB, *SONET* serve a variety of applications (Local/wide area networks, computer busses, storage devices, portable/peripheral devices, high speed data converters)
- Data is converted from parallel to serial via the **ser**ializer in the transmitter
- Then it is converted back from serial to parallel in the receiver **des**erializer
- Hence the name SERDES (**ser**ializer **des**erializer)
- A PLL is required to generate the high speed clock from a low frequency reference

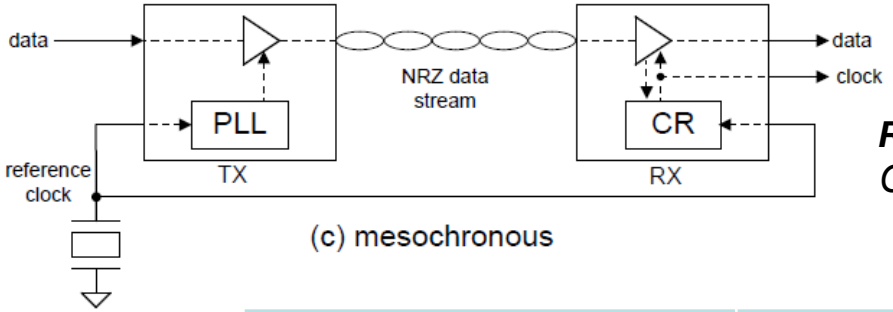
Clocking Schemes in Serial links



(a) asynchronous



(b) plesiochronous



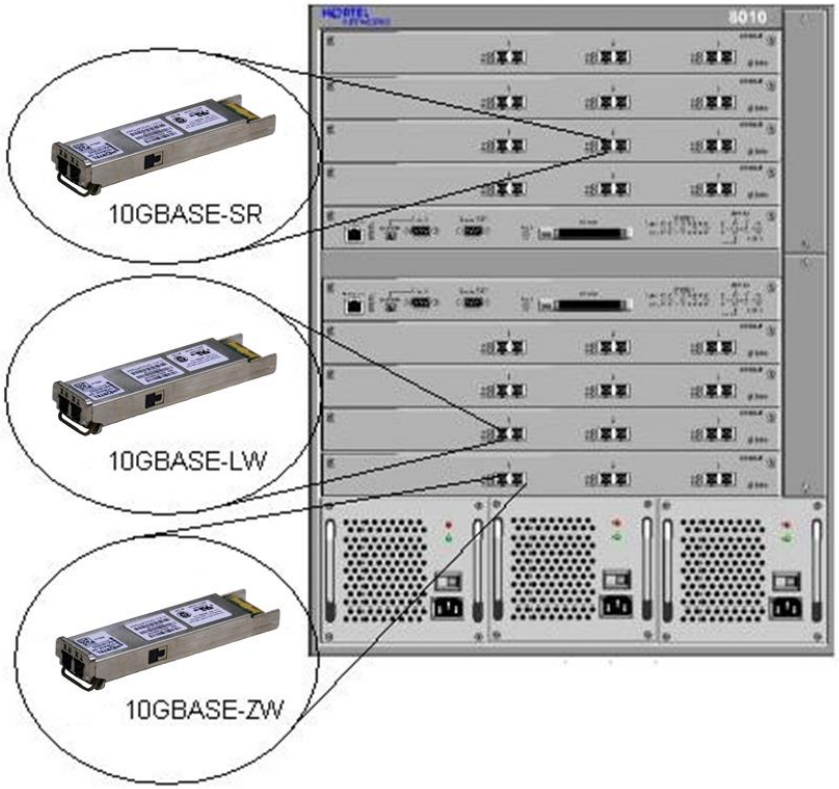
(c) mesochronous

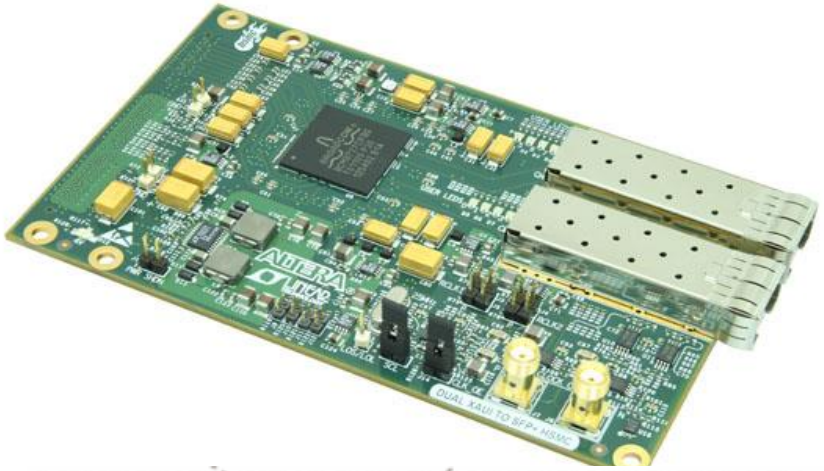
***Ref**: course slides "Topics in IC Design: 6.1 Introduction to Clock and Data Recovery" by Prof. Deog-Kyoon Jeong*

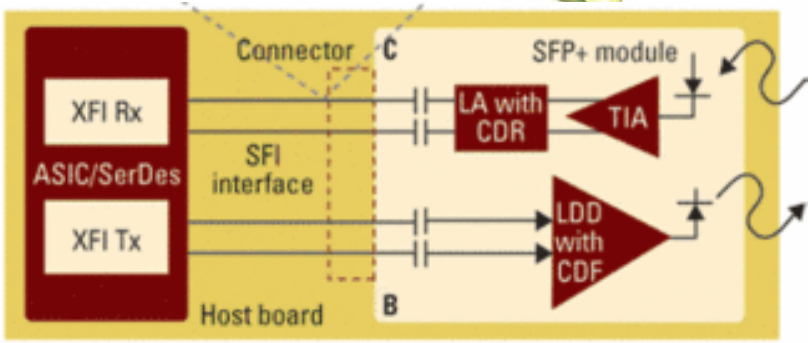
Type	Frequency drift	Phase drift
Asynchronous	varying	varying
Plesiochronous	Small difference	Slowly varying
Mesochronous	Same	Constant
Synchronous	Same	Same

- In a chip-to-chip application the Tx & Rx can use the same clock source → **source-synchronous**

10Gigabit Ethernet (wireline/optical interfaces)



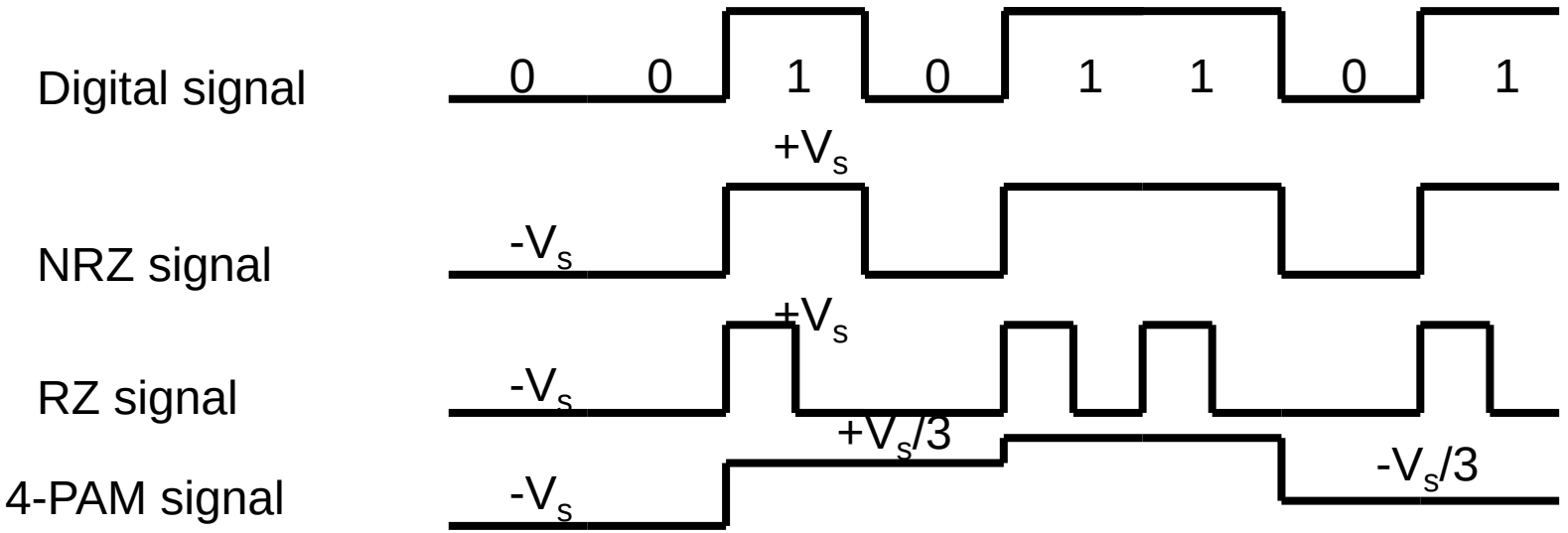




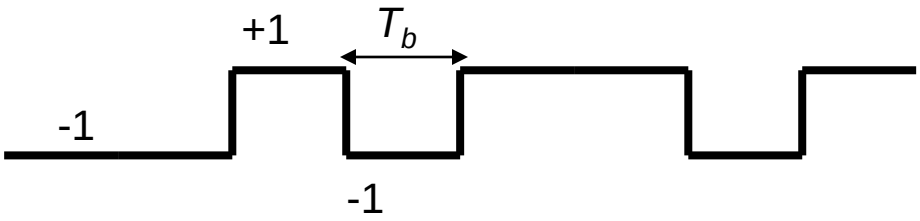
- Router with 10G Ethernet ports use 10G SFP/SFP+ (small form-factor pluggable) modules to interface to fiber optic cables
- SFP+ modules can retime the data and re-transmit it through PCB traces/connectors to the SerDes (**S**erDes **F**ramer **I**nterface: SFI interface)

Digital Modulation

- The most common modulation technique used in serial links is OOK (ON OFF keying), this is also termed NRZ (non-return to zero)
- Other common modulation techniques: RZ (return to zero), multi-level signaling such as pulse amplitude modulation (PAM)
- **NRZ** is the most commonly used line code due to it's simplicity and it requires less channel bandwidth compared to RZ
- RZ includes a spectral line at a frequency equal to the bit rate which facilitates clock recovery → need to process shorter pulses
- Some Ethernet standards use PAM signaling to reduce the channel bandwidth requirements



Properties of Binary NRZ Random Data



- The Binary NRZ signal can be represented by:

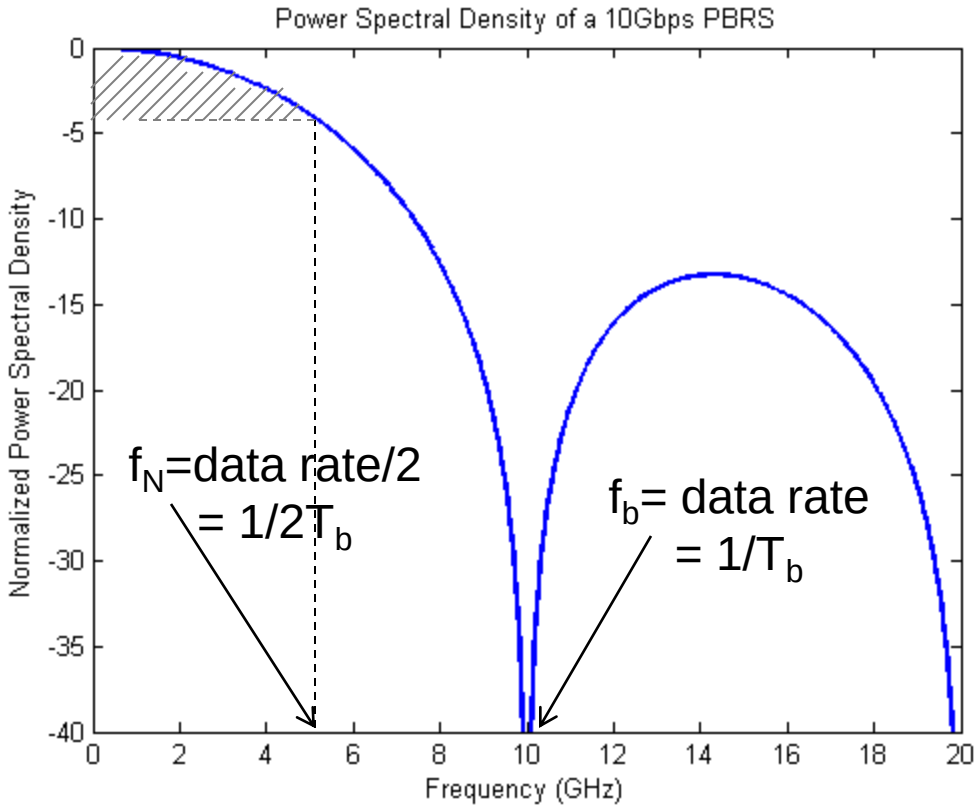
$$x(t) = \sum_k a_k \, p(t - kT_b)$$

where a_k is ±1 and represents the transmitted symbols, *p(t)* is a rectangular pulse shape, T_b is the bit duration

- The power spectral density $S_x(f)$ of x(t) has a sinc^2 shape and is given by:

$$S_x(f) = T_b \left[\frac{\sin(\pi f T_b)}{\pi f T_b} \right]^2$$

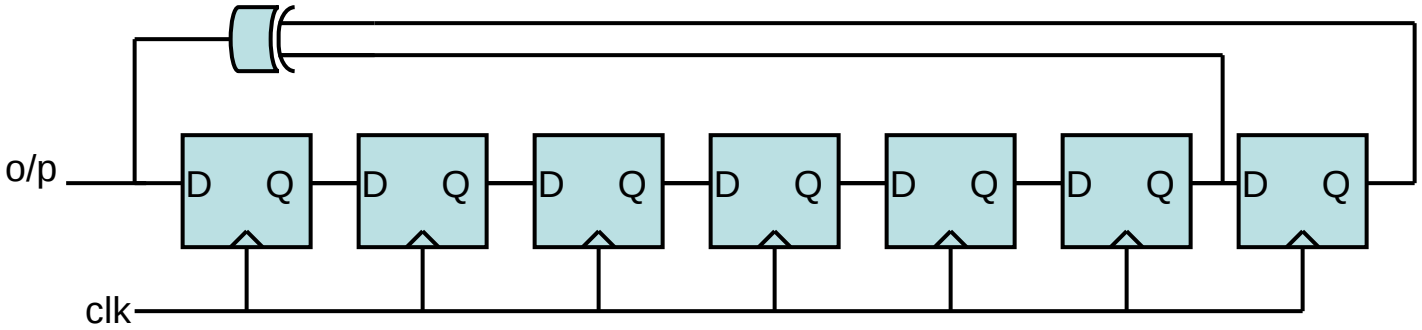
Properties of Binary NRZ Random Data (Cont'd)



- Spectrum doesn't include any spectral lines to facilitate clock recovery
- For the 10Gbps example shown above, the majority of the signal power is concentrated between DC and 5GHz ($1/2T_b$, Tb=100ps) i.e. the Nyquist frequency

Pseudo Random Binary Sequences

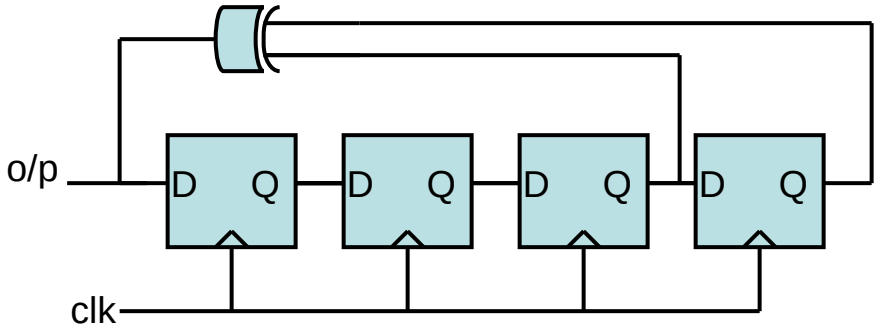
- During design & characterization of PHYs it is typical to use a known PRBS length (psuedo random binary sequence) for example PRBS 7, 15, or 31
- PRBS sequences are generated using LFSRs (linear feedback shift registers) which emulates random signals.
- The feedback taps of an n-bit LFSR are chosen for the output sequence to appear random and only start repeating after 2^n-1 bits
- The longer the prbs order the more it's spectrum would look like that of a real random signal
- For example, the feedback polynomial for prbs7 is: x^7+x^6+1



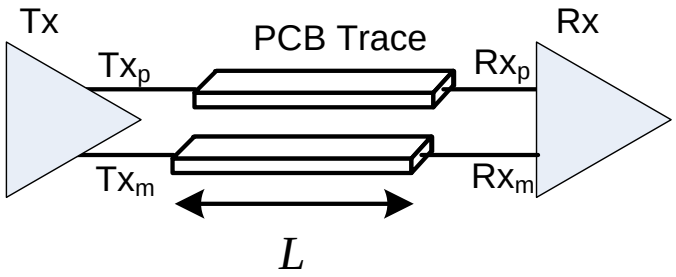
Pseudo Random Binary Sequences (Cont'd)

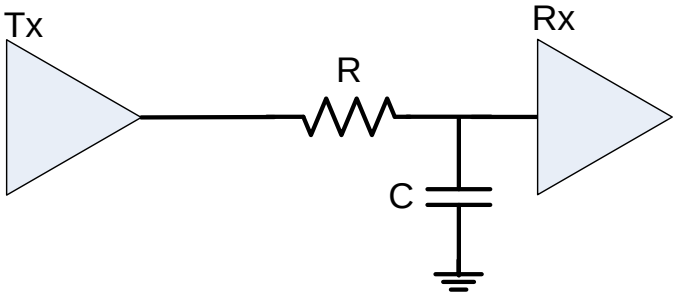
- Problem: Obtain the first 10 bits of prbs4 given that the polynomial for prbs4 is x^4+x^3+1. Assume the flip-flops are set to all 1's.

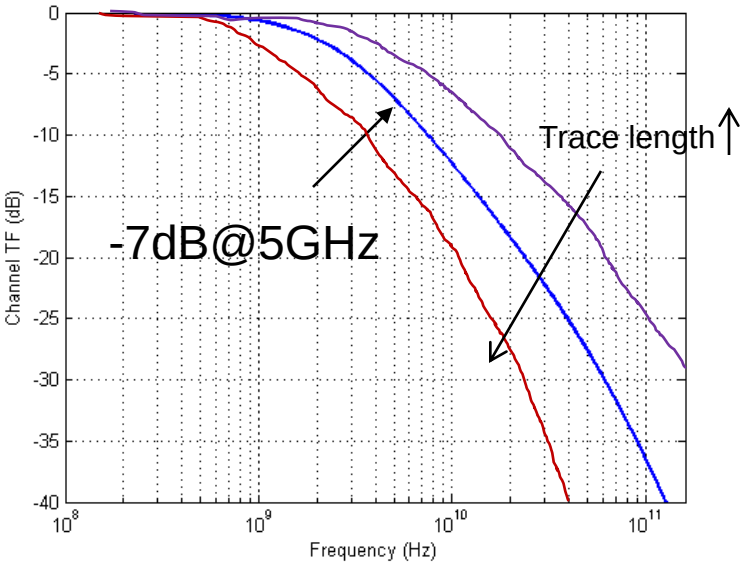
Current state	Next state	o/p
1111	0111	0
0111	0011	0
0011	0001	0
0001	1000	1
1000	0100	0
0100	0010	0
0010	1001	1
1001	1100	1
1100	0110	0
0110	1011	1



Finite Channel Bandwidth

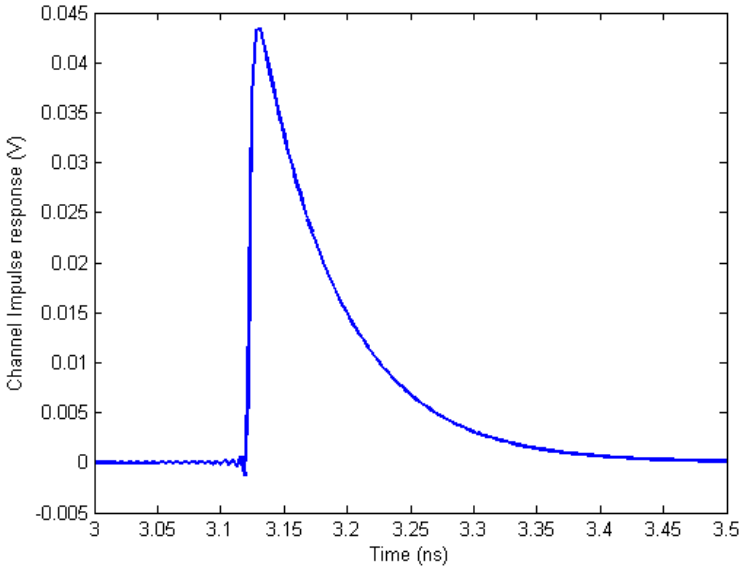


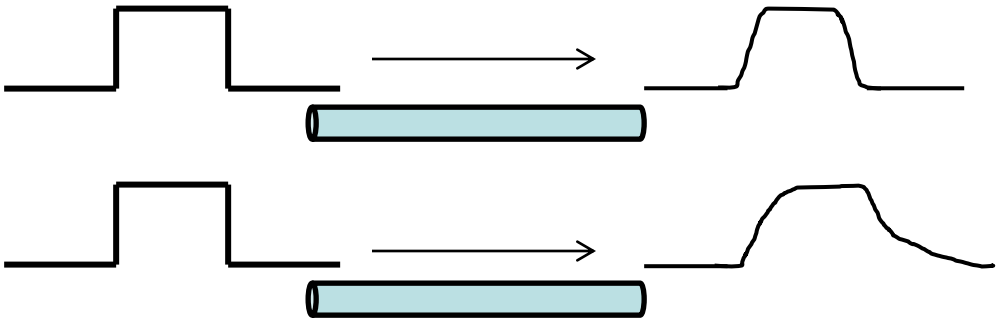




- As the signal propagates through the main channel it is attenuated according to the frequency profile of the channel
- Simplifying the 4-port channel into a differential 2-port representation allows us to model the differential signal
- We can model the PCB with a single RC filter with the same cut-off frequency
- Note the channel doesn't present any DC attenuation, but provides attenuation for the high frequency components in the signal
- As the channel length increases the high frequency loss will also increase, implying that the cut-off frequency should be a function of the channel length
- Standards specify a max attenuation for the channel

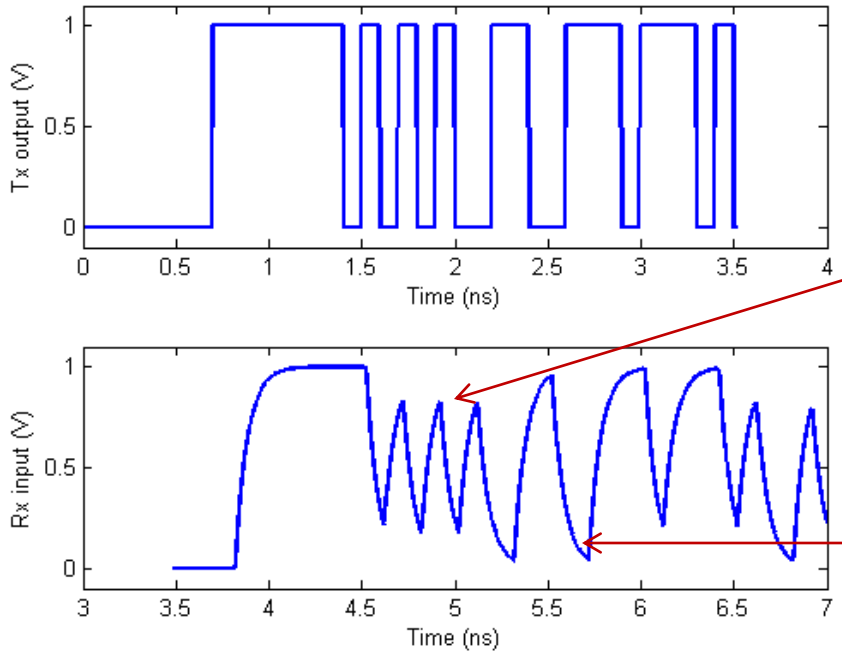
Finite Channel Bandwidth (Cont'd)





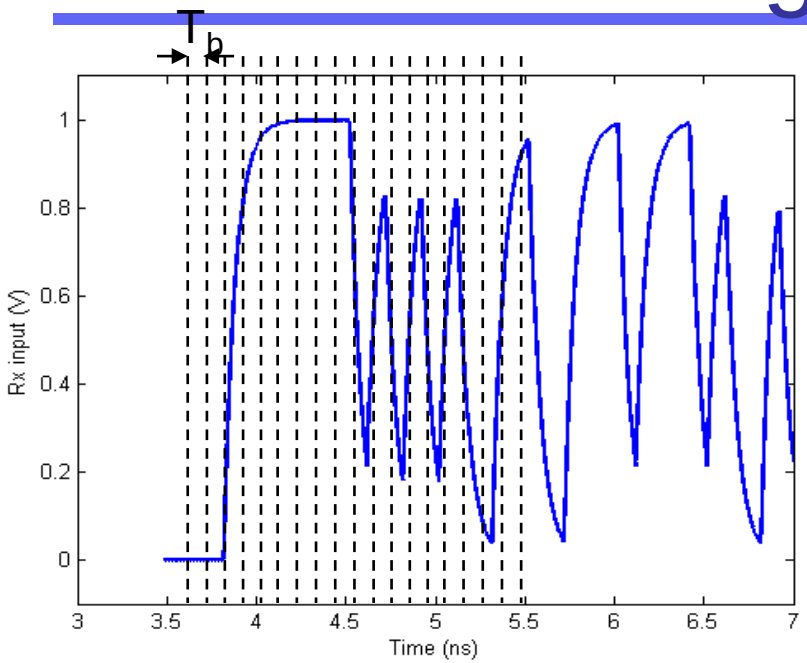
- The channel impulse response has a long tail implying that once a pulse is transmitted it spreads over to the adjacent pulses creating inter-symbol interference (ISI)
- ISI is one of the main signal impairments that serial link transceivers try to combat using linear/non-linear equalization techniques in order to achieve low bit error rates
- The Rx input signal is the result of the convolution of the Tx output signal with the channel impulse response

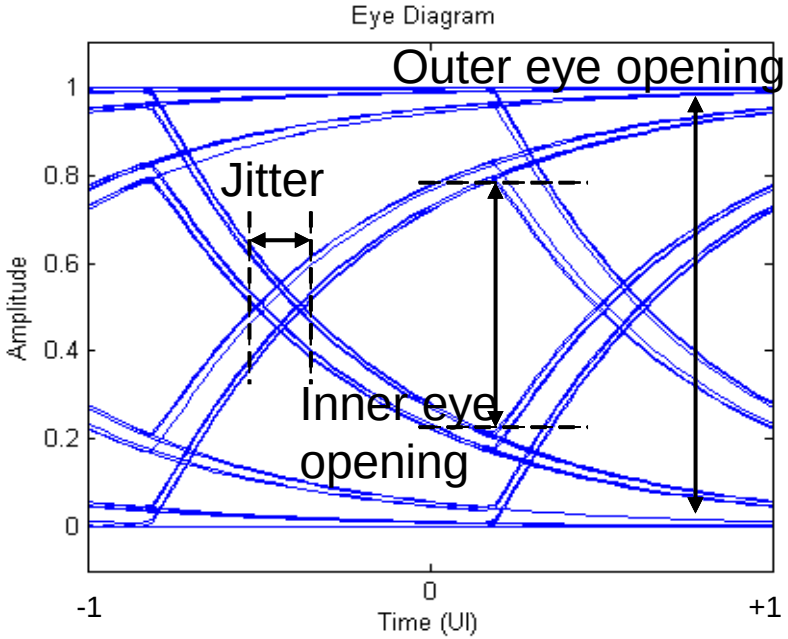
Finite Channel Bandwidth (Cont'd)



- A 10Gbps prbs7 is transmitted though the PCB trace model
- The Tx ideal output is assumed to have a 1V swing and is shown in the top plot
- The Rx input signal is shown in the lower plot
- Note that single bit transitions don't have enough time to settle resulting in less swing, whereas double bit transitions and higher, settle to the full 1V level
- This indicates that the signal is corrupted by ISI as the signal level is a function of the transmitted bits

Received Signal Eye Diagram

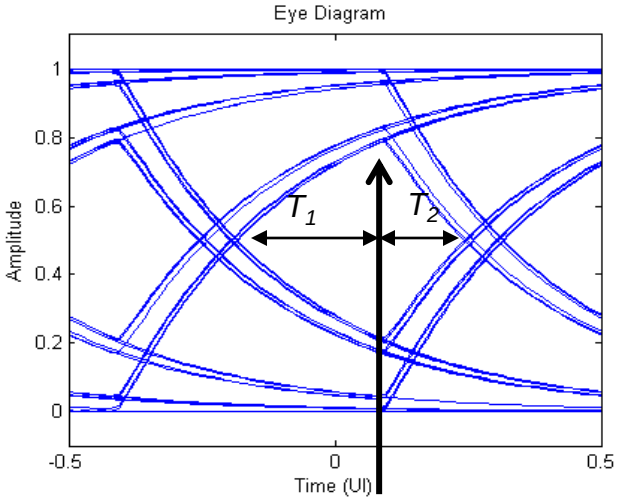




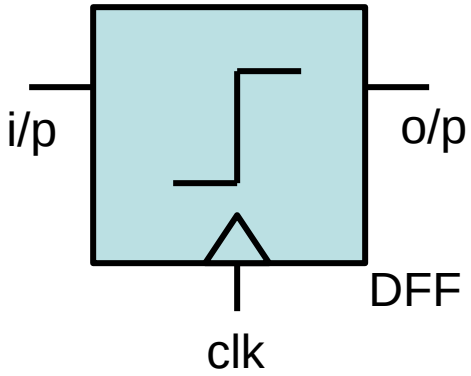
- The signal is sliced into many sections T_b or $2T_b$ apart and all the different sections are overlaid to produce the eye diagram
- The single bit transitions only reach to a portion of the full eye height resulting in vertical eye closure
- The traces which have the full swing level represent non-transition bits
- The difference between the inner and outer eye openings represents the quality of the received signal
- The high frequency attenuation by the channel also results in some closure in the horizontal eye opening, i.e. a finite error at the eye zero crossing (**jitter**)

Received Signal Eye Diagram (Cont'd)

i/p eye

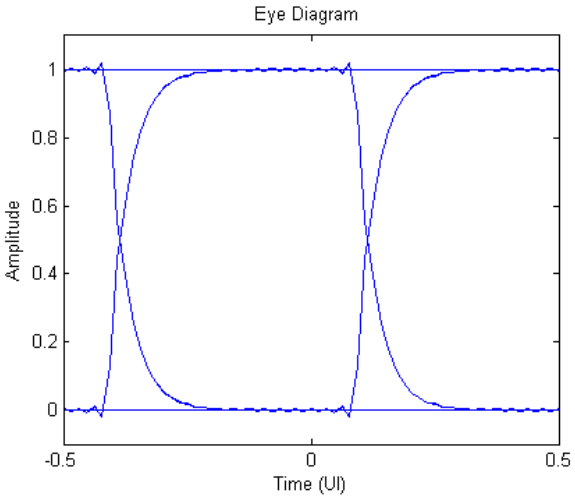


Optimal sampling point



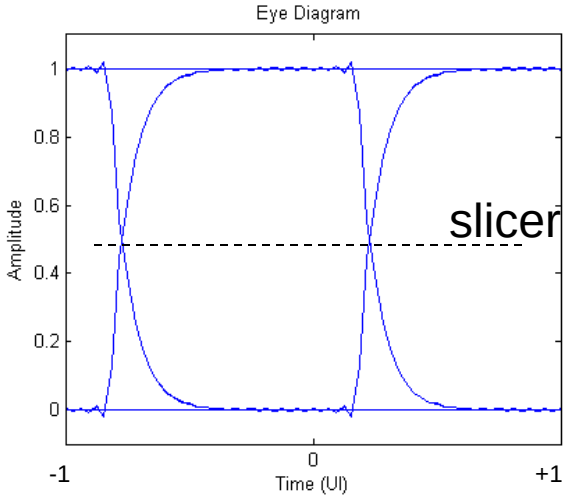
Re-timer/sampler: **need for clock recovery**

o/p eye

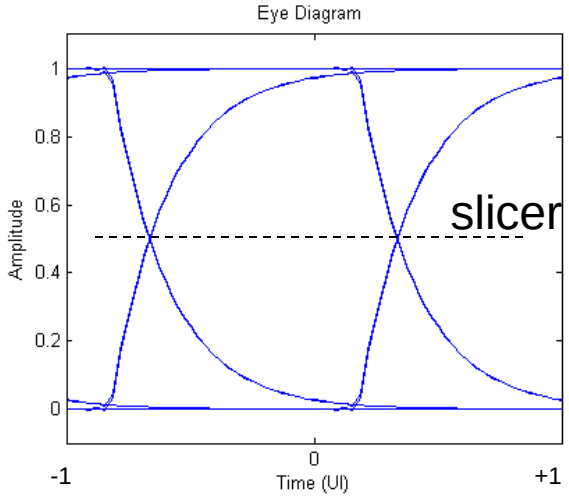


- If vertical eye opening is not high enough the sampler might not be able to take the correct decisions
- If $T_1 > T_{setup}$ no setup time violation
- If $T_2 > T_{hold}$ no hold time violation
- $T_1 + T_2$=horizontal eye opening
- The sampler (i.e. receiver) produces a clean output eye i.e. retimes the data

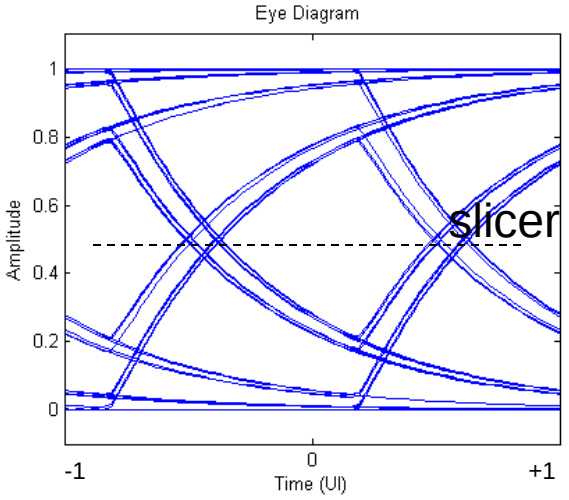
Received Signal Eye Diagram (Cont'd)



$BW_{3db}=2*f_b$



$BW_{3db}=0.7*f_b$



$BW_{3db}=0.25*f_b$

- As a rule of thumb $0.7*f_b$ is the optimal BW, where f_b is the bit rate
- A smaller BW would result in ISI reducing the vertical & horizontal sampler margins resulting in higher BER
- A larger BW doesn't provide more eye opening at the sampler but results in more noise power at the sampler input since it is being integrated over a wider receiver BW