Wireline Transceiver Circuits

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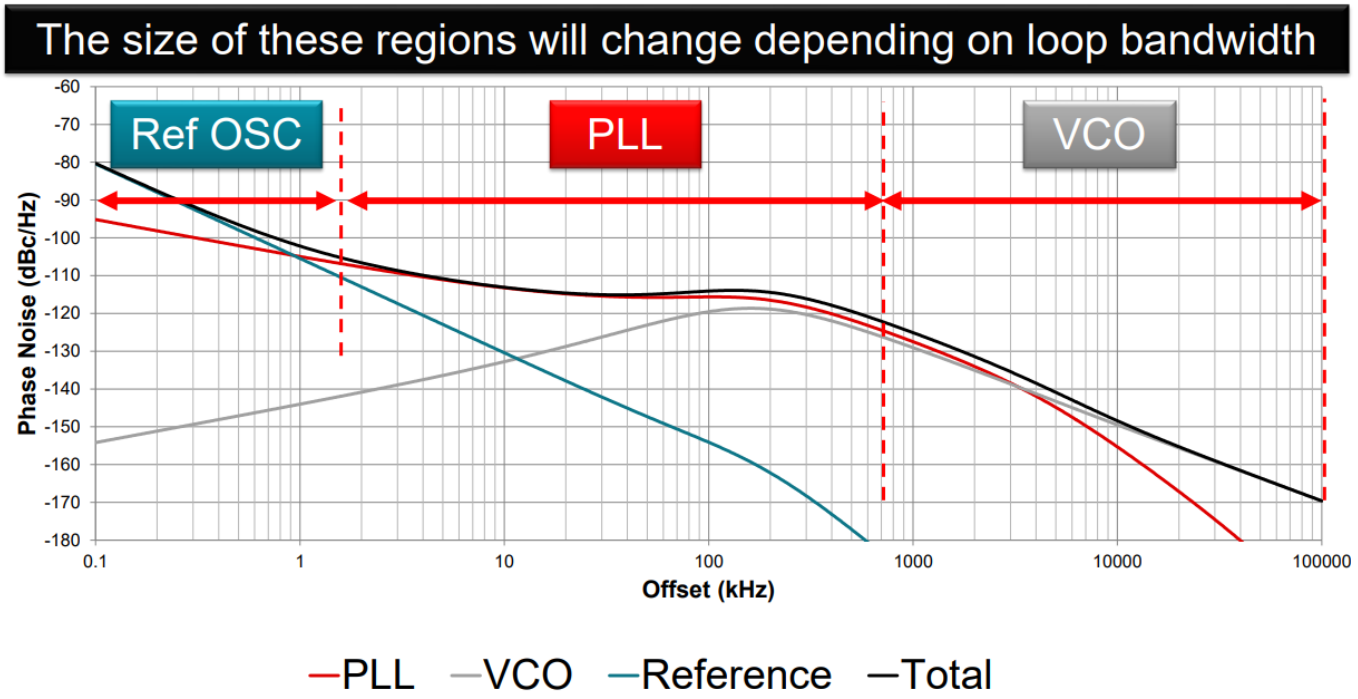
VCO Phase Noise Summary

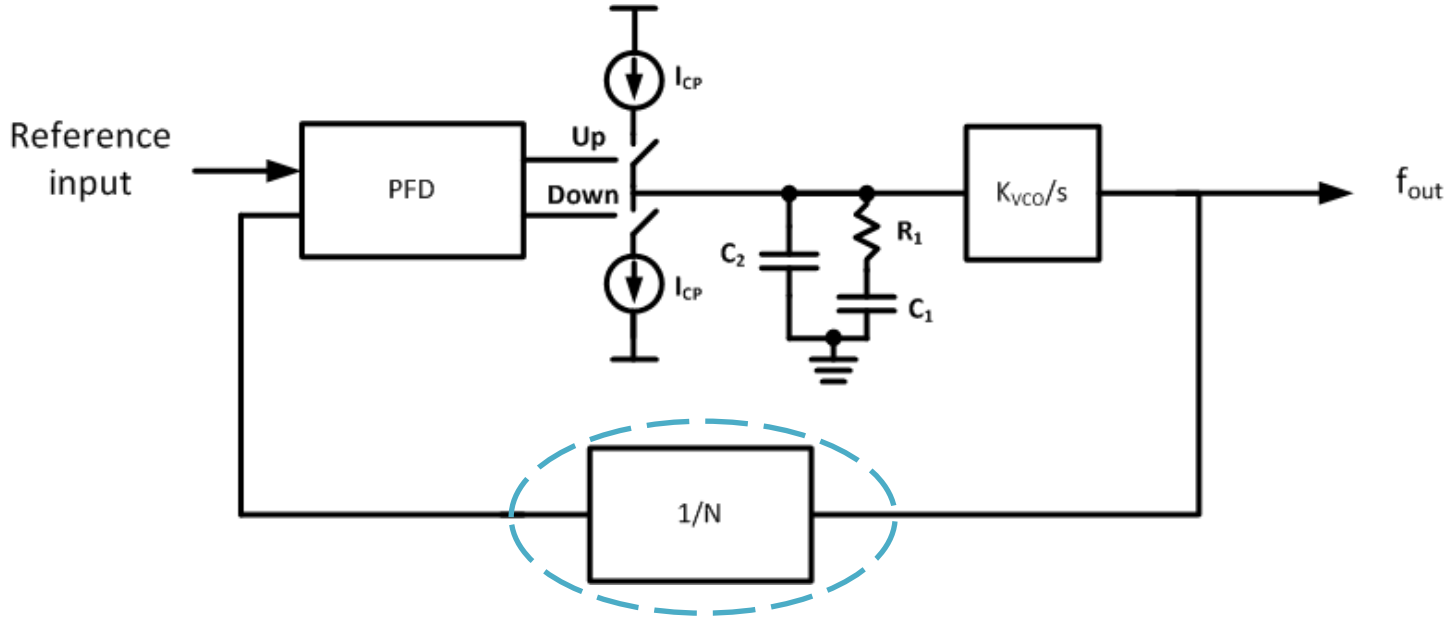
- To reduce VCO phase noise
  - Improve quality factor and reduce loss
  - Improve symmetry
  - Select topology that has current injected at voltage peaks
  - Increase power consumption
- Ring oscillator is used in application where area is most critical and phase noise is not very stringent

PLL Phase Noise Contributions



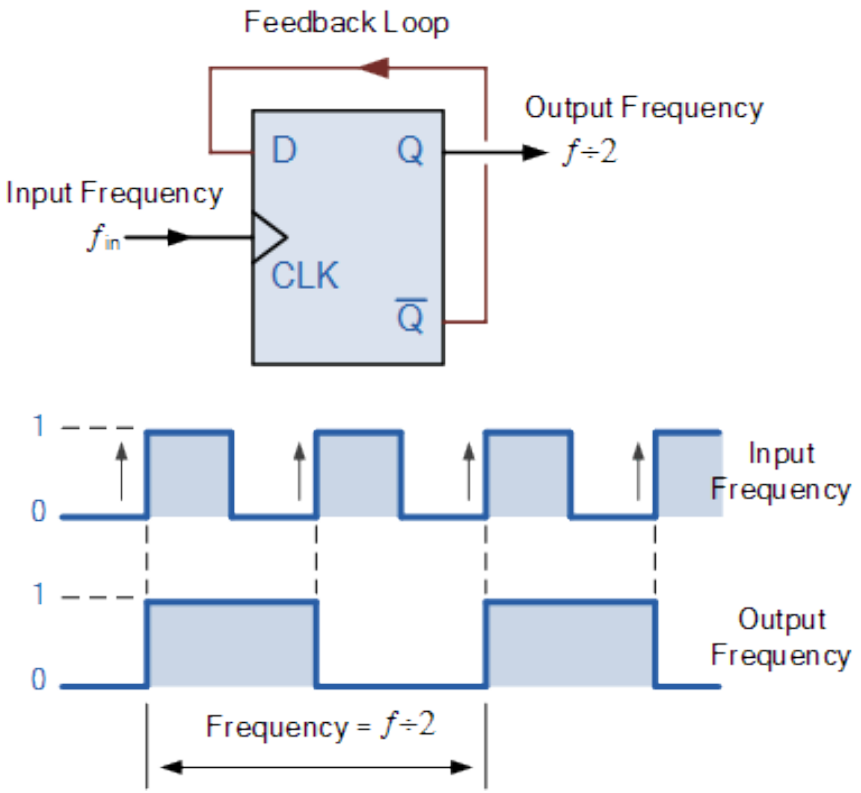
- Reference oscillator noise, and PFD/dividers has low pass response, while VCO has high pass response
- Large division ratio causes high noise
  - ➢ Use fractional dividers to avoid large N

Frequency Dividers



- Frequency divider takes the form of a counter
- VCO frequency is usually very high
- Divider power consumption is proportional to its frequency
  - Power consumption of single CMOS inverter $P = fCV_{DD}^2$

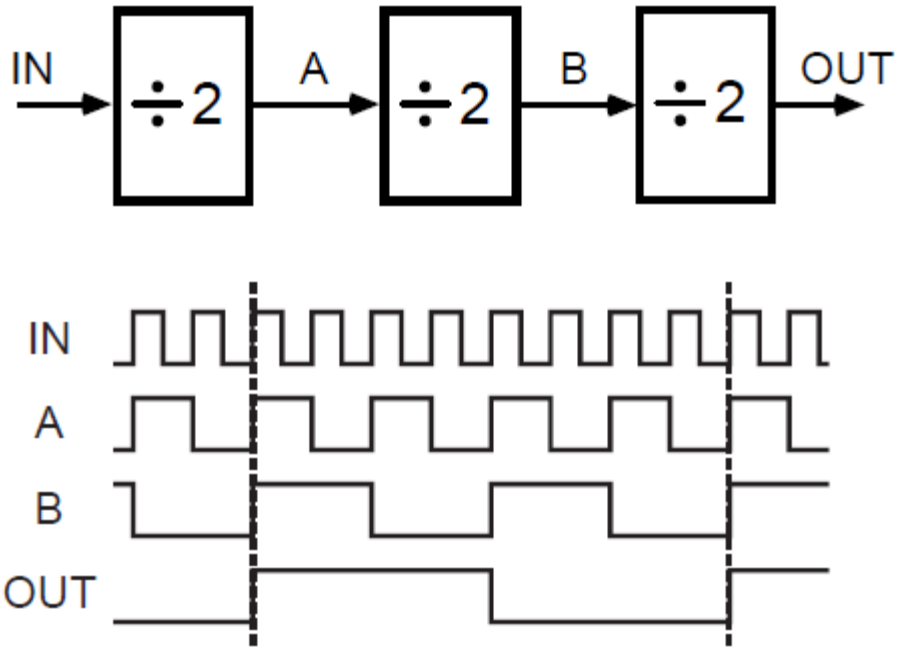
Frequency Dividers



- Divide by 2 circuit

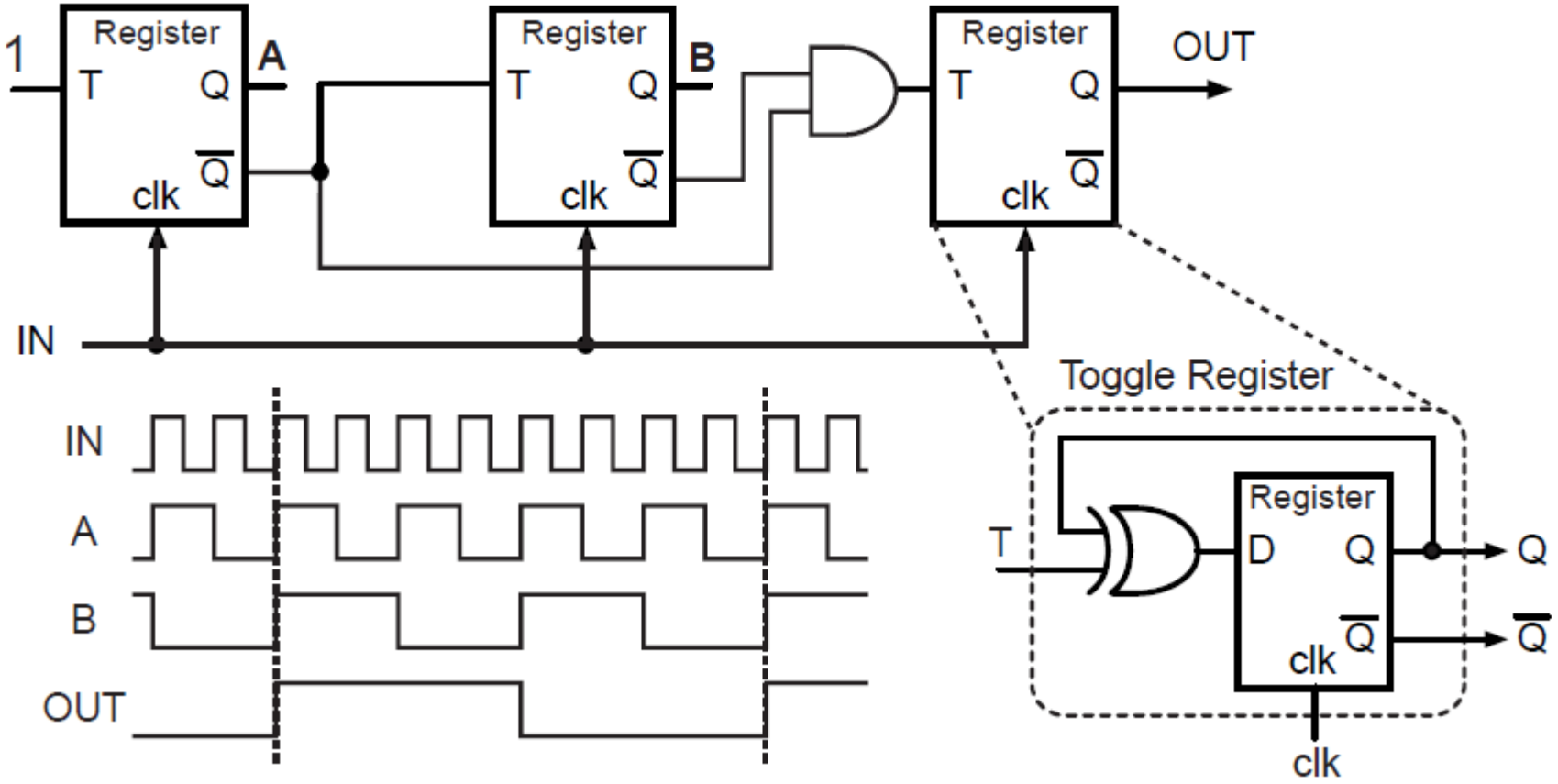
Counter Types

- Counters can be asyncrhonous or synchronous
- Asynchrounous counters have
  - Less loading on the clock
  - Lower power consumption
- Asynchronous counters suffer from higher noise



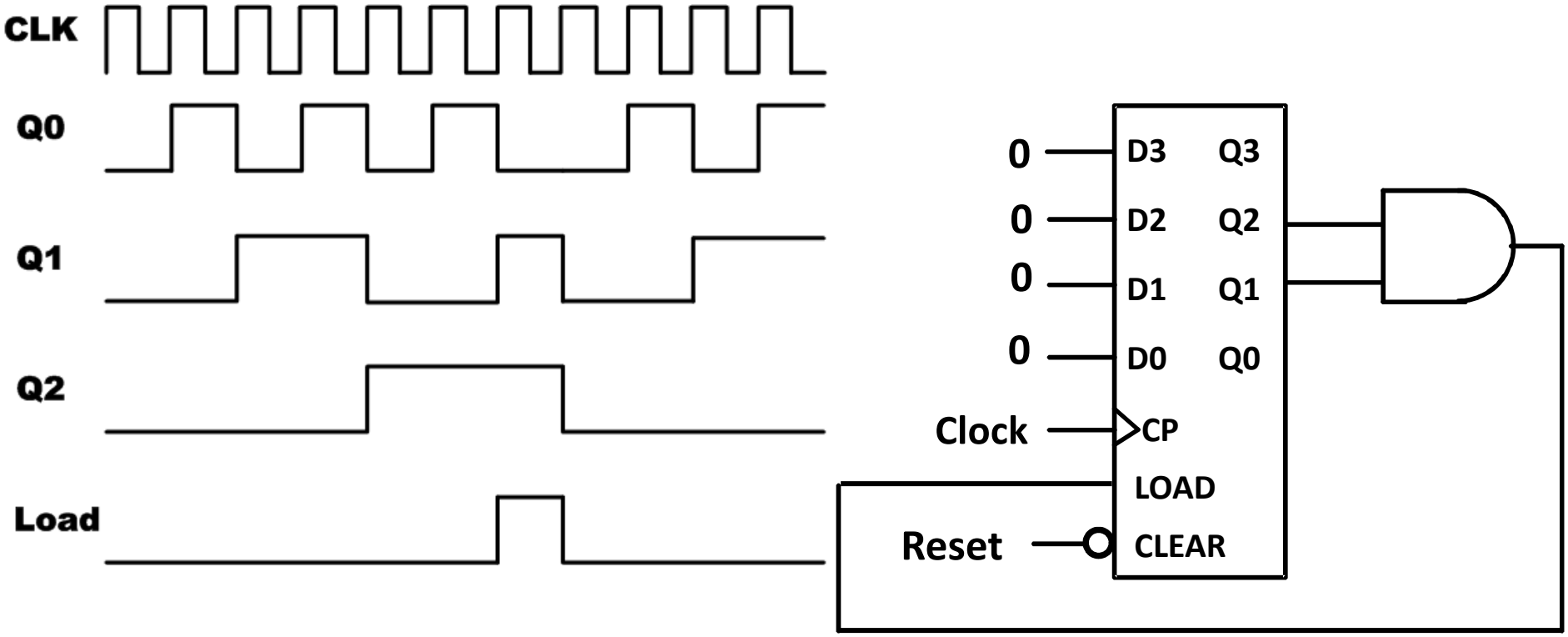
Counter Types

- Synchronous counters have less noise but more power consumption



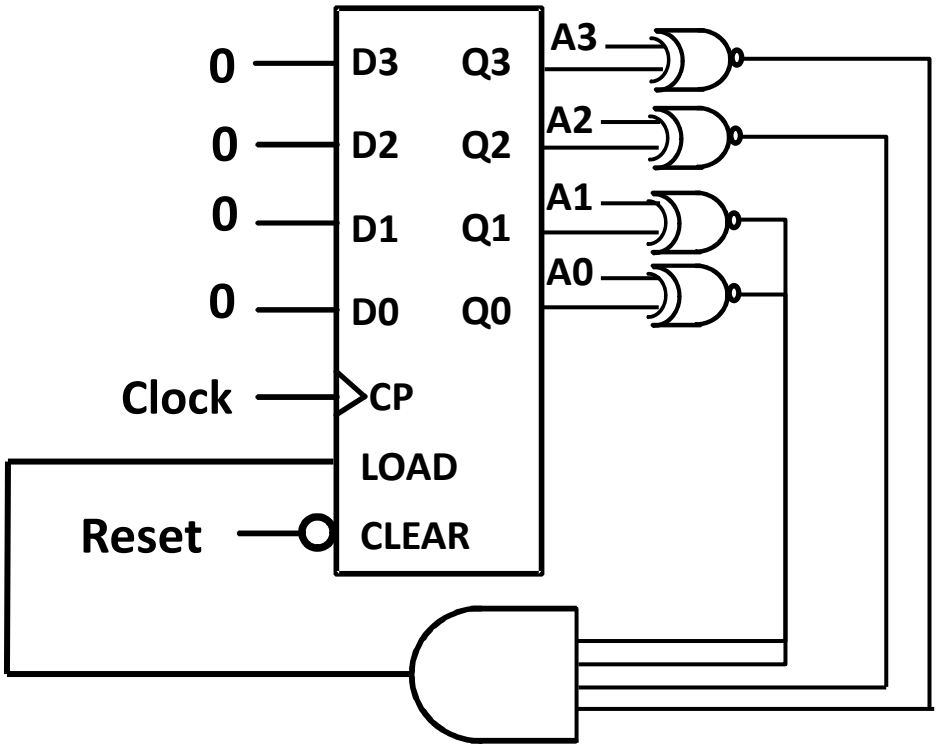
Program Counter

- Divide by 7 counter



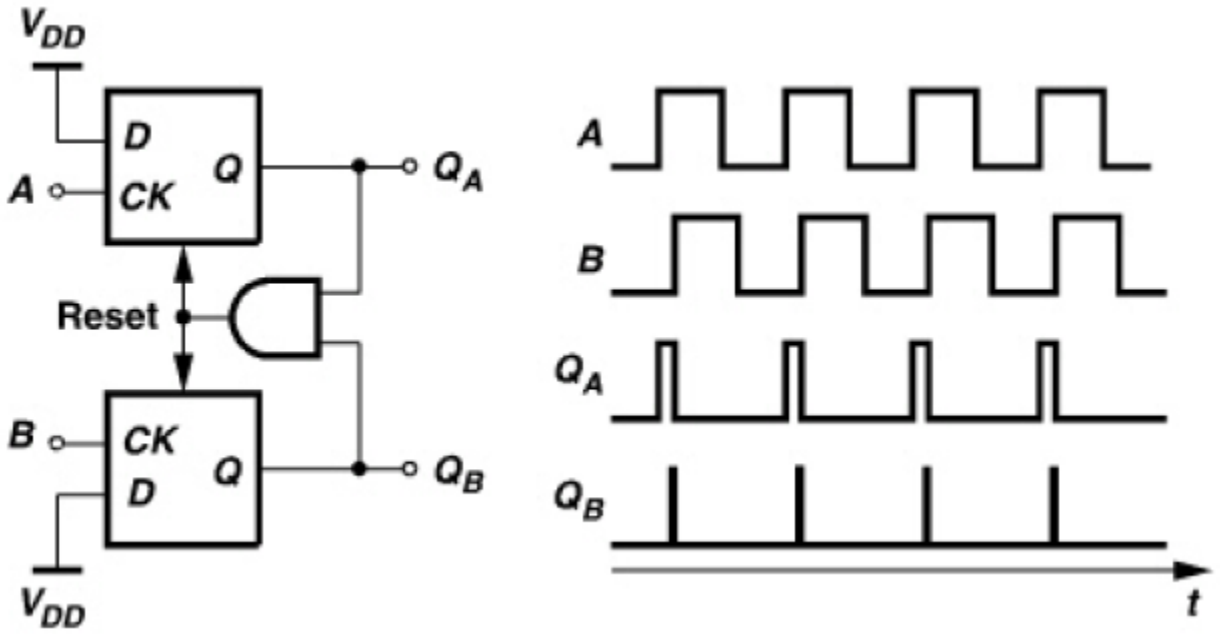
Program Counter

- Programmable counter can be done using count up or count down counters



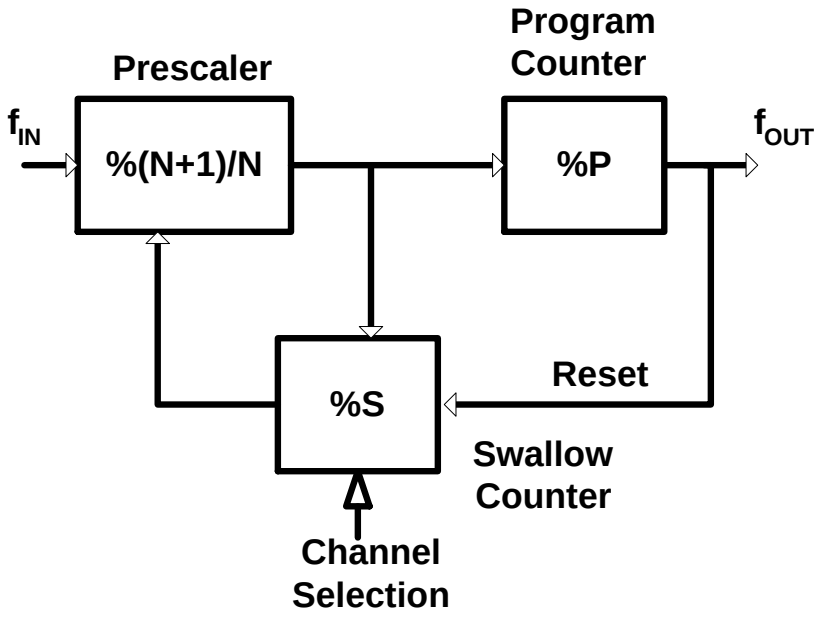
Program Counter

- Note that output pulse of divider does not have 50% duty cycle
  - Works fine with PFD



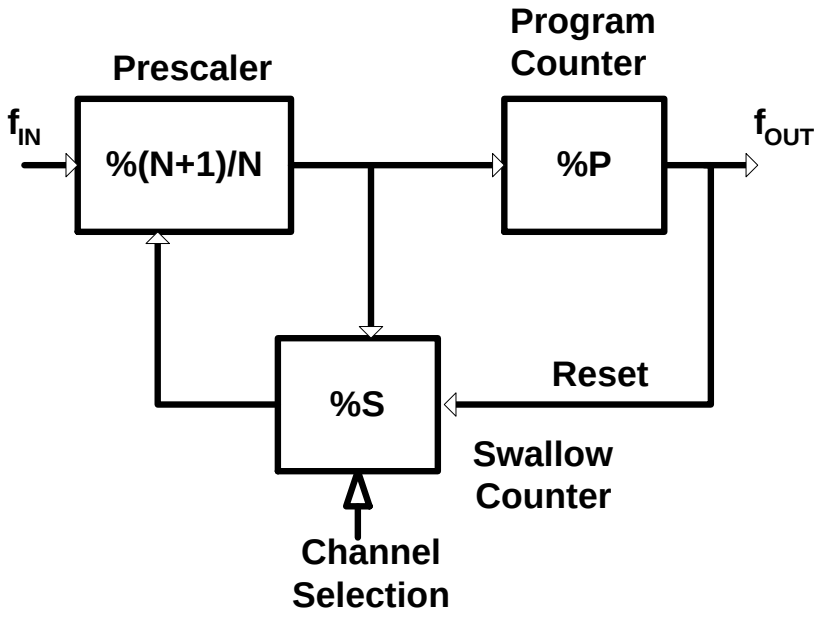
Pulse Swallow Counter

- Pulse swallow counter is used to lower power consumption of synchronous divider
- Counter consists of
  - Dual modulus prescaler which divides by N+1 or N according to its logic input
  - Pulse swallow counter which divides the input frequency by S
  - Program counter which divide the input by P

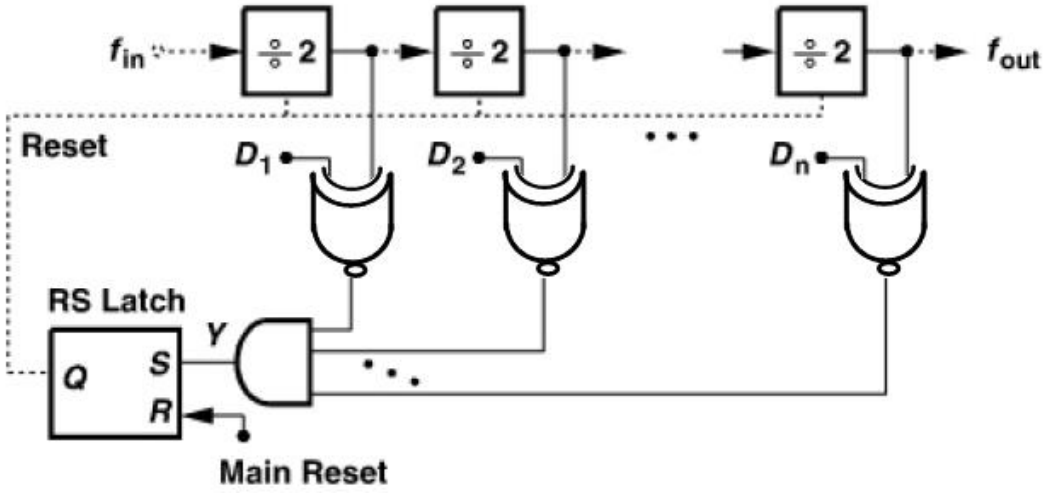


Pulse Swallow Counter

- Prescaler divides the input by N+1 then gives S counter one pulse
- After the S counter receives S pulses it changes the modulus of prescaler to divide by N and holds its state
  - The main input require to receive (N+1)×S pulses
- The P counter so far received S pulses and requires (P-S) pulses to return to its starting state
  - The main input require to receive N×(P-S) pulses
- The total number of pulses needed is (N+1)S+N(P-S)=PN+S
- Note that P must be greater than S (P>S)



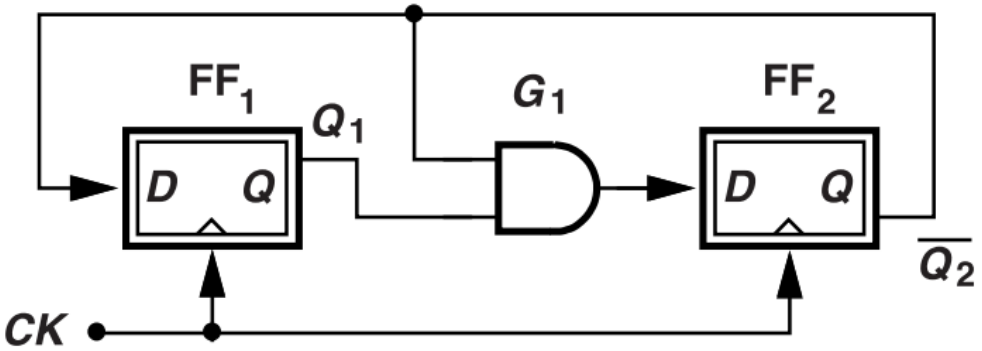
Swallow Counter

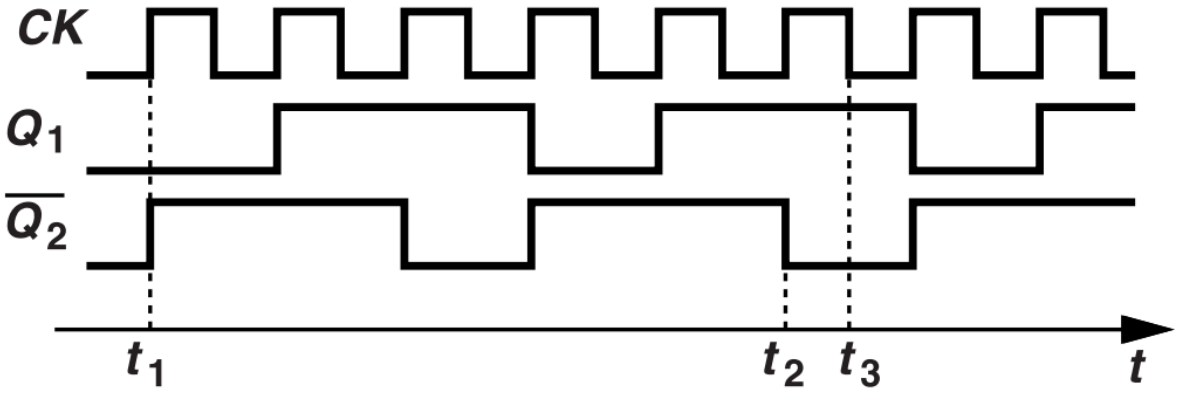


- Asynchronous logic
- After reaching the desired division ratio the counter holds its state
- After receiving reset pulse counter goes back to active mode

Dual Modulus Prescaler

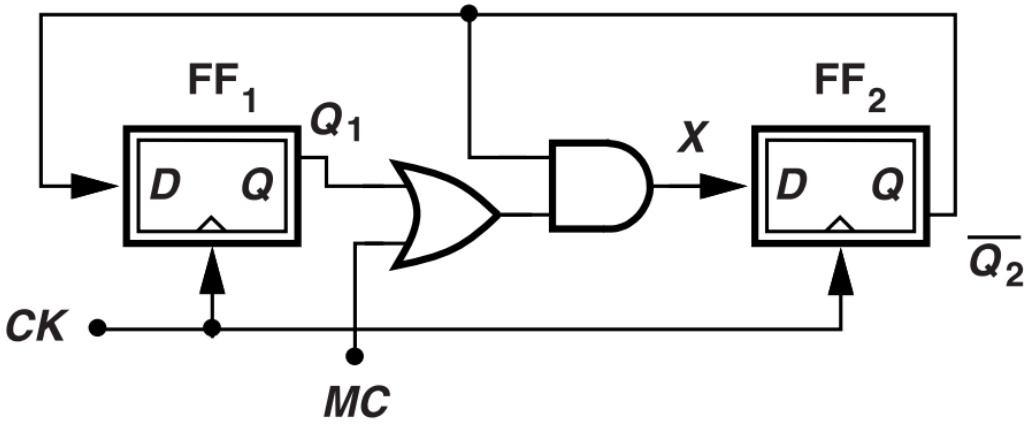
- Divide by 3
- Suppose that $\overline{Q}_2Q_1$ initially is 10
- $\overline{Q}_2Q_1$= 11, 01, 10 and then repeats



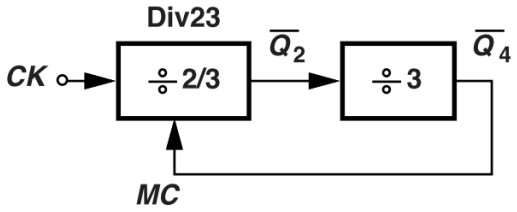


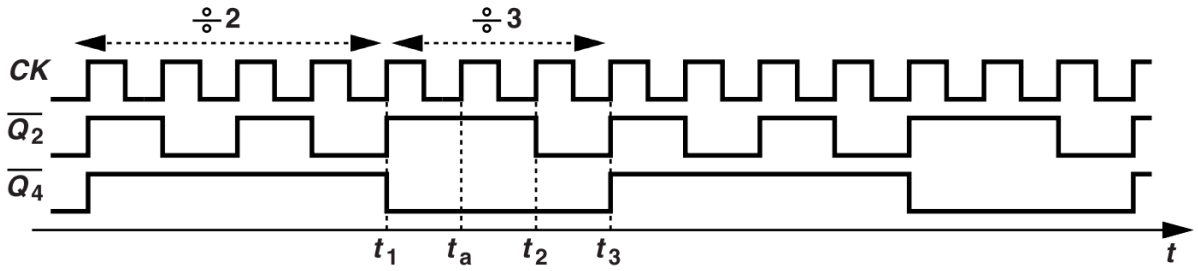
Dual Modulus Prescaler

- If MC=0 circuit is a divide by 3
- If MC=1 circuit is a divide by 2 (feedback from Q_2 to D_2).

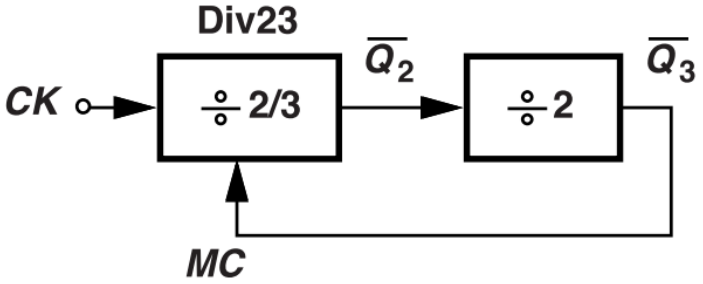


Modular Divider

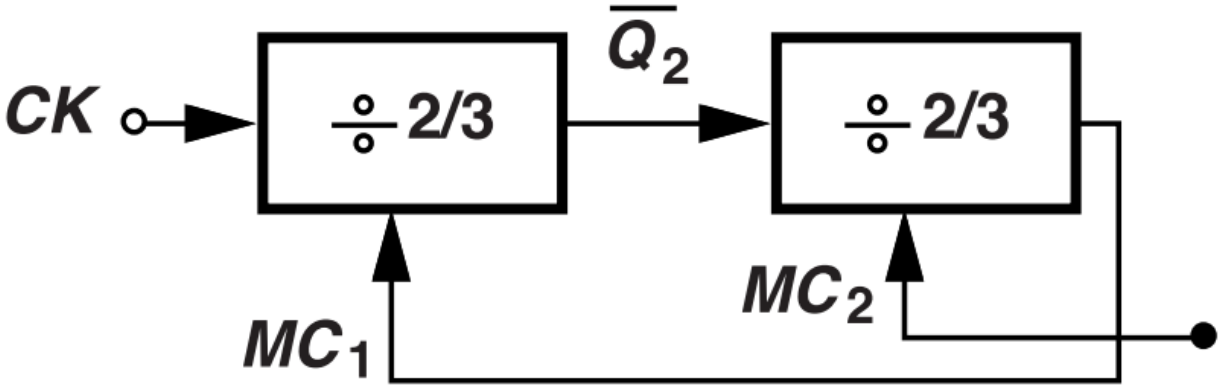




- Divide by 7 can be obtained by cascading divide by 2/3 and divide by 3
- If divide by 3 is replaced by divide by 2 then we obtain divide by 5

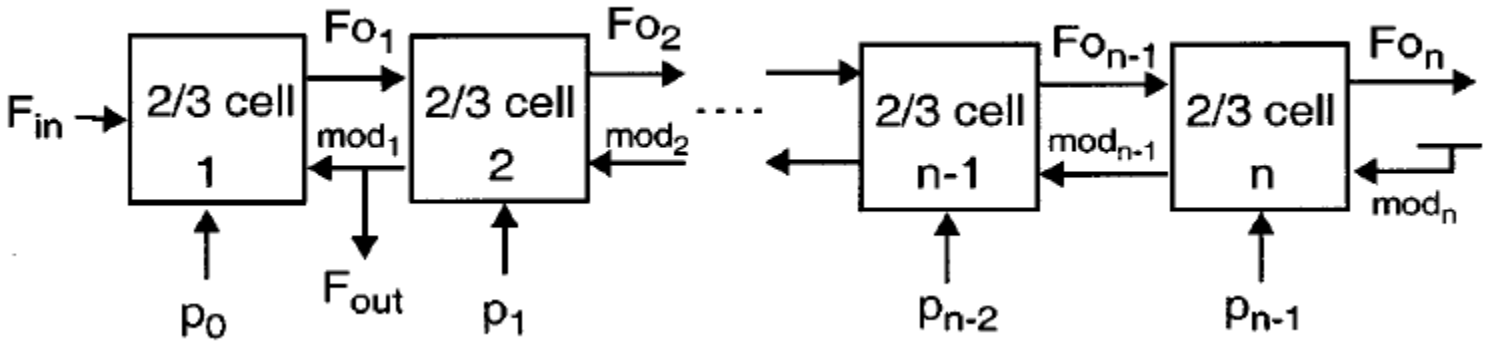


Modular Divider

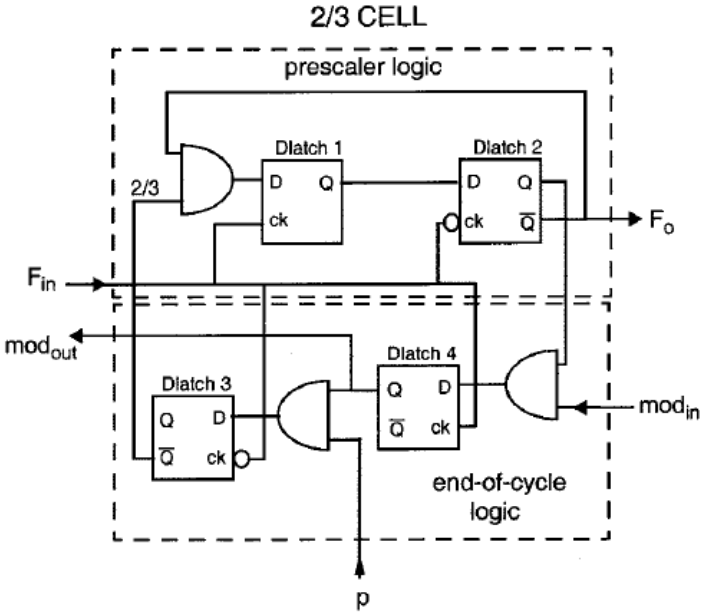


- If MC2=0, then total division by 7. If MC2=1. so division by 5
- If both MC1, MC2=1 then divide by 4
  - Need to force MC1=1
- If MC1=1, MC2=0 then divide by 6

Modular Divider

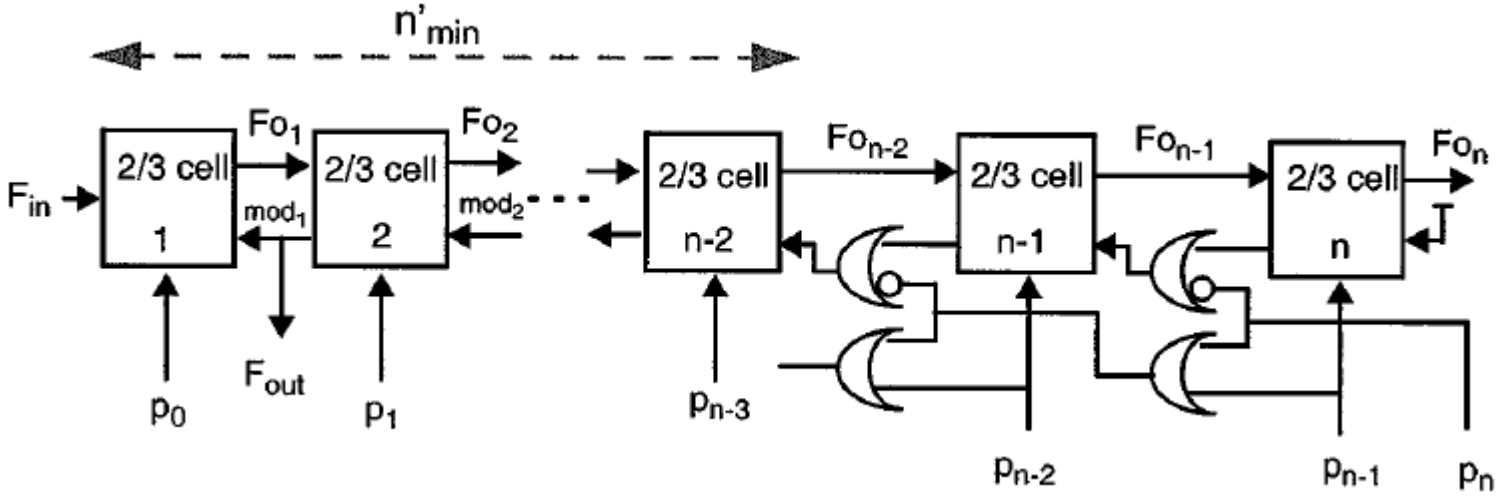


- Saves layout time
- Output is sampled at input clock speed
  - Low jitter on output
- $Tout=2^nT_{in}+2^{n-1}p_{n-1}T_{in}+\ldots+2T_{in}p_1+T_{in}p_0$
- Slow response if division ratio change, might be challenge for fractional PLL



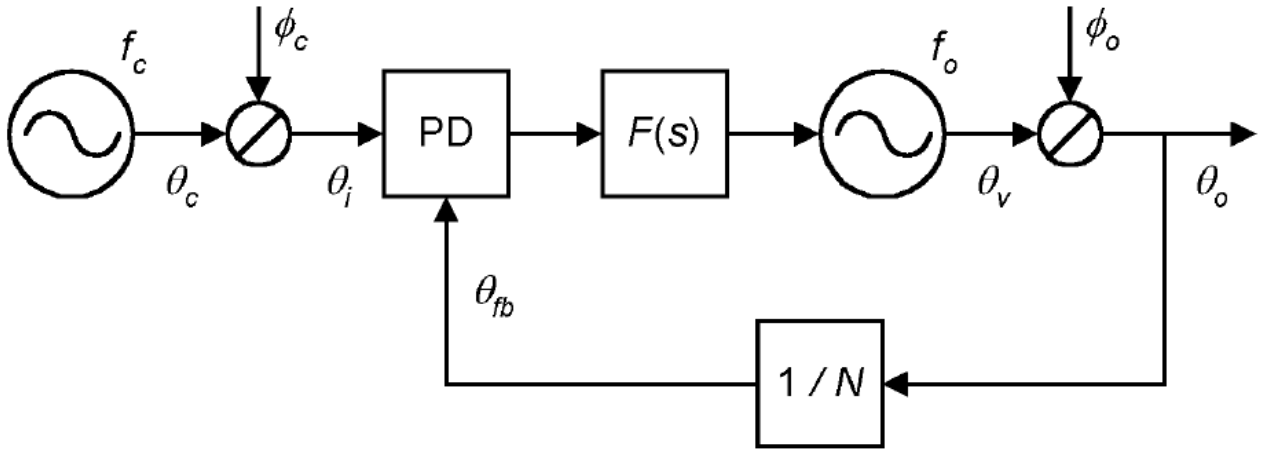
Modular Divider

- Modified architecture to extend division ratio



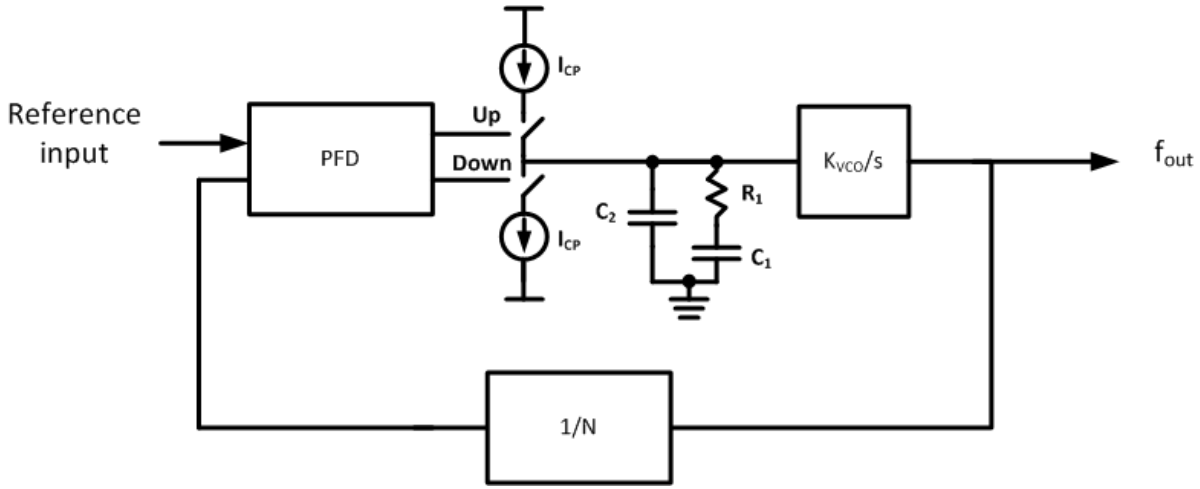
- C. S. Vaucher, I. Ferencic, M. Locher, S. Sedvallson, U. Voegeli and Z. Wang, "A family of low-power truly modular programmable dividers in standard 0.35-/spl mu/m CMOS technology," in IEEE Journal of Solid-State Circuits, vol. 35, no. 7, pp. 1039-1045, July 2000

Effect of Frequency Division on Phase Noise



- Phase noise also gets divided by division ratio
- Assume timing jitter is the same, if frequency is lower the relative error is less
  - $\phi_n = 2\pi f_0 t_n$

Crystal Oscillator



- PLL reference signal should be
  - Very accurate (0.01%-0.001%)
  - Has very low noise
- Crystals are used to achieve both requirement

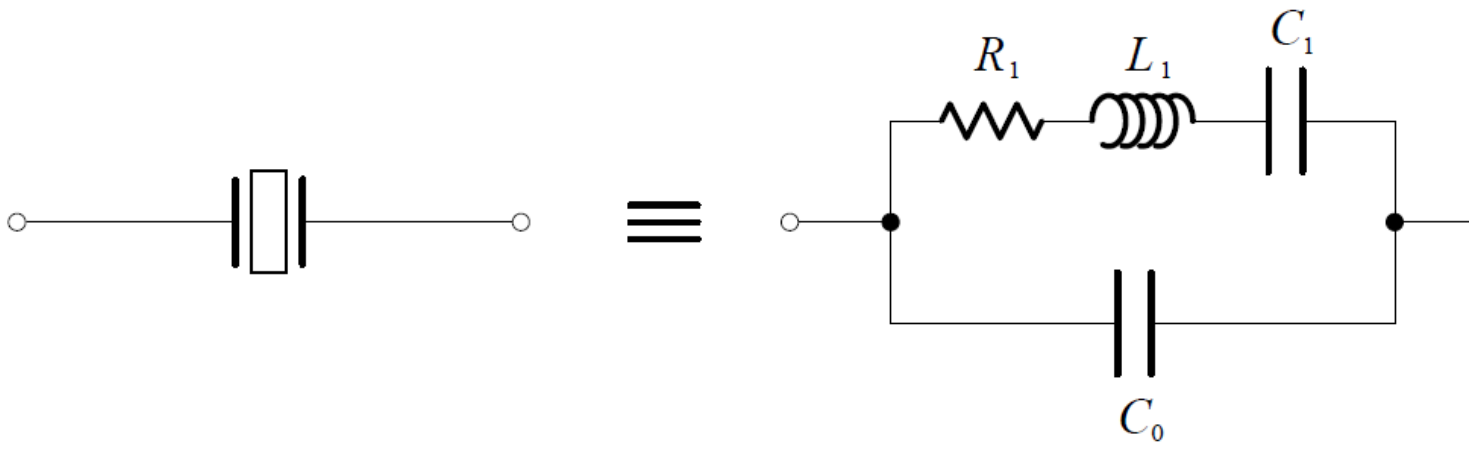
E. A. Vittoz, M. G. R. Degrauwe and S. Bitz, "High-performance crystal oscillator circuits: theory and application," in IEEE Journal of Solid-State Circuits, vol. 23, no. 3, pp. 774-783, June 1988

Crystal Oscillator

- Crystal are made of piezoelectric material
  - Piezoelectric Material converts electric signals to mechanical vibrations
  - Mechanical resonance frequency is set by physical dimensions
  - Quartz is the most commonly used material
  - There are many different ways to cut crystal, most common is AT cut

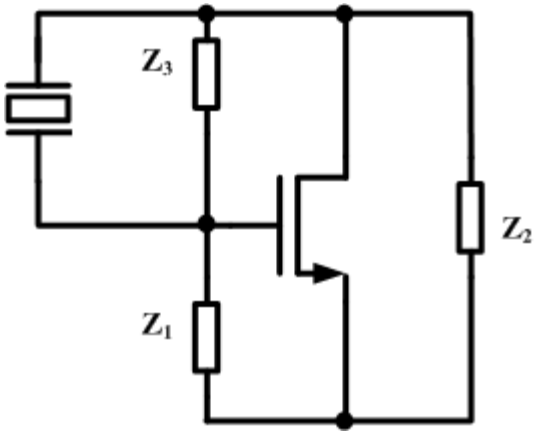
Crystal Model

- Crystals can be modeled as RLC circuit
- Has very high quality (10^4 to 10^6)
- For example a 10MHz crystal
  - R=100Ω, L=159mH, C=1.59fF, Q=10^5



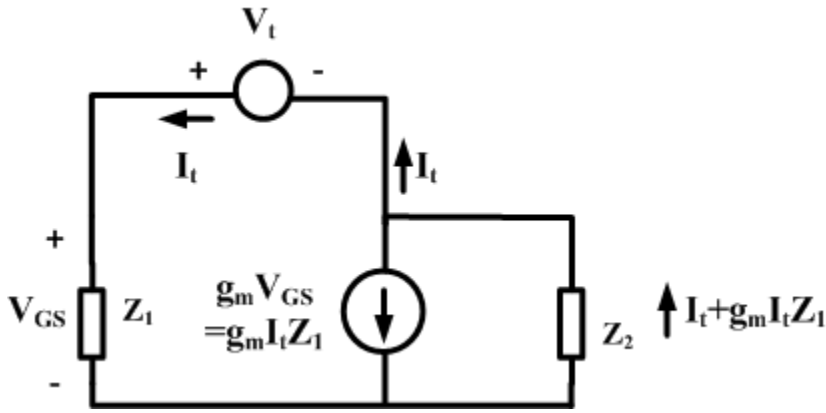
Basic Three Point Oscillator

- Ground can be at source or drain of gate
- If ground is chosen to be at source node, topology is called Pierce oscillator
- Pierce oscillator requires two external pins on chip while Colpitts/Clapp oscillator require only one external pin



Small Signal Model of Crystal Oscillator

Ignoring the affect of Z_3



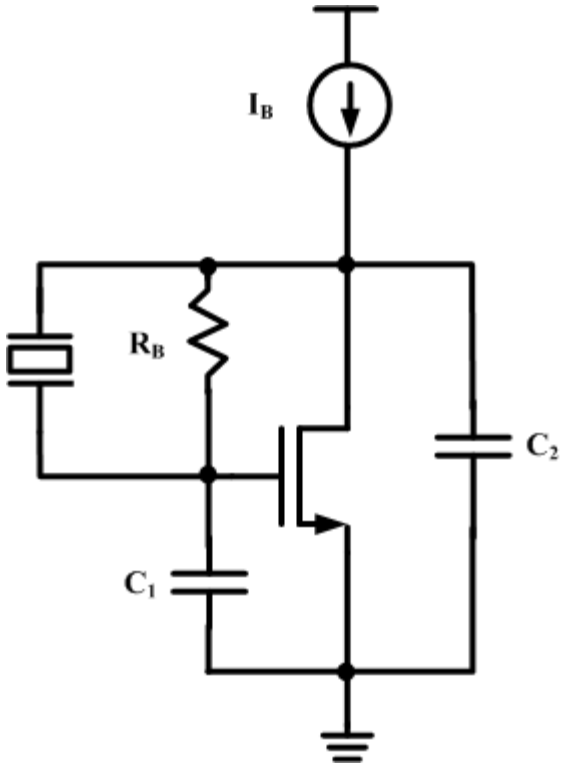
- $V_t=I_t(Z_1+Z_2+gmZ_1Z_2)$
- $Z_{in} = \frac{V_t}{I_t} = Z_1 + Z_2 + g_m Z_1 Z_2$
- If Z_1 and Z_2 are capacitors then
- $Z_{in} = \frac{V_t}{I_t} = \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2}$
- To form oscillator inductance is needed between drain and gate

Crystal Impedance

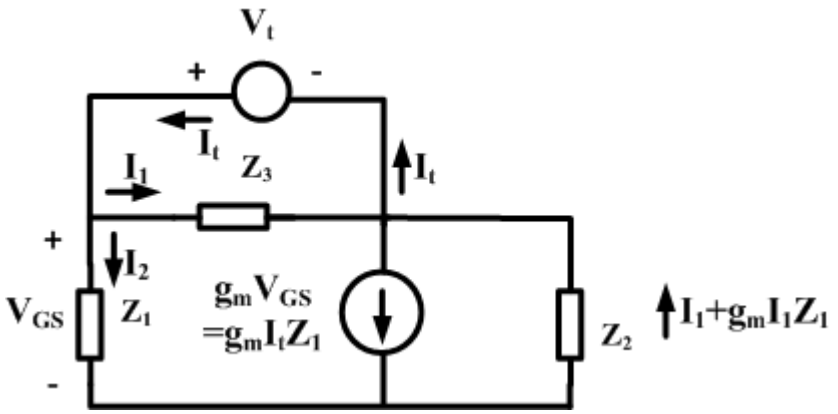
- $Z_m = R + j\omega L_m - \frac{j}{\omega C_m} = R + \frac{j}{\omega_m C_m}\left(\frac{\omega}{\omega_m} - \frac{\omega_m}{\omega}\right)$
- Define pulling factor $p = \frac{\omega - \omega_m}{\omega_m}$, usually p<<1
- $Z_m \approx R + \frac{j2p}{\omega C_m}$
- Oscillation condition Z_{total} =0
- $R + \frac{j2p}{\omega C_m} + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_2} - \frac{g_m}{\omega^2 C_1 C_2}$=0
- If C_1=C_2=1PF, C_m=1fF, then p=0.001

Crystal Oscillator Circuit

- Start up Rm is higher that steady state Rm
- Current at startup need to be higher than current at steady state
- Automatic gain control can be also used
- What the relation ship between V_G and V_D?
- Where is the output?

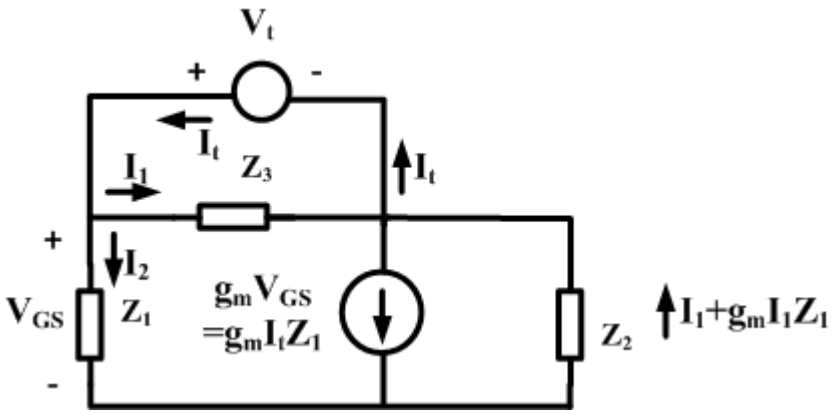


Effect of Z3



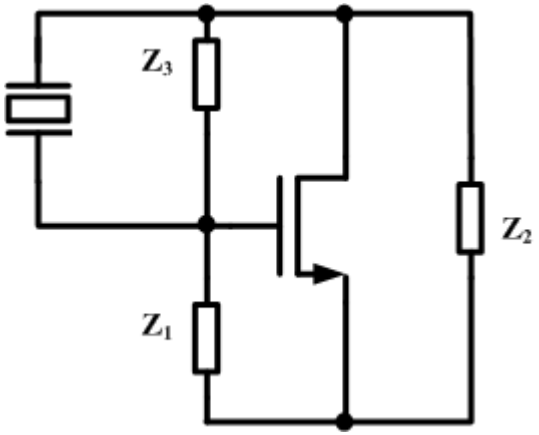
- $Z_{in} = \frac{Z_1Z_3+Z_2Z_3+g_mZ_1Z_2Z_3}{Z_1+Z_2+Z_3+g_mZ_1Z_2}$
- If Z_1, Z_2 and Z_3 are capacitors then
- $\mathrm{Re}(Z_{in}) = \frac{-g_mC_1C_2}{(g_mC_3)^2+\omega^2(C_1C_2+C_2C_3+C_1C_3)^2}$
- $\mathrm{Im}(Z_{in}) = \frac{g_m^2C_3+\omega^2(C_1+C_2)(C_1C_2+C_2C_3+C_1C_3)}{\omega[(g_mC_3)^2+\omega^2(C_1C_2+C_2C_3+C_1C_3)^2]}$

Effect of Z3



- Re(Z_{in})=$\frac{-g_m C_1 C_2}{(g_m C_3)^2+\omega^2(C_1C_2+C_2C_3+C_1C_3)^2}$
- Max –ve impedance is obtained when
- $g_m = g_{mopt} = \omega\left(C_1 + C_2 + \frac{C_1C_2}{C_3}\right)$
  - Max –ve impedance Re(Z_{in})=$\frac{-1}{2\omega C_3\left(1+\frac{C_1+C_2}{C_1C_2}C_3\right)}$

Which Topology is Better?



- Where should we put ground?