ECE 621
Signaling & Synchronization
Fall 2020

Topic 4
RX Circuitry

Sameh A. Ibrahim

Ain Shams University

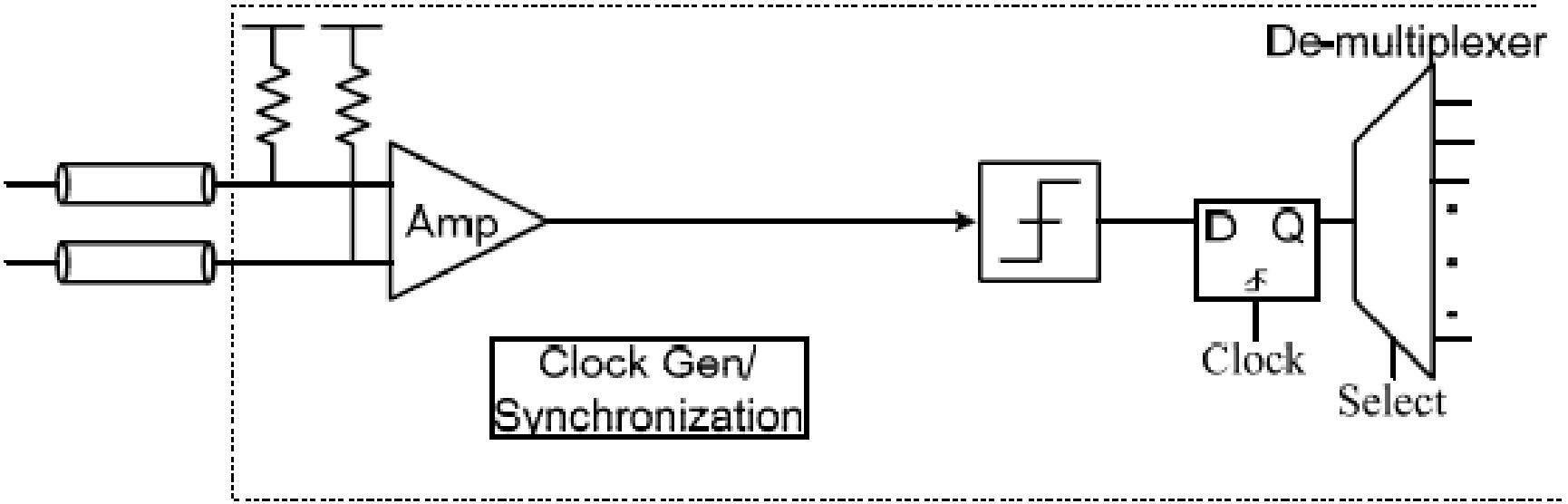
ICL

(Courtesy of S. Pamarti – UCLA, S. Palermo – TAMU, E. Alon – UCB, and D. Allstot – UW)

Outline

- **RX Overview**
  - Parameters
  - Architecture choices
- **RX Amplifiers**
  - Pre-amplifiers
  - Bandwidth extension techniques
- **Clocked Comparators**
  - Circuits
  - Characterization techniques
- **Demultiplexing**
- **RX Sensitivity**
  - Offset
  - Noise

Receiver Block Diagram



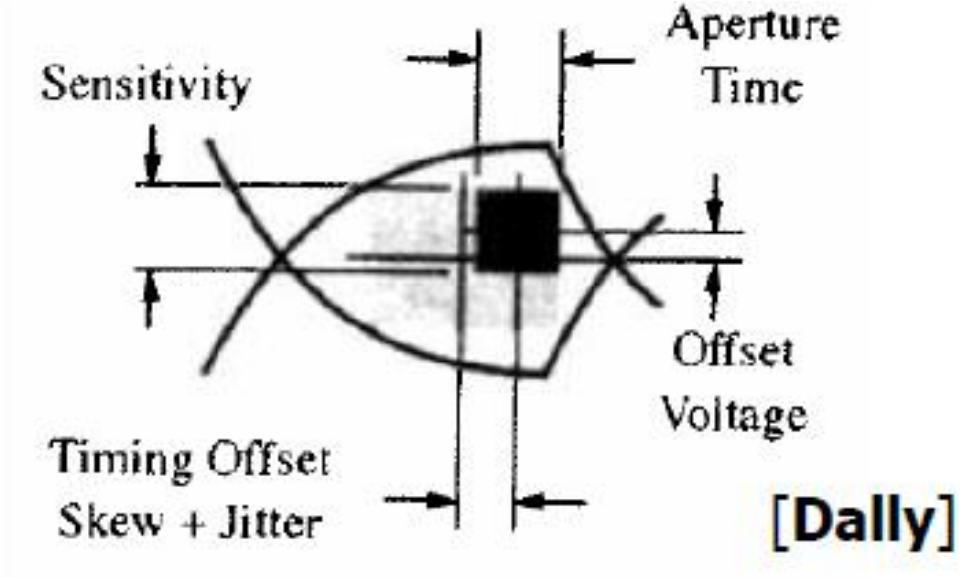
- **Goals**
  - High bit rate
  - Low power consumption
  - Low BER
    - Good voltage/current and timing margins

Receiver Components

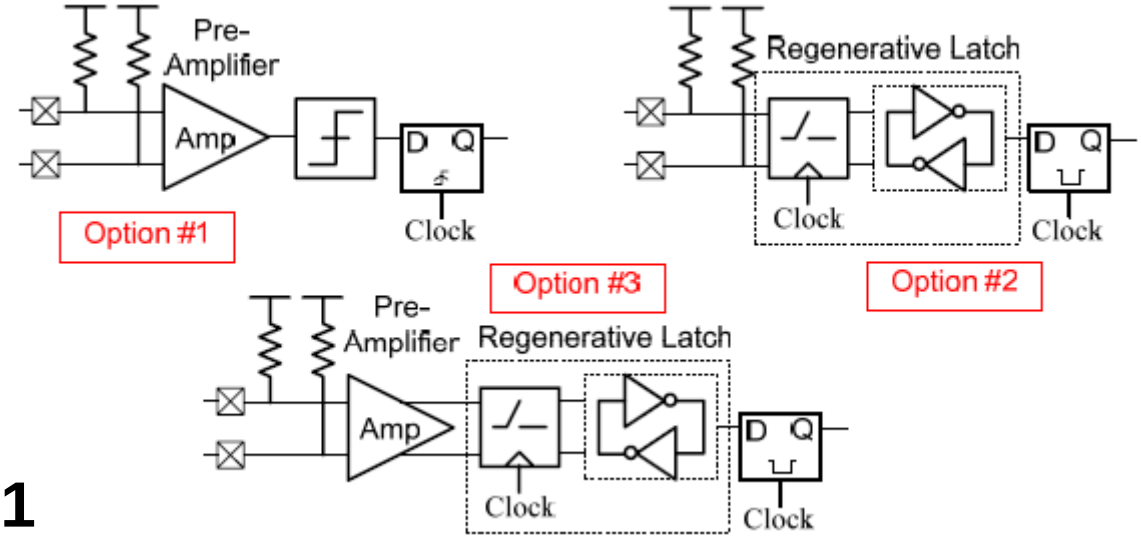
- **Pre-amplifier**
  - Compensates for average channel loss (not equalization).
  - Can be used also for equalization, offset correction, and fix sampler common-mode.
  - Must provide gain at high-bandwidth corresponding to full data rate.
- **Sampler / Slicer**
  - Extracts the data from the received signal.
  - Can be implemented with static amplifiers or clocked-regenerative amplifiers
    - Clock regenerative amplifiers are more power efficient.
- **De-multiplexer**
  - Separate data to supply multiple, slower, data destinations.

Receiver Parameters

- **RX sensitivity, offsets in voltage and time domain, and aperture time are important parameters**
- **Minimum eye width is determined by aperture time plus peak-to-peak timing jitter.**
- **Minimum eye height is determined by sensitivity plus peak-to-peak voltage offset.**



Receiver Architecture Choices



- **Option 1**
  - If wide bandwidth, high gain pre-amplifier is available.
- **Option 2**
  - If received signal is large, or
  - If wide bandwidth, high gain pre-amplifier is unavailable.
- **Option 3**
  - Very low received signal
  - Wide bandwidth, but low gain pre-amplifier

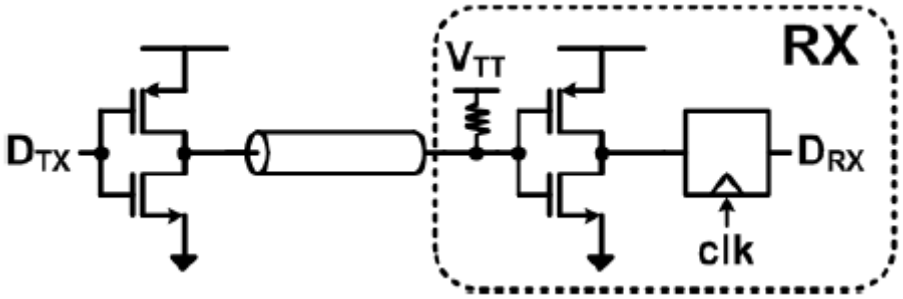
Outline

- RX Overview
  - Parameters
  - Architecture choices
- **RX Amplifiers**
  - Pre-amplifiers
  - Bandwidth extension techniques
- **Clocked Comparators**
  - Circuits
  - Characterization techniques
- **Demultiplexing**
- **RX Sensitivity**
  - Offset
  - Noise

Pre-Amplifier Goals

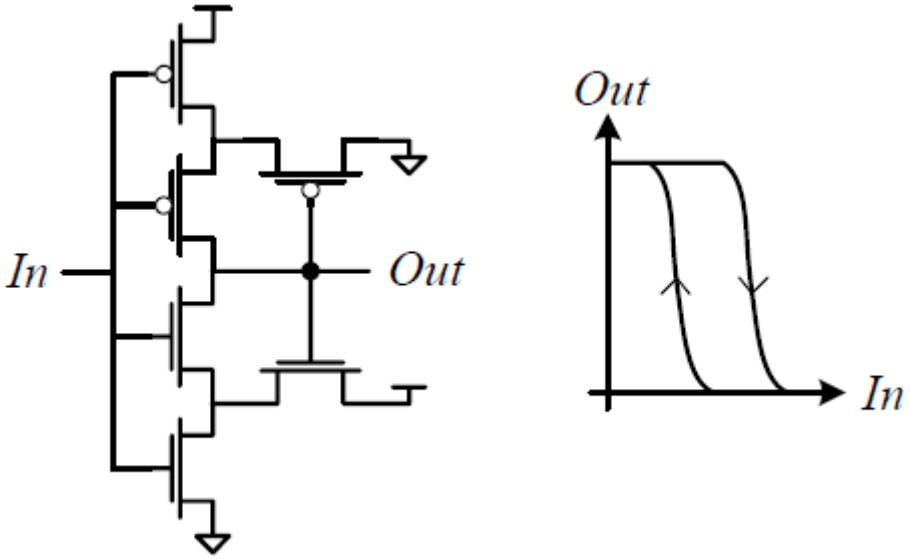
- **Provide a large swing input to the sampler/slicer.**
- **Filter noise outside the received signal bandwidth.**
- **Issues**
  - Power consumption
  - Input offset and its variability
  - High frequency operation

A Simple Single-Ended Pre-Amplifier



- **CMOS inverter is one of the simplest RX pre-amplifiers.**
- **Termination voltage, V_{TT}, should be placed near inverter trip point.**
- **Issues**
  - Limited gain (<20)
  - High PVT variation results in large input referred offset.
  - Single-ended operation makes it both sensitive to and generate supply noise.

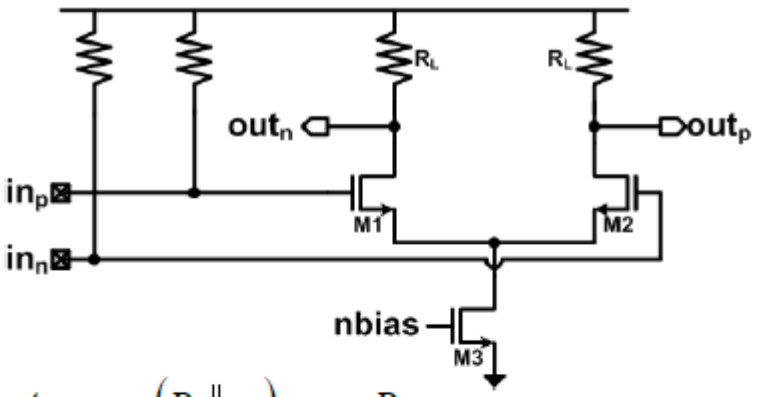
Schmitt Trigger Single-Ended Pre-Amplifier



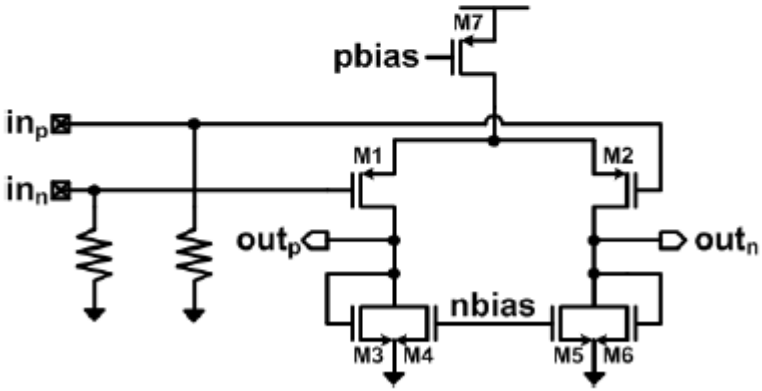
- **Different thresholds for pull-down and pull-up**
  - Better noise margin than the inverter
- **Reduced sensitivity to high frequency input noise**
  - Due to hysteresis of the Schmitt trigger
- **Still difficult to operate at high data rates**
  - The switching thresholds still vary with process, voltage, and temperature

Differential Pre-Amplifiers

- **Differential input amplifiers often used as input stage in high performance serial links.**
  - Rejects common-mode noise.
  - Sets input common-mode for the comparator.
- **Input stage type (n or p) often set by termination scheme**
- **High gain-bandwidth product necessary to amplify full data rate signal**
- **Offset correction and equalization can be merged into the input amplifier.**
- **Can be used for single-ended RX.**
- **Output is not fully rail-to-rail.**
  - Can cascade stages for more gain.
- **Sensitive to supply noise variations**

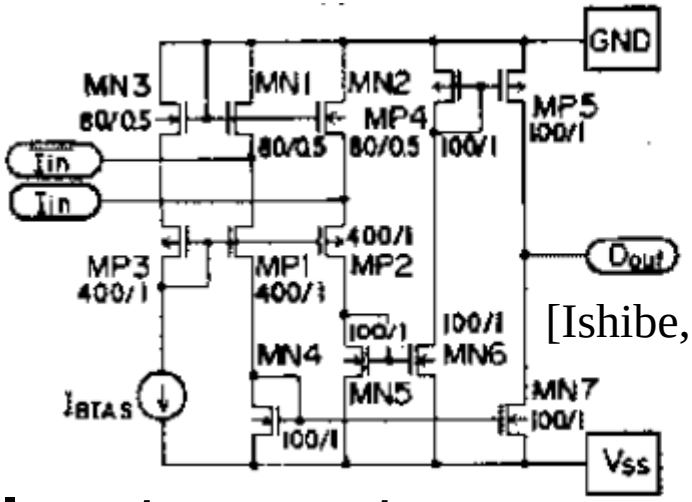


$$A_v = g_{m1}\left(R_L \| r_{o1}\right) \approx g_{m1} R_L$$

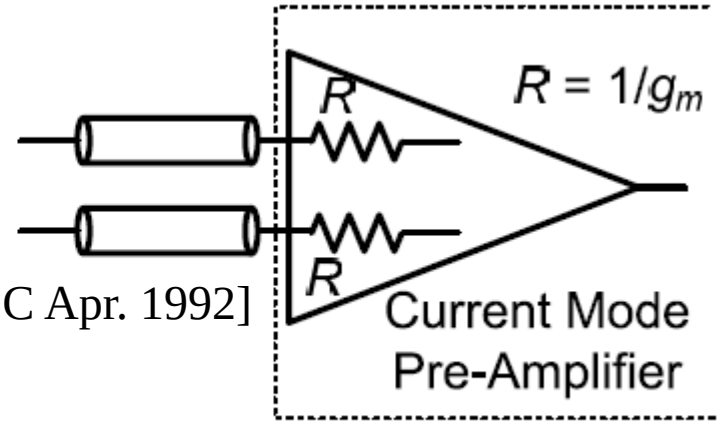


$$A_v = \frac{g_{m1}}{g_{m3} + g_{o3} + g_{o4} + g_{o1}} \approx \frac{g_{m1}}{g_{m3}}$$

Current Mode Diff. Pre-Amps

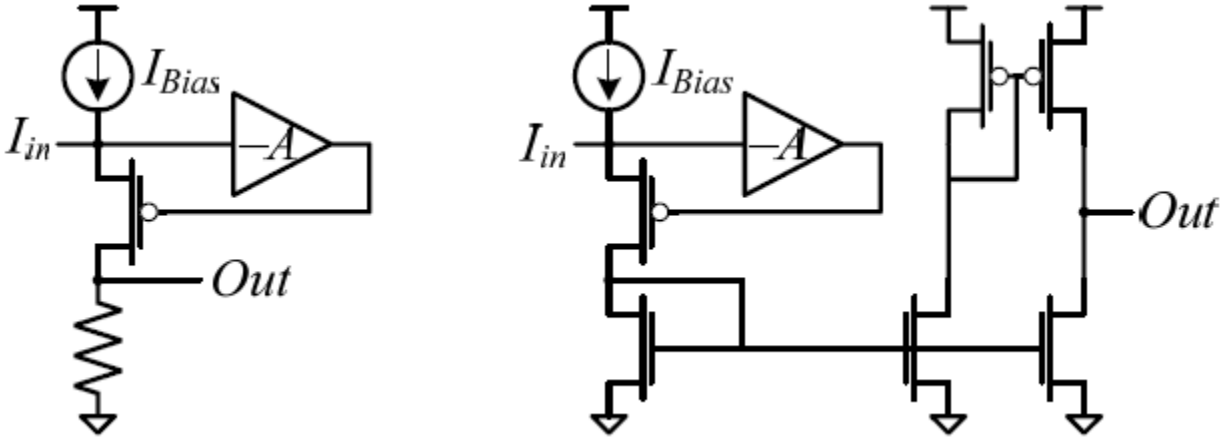


[Ishibe, JSSC Apr. 1992]



- **Input currents are amplified and subtracted from each other using current mirrors.**
  - Useful when series termination is used on the receiver.
  - Gain is obtained from current mirror ratio.
  - I–V conversion gain depends on rds of transistors.
- **T-line sees R= 1/gm.**
  - PVT variations.
  - 1/gm> 50 Ohms is likely

Reducing R_{in} in Current Mode Pre-Amps



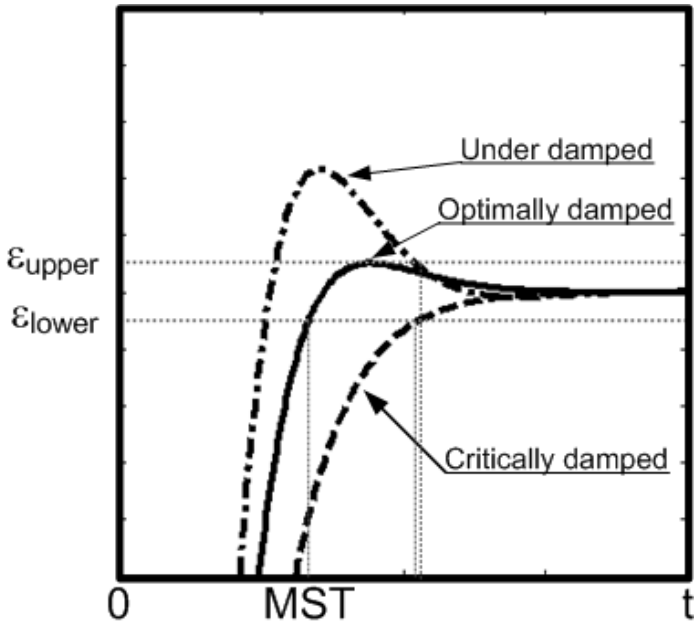
- **Negative feedback can be used to reduce R_{in}.**

$$Z_{in} \approx \frac{1}{g_m}\left(\frac{1}{1+A(s)}\right)$$

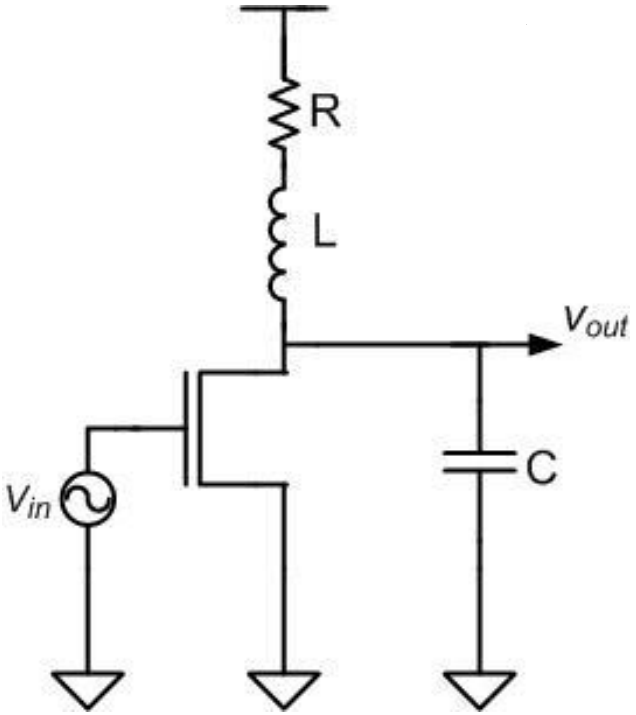
- **Maintaining loop gain at high frequencies would be power hungry.**

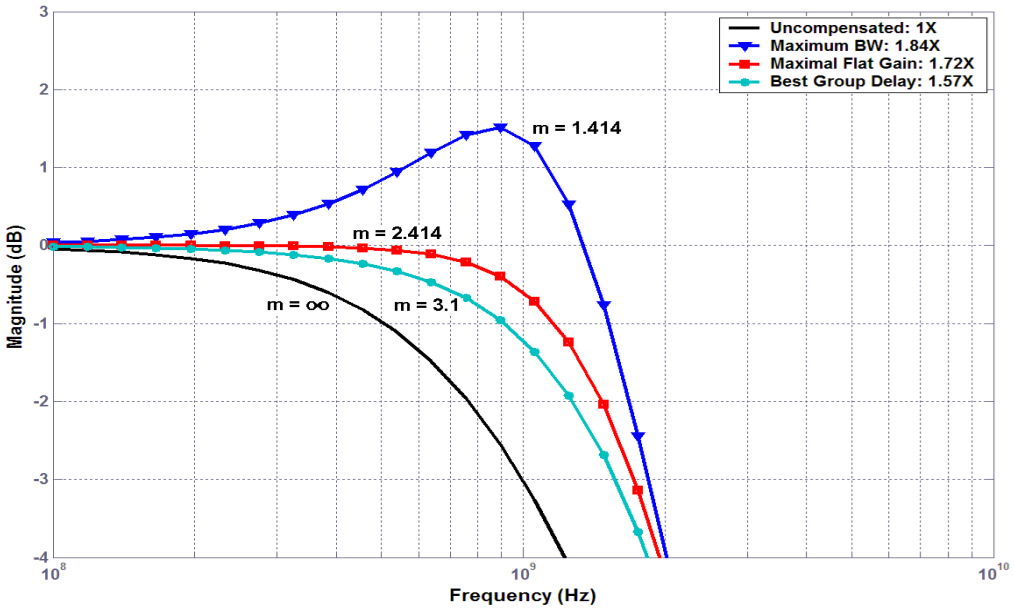
Bandwidth Extension: Terminology

- **BW extension ratio (BWER) = $f_{3dB,\,ext}$ / $f_{3dB,\,ref}$**
- **Settling Time (1%) reduction ratio (STRR) = $\tau_{s,\,ref}$ / $\tau_{s,\,ext}$**
- **Rise Time (10-90%) reduction ratio (RTRR) = $\tau_{r,\,ref}$ / $\tau_{r,\,ext}$**
- **BWER, STRR & RTRR hard to maximize simultaneously.**
  - Optimize for desired application.



BW Extension: Shunt Peaking





$$Z(s) = \frac{R + sL}{1 + sRC + s^2 LC}$$

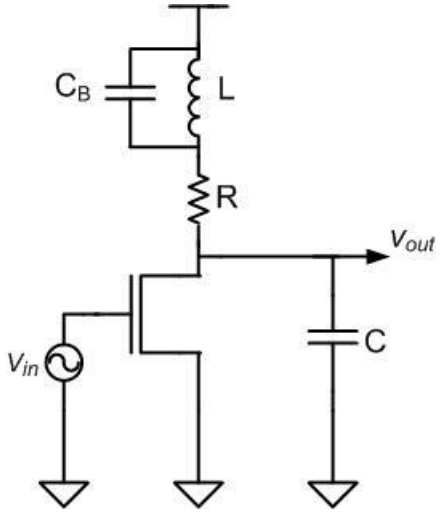
$$m = \frac{R^2 C}{L} \qquad \omega_0 = \frac{1}{RC}$$

$$Z_N(s) = \frac{1 + s/m\omega_0}{1 + s/\omega_0 + s^2/m\omega_0^2}$$

$m = \sqrt{2} \rightarrow$ 1.84X & 1.5dB Peaking

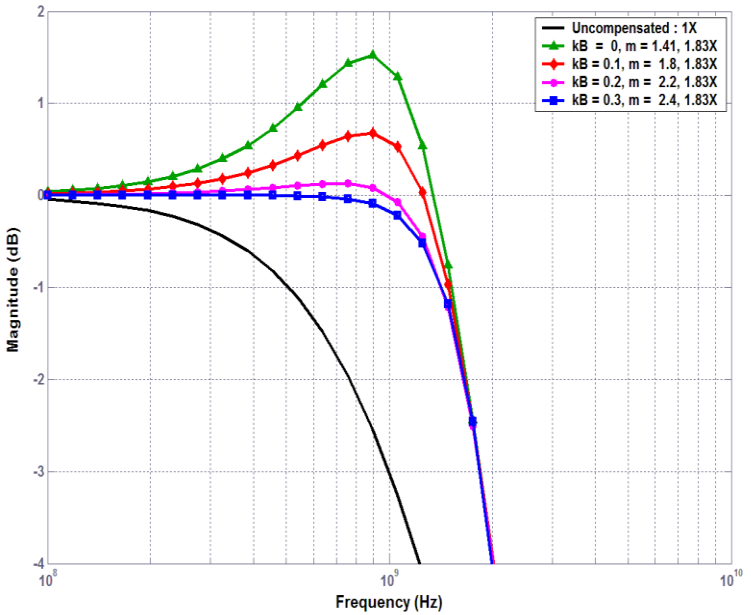
- Introduces a pole-zero pair.
- L improves impedance with freq.

BW Extension: Bridged Shunt Peaking



$$Z_N(s) = \frac{1 + \left(\frac{1}{m}\right)\frac{s}{\omega_0} + \left(\frac{k_B}{m}\right)\frac{s^2}{\omega_0^2}}{1 + \frac{s}{\omega_0} + \left(\frac{k_B + 1}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_B}{m}\right)\frac{s^3}{\omega_0^3}}$$

$$m = \frac{R^2 C}{L} \quad \omega_0 = \frac{1}{RC} \quad k_B = \frac{C_B}{C}$$



$m = 2.4$, $k_B = 0.3 \rightarrow$ 1.83X flat

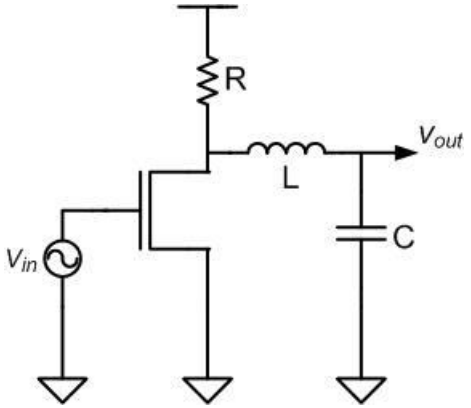
- C_B is inductor parasitics.

Bridged-Shunt Peaking Advantages

K_B	m	STRR	RTRR	BWER
0.0	1.4	0.70	2.18	1.84
0.1	2.84	2.40	1.74	1.69
0.3	2.4	1.39	1.87	1.83

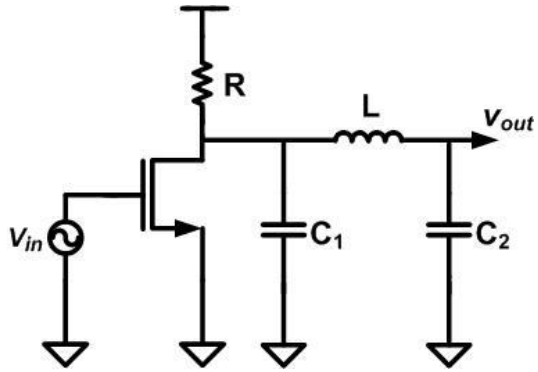
- Incorporates inductor parasitics (Add more CB if needed).
- Maximum BW possible with flat gain (No 1.5dB peaking)
- m ↑, L↓ → Smaller Area
- Area overhead for added C_B minimal

BW Extension: Series Peaking



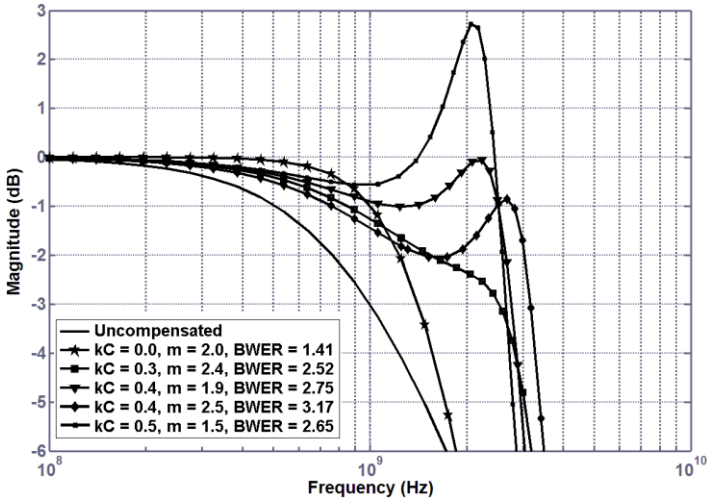
$$Z_N(s) = \frac{1}{1 + s/\omega_0 + s^2/m\omega_0^2} \qquad m = \frac{R^2C}{L} \qquad \omega_0 = \frac{1}{RC}$$

- Lack of zero
- Inferior to shunt peaking
- $m = 2 \rightarrow 1.41x$

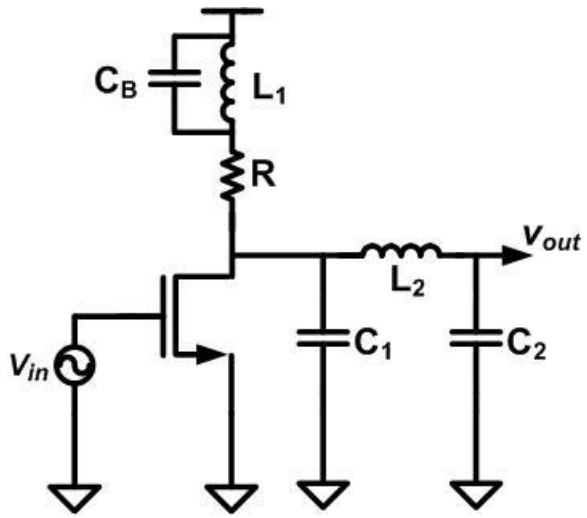


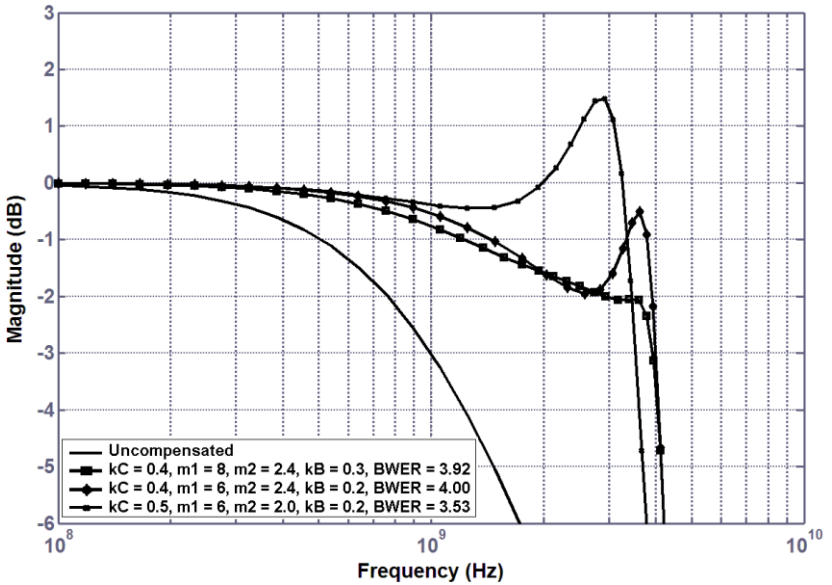
$$Z_N(s) = \frac{1}{1 + \frac{s}{\omega_0} + \left(\frac{1-k_C}{m}\right)\frac{s^2}{\omega_0^2} + \left(\frac{k_C(1-k_C)}{m}\right)\frac{s^3}{\omega_0^3}} \qquad k_C = \frac{C_1}{C}$$

- Extra Pole



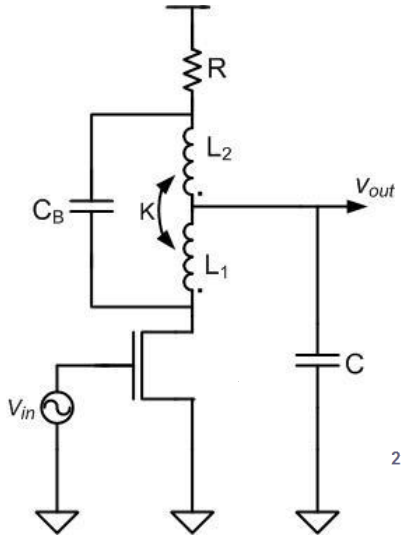
Bridged-Shunt-Series Peaking



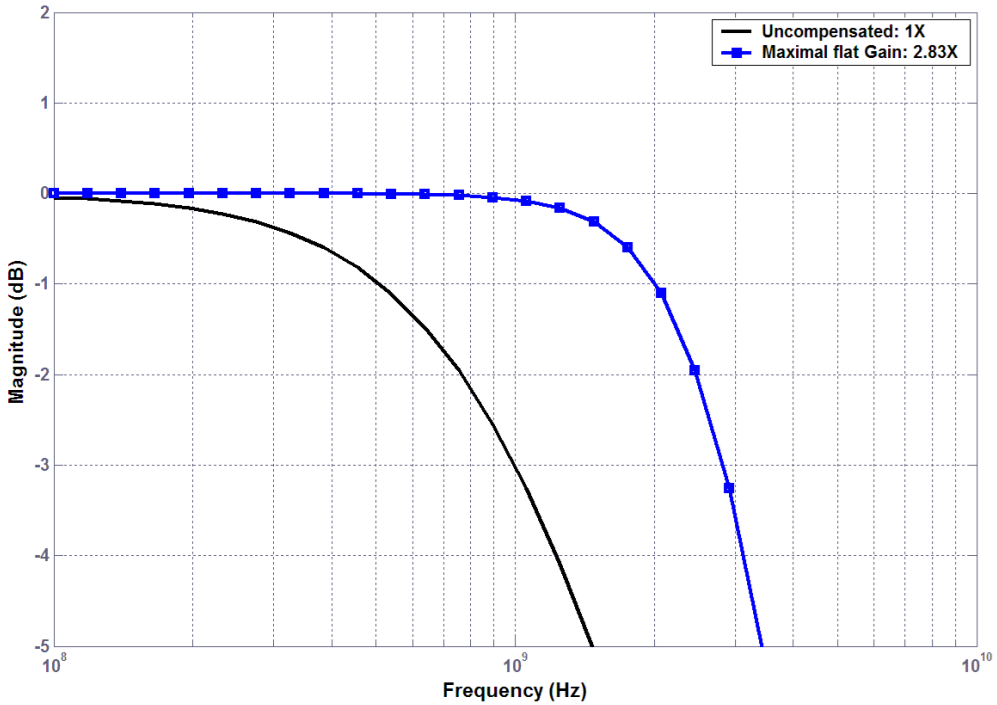


k_C	k_B	m_1	m_2	STRR	RTRR	BWER
0.4	0.0	6.3	2.6	1.32	2.73	3.47
	0.16	8	2.2	1.46	2.78	3.11
	0.2	6	2.4	0.71	2.89	4.00
	0.3	8	2.4	0.95	2.66	3.92
0.5	0.1	6	2	0.75	2.91	3.40
	0.2	6	2	0.77	2.88	3.53

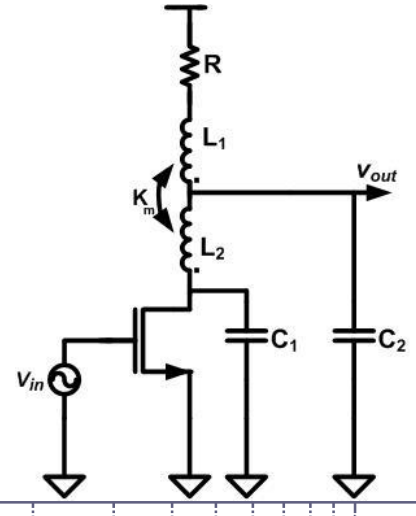
BW Extension: Symmetric T-Coil



- $L_1=L_2$
- Maximum flat BW
  - *m* = 2, k=-1/2 → 2.83x



BW Extension: Asymmetric T-Coil

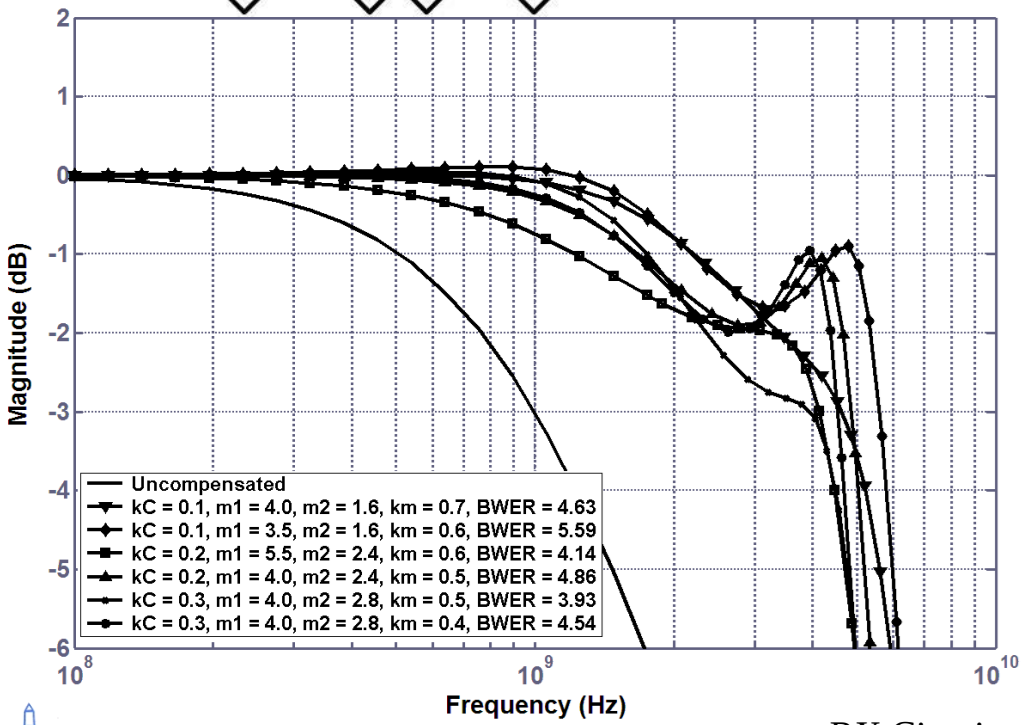


$$k_C = \frac{C_1}{C}$$

$$k_m = M / \sqrt{L_1 L_2}$$

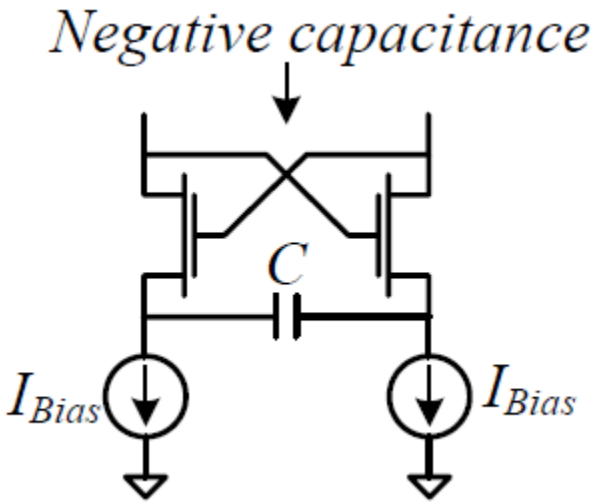
$$m_1 = \frac{R^2 C}{L_1}$$

$$m_2 = \frac{R^2 C}{L_2}$$



k_C	k_m	m_1	m_2	STRR	RTRR	BWER
0.1	0.7	4.0	1.6	1.90	4.20	4.63
	0.6	3.5	1.6	1.32	4.50	4.92
	0.6	3.5	1.2	1.57	4.43	5.59
	0.7	4.1	1.6	2.91	4.19	4.66
0.2	0.6	5.5	2.4	1.94	3.39	4.14
	0.6	3.0	2.0	1.23	3.91	4.51
	0.5	4.0	2.4	1.42	3.80	4.86
	0.7	4.6	2.2	4.11	3.35	3.34
0.3	0.5	4.0	2.8	1.54	3.40	3.93
	0.4	3.5	2.0	1.09	3.45	3.98
	0.4	4.0	2.8	1.10	3.52	4.54
	0.6	5.0	2.6	3.70	3.06	3.07

BW Extension: Negative capacitance



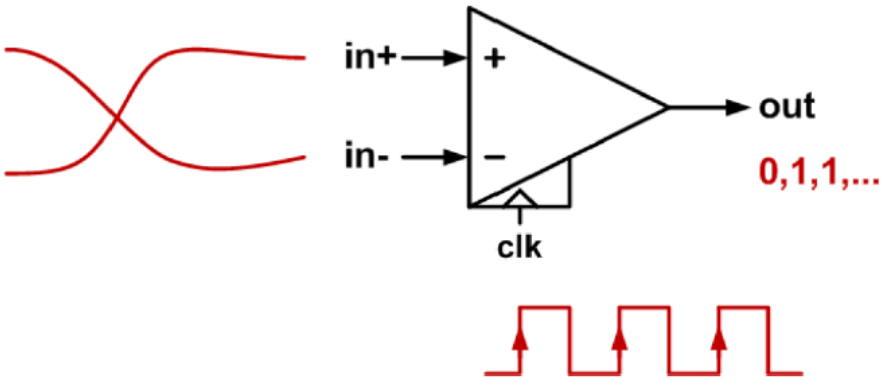
- **Active reduction of capacitance**
  - Use positive feedback to obtain effective negative capacitance.
- **Have to sustain loop gain past the signal bandwidth.**
  - Difficult and/or power hungry

Outline

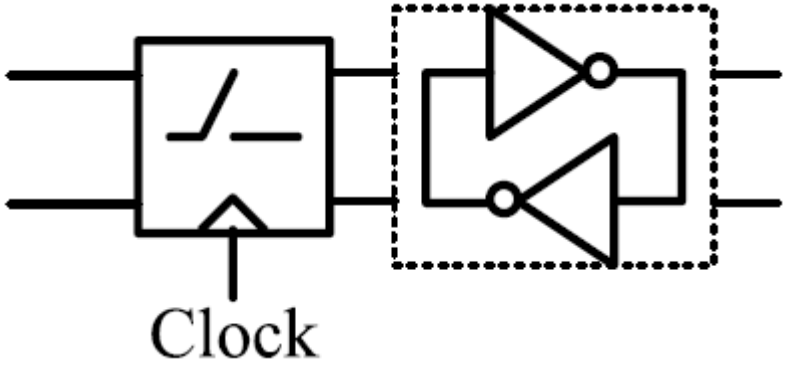
- RX Overview
  - Parameters
  - Architecture choices
- RX Amplifiers
  - Pre-amplifiers
  - Bandwidth extension techniques
- **Clocked Comparators**
  - Circuits
  - Characterization techniques
- **Demultiplexing**
- **RX Sensitivity**
  - Offset
  - Noise

RX Clocked Comparators

- **Also called regenerative amplifier, sense-amplifier, flip-flop, latch.**
- **Samples the continuous input at clock edges and resolves the differential to a binary 0 or 1.**
- **Characteristics**
  - Offset and hysteresis (hysteresis is data dependent)
  - Sampling aperture, timing resolution, uncertainty window
  - Regeneration gain, voltage sensitivity, metastability
  - Random decision errors, input-referred noise

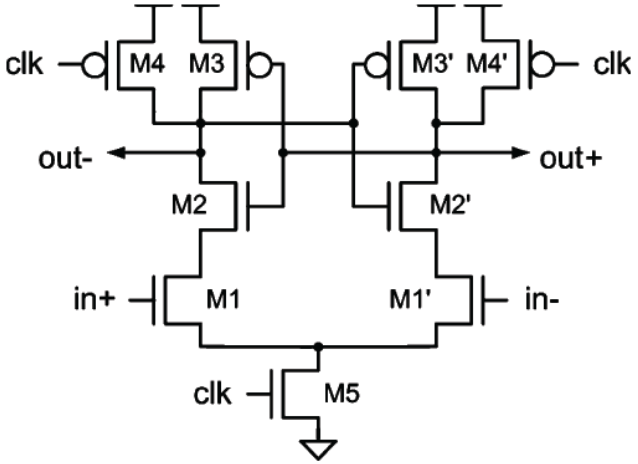


Regenerative Latch Basics

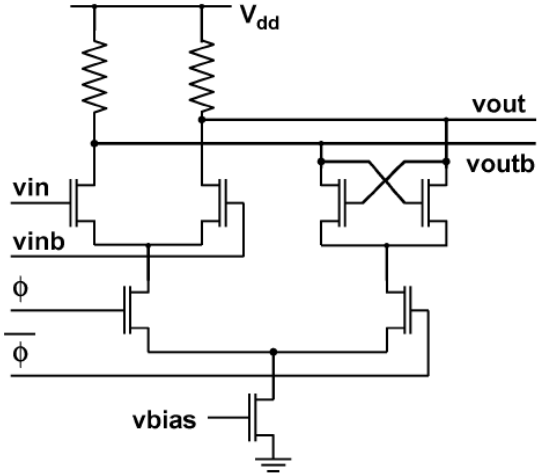


- **Operation**
  - Track phase: Some amplification is achieved (normal and regenerative)
  - Hold/Reset phase: In some versions, more amplification (+ve feedback) is achieved. In other versions, the held value is reset.
- **Requirements**
  - Low input capacitance
  - Small setup-hold window, high sampling bandwidth
  - Low power consumption

Dynamic Comparator Circuits



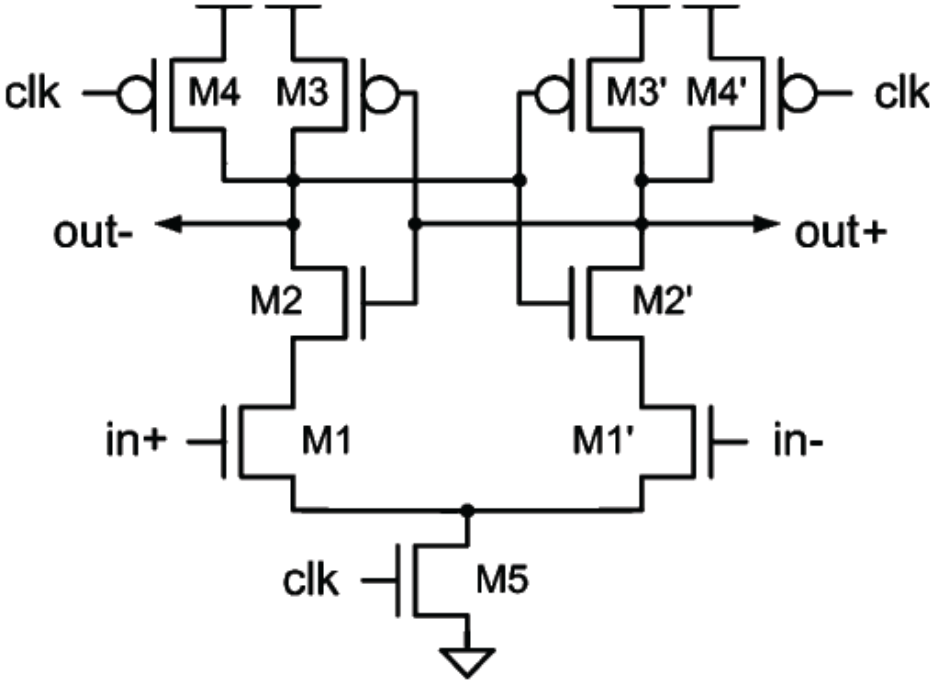
Strong-Arm Latch

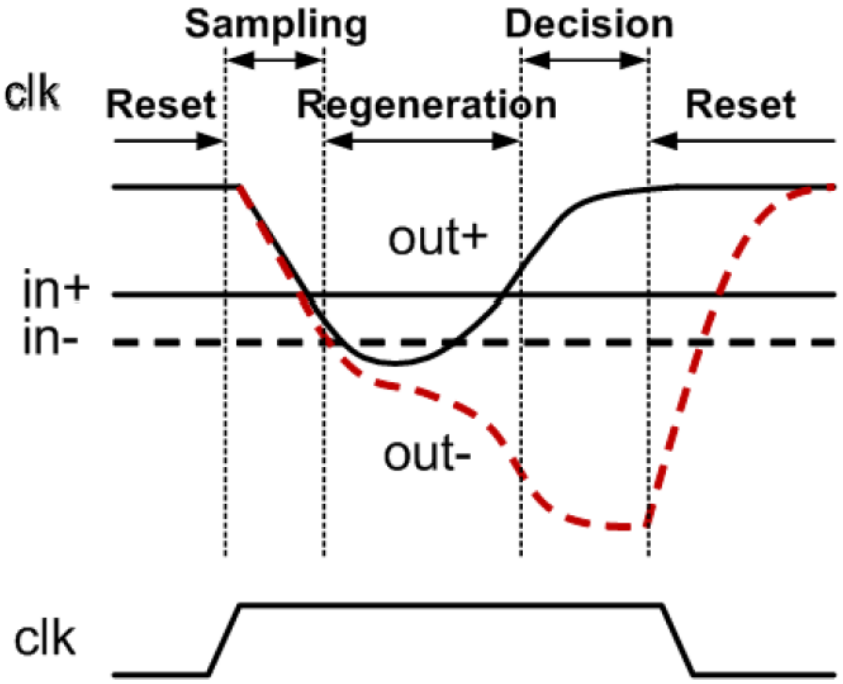


CML Latch

- **To form a flip-flop**
  - After strong-arm latch, cascade an R-S latch
  - After CML latch, cascade another CML latch
- **Strong-Arm flip-flop has the advantage of no static power dissipation and full CMOS output levels.**

StrongARM Latch Operation

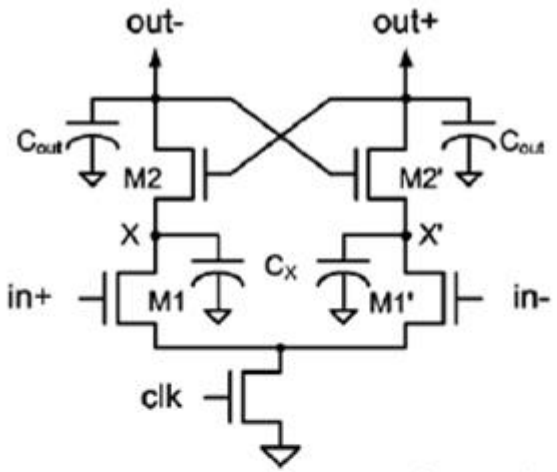


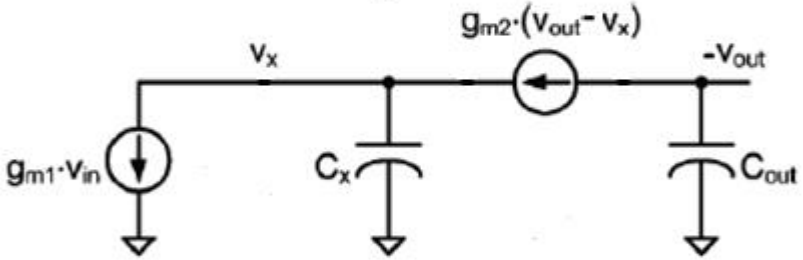


- **4 operating phases: reset, sampling, regeneration, and decision**

StrongARM Latch: Sampling Phase

- Sampling phase starts when clk goes high, t_0, and ends when PMOS transistors turn on, t_1.
- M1 pair discharges X/X'.
- M2 pair discharges out+/-.

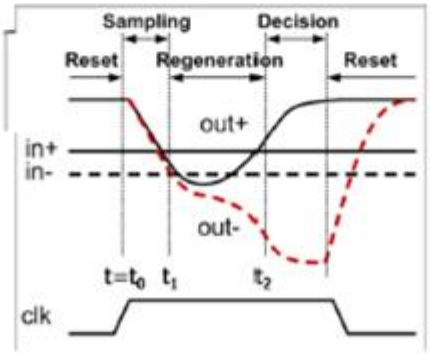




$$\frac{v_{out}(s)}{v_{in}(s)} = \frac{g_{m1}g_{m2}}{sC_{out}C_x\left(s + \frac{g_{m2}(C_{out} - C_x)}{C_{out}C_x}\right)}$$

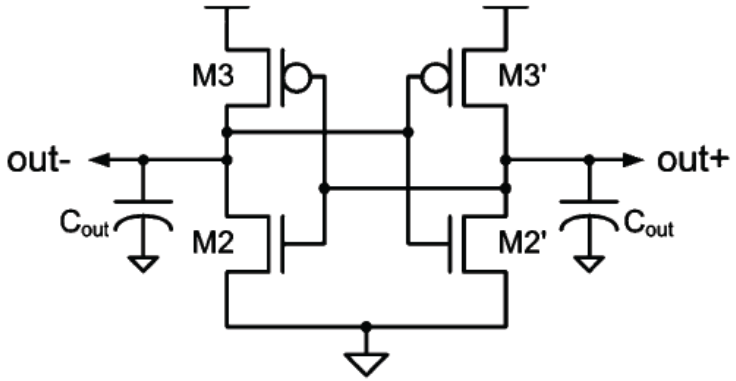
$$\cong \frac{g_{m1}g_{m2}}{s^2 C_{out}C_x} = \frac{1}{s^2 \tau_{s1}\tau_{s2}}$$

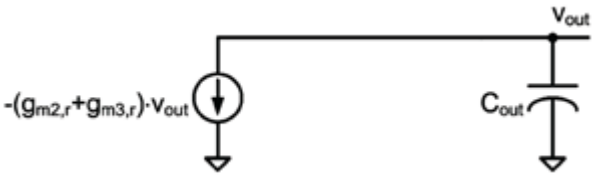
where $\tau_{s1} \equiv C_x / g_{m1}$, $\tau_{s2} \equiv C_{out} / g_{m2}$



StrongARM Latch: Regeneration

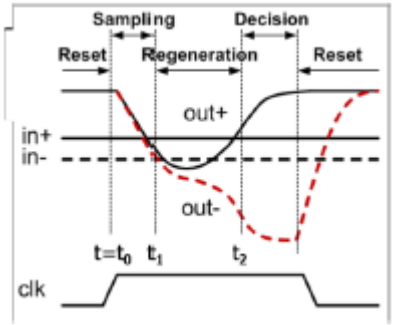
- Regeneration phase starts when PMOS transistors turn on, t_1, until decision time, t_2.
- Assume M1 is in linear region and circuit no longer sensitive to v_{in}.
- Cross-coupled inverters amplify signals via positive-feedback:





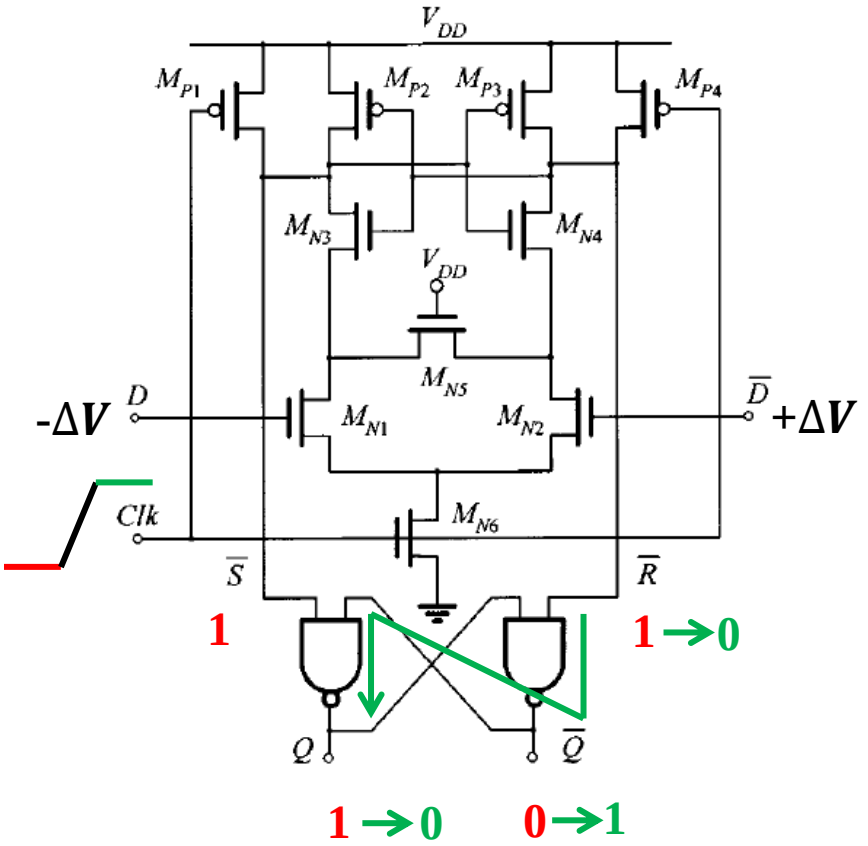
$$G_R = \exp\left(\frac{t_2 - t_1}{\tau_R}\right)$$

$$\tau_R = C_{out} / \left(g_{m2,r} + g_{m3,r}\right)$$



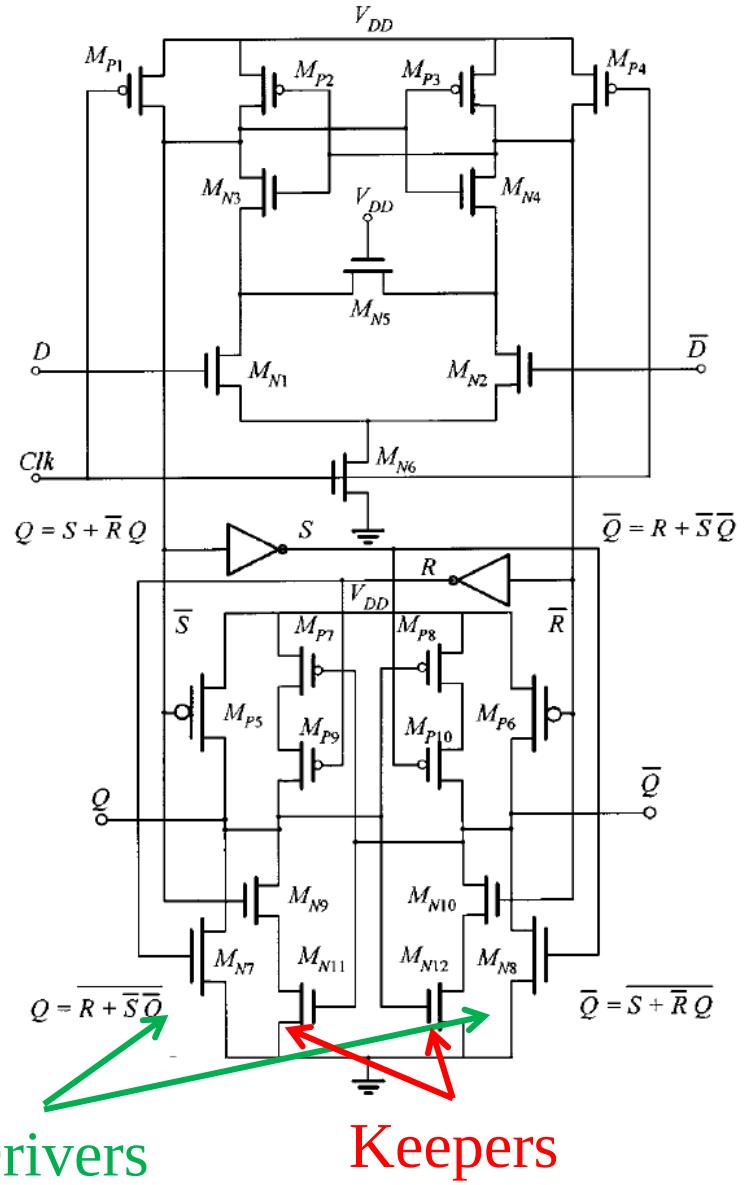
Conventional RS Latch

- **RS latch holds output data during latch pre-charge phase.**
- **Conventional RS latch rising output transitions first, followed by falling transition.**



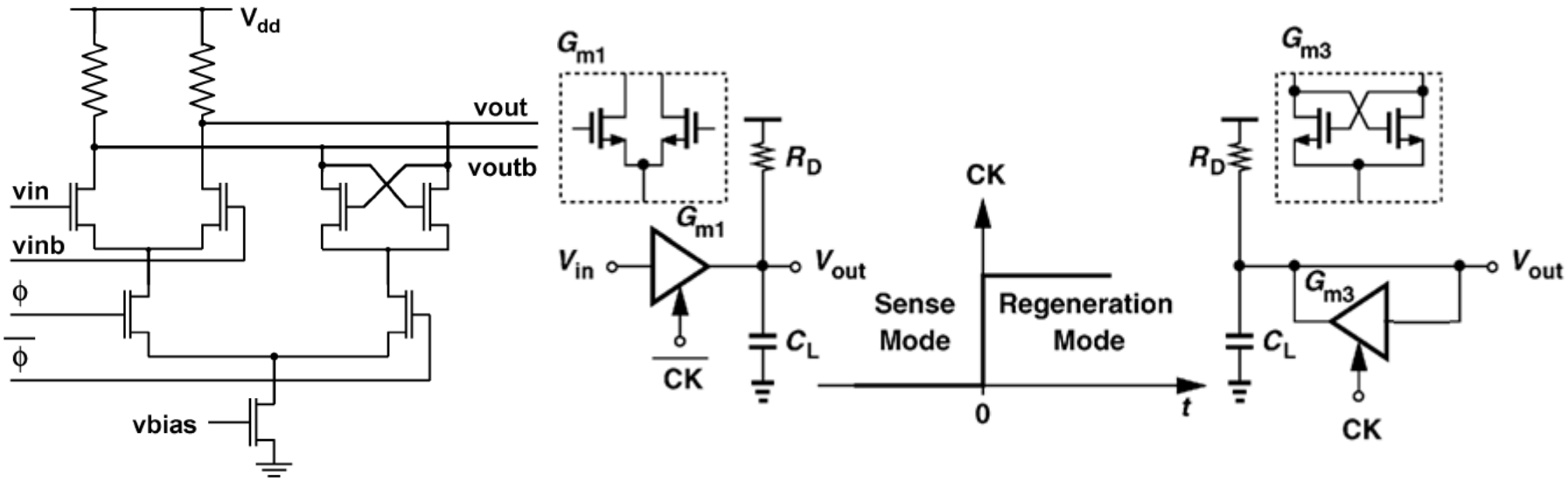
Optimized RS Latch

- **Optimizing RS latch for symmetric pull-up and pull-down paths allows for considerable speed-up.**
- **During evaluation, large driver transistors are activated to change output data and the keeper path is disabled.**
- **During pre-charge, large driver transistors are tri-stated and small keeper cross-coupled inverter activated to hold data.**



[Nikolic, JSSC Jun. 2000]

CML Latch Operation



- **At the beginning of regeneration phase**

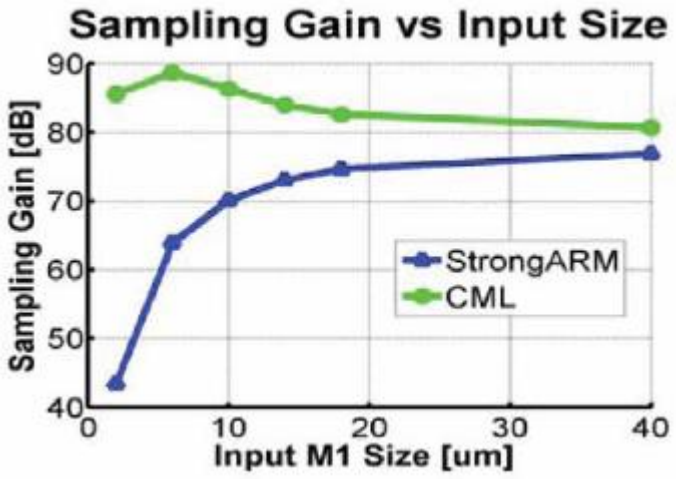
$$V_{out}(0) = G_{m1} R_D V_{in}$$

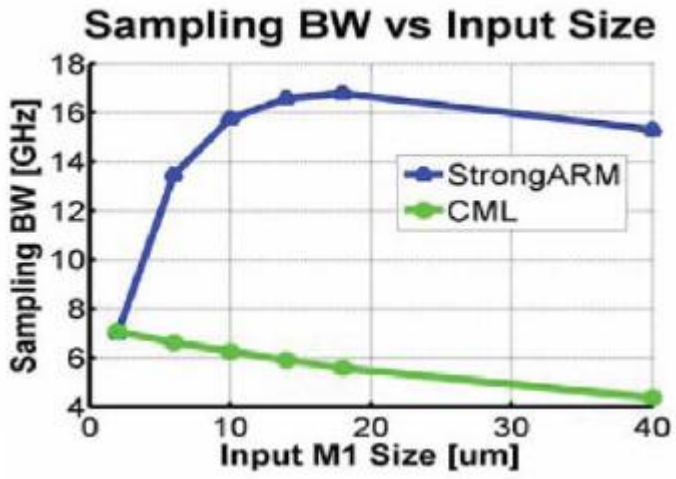
- **Then**

$$G_{m3}\ V_{out} = \frac{V_{out}}{R_D} + C_L \frac{dV_{out}}{dt}$$

$$V_{out}(t) = G_{m1} R_D V_{in} \exp \frac{G_{m3} t}{C_L} \exp \frac{-t}{R_D C_L}$$

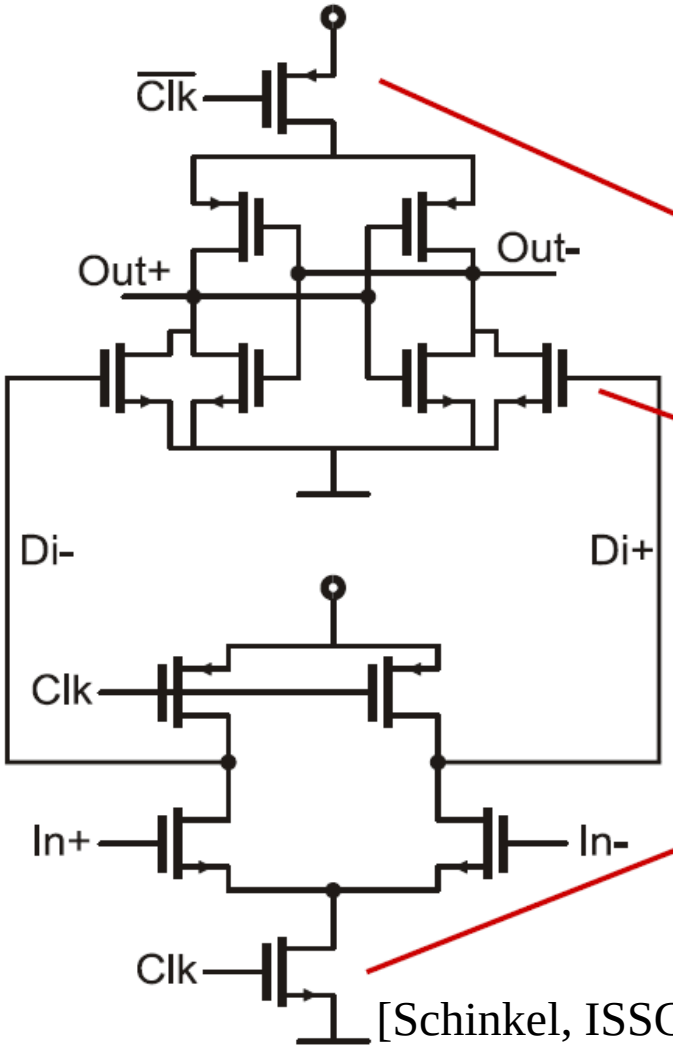
Comparison of SA and CML Comparator (1)





- **CML latch has higher sampling gain with small input pair.**
- **StrongARM latch has higher sampling bandwidth.**
  - For CML latch increasing input pair also directly increases output capacitance.
  - For SA latch increasing input pair results in transconductance increasing faster than capacitance.

Low-Voltage SA (1)



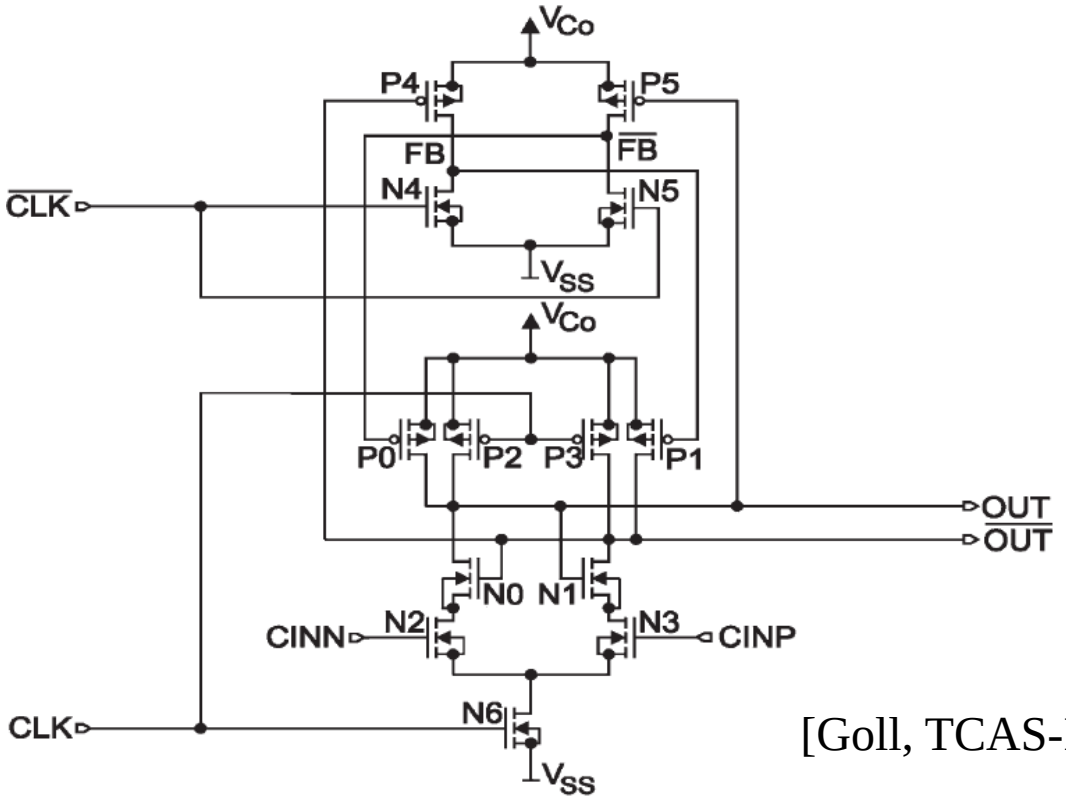
[Schinkel, ISSCC 2007]

Advantages:

- Less stacking
- Wide tail for fast latching
- More isolation between in- and output
- Small tail → input stage in weak inversion → less offset from latch $(V_{OS}\ \alpha\ V_{OV})$

- But requires Clk and Clk_b.

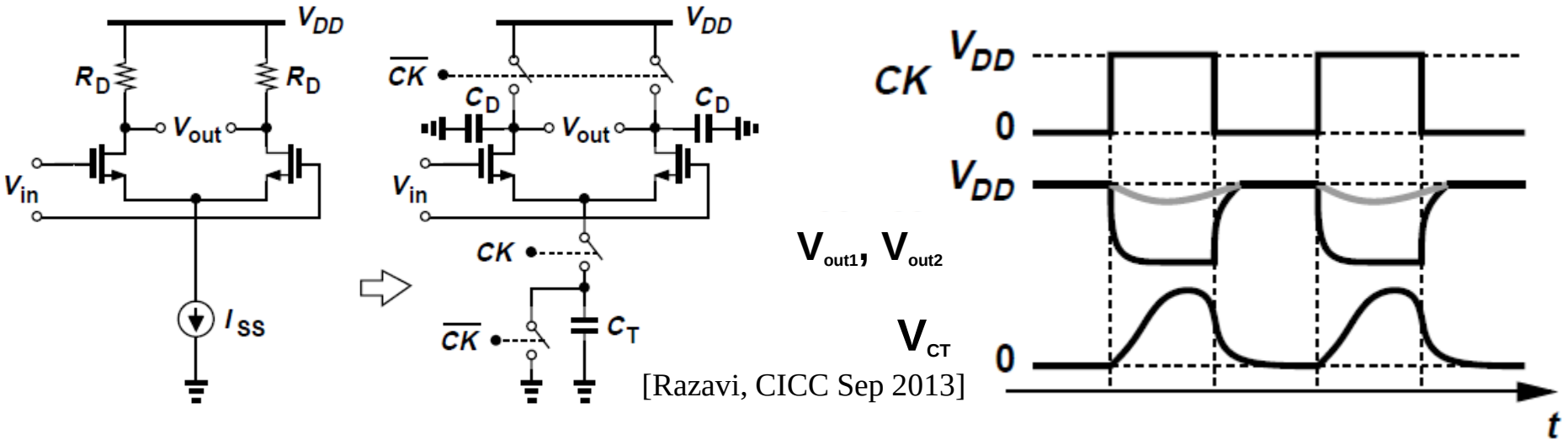
Low-Voltage SA (2)



[Goll, TCAS-II Nov. 2009]

- **Similar stacking to conventional SA latch**
- **However, now P0 and P1 are initially on during evaluation which speeds up operation at lower voltages.**
- **Requires clk & clk_b.**

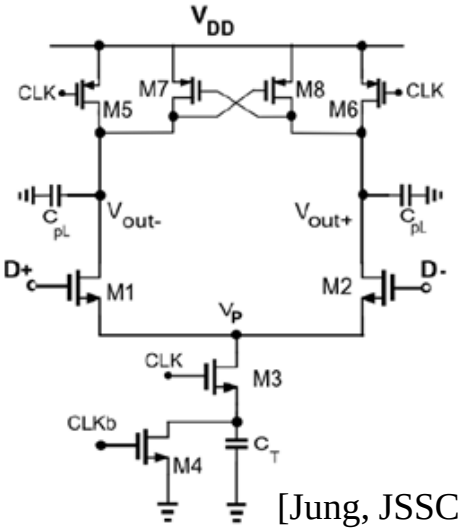
Charge-Steering Concept



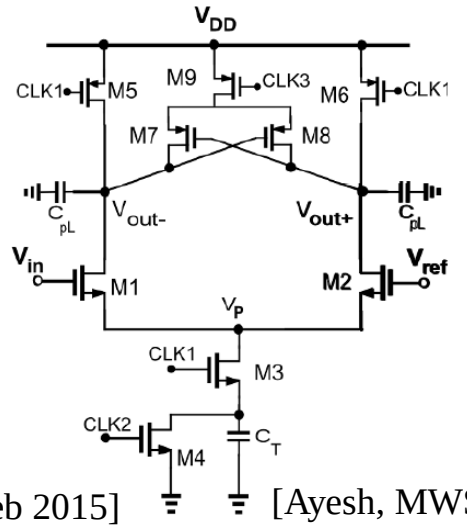
[Razavi, CICC Sep 2013]

- **Tail current sources converted into a charge source.**
- **Two phases: Reset Phase (CK Low) and Amplification Phase (CK High)**
- **In Reset phase, C_T is discharged and V_{out} Reset**
- **In amplification phase, charge redistribution occurs between C_D and C_T. V_{out} difference exists based on V_{in}.**

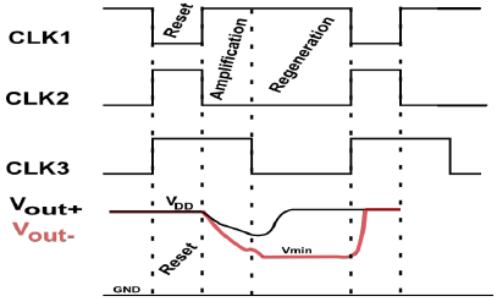
Charge-Steering Comparator



[Jung, JSSC Feb 2015]



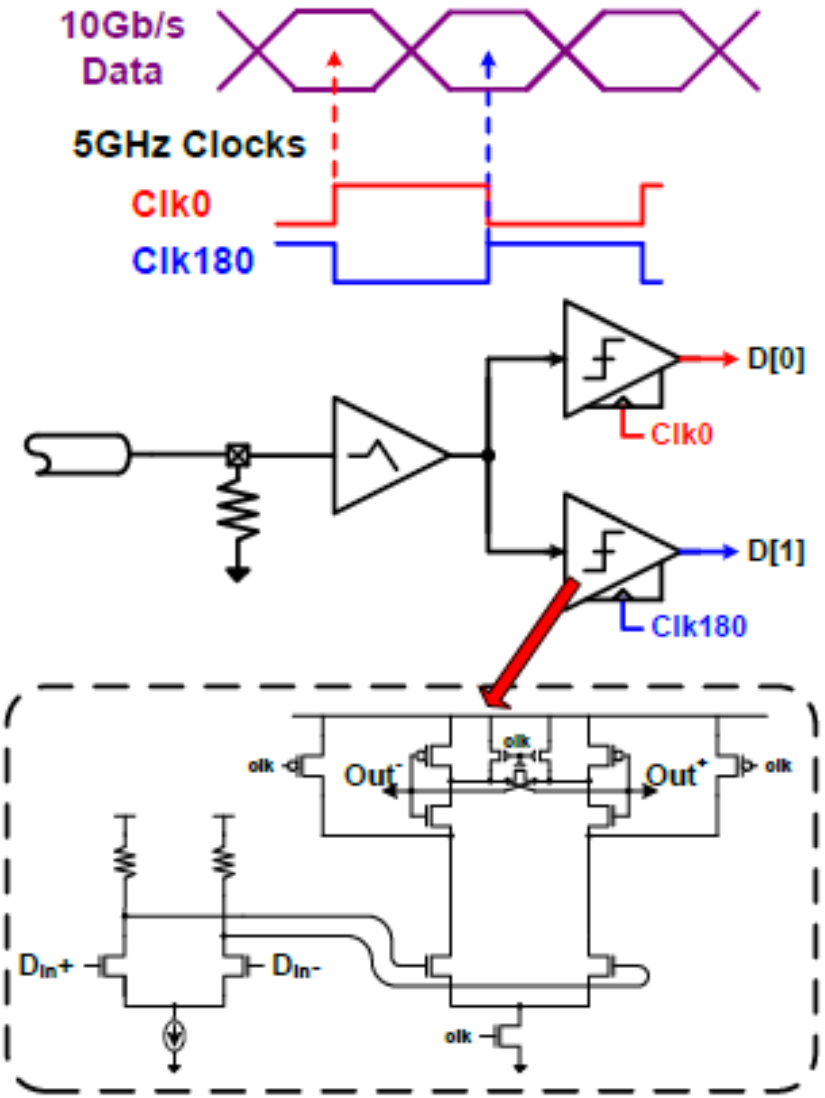
[Ayesh, MWSCAS Aug 2015]



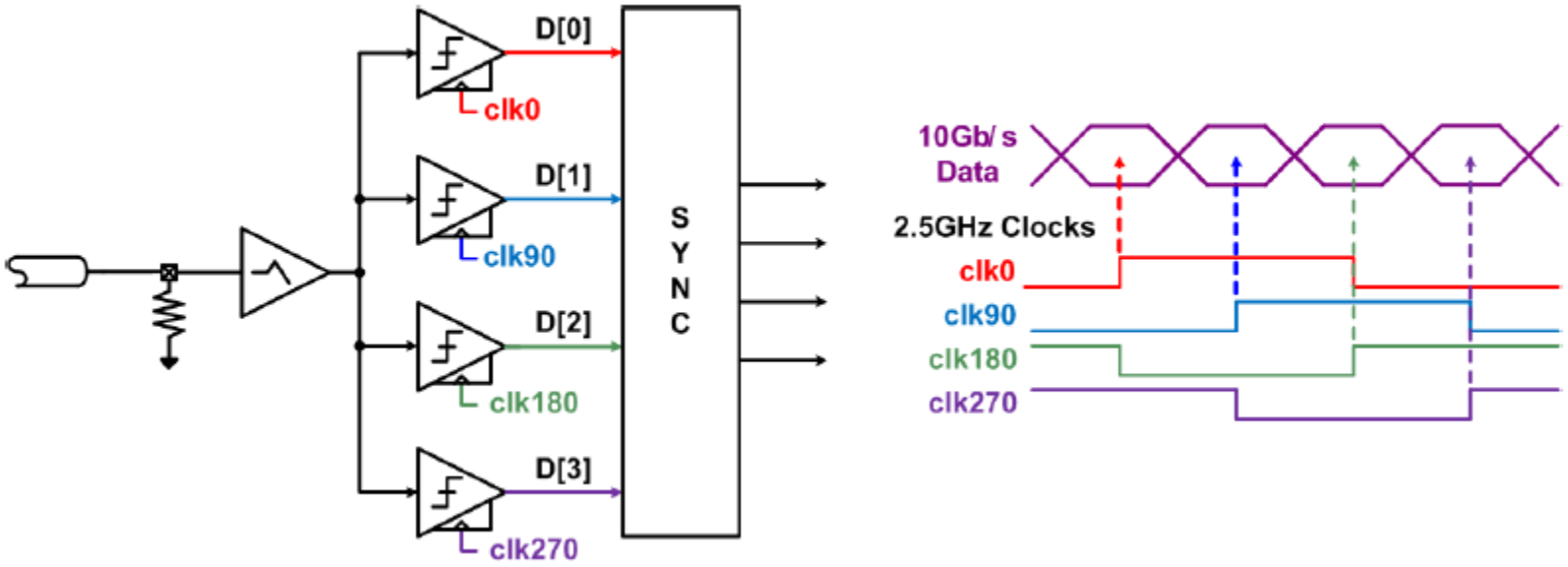
- **Cross-coupled pairs added for regeneration.**
- **Two-phase design has contention between cross-coupled pair and differential pair.**
- **Three-phase design resolves this issue and results in better sensitivity.**
- **Overall, low power operation is achieved. (66 µW at 6 GHz with 1-mV sensitivity)**

RX Demultiplexing

- Demultiplexing allows for lower clock frequency relative to data rate.
- Gives extra regeneration and pre-charge time in comparators.
- Need precise phase spacing, but not as sensitive to duty-cycle as TX multiplexing.



1:4 Demultiplexing



- **Increased demultiplexing allows for higher data rate at the cost of increased input or pre-amp load capacitance.**
- **Higher multiplexing factor more sensitive to phase offsets in degrees**

Outline

- **RX Overview**
  - Parameters
  - Architecture choices
- **RX Amplifiers**
  - Pre-amplifiers
  - Bandwidth extension techniques
- **Clocked Comparators**
  - Circuits
  - Characterization techniques
- **Demultiplexing**
- **RX Sensitivity**
  - Offset
  - Noise

Receiver Sensitivity

- **RX sensitivity is a function of the input referred noise, offset, and minimum latch resolution voltage.**

$$v_S^{pp} = 2v_n^{rms}\sqrt{SNR} + v_{\min} + v_{offset}$$

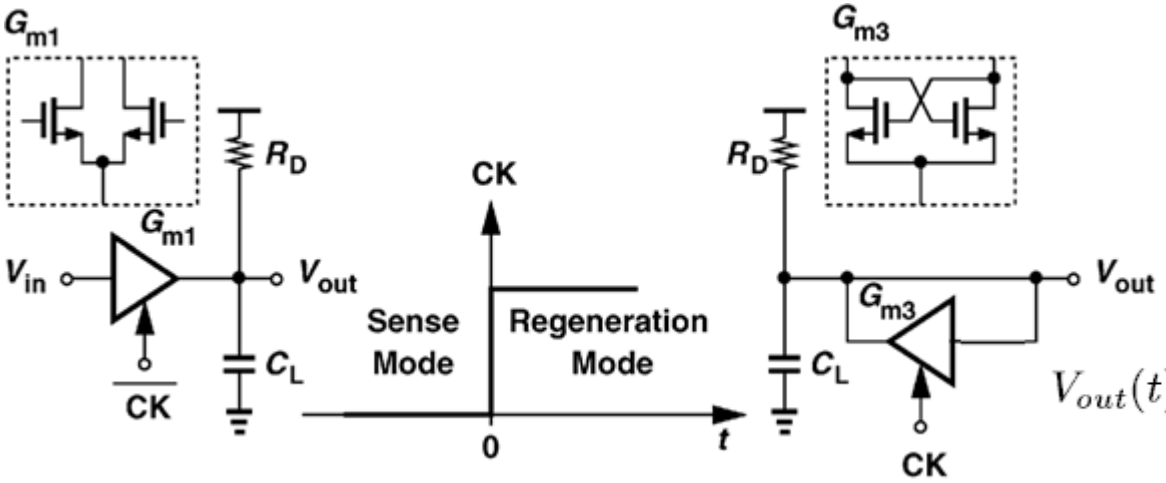
- **Gaussian (unbounded) input referred noise comes from input amplifiers, comparators, and termination.**
  - A minimum signal-to-noise ratio (SNR) is required for a given bit-error-rate (BER). $\text{For BER} = 10^{-12}\ (\sqrt{\text{SNR}} = 7)$
- **Minimum latch resolution voltage comes from hysteresis, finite regeneration gain, and bounded noise sources.**

$$\text{Typical } v_{\min} < 5mV$$

- **Input offset is due to circuit mismatch (primarily V_{th} mismatch) & is most significant component if uncorrected.**

Latch Resolution

- **Taking CML latch as an example**



$$V_{out}(t) = G_{m1}R_D V_{in} \exp\frac{G_{m3}t}{C_L} \exp\frac{-t}{R_D C_L}$$

- **Define the resolution as the input voltage that yields an output equal to 80% of the final value.**

$$V_{sens} = \frac{0.8I_{SS}}{G_{m1}} \exp\left(-\frac{G_{m3}R_D - 1}{2R_D C_L f_{CK}}\right)$$

- **Including Hysteresis, worst case resolution becomes**

$$V_{sens} = \frac{0.8I_{SS}}{(1-\kappa)G_{m1}} \left(1 + \kappa \exp\frac{G_{m3}R_D - 1}{2R_D C_L f_{CK}}\right) \exp\left(-\frac{G_{m3}R_D - 1}{2R_D C_L f_{CK}}\right)$$

Where $\kappa = \exp\left(-\frac{1}{2R_D C_L f_{CK}}\right)$

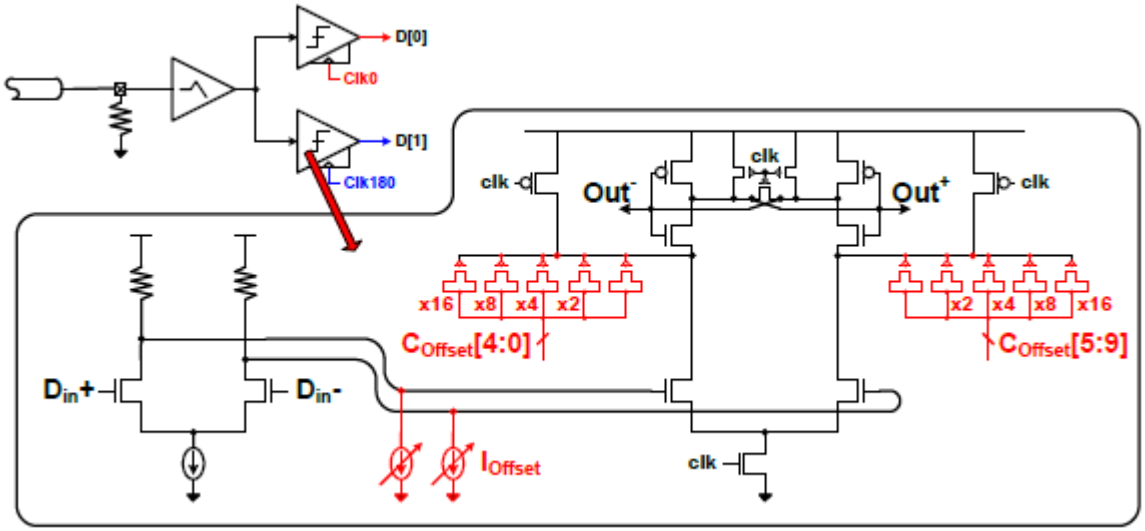
RX Sensitivity & Offset Correction

- **RX sensitivity is a function of the input referred noise, offset, and min latch resolution voltage.**

$$v_S^{pp} = 2v_n^{rms}\sqrt{SNR} + v_{\min} + v_{offset*} \qquad \text{Typical Values}: v_n^{rms} = 1mV_{rms},\ v_{\min} + v_{offset*} < 6mV$$

$$\text{For BER} = 10^{-12}\ (\sqrt{\text{SNR}} = 7) \Rightarrow v_S^{pp} = 20mV_{pp}$$

- **Circuitry is required to reduce input offset from a potentially large uncorrected value (>50mV) to near 1mV.**



Input Referred Offset

- **The input referred offset is primarily a function of V_{th} mismatch and a weaker function of β (mobility) mismatch.**

$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}}, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}}$$

- **To reduce input offset 2x, we need to increase area 4x.**
  - Not practical due to excessive area and power consumption.
  - Offset correction necessary to efficiently achieve good sensitivity.
- **Ideally the offset coefficients are given by the design kit and Monte Carlo is performed to extract offset sigma.**
- **Here are some common values:**
  - A_{Vt} = 1mVμm per nm of t_{ox}.
    - For 90nm technology, t_{ox}=2.8nm → A_{Vt} ~2.8 mVμm.
  - A_β is generally near 2%μm.

Offset Correction Range & Resolution

- Generally circuits are designed to handle a minimum variation range of ±3σ for 99.7% yield.
- Example: Input differential transistors W=4µm, L=150nm

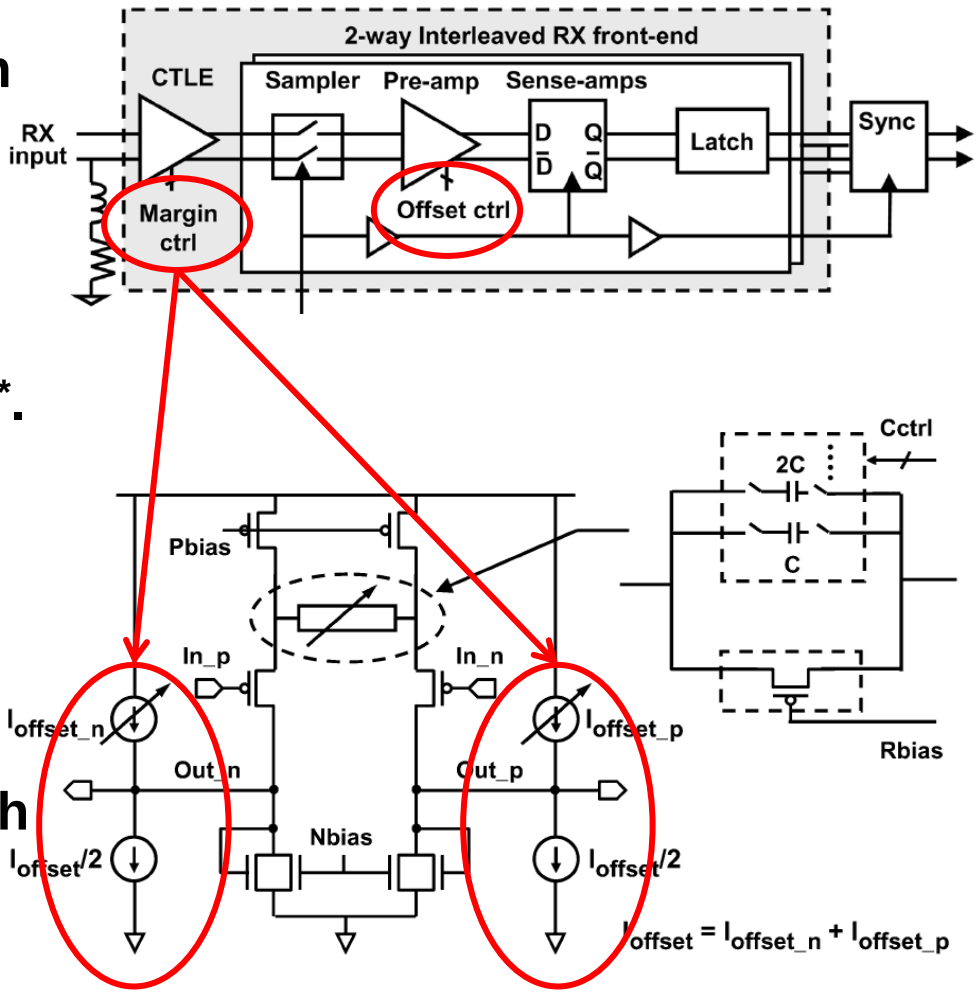
$$\sigma_{V_t} = \frac{A_{V_t}}{\sqrt{WL}} = \frac{2.8mV\mu m}{\sqrt{4\mu m \cdot 150nm}} = 3.6mV, \quad \sigma_{\Delta\beta/\beta} = \frac{A_\beta}{\sqrt{WL}} = \frac{2\%\mu m}{\sqrt{4\mu m \cdot 150nm}} = 2.6\%$$

- If we assume (optimistically) that the input offset is only dominated by the input pair V_t mismatch, we would need to design offset correction circuitry with a range of about ±11mV.
- If we want to cancel within 1mV, we would need an offset cancellation resolution of 5bits, resulting in a worst-case offset of

$$1LSB = \frac{\textbf{Offset Correction Range}}{2^{\textbf{Resolution}} - 1} = \frac{22mV}{2^5 - 1} = 0.65mV$$

Current-Mode Offset Correction Example

- Differential current injected into input amplifier load to induce an input-referred offset that can cancel the inherent amplifier offset.
- Can be made with extended range to perform link margining*.
- Passing a constant amount of total offset current for all the offset settings allows for constant output common-mode level.
- Offset correction performed both at input amplifier and in individual receiver segments of the 2-way interleaved architecture.

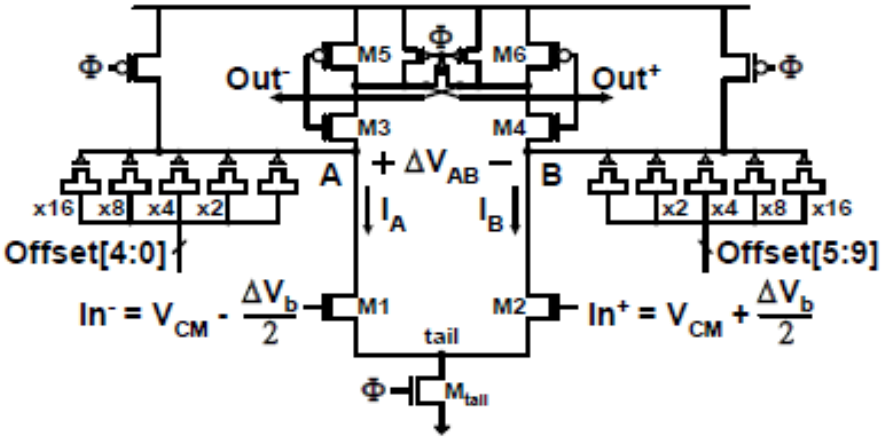


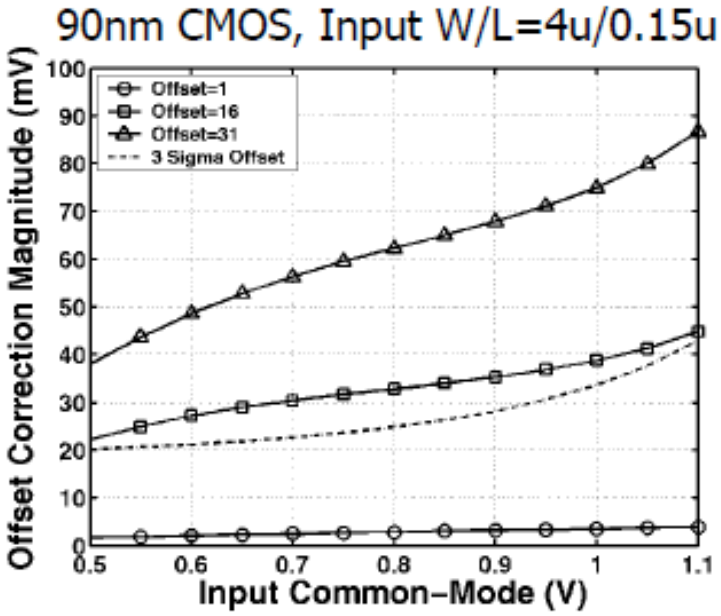
[Balamurugan, JSSC Apr. 2008]

* Introducing offset and get BER to establish an eye.

Capacitive Offset Correction Example

- A capacitive imbalance in the sense-amplifier internal nodes induces an input-referred offset.
- Pre-charges internal nodes to allow more integration time for more increased offset range.
- Additional capacitance does increase sense-amp aperture time.
- Offset is trimmed by shorting inputs to a common-mode voltage and adjusting settings until an even distribution of "1"s and "0"s are observed.
- Offset correction settings can be sensitive to input common-mode.





[Palermo, thesis 2008]