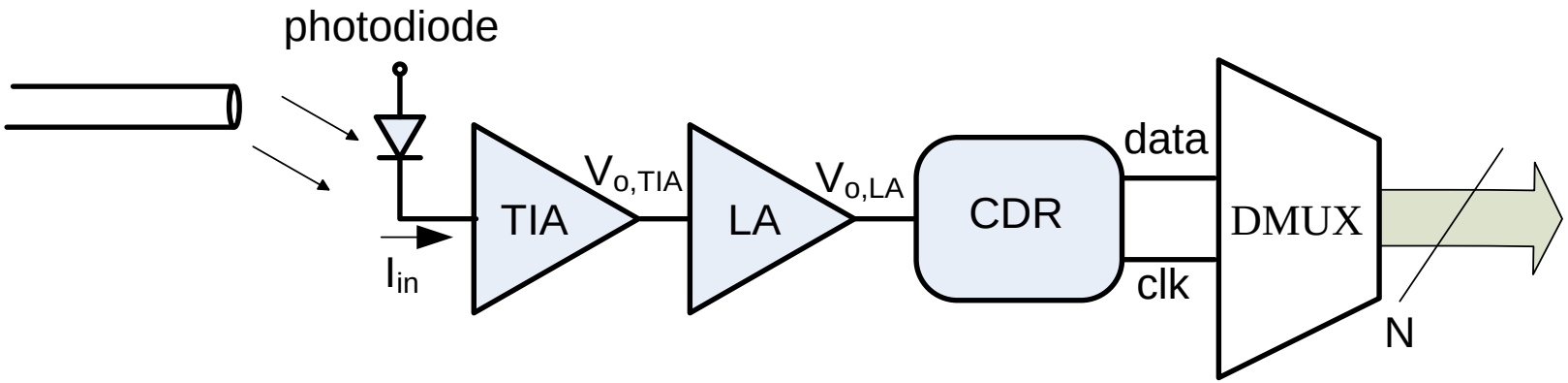
High-Speed Optical Receivers

Lecture 7

Optical Receivers Block Diagram

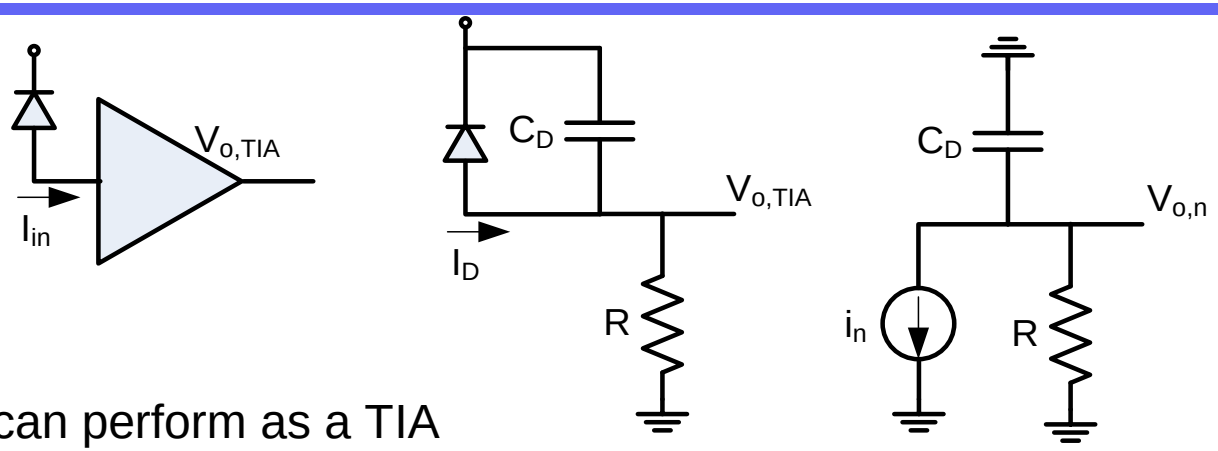


- A photo diode converts the optical signal into an electrical current proportional to the optical signal
- $I_{in\text{-}P}=RxP_{in}$, where R is the photodiode responsivity (A/W)→ represents photodiode efficiency
- The current is amplified and converted into a voltage by a **T**rans-**I**mpedance **A**mplifier (TIA)
- The TIA output is amplified further by a **L**imiting **A**mplifier (LA)
- The CDR extracts the clock and re-times the data which is fed to a DEMUX to produce the slower parallel data

Optical Receiver (Cont'd)

- Problem: If the input current is $5.3uA_{pp}$, the TIA gain is $1.5k\Omega$, and the LA gain is 30dB calculate the output voltage of the TIA and LA
  - $V_{o,TIA}=I_{in}*1.5k=8mV_{pp}$
  - $V_{o,LA}=V_{o,TIA}*G_{LA}=8m*10^{(30/20)}=0.25V_{pp}$
- Problem: Given an input referred rms noise of 380nA, a responsivity of 0.8A/W for the photo diode, and a required BER of 10^{-12} calculate the optical sensitivity in dBm.
  - Minimum value of input current $I_{in\text{-}P,min}$= 380nA*7 = $2.66uA_p$
  - Sensitivity = Minimum input optical power = $10\log(I_{in\text{-}P,min}/0.8*10^3)$ = -24.8dBm

Passive TIA



- A resistor can perform as a TIA
- TIA trans-impedance gain $R_T=V_{o,TIA}/I_{in}=R$
- TIA bandwidth $BW=1/RC_D$ (rad/s), where C_D is the photo diode/package capacitance
- TIA input referred noise current $i_n^2= 4KT/R$ (A^2/Hz)= R thermal noise
- Total integrated output noise voltage:

$$v_n^{\,2} = \int_0^{\infty} \frac{4KT}{R} \left| \frac{R}{1+sC_DR} \right|^2 df = KT/C_D\,(V^2)$$

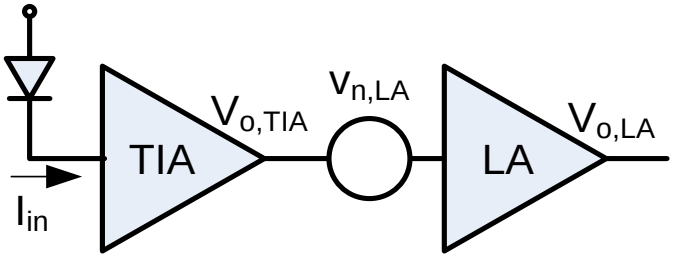
- Total integrated input referred noise current $i_n^2=KT/R^2C_D$ (A^2)
- Gain, noise, and BW trade-off

Passive TIA Gain, Noise, BW Trade-off

- Problem: Calculate the trans-resistance gain and the total input referred noise current for a resistor-based TIA for 10Gbps given that C_D=0.2pF
  - For 10Gbps the required BW~7GHz
  - Trans-resistance gain= R = 1/(BWxC_D)= 114Ω
  - Total input referred noise current, $i_n = \sqrt{(KT/R^2C_D)}$= 1.26 uA_{rms}

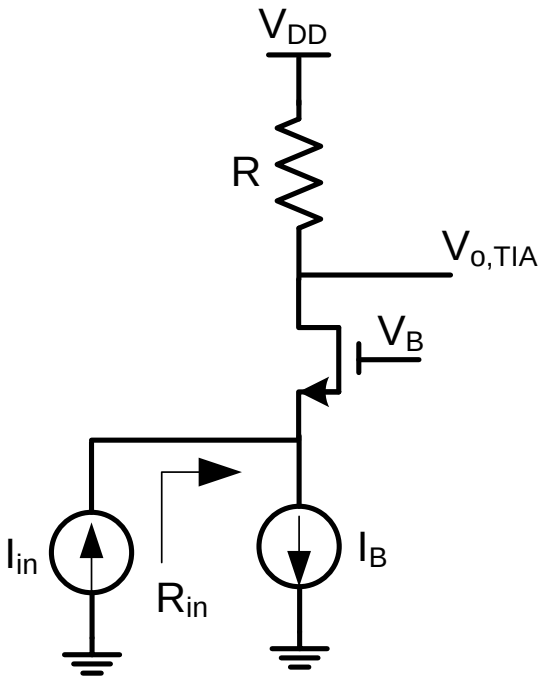
• Problem: Calculate the required TIA gain to reduce the contribution of the LA noise to 1pA/√Hz given that the LA input referred noise voltage is 5nV/√ Hz

  – R_T=(5nV/√Hz)/(1pA/√Hz)=5KΩ



Open Loop TIAs

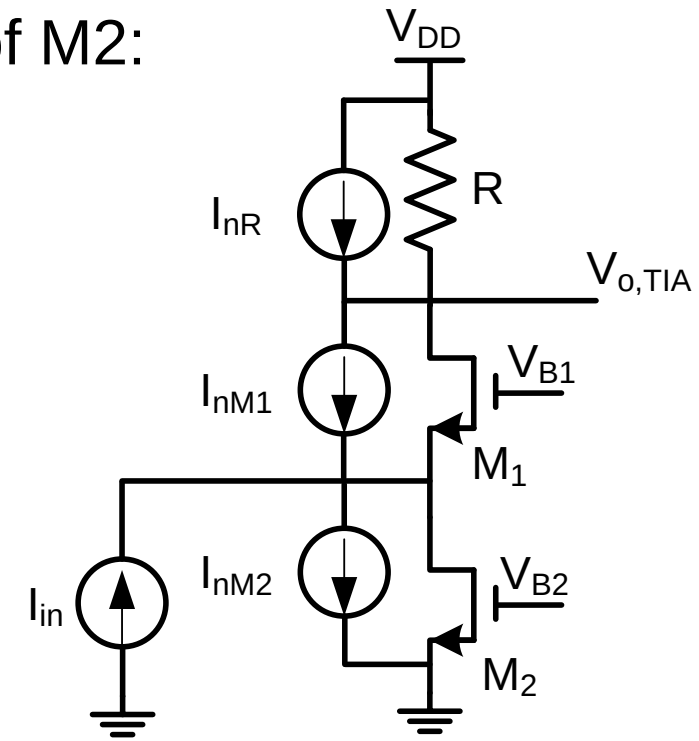
- Desired Properties: high gain, low noise, low input impedance (for high speed)
- Common gate/base amplifiers can act as a TIA
- trans-impedance gain $R_T=R$
- $R_{in}=(r_o+R)/(1+g_m r_o)\approx 1/g_m$, biasing the transistor with a large I_B can reduce R_{in}
- Reducing R_{in} moves the pole associated with the input node capacitance (C_D) to higher frequencies
- TIA trans-conductance gain and BW are decoupled



B. Razavi, Design of Integrated Circuits for Optical Communications, New York:McGraw-Hill, 2002.

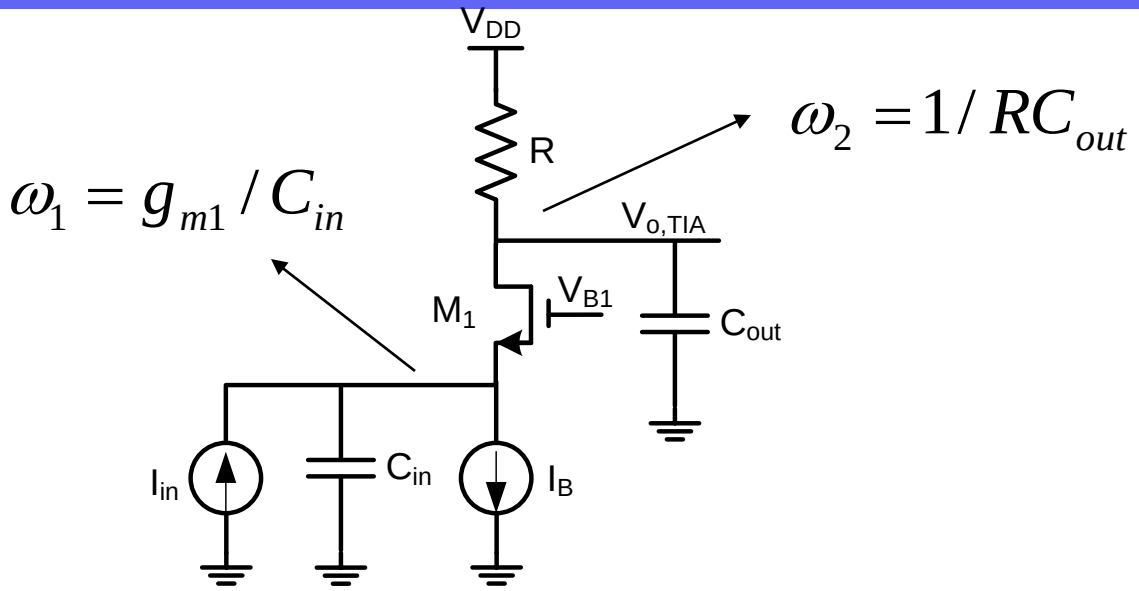
Common-gate TIA Noise

- Due to the high output impedance of M2:
  - All of I_{nM2} flows through R
  - All of I_{nR} flows through R
  - No portion of I_{nM1} flows through R
- $V_{n,out}^2 = I_{nM2}^2R^2 + I_{nR}^2R^2$
- $V_{n,out}^2 = 4KT(\gamma g_{m2}+1/R)R^2$



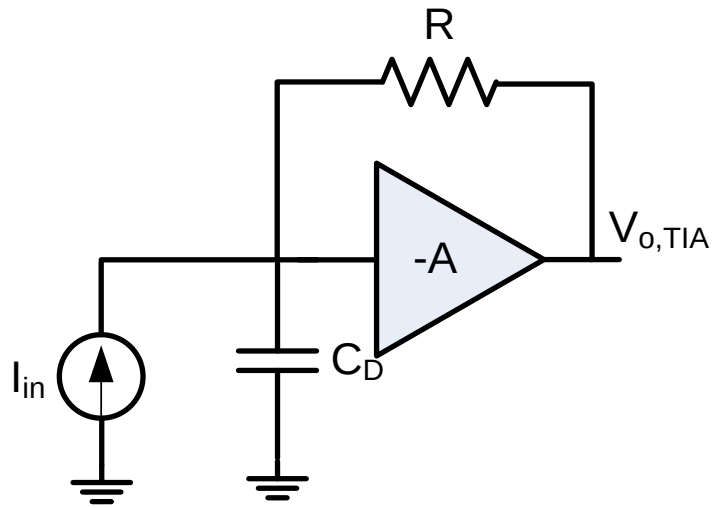
- The input referred noise current $I_{n,in}^2 = 4KT(\gamma g_{m2}+1/R)$
- Note that the resistor and M_2 noise are directly referred to the TIA input with a unity scaling factor
- Noise and headroom trade off

Common-gate TIA Frequency response



- The common-gate TIA has 2 poles associated with the input and output nodes (no Miller)
- C_{in} includes the large photodiode capacitance making the input node typically lower in frequency than the output node
- C_{out} includes the input capacitance of the LA

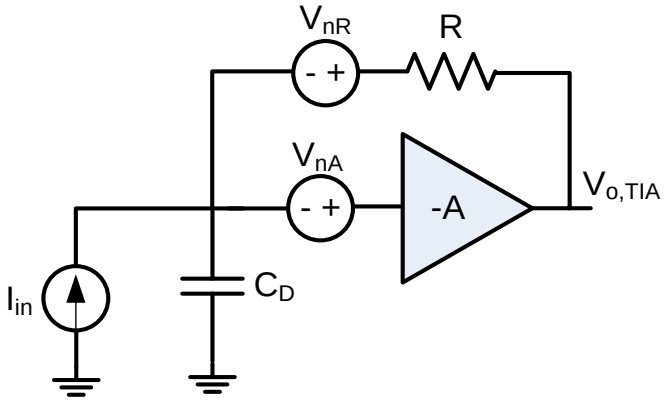
Feedback TIAs

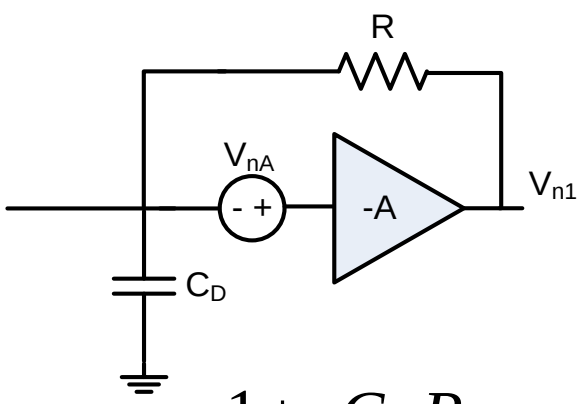


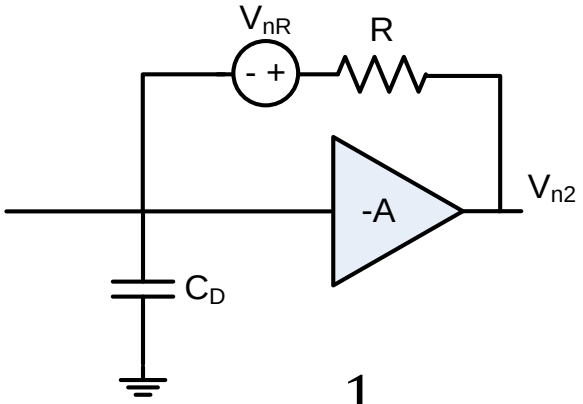
$$\frac{V_{o,TIA}}{I_{in}} = -\frac{A}{1+A}\frac{R}{1+\frac{RC_D}{1+A}s}$$

- Employ shunt-shunt feedback, sense the output voltage and feedback a proportional current to the input
- For A>>1, the low frequency trans-impedance gain is R
- The TIA 3dB frequency is at $(1+A)/RC_D$, a factor (1+A) higher than the passive TIA
- Input TIA resistance = R/(1+A)
- Provides a mean to obtain a large gain with a small input resistance

Feedback TIA Noise







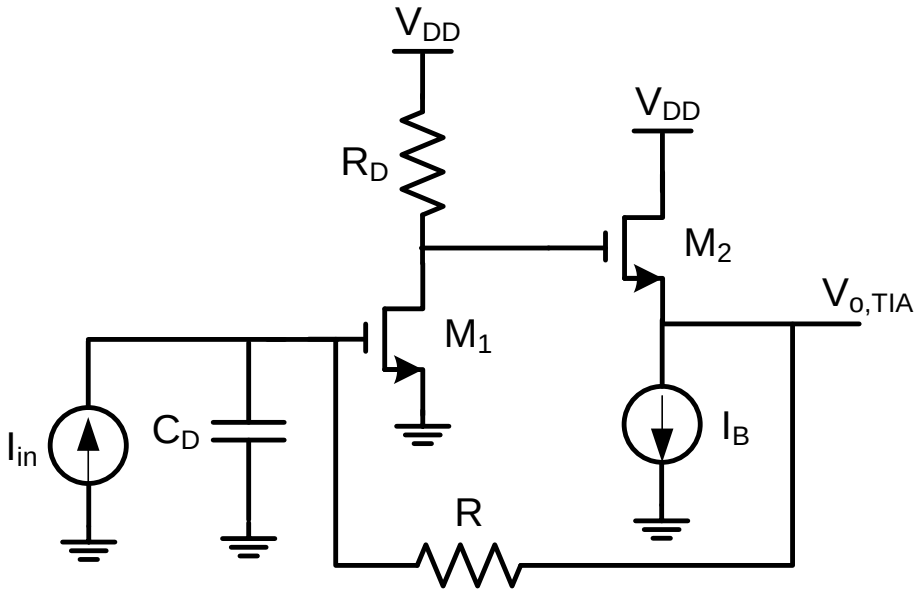
$$V_{n,out}^2 = V_{n1}^2 + V_{n2}^2$$

$$V_{n1} \approx -\frac{1+sC_DR}{1+\frac{sC_DR}{A}}V_{nA}$$

$$V_{n2} \approx \frac{1}{1+\frac{sC_DR}{A}}V_{nR}$$

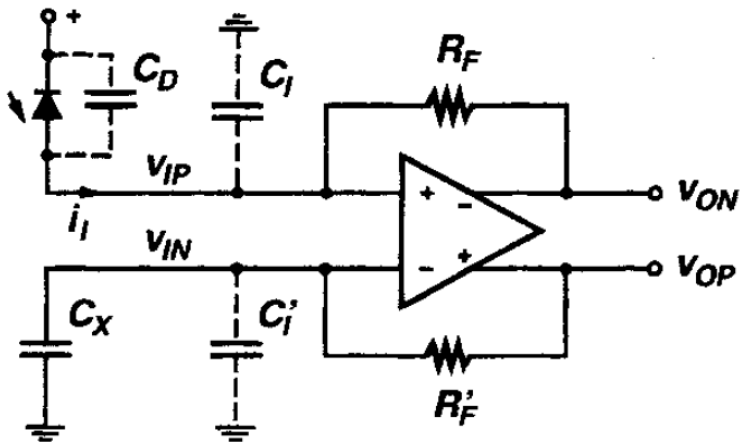
- For low frequencies s→0 $V_{n1}=V_{nA}$, & $V_{n2}=V_{nR}$
- $V_{n,out}^2 = V_{nR}^2+V_{nA}^2 \rightarrow I_{n,in}^2=(V_{nR}^2+V_{nA}^2)/R^2$
- $I_{n,in}^2=4KT/R+V_{nA}^2/R^2$
- To minimize noise use large R, no headroom issues as in common-gate TIA
- Also second term can be smaller than the current source noise in the common-gate TIA

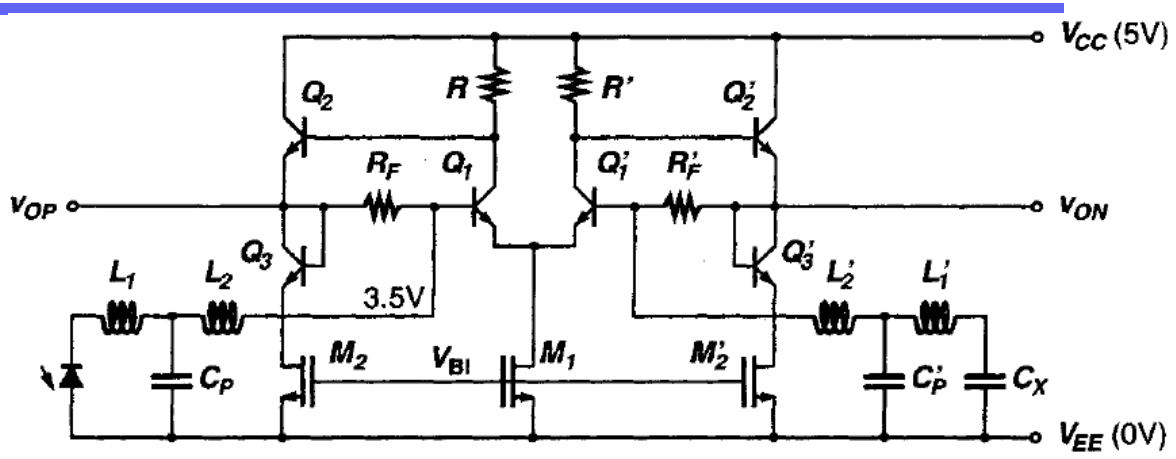
Feedback TIA Implementation



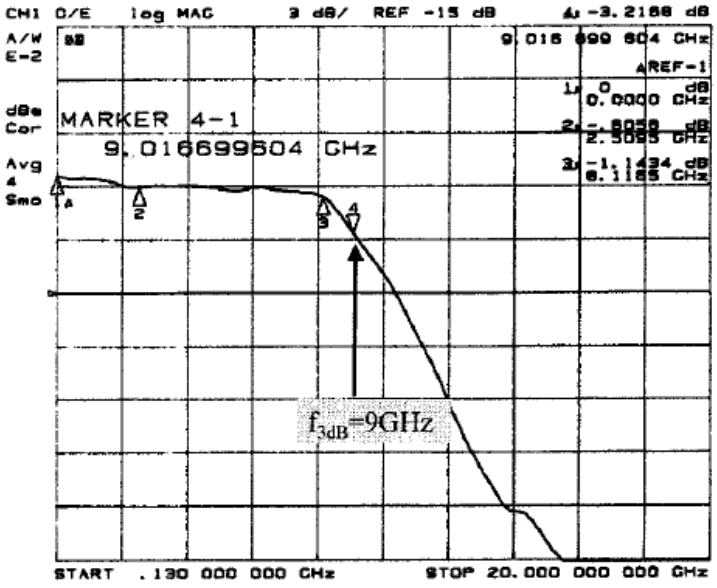
- The feed forward amplifier is replaced with a common source amplifier (for large gain) and a source follower
- The source follower isolates the gain of the common source from the loading effect of the feedback resistance R
- $A \approx g_{m1}R_D$
- The trans-impedance gain $R_T = R\, g_{m1}R_D/(1+ g_{m1}R_D)$
- $R_{in}= R/(1+ g_{m1}R_D)$
- $R_{out}= (R \,//1/g_{m2})/(1+ g_{m1}R_D)$

JSSC 2001: Si BiCMOS Trans-impedance Amplifier for 10-Gb/s SONET Receiver

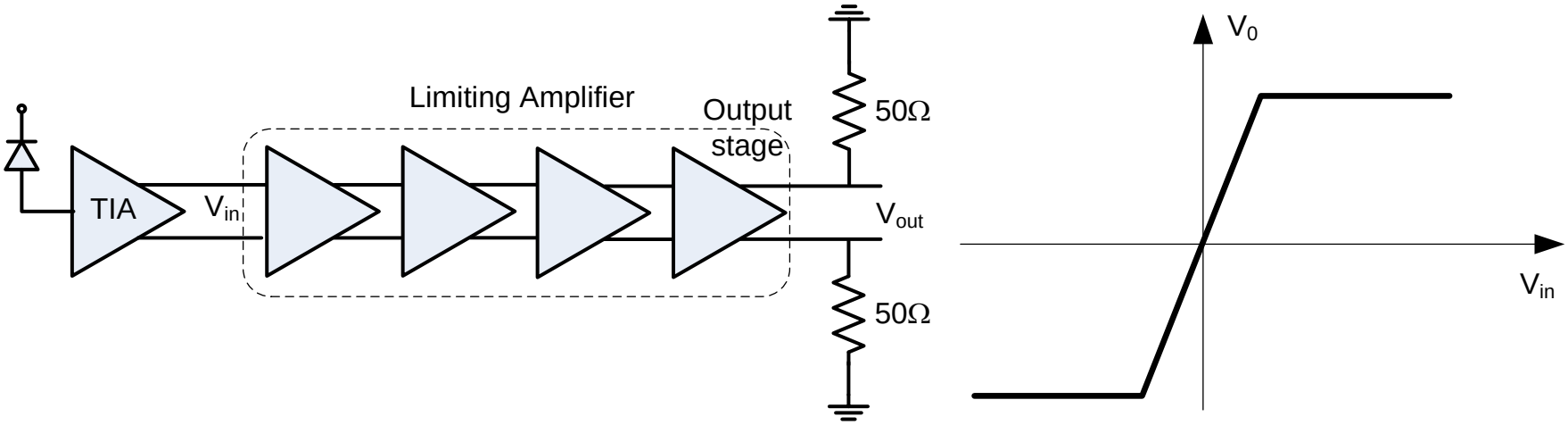




Bandwidth (f_{3dB})	**9GHz**
Differential trans-impedance	**55dBΩ (vs. 57dB Ω simulated)**
Optical Sensitivity (@BER=10^{-12})	**-17dBm**
Max. input photo current	**< 1.4mA_{p-p}**
Group delay	**+/-9ps**
Max. differential output swing	**1V_{p-p} (simulated)**
Power Dissipation	**140mW @ 5V(incl. 80mW output buffer)**
Device Technology	**0.25um (We=0.4um) Modular BiCMOS**



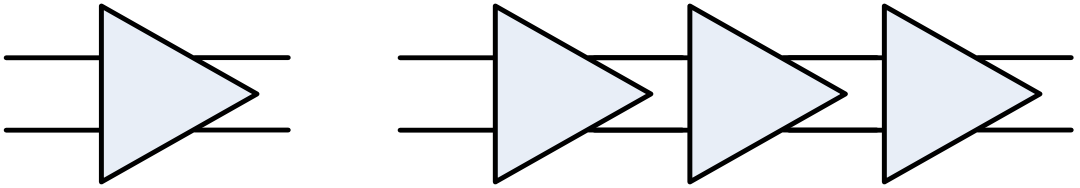
Limiting Amplifiers



- LA provide large gains and signal swings for the reliable CDR operation
- LA introduces non-linearity (limiter) and hence is not usually used in combination with linear equalization techniques in the receiver
- If high linearity is required for equalization or as a result of the modulation scheme linear amplifiers must be used instead of LAs
- The last stage in the LA needs to drive its load, which might be a 50Ω if the LA is not integrated with the CDR on the same chip
- Also might require a 50 Ω input impedance if not with TIA on same chip
- Offset voltage is one of the main challenges in LA design, as any small offset gets multiplied by the large gain and can saturate the entire receiver

E. Sckinger, Broadband Circuits for Optical Fiber Communication, New York:Wiley, 2005.

Limiting Amplifiers (Cont'd)



- For a 2.5Gbps we might need a 30dB LA (31.6x) with a BW of ~3GHz
- Can we design an amplifier with these specs?
- Single stage approach: GBW_{tot} = 31.6x3 = 95GHz close to modern process f_T (transistor unity gain frequency)!!!
- For a 3-stage solution, the gain per stage 10dB =3.1x
- Assume amplifiers have a brick wall response GBW_s= 3.1 x 3GHz = 9.3GHz
- Using a multi-stage amplifier allows us to use a smaller GBW per stage (GBW_s), or in other words resulted in a BW extension given by

$$\frac{GBW_{tot}}{GBW_s} \approx A_{tot}^{\,1-1/n}$$

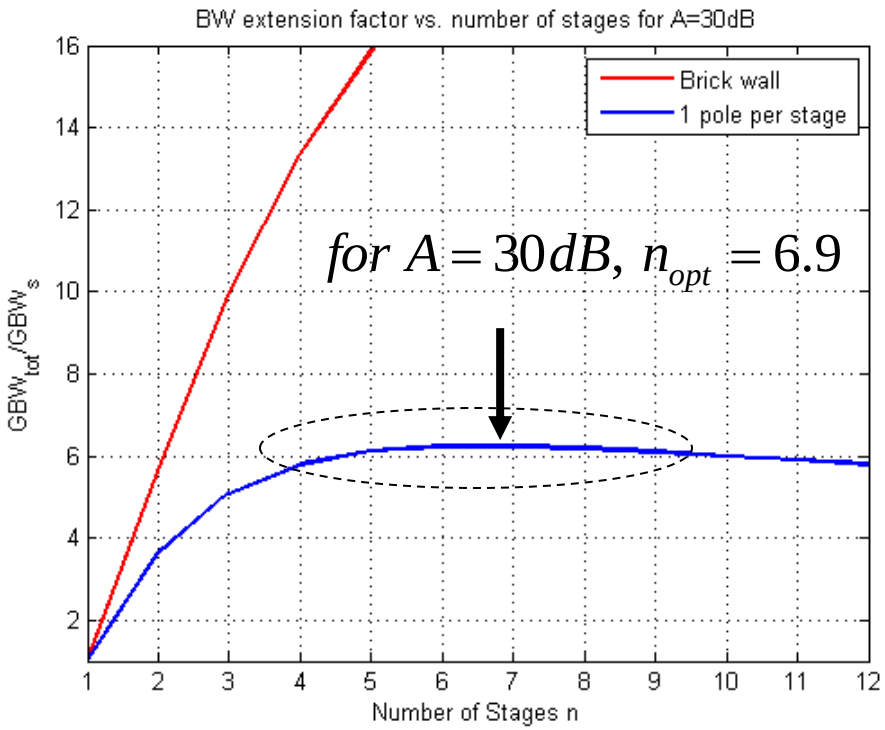
Limiting Amplifiers (Cont'd)

- For amplifiers with a single pole per stage the bandwidth extension factor becomes:

$$\frac{GBW_{tot}}{GBW_s} \approx A_{tot}^{\,1-1/n}\sqrt{2^{1/n}-1}$$

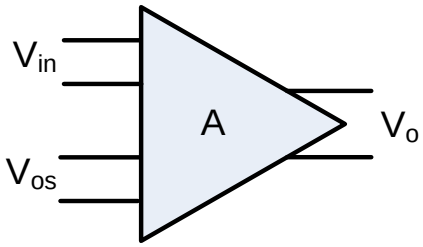
- The optimal number of stages n_{opt} is:

$$n_{opt} = 2\ln(A_{tot})$$



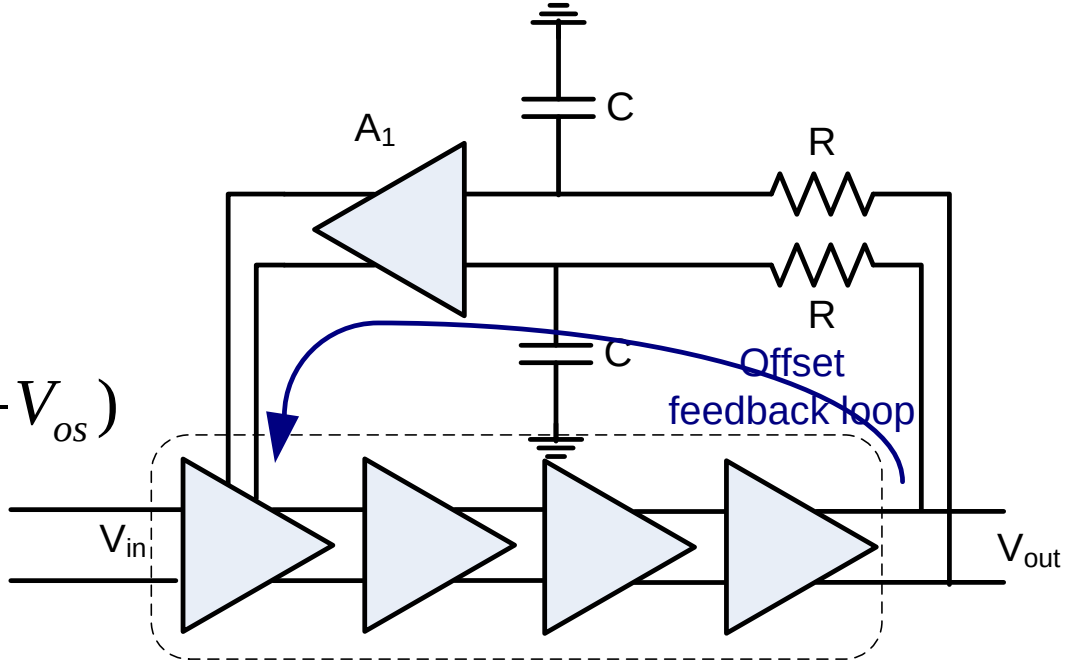
- For 30dB gain, N ≥ 4 results in the same BW extension factor
- Using more than necessary stages might result in extra power consumption and noise

Limiting Amplifiers: Offset



$$V_o = AV_{in} \xrightarrow{\text{offset}} V_o = A(V_{in} - V_{os})$$

$$V_{os} = \left.\frac{V_o}{A}\right|_{V_{in}=0}$$



Limiting Amplifier gain= A

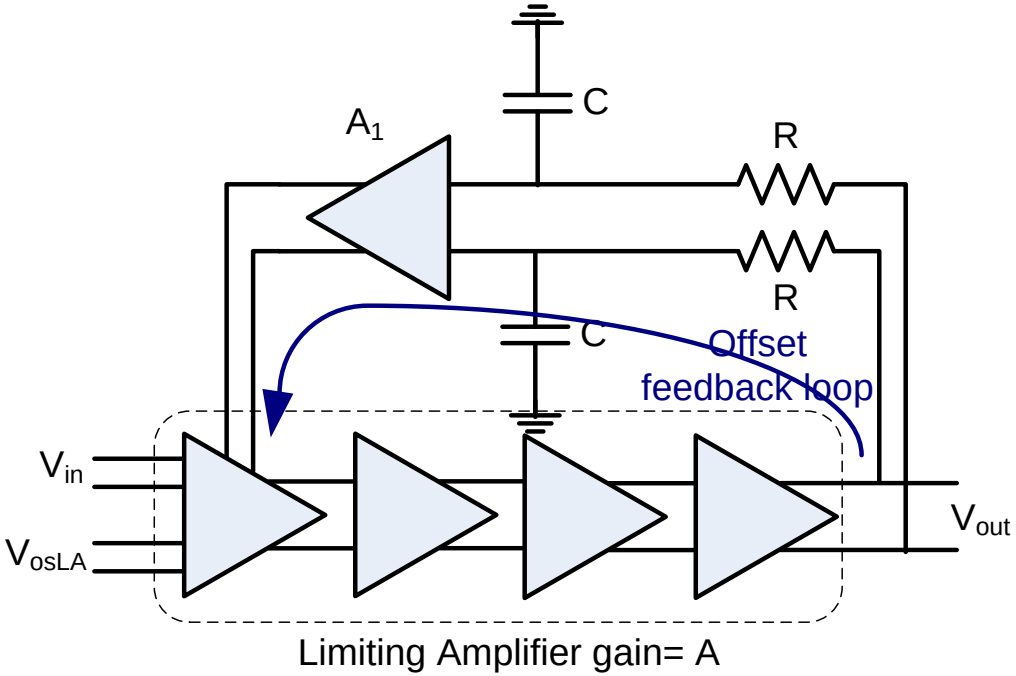
- Offsets arise from layout/fabrication mismatches
- The offset of an amplifier can be modeled with a second input signal (V_{os})
- A 30dB LA with an input referred offset of 10mVpp would result in a 310mVpp signal at the LA output
- Feedback techniques can be used to cancel the effect of offsets
- The RC low pass filter ensures only the DC offset at V_{out} is fed back

Limiting Amplifiers: Offset (Cont'd)

$$V_{out} = A(V_{osLA} - A_1 V_{out})$$

$$V_{out} = \frac{AV_{osLA}}{1 + AA_1}$$

$$V_{os1} = \frac{V_{out}}{A} = \frac{V_{osLA}}{1 + AA_1} \approx \frac{V_{osLA}}{AA_1}$$



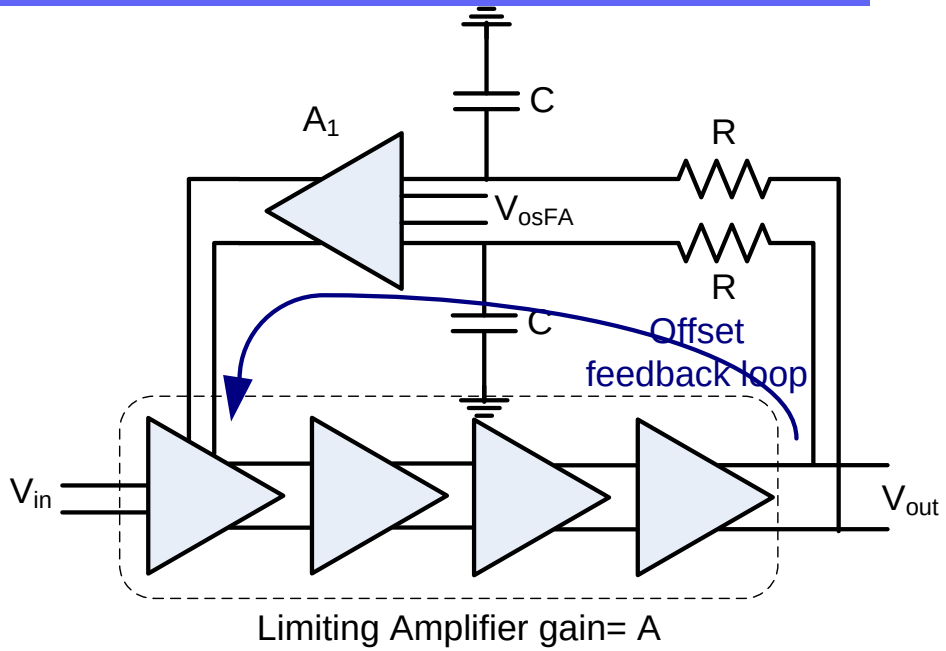
- Assume the offset of the LA is represented by the input referred offset V_{osLA}
- The feedback loop divides the LA offset by the loop gain AA_1
- This analysis assumes that the feedback amplifier is offset free

Limiting Amplifiers: Offset (Cont'd)

$$V_{out} = AA_1(V_{osFA} - V_{out})$$

$$V_{out} = \frac{AA_1 V_{osFA}}{1 + AA_1}$$

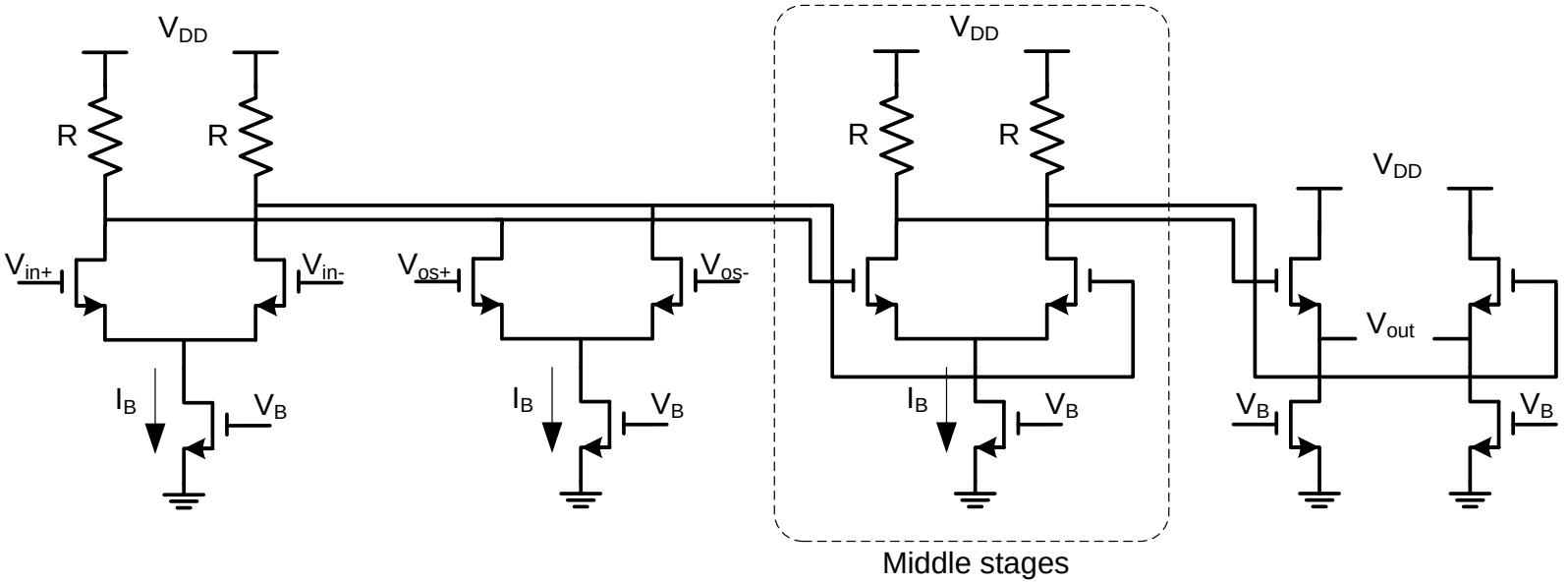
$$V_{os2} = \frac{V_{out}}{A} = \frac{A_1 V_{osFA}}{1 + AA_1} \approx \frac{V_{osFA}}{A}$$



- The offset of the feedback amplifier also contributes to the total input referred offset, but is divided by the LA gain
- V_{osLA} and V_{osFA} are generated from different blocks and should be treated as uncorrelated random signals
- Offsets are added in an rms fashion

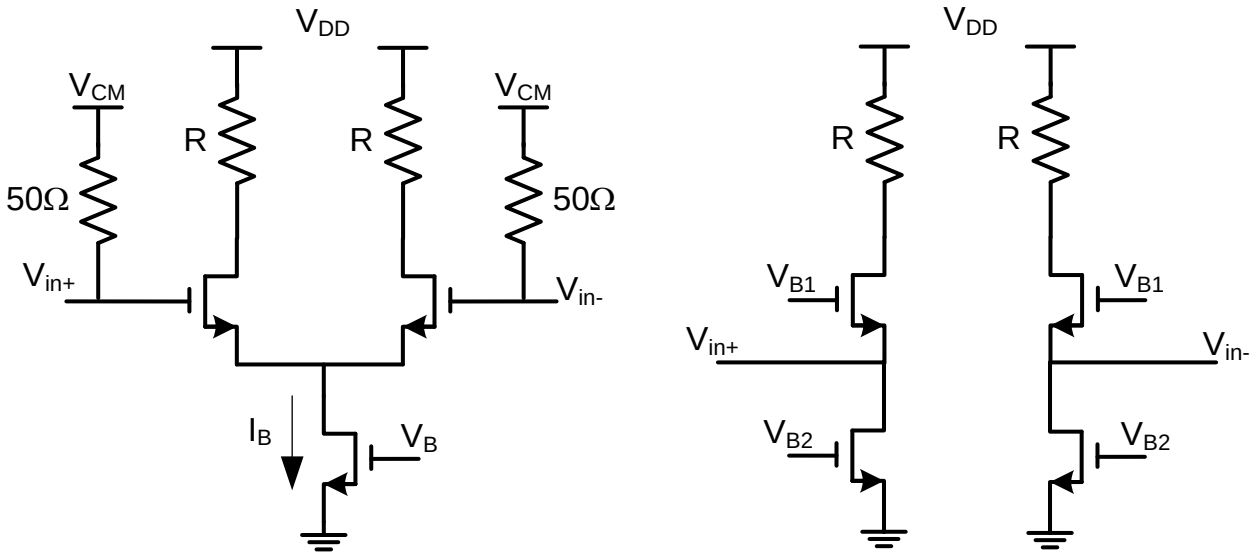
$$V_{osT} = \sqrt{V_{os1}^2 + V_{os2}^2}$$

Limiting Amplifiers (Cont'd)



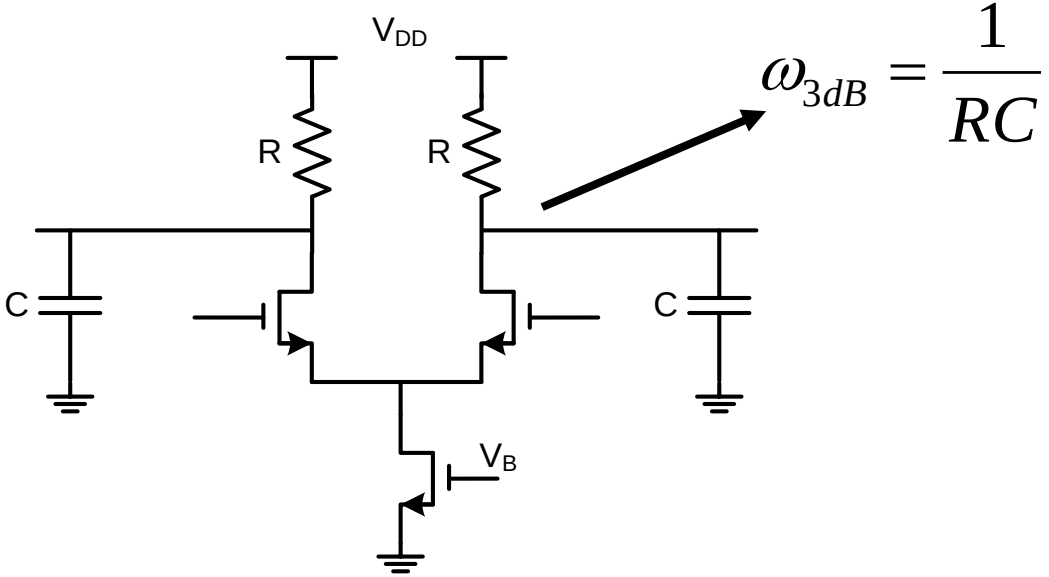
- First stage provides high input impedance, minimize loading on TIA if on the same chip
- Offset cancellation of the LA can be achieved via a differential pair that injects a differential current proportional to the offset value
- Input referred offset = V_{os+}-V_{os-}
- Middle stages could be scaled using inverse scaling to save power
- Last stage is designed to handle the loading of the CDR

Limiting Amplifiers (Cont'd)



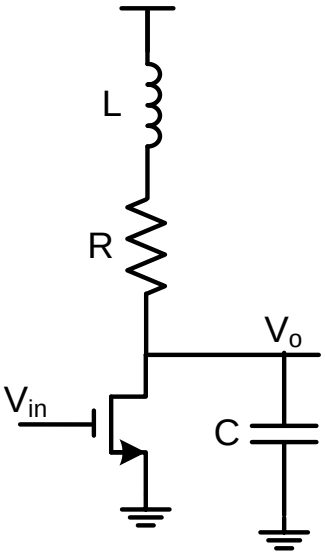
- A 50Ω interface has to be used when the TIA and LA are not integrated on the same chip
- A Differential Common-gate stage could be used as the first stage to provide a 50Ω input impedance

Bandwidth Extension Techniques



- The bandwidth of an amplifier is limited by its poles
- For this example the bandwidth is limited by the output node
- Increasing R to increase the gain reduces the 3dB bandwidth
- How can we extend the bandwidth of such an amplifier?
  - Capacitive degeneration
  - Inductive Peaking & T-coils
  - Cherry-Hooper Amplifier
  - F_t doublers

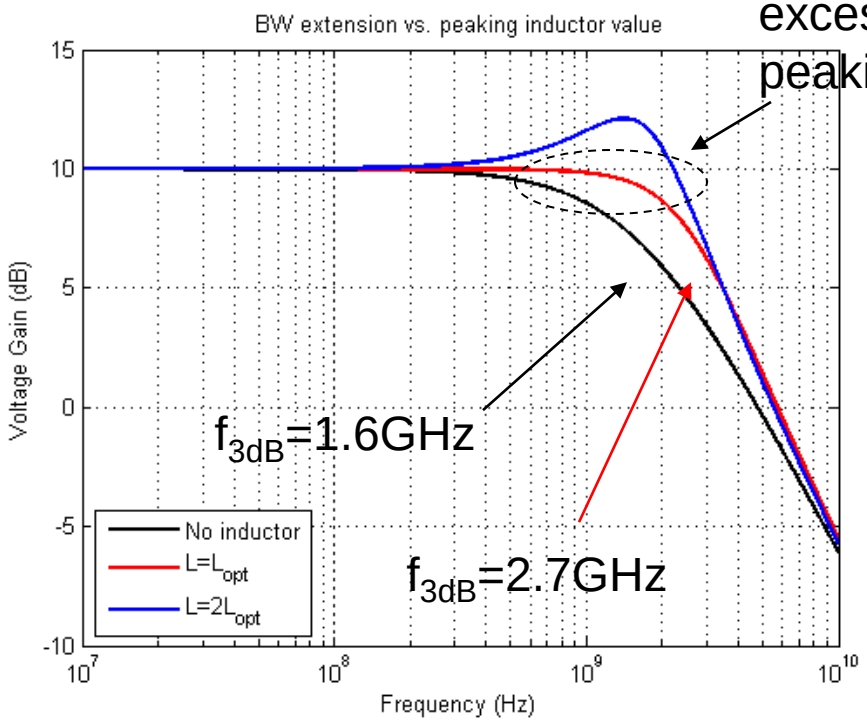
Inductive Peaking



$$\omega_z = \frac{R}{L}$$

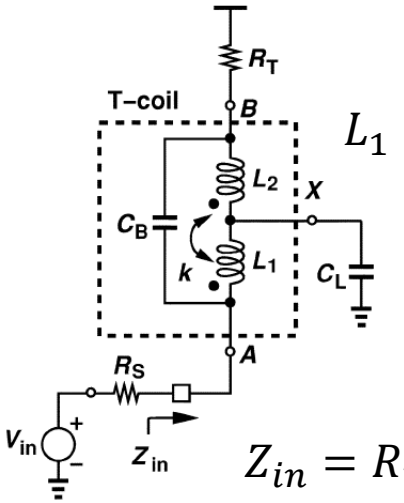
$$L_{opt} = 0.4R^2C$$

$$\omega_{3dB} = \frac{1.7}{RC}$$



- Adding a shunt inductor adds a zero to the transfer function ω_z which can help extend the bandwidth
- Choosing an appropriate value for the shunt inductor (L_{opt}) guarantees minimal peaking due to the complex poles and results in a 70% bandwidth extension
- At L_{opt} → complex poles have maximally flat response Q≈0.69

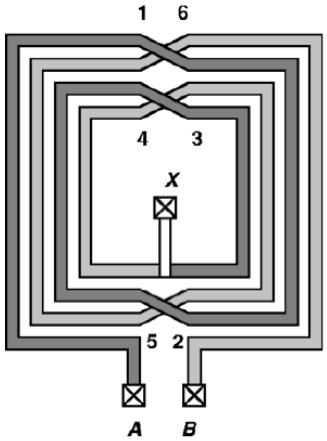
Bandwidth Extension using T-coils



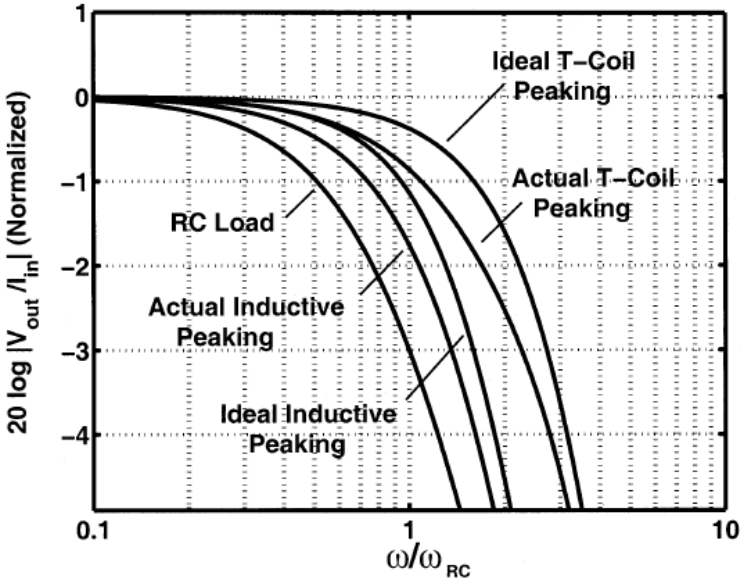
$$L_1 = L_2 = \frac{C_L R_T}{3}$$

$$C_B = \frac{C_L}{12}$$

$$k = 0.5$$



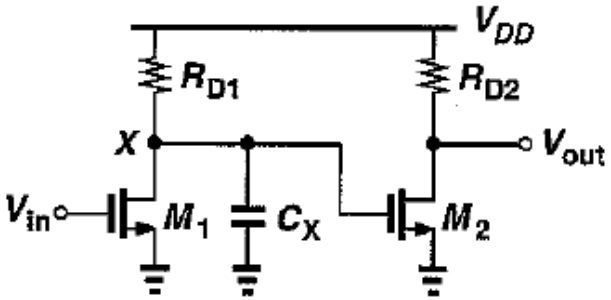
$Z_{in} = R_T$ regardless of frequency

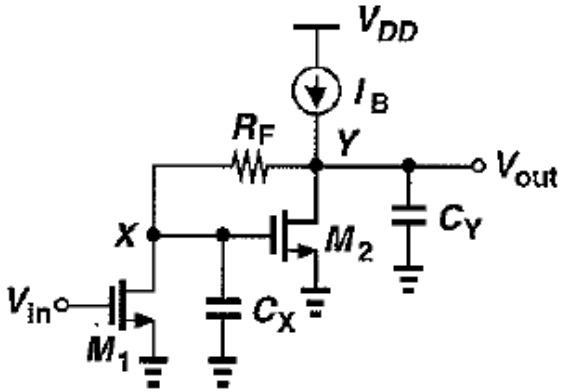


- A T-coil consists of two coupled inductors with a coupling coef. k and a bridge capacitor C_B
- The input is applied to terminal A, the termination resistor → terminal B and the load capacitance C_L → terminal X
- At low frequencies, L_1+L_2 short the input to R_T, & at high frequencies, C_B plays the same role
- Symmetric spiral coupled inductors can be used to realize a T-coil with the center tap representing the output terminal
- BW is broadened by a factor of 2.72, 70% than inductive peaking

S. Galal and B. Razavi, "Broadband ESD protection circuits in CMOS technology," in IEEE Journal of Solid-State Circuits, vol. 38, no. 12, pp. 2334-2340, Dec. 2003

Cherry-Hopper Amplifier



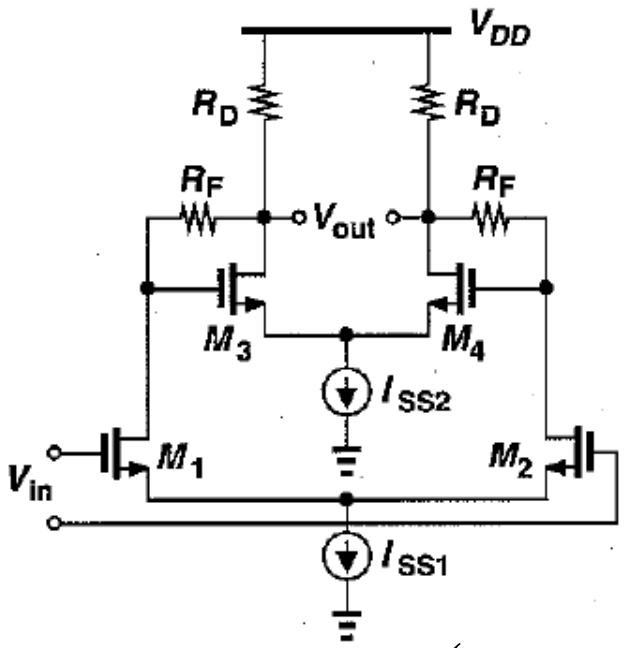


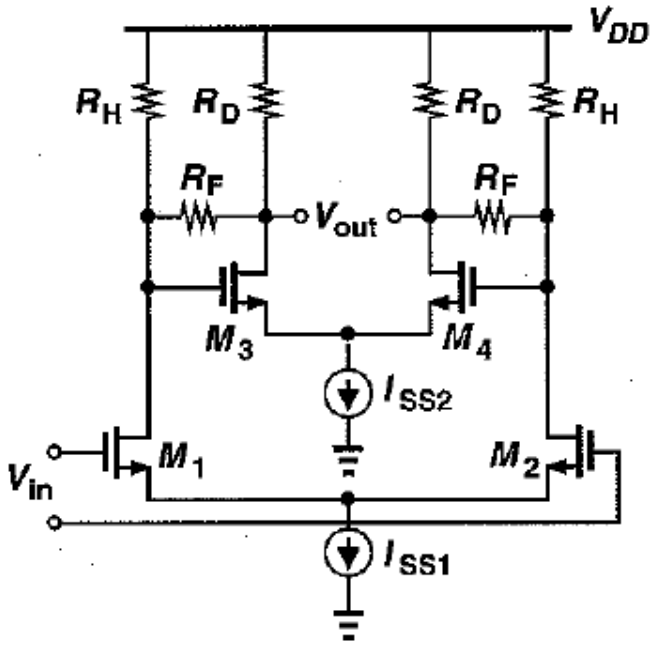
$$|A_{v1}| = g_{m1}R_{D1}, \omega_{p,X} = \frac{1}{R_{D1}C_X} \qquad |A_v| = g_{m1}R_F - \frac{g_{m1}}{g_{m2}}, \omega_{p,X} \approx \frac{g_{m2}}{C_X}, \omega_{p,Y} \approx \frac{g_{m2}}{C_Y}$$

- The gain is apprx. the same as the CS with R_F as the load, but much higher pole frequencies
- Deriving the exact transfer function of the Cherry-Hopper Amplifier, and assuming the 2 poles are equal results in:

$$\omega_{p,1} = \omega_{p,2} = \frac{2g_{m2}}{C_X + C_Y + g_{m2}R_F C_{GD2}}$$

Differential Cherry-Hopper Amplifier

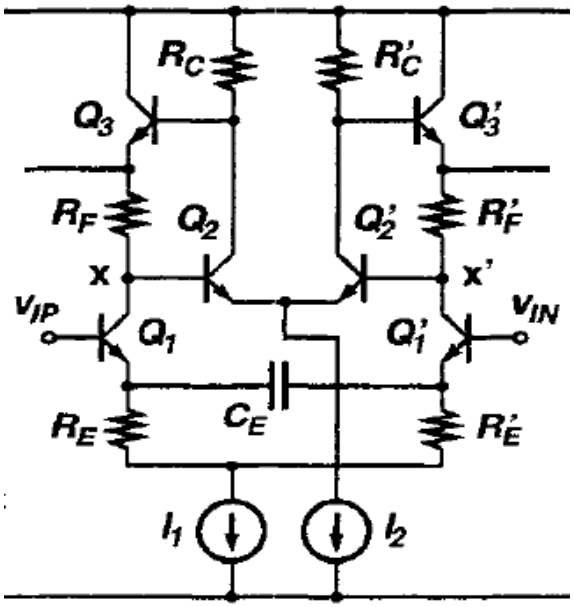


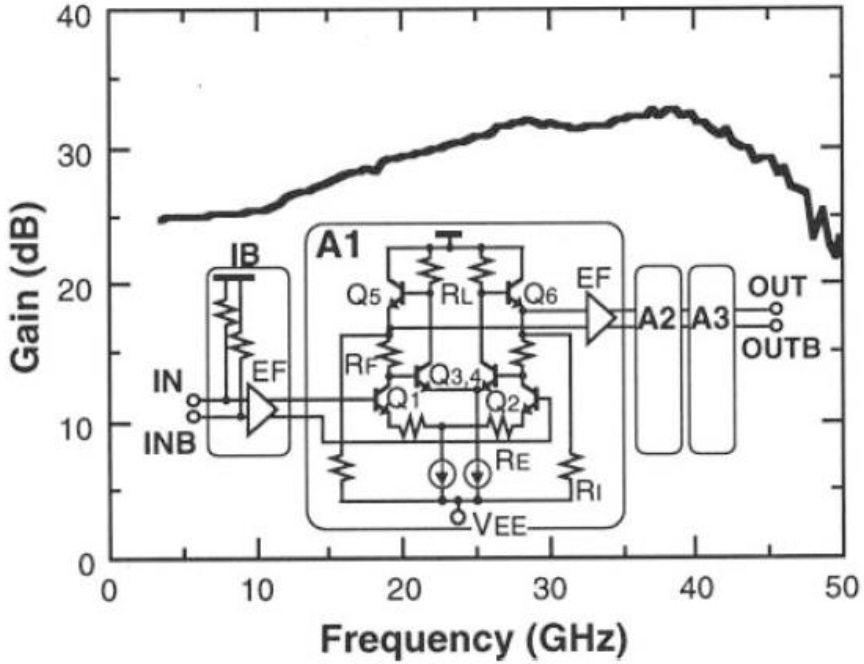


$$V_{DD,\min} = \frac{(I_{SS1} + I_{SS2})}{2} R_D + \frac{I_{SS1}}{2} R_F + V_{GS3,4} + V_{ISS2}$$

- Instead of large PMOS current mirrors a resistor is used for biasing → imposes gain-headroom issues
- Adding R_H help route some of the bias current away from R_F

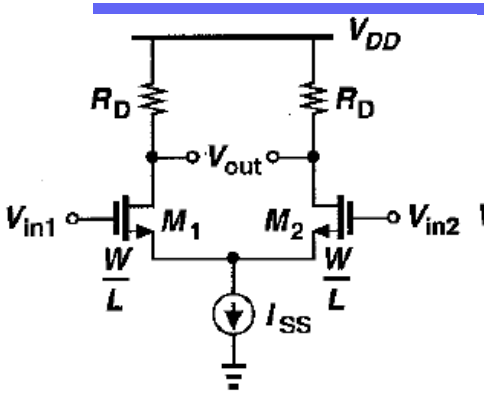
ISSCC2000: 45GHz Trans-impedance 32dB Limiting Amplifier and 40Gb/s ..Optical Receiver

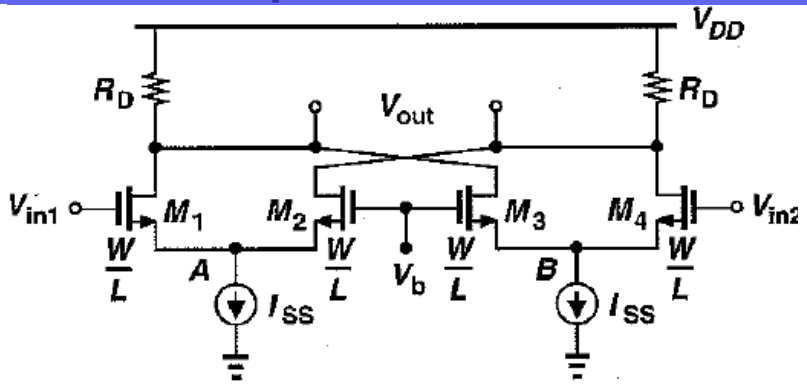


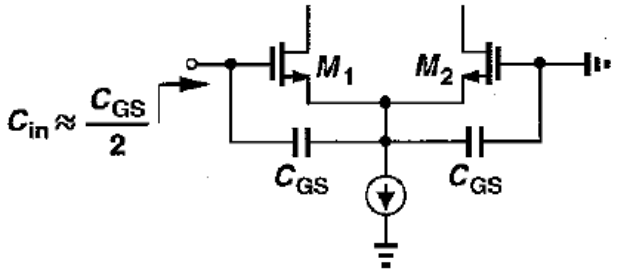


- Differential Cheery-Hopper Amplifier
- Capacitive degeneration helps extend the BW of stage 1
- Emitter followers are inserted in the feedback path to help derive the load capacitance (lower output impedance) and isolate the collectors of Q2 from the load capacitance

F_T Doublers







$$V_{out} = g_{m1,2} R_D (V_{in1} - V_{in2})$$

- Input ports are placed in series & output ports are connected in parallel
- Bias voltage V_b tracks the input common mode of V_{in1} & V_{in2}
- Using superposition: $V_{out} = g_{m1,2} R_D (V_{in1} - V_{in2})$
- Same voltage gain but with half the input capacitance
- Input capacitance is halved while maintaining the same gain → F_T doubler
- Double the area & power consumption, & voltage drop across R_D (headroom)
- Doubles the output capacitance → lowers output pole
- Current source capacitance limits the reduction in the input capacitance