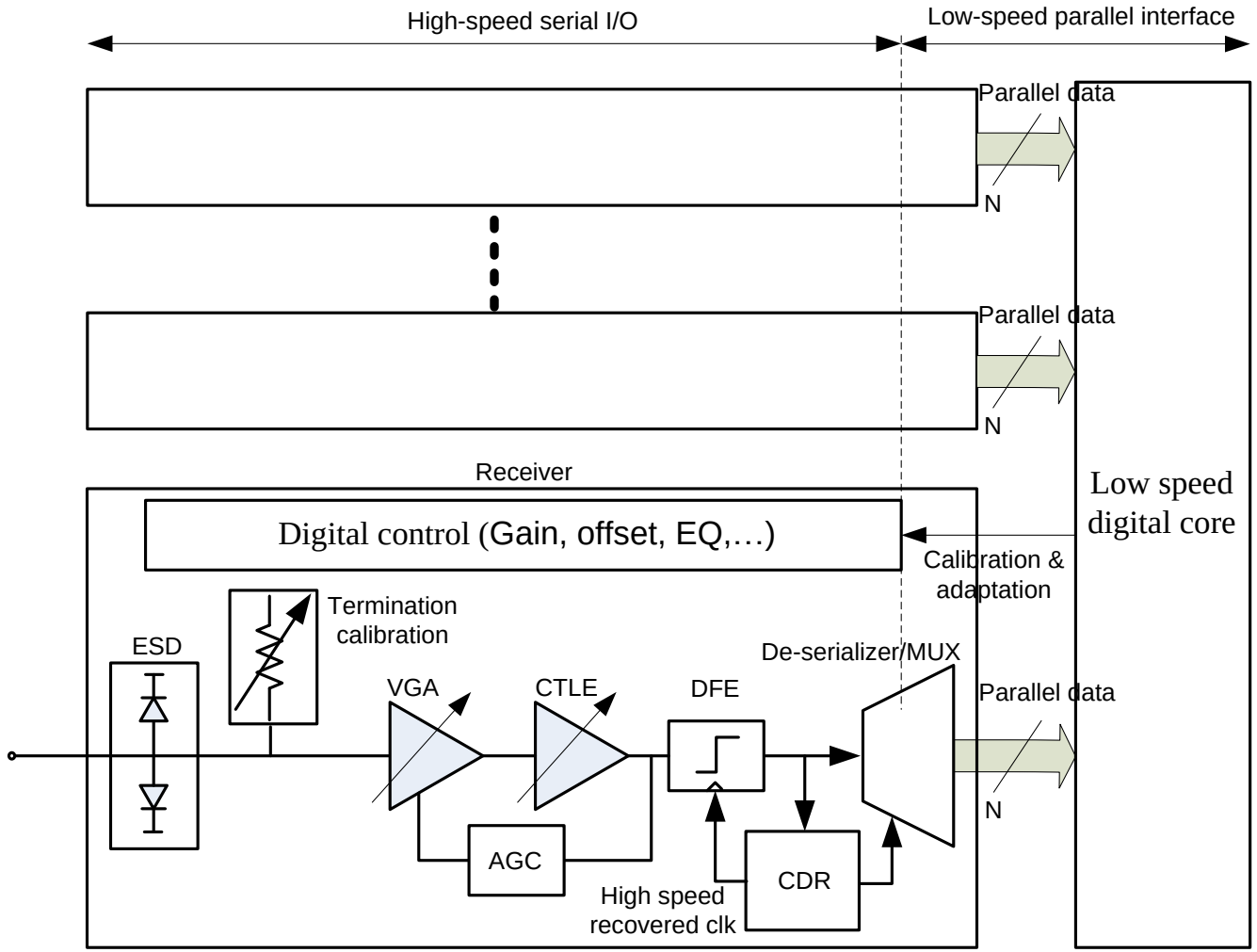
High-Speed Wire Line Receivers

Lecture 5

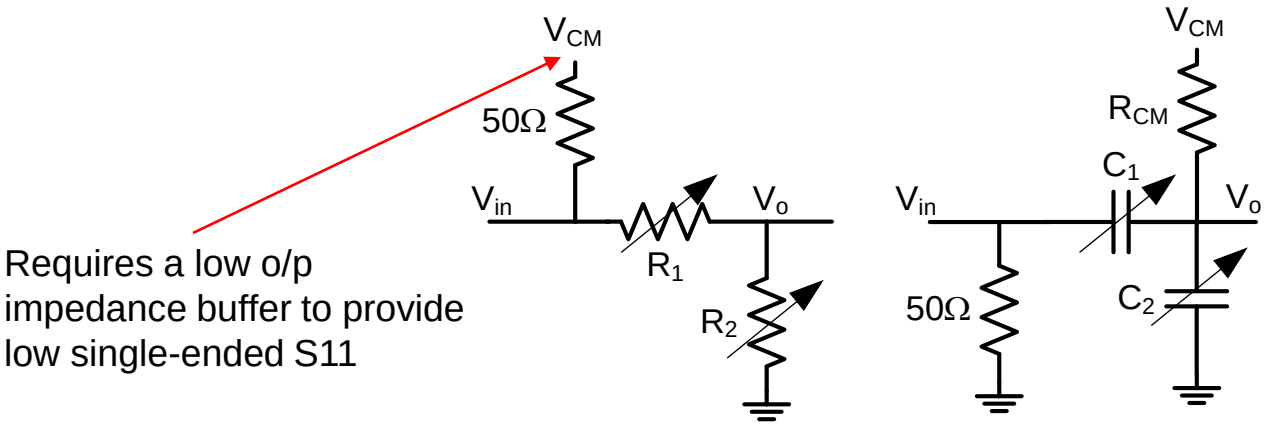
Receiver Block Diagram



Variable Gain Amplifiers (VGA)

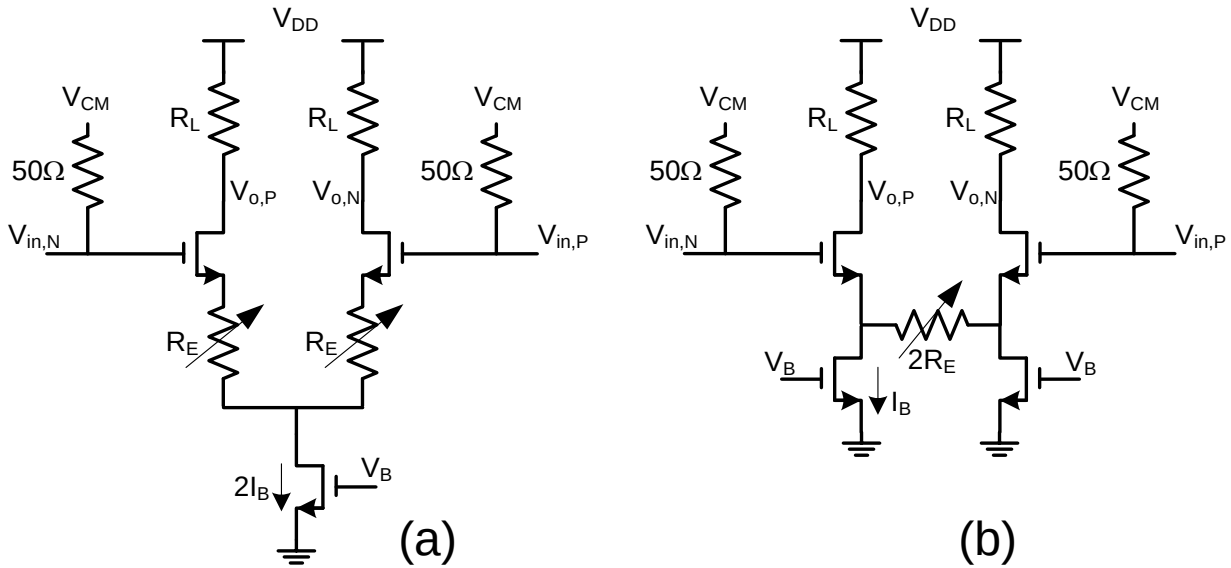
- Standard defines min and max signal amplitude
- Exact amplitude used by the transmitter is unknown to the Rx a priori
- To prevent saturation of the receiver for very large amplitudes and degradation of the BER for very small amplitudes a VGA is required
- VGA can by active or passive or a mix
  - Passive: resistive or capacitive dividers
  - Active: CML with variable load/degeneration resistors
  - Both active and passive: to increase the tuning range without losing bandwidth
- AGC (automatic gain control) loop is required to sense the swing of the signal and automatically adjust the VGA gain
- Key VGA design challenges:
  - minimize its input capacitance for better high frequency return loss (S_{11})
  - minimize noise contribution (first stage in the receiver chain)
  - high linearity
  - gain tuning range

Passive Attenuators



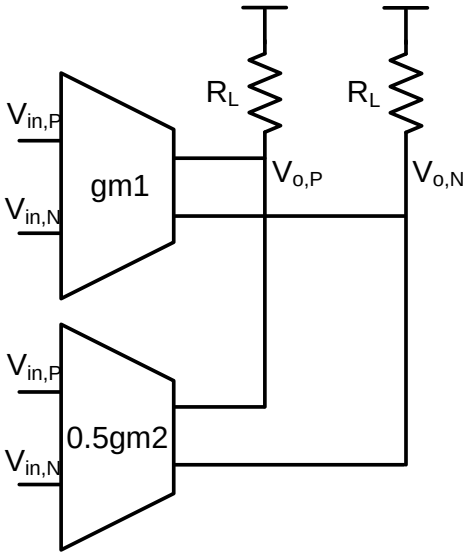
- If the passive VGA is the 1st block in the receiver, a 50 ohm termination is required to properly terminate the channel
- In AC coupled links the Rx common mode needs to be supplied to the receiver
- $A_v=R_2/(R_1+R_2)$ or $C_1/(C_1+C_2)$
- To increase the tuning range both the series and shunt components can be programmable in opposite directions to maintain a fixed impedance

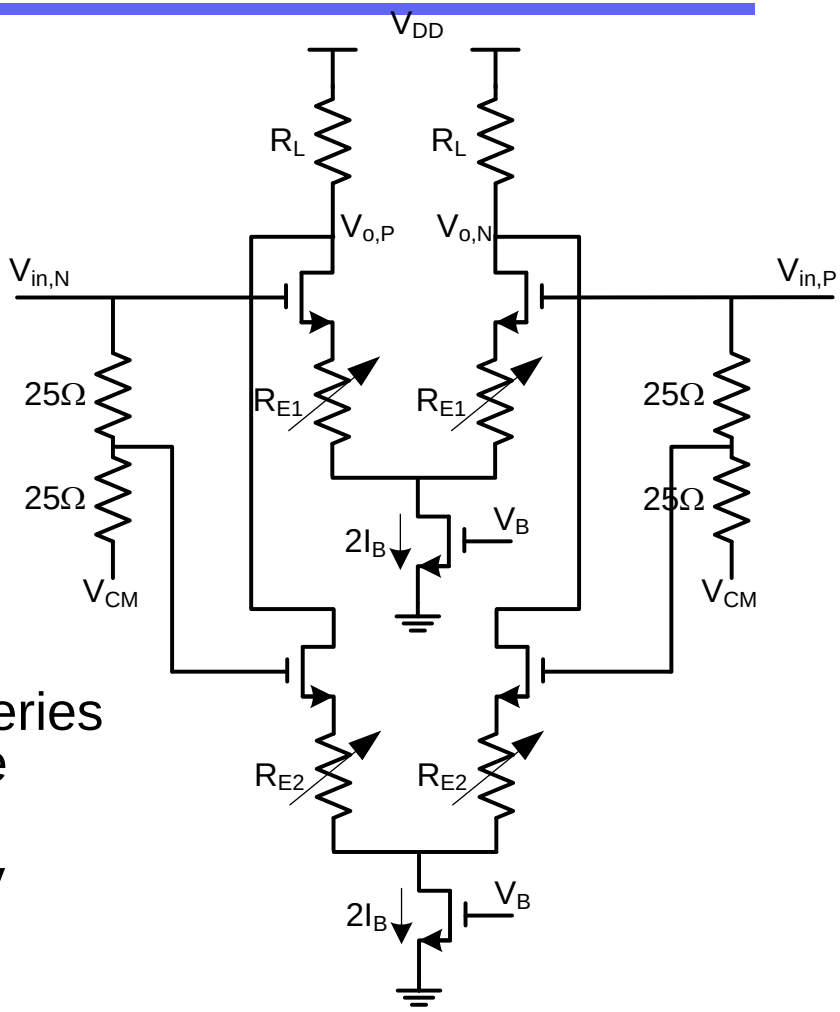
Active VGAs



- Source degeneration can be used to control the gain of a CML stage, & improve linearity
- $A_v \approx -R_L/R_E$
- The dominant pole is at the output node → R_L and the load capacitance determine the circuit speed (hence the fixed R_L)
- What is the differences between the two circuits?
  - R_E consumes some voltage headroom in circuit (a), non in (b)
  - Noise contribution by the current source doesn't appear at the differential output in (a), whereas in (b) each current source is treated as an independent noise source

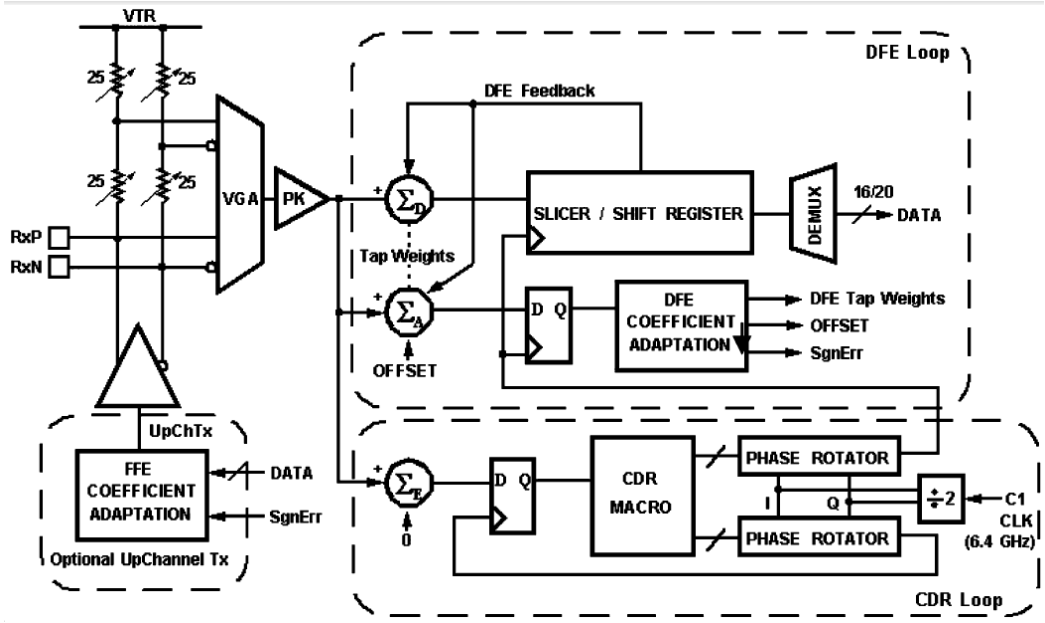
Combining Passive & Active VGAs

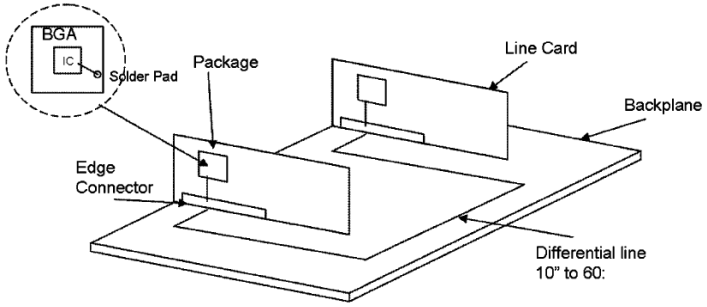


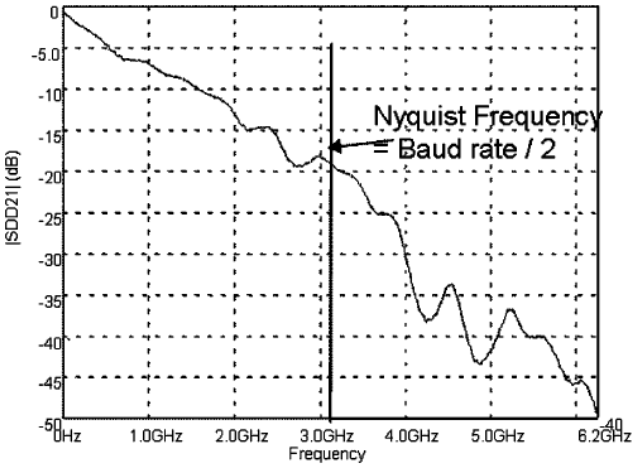


- The 50 Ohms can be divided into 2series resistors and used to provide half the signal
- Gain control can be achieved by fully turning ON/OFF the gm blocks or by controlling their relative gain
- $A_v=a_1*R_L/R_{E1}+a_2*0.5*R_L/R_{E2}$

JSSC 2005: 6.4-Gb/s CMOS SerDes core with FFE and DFE



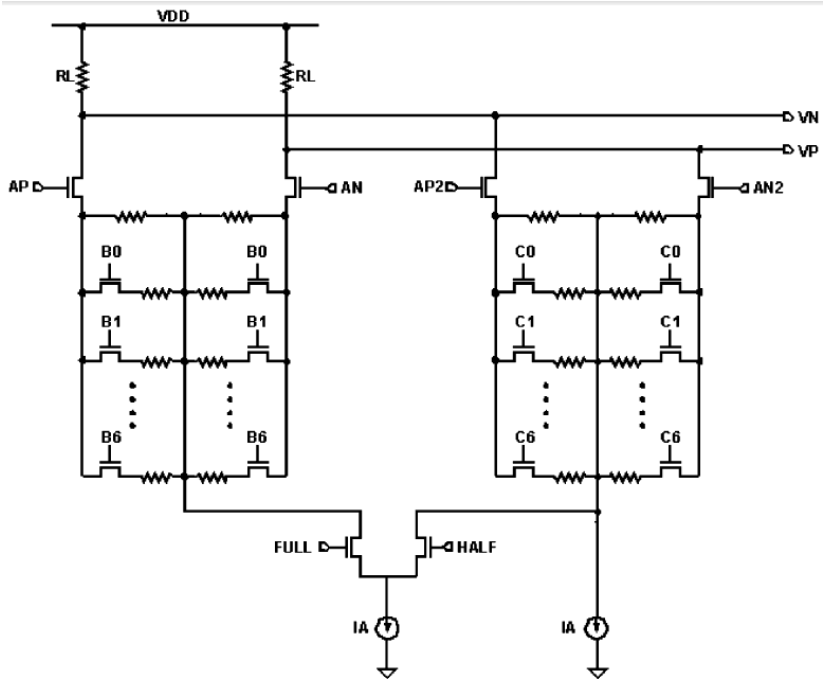




- The receiver consists of a :VGA, peaking amplifier, 5-tap DFE, & analog phase-rotator-based CDR loop
- Splitting the received signal into full-amplitude and half-amplitude paths improves linearity of the VGA for high input levels and to allow operation with high input signals at low supply voltages

T. Beukema et al., "A 6.4-Gb/s CMOS SerDes core with feed-forward and decision-feedback equalization," in IEEE Journal of Solid-State Circuits, vol. 40, no. 12, pp. 2633-2645, Dec. 2005.

JSSC 2005: 6.4-Gb/s CMOS SerDes core with FFE and DFE

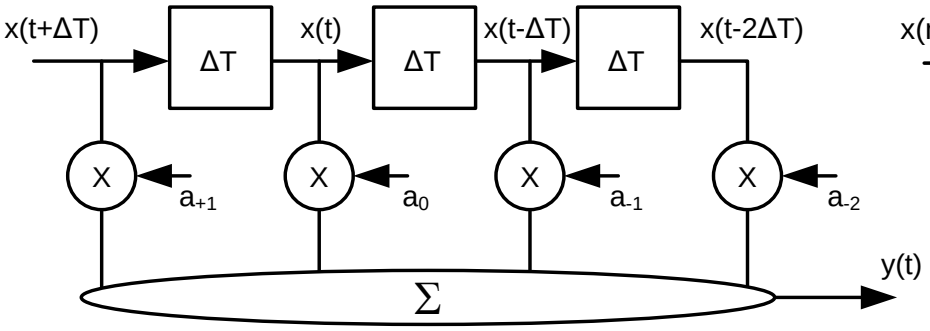


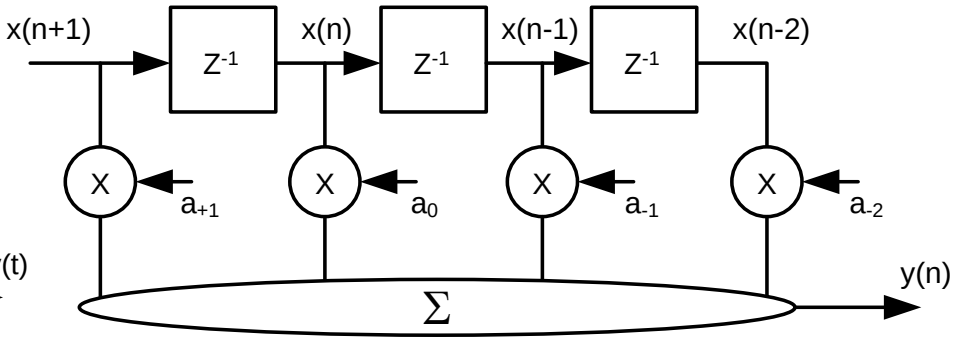
- The full- and half-signal data paths each drive a separate switched-gain amplifier
- The gain is adjusted by setting the degeneration resistance of each amplifier
- At low values of gain, only the half-signal amplifier is active
- As the gain is increased, the full-signal amplifier is enabled
- The common mode voltage at the output is maintained across gain states by steering I_A of the HALF amplifier to the FULL amplifier when it is switched ON

Receiver Equalization

- Linear
  - Continuous time
    - Continuous time linear equalizers (CTLE): Passive/active
    - Rx analog FFE
  - Sampled (Not widely used in Rx since clock information is still not available before equalization)
    - Rx FFE (mostly relay on Tx FFE)
- Non-Linear
  - Decision feedback equalizers (DFEs)
- Rx Equalization types and amounts are usually determined by the standards
- In most cases Rx equalization is a mixture of CTLE & DFE

Continuous time vs. sampled Rx FFE





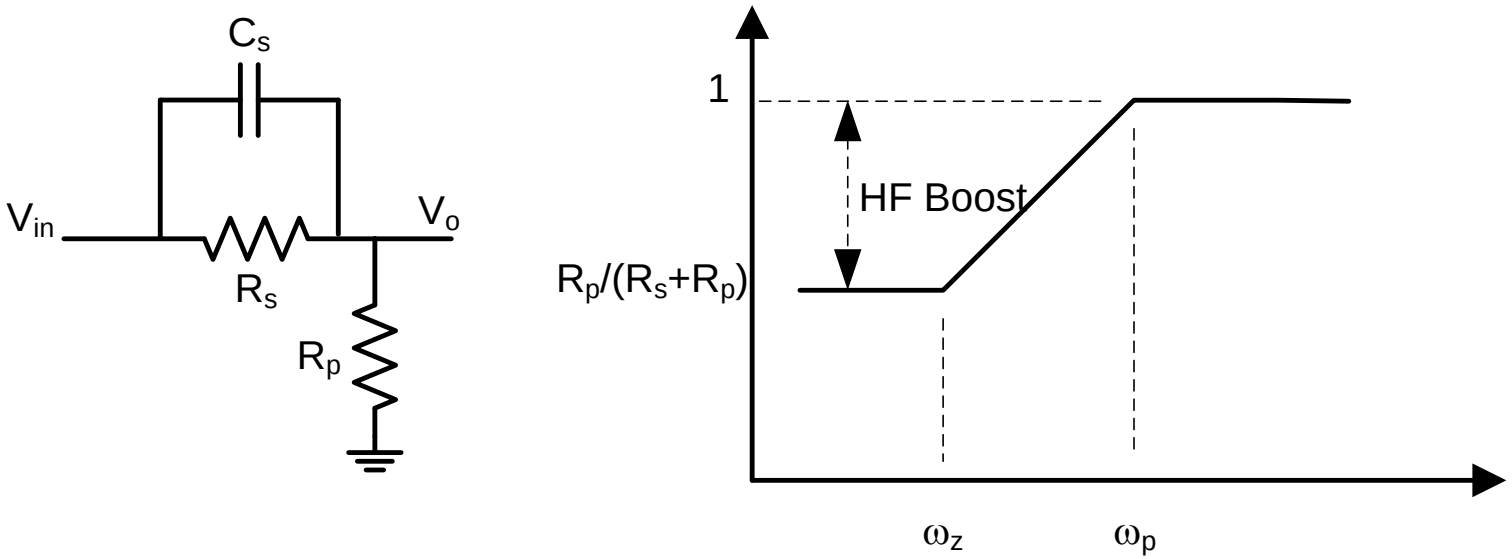
Analog Rx FFE:

- Needs precise delay adjustment
- Can use a delay locked loop to adjust the delay element for a given data rate
- Delay elements have a limited tuning range → limiting the operating data rates

Sampled Rx FFE:

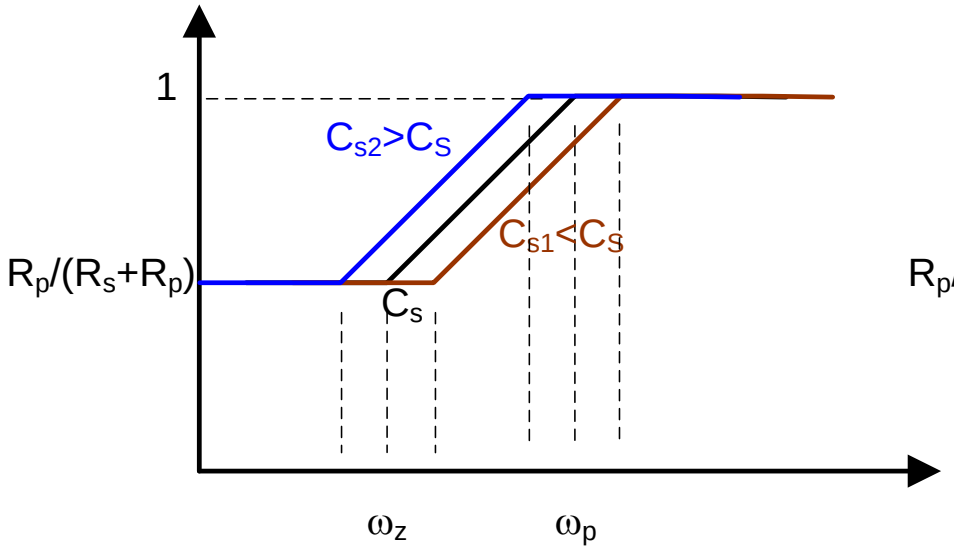
- Needs information about the recovered clock!
- Delay elements can be implemented using sample and hold blocks, allowing it to operate for any data rate, only limit is the VCO tuning range

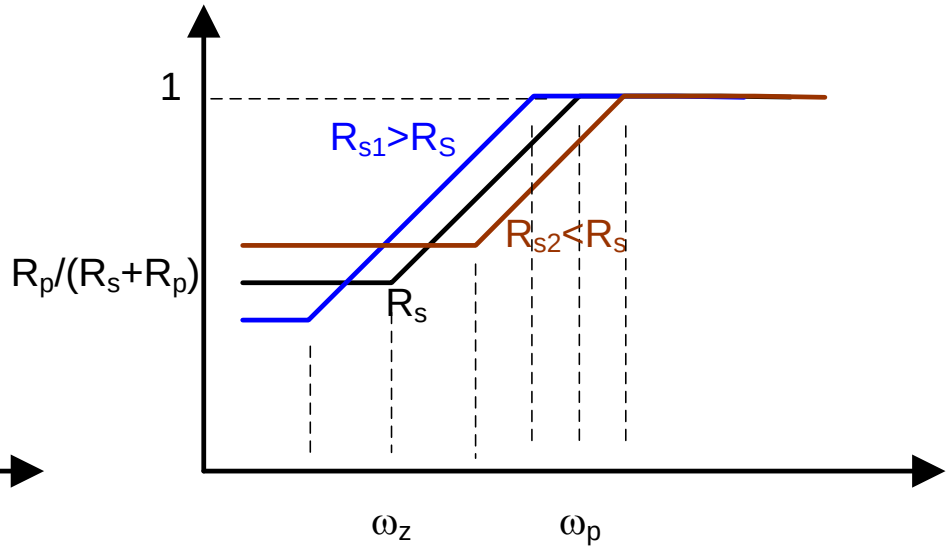
Passive Continuous time linear Equalizer (CTLE)



- At low frequencies, C_s is an open circuit and the DC gain is $R_p/(R_s+R_p)$
- At high frequencies, C_s shorts R_s and the HF gain is 1
- The HF boost is $20*\log_{10}(1+R_s/R_p)$
- C_s adds a zero at $\omega_z= 1/R_sC_s$ and a pole at $\omega_p=1/(R_s||Rp)C_s$
- Note that a passive CTLE can't results in gain >1, to achieve HF boost it lowers the DC gain (de-emphasis)
- What is the impact of the input capacitance of the following stage?

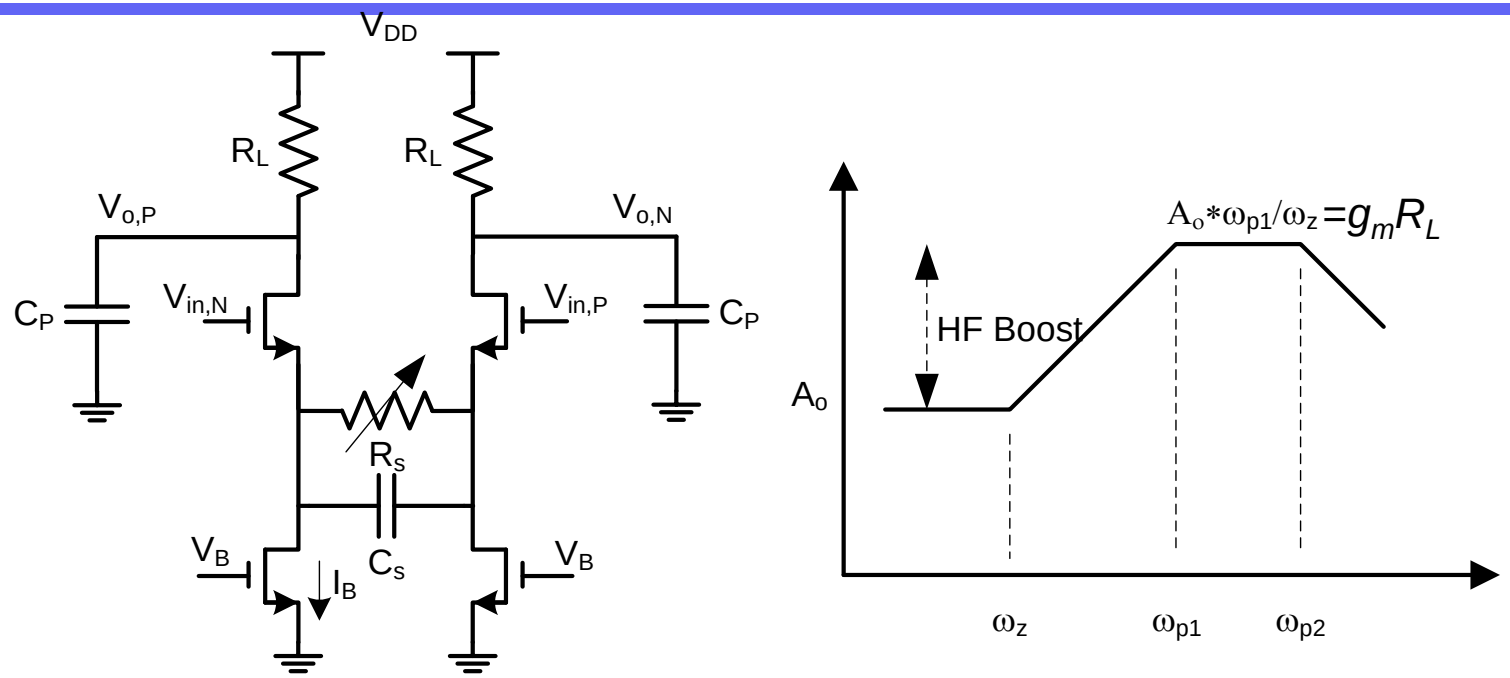
Passive CTLE (Cont'd)





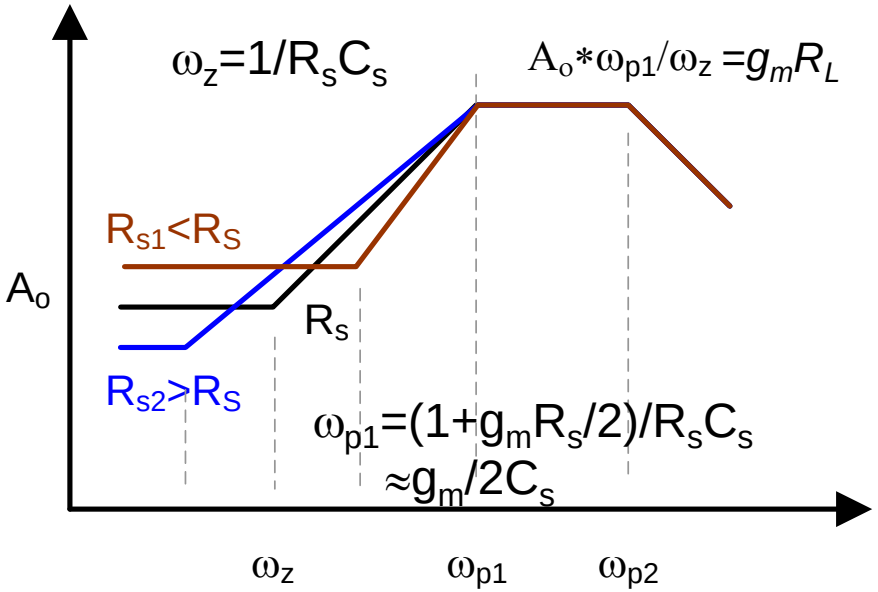
- Varying C_s shifts the locations of the zero and pole but leaves the HF boost constant
- The HF boost can be programmed by varying one or both the resistors
- Note that the DC gain is also changing with the HF boost, VGA action might be necessary to fix the DC swing
- AGC will need to re-adjust the gain after the CTLE adaptation
- How does the curves look like if we change R_p?

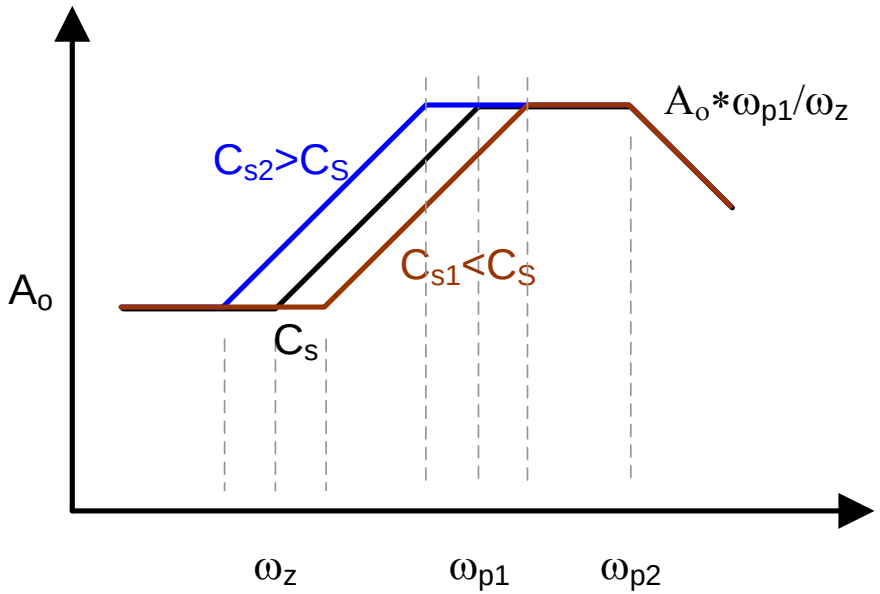
Active CTLEs



- For low frequencies, C_s acts as an open circuit $A_o=g_mR_L/(1+g_mR_s/2)$
- For High frequencies, C_s shorts Rs increasing the gain
- The equalizer output pole is determined by the output node $\omega_{p2}=1/R_LC_p$
- C_s introduces a zero at $\omega_z=1/R_sC_s$, and a pole at $\omega_{p1}=(1+g_mR_s/2)/R_sC_s$
- The HF boost is determined by the ratio $\boldsymbol{\omega_{p1}/\omega_z=(1+g_mR_s/2)}$
- Hence, by controlling R_s, the HF boost can be adjusted

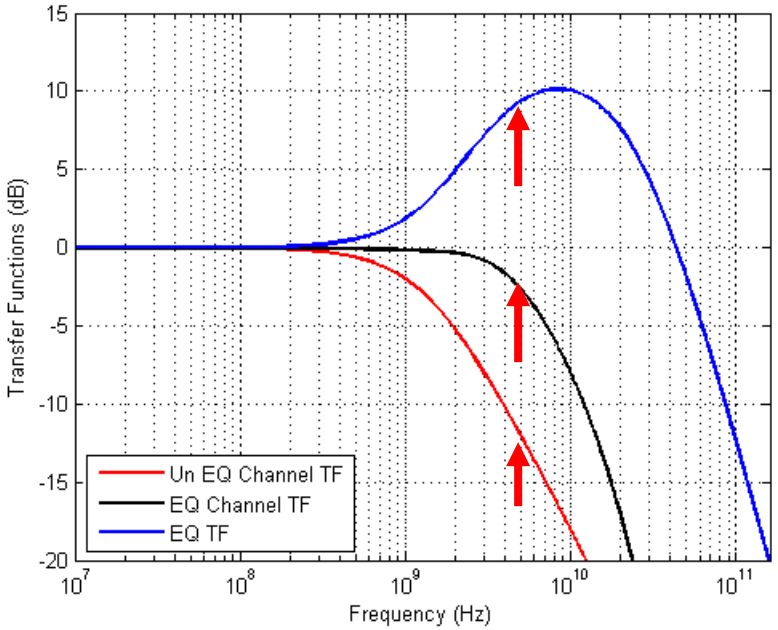
Active CTLE (Cont'd)

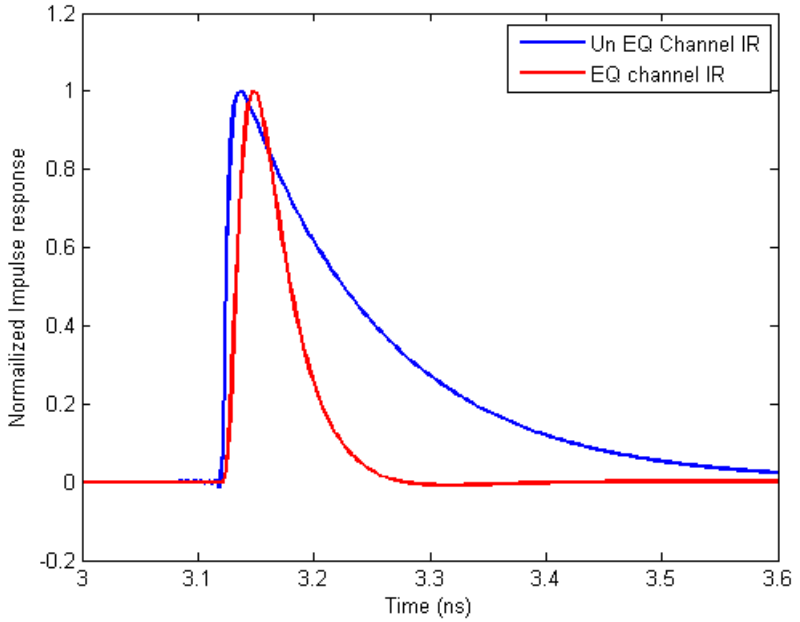




- The CTLE frequency response can be adjusted by varying the degeneration resistor or capacitor or both
- Varying R_s changes the HF boost and the DC gain,
- The VGA gain should compensate for the DC gain change
- Varying C_s doesn't impact the DC gain
- In order to increase the boost range multiple stages can be cascaded

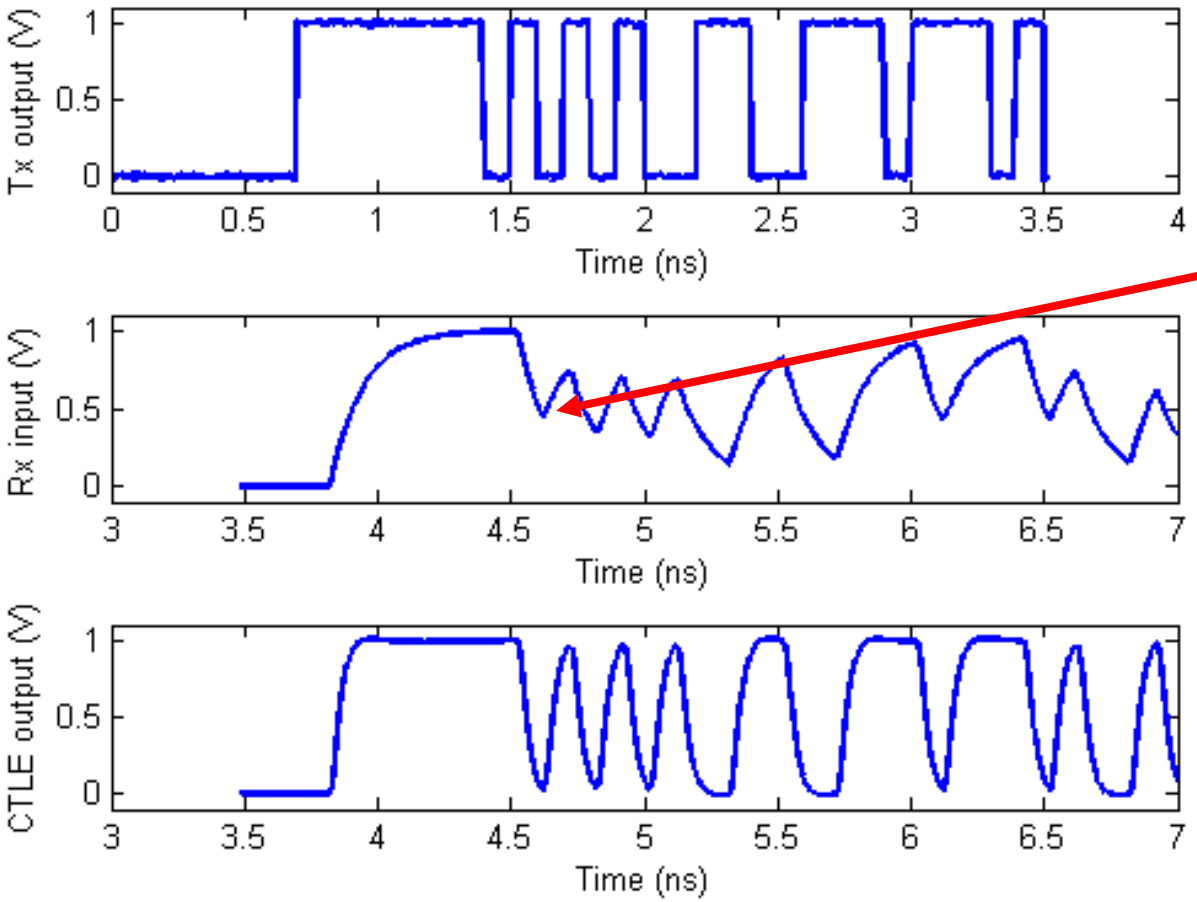
Un Equalized vs. Equalized Channel Response





- Channel has 12dB loss at Nyquist (5GHz)
- A 2 stage equalizer is used to compensate this channel
- The combined EQ stages provide up to 9.5dB of boost at Nyquist
- The equalized channel 3-dB BW is roughly 5GHz
- The channel impulse response shows significant pulse spreading before equalization

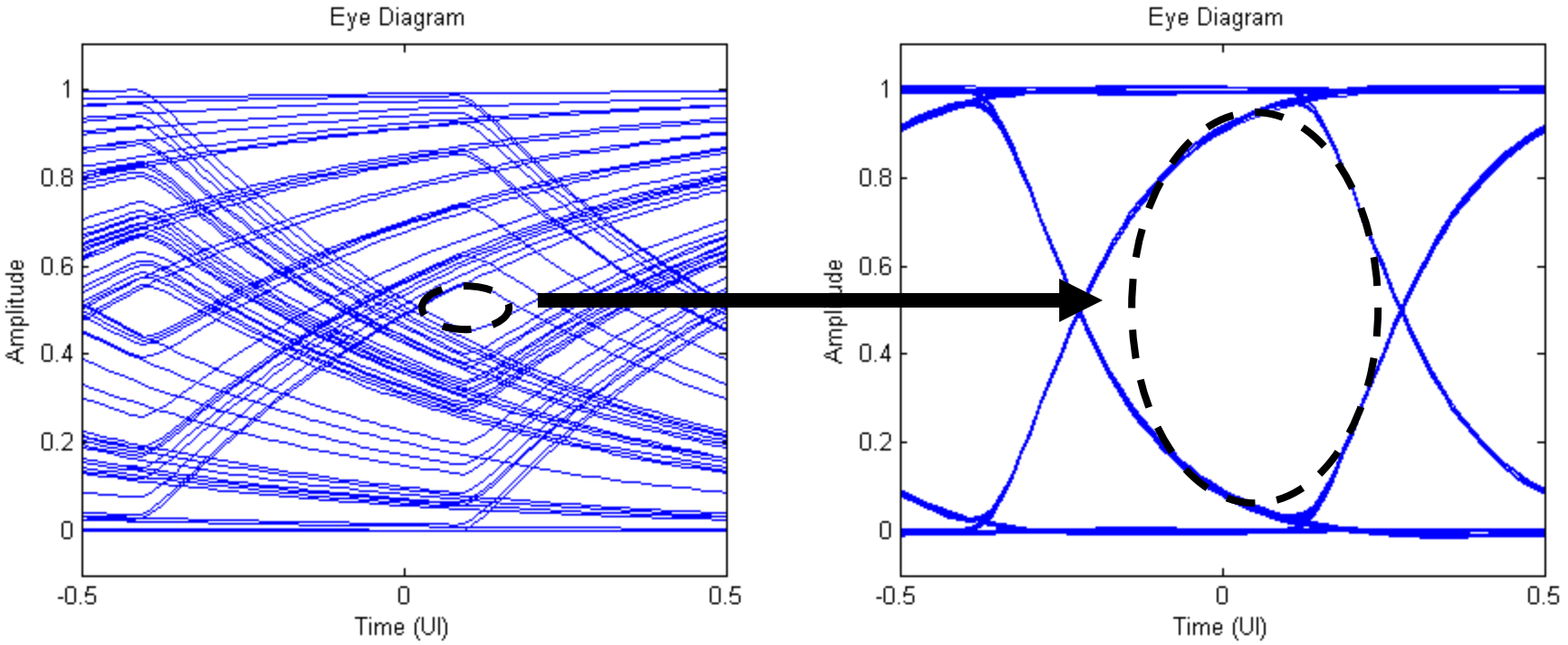
10Gbps Transient waveforms



Single-bit transitions show significant ISI

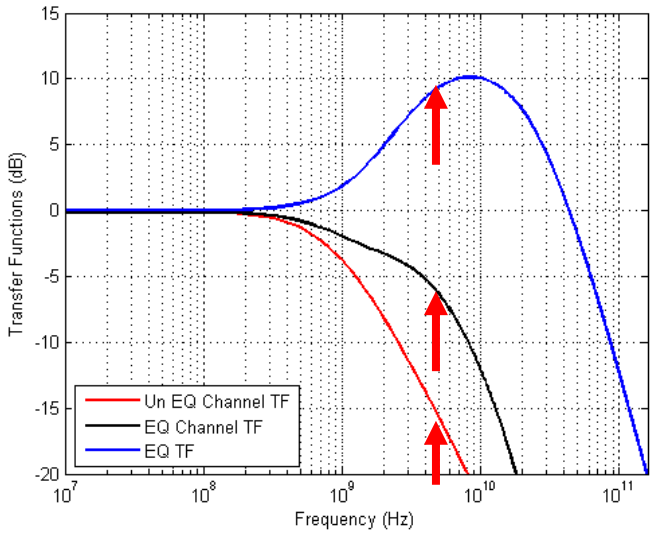
Single-bit transitions and CIDs have roughly the same swing at the CTLE output

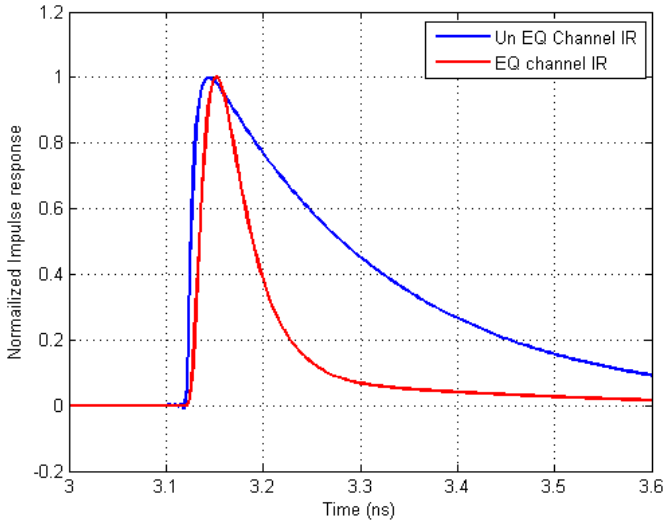
10Gbps Eye diagrams before & after the CTLE



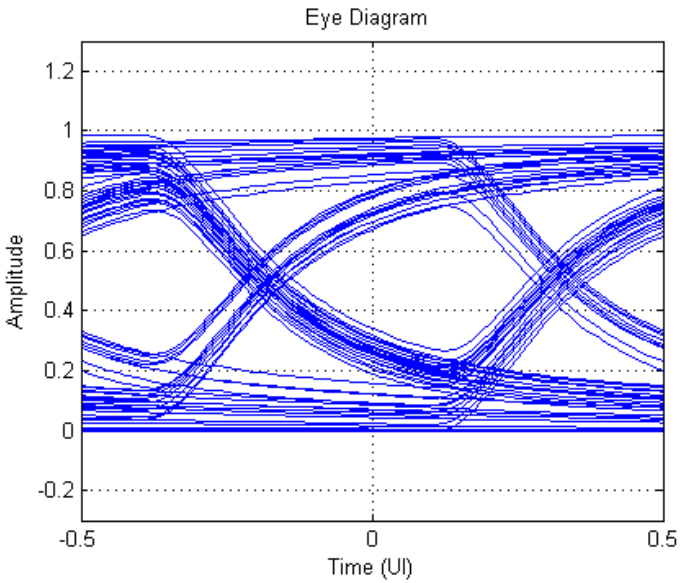
- The CTLE is capable of restoring the 10Gbps input eye from a nearly closed eye
- For this scenario, the CTLE does not provide any DC gain, since the outer eye opening is the same before and after the CTLE

Under Equalized Scenario

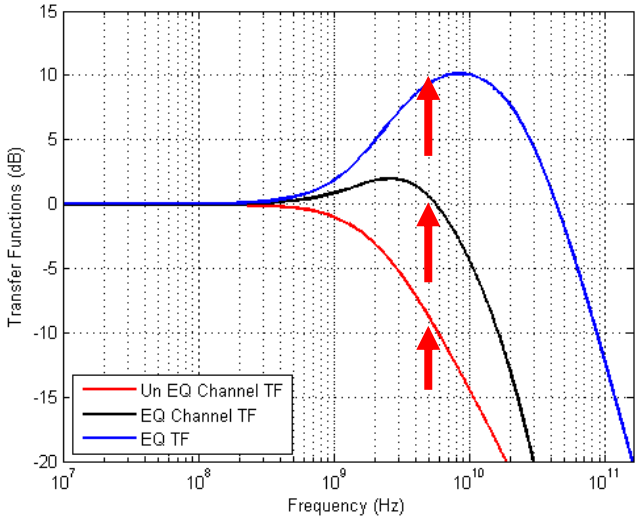


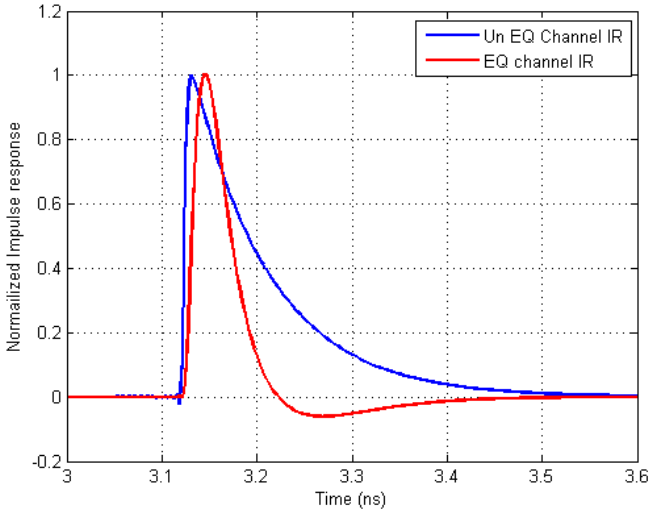


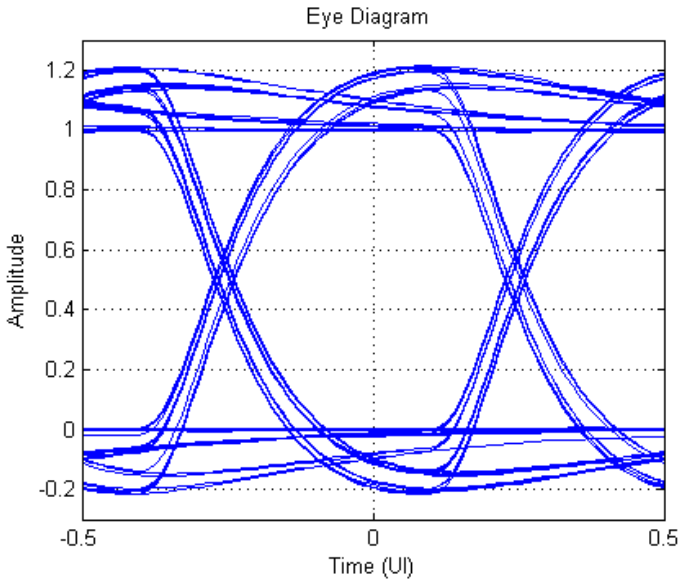
- If channel has higher loss @ F_N
- Equalized channel response starts rolling off before Nyquist frequency (6.5dB @ 5GHz)
- Equalized impulse response still has residual ISI
- Eye has vertical/horizontal eye closure



Over Equalized Scenario



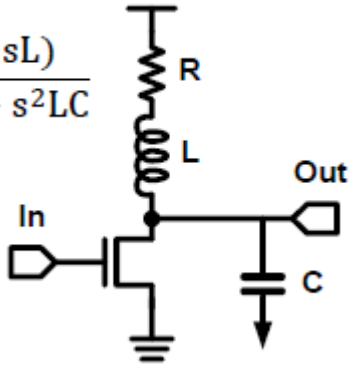


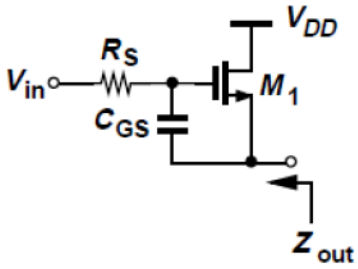


- If channel has less loss @ F_N
- Equalized channel response exhibits excessive boost
- Equalized impulse response has an under-shoot
- Eye shows excessive boost for transition bits

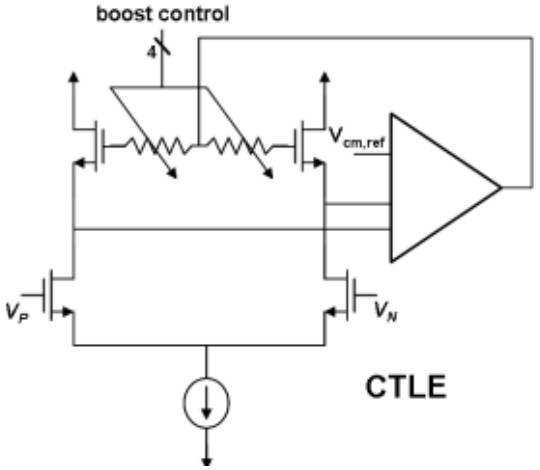
CTLE Using Inductive Loads

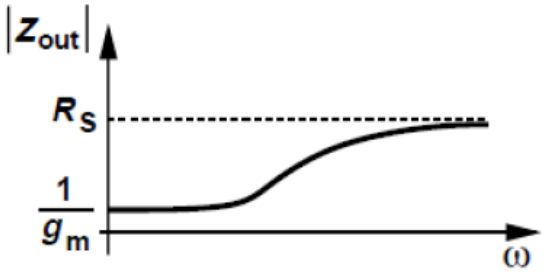
$$H(s) = \frac{g_m(R + sL)}{1 + sRC + s^2LC}$$





$$Z_{out} = \frac{1 + sC_{gs}R_S}{g_m + sC_{gs}}$$





- A series inductor with the load resistance provides a fixed zero that results in a high frequency boost
- CTLEs can use a differential-pair with inductive peaking
- Active inductors improves the portability of the design to other technologies/metal stacks and help reduce the CTLE area
- Furthermore, tuning the gate resistor R_s allows digitally tuning the zero location/high frequency boost
- However active inductors have worse noise/linearity compared to spiral inductors

M. Ramezani et al., "An 8.4mW/Gb/s 4-lane 48Gb/s multi-standard-compliant transceiver in 40nm digital CMOS technology," 2011 IEEE International Solid-State Circuits Conference, 2011, pp. 352-354.