CICC

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Clocking for Serial Links

Saurabh Saxena

Department of Electrical Engineering

Indian Institute of Technology Madras

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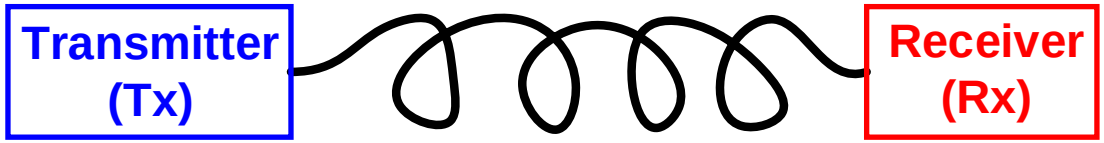
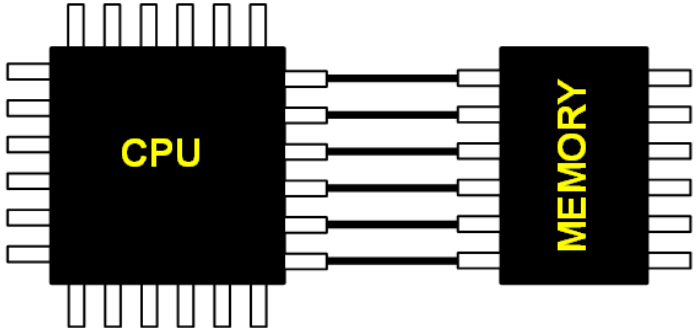
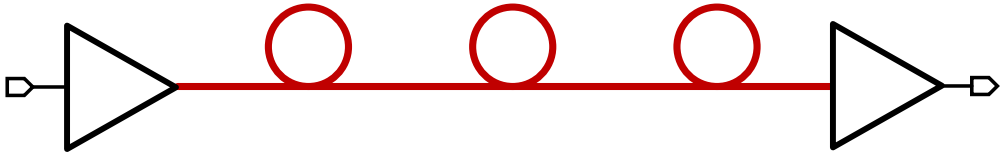
Serial Link Applications



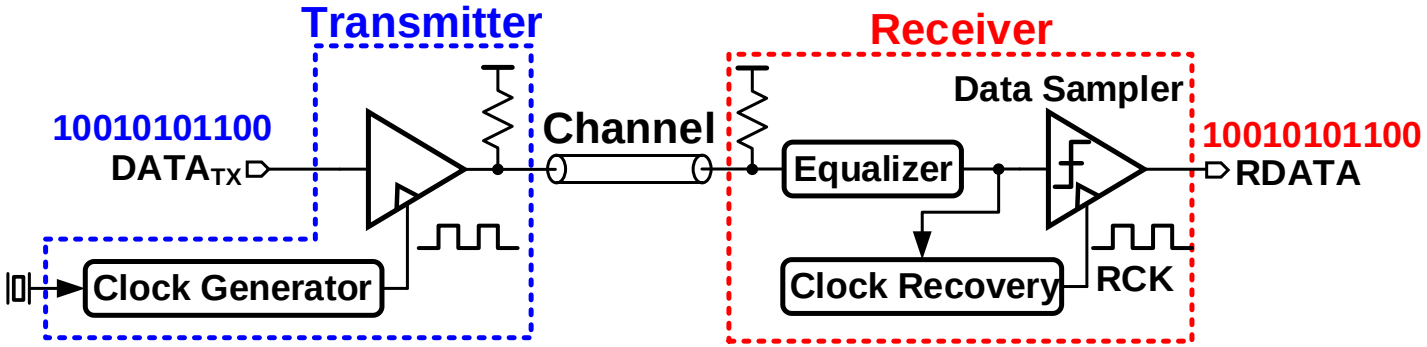
Chip-to-chip
Electrical link



Optical link

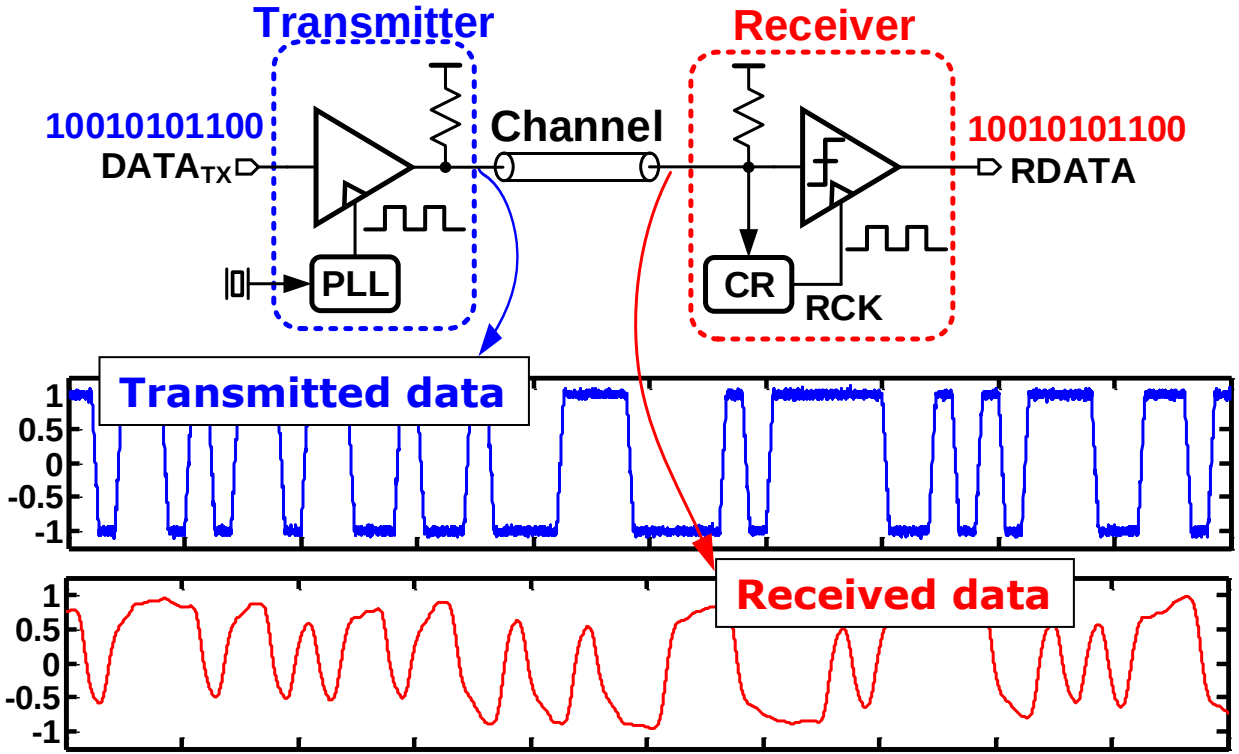


Serial Link Components

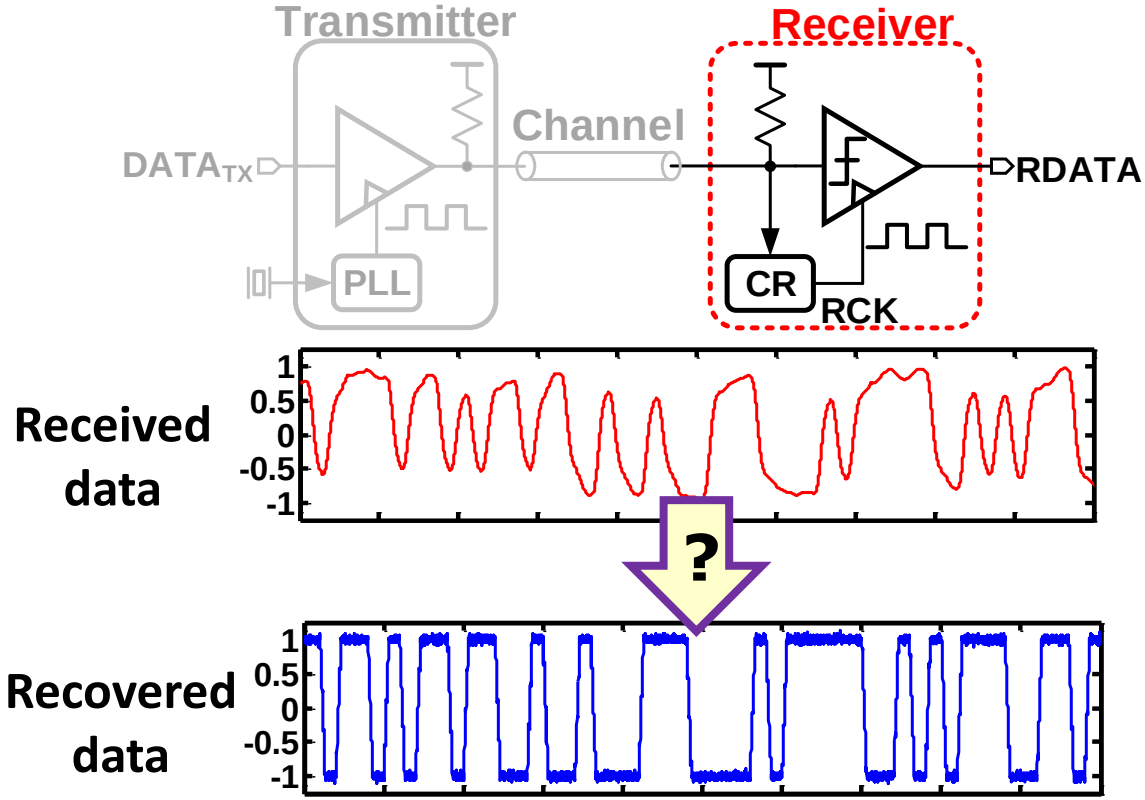


- Transmitter
- Channel
- Receiver
- Serial links with embedded clock ⇒ RCK is recovered from received data
- Clock Recovery (CR) + Data sampler = CDR

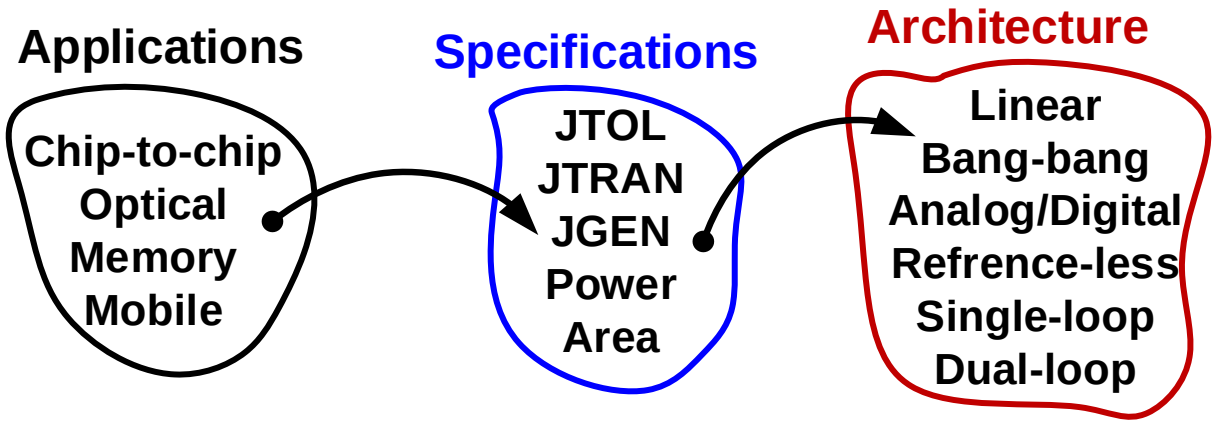
Serial Link Waveforms



Clock and Data Recovery



Goals



- Map application requirements to CDR specifications
- Optimal architecture choice based on CDR specifications
  - Exposure to different CDR architectures
  - Develop intuition for design tradeoffs
  - Awareness to practical considerations

Overview

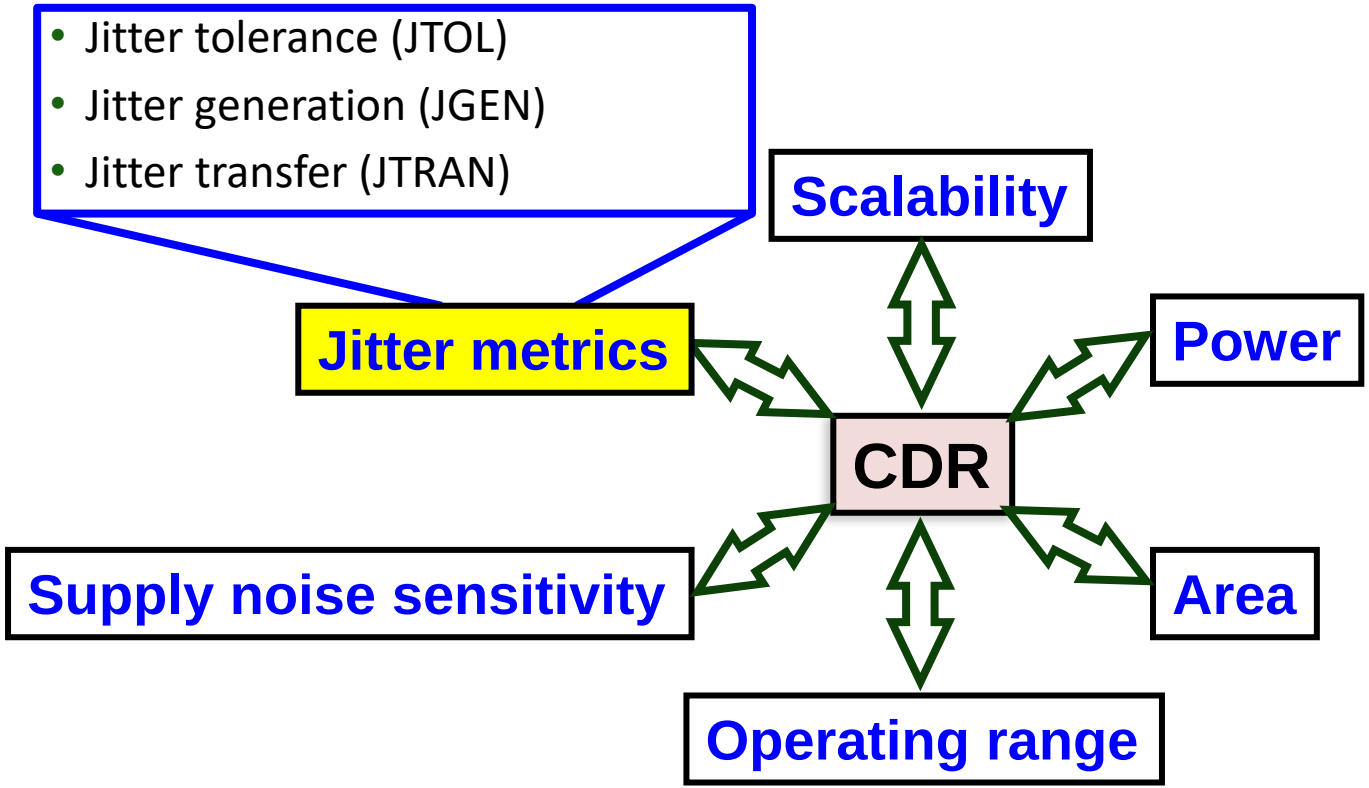
- Performance metrics

- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid

- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables

- Frequency detectors

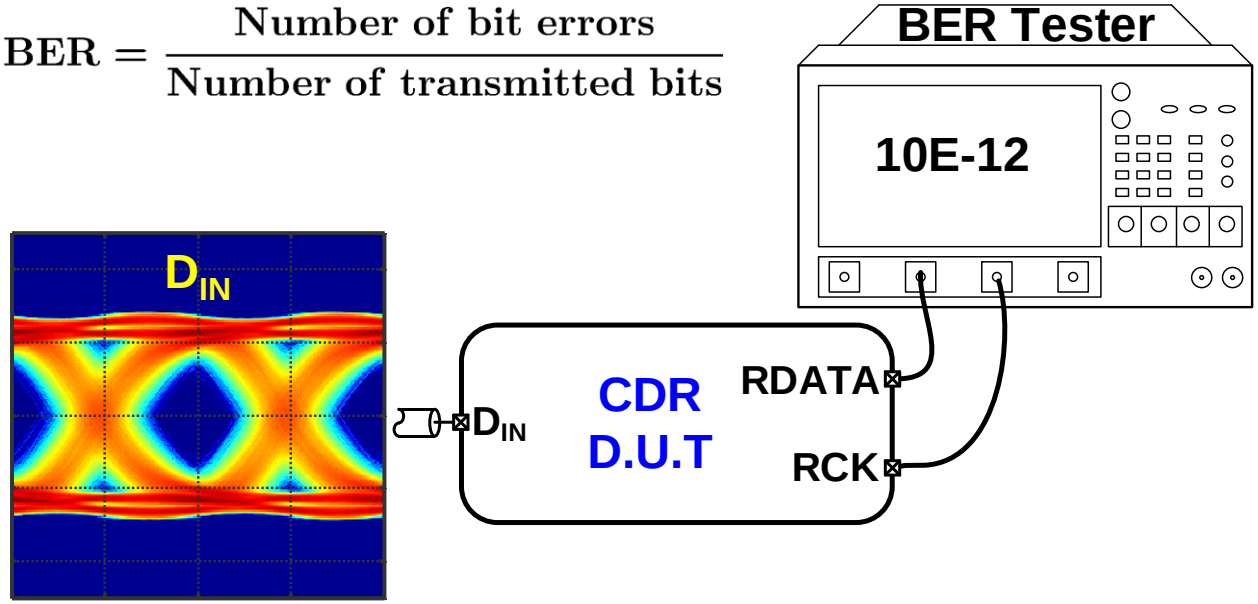
CDR Performance Metrics



Jitter Tolerance (JTOL)

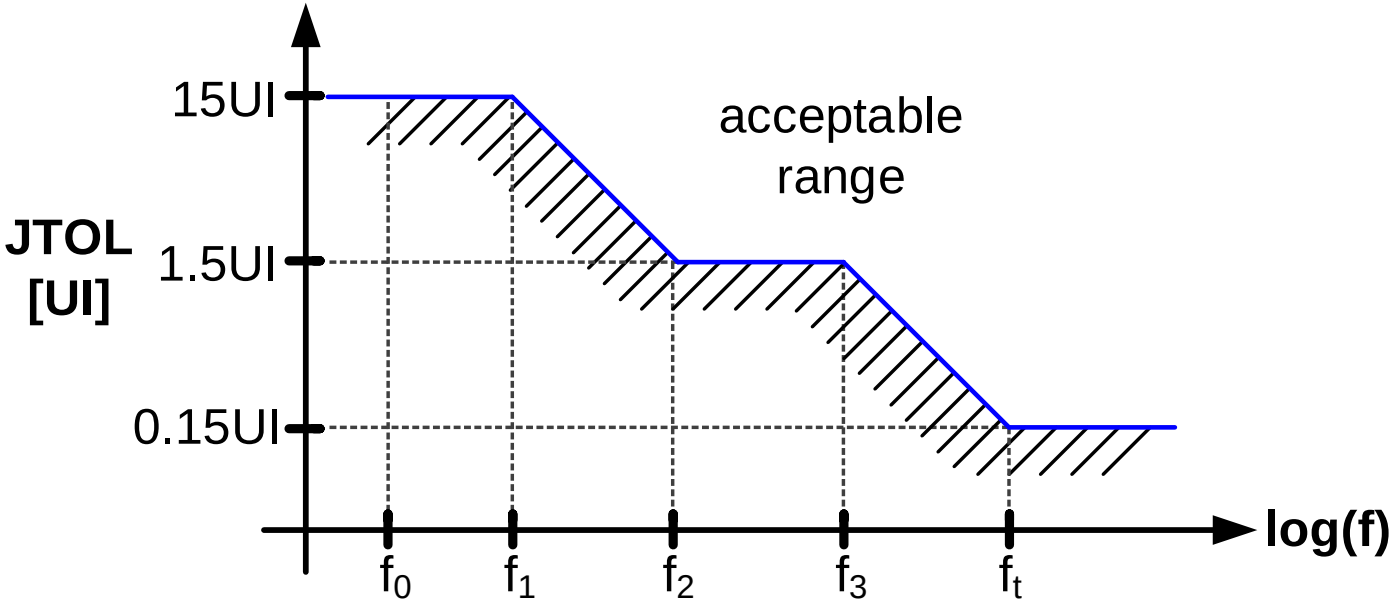
- Maximum tolerable peak-to-peak sinusoidal input jitter for a given BER

$$\text{BER} = \frac{\text{Number of bit errors}}{\text{Number of transmitted bits}}$$



- JTOL varies with frequency of the sinusoidal input

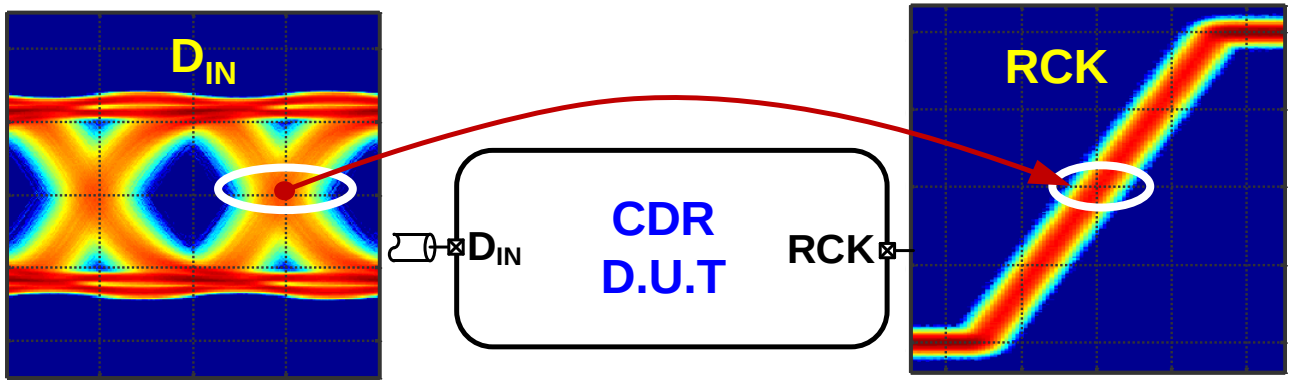
JTOL Mask



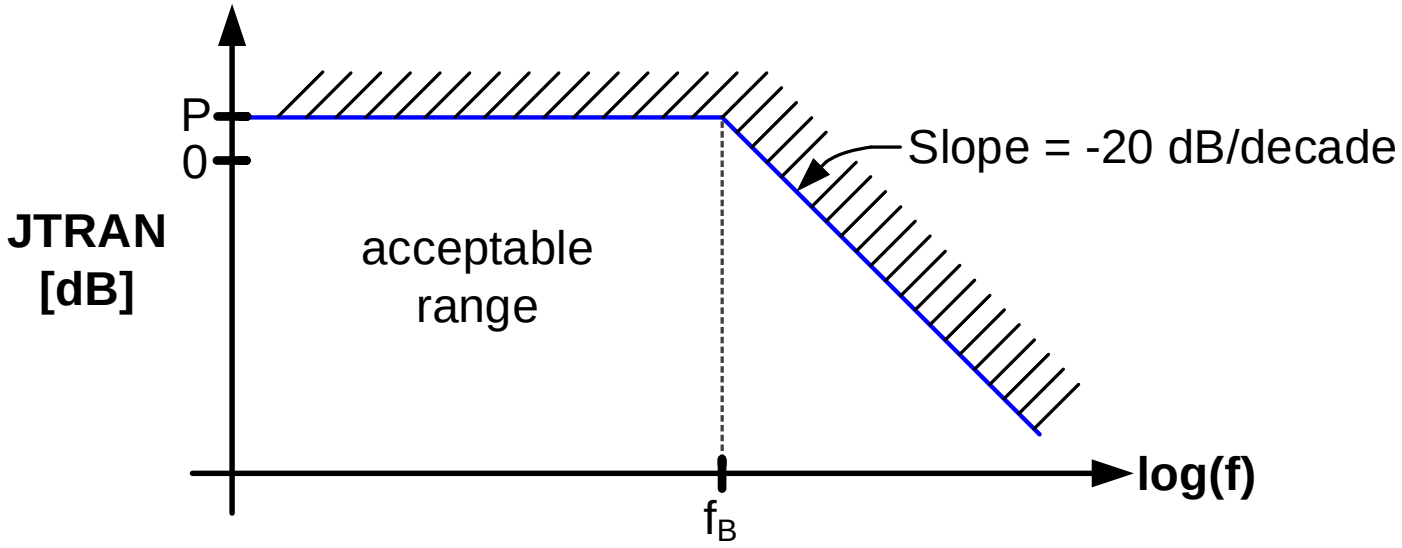
- Increase data input sinusoidal jitter until BER exceeds target

Jitter Transfer (JTRAN)

- Amount of jitter attenuation provided by CDR



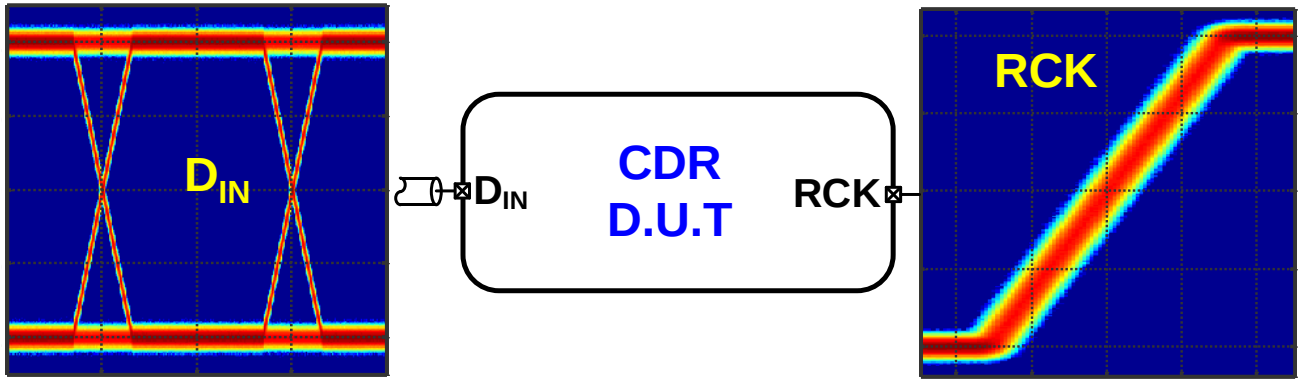
JTRAN Mask



- Modulate data input with sinusoidal jitter & measure resulting output jitter

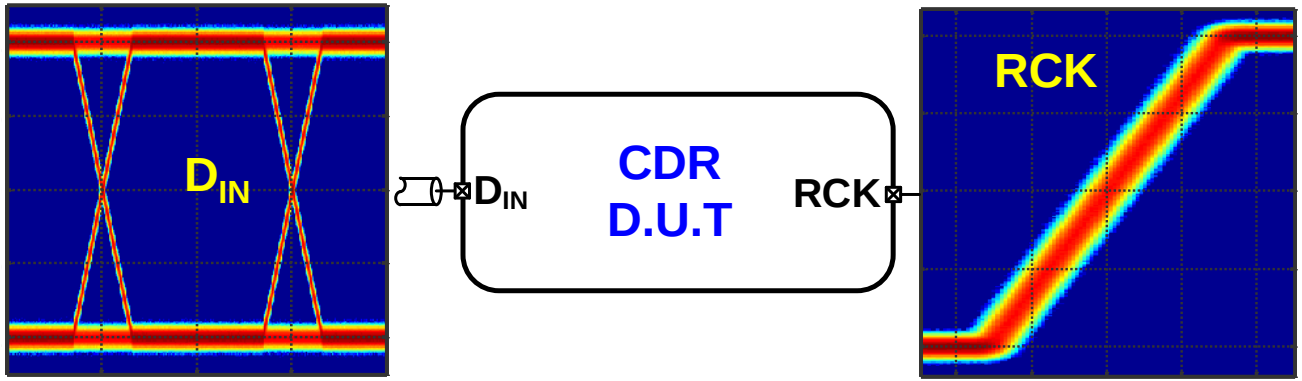
Jitter Generation (JGEN)

- Amount of output jitter when fed with clean data



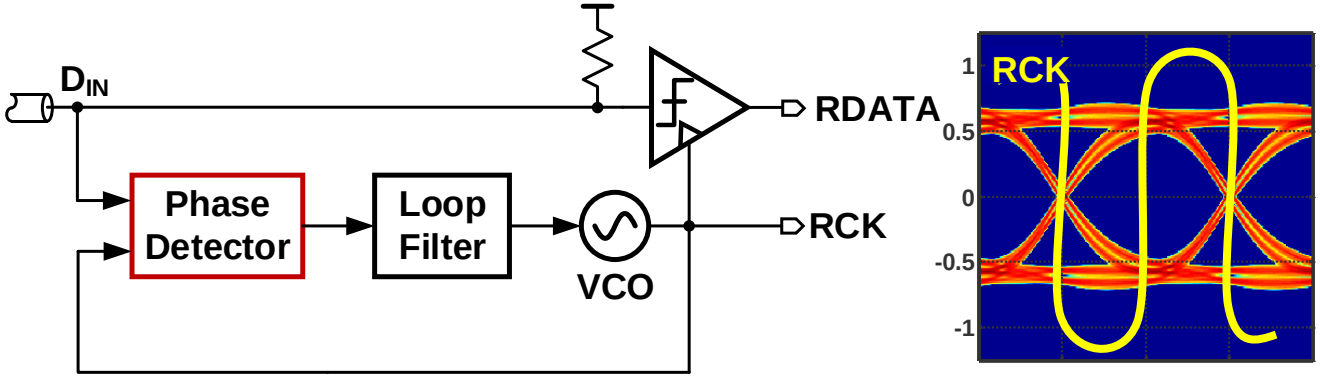
Jitter Generation (JGEN)

- Amount of output jitter when fed with clean data



Need: Design CDR for given JTOL corner frequency, JTRAN BW, and JGEN

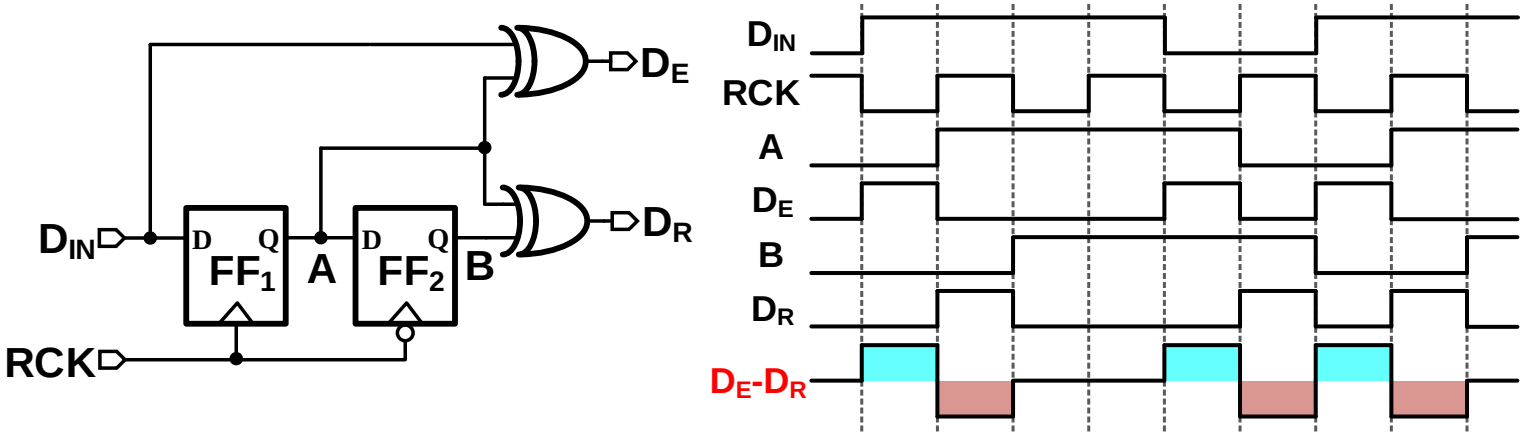
Phase Locked Loop based CDR



- Building blocks similar to a PLL
- Phase detector should tolerate missing transitions

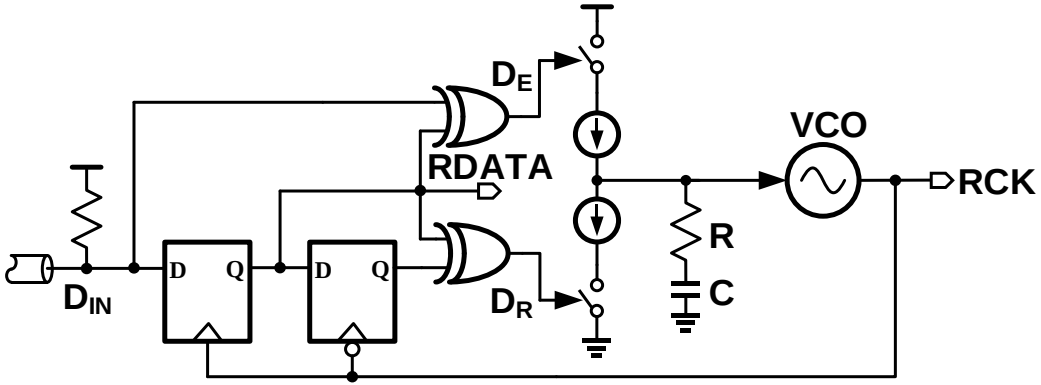
- Negative edge of recovered clock locks to data edge
- Positive edge samples data in the middle of the eye

Linear (Hogge) Phase Detector[1]



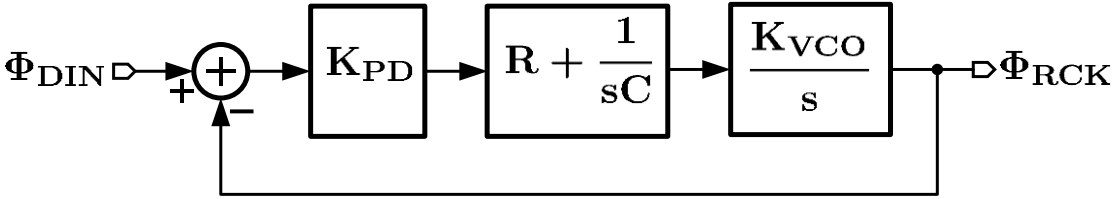
- Error output (D_E-D_R) is difference of 2 pulses
  - Pulse width of D_E is proportional to phase error
  - Pulse width of D_R is fixed and is equal to $T_{RCK}/2$
- Area under D_E-D_R is proportional to phase error
  - Area is zero when RCK is aligned with D_{IN}

CDR Using Hogge Phase Detector



- Type-II response
  - 2 integrators – one in the loop filter and the other is VCO
- Zero static phase offset (ideally)
  - CP output should be zero in steady state
  - Implies input phase error = 0

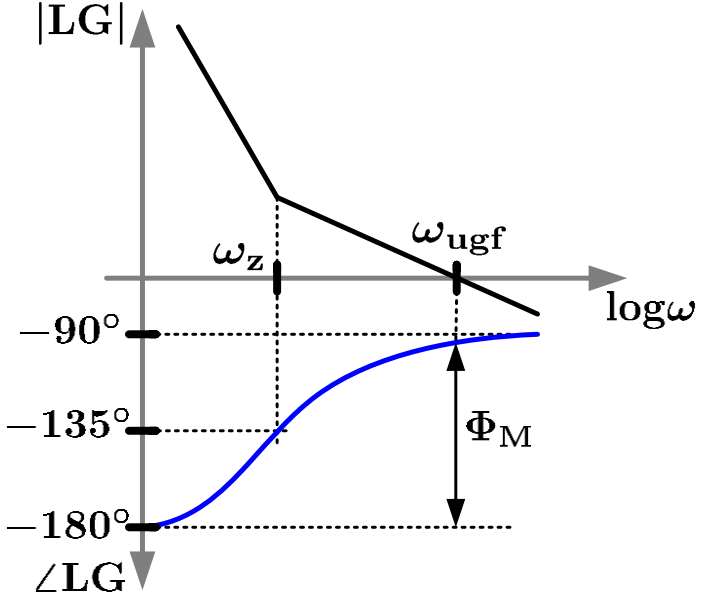
Choosing Loop Parameters



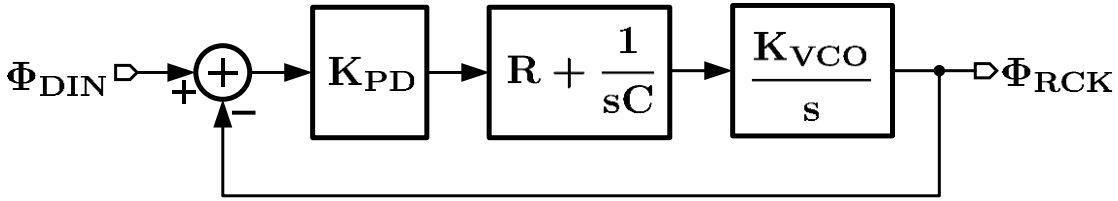
$$LG(s) = K_{PD} \cdot \left(R + \frac{1}{sC}\right) \cdot \frac{K_{VCO}}{s}$$

$$\omega_z = \frac{1}{RC},\ \omega_{p1} = 0,\ \omega_{p2} = 0$$

$$\Phi_M = \arctan\left(\frac{\omega_{ugf}}{\omega_z}\right)$$



Jitter Transfer Function (JTRAN)



$$H_{JTRAN}(s) = \frac{\Phi_{RCK}(s)}{\Phi_{DIN}(s)}$$

$$= \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

$$\equiv \frac{1 + s/\omega_z}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

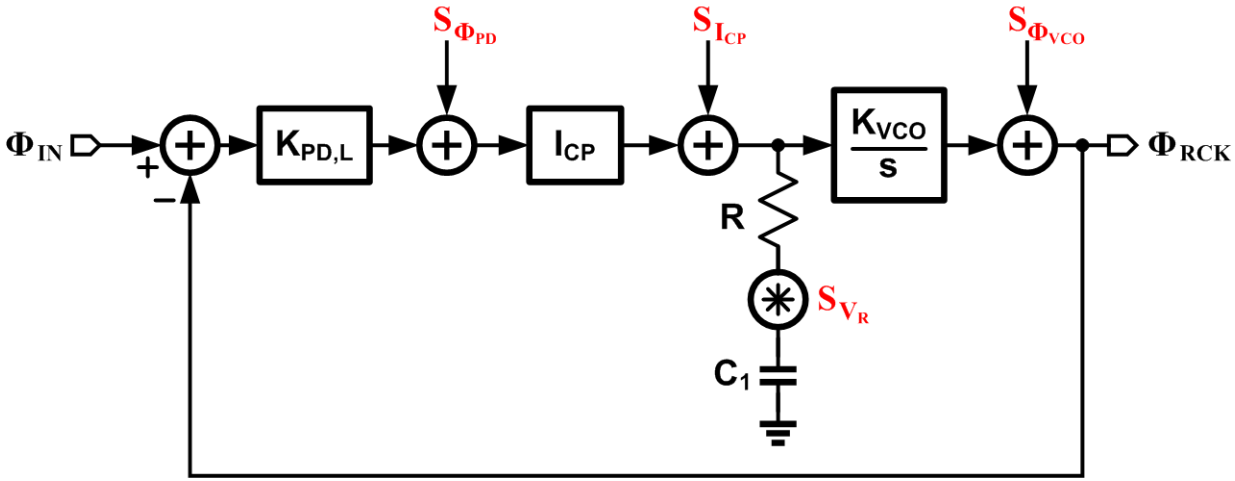
$$\omega_z = 1/RC$$

$$\omega_{PL} \approx 1/RC$$

$$\omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$$

JTRAN BW $= \omega_{-3dB} \approx \omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$

Phase Noise Analysis of Linear CDR (I)



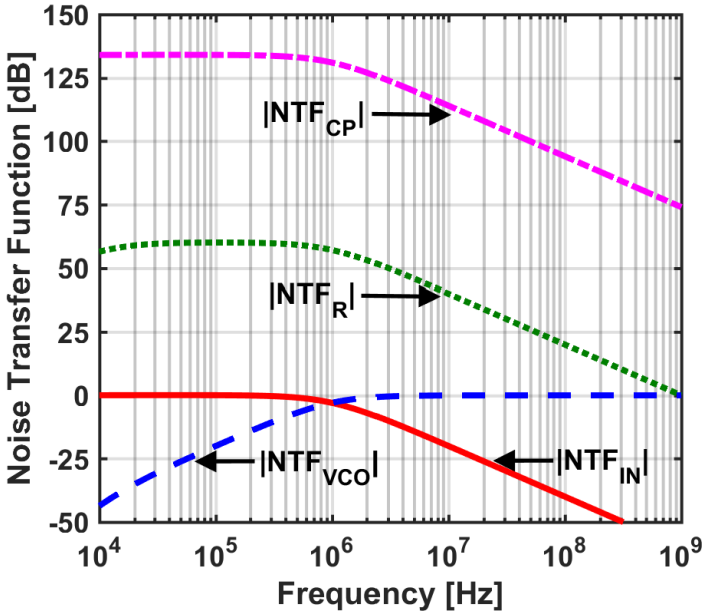
$S_{\Phi_{PD}}$: PD's noise PSD
$S_{I_{CP}}$: Charge-pump's noise PSD
S_{V_R} : Resistor's noise PSD
$S_{\Phi_{VCO}}$: VCO's noise PSD

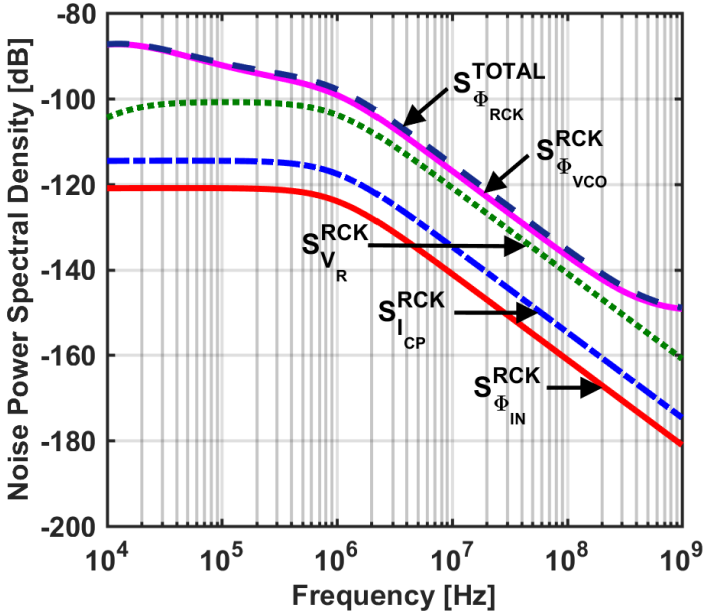
- $NTF_{IN} = \frac{LG}{1+LG}$
- $NTF_{PD} = \frac{1}{K_{PD,L}} \times \frac{LG}{1+LG}$
- $NTF_{CP} = \frac{1}{K_{PD,L}I_{CP}} \times \frac{LG}{1+LG}$
- $NTF_{R} = \frac{K_{VCO}}{s} \times \frac{1}{1+LG}$
- $NTF_{VCO} = \frac{1}{1+LG}$
- $JGEN = \frac{T_{RCK}}{2\pi}\sqrt{\int_0^\infty S_{\Phi_{RCK}}^{Total}\,df}$

where $S_{\Phi_{RCK}}^{Total} = \sum S_i \times |NTF_i|^2$

S_i : i^{th} noise source

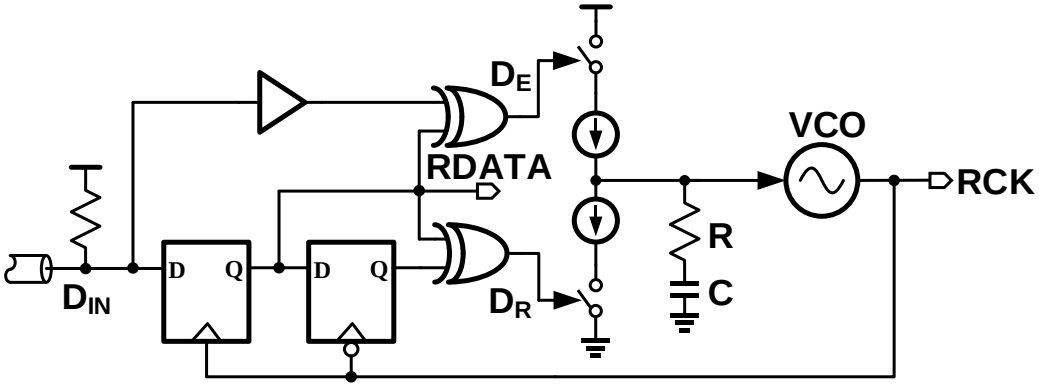
Phase Noise Analysis of Linear CDR (II)





- Design Example:
  - DR = 2.5Gb/s, f_{RCK} = 2.5GHz, K_{VCO} = 2π Grad/s/V, Phase margin = 85°, JTRAN BW < 1MHz
  - I_{CP} = 1.26 µA, R = 5 kΩ, C_1 = 2.76 nF
  - VCO's noise dominates in low JTRAN BW designs

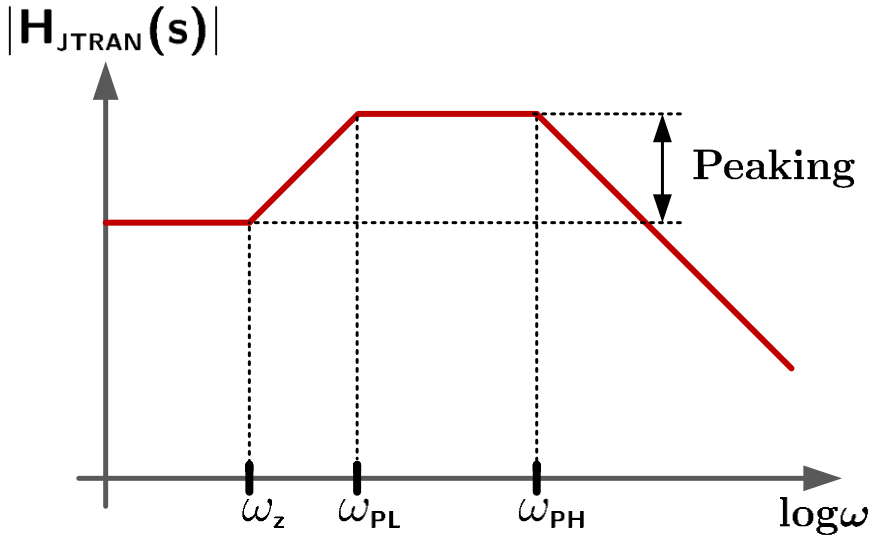
Linear CDR Drawbacks



- JTRAN peaking vs large loop filter capacitor
- Coupled JTRAN and JTOL
- Hogge PD non-idealities

Jitter Peaking[2]

- Zero in feed-forward path → inevitable peaking



$$H_{JTRAN} = \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

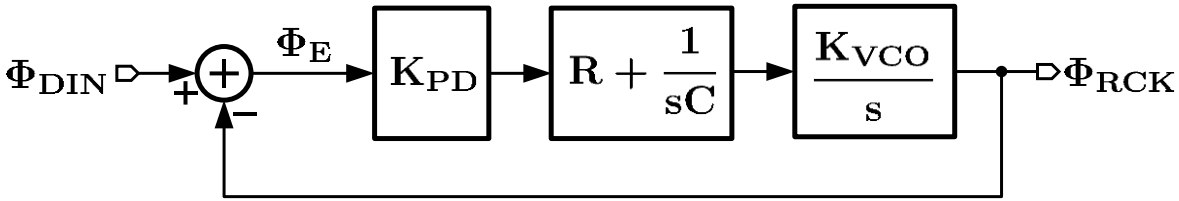
$$\omega_z = 1/RC$$

$$\omega_{PL} \approx 1/RC$$

$$\omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$$

$$\text{Jitter Peaking [dB]} \approx \frac{8.686}{K_{VCO}K_{PD}CR^2} \approx \frac{8.686}{\omega_{-3dB}CR} = \frac{8.686\omega_z}{\omega_{-3dB}}$$

Jitter Tracking



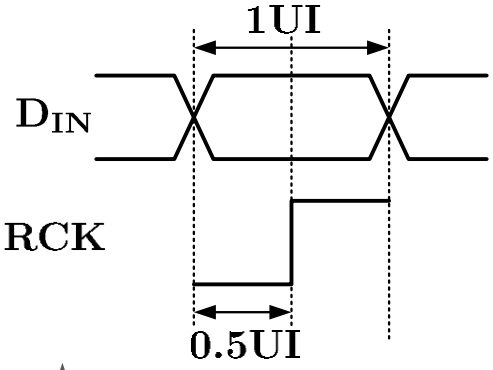
$$H_{JTRACK}(s) = \frac{\Phi_E(s)}{\Phi_{DIN}(s)} = \frac{1}{1 + LG(s)}$$

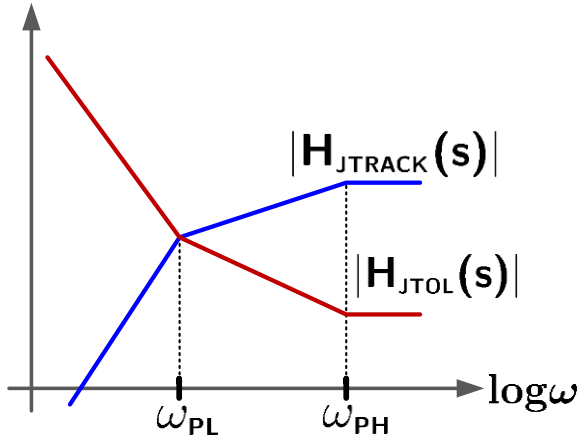
$$= \frac{s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

$$\equiv \frac{s^2/\omega_{PL}\omega_{PH}}{(1 + s/\omega_{PL})(1 + s/\omega_{PH})}$$

$$\text{JTRACK BW} = \omega_{-3dB} \approx \omega_{PH} \approx K_{VCO} \cdot K_{PD} \cdot R$$

Jitter Tolerance (JTOL)





$$|\Phi_E| < 0.5\,\mathrm{UI}$$

$$\Phi_{DIN} \times H_{JTRACK}(s) < 0.5\,\mathrm{UI}$$

$$\Longrightarrow \Phi_{DIN} < \frac{0.5\,\mathrm{UI}}{H_{JTRACK}(s)}$$

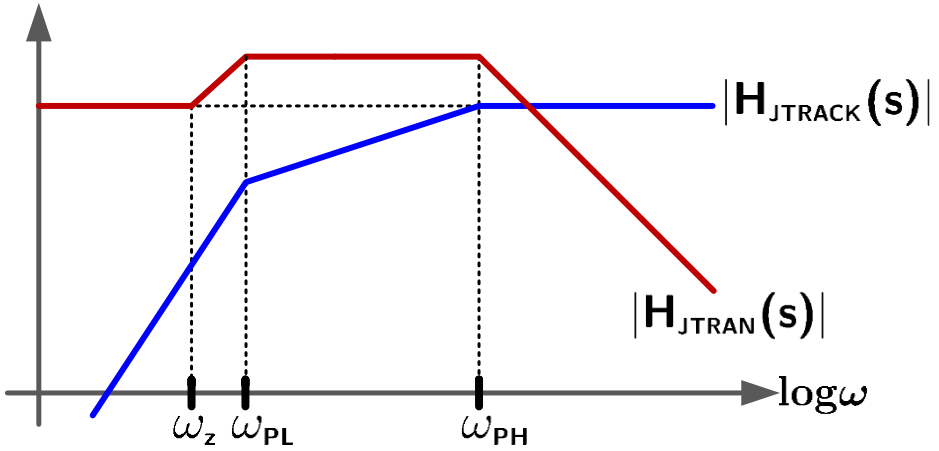
$$H_{JTOL}(s) = \frac{0.5}{H_{JTRACK}(s)}$$

$$H_{JTOL}(s) = \frac{0.5\,(1+s/\omega_{PL})\,(1+s/\omega_{PH})}{s^2/\omega_{PL}\omega_{PH}}$$

Coupled JTRAN/JTOL Behavior

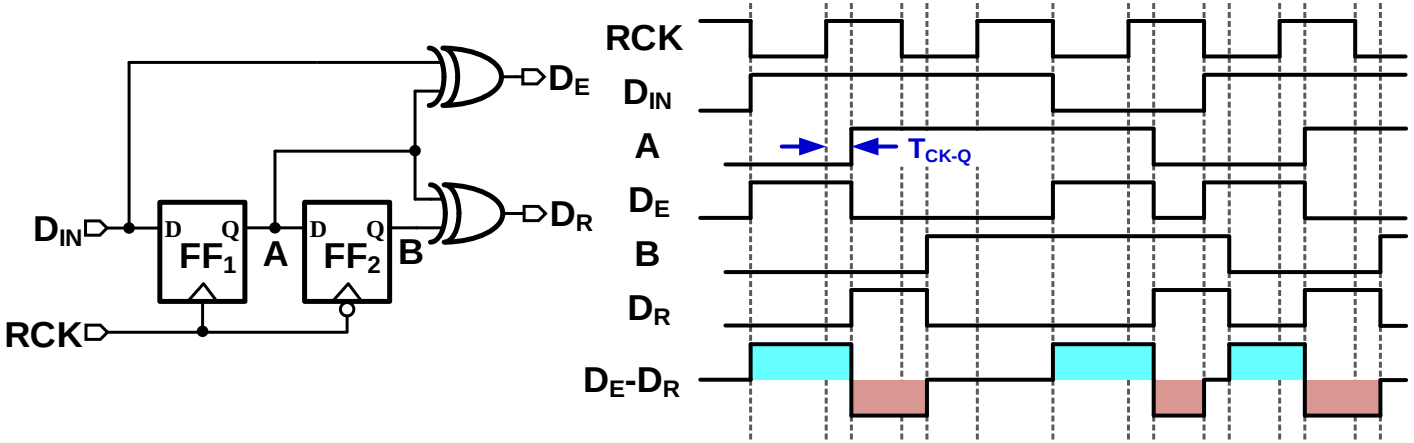
$$H_{JTRAN}(s) = \frac{1 + sRC}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$

$$H_{JTRACK}(s) = \frac{s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}{1 + sRC + s^2 \cdot \frac{C}{K_{VCO}K_{PD}}}$$



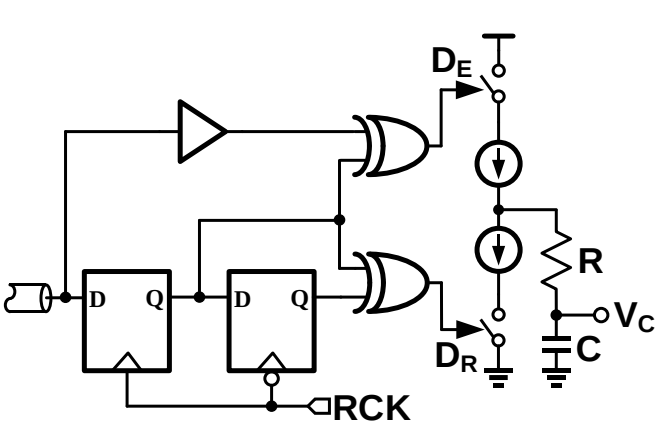
- Both JTRAN and JTOL are governed by ω_{PH}

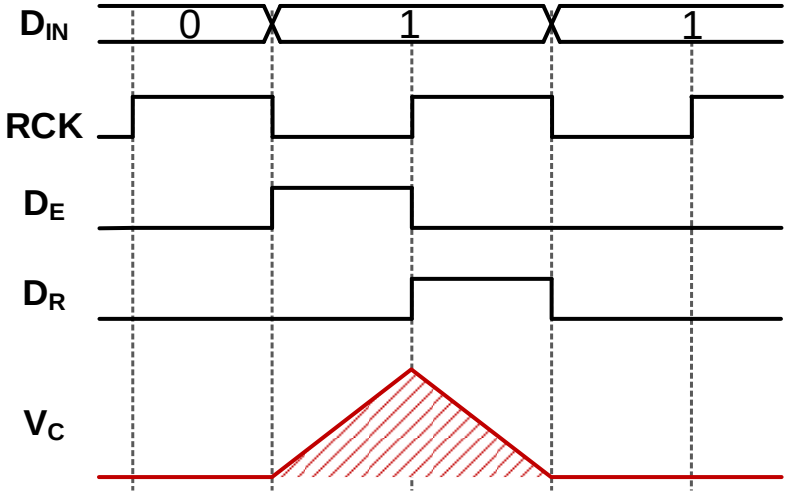
Hogge PD Non-idealities: Offset [2]



- FF_1 clock-to-Q delay introduces phase offset

Hogge PD Non-idealities: DDJ[2]

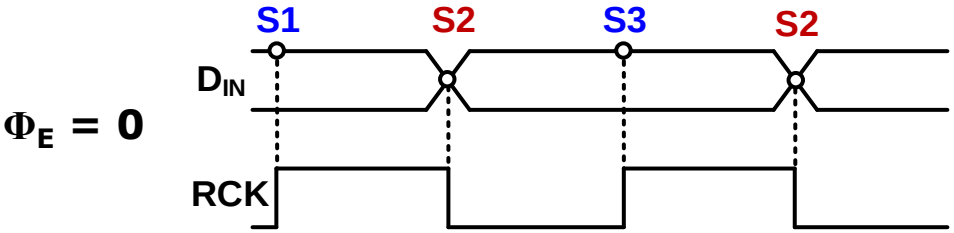




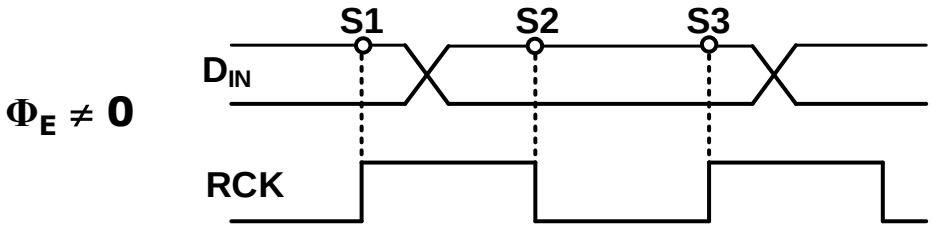
- D_E/D_R pulses not aligned in time
  - "Tri-wave" on V_C causes Data Dependent Jitter (DDJ)

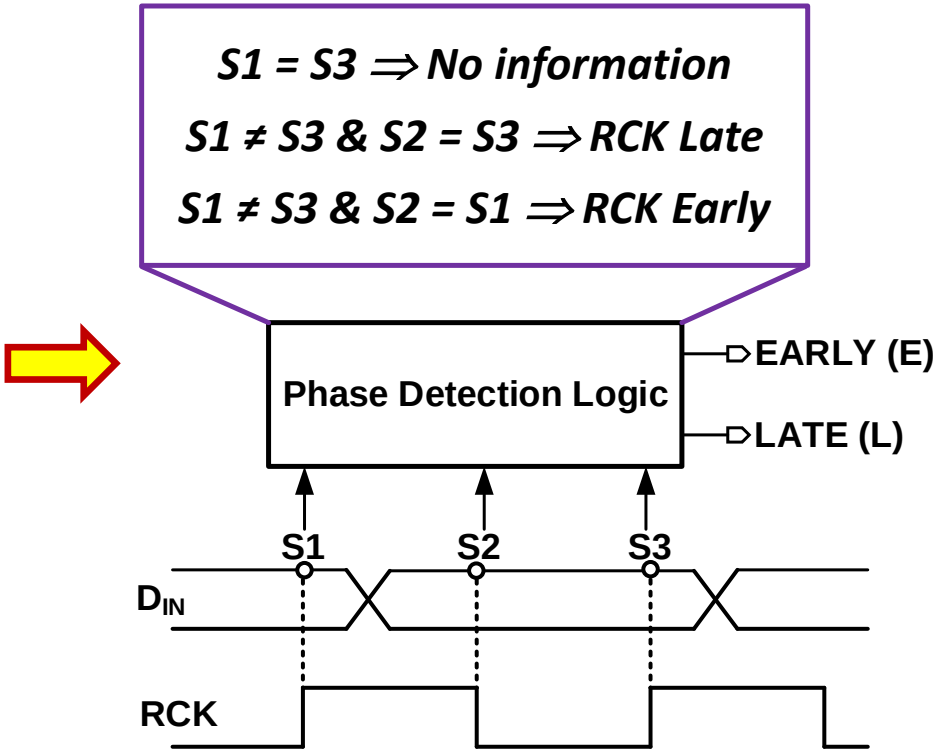
- See [2] for modified Hogge PD to mitigate offset and DDJ

Bang-Bang Phase Detector (BBPD)[3]

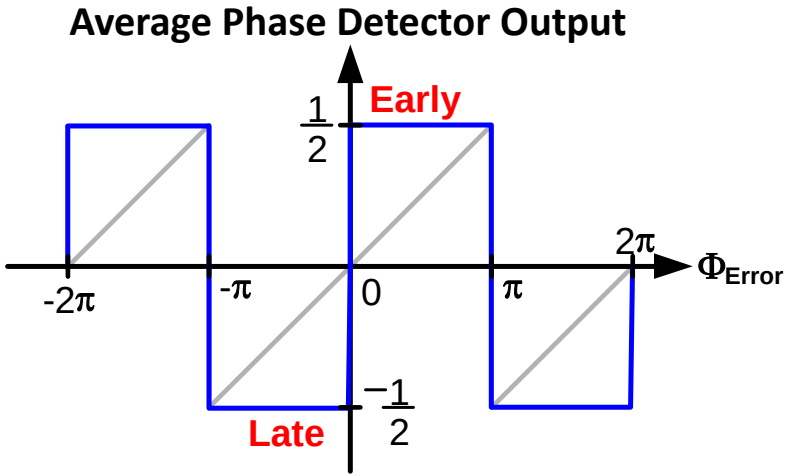


S1 and S3 are data samples S2 is edge sample





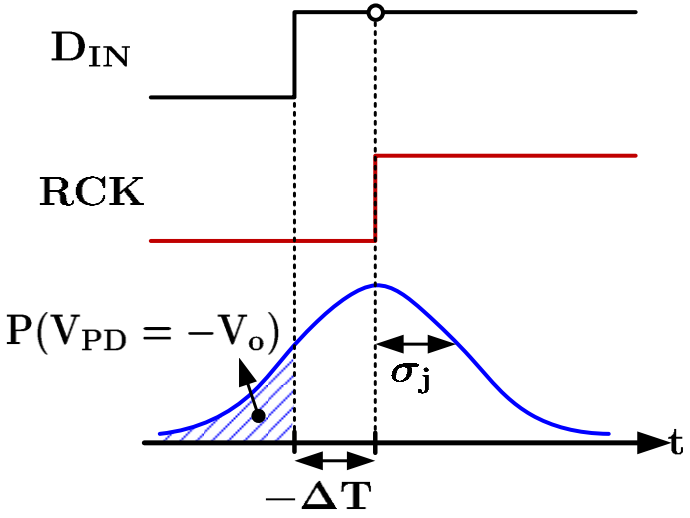
BBPD Characteristics: w/o Jitter



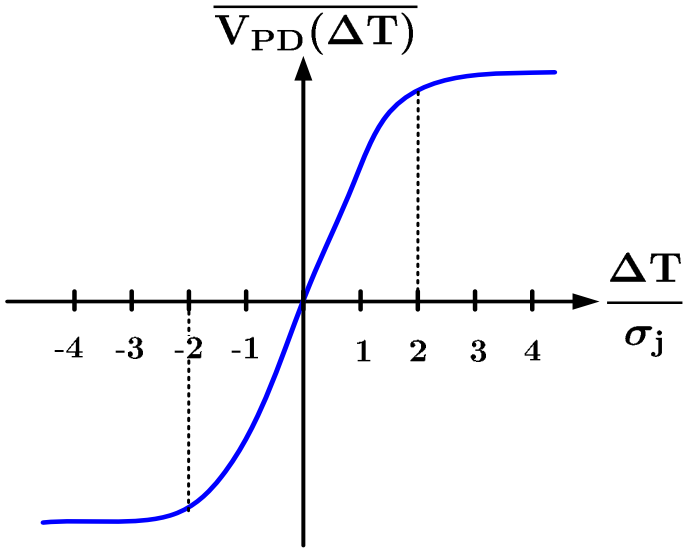
$$\text{Useful range} : \pm\pi$$

$$\text{Gain } K_{PD}|_{\Delta T=0} = \infty$$

BBPD Characteristics: w/ Jitter[4]



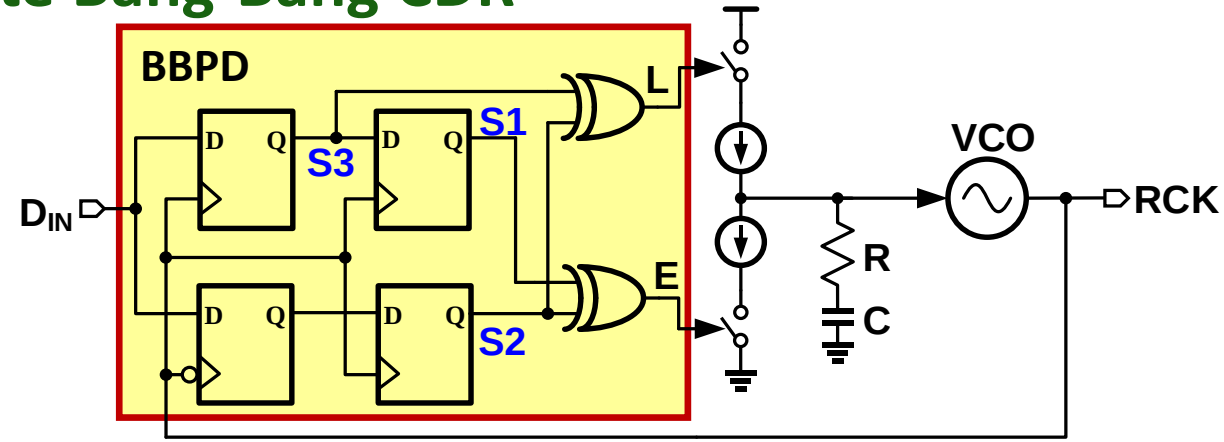
$$\overline{V_{PD}(\Delta T)} = -V_o \cdot P(V_{PD} = -V_o) + V_o \cdot P(V_{PD} = V_o)$$



$$\overline{V_{PD}(\Delta T)} = \frac{2V_o}{\sqrt{2\pi}} \int_0^{\Delta T/\sigma_j} e^{-y^2} dy$$

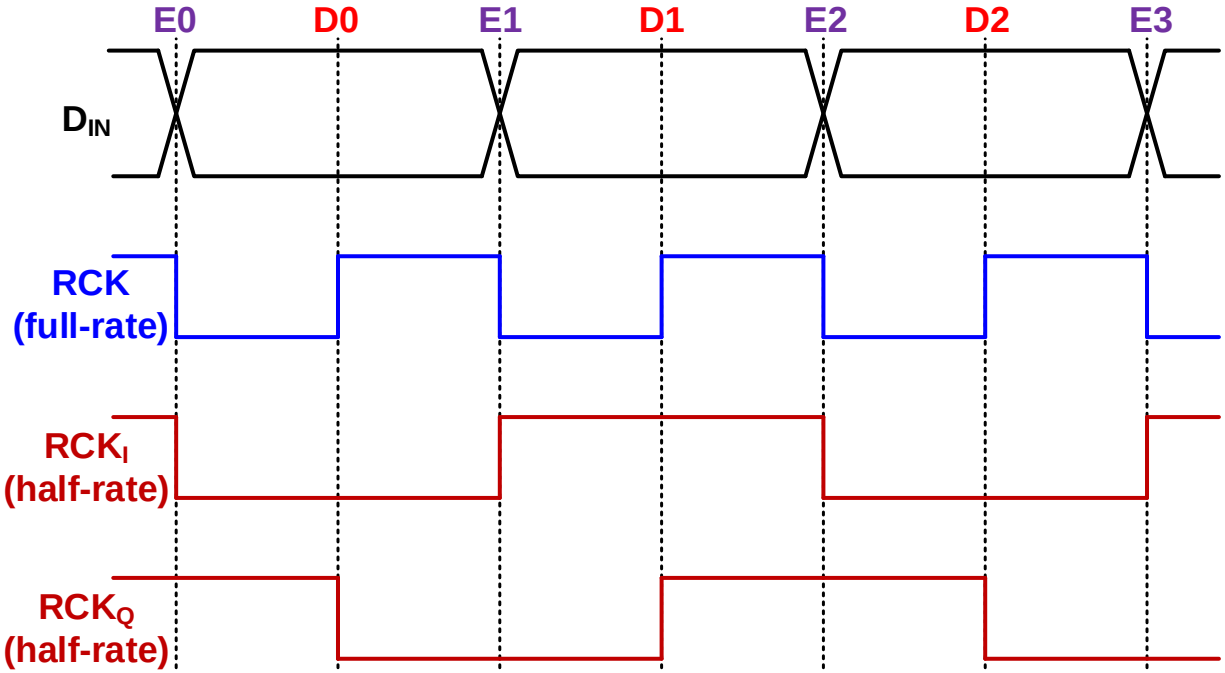
$$K_{PD} = \frac{d\overline{V_{PD}(\Delta T)}}{d\Delta T} = \frac{2V_o}{\sqrt{2\pi}\sigma_j} e^{\left(-\frac{\Delta T}{\sqrt{2}\sigma_j}\right)^2}$$

Full-rate Bang-Bang CDR

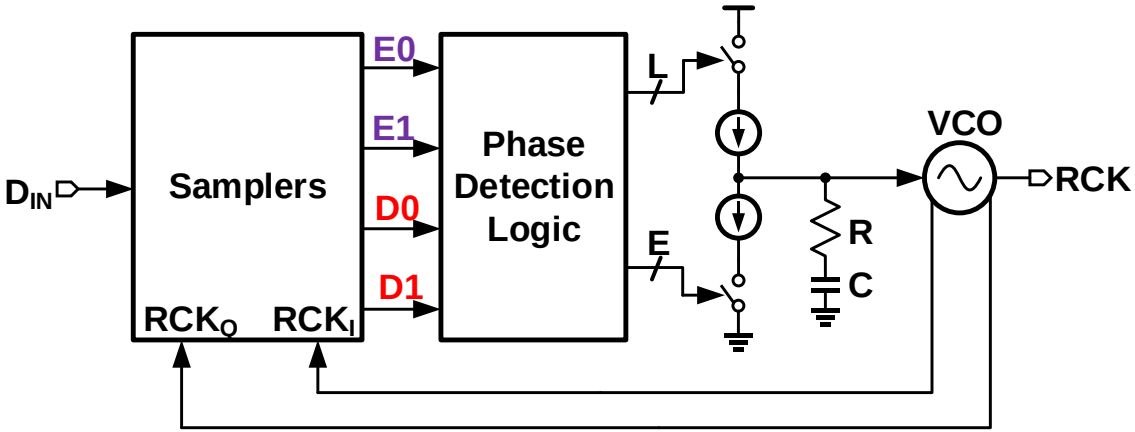


- Type-II response
- Near-zero static phase offset
- Insensitive to charge-pump non-idealities
- VCO & PD operate at full-rate or data rate ($F_{VCO} = F_{DIN}$)
  - Could become a speed bottleneck
  - Solution: Half-rate bang-bang CDR

Half-rate CDR Waveforms



Half-Rate Bang-Bang CDR



- Topology same as full-rate architecture
- Requires quadrature VCO
- Lower loop update rate → higher loop latency
- Non-linear loop dynamics due to non-linear BBPD's gain. To ensure stability[5]

$$\text{Damping factor } \zeta = \frac{\Delta\Phi_{RCK} \text{ due to prop. path}}{\Delta\Phi_{RCK} \text{ due to integ. path}} = \frac{2RC}{T_{UPDATE}} \gg 1$$

Bang-Bang CDR Drawbacks

- Coupled JTRAN and JTOL
- Jitter peaking
- Large loop filter area

} **Similar to linear CDR**

- **JGEN caused by limit cycles due to BBPD's behavior**

- **JTRAN dependence on input jitter**

$$\text{JTRAN BW} \approx K_{PD} \cdot K_{P} \cdot K_{VCO}$$

$$\text{Gain } K_{PD}|_{\Delta T=0} = \frac{2V_o}{\sqrt{2\pi}\sigma_j} \implies \text{JTRAN BW} \propto \frac{1}{\sigma_j}$$

Overview

- Performance metrics

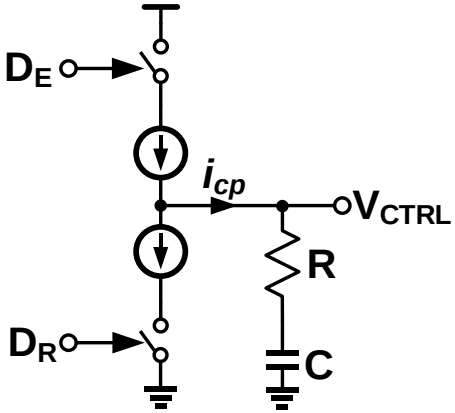
- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid

- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables

- Frequency detectors

Eliminating Loop Filter Capacitor

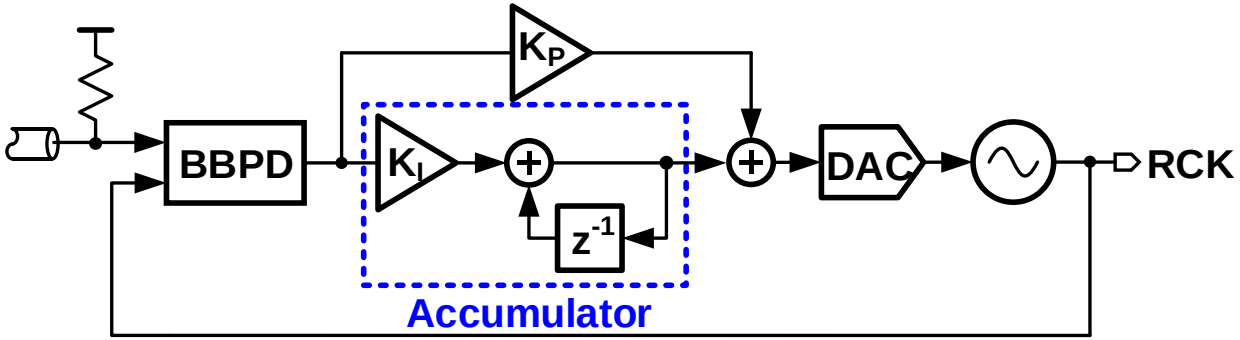
- Map CP + LF into digital domain directly

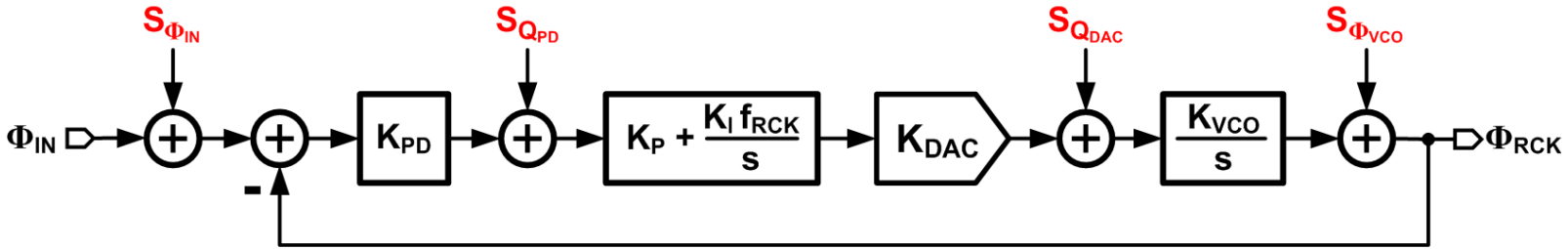


$$i_{cp}\mathrm{R} + \frac{i_{cp}}{\mathrm{C}s} \Rightarrow i_{cp}\mathrm{R} + \frac{i_{cp}\mathrm{T}}{\mathrm{C}}\frac{z^{-1}}{1-z^{-1}}$$

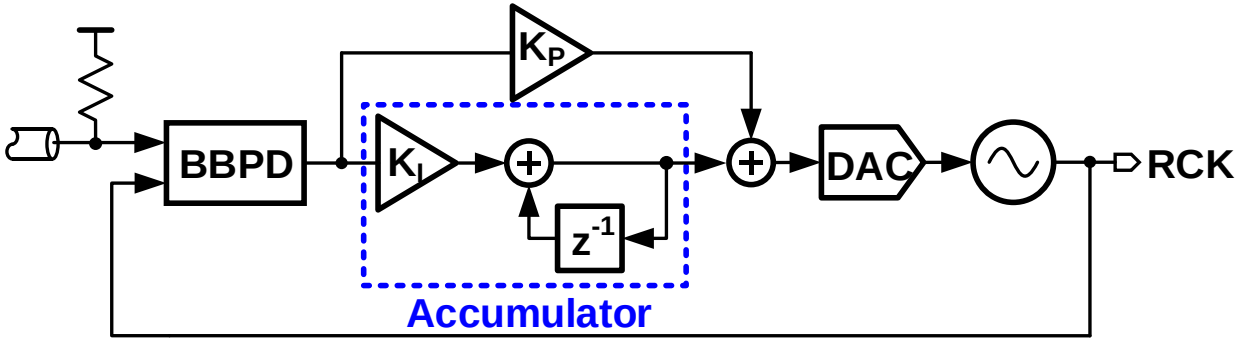
- Digital accumulator replaces loop filter capacitor
  - Large time constant with small area
  - Infinite DC gain → ideal Type-II behavior
  - PVT insensitive
  - Easy to reconfigure for loop dynamics control

Simple Digital CDR[6]





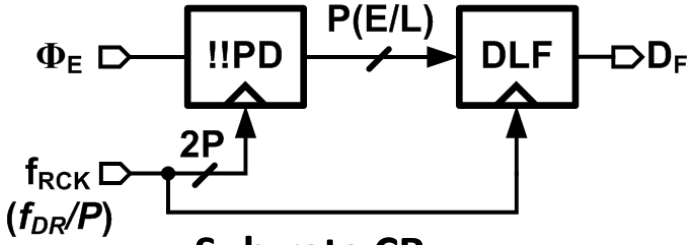
Simple Digital CDR[6]



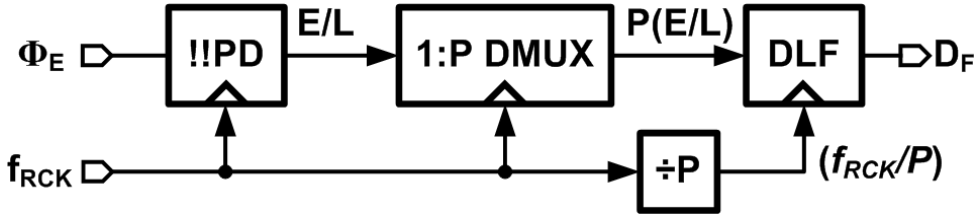
- Loop filter must operate at data rate

- **Need:**
  - Wide operand high-speed adders
  - High speed/resolution **D**igital to **A**nalog **C**onverter (**DAC**)

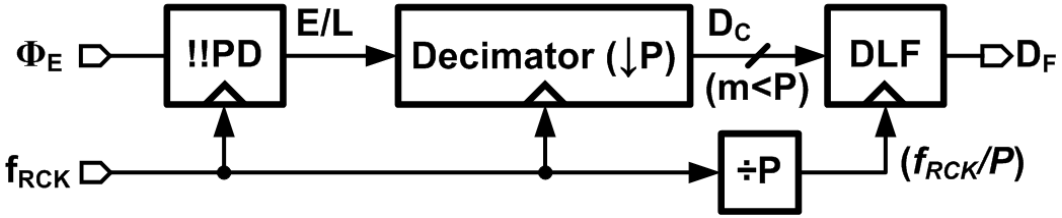
Reducing Speed Requirements (I)



Sub-rate CR



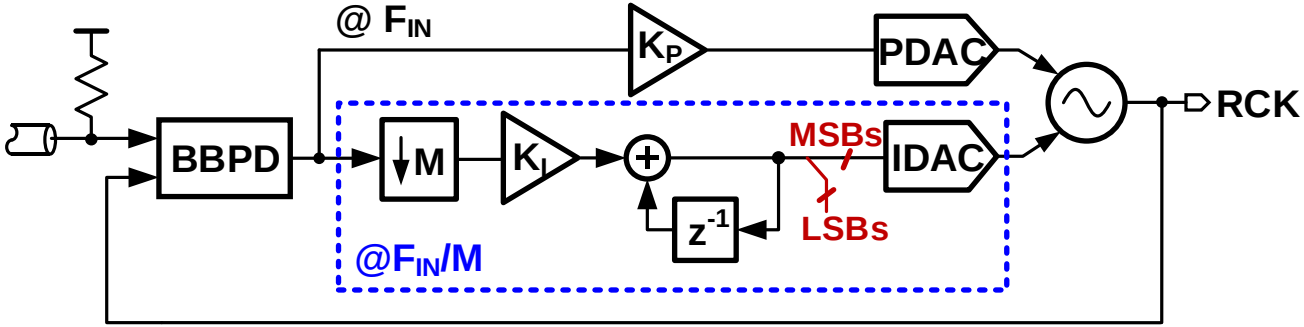
1:P Deserialized E/L Signals



Decimated !!PD's Output

- DLF operates at lower speed, f_{RCK}/P. It delays feedback in the loop
- Increased loop delay adversely affects phase-margin, jitter peaking, & JTOL
- **Observation:** Proportional path dominates jitter

Reducing Speed Requirements (II)



- Fast proportional path
  - Minimize latency → reduce dithering jitter
- High resolution integral path
  - Minimize tracking jitter
- Minimal hardware penalty
  - Needs only 2-level high-speed PDAC
- IDAC implemented using $\Delta\Sigma$ techniques
- Proportional and integral controls summed in VCO

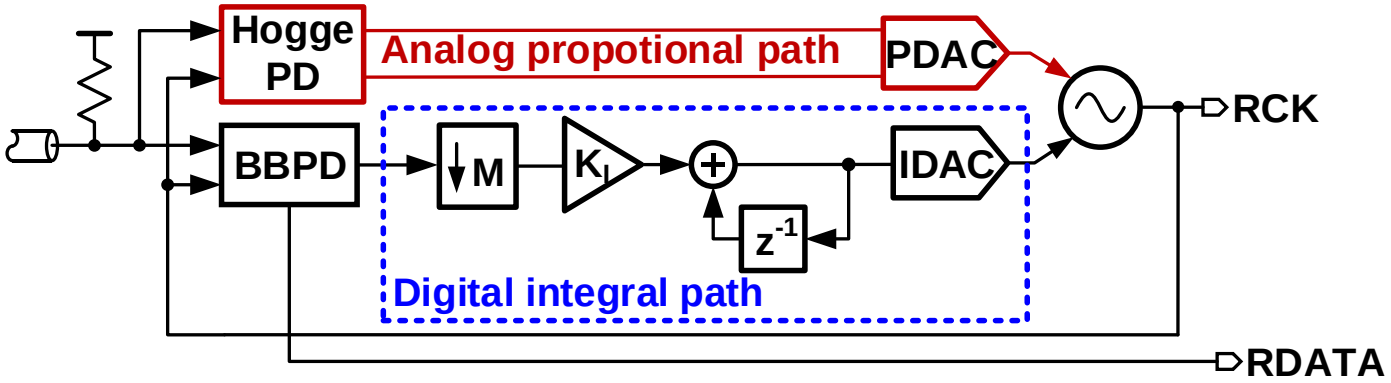
Analog vs. Digital CDRs

- Analog CDR using linear PD
  - Well-controlled loop dynamics
  - PD non-idealities degrade timing margin/BER
  - Large loop filter capacitor
  - Sensitive to Consecutive Identical Digits (CIDs)[7]

- Digital CDR using bang-bang PD
  - Non-linear loop dynamics (JTRAN depends on jitter)
  - Bang-bang PD maximizes timing margin
  - No large capacitor (small area)
  - Sensitive to Consecutive Identical Digits (CIDs)

- Can we combine the advantages?

Hybrid Analog/Digital CDR[8]



- Proportional path sets loop bandwidth (JTRAN)
  - Fixed gain leads to linear loop dynamics
  - Eliminates phase quantization error
- Digital integral path sets steady state
  - Makes it insensitive to linear PD phase offset
  - Accumulator filters BBPD quantization error
  - BBPD's offset causes ripple on the proportional path

Overview

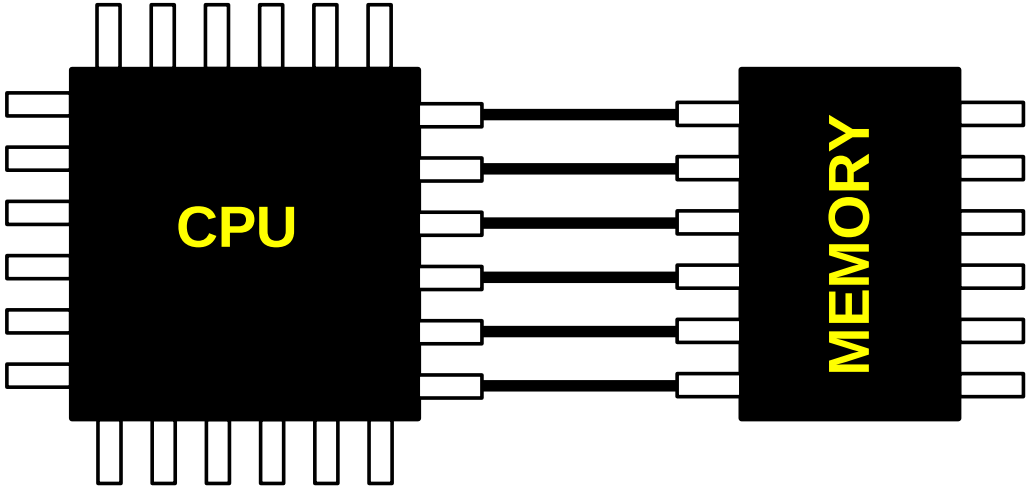
- Performance metrics

- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid

- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables

- Frequency detectors

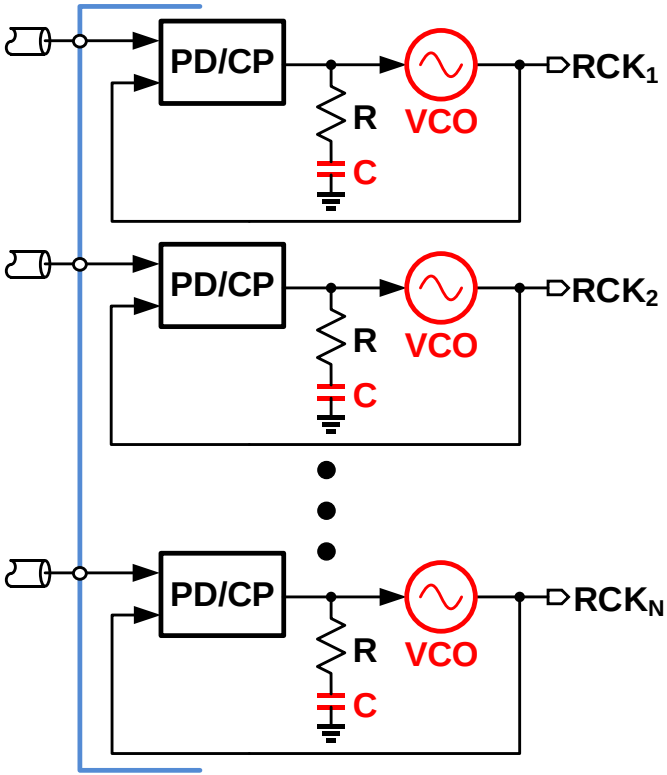
Multi-Lane Chip-to-Chip Links



- Source synchronous clocking is common

- BUT many standards mandate embedded clocking
  - Examples: PCIe, XAUI, SATA, etc.
  - Clock & data recovery is required for each lane of the multi-lane link

Multi-Lane CDR Challenges



- Many VCOs
- VCO's noise dominates low BW CDRs
- Harmonic locking
- Large capacitors & large area

Oscillators in Multi-Lane CDRs

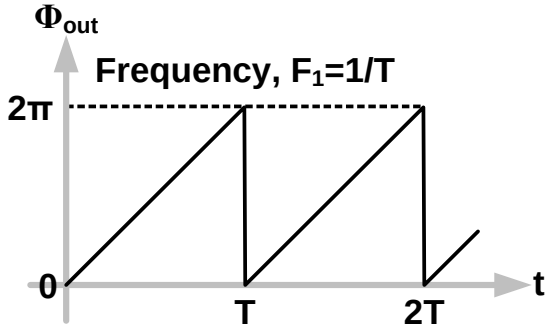
- Oscillator's properties needed in multi-lane CDR
  - Good phase noise performance w/ low o/p jitter
  - Multiple sampling clock phases for sub-rate CDRs
  - Independent & wide frequency tuning range for each lane
  - Lower power consumption
  - Small chip-area

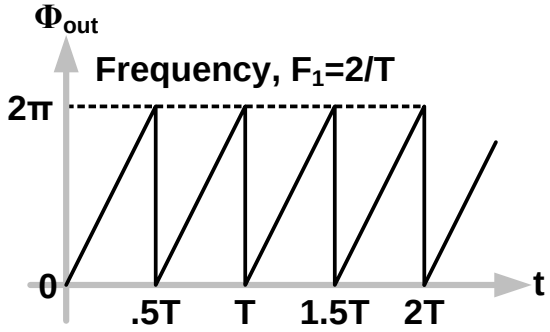
	LC Oscillator	Ring Oscillator
1	Excellent phase noise	Poor phase noise
2	Low power consumption	Large power consumption compared to LC osc.
3	Limited frequency tuning range	Wide frequency tuning range
4	Reduced # of clock phases for sub-rate CDRs	Easily available clock phases for sub-rate CDRs
5	Large chip-area	Small chip-area

Both LC/ring-oscillators are not suited standalone for multi-lane CDRs

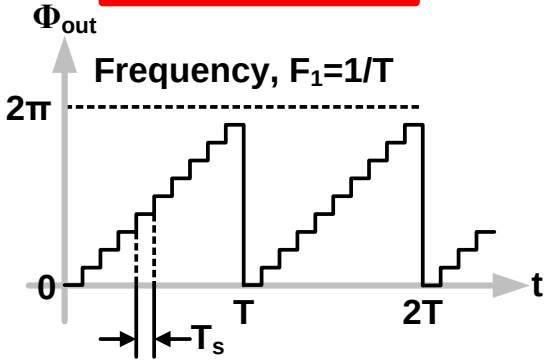
Phase of Analog/Digital Oscillator

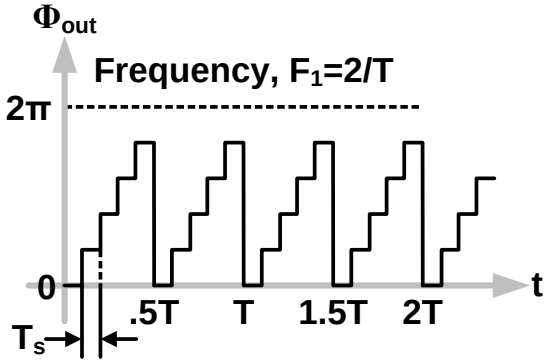
Analog Oscillator





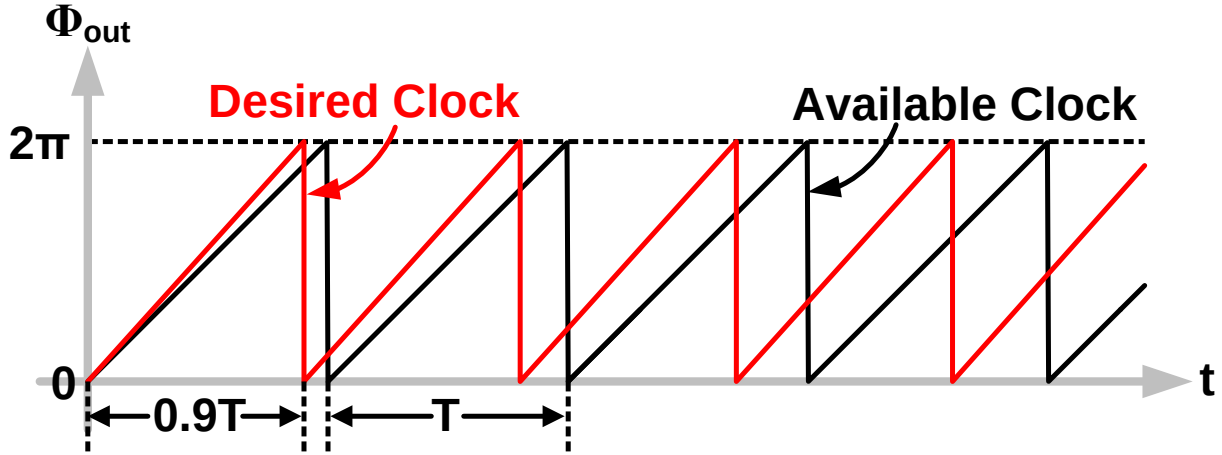
Digital Oscillator





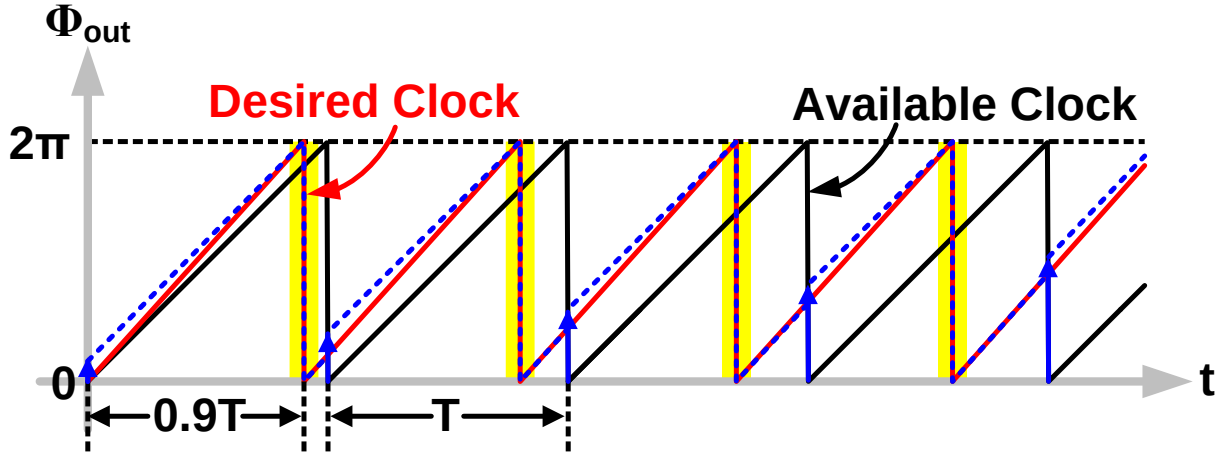
- Multiple digital clocks from
  - Single clock $F_s = 1/T_s$ ($>F_1$)
  - Accumulating phase proportional to o/p frequency

Digital Oscillator Requirements in CDR



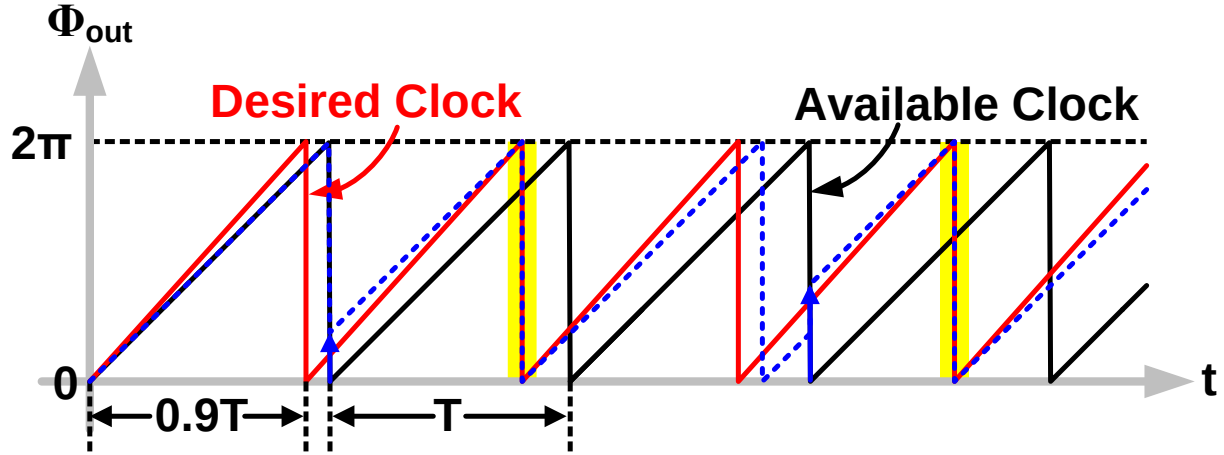
- Available clock frequency, $f_{ava}=1/T$
- Desired clock frequency, $f_{des}=1/0.9T$
- A 2π phase accumulation marks the rising or falling clock edges

Digital Oscillator w/ Desired Transitions



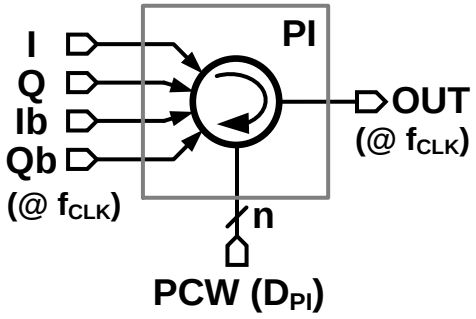
- Add accumulated phase to f_{ava} periodically
- Phase rotators, phase interpolators, etc. are used to add/subtract phase for desired frequency

Limitations of Digital Phase Addition

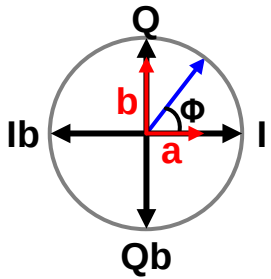


- Minimum phase addition has a lower bound
  - Leads to increased o/p jitter
  - Demands a lower CDR bandwidth
- Track desired frequency w/ reduced update rate

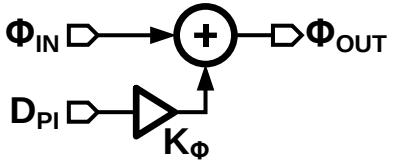
Phase Interpolator (PI)



Block Diagram



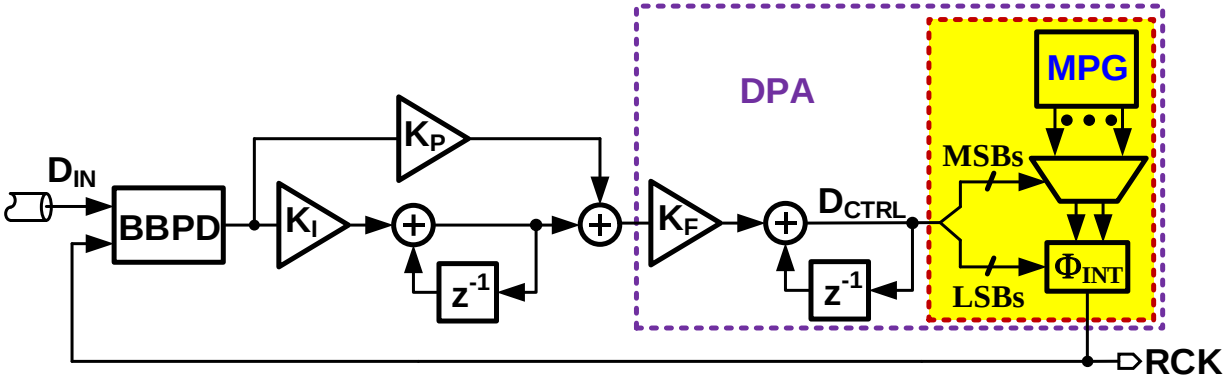
Phasor Diagram



Small Signal Model

- PI interpolates I/P clock → intermediate O/P clock
- O/P phase $\propto$ n-bit phase control word (PCW)
- Phase resolution is limited by # of bits
- # of PIs increase with # of o/p phases required

Practical Dual-Loop CDR[9]

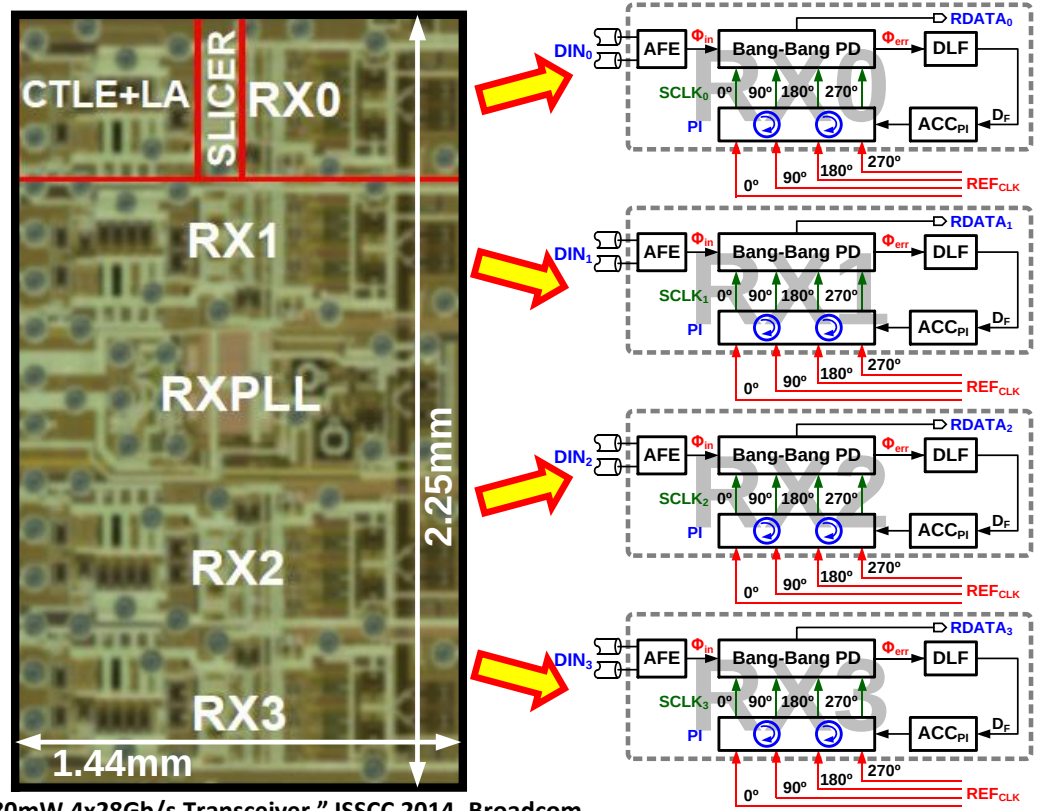


DPA: Digital Phase Accumulator

MPG: Multi Phase Generator

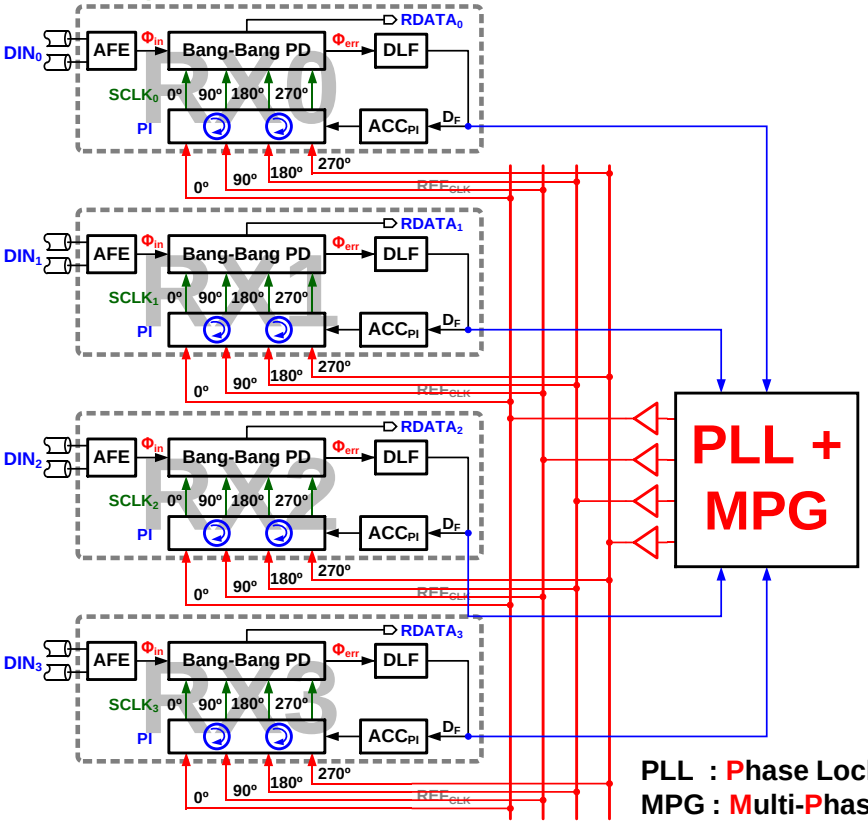
- Phase interpolator (Φ_{INT}) improves DPA resolution
- Multi-phase generator is not inside CDR loop
- Accumulator + PI = Digitally Controlled Oscillator

PI-based Multi-Lane Chip-to-Chip Link[10-14]



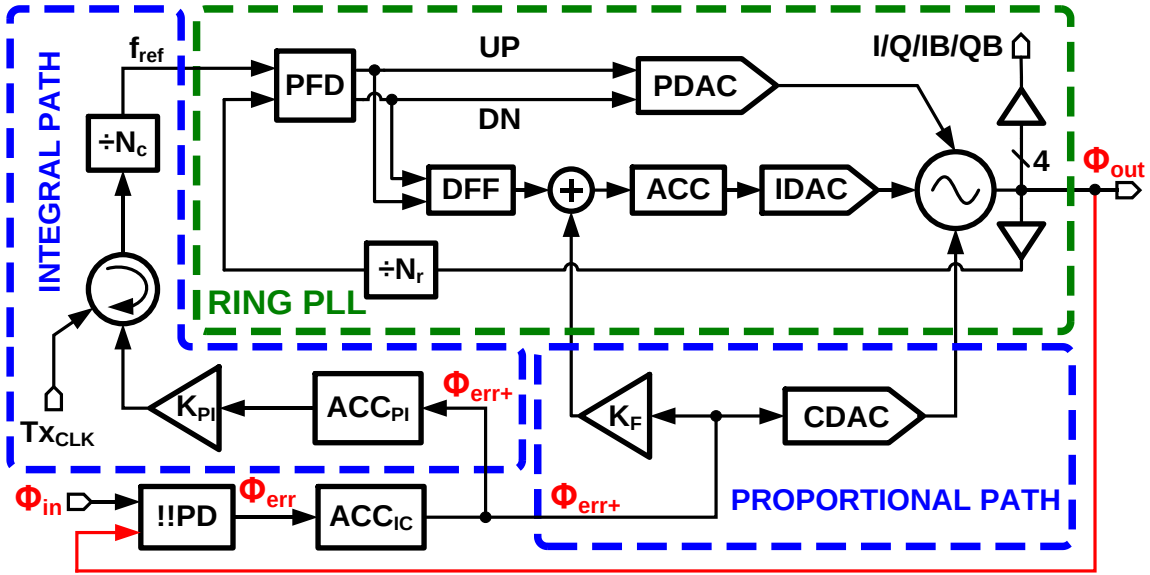
"A 780mW 4x28Gb/s Transceiver," ISSCC 2014, Broadcom

High Speed Multi-phase Reference Clock

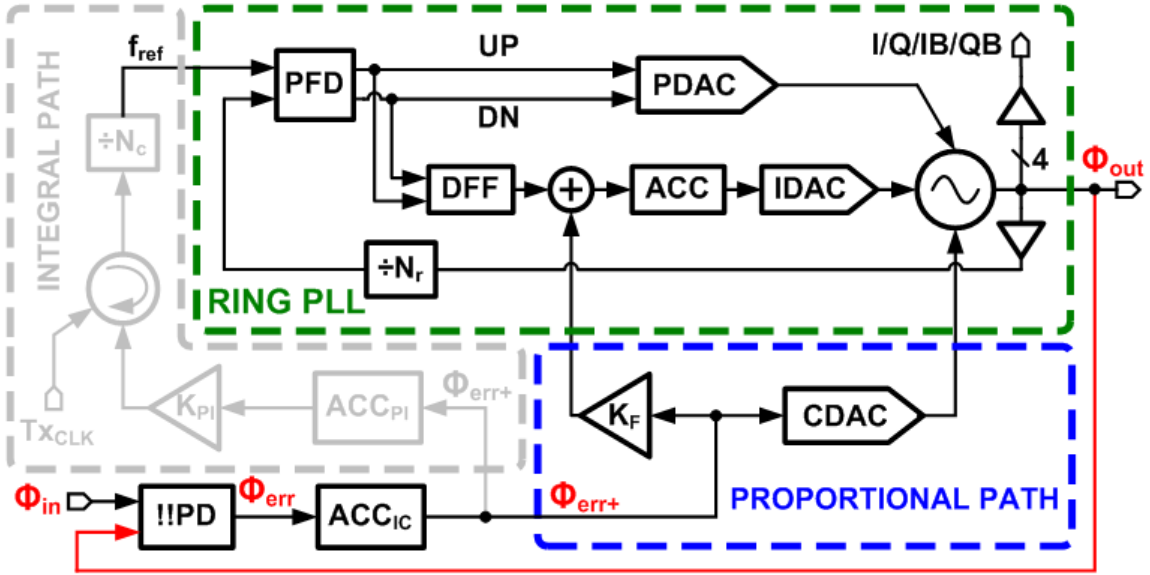


PLL : Phase Locked Loop
MPG : Multi-Phase Generator

BBPD based Sub-rate Digital CDR w/ Embedded PLL[13]



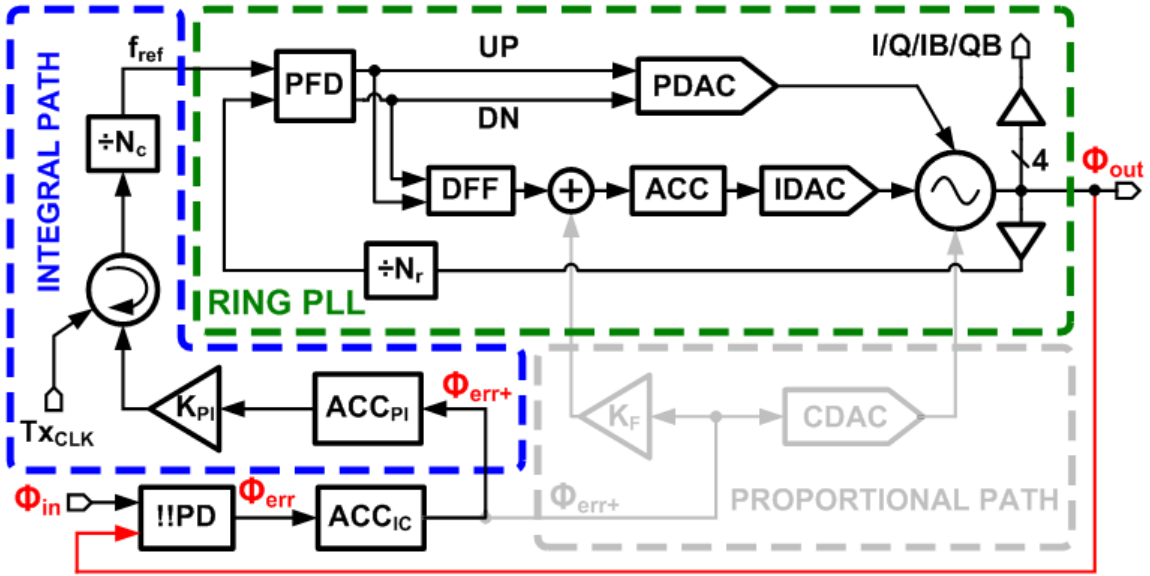
Proportional Control in Digital CDR w/ Embedded PLL (I)



$$\mathrm{LG_{prop,cdr}(s)} = \left.\frac{\Phi_{out}}{\Phi_{in}}\right|_{prop,cdr}$$

$$= \frac{K_{bbpd} f_{ref}}{s} \times \frac{N_r LG_{RPLL}(s)}{1+LG_{RPLL}(s)} \left[\frac{K_{pc,pr}+\frac{K_{pc,ir} f_{ref}}{s}}{K_{pr}+\frac{K_{ir} f_{ref}}{s}}\right]$$

Integral Control in Digital CDR w/ Embedded PLL (II)



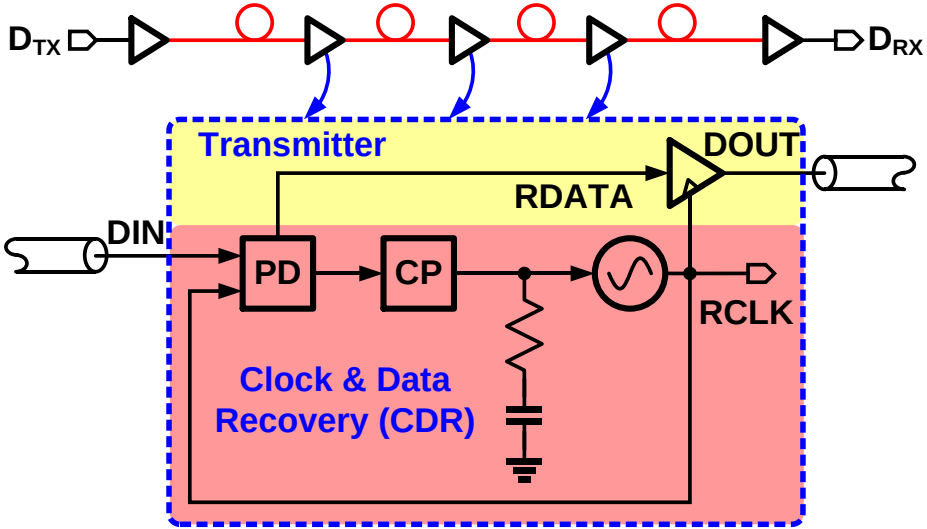
$$LG_{int,cdr}(s) = \frac{K_{bbpd}K_{ic}f_{ref}^2}{s^2N_c} \times \frac{N_r LG_{RPLL}(s)}{1+LG_{RPLL}(s)}$$

$$\approx \frac{K_{bbpd}K_{ic}f_{ref}^2N_r}{s^2N_c}$$

Overview

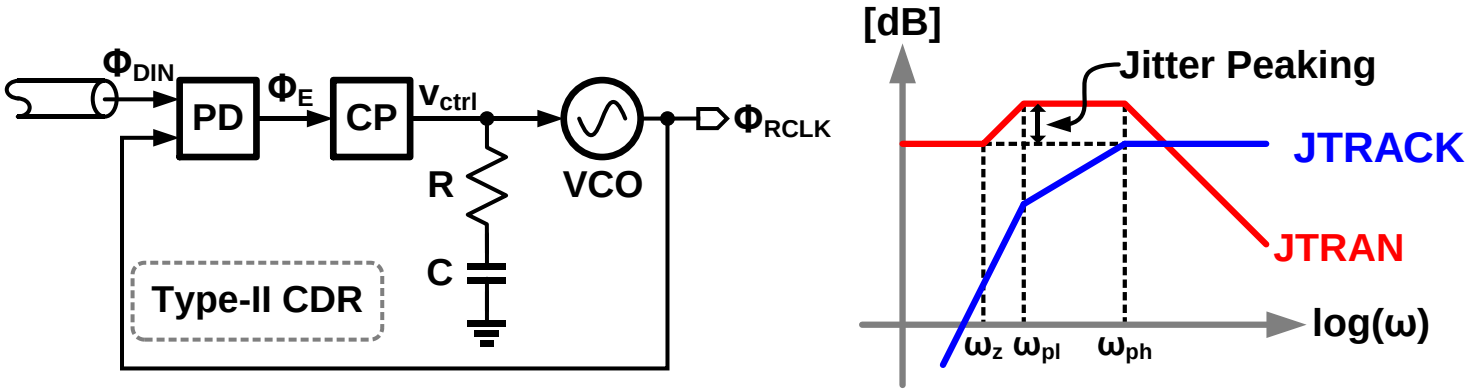
- ❑ Performance metrics
- ❑ Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid
- ❑ Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables
- ❑ Frequency detectors

Long Haul Communication w/ Repeaters



- Repeater requirements
  - Tolerate large input jitter present on DIN (high JTOL)
  - Filter input jitter (low JTRAN BW) w/ minimal peaking
  - Re-transmit with low jitter (low JGEN)

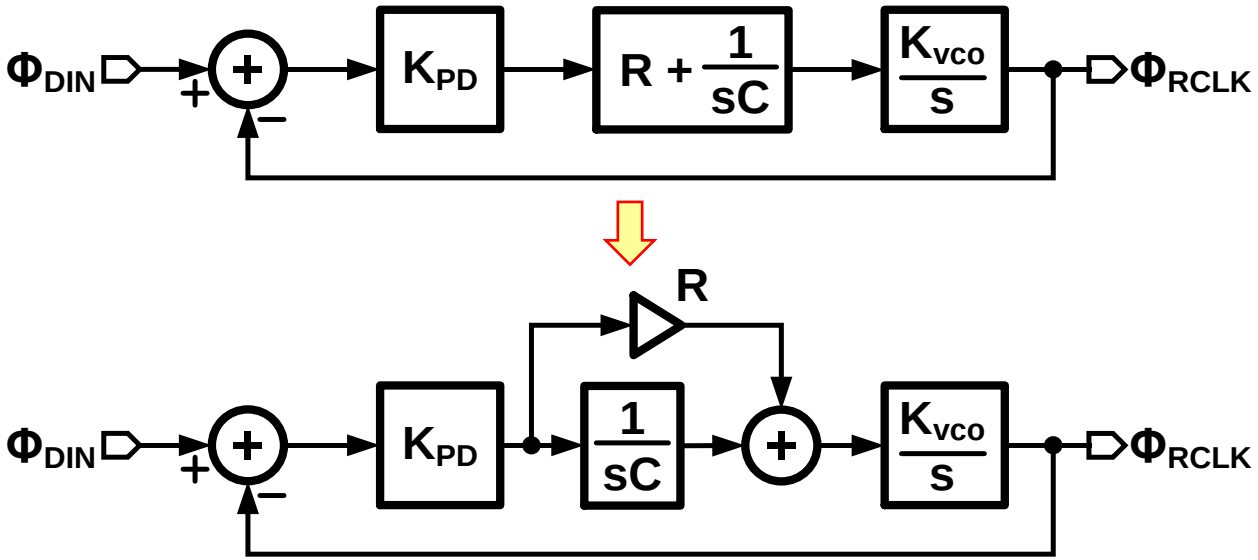
Conventional Type-II CDR in Repeaters



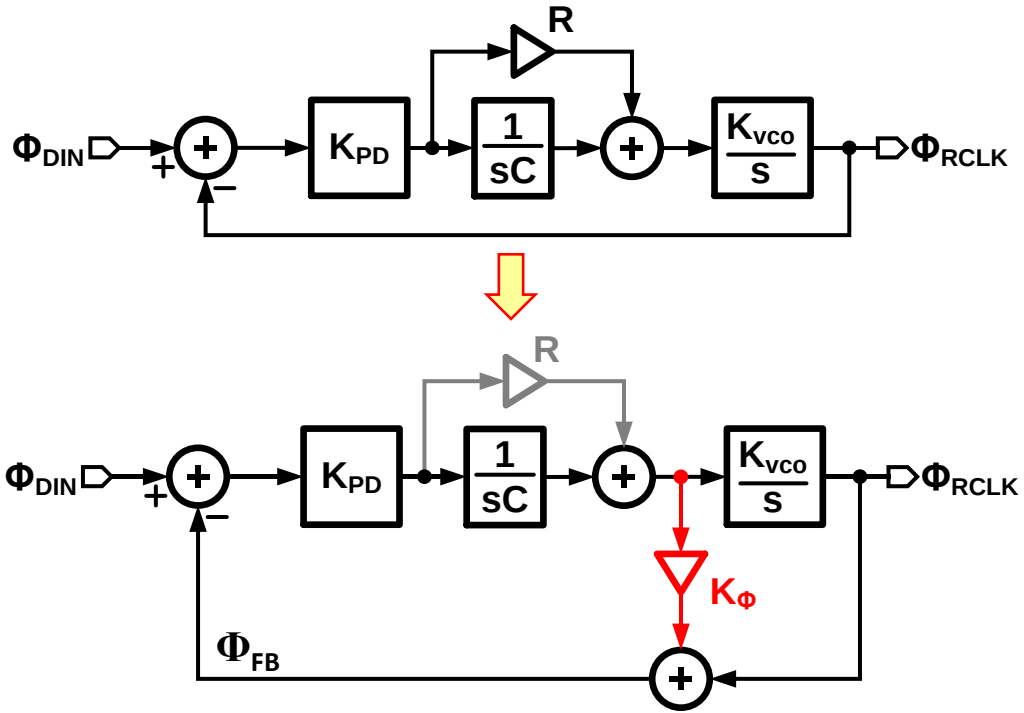
- ω_z is cause for jitter peaking in forward path but must for stability
- High JTRACK BW (or JTOL corner freq.) → high JTRAN BW
- Inadequate filtering of Φ_{DIN} → more R_{CLK} jitter → Retransmission with more jitter

How to Eliminate Jitter Peaking?

- Main Idea:
  - Retain ω_z in loop for stability
  - Remove ω_z from forward path to eliminate peaking

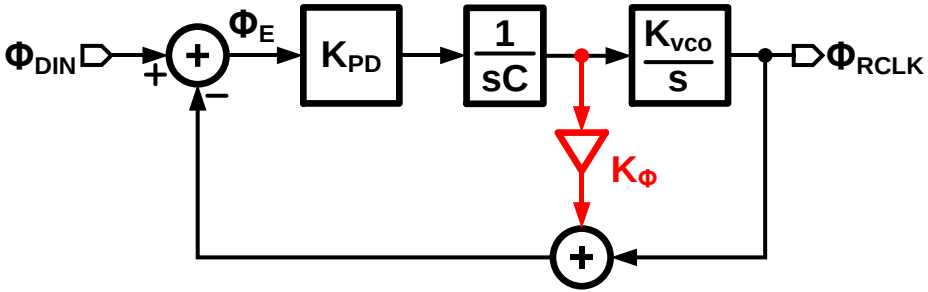


Add to VCO's Output Phase (I)



- No zero in feed-forward path

Add to VCO's Output Phase (II)



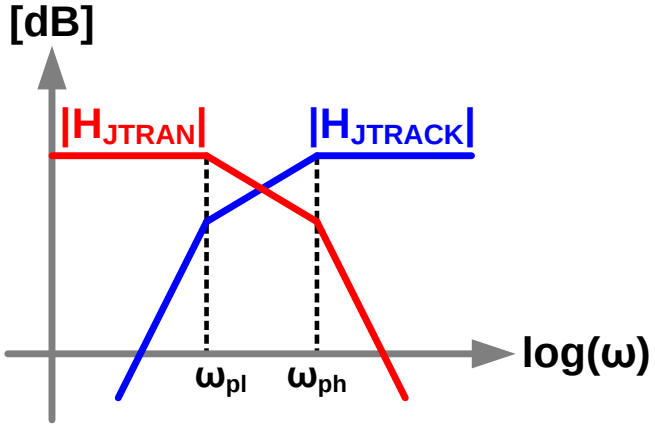
$$\mathrm{LG(s)} = \frac{\mathrm{K_{PD}K_{vco}}}{\mathrm{s^2C}}\left(1 + \frac{\mathrm{sK}_\phi}{\mathrm{K_{vco}}}\right) = \frac{\mathrm{K}}{\mathrm{s^2}}\left(1 + \mathrm{s}/\omega_\mathrm{z}\right)$$

$$\mathrm{H_{JTRAN}} = \frac{\Phi_\mathrm{RCLK}(\mathrm{s})}{\Phi_\mathrm{DIN}(\mathrm{s})} = \frac{\mathrm{LG(s)}}{1 + \mathrm{LG(s)}}\frac{1}{(1 + \mathrm{s}/\omega_\mathrm{z})} = \frac{\mathrm{K_{PD}K_{vco}}}{\mathrm{s^2C} + \mathrm{sK_{PD}K}_\phi + \mathrm{K_{PD}K_{vco}}}$$

$$\mathrm{H_{JTRACK}} = \frac{\Phi_\mathrm{E}(\mathrm{s})}{\Phi_\mathrm{DIN}(\mathrm{s})} = \frac{1}{1 + \mathrm{LG(s)}} = \frac{\mathrm{s^2}}{\mathrm{s^2C} + \mathrm{sK_{PD}K}_\phi + \mathrm{K_{PD}K_{vco}}}$$

- Phase is added to output clock, RCLK
- Loop can be stable with no jitter peaking (ζ>0.707)

Decoupled JTRAN & JTRACK/JTOL

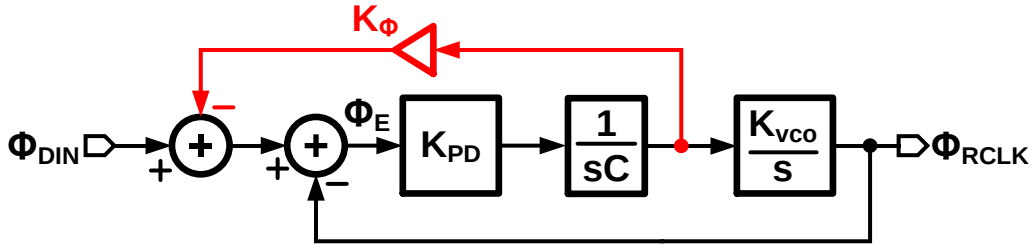


$$H_{JTRAN}(s) = \frac{\Phi_{RCLK}(s)}{\Phi_{DIN}(s)} = \frac{K_{PD}K_{vco}}{s^2C + sK_{PD}K_{\phi} + K_{PD}K_{vco}}$$

$$H_{JTRACK}(s) = \frac{\Phi_{E}(s)}{\Phi_{DIN}(s)} = \frac{s^2}{s^2C + sK_{PD}K_{\phi} + K_{PD}K_{vco}}$$

- ω_{pl} ($\approx K_{PD}K_{\Phi}/C$) limits JTRAN bandwidth
- ω_{ph} ($\approx K_{VCO}/K_{\Phi}$) limits JTRACK or JTOL bandwidth

Add to Input Phase (II)[15]



$$LG(s) = \frac{K_{PD}K_{vco}}{s^2C}\left(1 + \frac{sK_\phi}{K_{vco}}\right) = \frac{K}{s^2}(1 + s/\omega_z)$$

$$H_{JTRAN}(s) = \frac{\Phi_{RCLK}(s)}{\Phi_{DIN}(s)} = \frac{LG(s)}{1 + LG(s)}\frac{1}{(1 + s/\omega_z)} = \frac{K_{PD}K_{vco}}{s^2C + sK_{PD}K_\phi + K_{PD}K_{vco}}$$

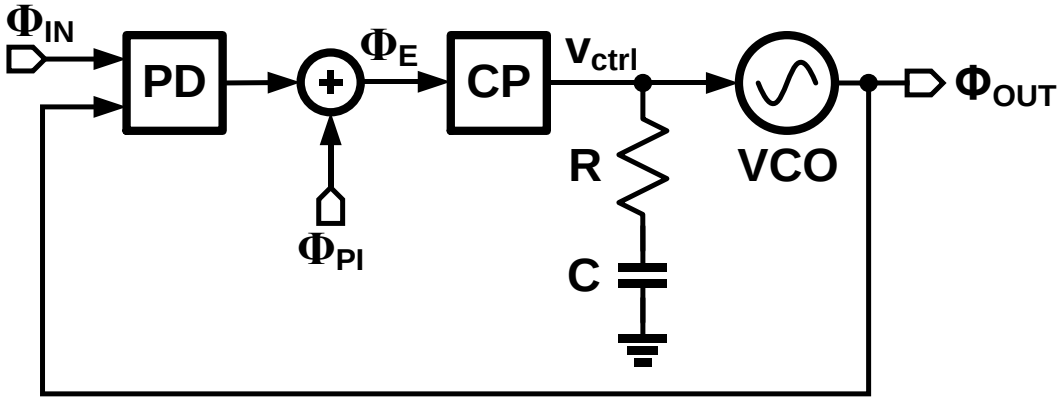
$$H_{JTRACK}(s) = \frac{\Phi_E(s)}{\Phi_{DIN}(s)} = \frac{1}{1 + LG(s)} = \frac{s^2}{s^2C + sK_{PD}K_\phi + K_{PD}K_{vco}}$$

- Phase is added to input data, DIN
- JTRAN and JTOL/JTRACK are decoupled

How to Add Phase to Input/Output ?

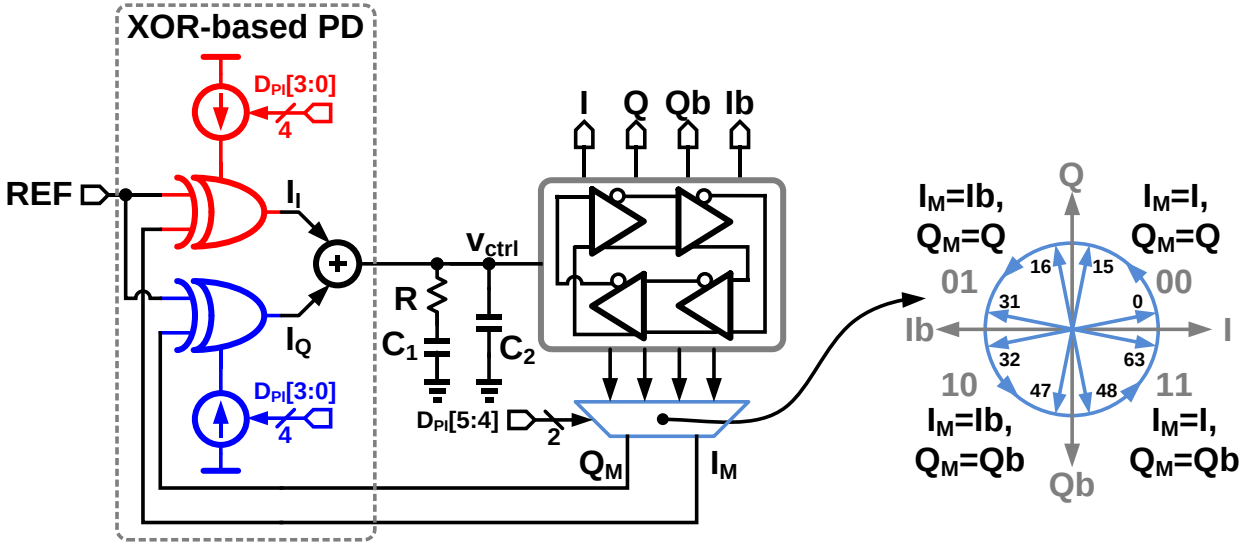
- Phase Interpolator (PI)
- Phase Rotating Phase-Locked Loop (PRPLL)
- Delay Line

PRPLL's Basic Principle



- Φ_{PI} is an external phase added to PLL
- In steady state of PLL, $\Phi_{OUT} = \Phi_{IN} - \Phi_{PI}$
- Ring oscillator (VCO) generates multiple output clock phases shifted by Φ_{PI} and used in CDR

Phase-Rotating Phase-Locked Loop



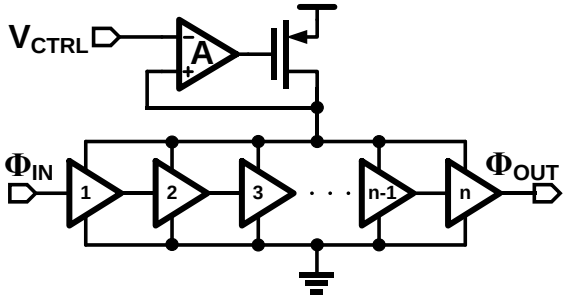
- PLL generates multiple clock phases (I/Q/Ib/Qb)
- Phase added to output clock in XOR-PD through D_{PI}
- $D_{PI}[5:4]$ select I_M & Q_M from clock phases I,Q,Ib,Qb
- $D_{PI}[3:0]$ change weight of I_M & Q_M in XOR-PD

How to Add Phase to Input/Output ?

- Phase Interpolator (PI)
- Phase Rotating Phase-Locked Loop (PRPLL)
- Delay Line

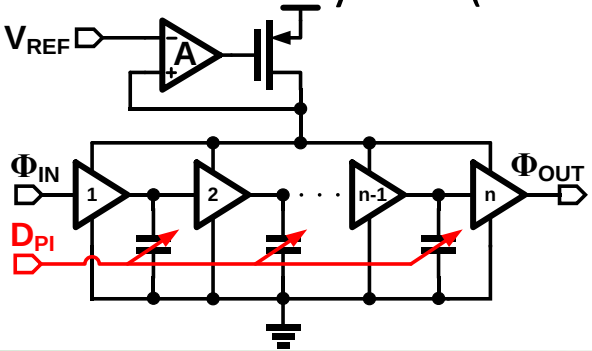
Delay Line

- Voltage Controlled Delay Line (VCDL)



$$\Phi_{OUT} = \Phi_{IN} + K_{VCDL}.V_{CTRL}$$

- Digitally Controlled Delay Line (DCDL)



$$\Phi_{OUT} = \Phi_{IN} + K_{DCDL}.D_{PI}$$

Comparison b/w Phase Addition Methods

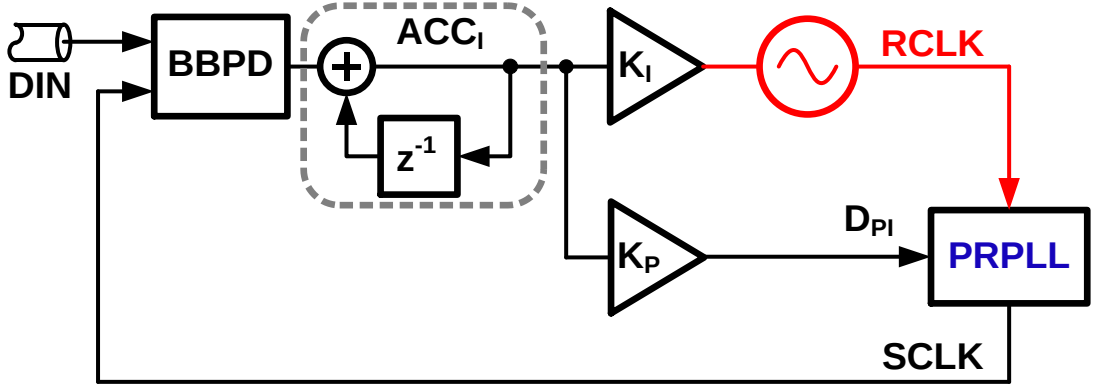
	PI	PRPLL	Delay Line
Architecture	Open loop	Closed loop	Open loop
Range	Infinite	Infinite	Limited
Φ added to CLK	Yes	Yes	Yes
Φ added to Data	No	No	Yes
Hardware for sub-rate CDRs	Increases	No change	Increases for CLK, No change for Data

- Φ addition in data path adds to data dependent ISI

CDR Examples w/ JTRAN & JTOL Decoupling

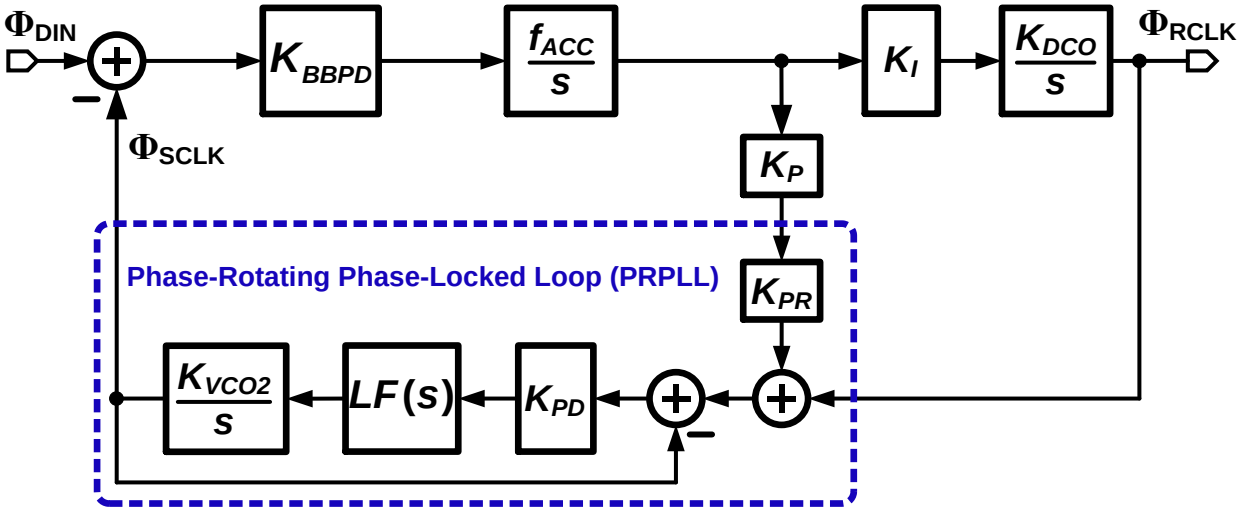
- Digital clock & data recovery using phase-rotating phase-locked loop (PRPLL)
- Digital clock & data recovery using digitally controlled delay line in data path

Block Diagram of 5Gb/s PRPLL-based Digital CDR[21]



- Input jitter is filtered at recovered clock O/P, RCLK
- Input jitter is tracked at sampling clock, SCLK, using phase-rotating phase-locked loop (PRPLL)
- Recovered clock is a reference for PRPLL

Linearized Model of PRPLL-based Digital CDR



$$\mathrm{LG(s)} = \rho \mathrm{K_{BBPD}} \frac{\mathrm{f_{ACC}}}{\mathrm{s}} \left(\mathrm{K_P K_{PR}} + \frac{\mathrm{K_I K_{DCO}}}{\mathrm{s}} \right) \times \frac{\mathrm{LG_{PRPLL}(s)}}{1 + \mathrm{LG_{PRPLL}(s)}}$$

$$\mathrm{LG_{PRPLL}(s)} = \mathrm{K_{PD} LF(s)} \frac{\mathrm{K_{VCO2}}}{\mathrm{s}}$$

- ρ is input transition density

Loop Analysis of PRPLL-based Digital CDR

Approximating, $\frac{LG_{PRPLL}(s)}{1+LG_{PRPLL}(s)} \approx 1$

$$H_{IN2RCLK} = \frac{\Phi_{RCLK}(s)}{\Phi_{DIN}(s)} = \frac{\rho K_{BBPD} f_{ACC} K_I K_{DCO}}{s^2 + s\rho K_{BBPD} f_{ACC} K_P K_{PR} + \rho K_{BBPD} f_{ACC} K_I K_{DCO}}$$

$$H_{IN2SCLK} = \frac{\Phi_{SCLK}(s)}{\Phi_{DIN}(s)} = \frac{s\rho K_{BBPD} f_{ACC} K_P K_{PR} + \rho K_{BBPD} f_{ACC} K_I K_{DCO}}{s^2 + s\rho K_{BBPD} f_{ACC} K_P K_{PR} + \rho K_{BBPD} f_{ACC} K_I K_{DCO}}$$

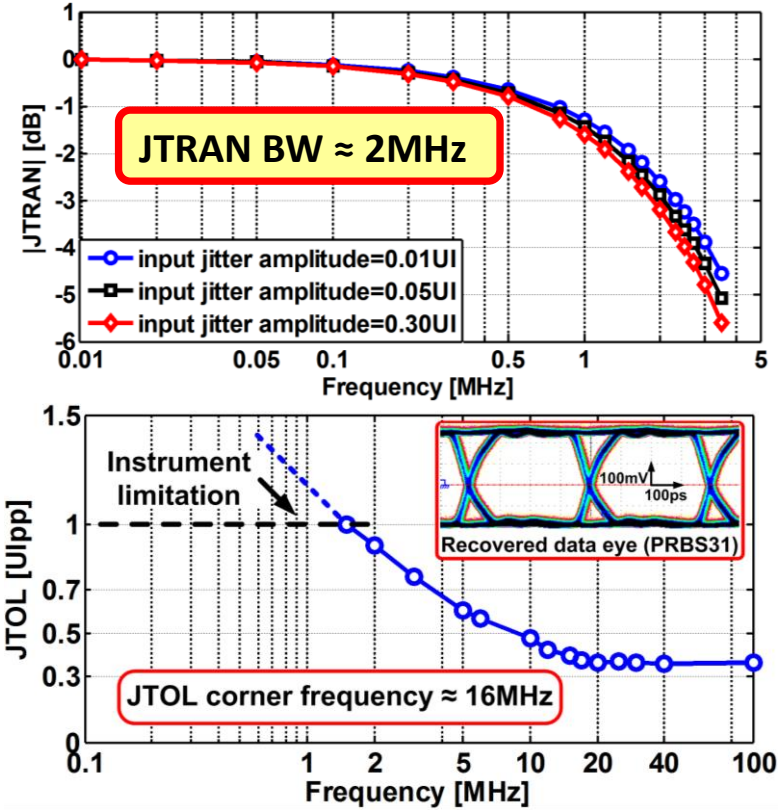
$$\omega_{p1} = \frac{K_{PP}}{2}\left(1 - \sqrt{1 - \frac{4K_{INT}}{K_{PP}^2}}\right) \approx \frac{K_{INT}}{K_{PP}} = \frac{K_I K_{DCO}}{K_P K_{PR}}$$

$$\omega_{p2} = \frac{K_{PP}}{2}\left(1 + \sqrt{1 - \frac{4K_{INT}}{K_{PP}^2}}\right) \approx K_{PP} = \rho K_{BBPD} f_{ACC} K_P K_{PR}$$

- No peaking for $Q_P = \frac{\sqrt{K_{INT}}}{K_{PP}} \leq \frac{1}{\sqrt{2}}$
- In general, ω_{p1} limits JTRAN bandwidth and ω_{p2} limits JTRACK bandwidth

PRPLL-based Digital CDR Measurement Results (I)

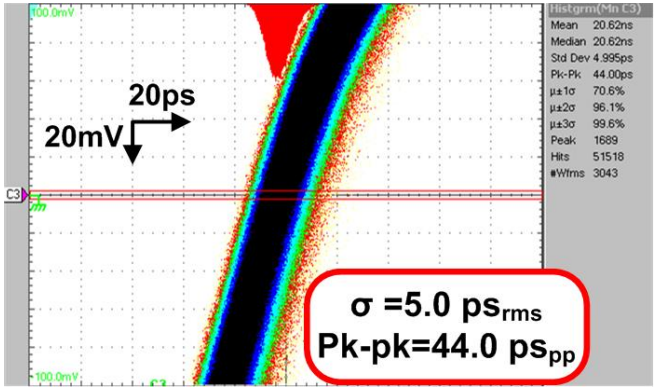
K_{PR}	2π/64 rad/s
K_{DCO}	2π x 10^5 rad/s/LSB
K_P	0.5
K_I	0.25
f_{ACC}	$f_{VCO}/4$
DCO's PN	-100 dBc/Hz @1M
DCO's DAC	0.4 MHz/LSB



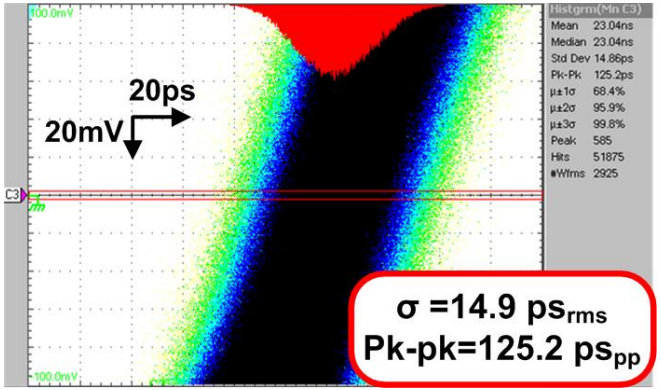
PRPLL-based Digital CDR Measurement Results (II)

K_{PR}	2π/64 rad/s
K_{DCO}	2π x 10^5 rad/s/LSB
K_P	0.5
K_I	0.25
f_{ACC}	f_{VCO}/4
DCO's PN	-100 dBc/Hz @1M
DCO's DAC	0.4 MHz/LSB

Recovered Clock



Sampling Clock

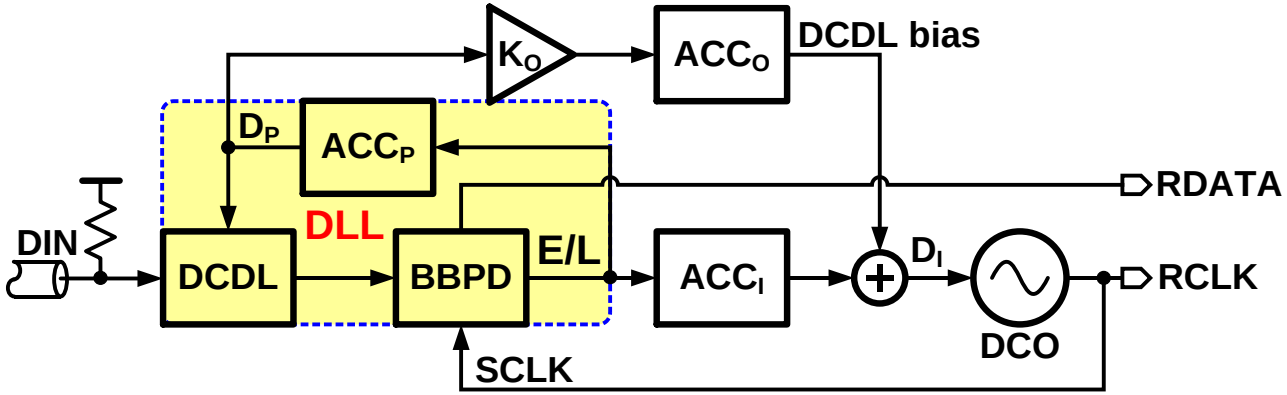


CDR Examples w/ JTRAN & JTOL Decoupling

- Digital clock & data recovery using phase-rotating phase-locked loop (PRPLL)

- Digital clock & data recovery using digitally controlled delay line in data path

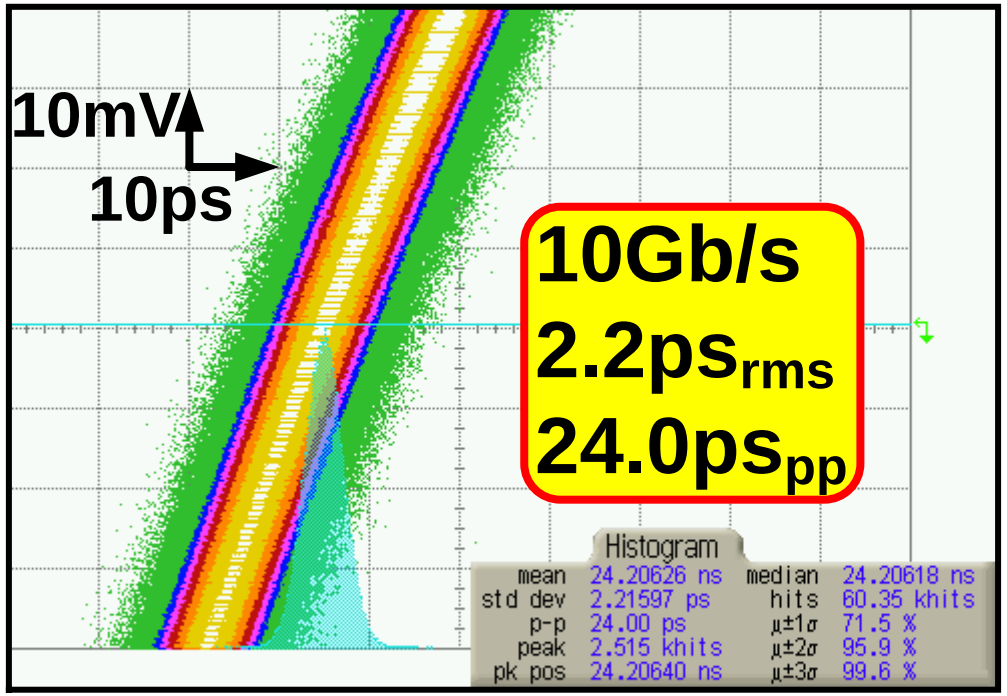
Block Diagram of a 4-10Gb/s Half-Rate Digital CDR[22]



DCDL: Digitally Controlled Delay Line

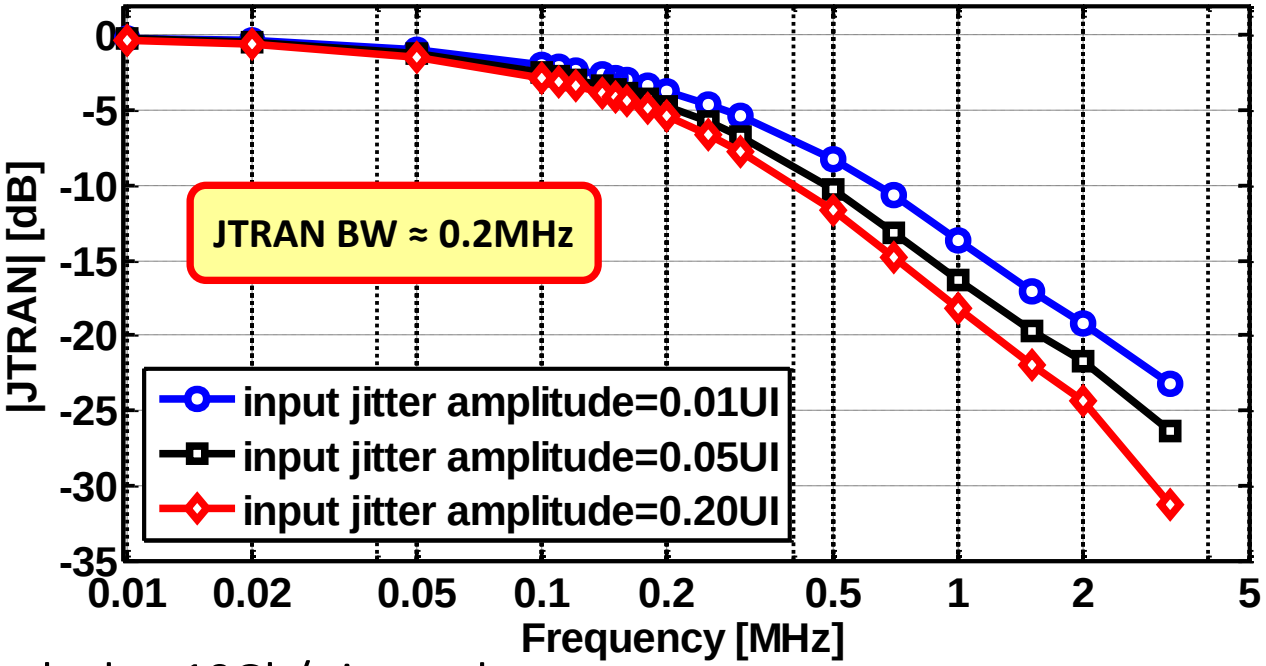
- Decoupled JTRAN/JTOL w/ no jitter peaking
  - JTRAN=K_{DCO}/K_{DCDL} (Doesn't depend on BBPD gain)
- DCDL using CMOS buffers for low power
- Wide-range fractional-N PLL based low noise DCO
- Digital CDR realized in TSMC 65nm CMOS process

Recovered Clock of CDR locked at 10Gb/s



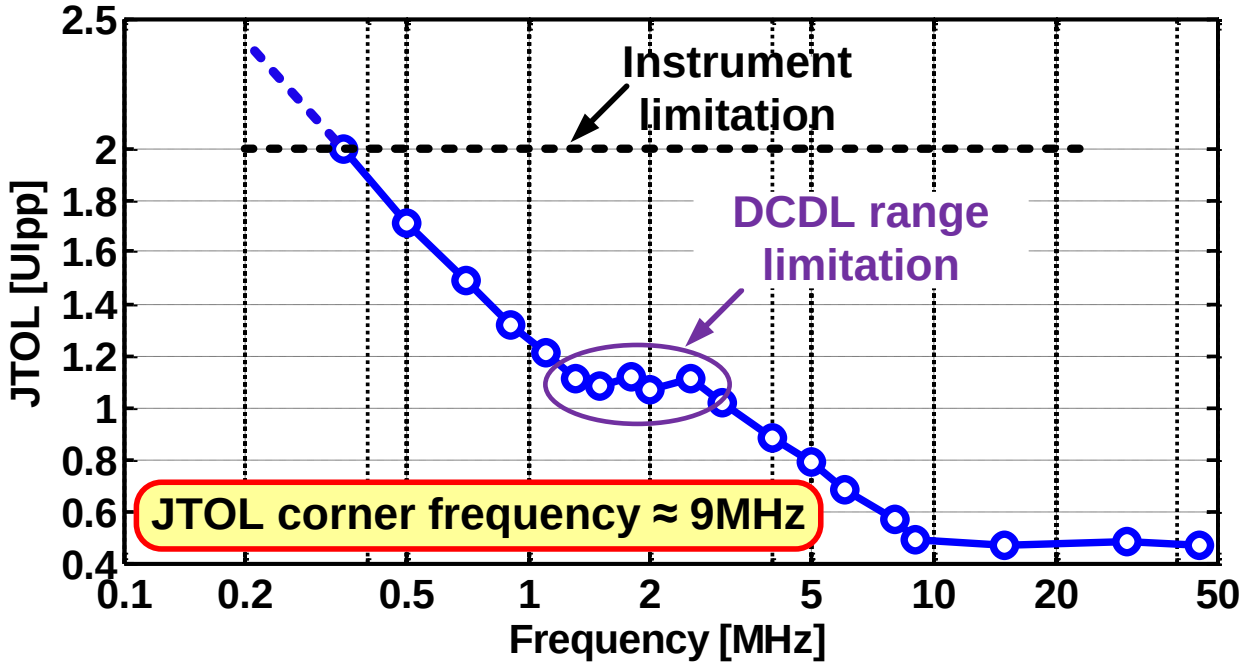
- 2.2 ps_{rms} jitter for 5GHz recovered clock (R_{CLK})

Measured Jitter Transfer Function (JTRAN)



- CDR is locked to 10Gb/s input data
- JTRAN bandwidth ≈ 0.2MHz

Measured Jitter Tolerance (JTOL)

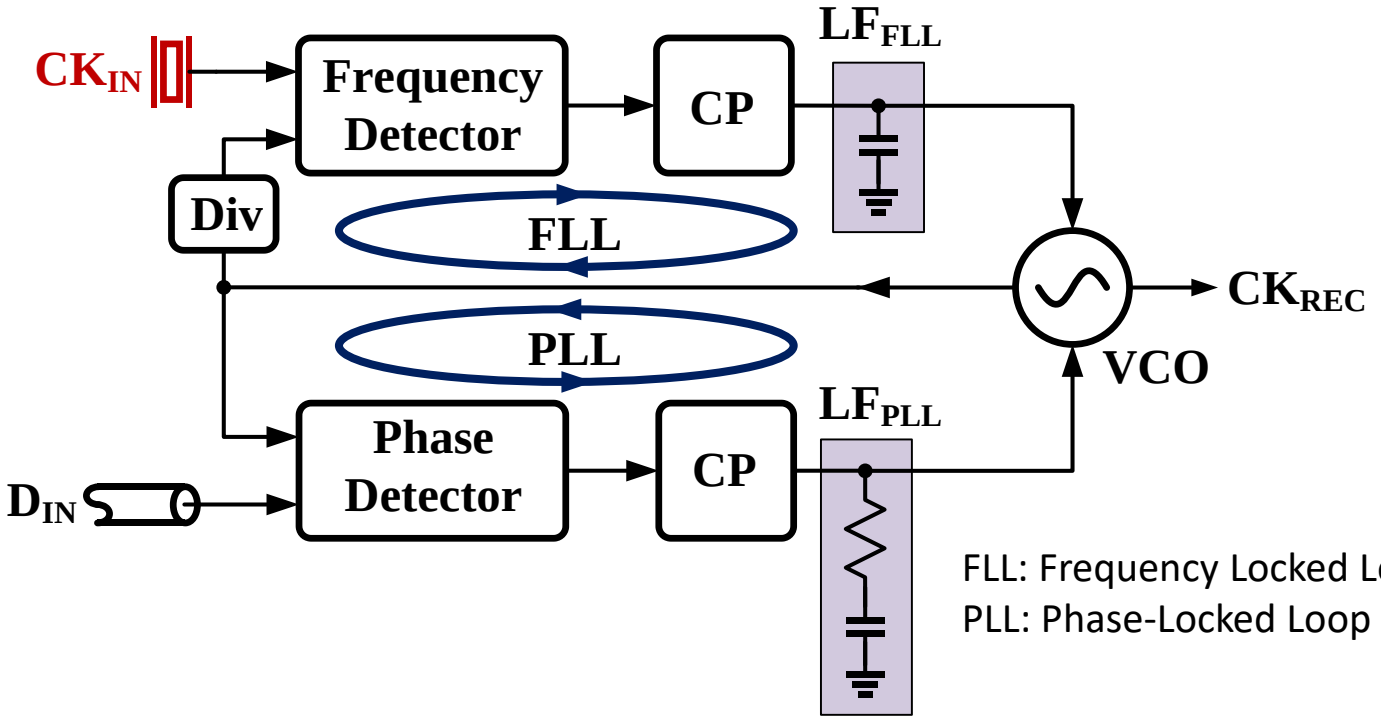


- JTOL measured w/ BER threshold of 10^{-12} & PRBS7 data 10Gb/s

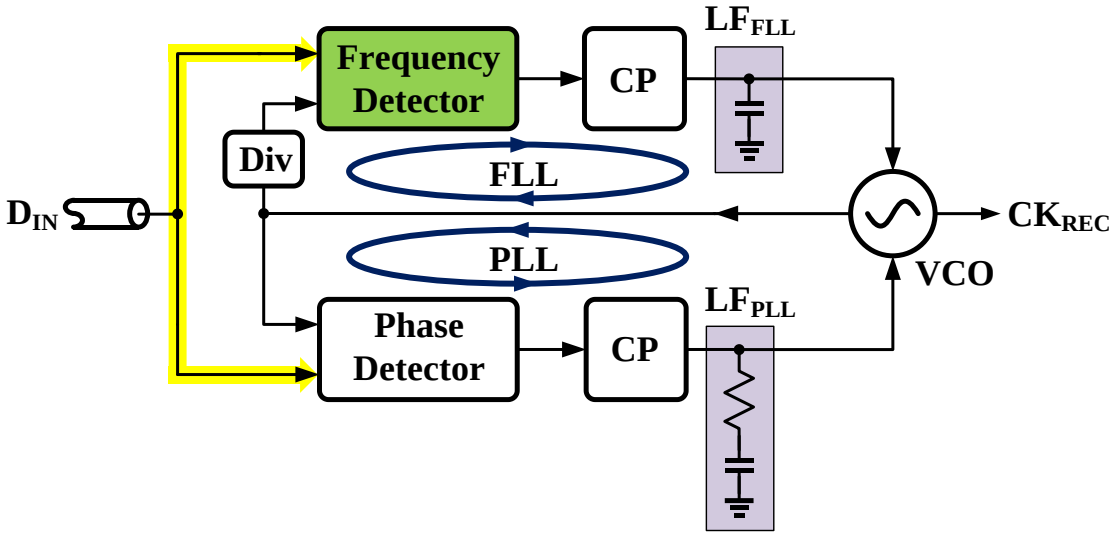
Overview

- Performance metrics
- Basic architectures
  - Linear/Bang-bang
  - Digital
  - Hybrid
- Application-specific CDRs
  - Multi-lane chip-to-chip links
  - Repeaters for optical links and active cables
- Frequency detectors

Frequency & Phase Tracking in CDRs

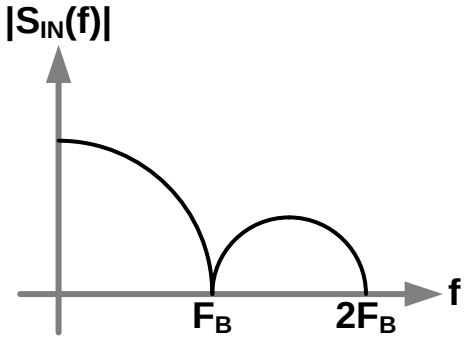


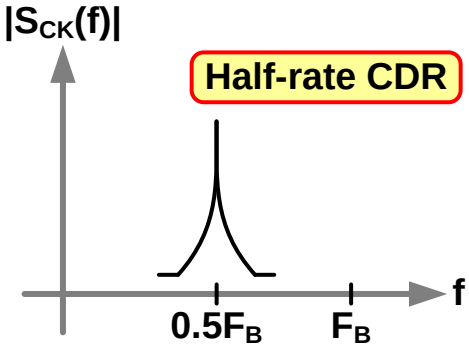
Reference-less CDR

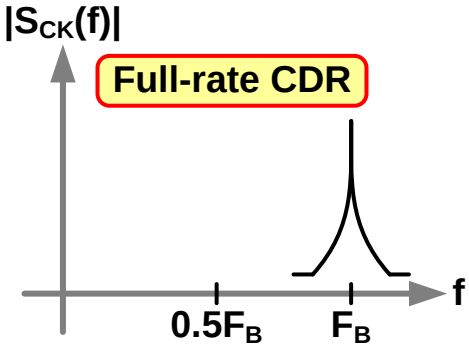


- Reference extracted from incoming random data
- Continuous data-rate
- Requires *frequency extraction* from random data

Role of FLL: Frequency Domain View







Frequency Detector

- Rotational frequency detector[22-24]
- Quadri-correlator frequency detector[25-26]
- Stochastic reference clock generator[27]
- Miscellaneous FDs
  - Strobed linear PD[27]
  - Counting based FDs [28-29]

Frequency Detector

- Rotational frequency detector[22-24]
- Quadri-correlator frequency detector[25-26]
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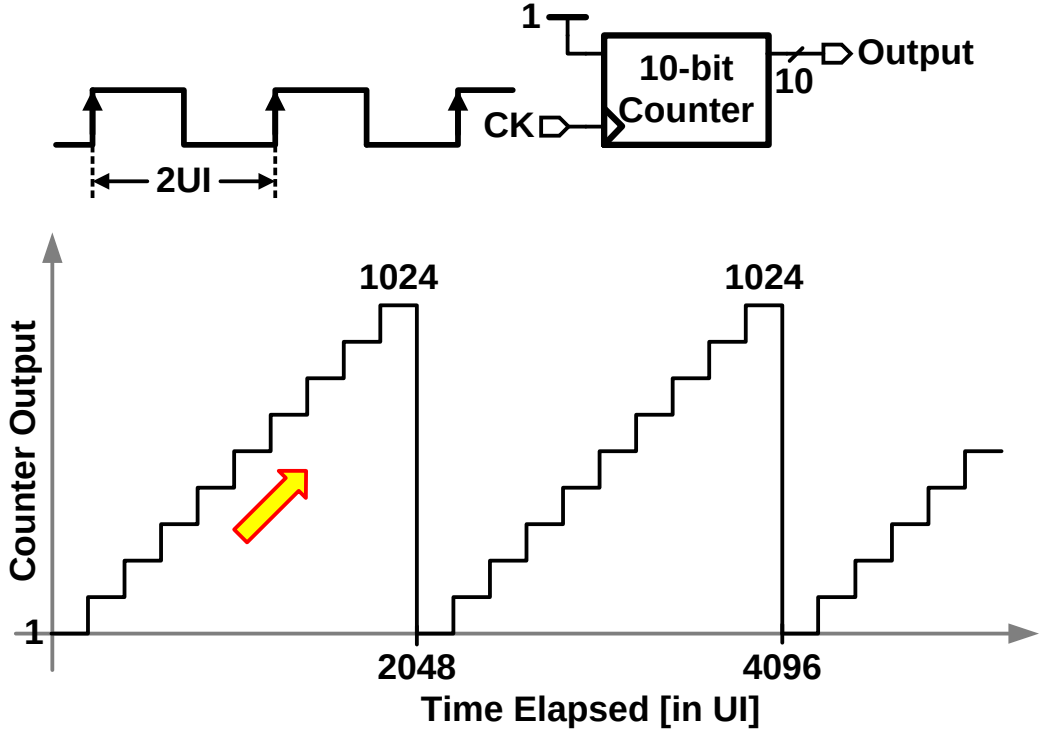
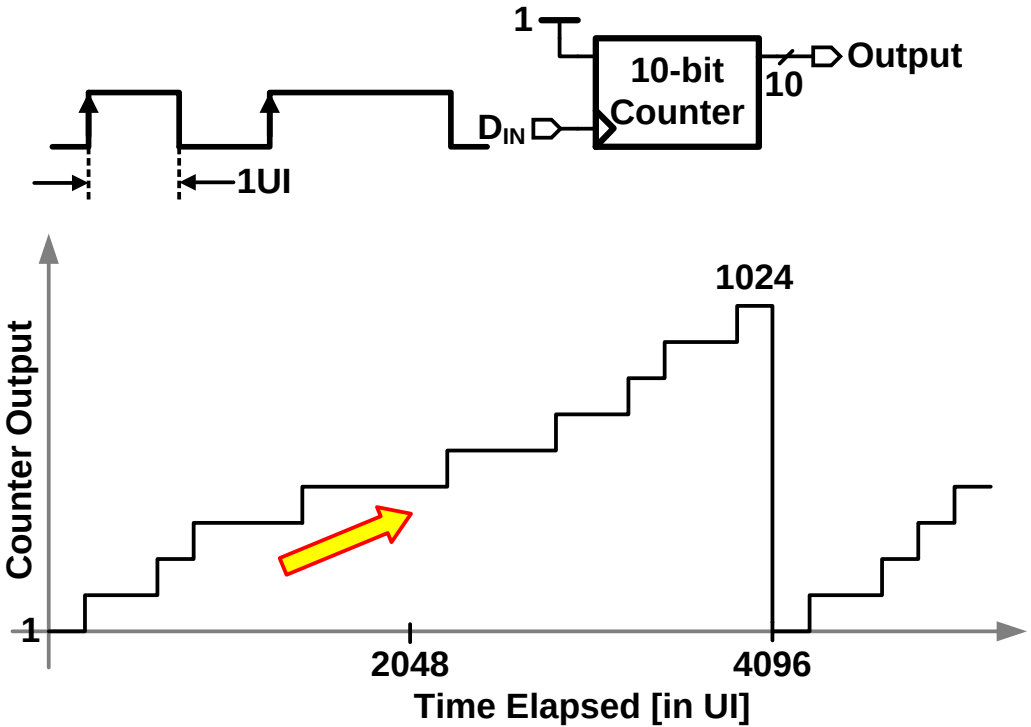
  - Strobed linear PD[27]
  - Counting based FDs[28-29]

Accumulation – Alternating Data



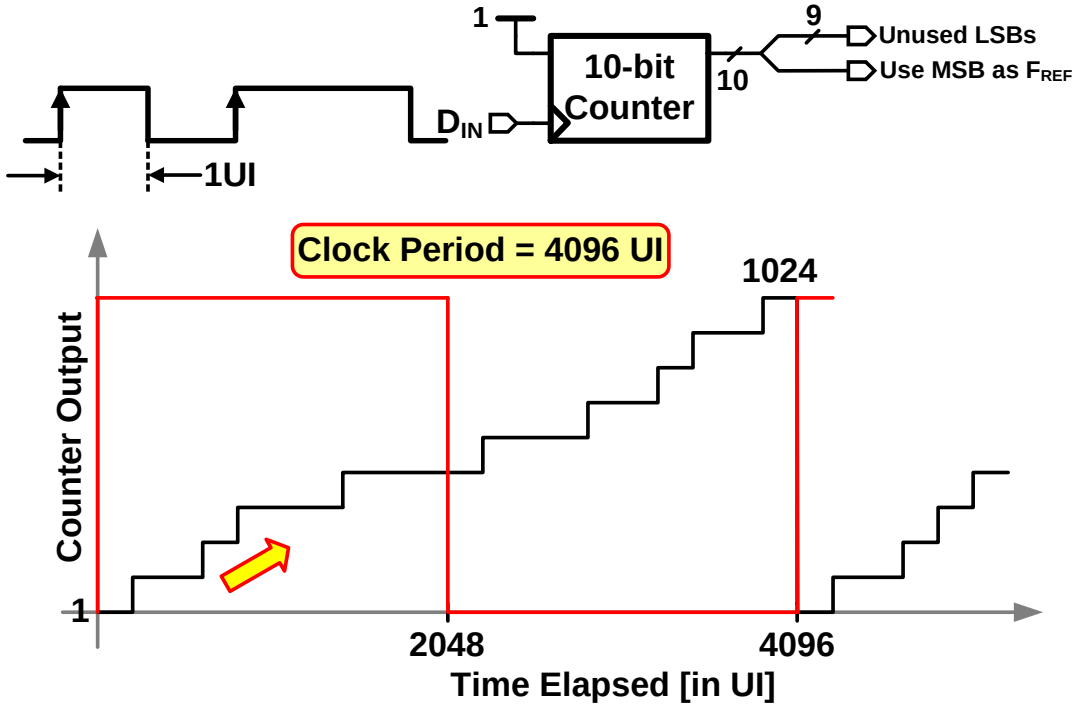
- Accumulator rolls over after 2048 UI

Accumulation – Random Data



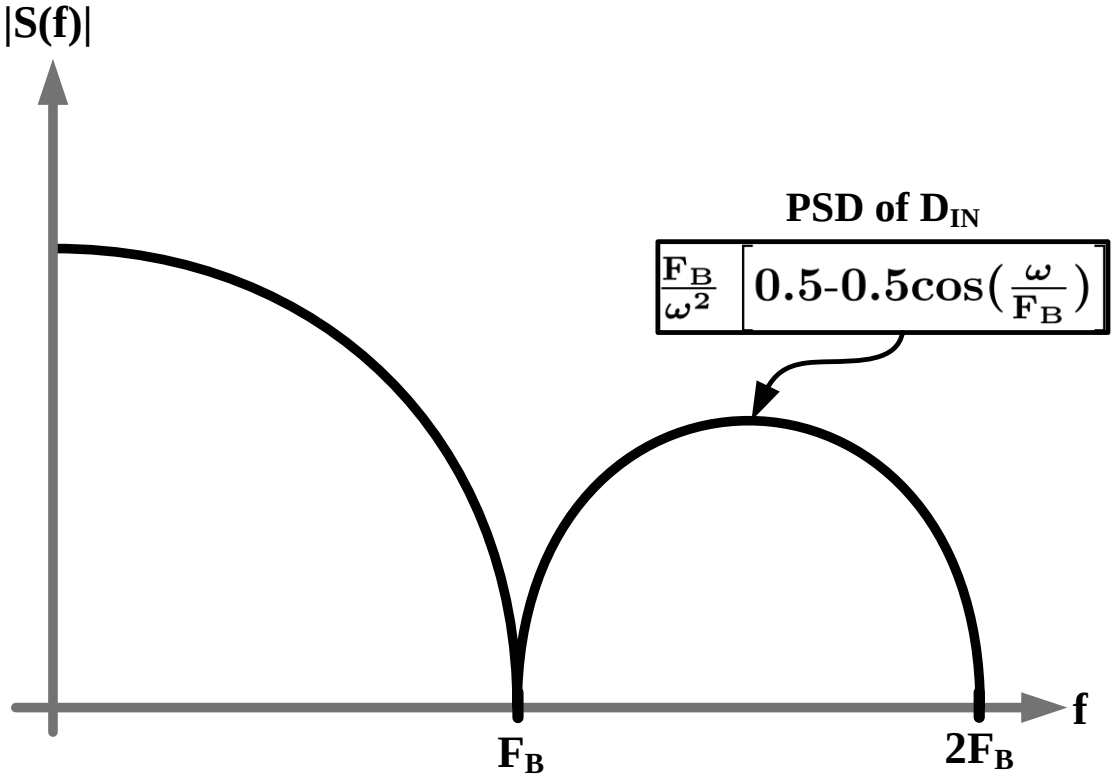
- With random input accumulator rolls over after 4096 UI

Extracting Clock from Counter Output

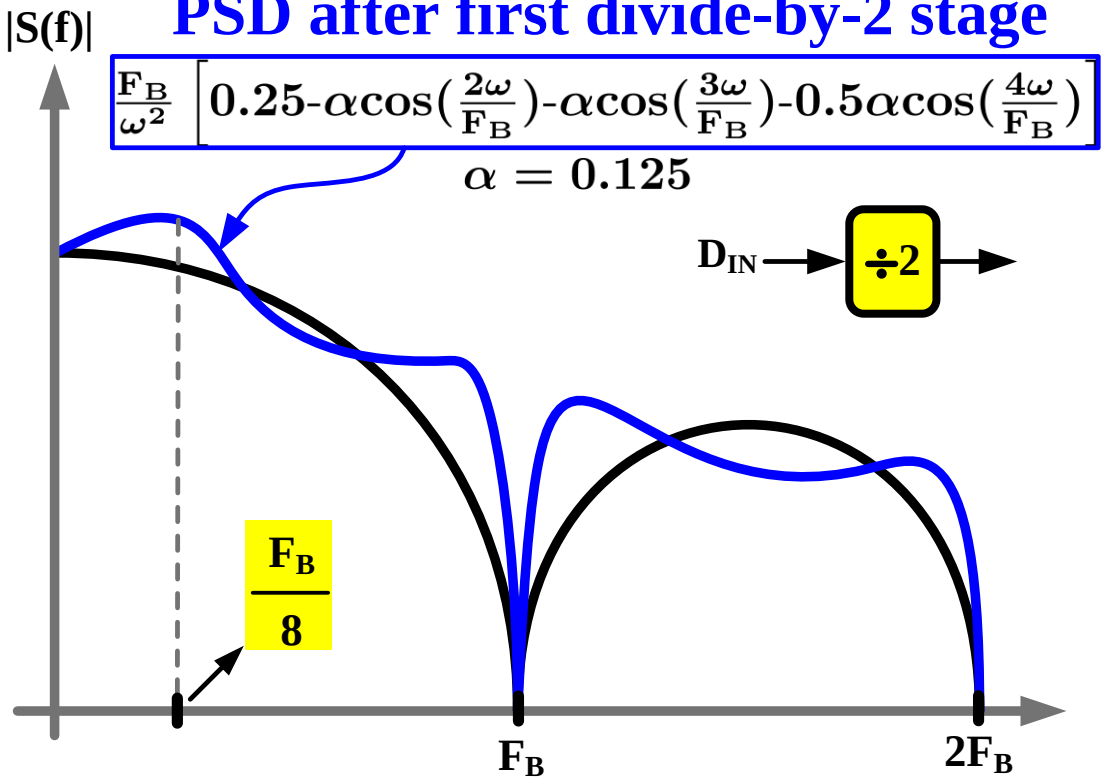


- MSB can be used for ref. clock w/ $1/F_{REF}$=4096UI

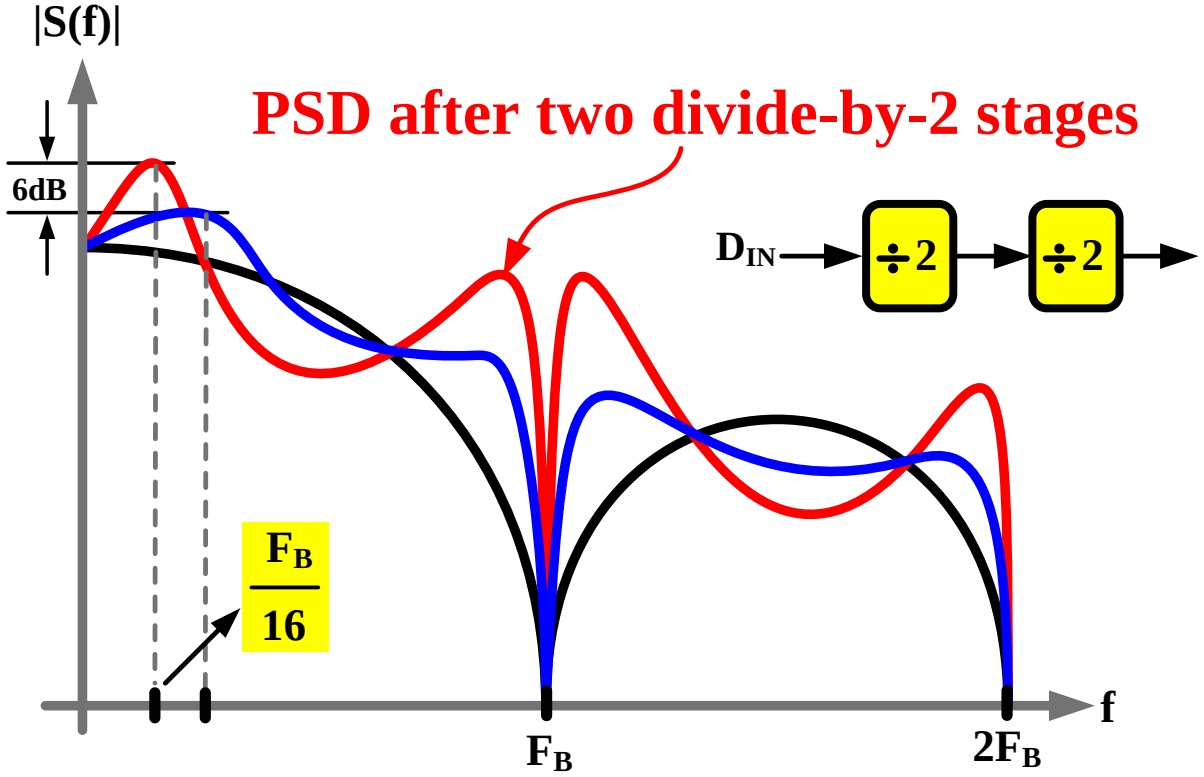
PSD of NRZ Random Data



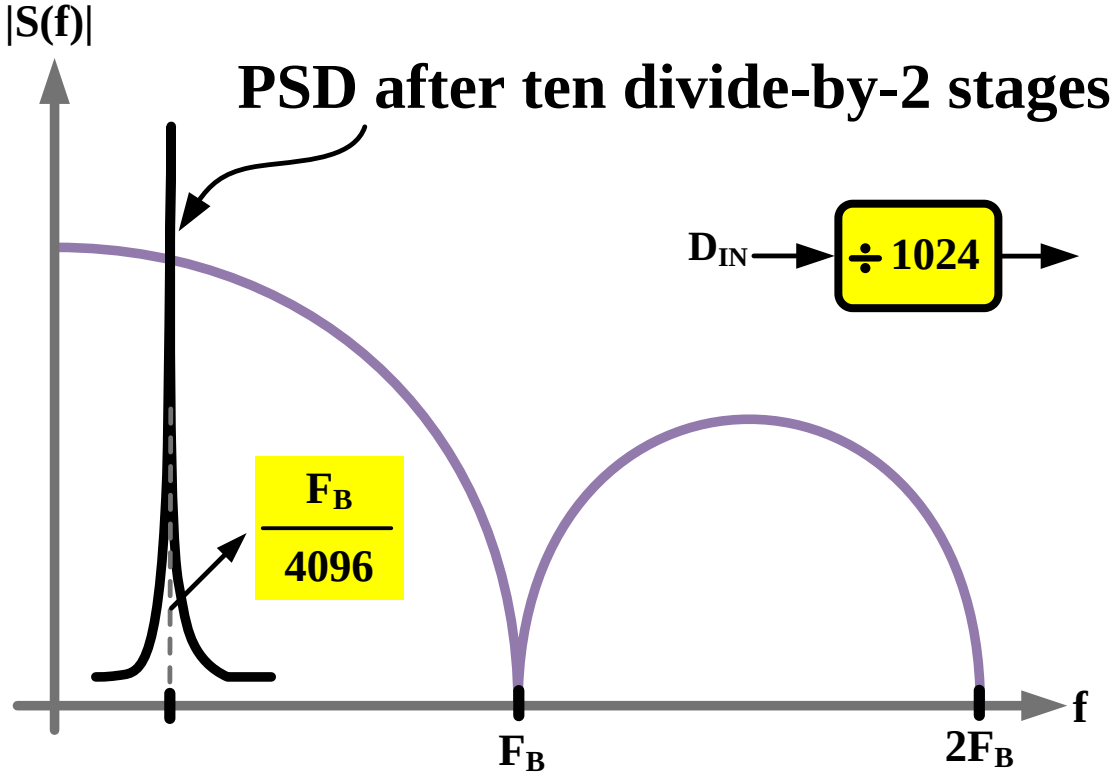
PSD After First Divide-by-2 Stage



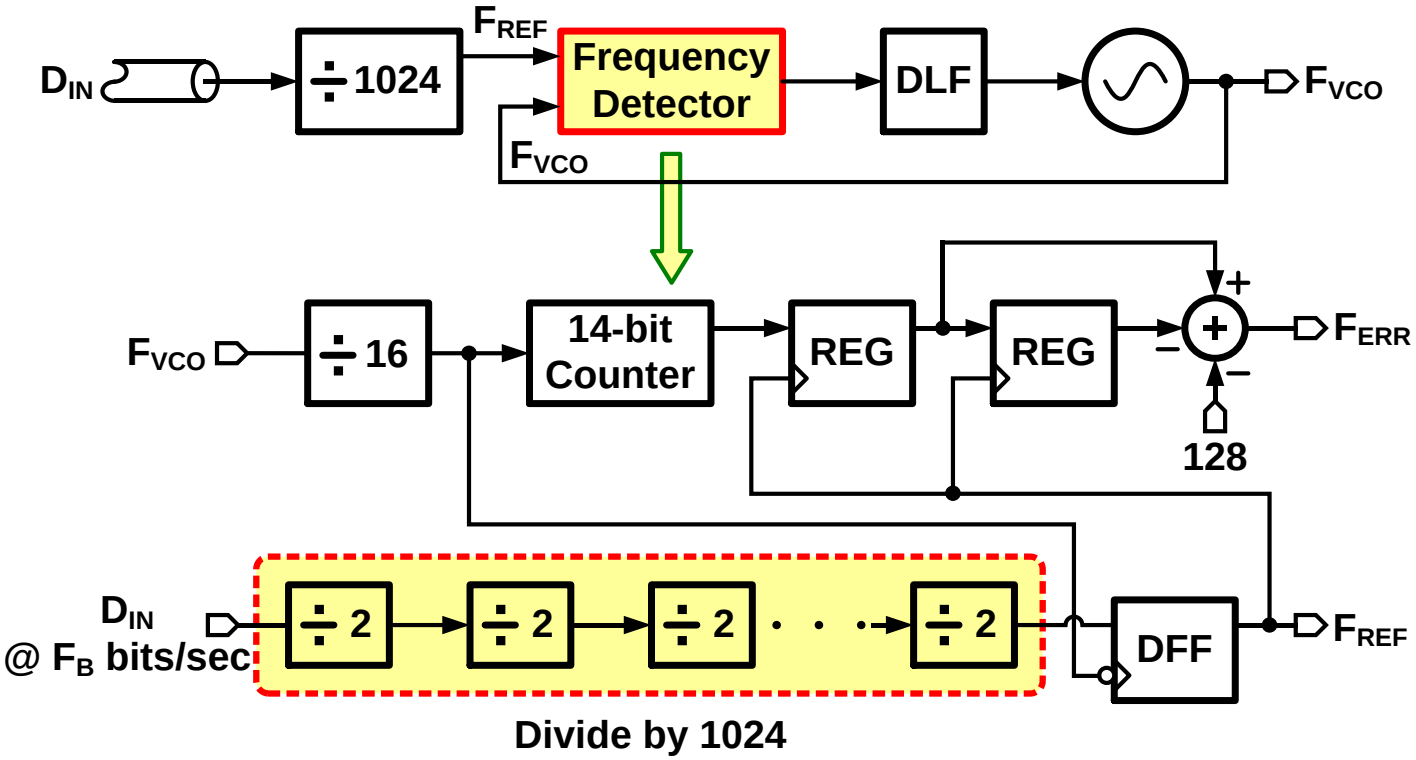
PSD After Two Divide-by-2 Stages



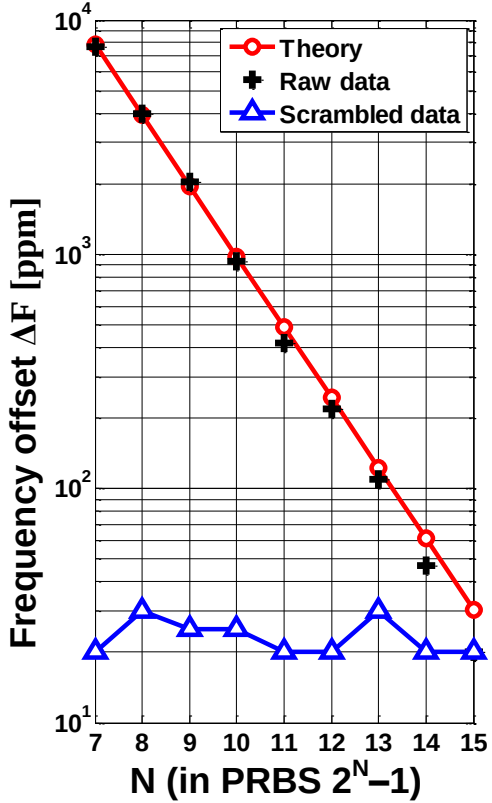
PSD After Ten Divide-by-2 stages



Frequency Locking Loop[28]



FLL only Mode

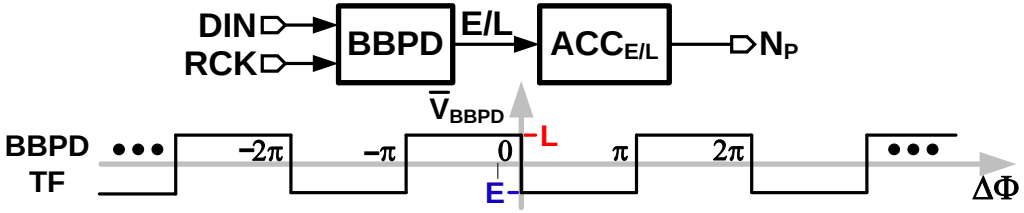


- PRBS patterns have *imbalance* in the 1→0, 0→1 transitions

$$\textbf{Theoretical } \Delta F \textbf{ [ppm]} \approx \frac{10^6}{2^N}$$

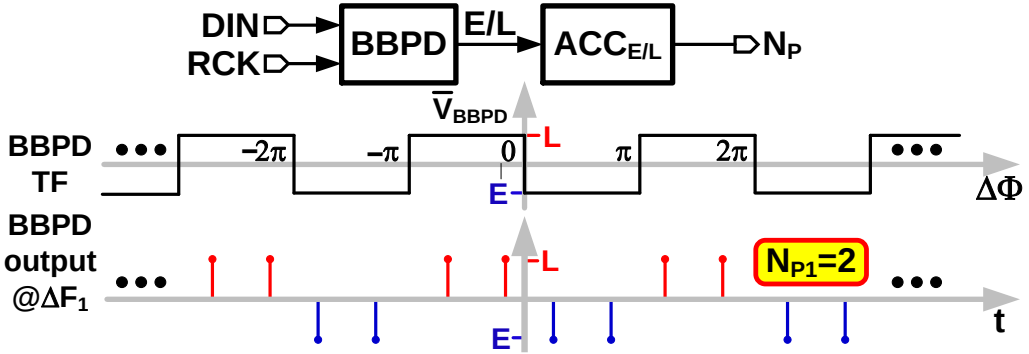
- Ex: PRBS7 imbalance = 1/127
- Improved by scrambling

Principle of Frequency Detection$_{1/4}$



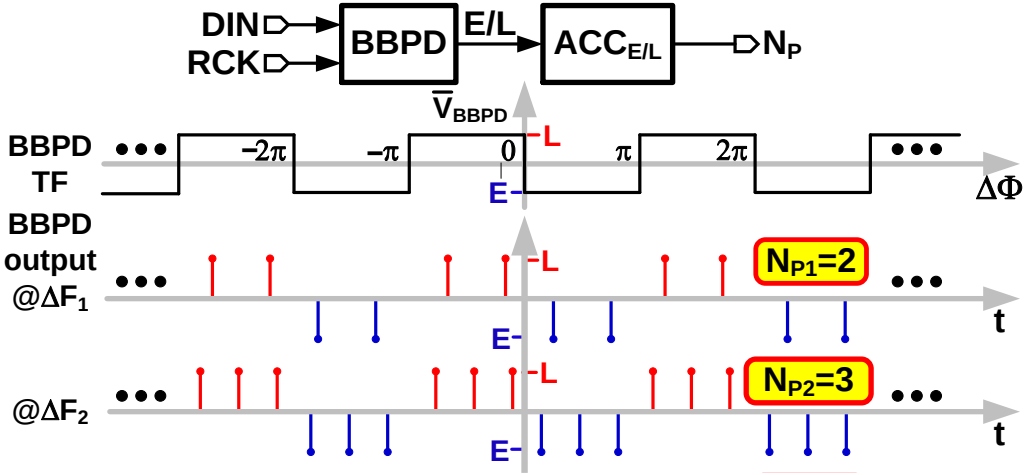
- BBPD output changes sign at $\Delta\Phi=n\pi$

Principle of Frequency Detection$_{2/4}$



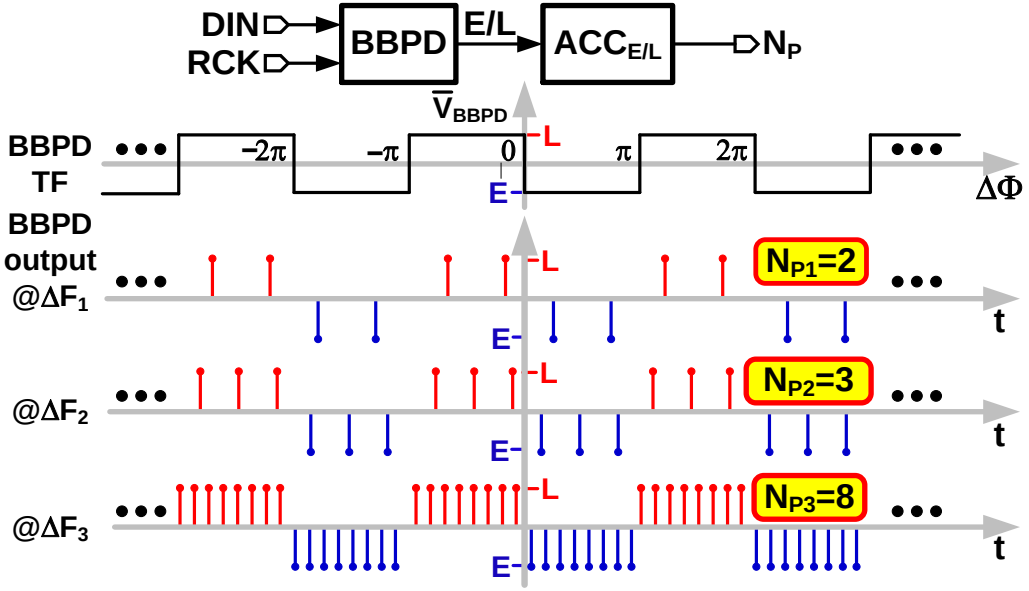
- N$_P$ is consecutive Early or Late number in π interval

Principle of Frequency Detection$_{3/4}$



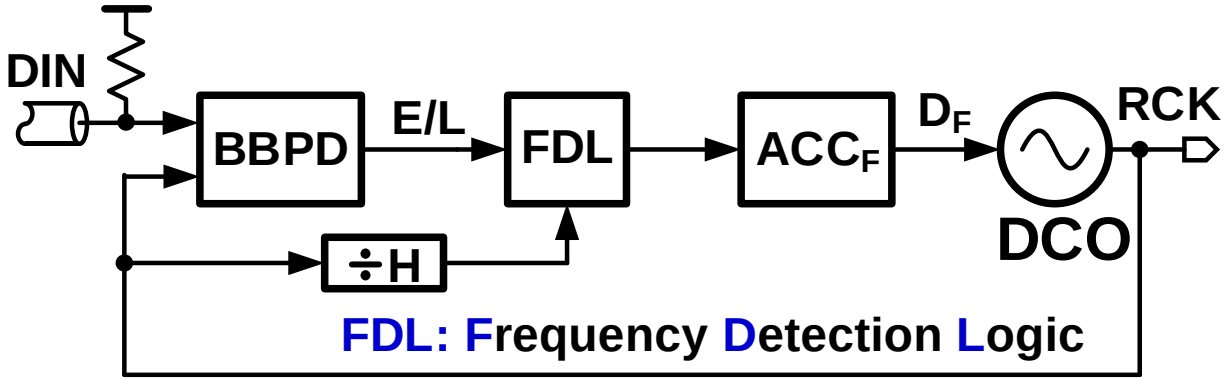
$\Delta F_2 < \Delta F_1$ leads to $N_{P2} > N_{P1}$

Principle of Frequency Detection 4/4



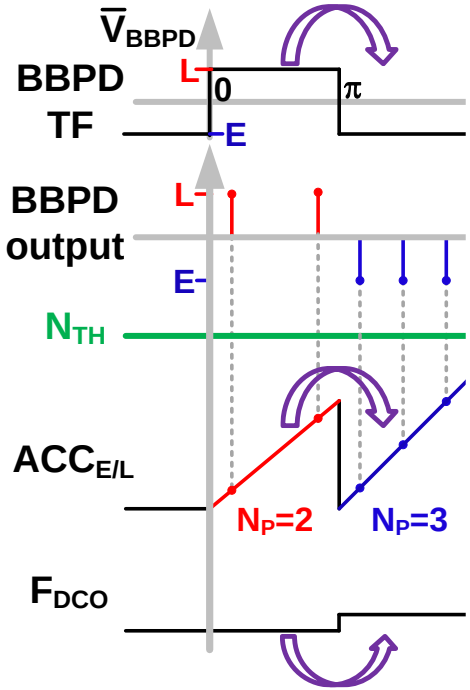
ΔF∝1/N_P → Can be used for frequency detection

BBPD-based Frequency-Locked Loop[29]



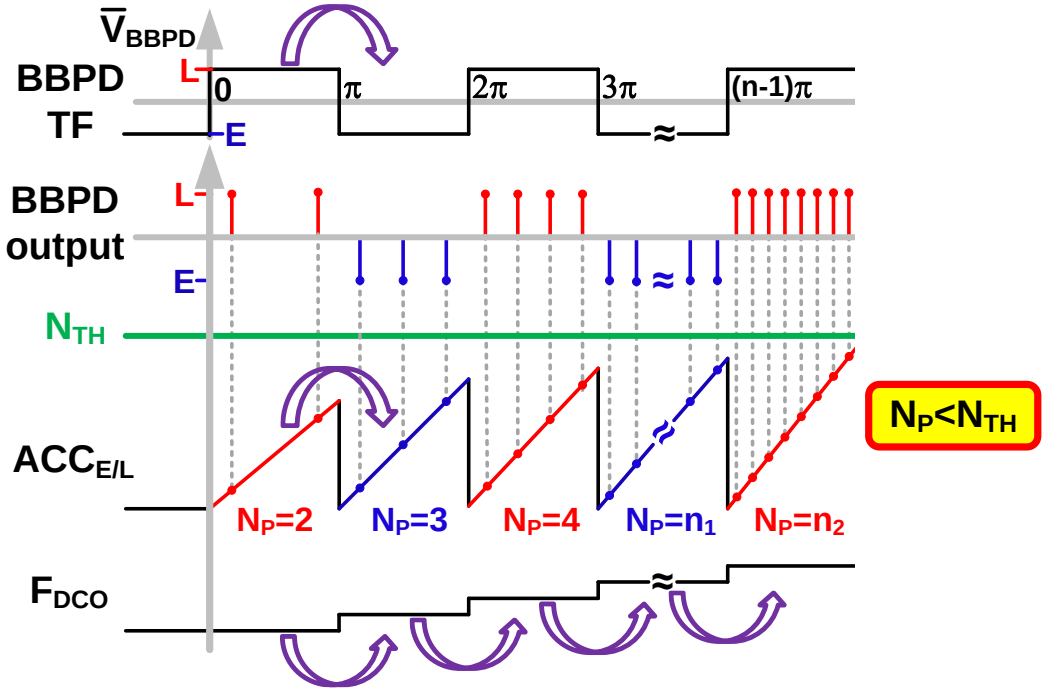
- No explicit frequency detector
- Immune to input transition density ρ
- Unlimited frequency acquisition range

Frequency Acquisition Process$_{1/3}$



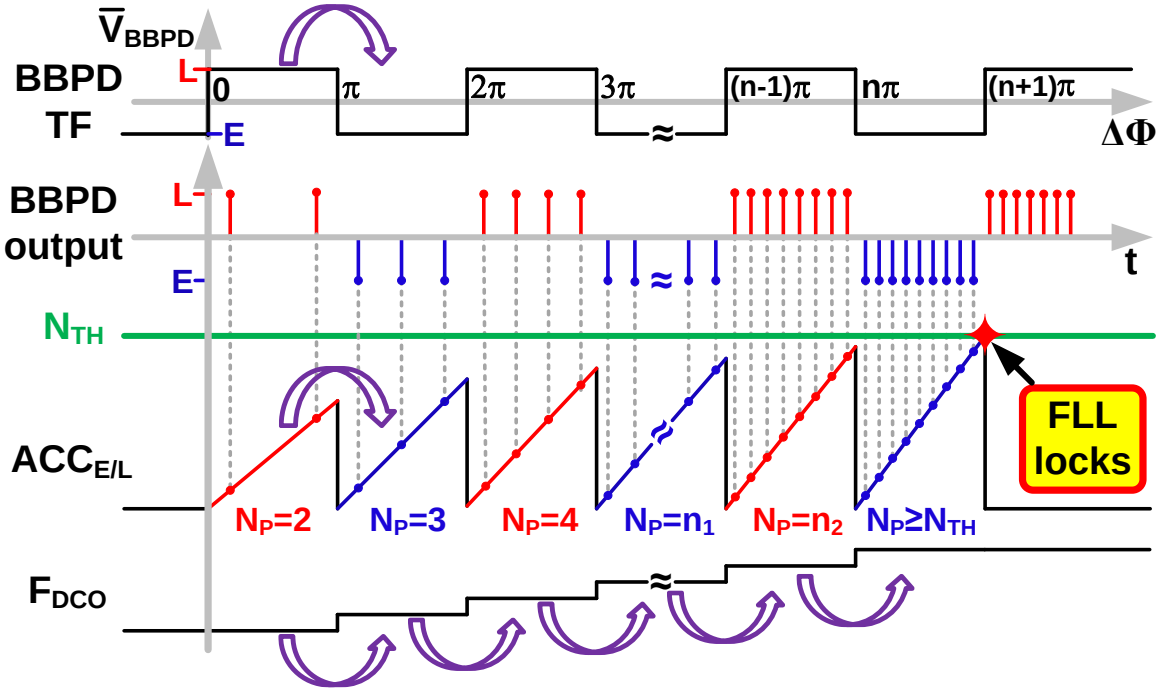
DCO starts from its lowest frequency

Frequency Acquisition Process$_{2/3}$



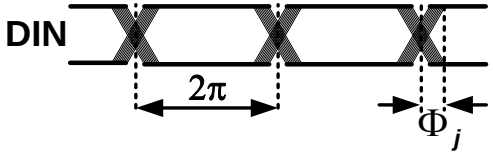
Increment F_{DCO} at each E→L or L→E transition

Frequency Acquisition Process$_{3/3}$



Lock is achieved when $N_P \geq N_{TH}$

Transition Density Dependence w/ Jitter



$$N_{TH} = N_P = \rho \frac{F_{DIN}}{\Delta F} \frac{\pi - \Phi_j}{2\pi}$$

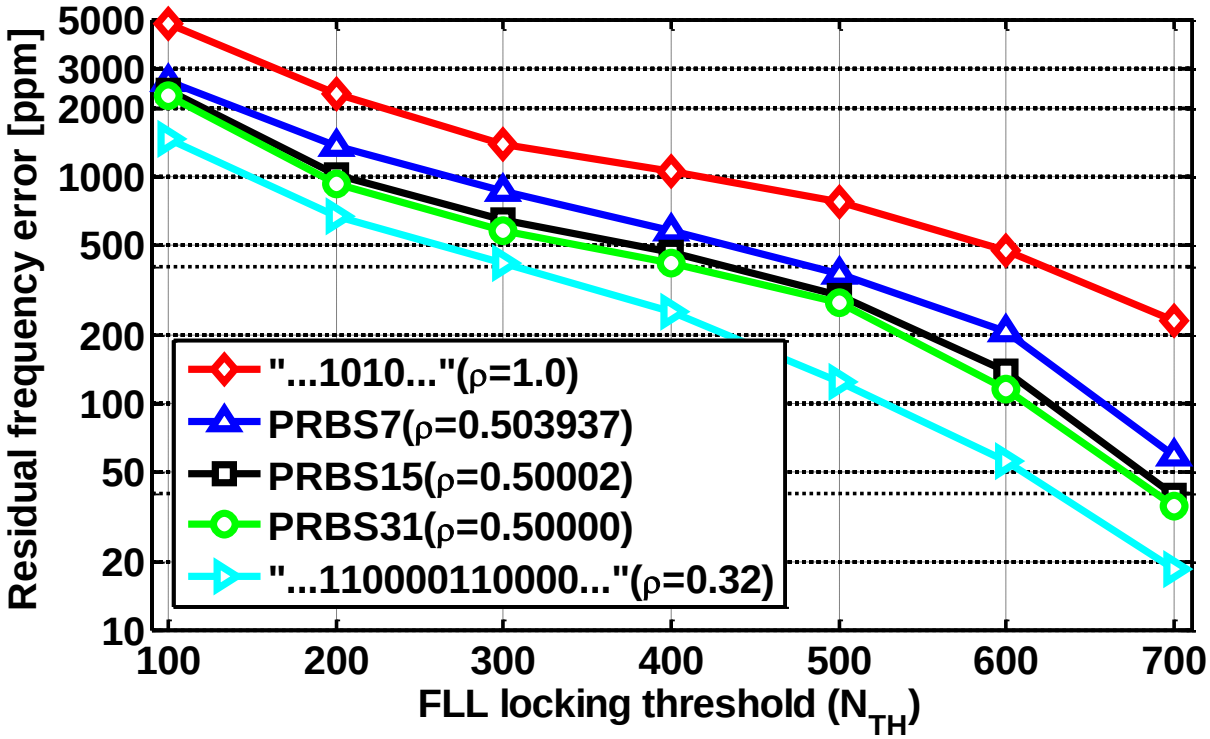
$$\Rightarrow \frac{\Delta F}{F_{DIN}} = \frac{\rho}{N_P} \frac{\pi - \Phi_j}{2\pi}$$

$N_{TH} = 500$

ρ	0.1	0.5	1.0
$\Phi_j=0$ $\Delta F/F_{DIN}$ [ppm]	100	500	1000
$\Phi_j=\pi/4$ $\Delta F/F_{DIN}$ [ppm]	75	375	750

$N_{TH}=N_P=500$, $\Delta F<1000$ppm when $0\le\rho\le1$

Residual Frequency Error



- N_{TH}≥500, residual frequency error within 1000ppm

Summary

- Basic analog/digital clock and data recovery design for given jitter metrics
- Benefits analog and digital CDRs are exploited in hybrid analog/digital CDRs
- Multi-lane CDRs with local sampling clock & global low jitter recovered clock
- CDRs in repeaters with decoupled JTRAN & JTOL bandwidth
- FDs with simple counting of received signal transitions or !!PD outputs

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1. C. Hogge, "A self correcting clock recovery circuit," J. Lightwave Technol., pp. 1312-1314, Dec. 1985.
2. L. DeVito, "A versatile clock recovery architecture and monolithic implementation," in Monolithic Phase-Locked Loops and Clock Recovery Circuits, B. Razavi, Ed. Wiley-IEEE Press, 1996, pp. 405-420.
3. J. Alexander, "Clock recovery from random binary signals," Electr. Lett., pp. 541-542, Oct. 1975.
4. J. Lee and B. Razavi, "Analysis and modeling of bang-bang clock and data recovery circuits," *IEEE J. Solid-State Circuits,* pp. 1571-1580, Sep. 2004.
5. R. Walker, et al., "A 2-Chip 1.5 Gigabaud serial link interface," *IEEE J. Solid-State Circuits*, pp. 1805-1811, Dec. 1992.
6. J. Sonntag and J. Stonick "A digital clock and data recovery architecture for multi-gigabit/s binary links", *IEEE J. Solid-State Circuits*, pp.1867-1875, Aug. 2006.
7. M. Talegaonkar, R. Inti, P. Hanumolu, "Digital clock and data recovery circuit design: Challenges and tradeoffs", *IEEE Custom Integrated Circuits Conference , 2011.*
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9. S. Sidiropoulos and M. Horowitz, "A semidigital dual delay-locked loop," *IEEE J. Solid-State Circuits*, 1683–1692, 1997.

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