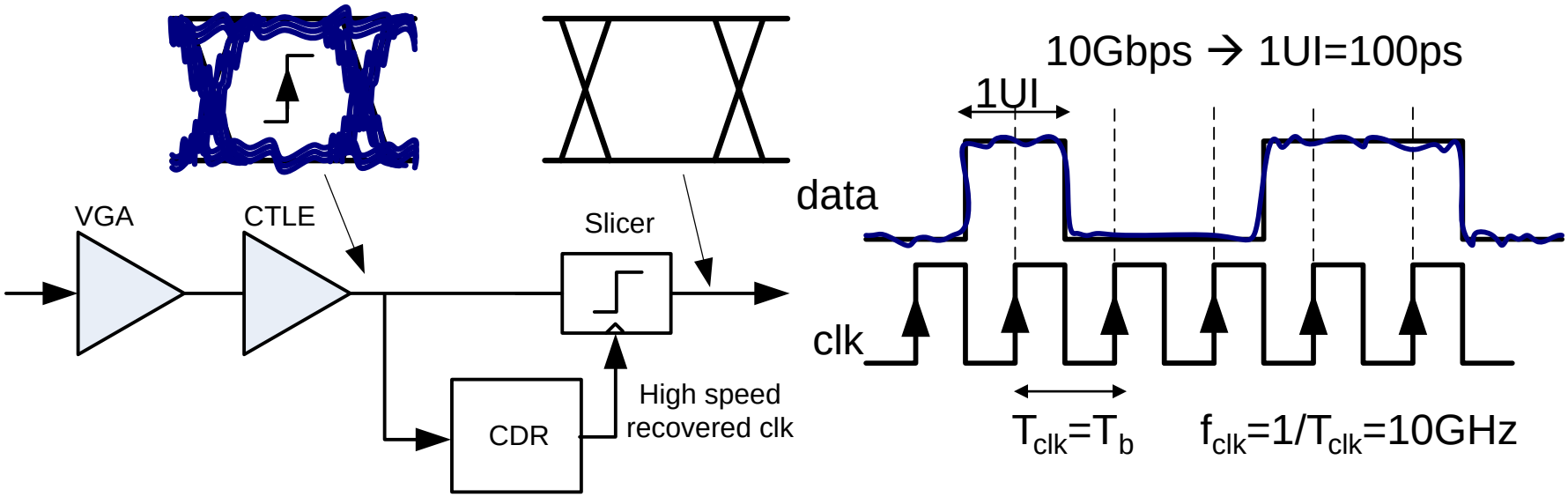
Clock and Data Recovery

Lecture 8

Clock & Data Recovery



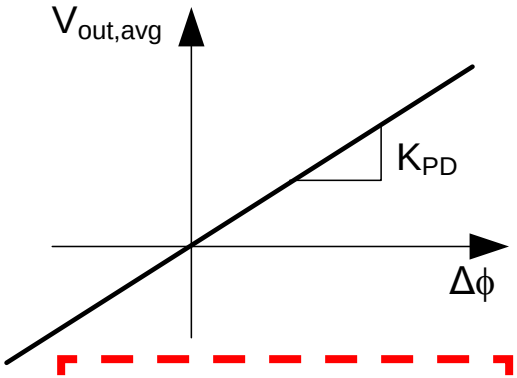
- The CDR senses the equalizer output and produces a clock typically with the same frequency centered at the eye opening to minimize the BER
- The slicer (decision circuit) is a flip-flop driven by the recovered clock
- Re-timing the data with the recovered clock reduces the jitter accumulated on the received data
- To produce a clock centered at the eye opening the CDR can employ a PD that compares the recovered clock with the input **random data**

Common CDR Architectures

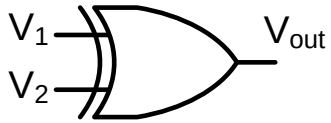
- Feedback-based CDRs can be classified according to their **architecture**:
  - PLL-based CDRs
    - Reference-less CDRs or CDRs with External Reference Clock
  - Delay Lock Loop (DLL) based CDRs
  - Phase Interpolator (PI) based CDRs
  - All Digital CDRs
- Feedback-based CDRs can be classified according to their **nature** into:
  - Linear/non-linear (band-bang) CDRs
- Feed Forward-based:
  - Over-sampling based CDRs

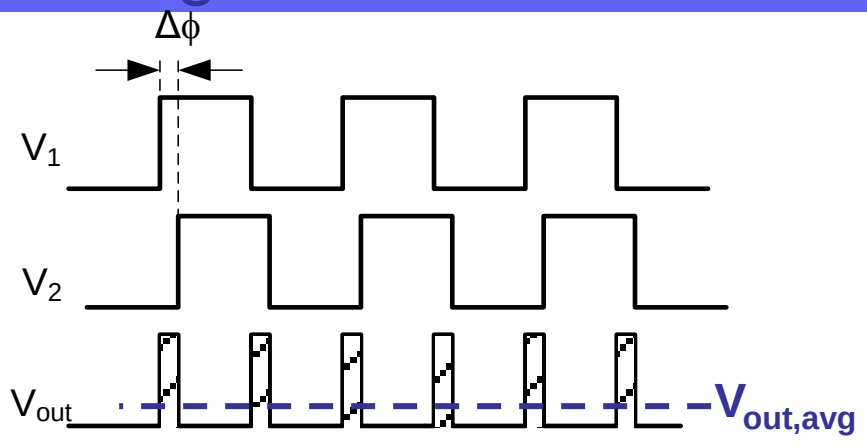
[Ref]: "Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery," IEEE Circ. & Sys. Magazine, 2008

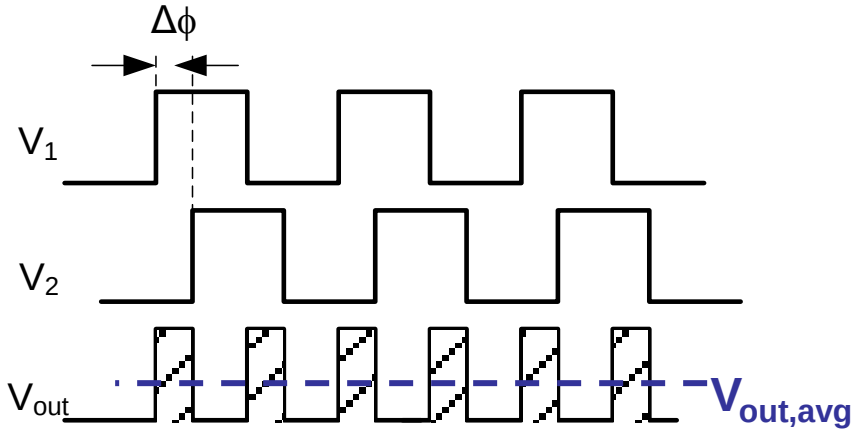
PLL-based CDRs: XOR as a Phase Detector for Periodic Signals



$$V_{out,avg} = K_{PD}\Delta\phi$$

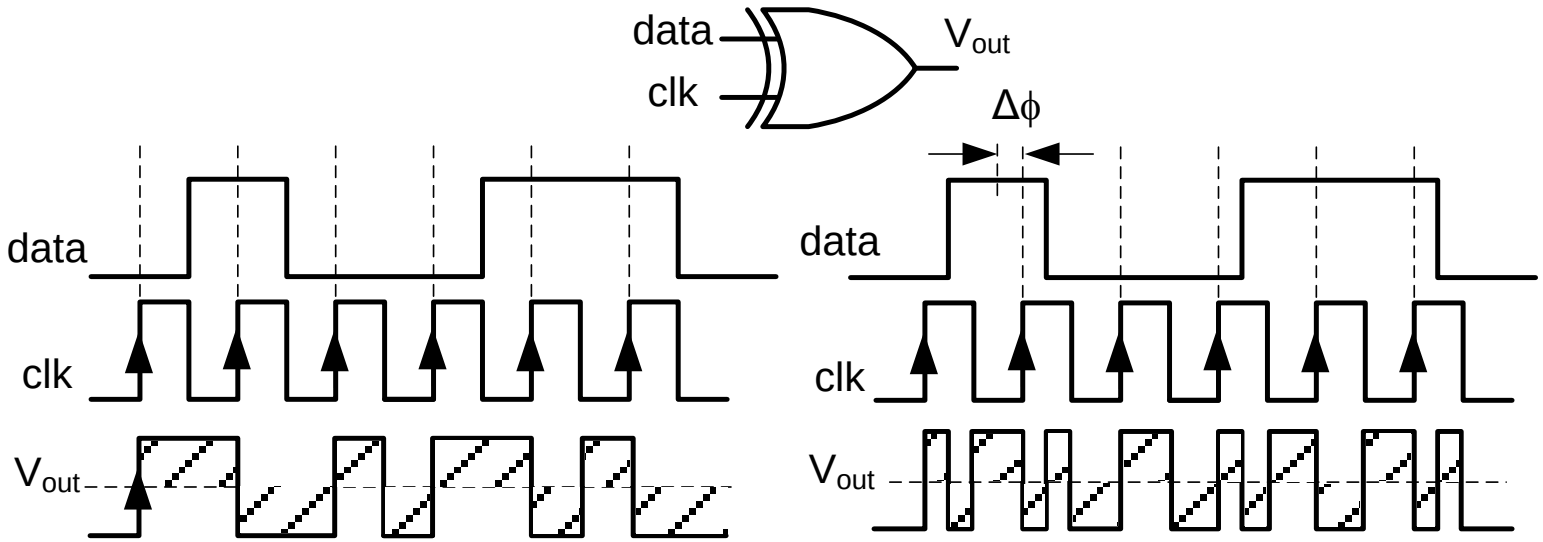






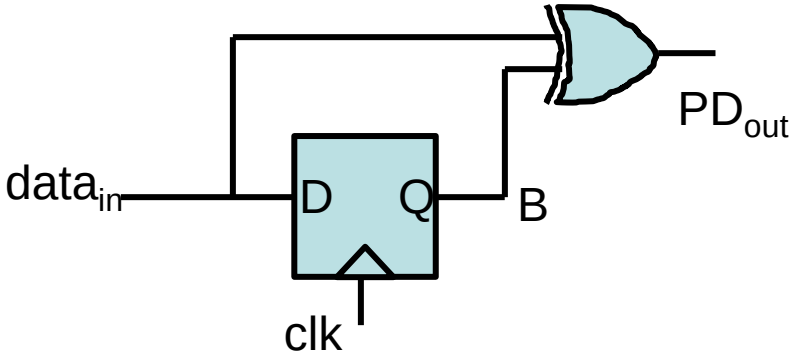
- A Phase detector is circuit which produces an output voltage V_{out} with an average value proportional to phase difference $\Delta\phi$ between its inputs
- The gain of the phase detector, K_{PD}, is the slope of the PD characteristics

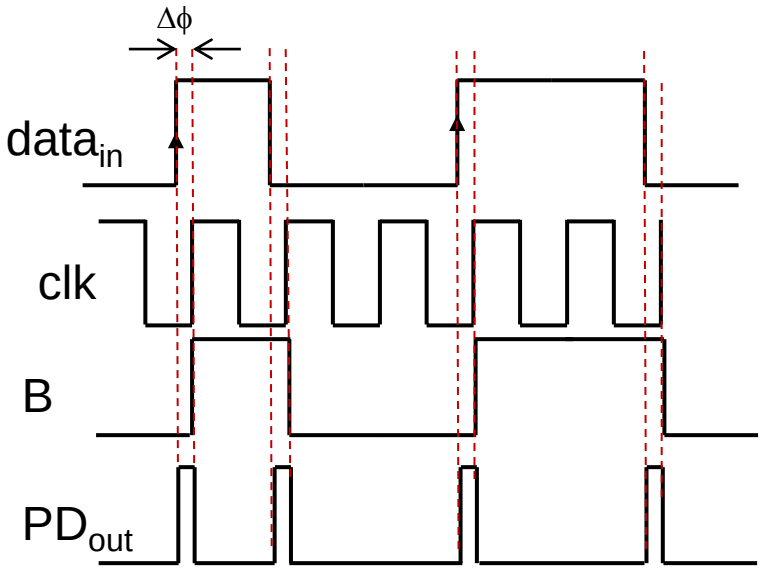
Random Data PDs: XOR



- If clock and data are aligned: the XOR produces a zero average at the output if the 1's and 0's occur with equal probabilities
- If clock is late by $\Delta\phi$: the XOR produces a zero average at the output if the 1's and 0's occur with equal probabilities
- The XOR fails to operate as a PD for random data

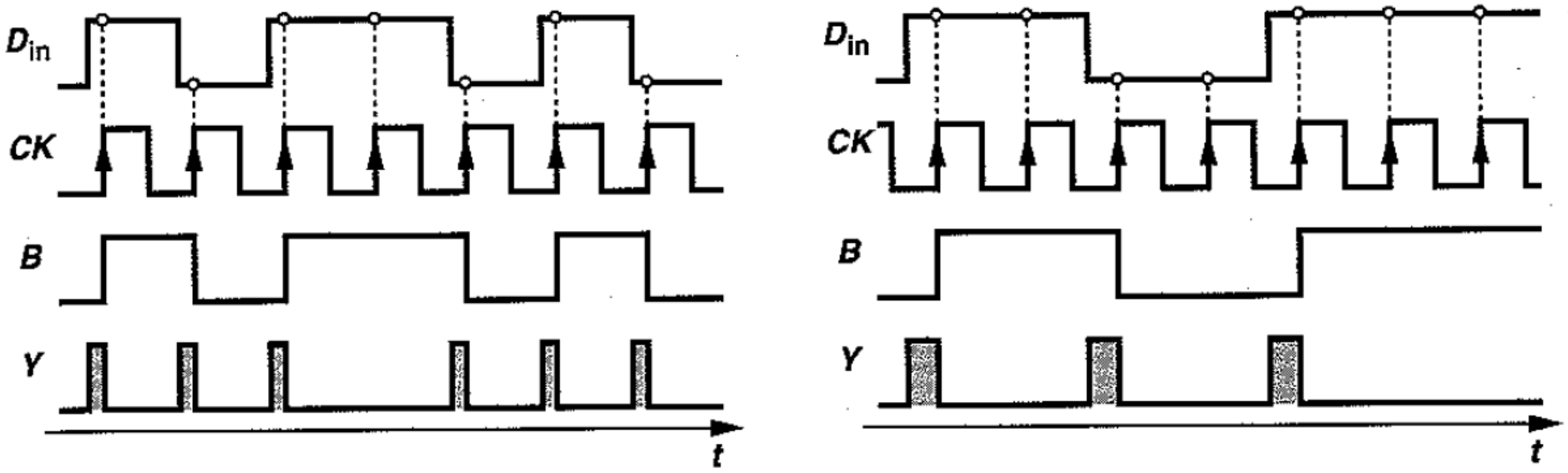
Linear Detectors: Hogge Phase Detector





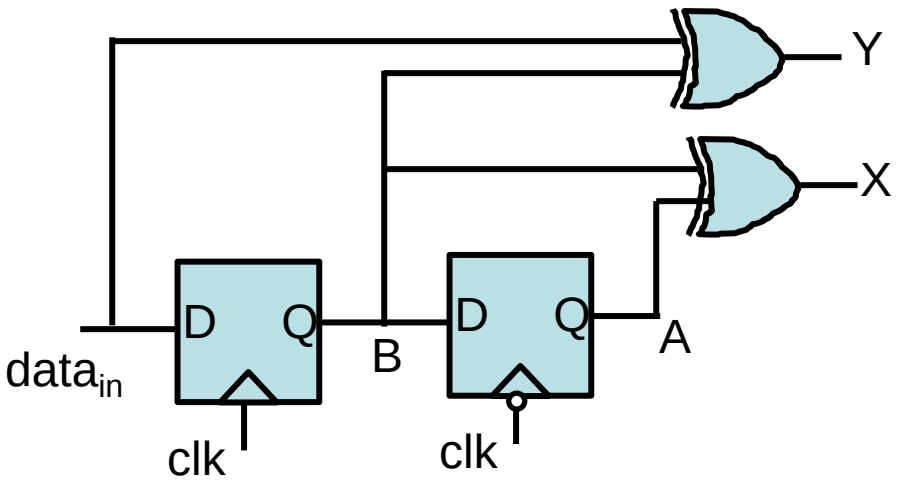
- Sampling the data with the clock produces a delayed version of the data (B)
- The output of the XOR is pulses which only occur at the data transitions → "edge detection"
- The width of the output pluses is linearly proportional to the delay between data and clock edges→ linear phase detector
- The average value of the output is a function in the phase difference as well as the transition density failing to uniquely represent the phase difference

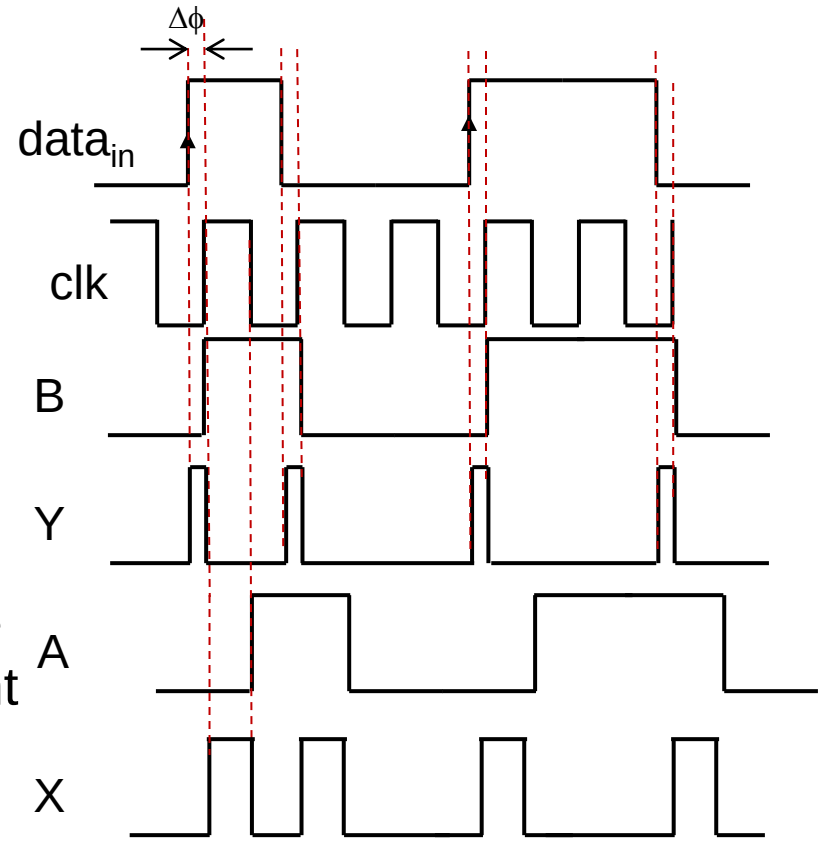
Linear Detectors: Hogge Phase Detector



- The 2 outputs have the same average value although the phase error is doubled in the right graph
- 2 different phase errors having the same average output could result in a false lock

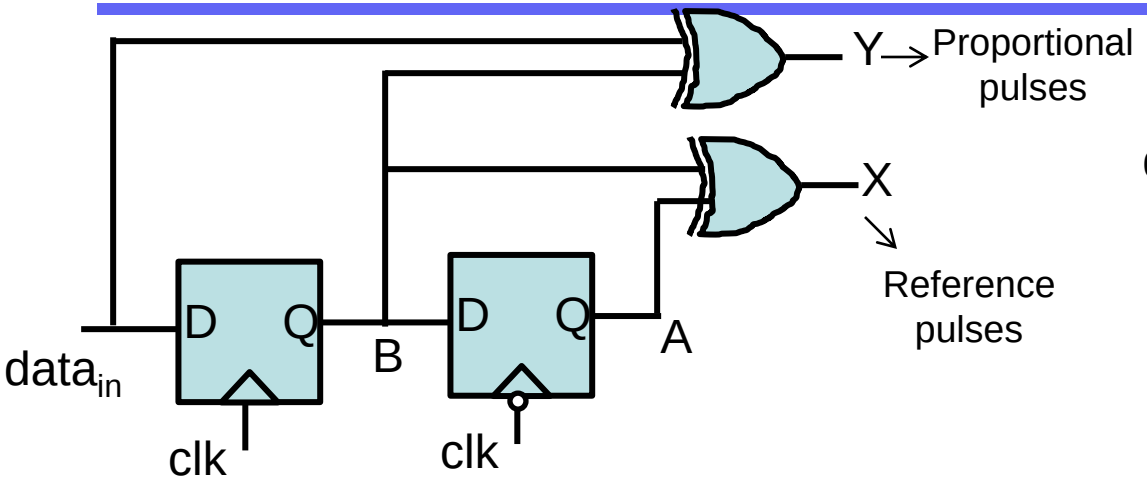
Linear Detectors: Hogge Phase Detector

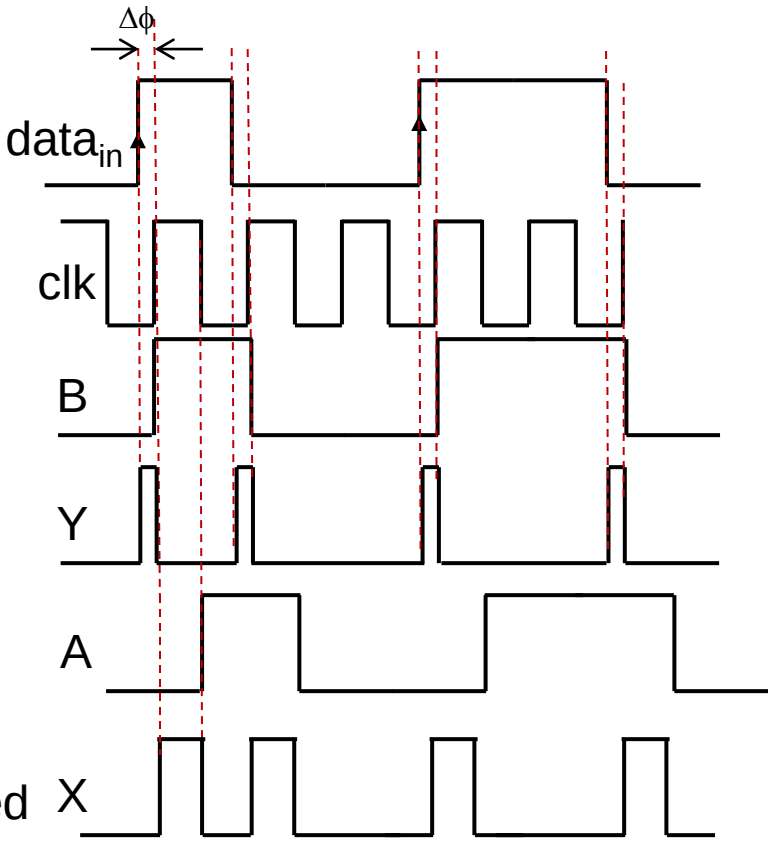




- To eliminate the pattern dependency, reference pulses are generated at the data transitions which have a constant width
- If the delayed signal B is re-sampled with the falling clock edge and the result is XOR-ed with B, pulses $T_{clk}/2$ wide are produced at data transitions

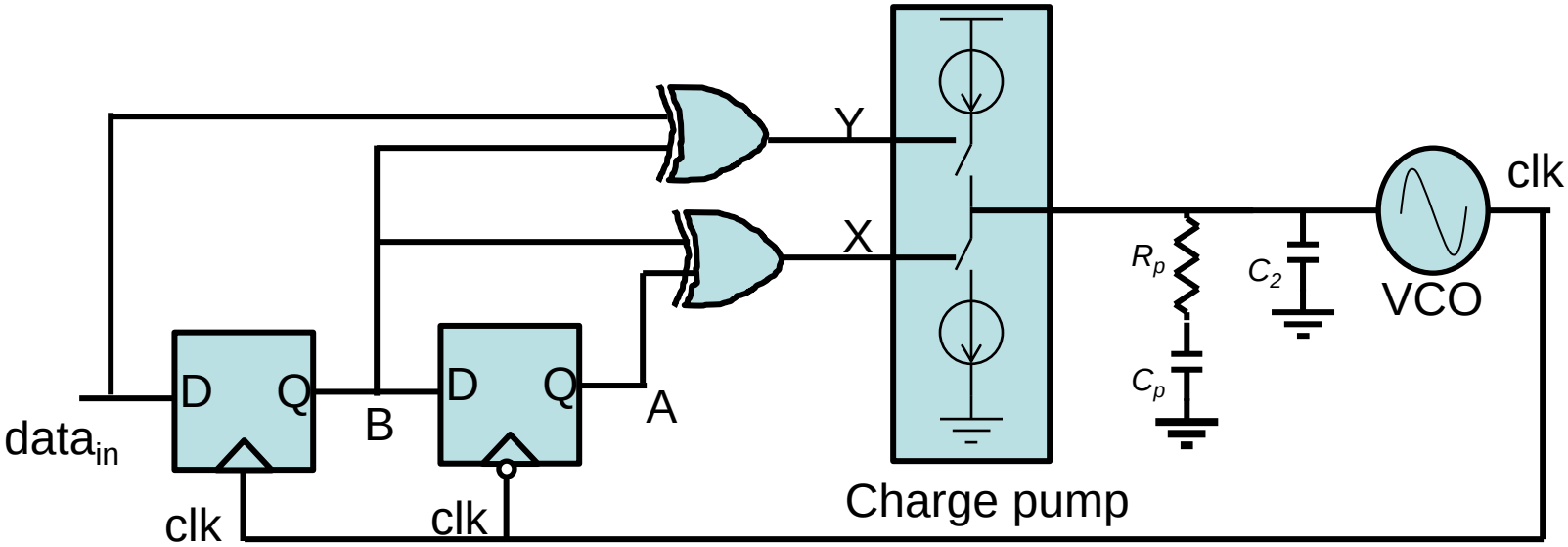
Linear Detectors: Hogge Phase Detector





- The difference between the area under the 2 signals X and Y is considered the PD output
- Under lock condition X and Y have pulses with equal width
- The DFF inside the Hogge phase detector automatically re-times the data with the recovered clock
- Disadvantage: Linear phase detectors need to handle very narrow pulses which requires circuits with very wide bandwidths

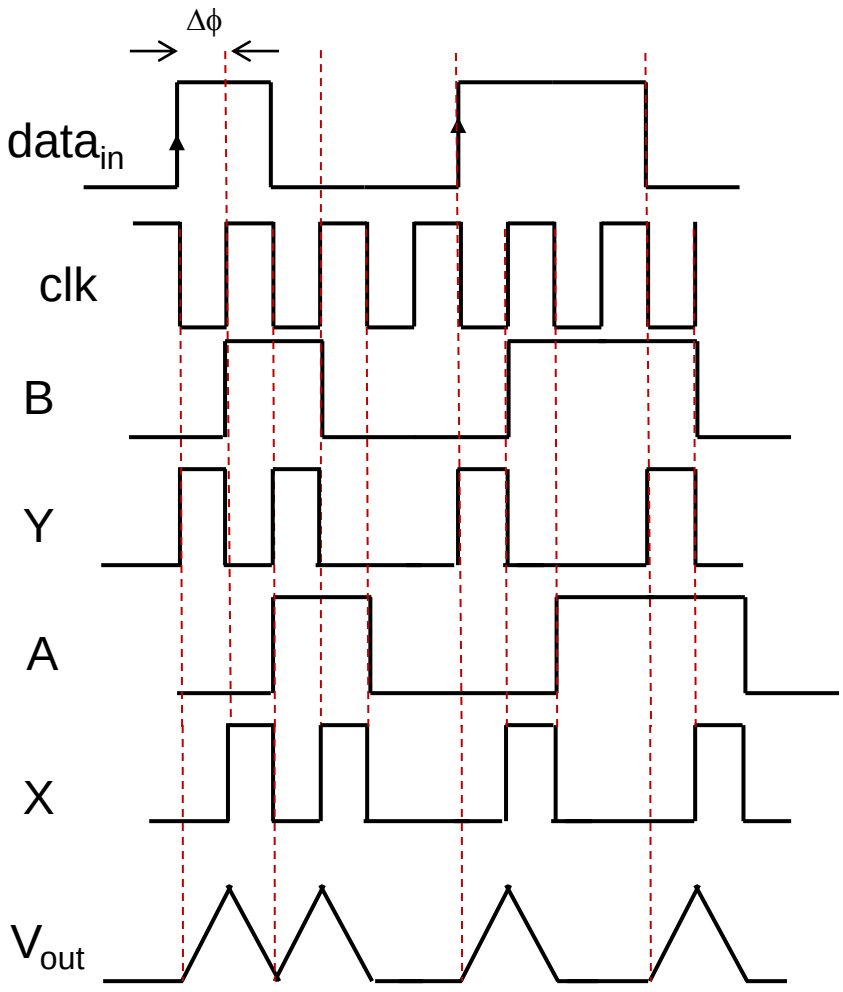
CDR Based on Hogge PD



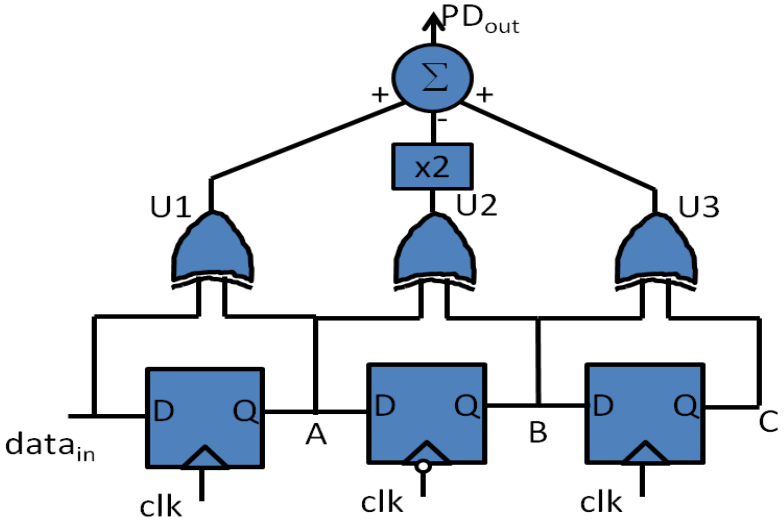
- The Y and X pulses can be subtracted and averaged using a charge pump and loop filter as in charge pump PLLs
- If the clock leads the data: the PD output avg(Y-X) will generate negative current pulse, reducing the VCO control voltage and running the VCO at a slower frequency until the phase of the clock aligns with the data reducing the phase error to zero
- As the Phase difference approaches zero the average of the PD output remains unchanged with little activity

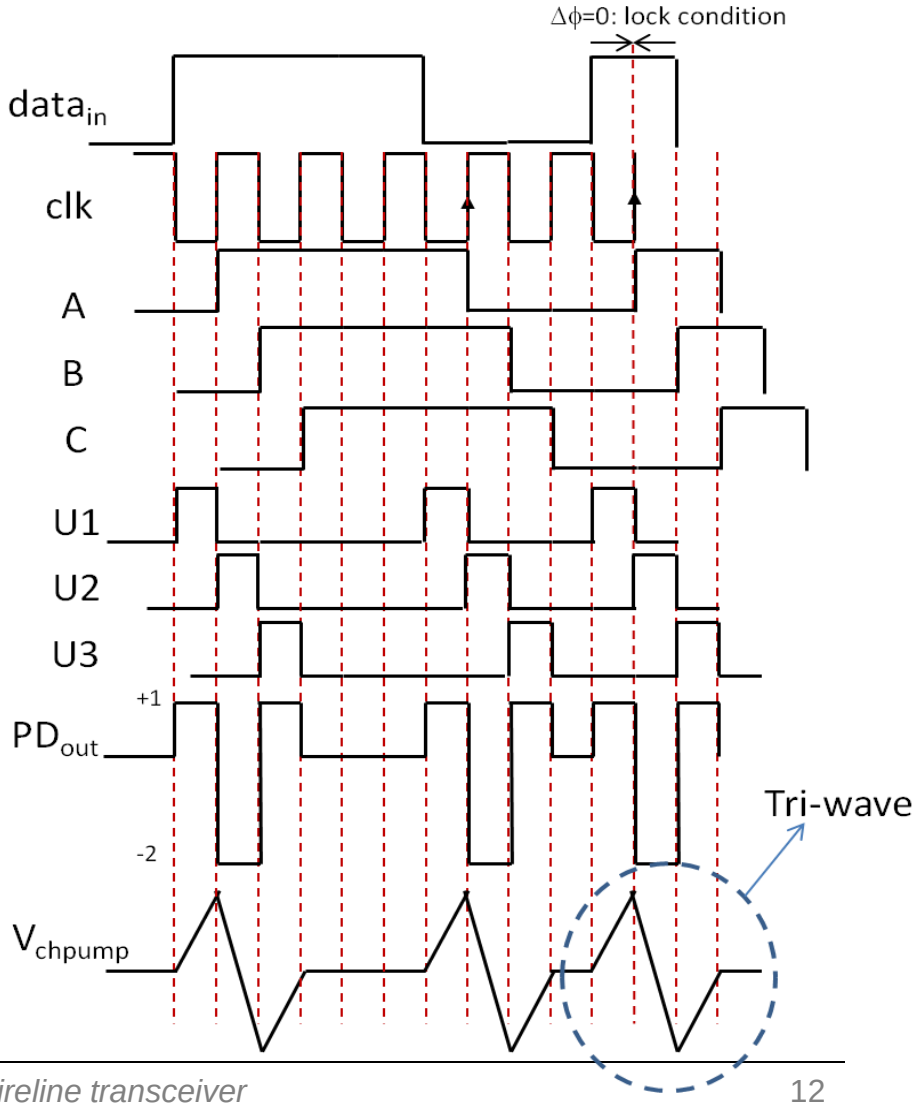
CDR Based on Hogge PD: Under lock Condition

- The drawback of this Hogge PD is the $T_{clk}/2$ skew between the two XOR outputs
- When the proportional pulses appear the top current source turns on for $T_{clk}/2$ forcing V_{out} to rise by $I_{CP}/C_P*T_{clk}/2$
- Following that the reference pulse turns on the bottom current source bringing down the V_{out} to its original value
- The triangular pulse that is generated has a non-zero net area, which disturbs the VCO phase (proportional to the integral of the control voltage)



Tri-wave Phase Detector



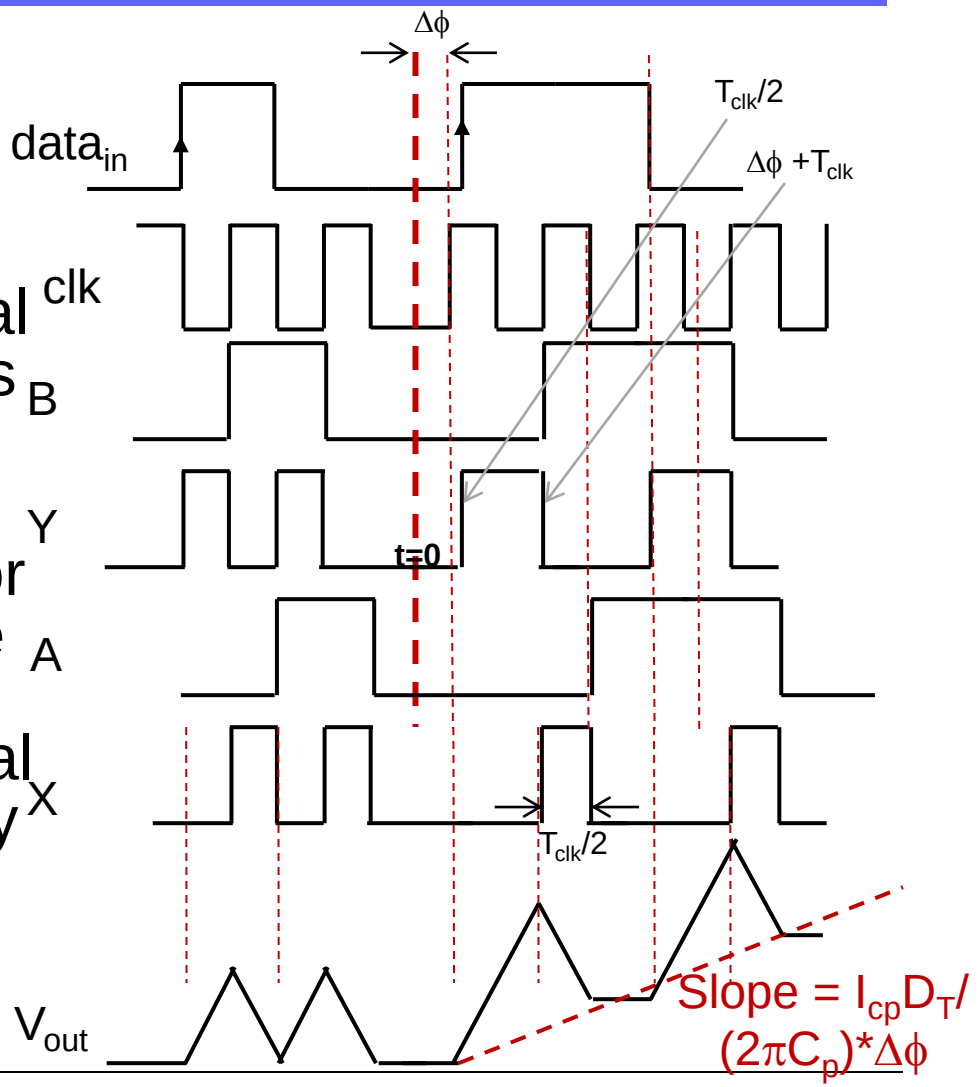


- The tri-wave phase detector reduces this problem; by replacing the triangular correction pulses with tri-waves whose net is 0 during the lock condition
- Pulses out of U1 & U3 are weighted by1 while pulses out of U2 are weighted by -2

Hogge CDR Loop Dynamics: CP Model

- Step response is obtained by applying a phase step $\Delta\phi u(t)$ to one of the PD inputs
- The width of the proportional pulses is $T_{clk}/2+\Delta\phi$, whereas the reference pulses are $T_{clk}/2$
- Note that the phase detector will have a zero slope in the absence of data transitions, hence its gain is proportional to the data transition density D_T

$$V_{step}(t) = \frac{I_{cp} D_T}{2\pi C_p} t \times \Delta\phi u(t)$$



Hogge CDR Loop Dynamics: CP Model

- For a random signal with equal probabilities for 1s and 0s D_T=0.5
- Impulse response is the derivative of the step response

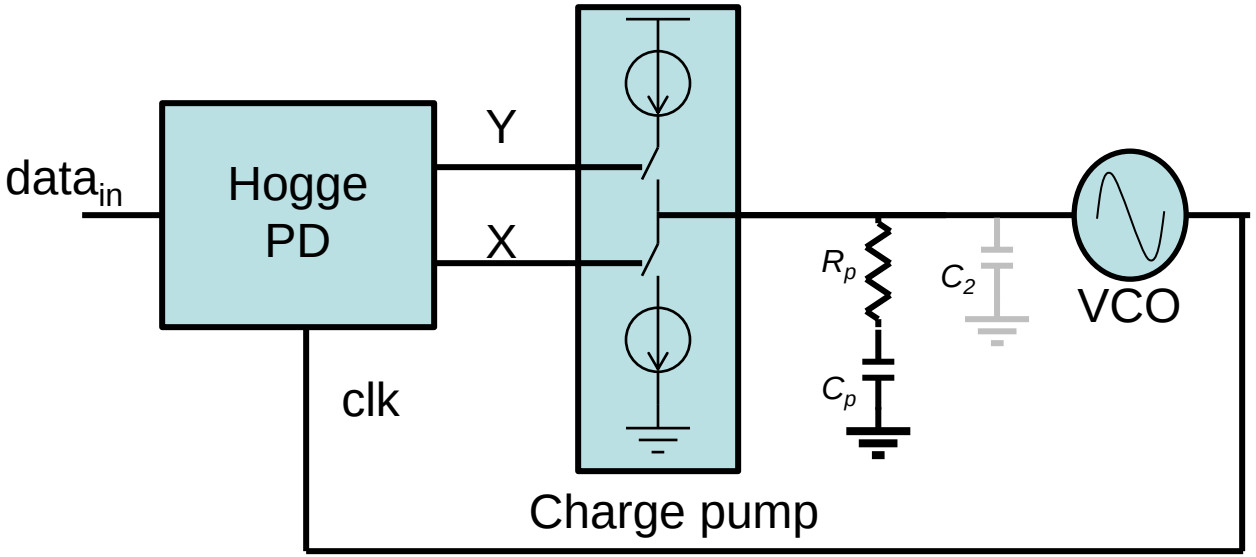
$$h_{PD\_CP}(t) = \frac{I_{cp} D_T}{2\pi C_p} u(t)$$

- Transfer function $H_{PD\_CP}(s)$:

$$H_{PD\_CP}(s) = \frac{V_{out}}{\Delta\phi}(s) = \frac{I_{cp} D_T}{2\pi} \frac{1}{sC_p}$$

- The equation is very similar to the charge pump PLL except for the effect of the data transition density
- The CP-PLL handles periodic signals and guarantees a transition each clock cycle, i.e. D_T=1

Hogge CDR Loop Dynamics



- Replacing the PD & charge pump with their linear model, one can write the expression of the CDR open loop gain:

$$H(s)\Big|_{open} = \frac{\phi_{out}}{\phi_{in}}(s)\Big|_{open} = \frac{I_{cp}D_T}{2\pi}\left(R_p + \frac{1}{sC_p}\right)\frac{K_{VCO}}{s}$$

- Adding a resistor in series with the capacitor adds a zero to the loop gain and helps stabilize the CDR

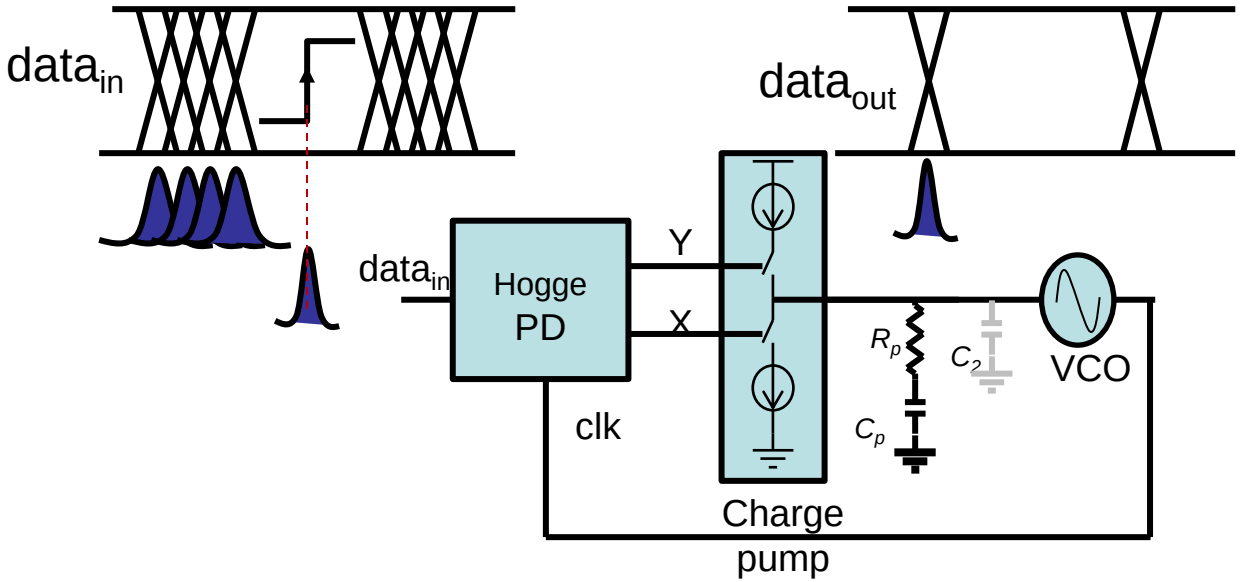
Hogge CDR Loop Dynamics (Cont'd)

$$H(s)\big|_{closed} = \frac{\phi_{out}}{\phi_{in}}(s)\bigg|_{closed} = \frac{I_{cp}D_T K_{VCO}/2\pi C_p\left(1+sC_pR_p\right)}{I_{cp}D_T K_{VCO}/2\pi C_p + I_{cp}D_T K_{VCO}R_p/2\pi\, s + s^2}$$

$$\omega_n = \sqrt{\frac{I_{CP}D_T K_{VCO}}{2\pi C_p}},\ \zeta = \frac{R_p}{2}\sqrt{\frac{I_{CP}D_T C_p K_{VCO}}{2\pi}}$$

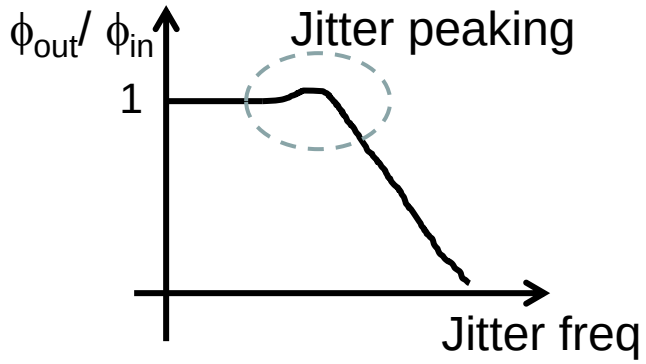
- If the phase of the input data varies slowly (s~0) the output phase tracks the input phase with a unity gain
- As the rate of change of the input phase increases the output phase fails to track the input, i.e. CDR will have a LPF response
- As $I_{CP}K_{VCO}$ decreases ζ decreases and stability degrades
- The loop settling time is proportional to $1/(\zeta\omega_n)=4\pi/R_pI_{CP}D_TK_{VCO}$

Jitter Transfer in CDRs



- Jitter Transfer: represents the output jitter as the input jitter is varied at different rates (frequencies) – same as PLL closed loop transfer function
- If the input jitter varies slowly then the output should follow the input to ensure phase locking and reduce bit errors
- If the input jitter varies rapidly the CDR should filter the jitter to avoid having a jittery clock and output eye
- The CDR jitter transfer function exhibits a low pass response (similar to PLLs)

Jitter Transfer in CDRs (Cont'd)



- ISI is one of the main sources of high frequency jitter, and should be removed by equalization before clock recovery → CDR can't track it
- SONET OC-192 standard specifics a BW of 120KHz, and requires the jitter peaking to be less than 0.1dB
- Jitter peaking: is defined as the amount of peaking in the jitter transfer function
- Jitter peaking is a very important spec. for repeaters in long-haul networks where 10 or more repeaters may be cascaded to re-generate the signal eliminating the non-idealities of the fiber. This is important to limit the overall system jitter bandwidth

Jitter Transfer in CDRs: Loop BW

$$H(s)=\frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \longrightarrow \omega_{3dB}^2=\left(1+2\zeta^2+\sqrt{4+\left(1+2\zeta^2\right)^2}\right)\omega_n^2$$

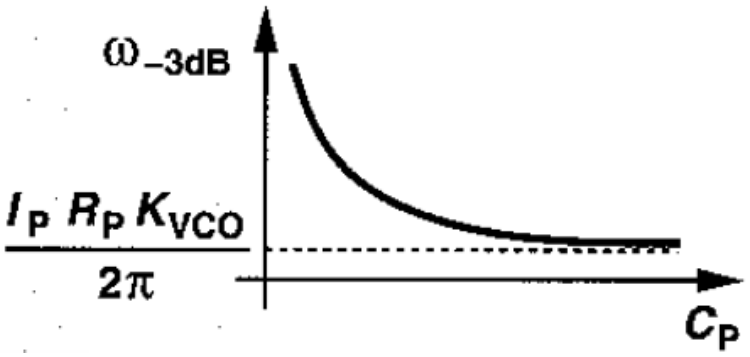
$$\omega_n=\sqrt{\frac{I_{CP}D_T K_{VCO}}{2\pi C_p}},\ \zeta=\frac{R_p}{2}\sqrt{\frac{I_{CP}D_T C_p K_{VCO}}{2\pi}}$$

- To achieve a small loop BW ω_n must be decreased without decreasing ζ due to loop stability ($\zeta>1/\sqrt{2}$ for a critically damped system)
- If ω_n is decreased by via $I_{CP}*K_{VCO}$ the loop stability will also be affected
- C_p is the only parameter that can be used to decrease the loop bandwidth without compromising stability→ large off chip capacitors can be employed to achieve small loop BWs

Jitter Transfer in CDRs: Loop BW

- For very large loop capacitors, ω_n will be very small and the square term can be neglected

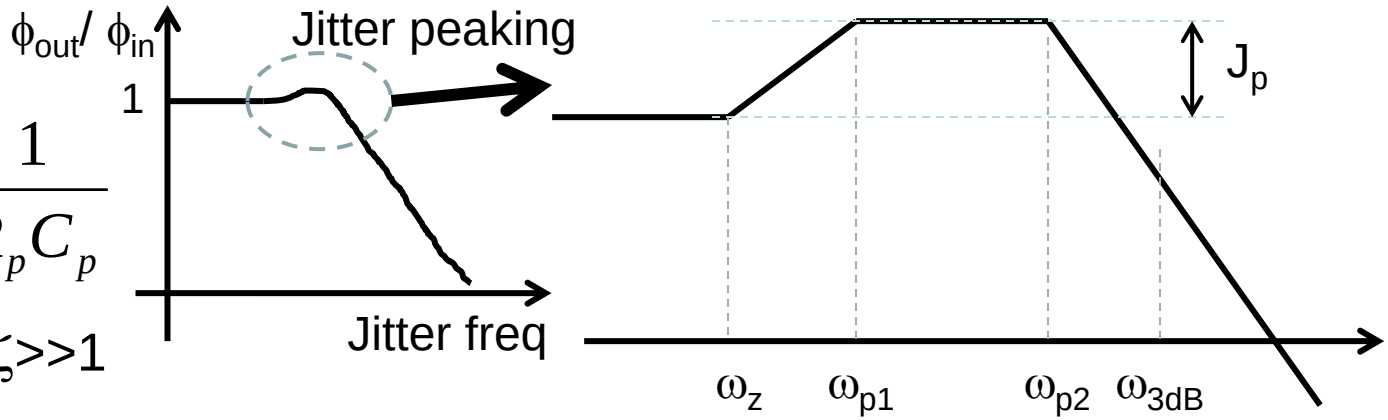
$$H(s) \approx \frac{2\zeta\omega_n}{s+2\zeta\omega_n} \longrightarrow \omega_{3dB} \approx 2\zeta\omega_n = \frac{R_p I_{CP} D_T K_{VCO}}{2\pi}$$



- This indicates that as the capacitor C_p is increased beyond a certain point the value of ω_{3dB} becomes independent of C_p
- However, this result might be miss leading, since in order to reduce the BW further we need to lower R_p which entails a significantly larger C_p in order to keep ζ constant

Jitter Transfer in CDRs: Jitter Peaking

$$\omega_z = -\frac{\omega_n}{2\zeta} = -\frac{1}{R_p C_p}$$



- Assuming that $\zeta >> 1$

$$\omega_{p1} = -\frac{\omega_n}{2\zeta} - \frac{\omega_n}{8\zeta^3}, \omega_{p2} = -2\zeta\omega_n + \frac{\omega_n}{2\zeta} + \frac{\omega_n}{8\zeta^3}$$

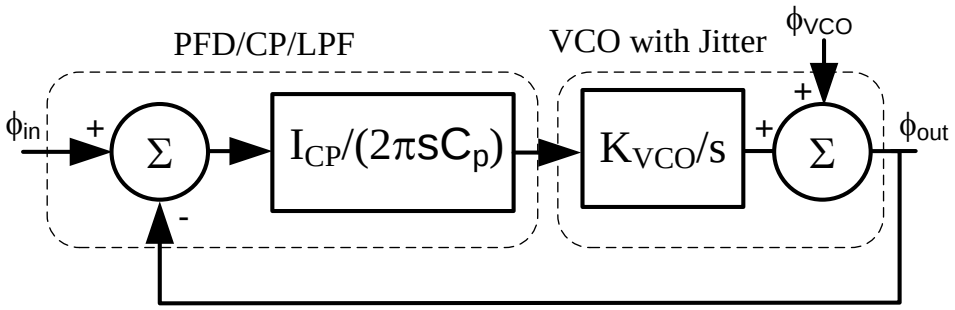
$$\omega_{3dB} \approx 2\zeta\omega_n$$

- The zero always appears before the poles inevitably leading to peaking
- The first pole is very close to the zero because $\zeta >> 1$

$$J_p\Big|_{dB} = 20\log\left(\frac{\omega_{p1}}{\omega_z}\right) \approx 20\log\left(1+\frac{1}{4\zeta^2}\right)$$

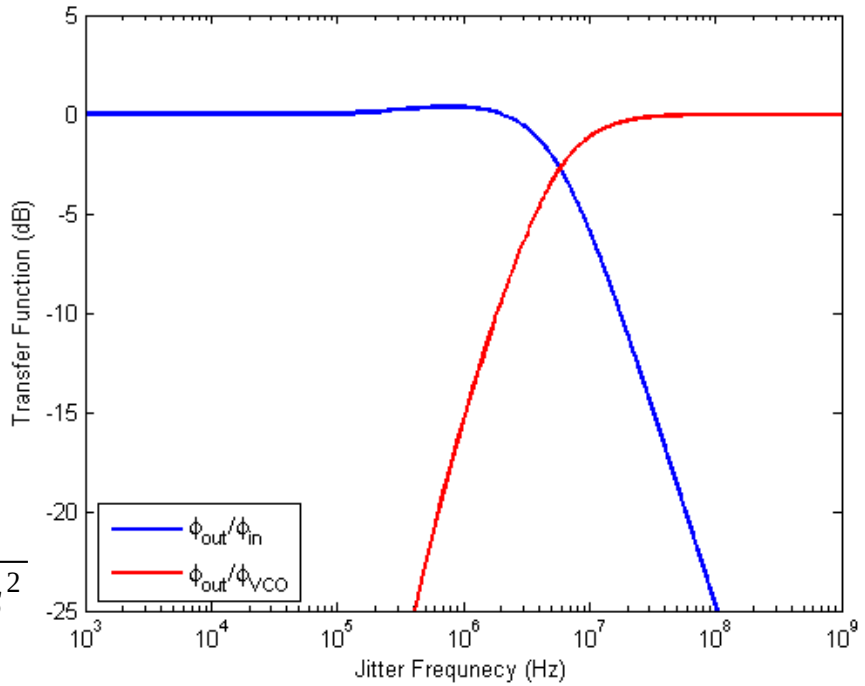
- If R_p is lowered to obtain a smaller loop bandwidth we should increase C_p in order to maintain a constant ζ and J_p

CDR Jitter Transfer/Generation



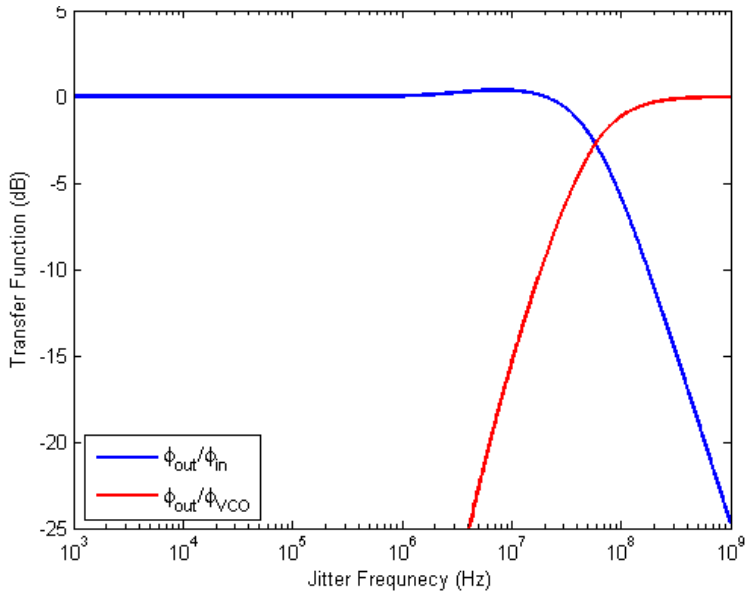
$$\frac{\phi_{out}}{\phi_{in}} = \frac{I_{cp} D_T K_{VCO} / 2\pi C_p \left(1 + sC_p R_p\right)}{I_{cp} D_T K_{VCO} / 2\pi\, C_p + sI_{cp} K_{VCO} R_p / 2\pi + s^2}$$

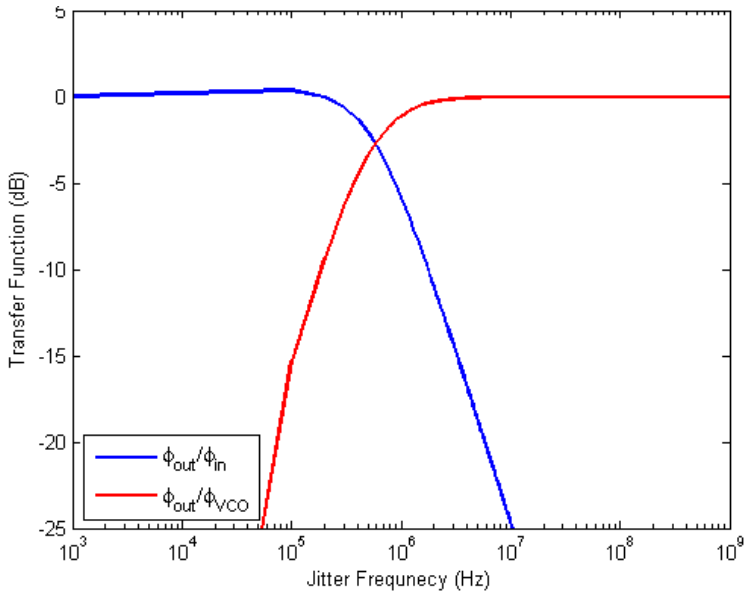
$$\frac{\phi_{out}}{\phi_{VCO}} = \frac{s^2}{K_{VCO} I_{cp} D_T / 2\pi C_p + s\, K_{VCO} I_{cp} D_T R_p / 2\pi + s^2}$$



- Jitter generation refers to the jitter produced by the CDR itself when the input data contains no input jitter
- The 2 main sources of output jitter are the input and the VCO phase noise ϕ_{VCO}
- The total output jitter is the rms sum of both sources
- The input jitter ϕ_{in} is shaped with the PLL's low pass transfer function
- The VCO phase noise ϕ_{VCO} is shaped with a high pass transfer function

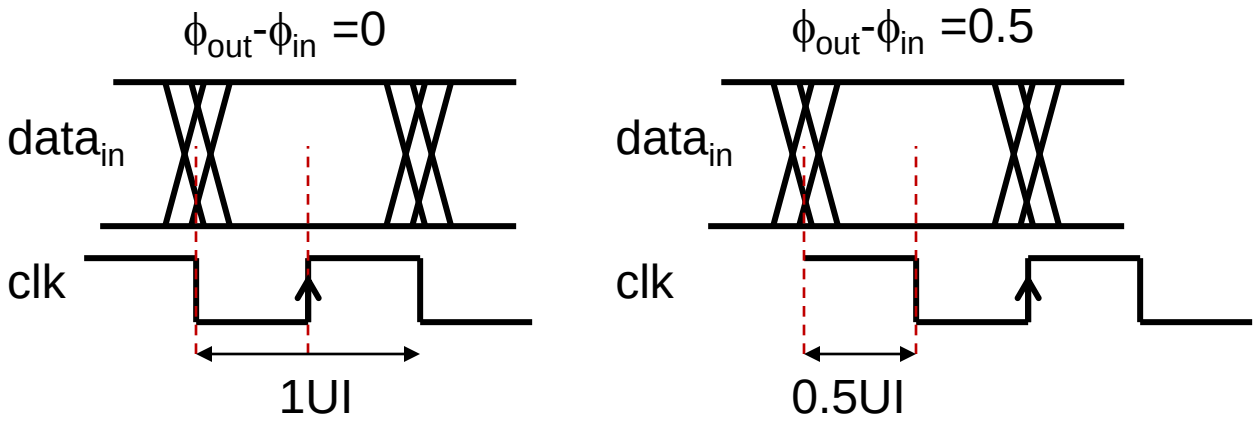
CDR Jitter Transfer/Generation (Cont'd)





- Increasing the CDR bandwidth results in integrating more input jitter and less VCO phase noise
- Whereas decreasing the CDR bandwidth results in less input jitter and higher jitter due to VCO phase noise
- A typical CDR design would target the maximum allowable BW by the standard to improve the CDR's jitter tracking capability, and minimize the VCO phase noise impact

CDR Jitter Tolerance

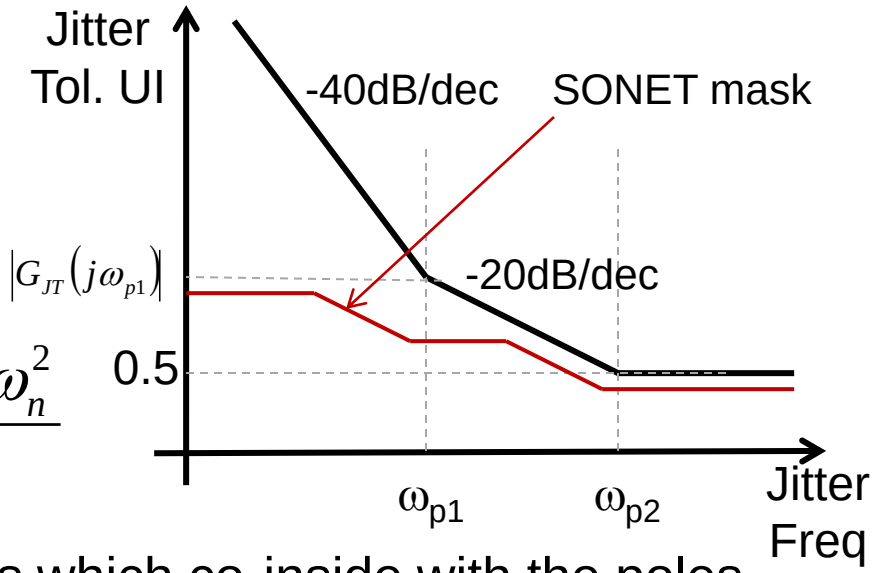


- Jitter tolerance: specifies how much jitter a CDR will tolerate for different jitter frequencies without increasing the bit error rate beyond a given limit set by the standard
- At a given jitter frequency, if the error between the input data phase ϕ_{in} and the recovered clock phase ϕ_{out} exceeds 0.5UI a sampling error occurs resulting in high BERs

$$\phi_{in} - \phi_{out} < 0.5UI \rightarrow \phi_{in}\left(1 - H(s)\right) < 0.5UI \rightarrow \phi_{in} < \frac{0.5UI}{\left(1 - H(s)\right)}$$

CDR Jitter Tolerance (Cont'd)

- We define GJT(s) as the largest jitter (phase modulation) at the input before the BER start to increase:

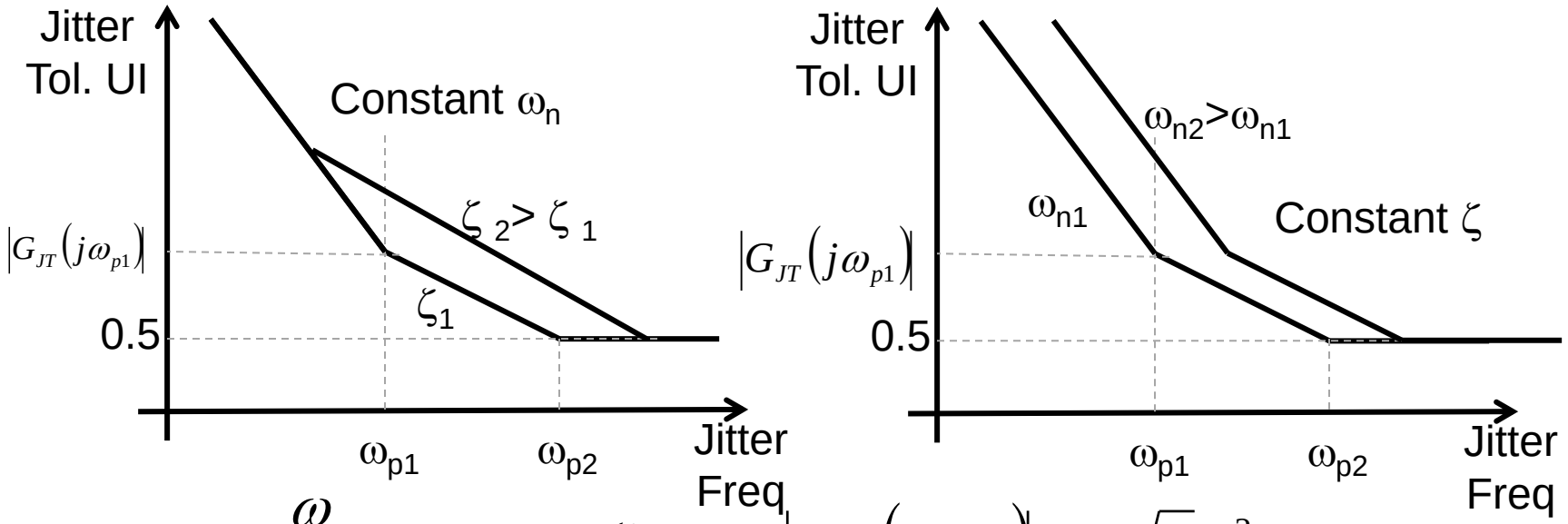


$$G_{JT}(s)=\frac{0.5}{1-H(s)}=\frac{1}{2}\frac{s^2+2\zeta\omega_n s+\omega_n^2}{s^2}$$

- G_{JT} has 2 poles at DC and two zeros which co-inside with the poles of H(s) (ω_{p1} and ω_{p2})
- GJT drops with -40dB/dec for $\omega < \omega_{p1}$ then with -20dB/dec for $\omega_{p1} < \omega < \omega_{p2}$, and approaches 0.5 for $\omega > \omega_{p2}$
- For $\zeta >> 1$ we can approximate the pole locations as:

$$\omega_{p1}\approx-\frac{\omega_n}{2\zeta},\omega_{p2}\approx-2\zeta\omega_n \longrightarrow \left|G_{JT}(j\omega_{p1})\right|\approx 2\sqrt{2}\zeta^2 \quad UI$$

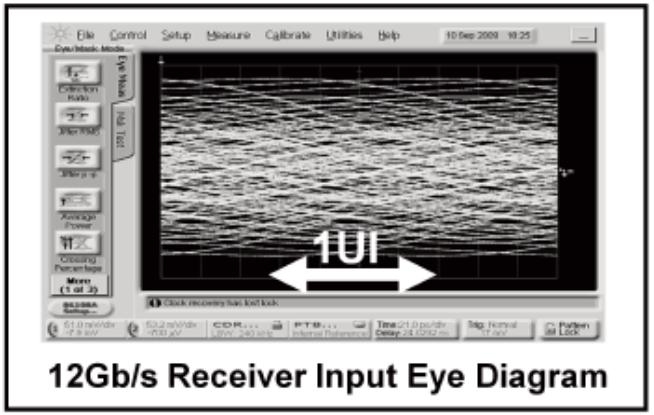
CDR Jitter Tolerance (Cont'd)



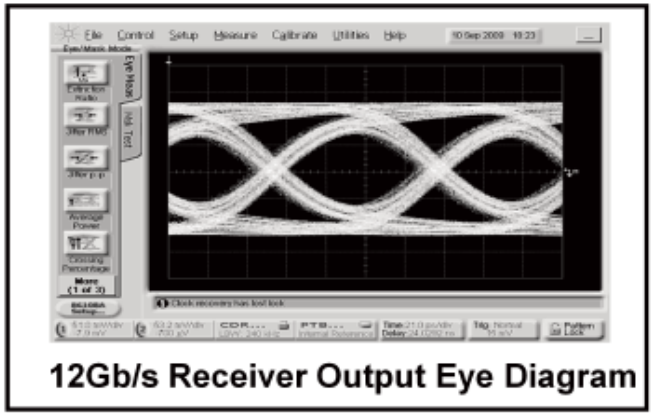
$$\omega_{p1} \approx -\frac{\omega_n}{2\zeta}, \omega_{p2} \approx -2\zeta\omega_n \qquad \left|G_{JT}\left(j\omega_{p1}\right)\right| \approx 2\sqrt{2}\zeta^2 \quad UI$$

- As ζ increases with a constant ω_n it is easier to meet the jitter tolerance mask (clearing the knee)
- Increasing ω_n with a constant ζ improves the jitter tolerance, but at the increases the jitter transfer BW, which might not be desirable for some applications → further jitter filtering using a second PLL can be used

ISSCC 2010: A 12Gb/s 39dB Loss-Recovery Receiver



12Gb/s Receiver Input Eye Diagram



12Gb/s Receiver Output Eye Diagram