



# ECE 621
# Signaling & Synchronization
# Fall 2020

## Topic 1
# Introduction

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**Ain Shams University**

**ICL**

**(Courtesy of S. Pamarti, UCLA)**

# Course Administration

- **Instructor: Dr. Sameh A. Ibrahim IC Lab, Third floor, Room 311**
- **Office Hours: Online**
- **e-mail address: sameh.ibrahim@eng.asu.edu.eg**
- **Website:**
  **LMS**
- **Time & Place: Sat. 10:00 AM – 12:00 PM (Weekly), Rm. 316**
- **Reference Material:**
  - Lecture Notes
  - Selected Papers
- **Grading:**
  - Design Project (Through Assignments) 50%
  - Final 50%

# Course Topics (1)

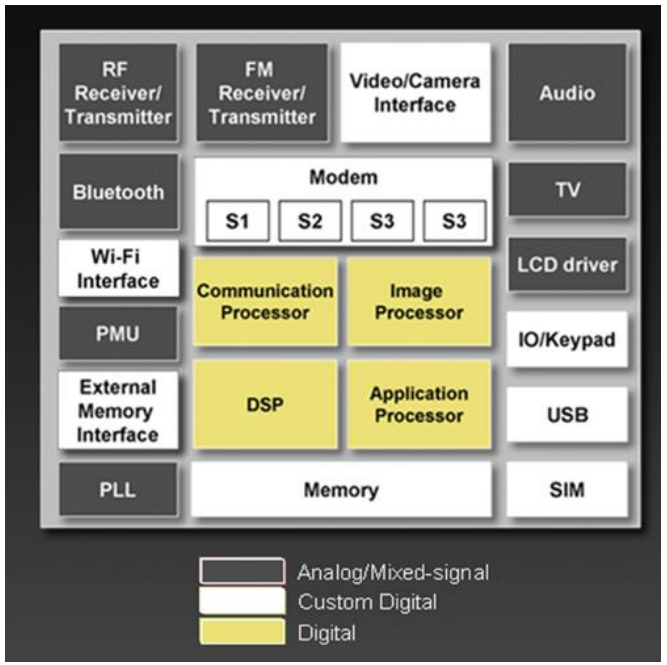
- **Introduction to Signaling and Synchronization**
- **I/O Channel Characteristics**
  - Frequency-Dependent Loss – ISI
  - Reflections
  - Cross-Talk
- **TX Building Blocks**
  - Voltage/Current Mode signaling
  - Line Drivers
  - Pre-Emphasis
  - Multiplexers

# Course Topics (2)

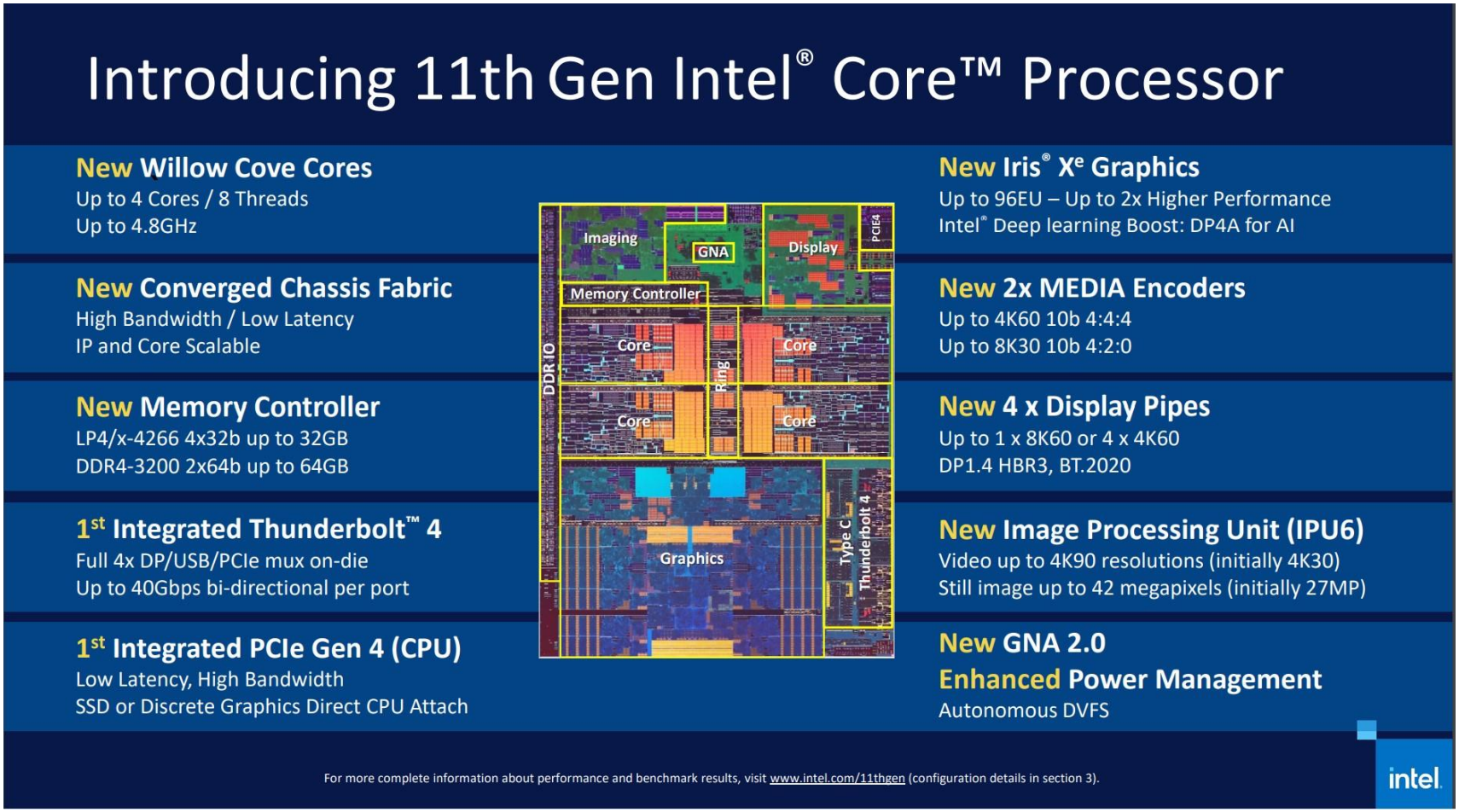
- **RX Building Blocks**
  - Equalization techniques and architectures
  - FFE and DFE circuits
  - Slicers
  - Demultiplexers
- **Clock and Data Recovery (CDR)**
  - PLL and DLL Basics
  - Jitter Concepts: generation, transfer and tolerance
  - Phase Detectors
  - Charge Pumps
  - Voltage-Controlled Oscillators (VCO)
  - Frequency Dividers
- **Advanced Signaling Techniques**

# The Road to SOCs

- **A typical system-on-chip SOC consists of:**
  - A microcontroller, microprocessor or DSP core(s)
    - Taught in a digital design course.
  - Memory blocks including a selection of ROM, RAM, EEPROM and flash memory
    - Taught in a digital design course.
  - Timing sources including oscillators and phase-locked loops.
    - Taught in an analog system design course
    - Taught in a serial-link design course.
  - External interfaces including industry standards such as USB, FireWire, Ethernet, USART, SPI
    - Taught in a serial-links design course.
  - Analog interfaces including ADCs and DACs
    - Taught in an analog system design course.
  - Voltage regulators and power management circuits
    - Taught in a power management course.

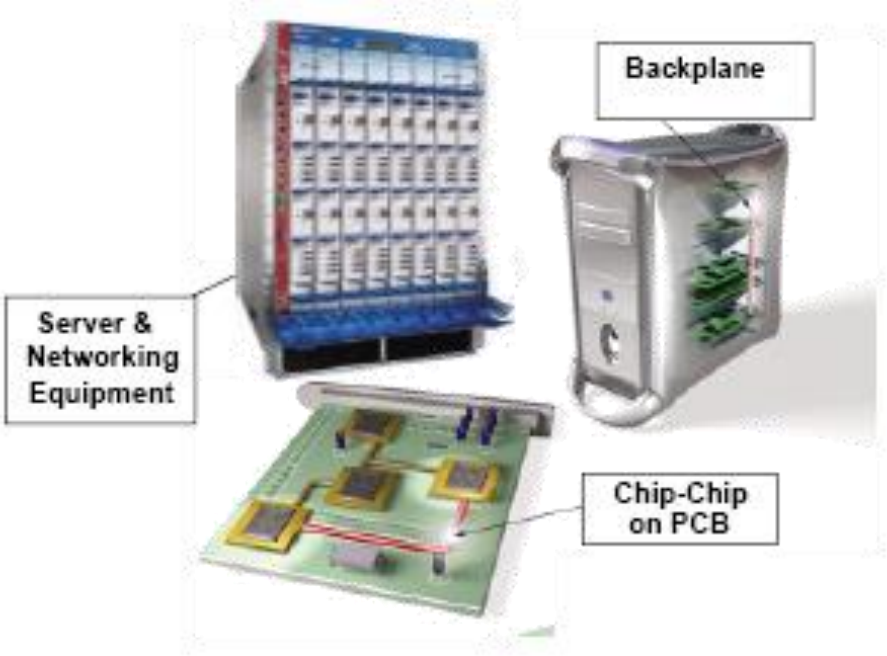


# Tiger Lake Architecture

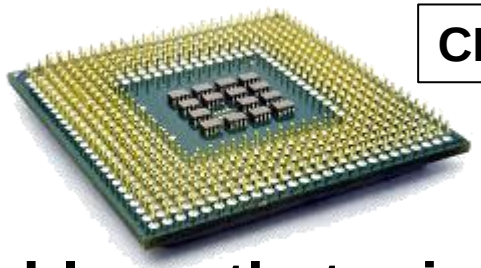



- **11th Generation Core Processor Released in October 2020 using 10nm++ (SuperFin) Tri-Gate 3D transistors.**
- **146.10 mm² die size (~13.64 mm x ~10.71 mm) – 4 Cores, 96 Eus – up to 12 MiB Cache**
- **5B transistors in its smallest version**

# Signal Integrity





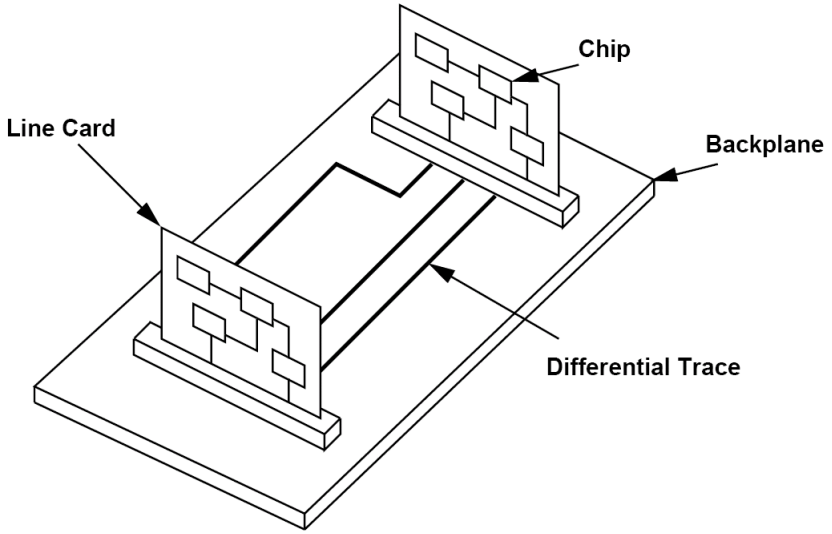


CPU-GPU

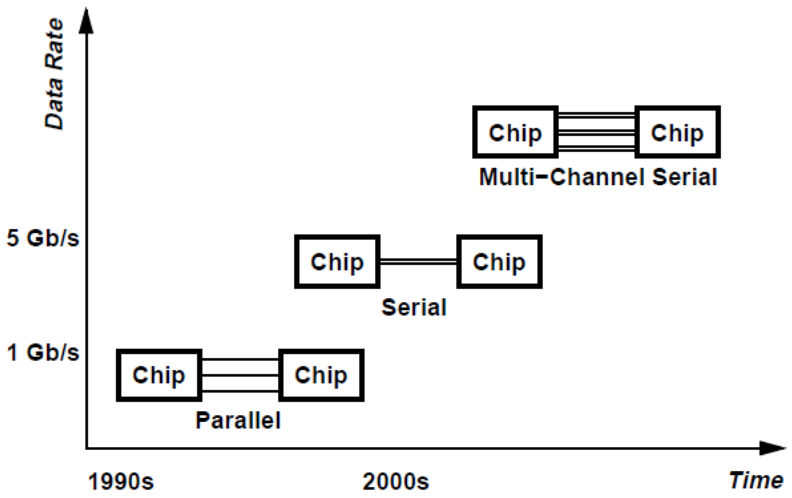
- **Signal Integrity refers to all the problems that arise in high-speed products due to the interconnects.**
- **Problems fall into one of three categories**
  - Timing
  - Noise
  - Electromagnetic Interference (EMI)

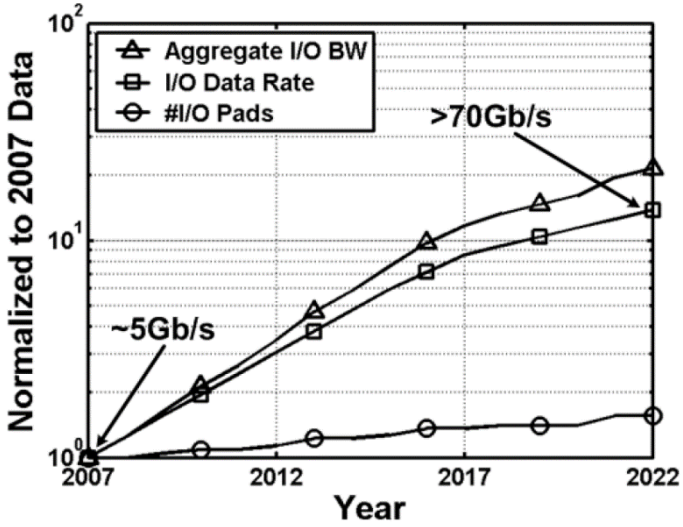
# How Important is SI?

- **Pre-1990**
  - 10 MHz Clock, 10 nsec rise and fall times
  - SI addressed only after failure
- **1990-2000**
  - >100 MHz Clock, < 1nsec rise and fall times
  - SI focused on channel models
  - SI integrated in high-speed digital system design
- **2000-Present**
  - GHz range Clock
  - Rise and fall times in psec
  - SI drives architecture choice.
  - SI models the entire link.



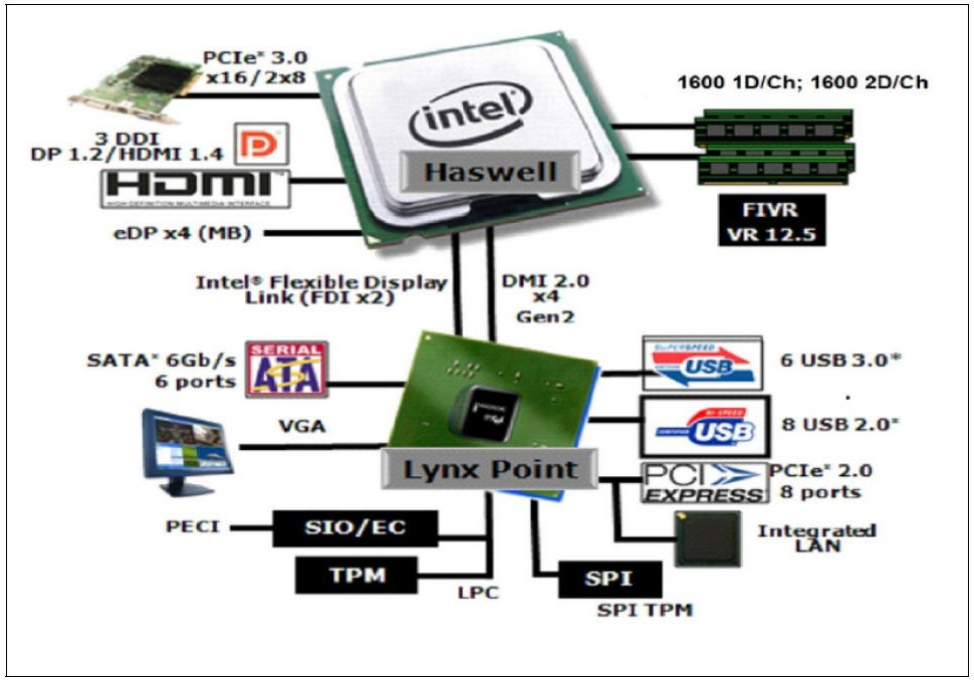
# Why Now?




- From parallel to serial to multiple-channel serial
- Data rates beyond 10 Gb/s
- Lower voltage swings
- Get it right or it does not work

# Serial Link Standards – Desktop



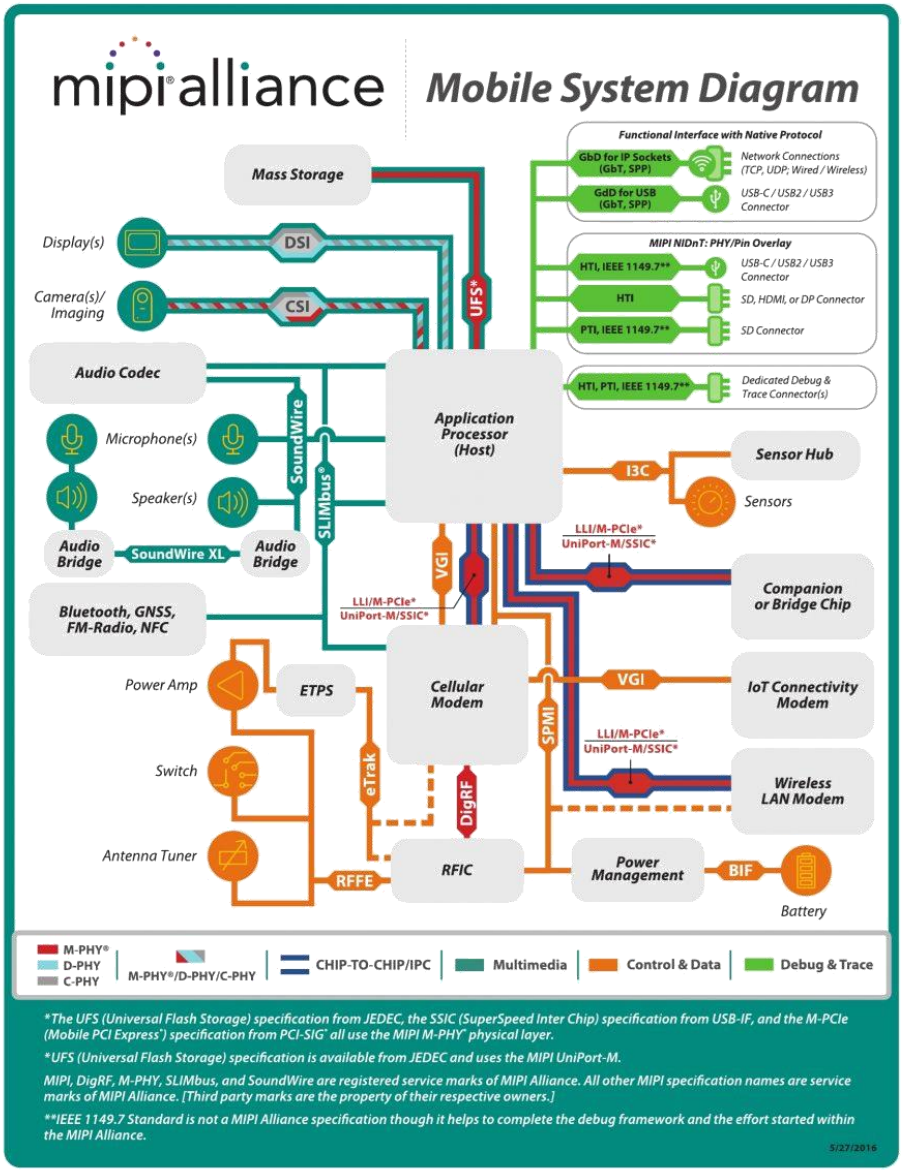

- PCIe (PCI Express)
  - Computer expansion bus
  - 2.5, 5, 8, 16 Gbps
- USB
  - Universal Serial Bus
  - For computer peripherals
  - 0.012, 0.48, 5, 10 Gbps
- SATA
  - Mass storage devices
  - 1.5, 3, 6, 16 Gbps

- HDMI
  - Audio/Video interface
  - 5, 10, 18 Gbps
- Ethernet
  - LAN 0.01, 0.1, 1, 10 , 100 Gbps
- DDR
  - Memory 0.2, 1.066, 2.133, 3.2 Gbps

- DMI
  - Connects controllers
  - 10, 20 Gbps

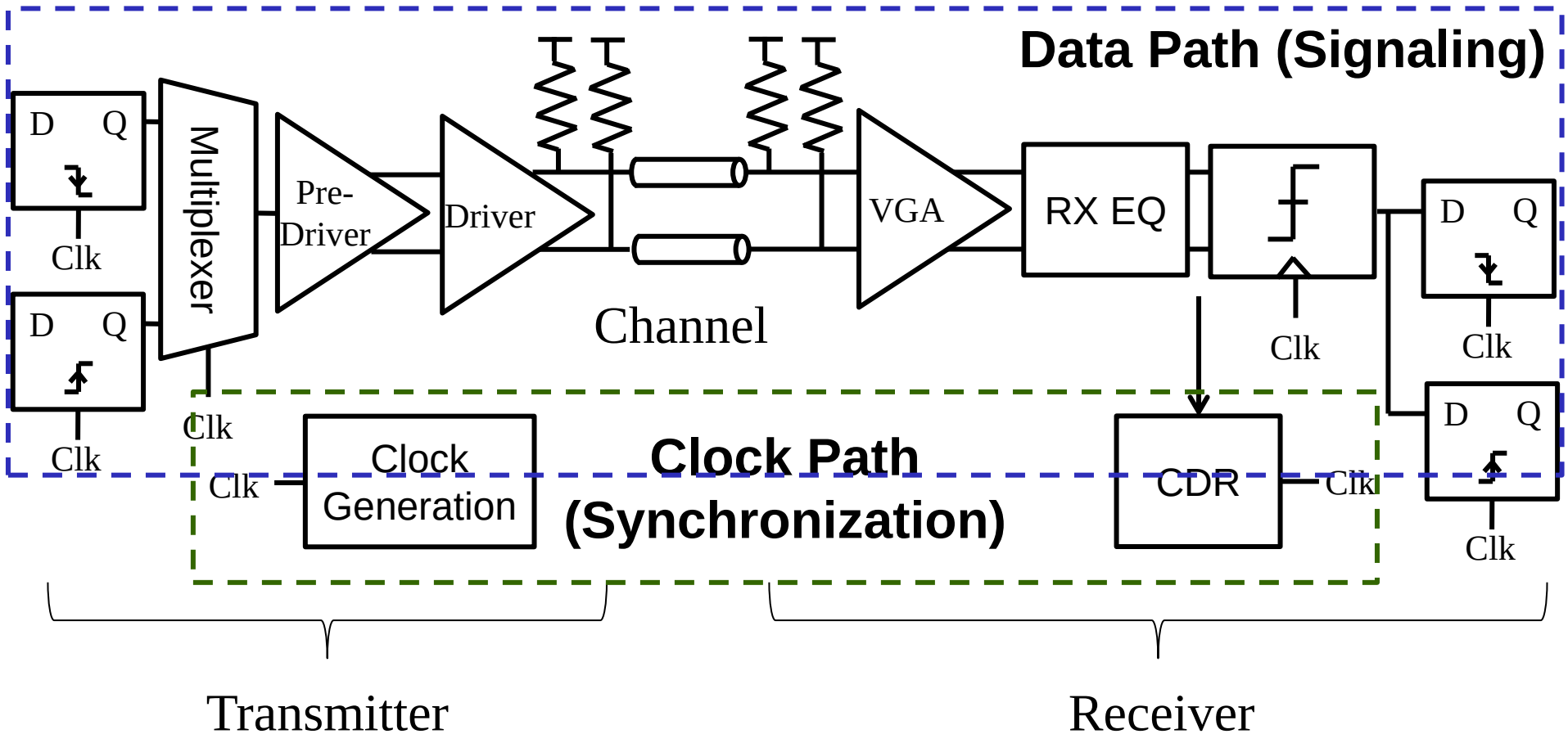
- SPI
  - Short distance, single master

# Serial Link Standards – Mobile

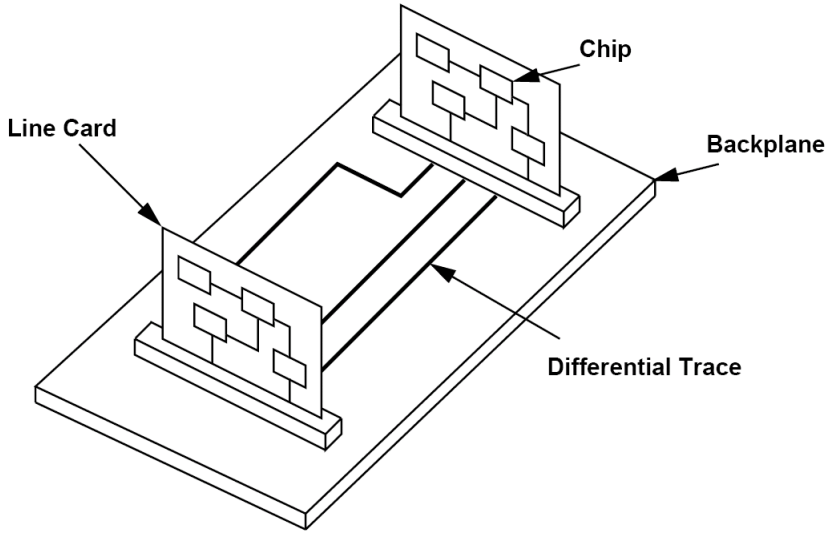


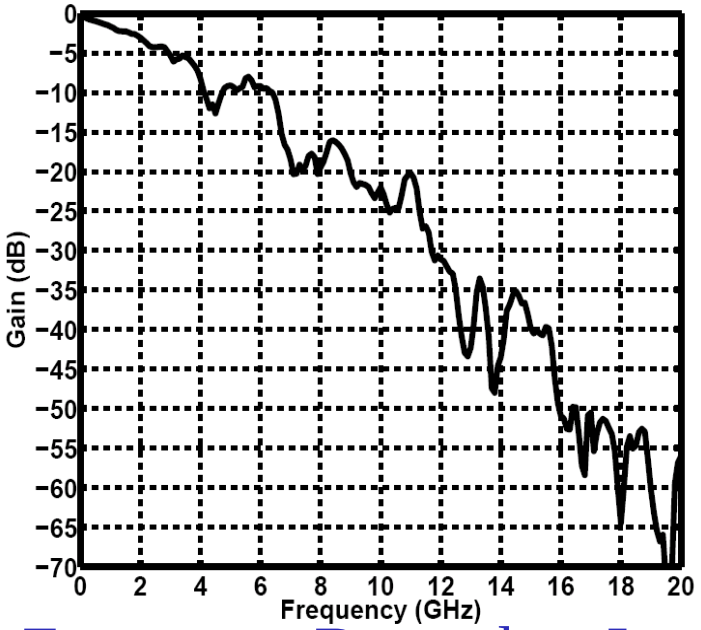

- MIPI
  - Low power
  - Mobile applications
  - 1.5, 3, 6, 12 Gbps

# System Block Diagram

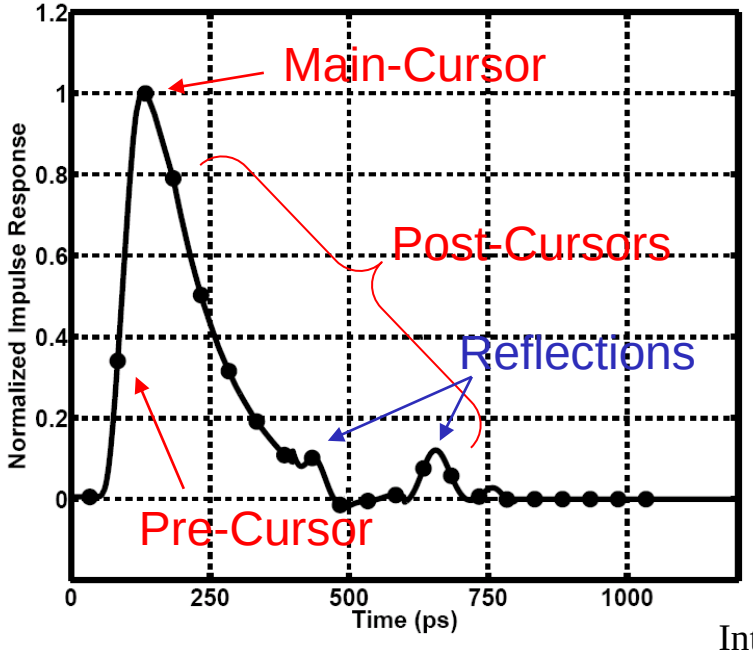


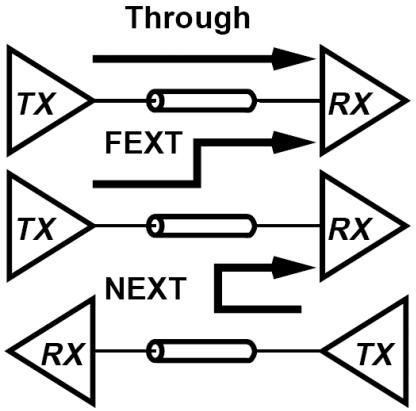
# Topic 2: Channel Characteristics



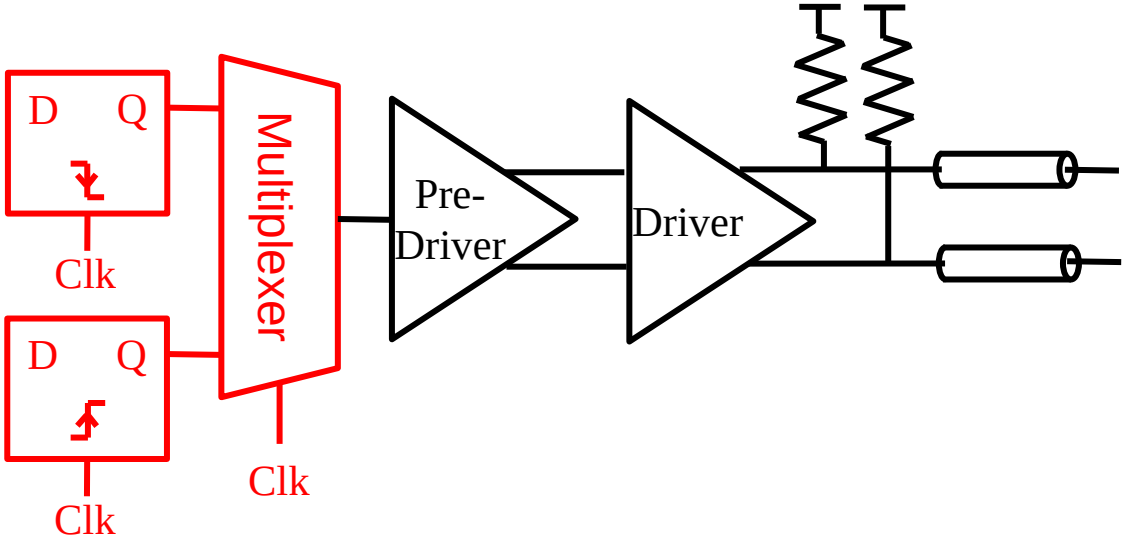

Frequency-Dependent Loss



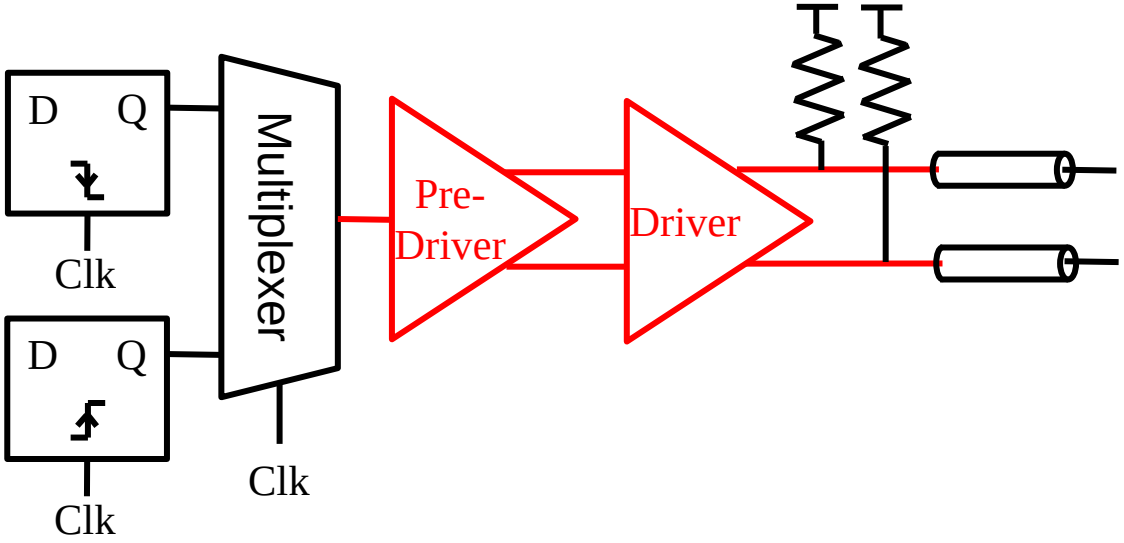

Cross-Talk

# Topic 3: TX Circuitry (1)



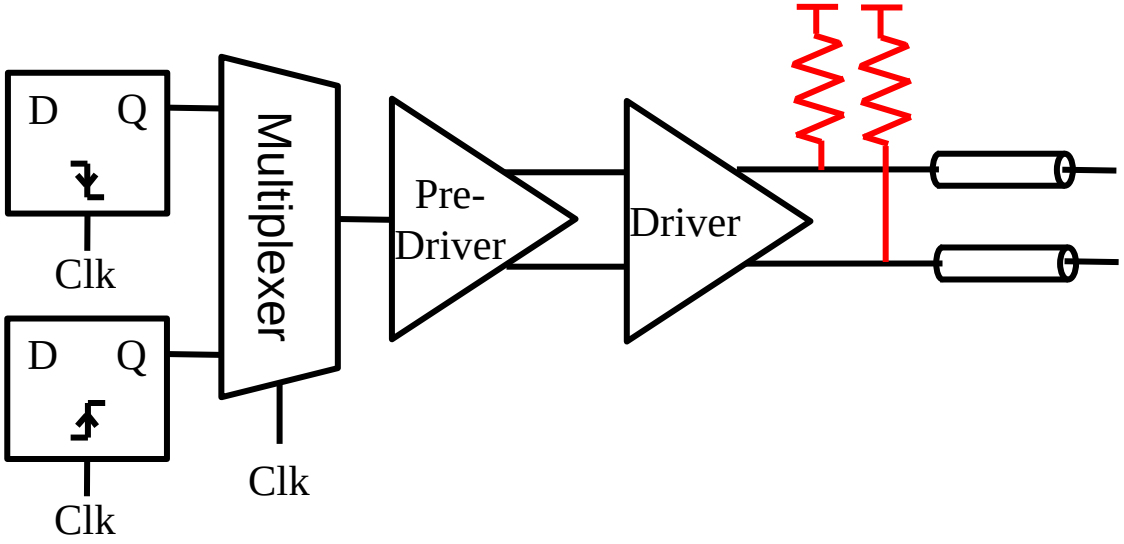

- **Multiplexing**
  - Circuit design
  - Clock distribution issues
  - Power consumption issues

# Topic 3: TX Circuitry (2)



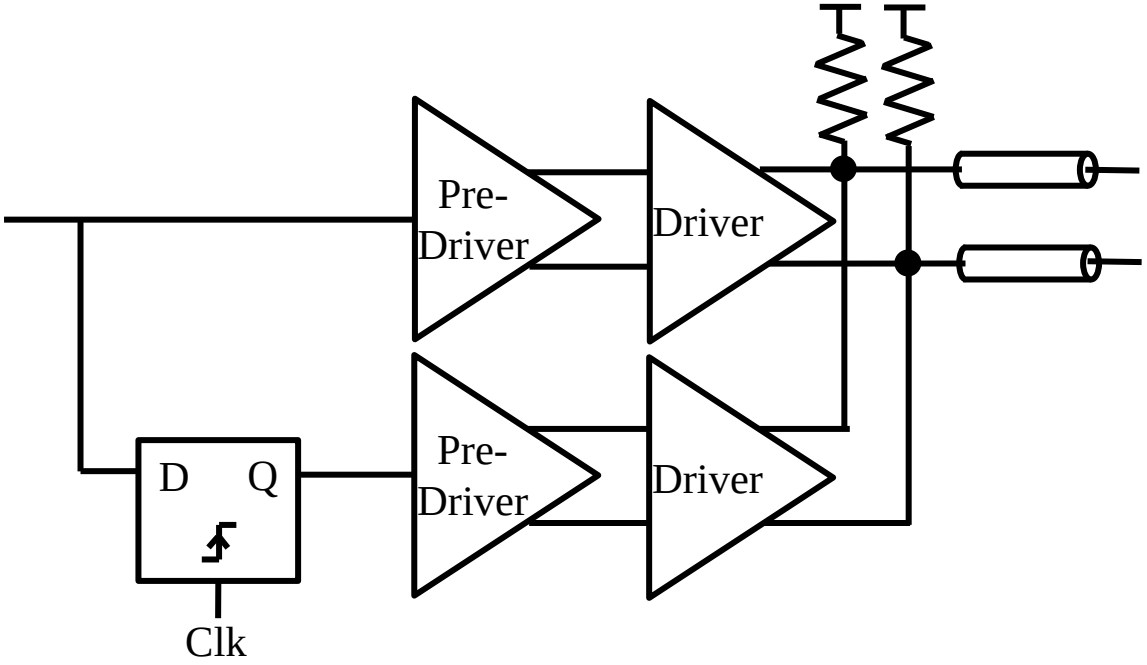

- **Driver and Pre-Driver**
  - Voltage and current mode drivers
  - Bandwidth issues
  - Swing control
  - Impedance control

# Topic 3: TX Circuitry (3)



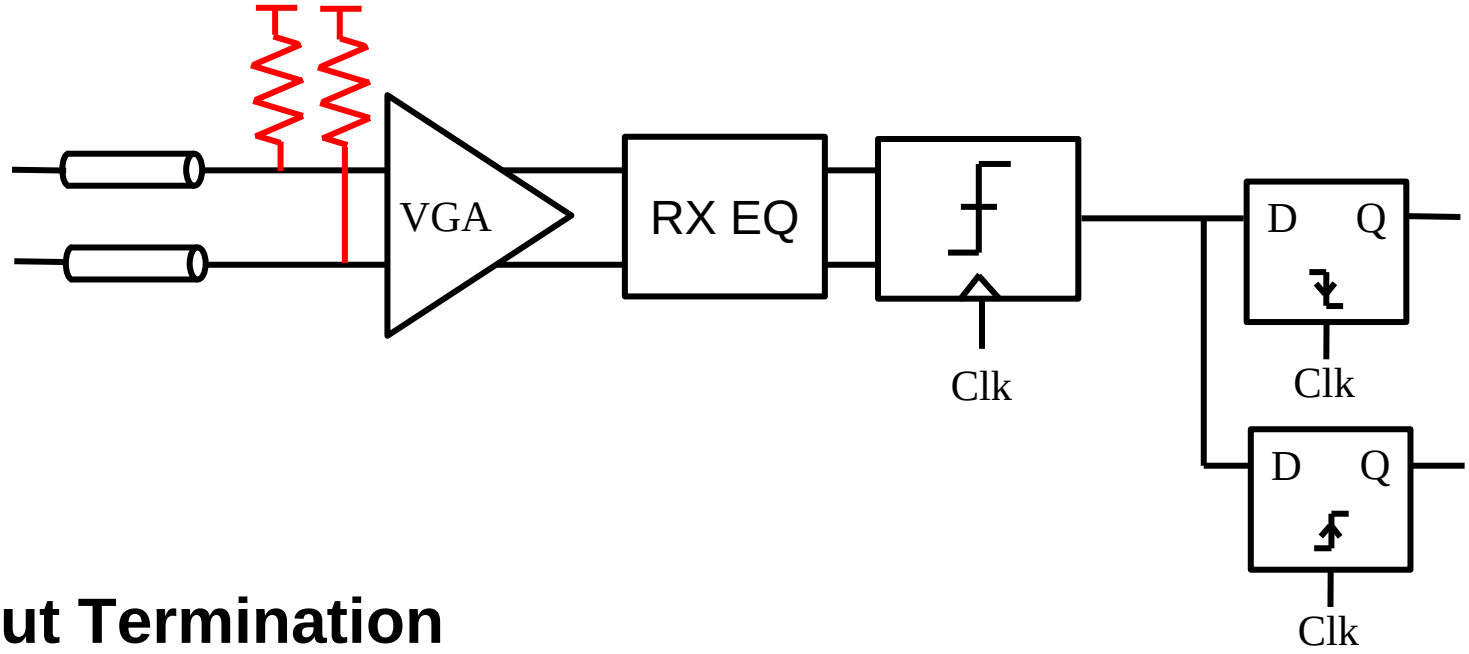

- **Termination Resistors**
  - On-chip or off-chip
  - PVT variations

# Topic 3: TX Circuitry (4)



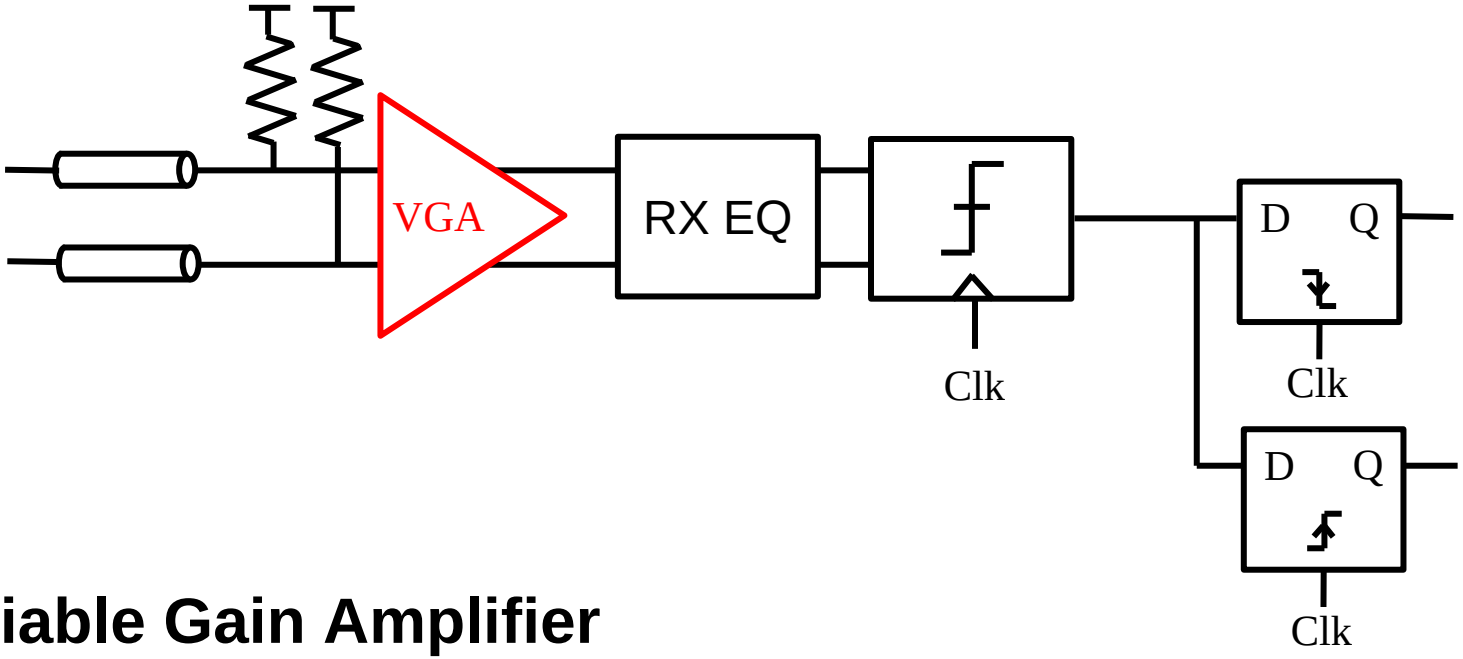

- **Pre-Emphasis**
  - Power consumption concerns
  - Coefficient choice
  - Pre-emphasis vs. de-emphasis

# Topic 4: RX Circuitry (1)



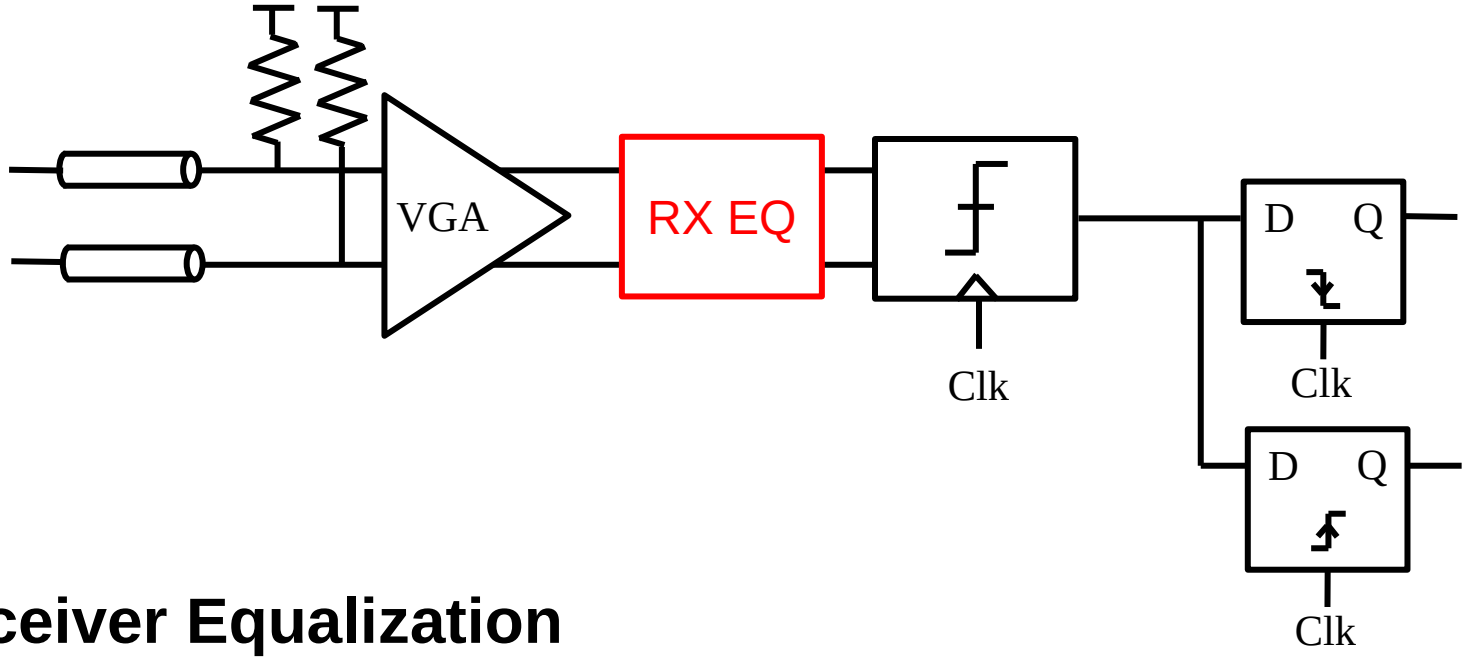

- **Input Termination**
  - On-chip or off-chip
  - PVT variations

# Topic 4: RX Circuitry (2)



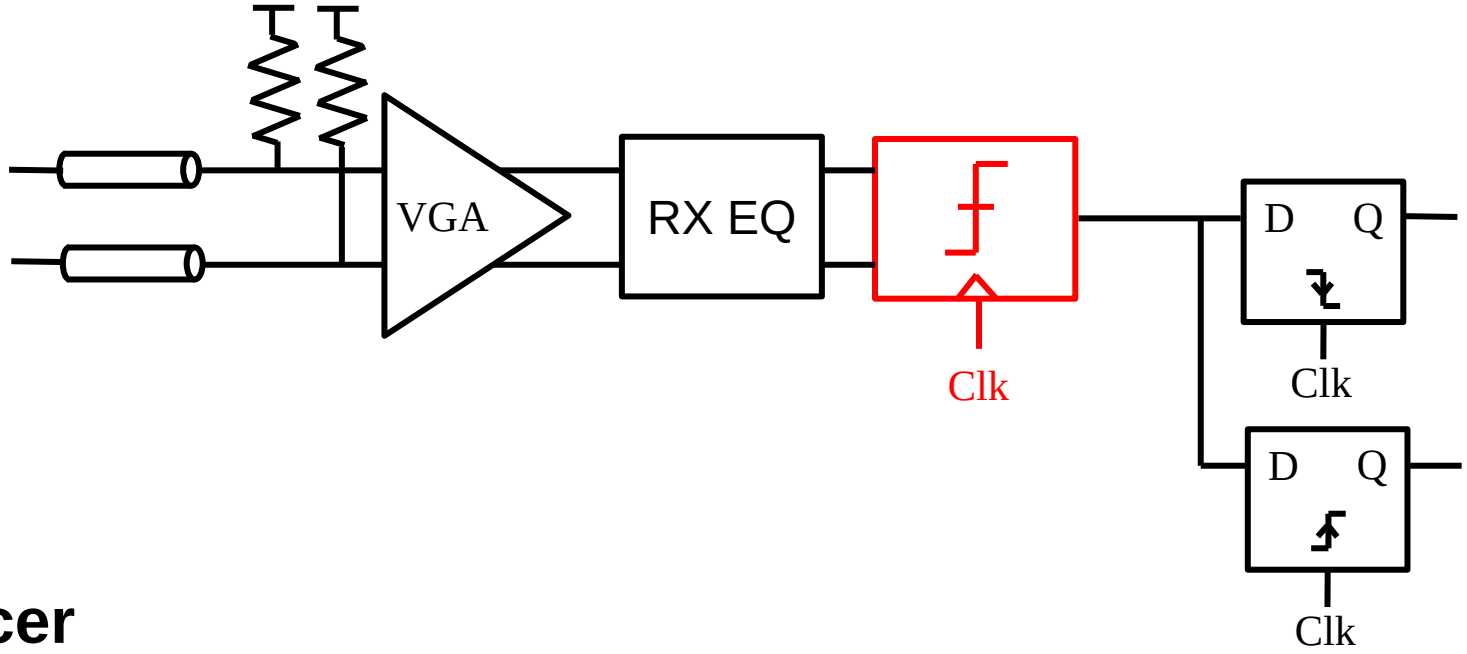

- **Variable Gain Amplifier**
  - Large bandwidth required
  - Offset and noise limitations
  - Gain profile

# Topic 4: RX Circuitry (3)



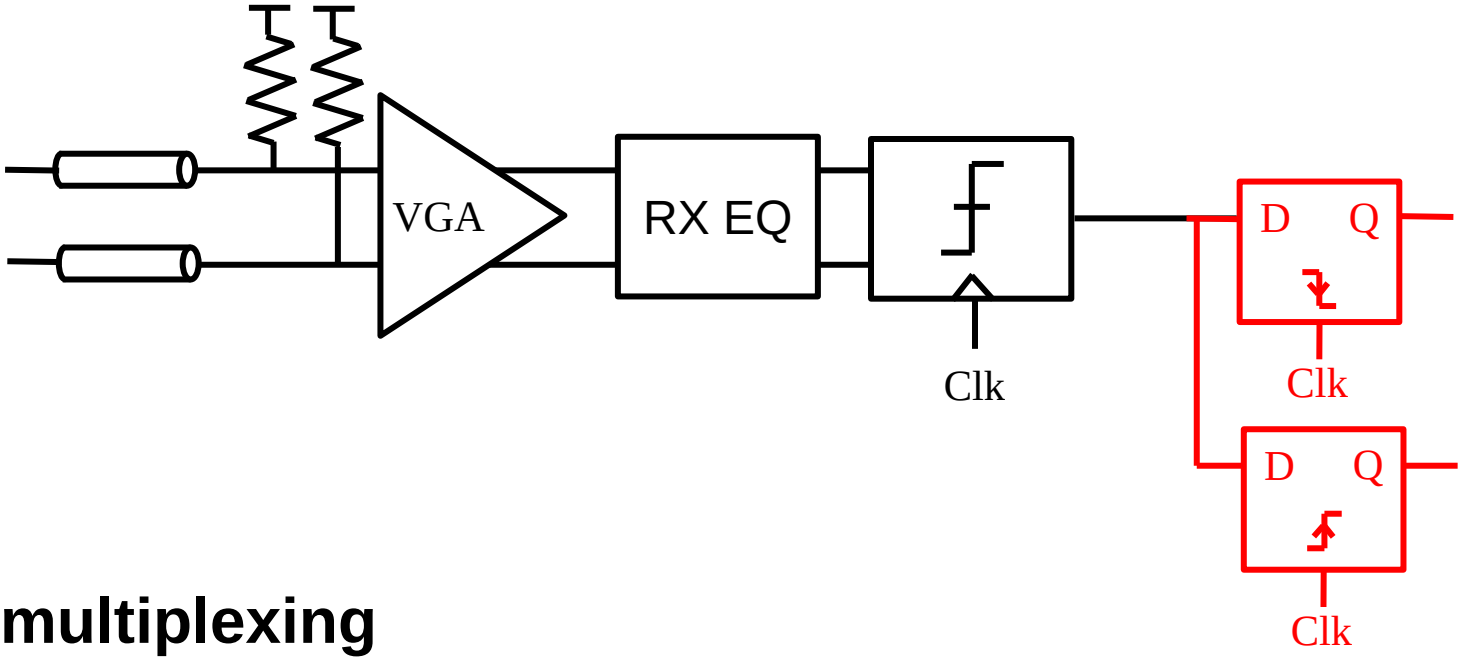

- **Receiver Equalization**
  - Linear vs. DFE
  - TX vs. RX equalization
  - Analog vs. Digital

# Topic 4: RX Circuitry (4)



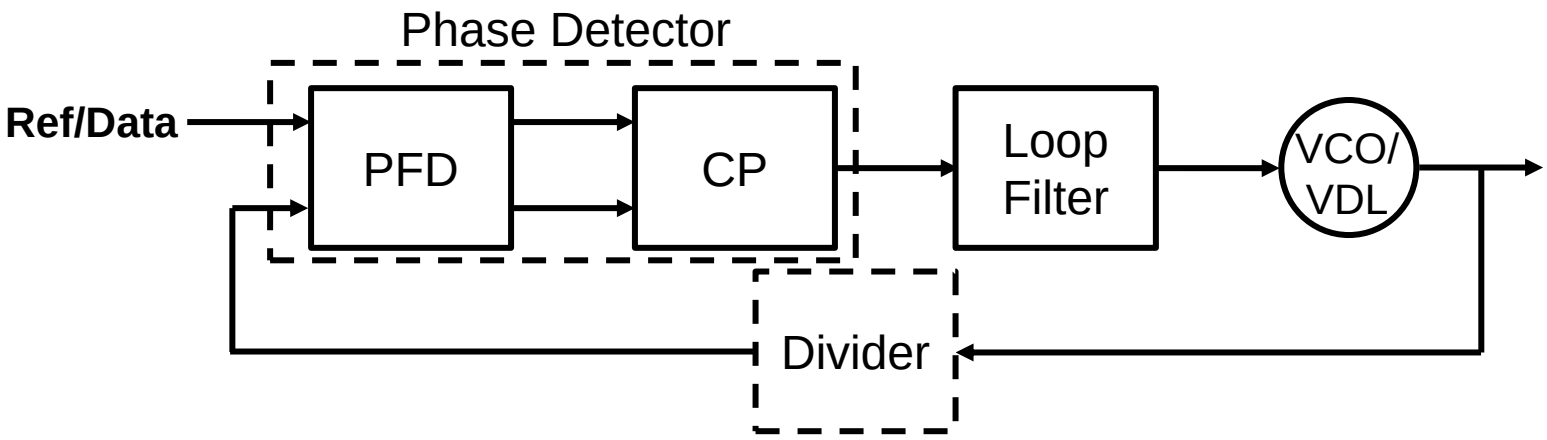

- **Slicer**
  - Offset and noise considerations
  - High speed requirements
  - Sensitivity

# Topic 4: RX Circuitry (5)




- **De-multiplexing**
  - Clock distribution
  - Power distribution

# Topic 5: Clock and Data Recovery (CDR)




- **PLLs and DLLs are used for clock generation and CDR**
- **PLL and DLL basics**
- **PLL and DLL Components**
- **Jitter and Noise analysis**
- **Linear and Non-linear clock recover systems**

# Topic 6: Advanced Signaling Techniques

- **Signaling techniques for better channel utilization**
  - 4-PAM signaling
  - Simultaneous bi-directional signaling
  - Mutli-tone signaling
  - Duo-binary signaling