Wireline Transceiver Circuits

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Course Outline

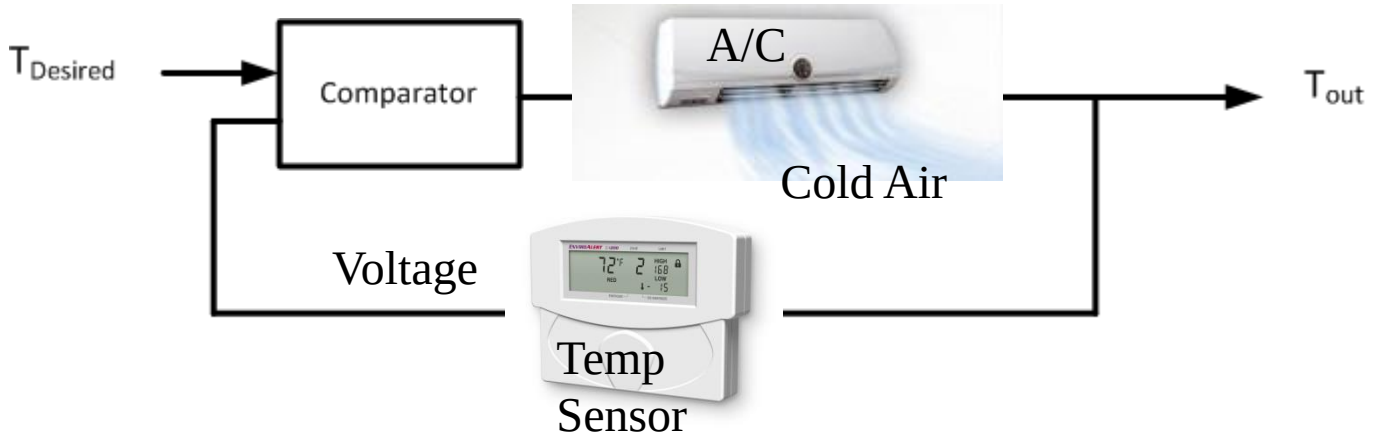
- Introduction to phase locked loops
- Phase locked loop top level analysis
- Phase locked loop building blocks
  - Phase detectors
  - Voltage controlled oscillators
  - Frequency dividers
- Phase locked loop noise analysis
- Crystal oscillator circuit

Introduction to Phase Locked Loops

- Phase locked loops (PLL) are used in many applications such as wireless and wireline transceivers
  - In radio/TV transceivers there are multiple channels
  - Phase locked loop is used to generate the required frequency for a certain channel
  - High accuracy and low noise is required
- PLLs are also used to generate clocks for digital processors, wireline communication systems

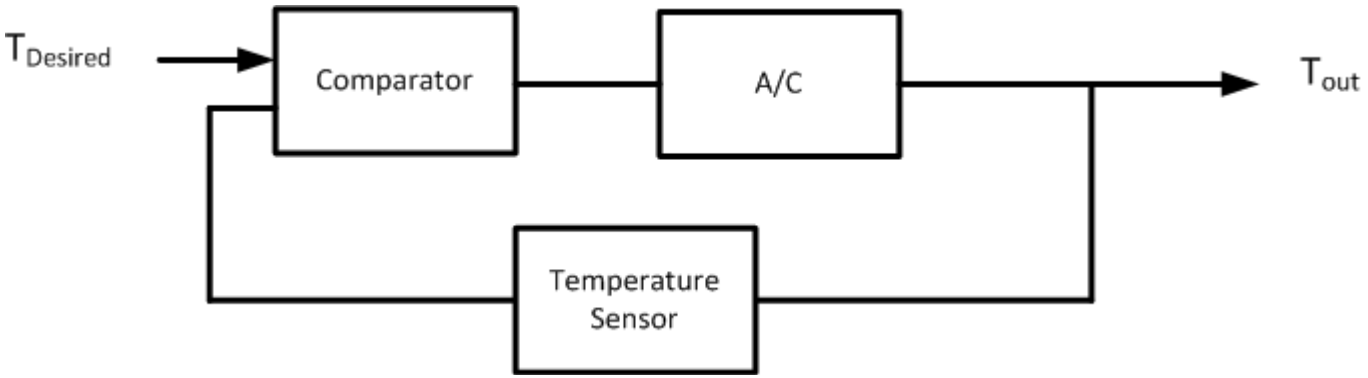
Introduction to Phase Locked Loops

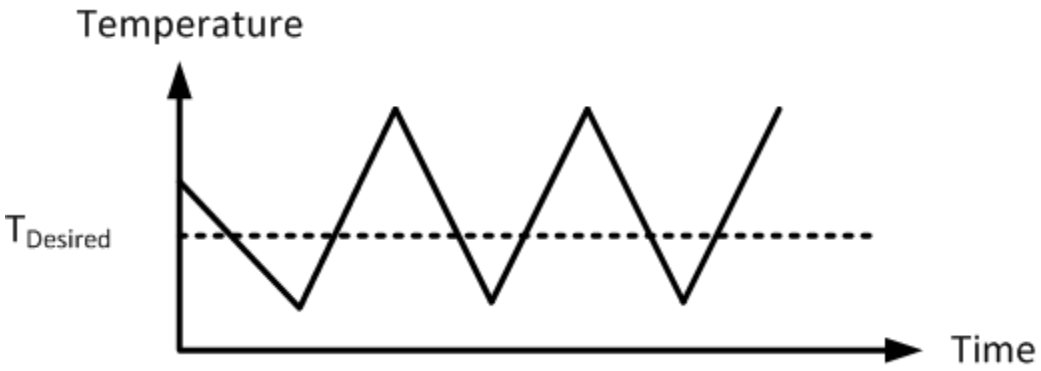
- PLL is used to generate a certain output frequency
- Feedback is used to generate precise output frequency
- An example of feedback system is air condition (A/C) systems where a desired output temperature is needed

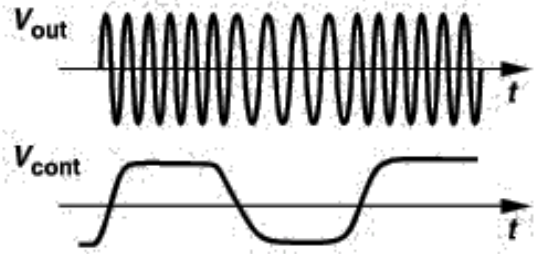


Introduction to Phase Locked Loops

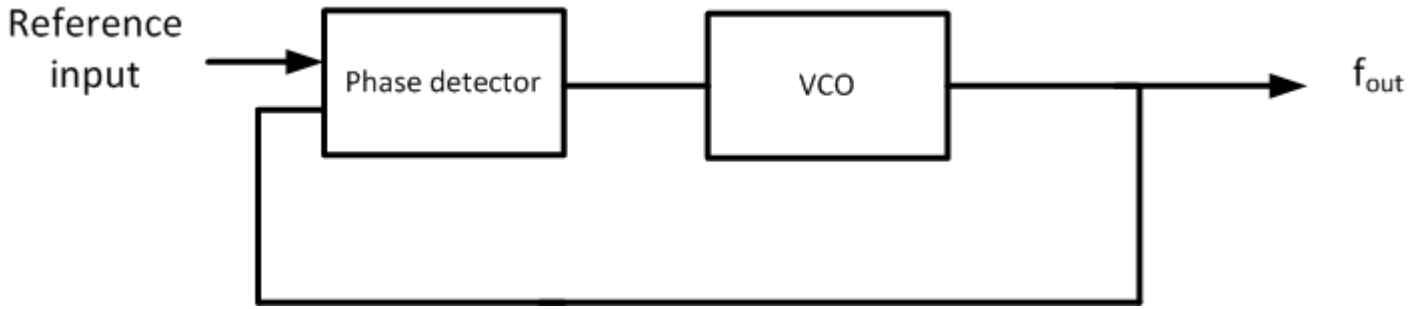
- Feedback system need to be stable
  - If comparator output is slow, the output temperature will oscillate



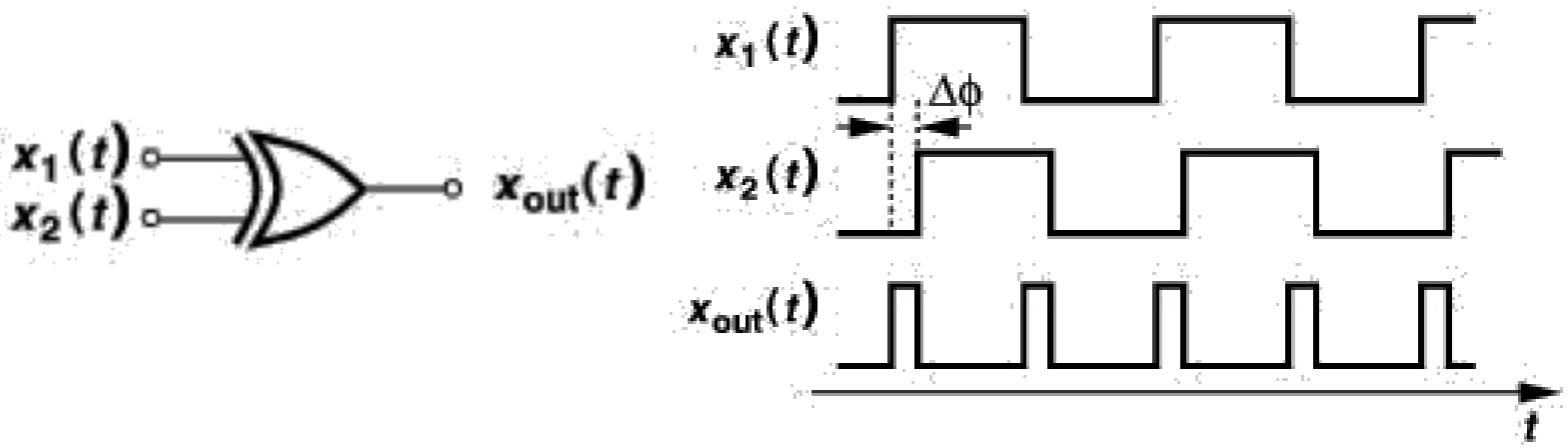




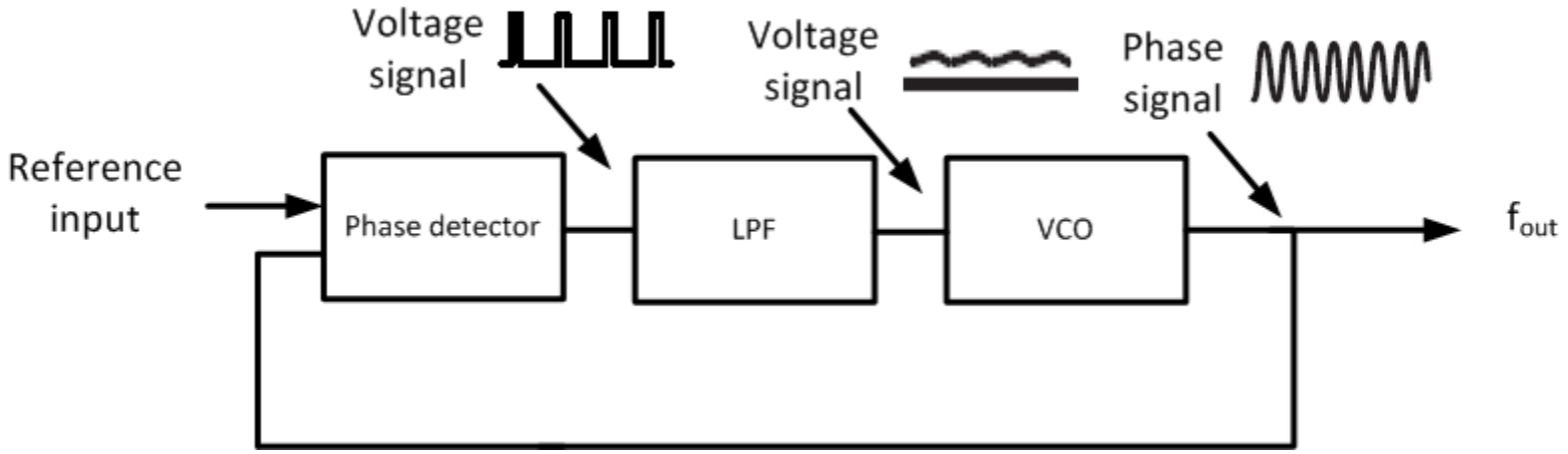
Basic PLL Block Diagram



- Main building blocks of PLL are
  - Voltage controlled oscillator (VCO)
  - Phase Detector (PD)
- Simplest frequency detector is XOR gate



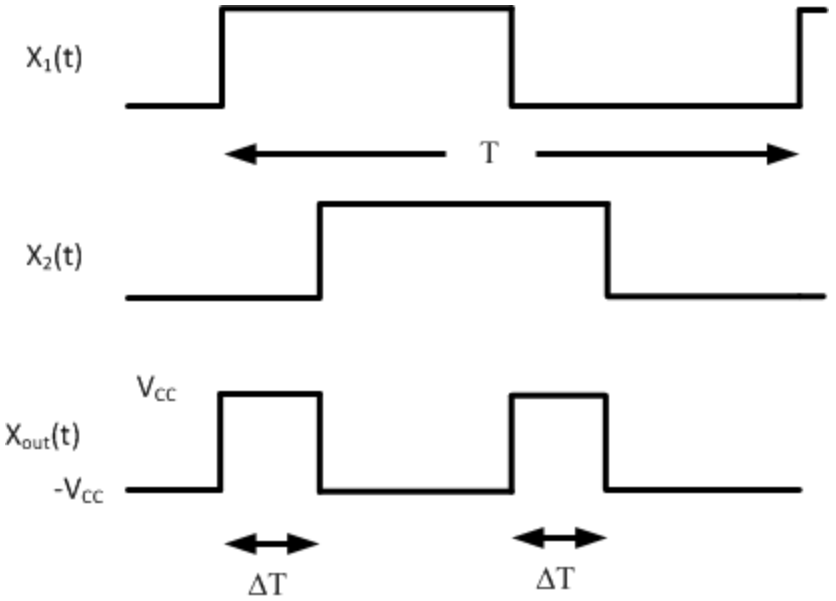
Basic PLL Block Diagram



- Note that phase detector output is voltage while VCO output is frequency or phase
- XOR output is a pulse proportional to the phase difference
  - Low pass filter is added to extract the average voltage which is proportional to the phase difference

XOR Phase Detector

Case 1: $-\pi<\phi 1-\phi 2<0$

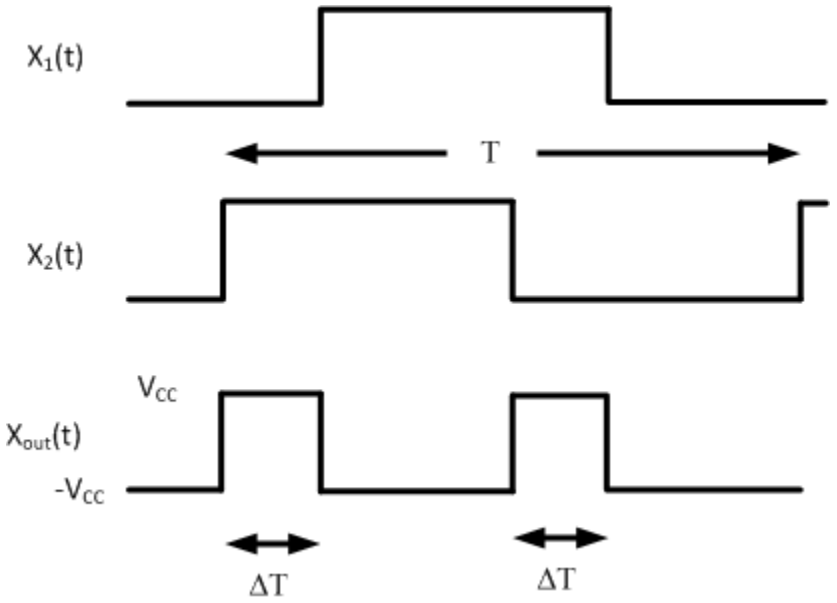


- Assume that supply of XOR gate is VCC and –VCC
- 1 period duration is T, which is also 2π
  - $\Delta T/T = -\Delta\phi/2\pi$
- The output $X_{out}(t)$ can be represented by a DC component and a summation of sinusoidal waves
  - Sinusoidal waves will be filtered by LPF and only DC component will pass
  - DC component of Xout = $\frac{1}{T}\int_0^T X_{out}(t)dt = \frac{1}{T}\left(V_{CC}2\Delta T - VCC(T-2\Delta T)\right)$

$$= 2V_{CC}\left(\frac{\Delta T}{T}\right) - V_{CC} = 4V_{CC}\left(\frac{-\Delta\emptyset}{2\pi}\right) - VCC$$

XOR Phase Detector

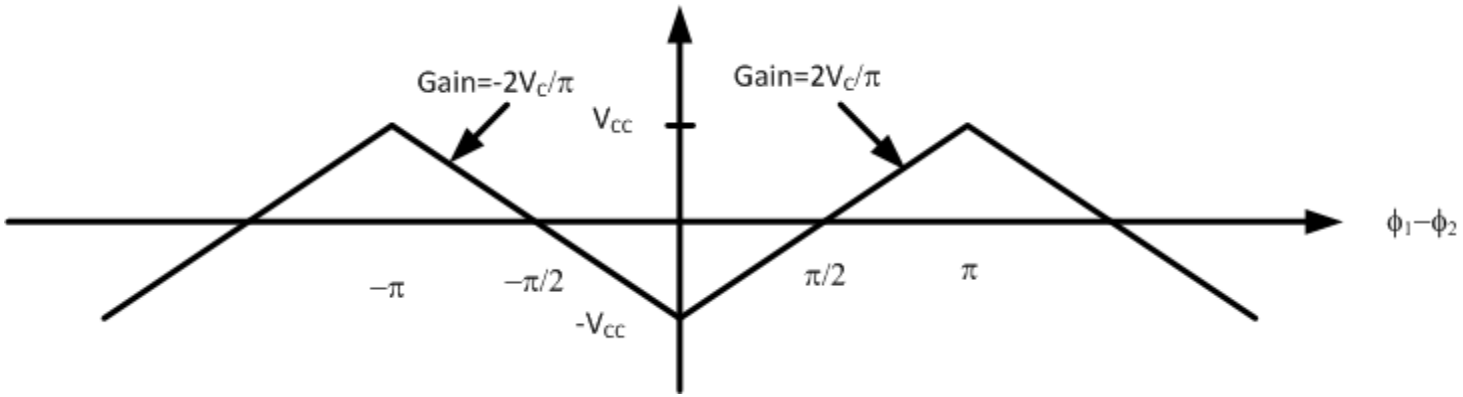
Case 2: $0<\phi 1-\phi 2<\pi$



- Assume that supply of XOR gate is VCC and –VCC
- 1 period duration is T, which is also 2π
  - $\Delta T/T = \Delta\phi/2\pi$
- The output $X_{out}(t)$ can be represented by a DC component and a summation of sinusoidal waves
  - Sinusoidal waves will be filtered by LPF and only DC component will pass
  - DC component of $X_{out} = \frac{1}{T}\int_0^T X_{out}(t)dt = \frac{1}{T}\left(V_{CC}2\Delta T - VCC(T-2\Delta T)\right)$

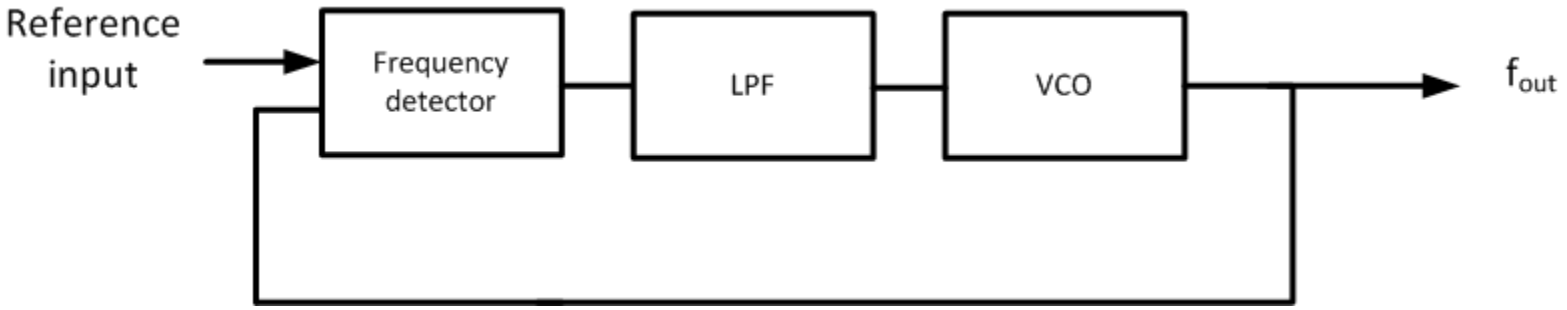
$$= 2V_{CC}\left(\frac{\Delta T}{T}\right) - V_{CC} = 4V_{CC}\left(\frac{\Delta \emptyset}{2\pi}\right) - VCC$$

XOR Phase Detector



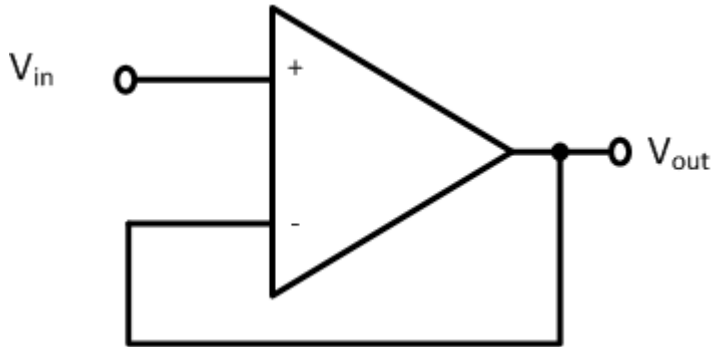
- One region will be stable while the other one will be unstable

Frequency Locked Loop



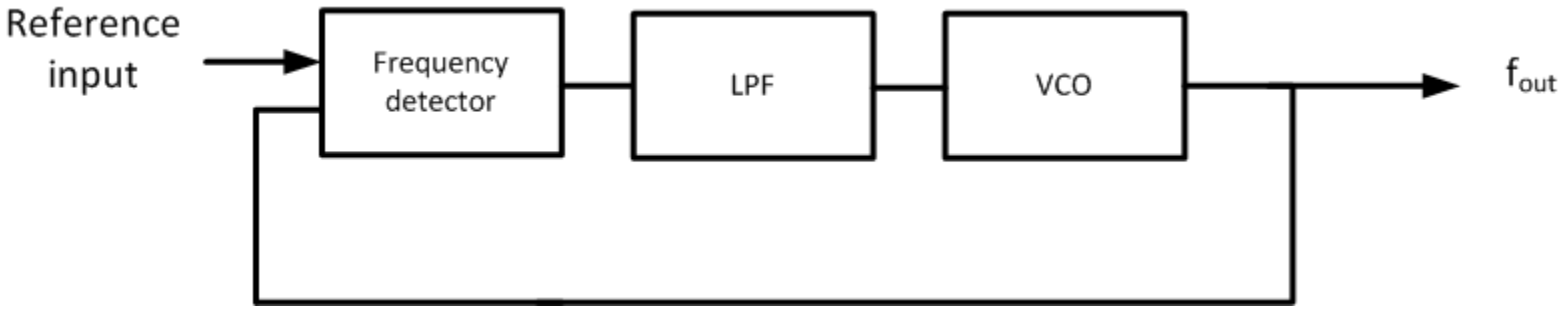
- Can we use frequency locked loop instead of phase locked loop?
  - Frequency is the differentiation of phase
  - Finite phase error exist in PLL

Frequency Locked Loop



- For an op-amp with infinite gain, $V_{out}=V_{in}$
- Due to finite op-amp gain
  - $V_{in} - V_{out} = V_{out}/A$
- For PLL due to finite loop gain, there is a finite phase difference
  - $\phi_{out}-\phi_{in} \neq 0$

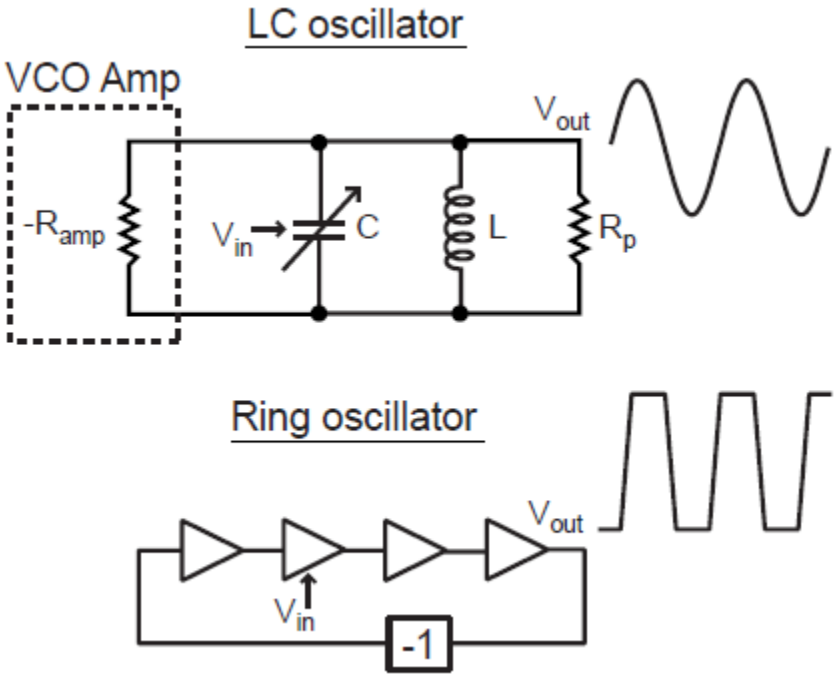
Frequency Locked Loop

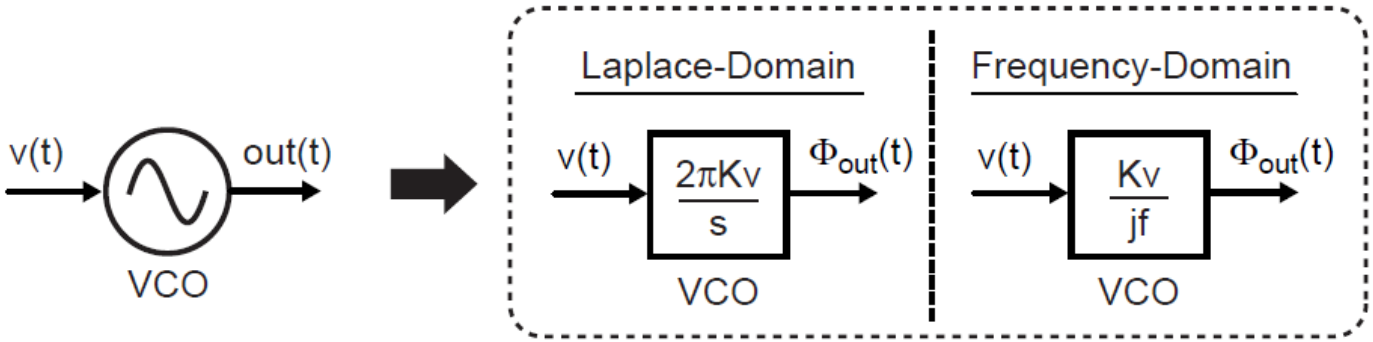


- For PLL with finite gain
  - ϕ_{out}-ϕ_{in} = Constant, then $f_{out}=d\phi_{out}/dt= f_{in}=d\phi_{in}/dt$
- For frequency locked loop, there will be a finite difference between input and output frequencies

VCO Model

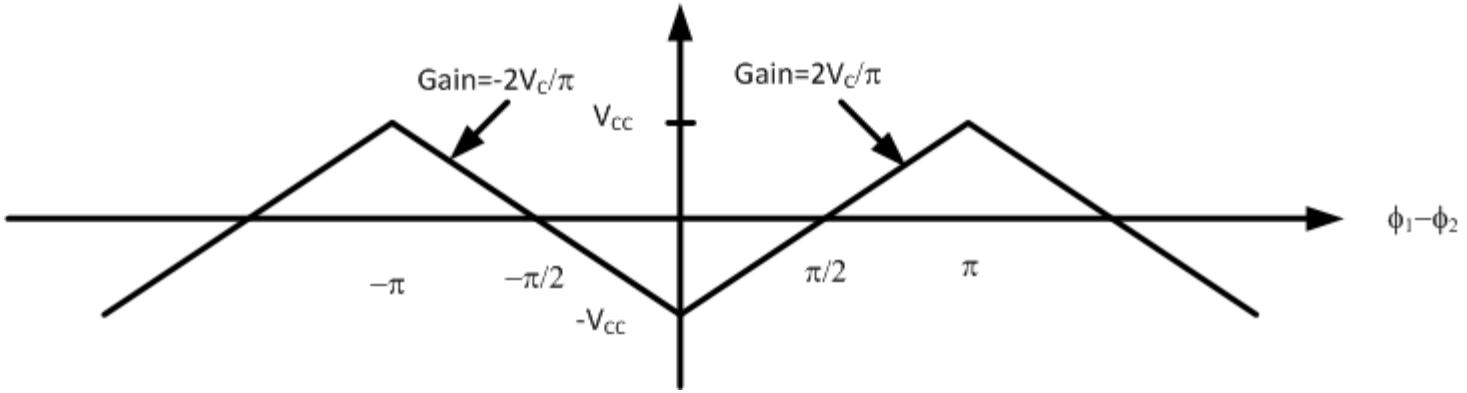
- $f_{out} = Kv_c$
- $\emptyset_{out} = \int 2\pi f_{out} dt$

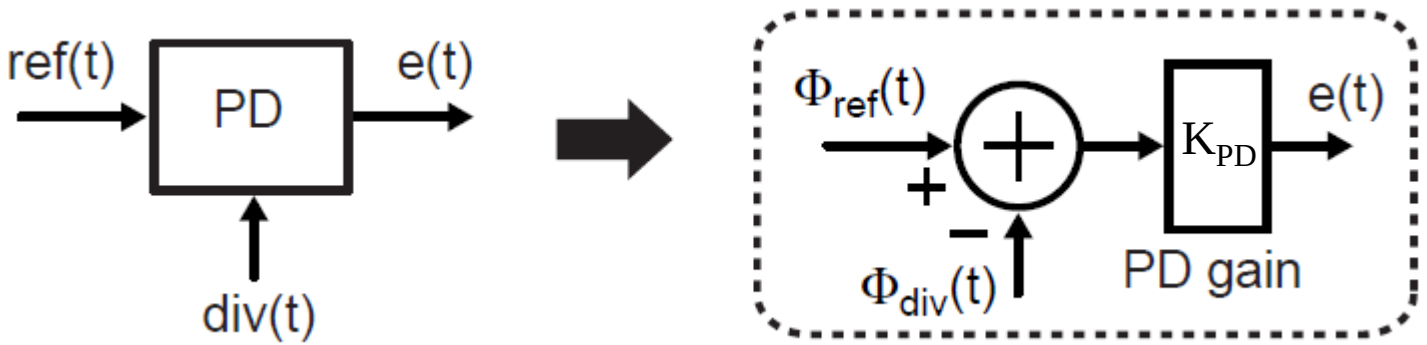




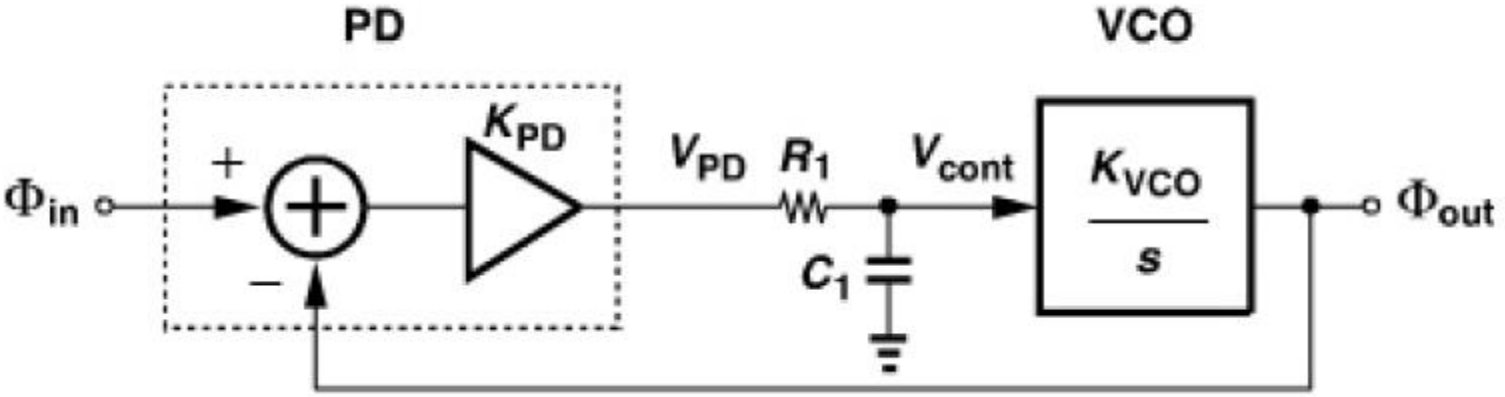
Phase Detector Model

- For $0<\phi1-\phi2<\pi$
  - Phase detector output is given by $4V_{CC}\left(\frac{\Delta\emptyset}{2\pi}\right) - VCC$
  - Phase detector can be modeled as a constant gain block





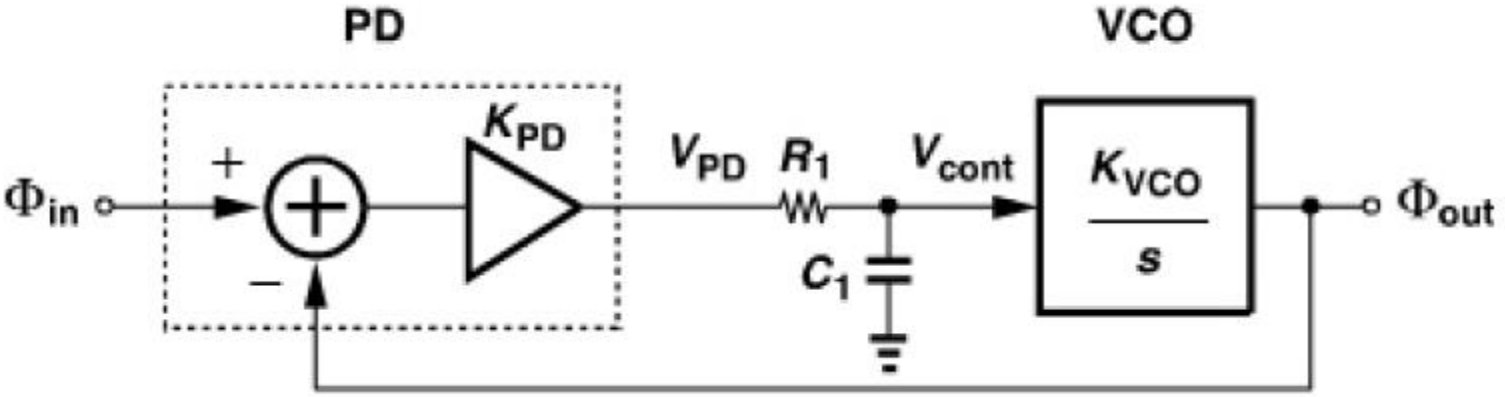
Loop Dynamics of PLL



- Phase domain is used to model the PLL
  - VCO act as an integrator
    - $f_{out}=K_{VCO}V_{in}$, or $\phi_{out}=K_{VCO}\int V_{in}dt$

$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}$$

Loop Dynamics of PLL



$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}$$

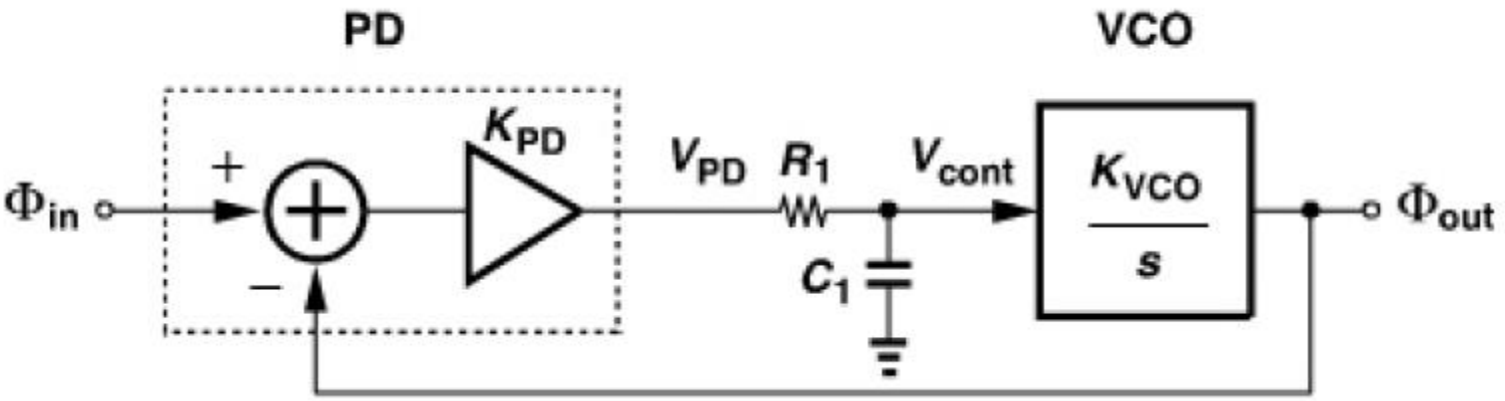
$$\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{PD}K_{VCO}}}$$

$$\frac{\phi_{out}}{\phi_{in}} = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\omega = \sqrt{K_{PD}K_{VCO}\omega_{LPF}}$$

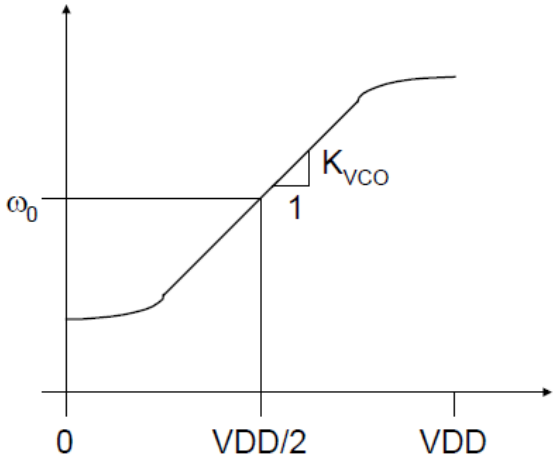
- PLL has a second order transfer function and it can have under-damped, critically damped, or over-damped response

Loop Dynamics of PLL

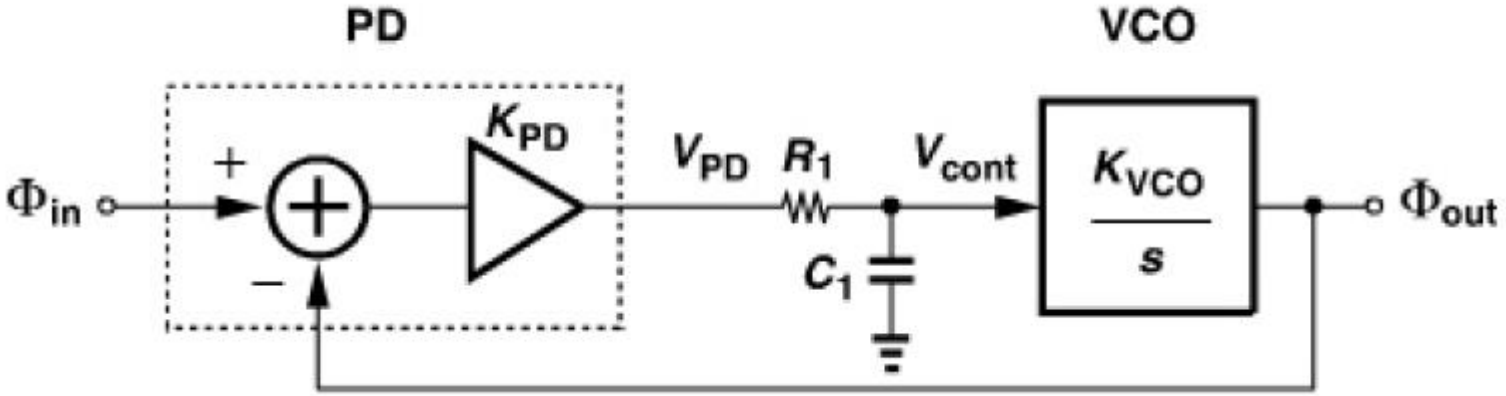


$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}}$$

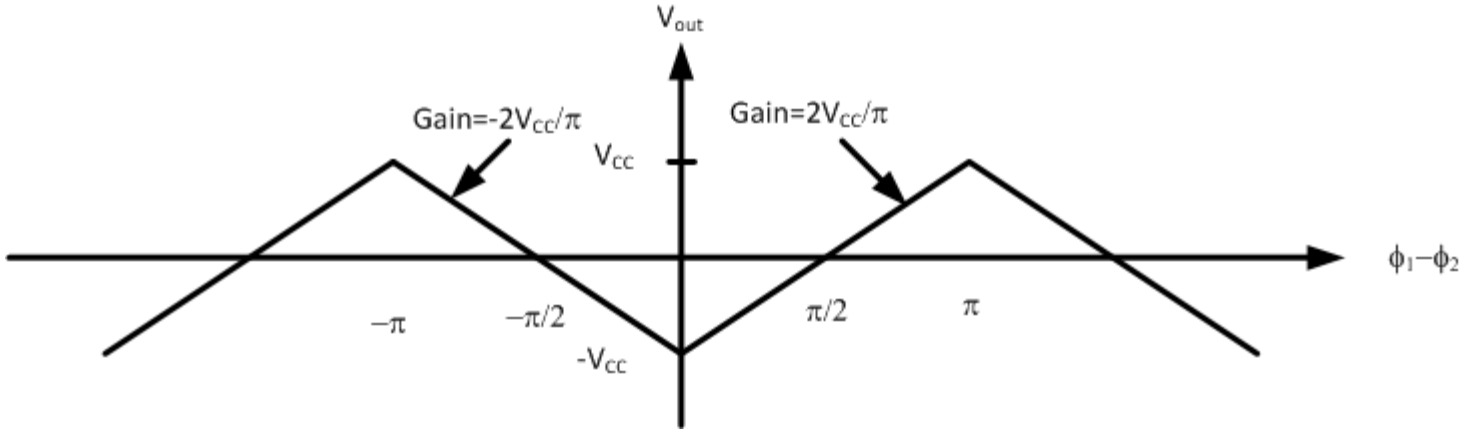
- The output frequency of VCO is given by: $\omega = \omega_0 + K_{vco}\Delta v_c$
- ω_0 is the steady state output frequency
- $K_{vco} = \Delta\omega/\Delta v_c$



XOR Phase Detector

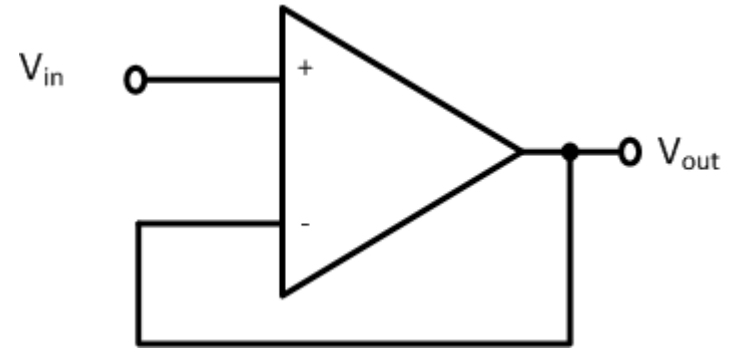


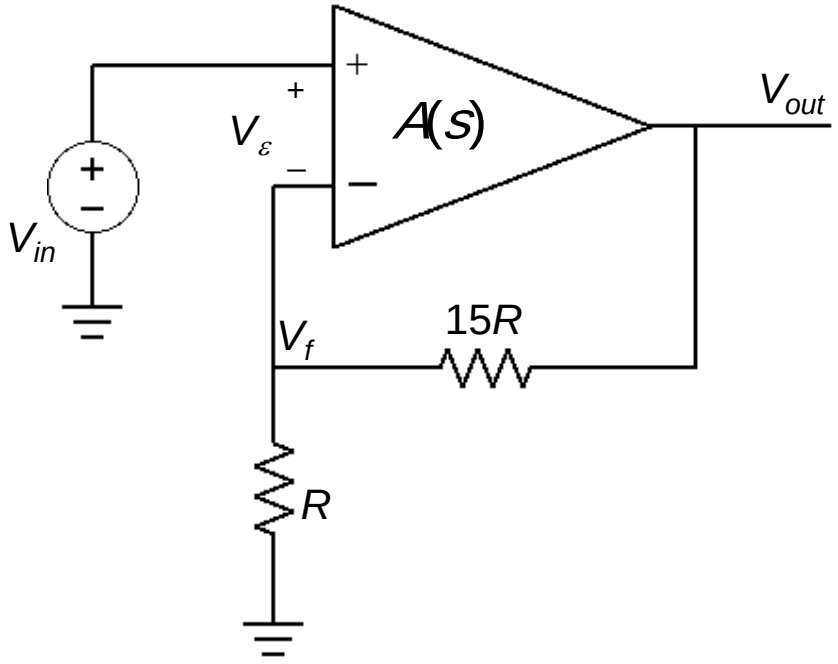
- Assume $\omega_{vco} = \omega_0 + K_{vco}V_{cont}$
- If $\omega_0=\omega_{ref}$, then $V_{cont}=0$ and $\phi_1-\phi_2=\pi/2$
- In general $V_{cont} = (\omega_{ref}-\omega_0)/K_{vco}$, $\phi_1 - \phi_2 = \frac{\pi}{2} + V_{cont}\pi/2V_{cc}$



Voltage Multiplication

- For ideal buffer $V_{out}=V_{in}$
- With voltage division network $V_{out}=16V_{in}$



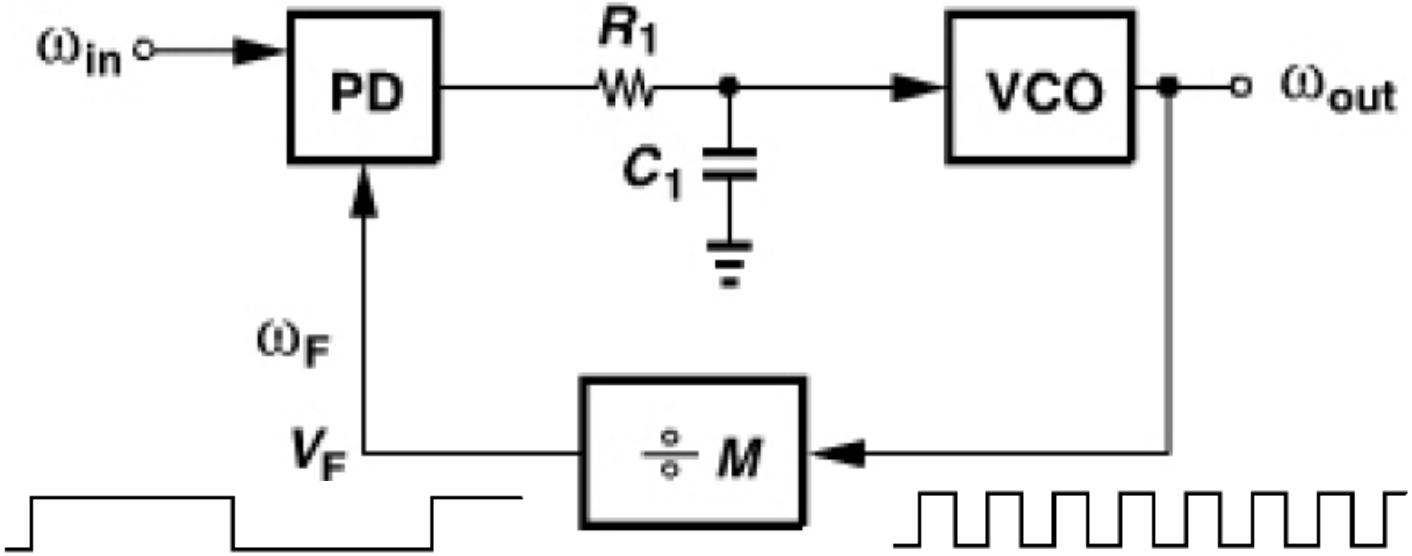


$$A(s)=\frac{A_0}{1+s/p}$$

$$\frac{V_{out}}{V_{in}}=\frac{1}{\frac{1}{A_0}+\frac{1}{N}} \longrightarrow \frac{V_{out}}{V_{in}}=N$$

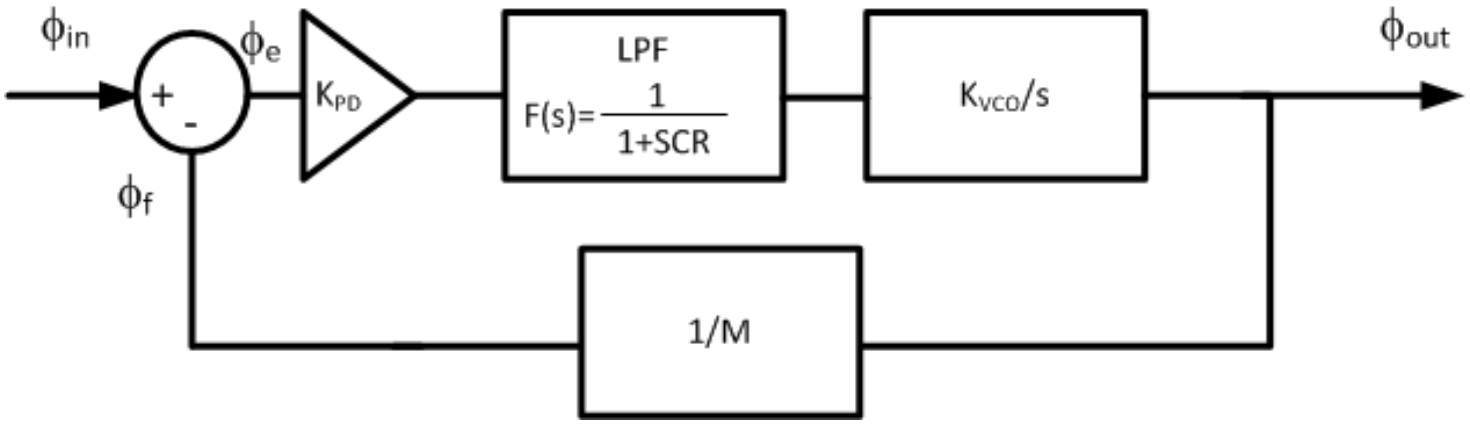
$$\frac{V_\varepsilon}{V_{in}}=\frac{1}{1+\frac{A_0}{N}} \longrightarrow \frac{V_\varepsilon}{V_{in}}=0$$

Frequency Multiplication



- $f_{out}=M\times f_{in}$
- As M changes, the output frequency also changes
  - Multiple frequencies can be generated from one reference

Frequency Multiplication



$$G(s) = \frac{K_{PD}K_{VCO}}{s + R_1C_1s^2} \qquad H(s) = \frac{1}{M}$$

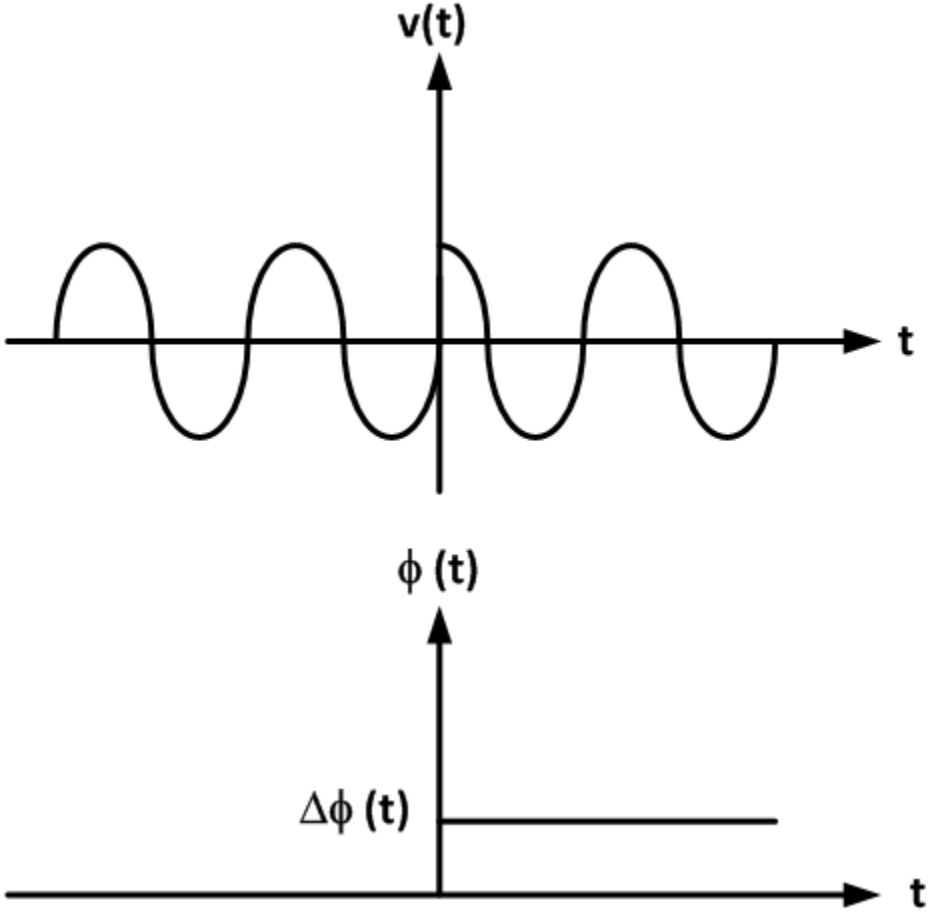
$$\frac{\phi_{out}}{\phi_{in}} = \frac{K_{PD}K_{VCO}}{R_1C_1s^2 + s + K_{PD}K_{VCO}/M} \qquad \zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}M}{K_{PD}K_{VCO}}}$$

$$\frac{\phi_{out}}{\phi_{in}} = \frac{M\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \omega_n = \sqrt{K_{PD}K_{VCO}\omega_{LPF}/M}$$

- What is the transfer function ω_{out}/ω_{in}?

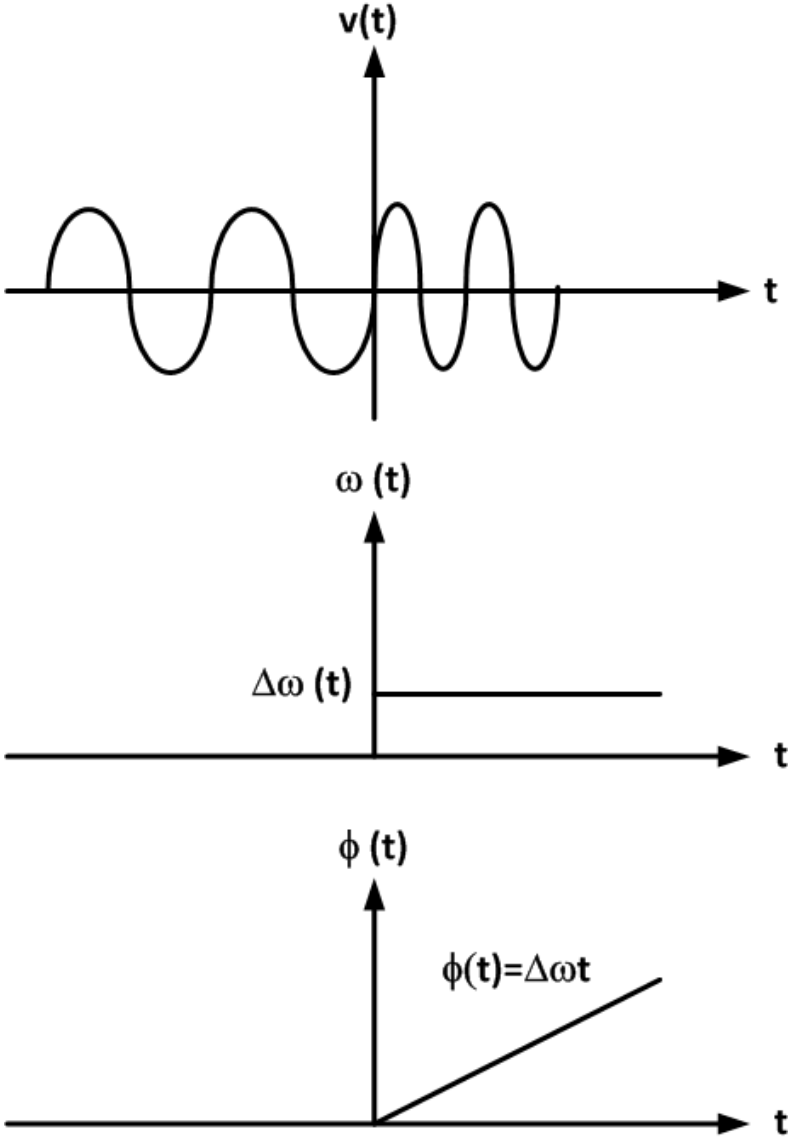
Phase Step

- *Frequency is the same, the phase take a step at t=0*
- $\emptyset(t) = \Delta\emptyset\, u(t)$
- $v(t) = \sin(\omega t + \Delta\emptyset\, u(t))$



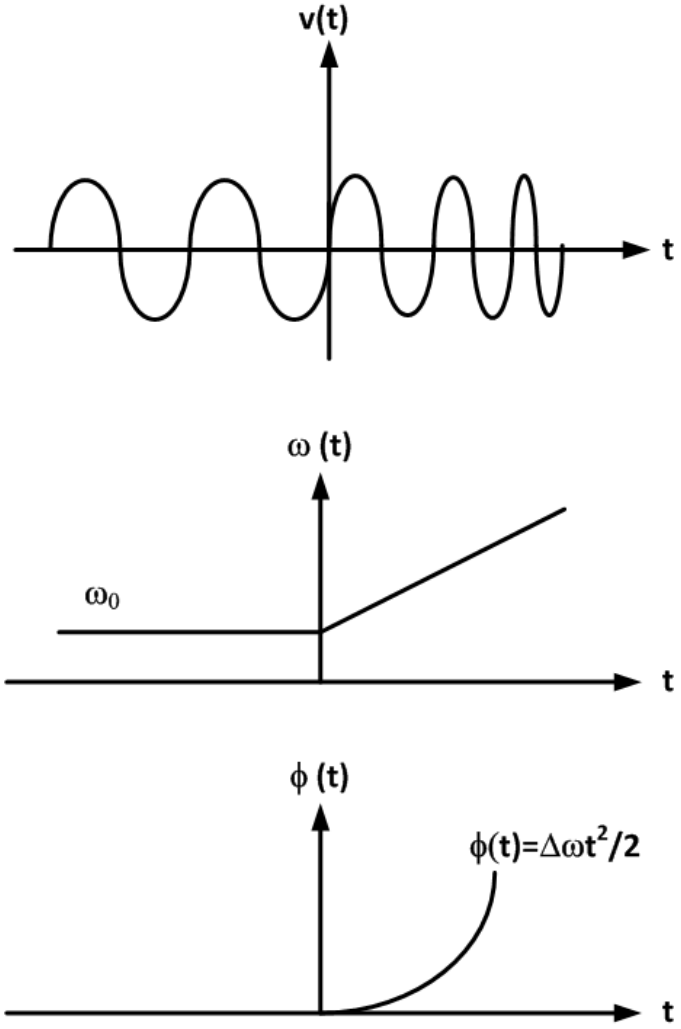
Frequency Step

- $\omega(t) = \omega_0 + \Delta\omega\, u(t)$
- $v(t) = \sin(\omega_0 t + \Delta\omega t\, u(t))$
  $= \sin(\omega_0 t + \phi(t)u(t))$
- $\phi(t) = \Delta\omega t$



Frequency Ramp

- $\omega(t) = \omega_0 + \Delta\omega t\, u(t)$
- $v(t) = \sin(\omega_0 t + \phi(t)u(t))$
- $\phi(t) = \int_0^t \Delta\omega\tau = \frac{\Delta\omega t^2}{2}$
- $v(t) = \sin(\omega_0 t + \frac{\Delta\omega t^2}{2}u(t))$



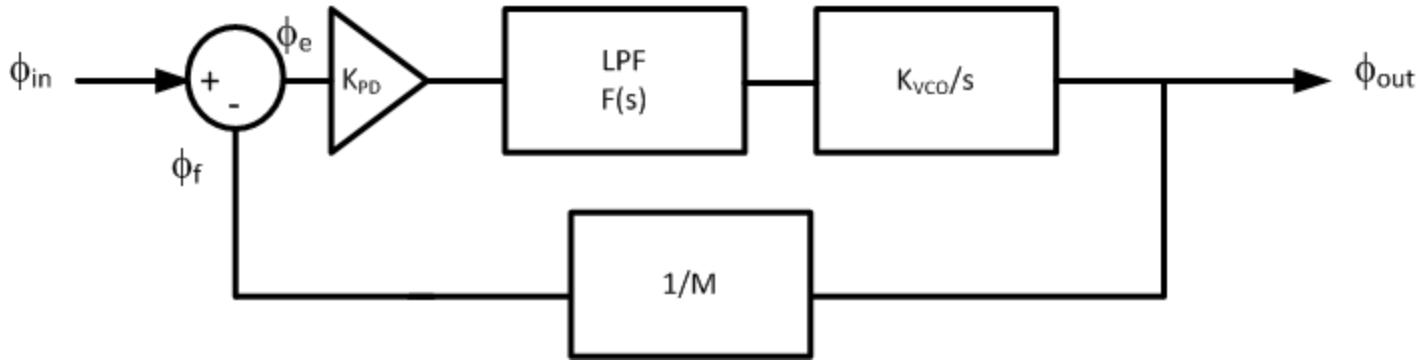
Order and Type

- Order of PLL system is the number of poles in the closed loop transfer function
- Type of PLL is the number of integrators that exists in the loop
- Order should be greater than or equal Type
- Since VCO is an integrator, PLL has to be at least type 1.
- Type 2 is the most common PLL type

Phase Error and Frequency Error

- The steady state error can be calculated from S domain $\lim_{t\to\infty} y(t) = \lim_{s\to 0} sY(s)$
- The phase error transfer function ($\phi_{e=}\phi_{in}$-ϕ_f)

$$\frac{\phi_e}{\phi_{in}} = \frac{s}{s + K_{PD}K_{VCO}F(s)/M}$$



Phase Error and Frequency Error

$$\phi_e(s) = \frac{s\phi_{in}(s)}{s + K_{PD}K_{VCO}F(s)/M}$$

$$\lim_{t\to\infty}\phi_e(t) = \lim_{s\to 0} s\phi_e(s) = \lim_{s\to 0}\frac{s^2\phi_{in}(s)}{s + K_{PD}K_{VCO}F(s)/M}$$

- For a phase step $\phi_{in}(s)=\Delta\phi/s$

$$\lim_{t\to\infty}\phi_e(t) = \lim_{s\to 0}\frac{s\Delta\phi}{s + K_{PD}K_{VCO}F(s)/M} = 0 \quad (\textit{for } F(0)\neq 0)$$

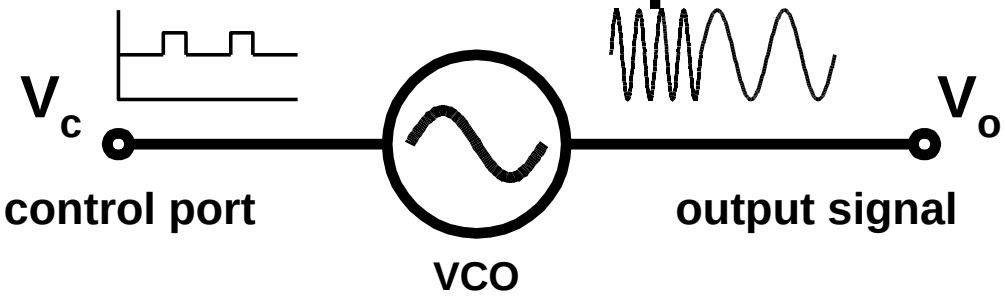
- For a frequency step $\omega(s)=\Delta\omega/s$ or $\phi_{in}(s)=\Delta\omega/s^2$

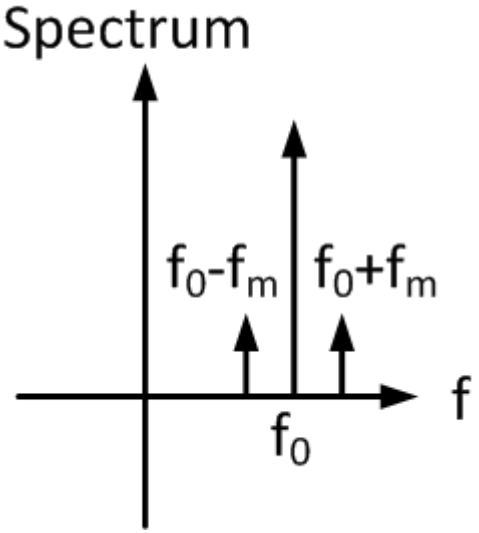
$$\lim_{t\to\infty}\phi_e(t) = \lim_{s\to 0}\frac{\Delta\omega}{s + K_{PD}K_{VCO}F(s)/M} = \frac{M\Delta\omega}{K_{PD}K_{VCO}F(0)}$$

Phase Error and Frequency Error

- For frequency step, the phase error is zero if $F(0)=\infty$, or there is 1/s term in the filter response
- Type II PLL is commonly used used since there is two poles at the origin and hence no static phase error for frequency step

PLL Spur





$$v_o(t) = V_o \cos(\omega_o t + K' \int v_c(t) dt)$$

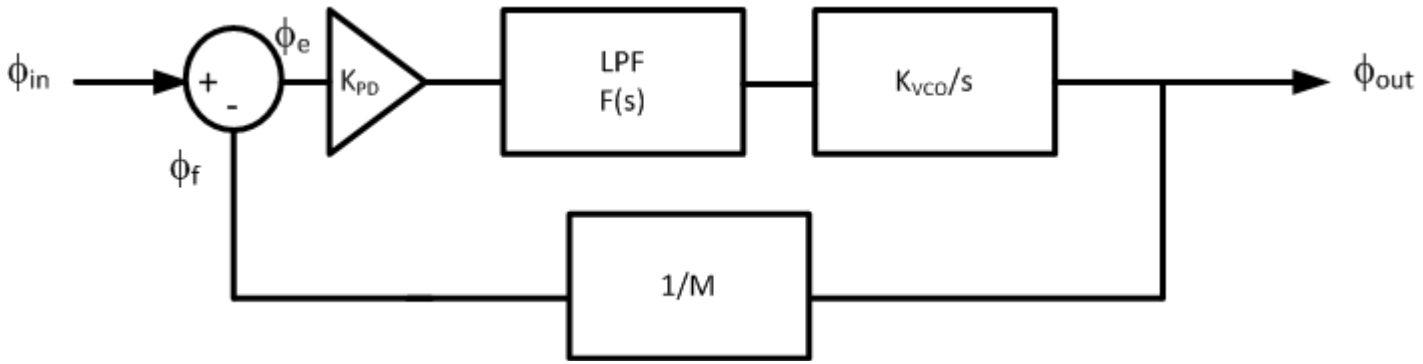
$$= V_o \cos(\omega_o t + K \sin \omega_m t)$$

$$\approx V_o (\cos \omega_o t - \sin \omega_o t \cdot K \sin \omega_m t)$$

$$= V_o \left(\cos \omega_o t - \frac{K}{2} \cos(\omega_o - \omega_m)t + \frac{K}{2} \cos(\omega_o + \omega_m)t \right)$$

- VCO output is modulated by coupled signal on control port.
- Two sideband tones at $\pm\omega_m$ away from the center frequency

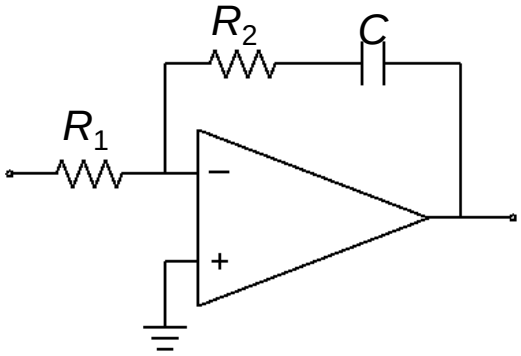
Type II PLL



Active loop filter:

$$F(s) = -\frac{1 + sCR_2}{sCR_1}$$

additional pole at 0 ⇒ Type II PLL



- Closed loop transfer function is given by

$$T(s) = \frac{N\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2} \qquad \zeta = \frac{R_2}{2R_1}\sqrt{K_{PD}K_{VCO}R_1C/N} \qquad \omega_n = \sqrt{K_{PD}K_{VCO}/R_1CN}$$

Settling time

DEFINITION: The time required for the PLL to change its output frequency from $f_{out}(0)$ to $f_{out}(\infty)$ within a frequency error smaller or equal to ε

The closed loop transfer function is:

$$T(s) = \frac{N\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2 + 2\zeta\omega_n s + \omega_n^2}$$

$$\varepsilon \geq \left| f_{out}(t) - f_{out}(\infty) \right|$$

Changing the division ratio from N to N+ΔN is equivalent to a frequency step from f_{ref} to $(1+ \Delta N/N)f_{ref}$

The output frequency of the VCO

$$f_{out} = \left(N + \Delta N\right) f_{ref} = N\left\{\left(1 + \frac{\Delta N}{N}\right) f_{ref}\right\}$$

Settling time

The PLL responds to the input frequency step as

$$\Delta f_{out}(s) = f_{out}(s) - Nf_{ref} = \frac{\Delta N f_{ref}}{N \cdot s} T(s)$$

$$\Delta f_{out}(s) = \Delta N f_{ref} \frac{\left(2\zeta\omega_n s + \omega_n^2\right)}{s(s^2 + 2\zeta\omega_n s + \omega_n^2)}$$

The steady state frequency can be found using the final value theorem

$$\Delta f_{out}(\infty) = f_{out}(\infty) - Nf_{ref} = \lim_{s\to 0} s\left[\frac{\Delta N f_{ref}}{N \cdot s} T(s)\right] = \Delta N f_{ref}$$

and the lock time can be calculated as:

$$t_{lock} = \left| L^{-1}\left\{\Delta f_{out}(s)\right\} - \Delta f_{out}(\infty)\right| < \varepsilon$$

$$t_{lock} = \left| L^{-1}\left\{\phi_e(s)\right\}\right| < \varepsilon$$

Settling time

$$\phi_e(s) = \frac{s^2\phi_{in}(s)}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{\Delta\omega}{s^2 + 2\zeta\omega_n s + \omega_n^2} \quad for \ \ frequency\ step\ \phi_{in}(s) = \Delta\omega / s^2$$

Depending on the value of the damping factor ξ, there are three different cases

$0 < \xi < 1$	Underdamped
$\xi = 1$	Critically Damped
$\xi > 1$	Overdamped

The poles of the transfer function for each case are

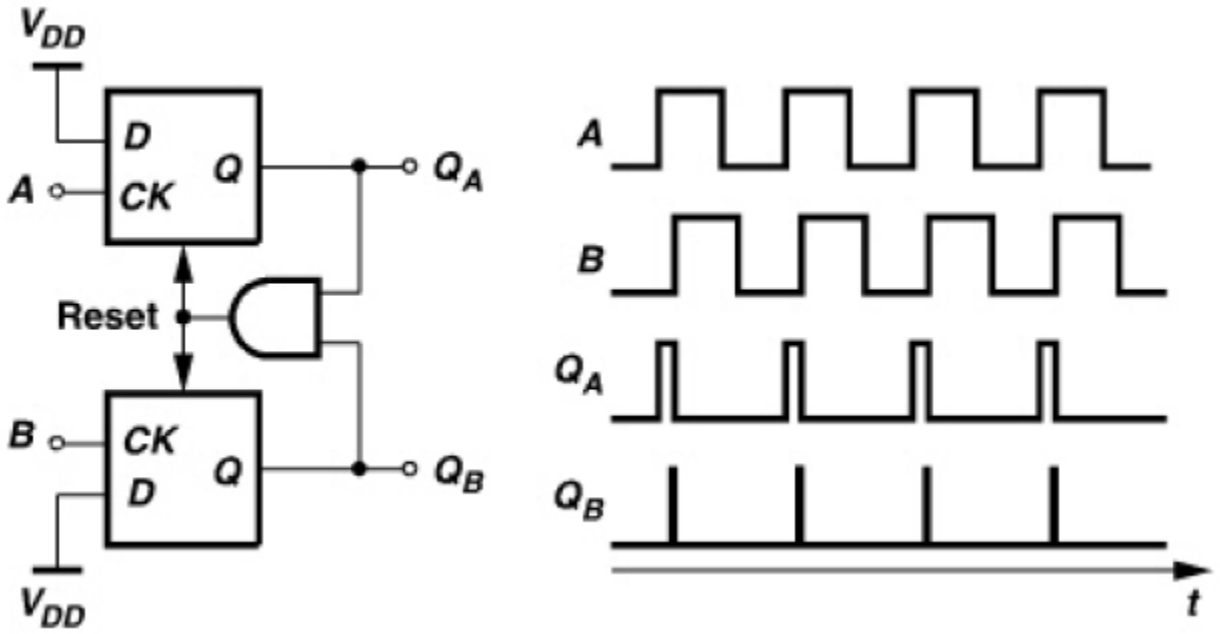
$$\omega_{1,2} = \begin{cases} -\omega_n\left(\zeta \pm j\sqrt{1-\zeta^2}\right) & \zeta < 1 \\ -\zeta\omega_n & \zeta = 1 \\ -\omega_n\left(\zeta \pm \sqrt{\zeta^2 - 1}\right) & \zeta > 1 \end{cases}$$

$$\begin{aligned}
\Delta\omega_{out}(t) &= \Delta\omega_{in}u(t) - \Delta\omega_{in}\left[\cos\left(\sqrt{1-\zeta^2}\omega_n t\right)\right. \\
&\quad \left. - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\sqrt{1-\zeta^2}\omega_n t\right)\right] e^{-\zeta\omega_n t}u(t) \quad \zeta < 1 \\
&= \Delta\omega_{in}u(t) - \Delta\omega_{in}(1-\omega_n t)e^{-\zeta\omega_n t}u(t) \quad \zeta = 1 \\
&= \Delta\omega_{in}u(t) - \Delta\omega_{in}\left[\cosh\left(\sqrt{\zeta^2-1}\omega_n t\right)\right. \\
&\quad \left. - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh\left(\sqrt{\zeta^2-1}\omega_n t\right)\right] e^{-\zeta\omega_n t}u(t) \quad \zeta > 1.
\end{aligned}$$

Fastest settling around $\xi=1$

Phase Frequency Detector

- If input and output frequencies are far from each other, phase detection is not enough
- Phase frequency detector (PFD) work with signal edges



Phase Frequency Detector

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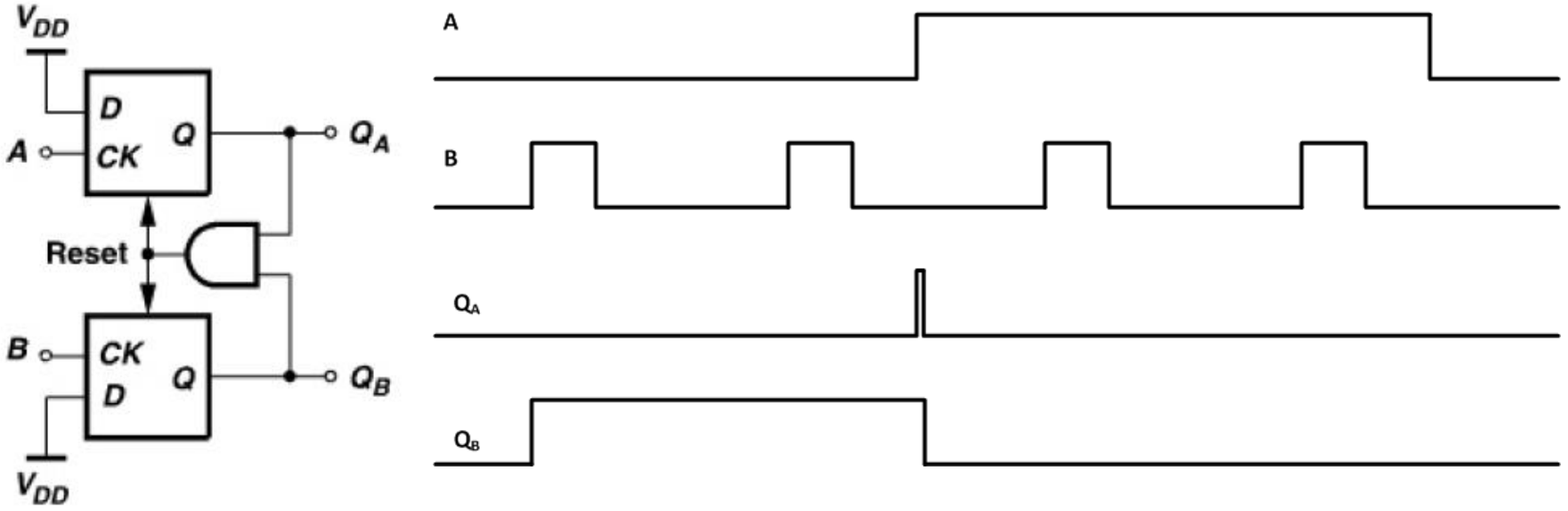
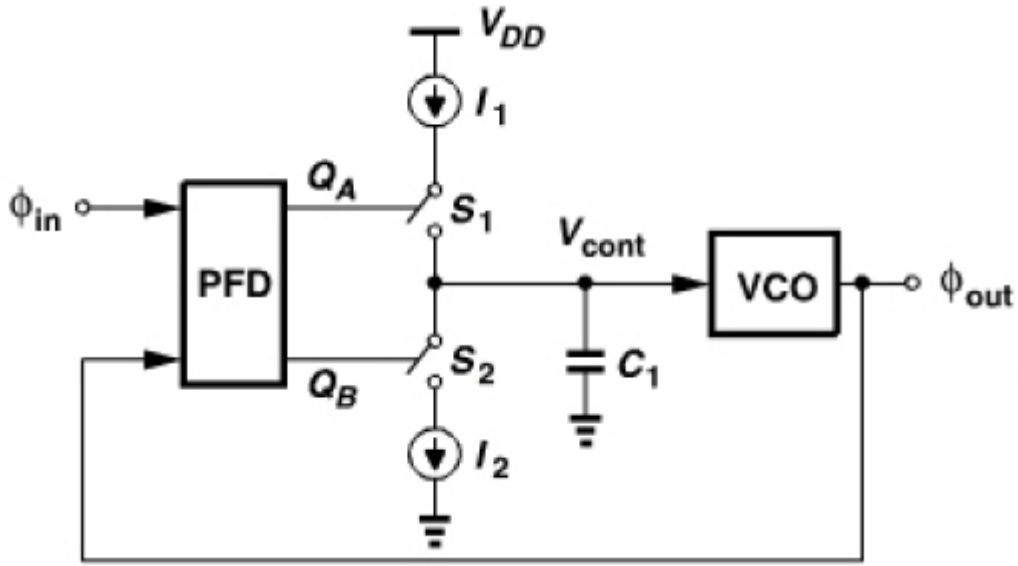
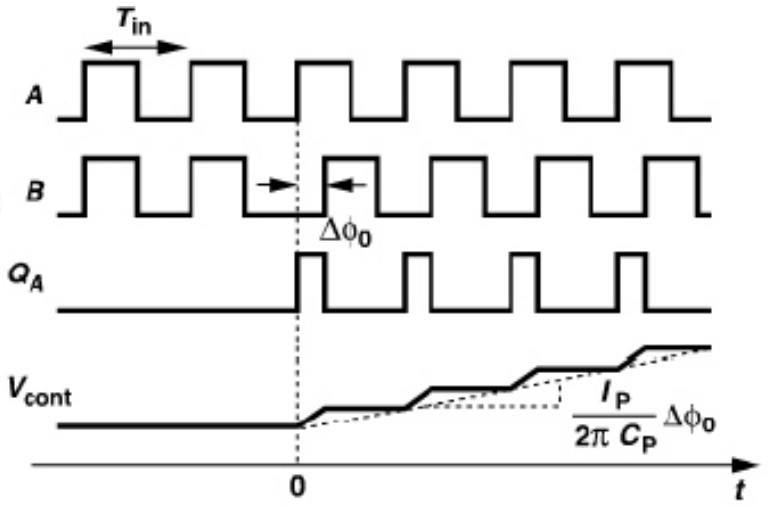


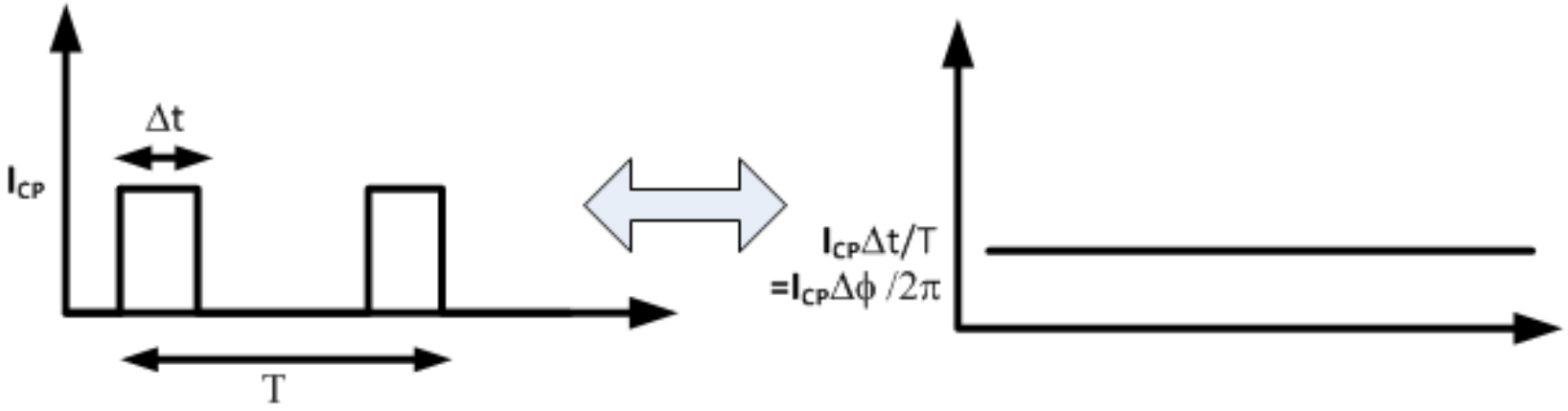
Charge Pump PLL





- Note that the current consists of pulses
  - Continuous time approximation will be used ($BW << F_{ref}$)

Charge Pump PLL

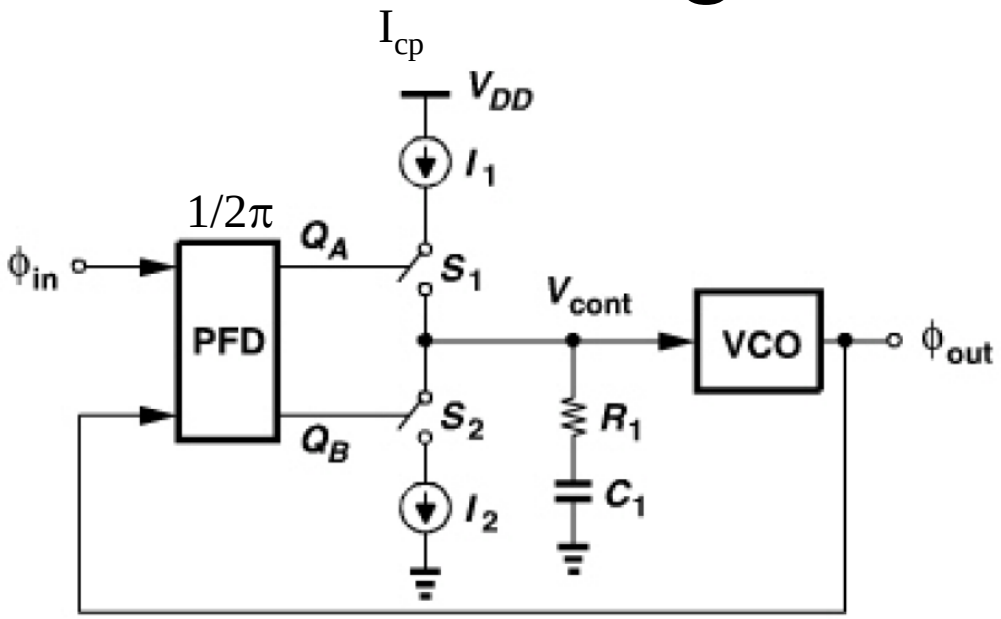


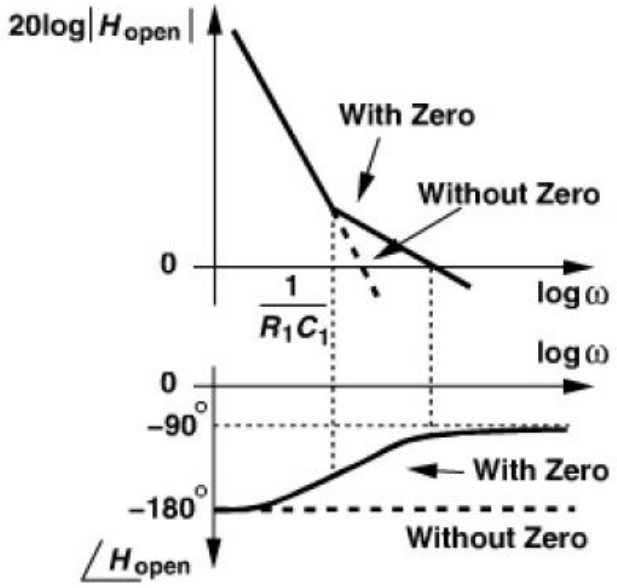
- If the phase difference between two signals is $\Delta\phi_0$, then time difference is $\Delta t=\Delta\phi\times T/2\pi$
  - I_{out} of CP=$I_{cp}\Delta t/T=I_{cp}\Delta\phi/2\pi$
  - Gain of PFD+CP= $I_{out}/\Delta\phi=I_{cp}/2\pi$

Charge Pump PLL

- $G(s) = \frac{I_{cp}}{2\pi}\frac{1}{sC_1}\frac{K_{VCO}}{s}$
- $T(s) = \frac{G(s)}{1+G(s)} = \frac{I_{cp}K_{VCO}}{2\pi C_1 s^2 + I_{cp}K_{VCO}}$
- Two poles at origin lead to unstable response

Charge Pump PLL

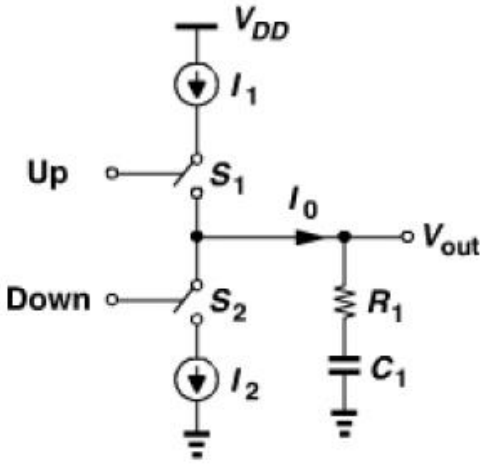


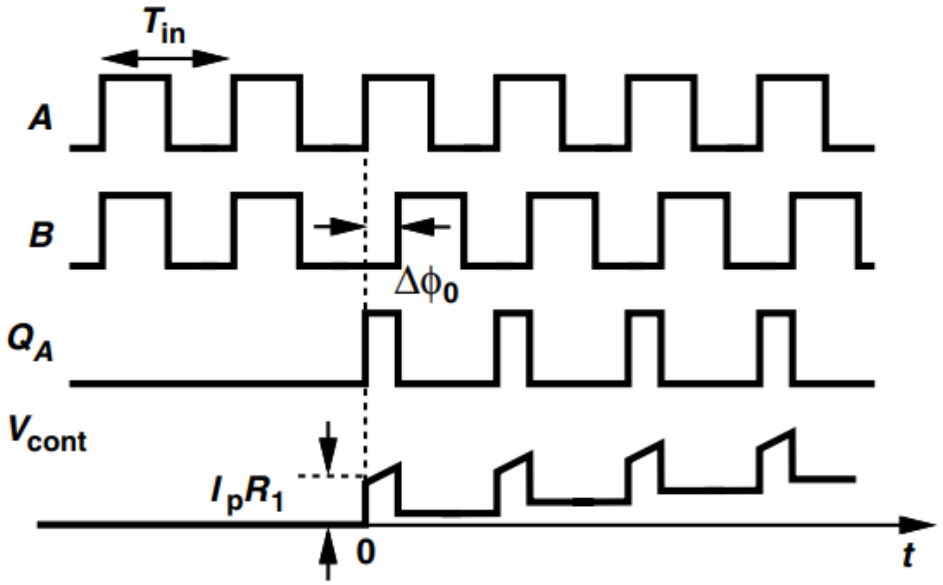


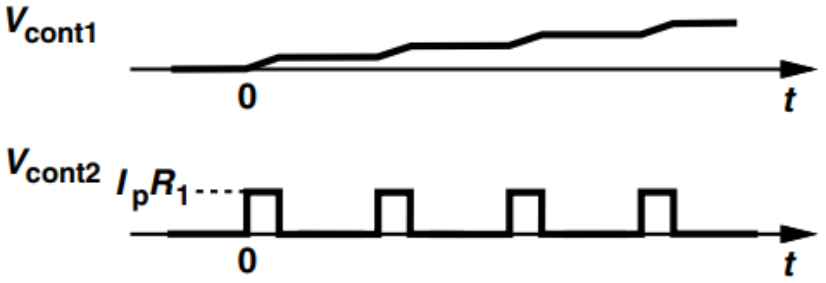
- Zero is added to stabilize response
- $G(s) = \frac{I_{cp}}{2\pi}\frac{1}{sC_1}\frac{K_{VCO}(1+sR_1C_1)}{s}$
- $T(s) = \frac{G(s)}{1+G(s)} = \frac{(I_{cp}K_{VCO}/2\pi C_1)(1+sR_1C_1)}{s^2+\left(\frac{I_{cp}K_{VCO}R_1}{2\pi}\right)s+\frac{I_{cp}K_{VCO}}{2\pi C_1}}$

Charge Pump PLL

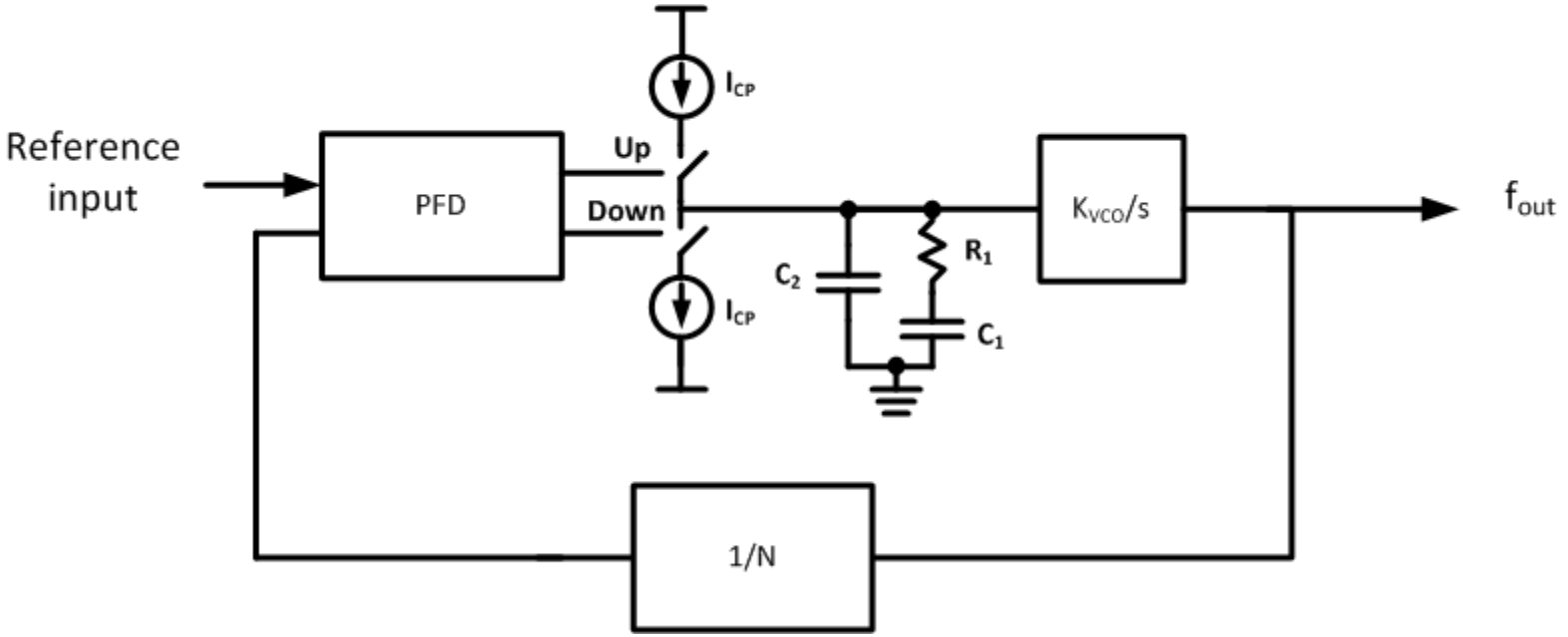
- Ripples exist due to R_1







Charge Pump PLL

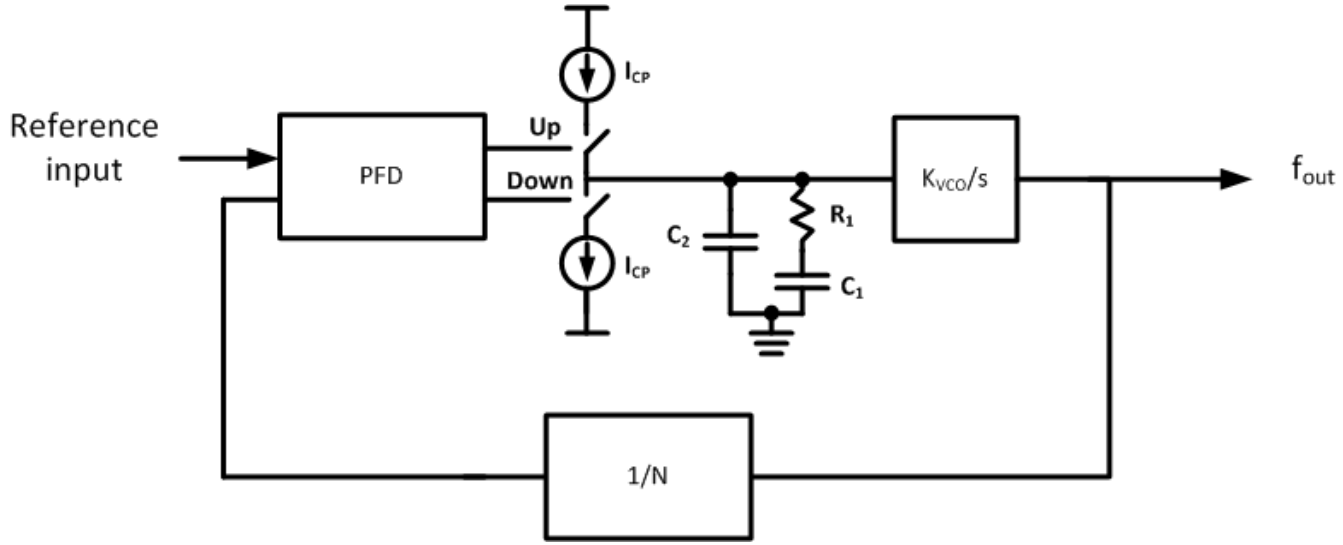


- Addition of R_1 will cause ripples on VCO control line
- Addition of C_2 will help to smooth ripples

$$F(s) = \frac{1}{s(C_1 + C_2)} \cdot \frac{1 + s/\omega_z}{(1 + s/\omega_p)} \qquad \omega_z = \frac{1}{R_1 C_1} \qquad \omega_p = \frac{1}{R_1 (C_1 C_2)/(C_1 + C_2)} \approx \frac{1}{R_1 C_2}$$

Charge Pump PLL

- C_2 is added to minimize ripples ($C_2 << C_1$)
- T_{OL} is the open loop gain G(s)*H(s)



$$T_{ol}(s) = \frac{IK_{VCO}}{2\pi \cdot N \cdot s} \cdot \frac{1}{C_1 + C_2} \cdot \frac{1 + s/\omega_z}{s(1 + s/\omega_p)} = \frac{K_D K_{VCO}(1 + s/\omega_z)}{s^2(1 + s/\omega_p)} \quad where\ K_D = \frac{I}{2\pi \cdot N \cdot (C_1 + C_2)} \approx \frac{I}{2\pi \cdot N \cdot C_1}$$

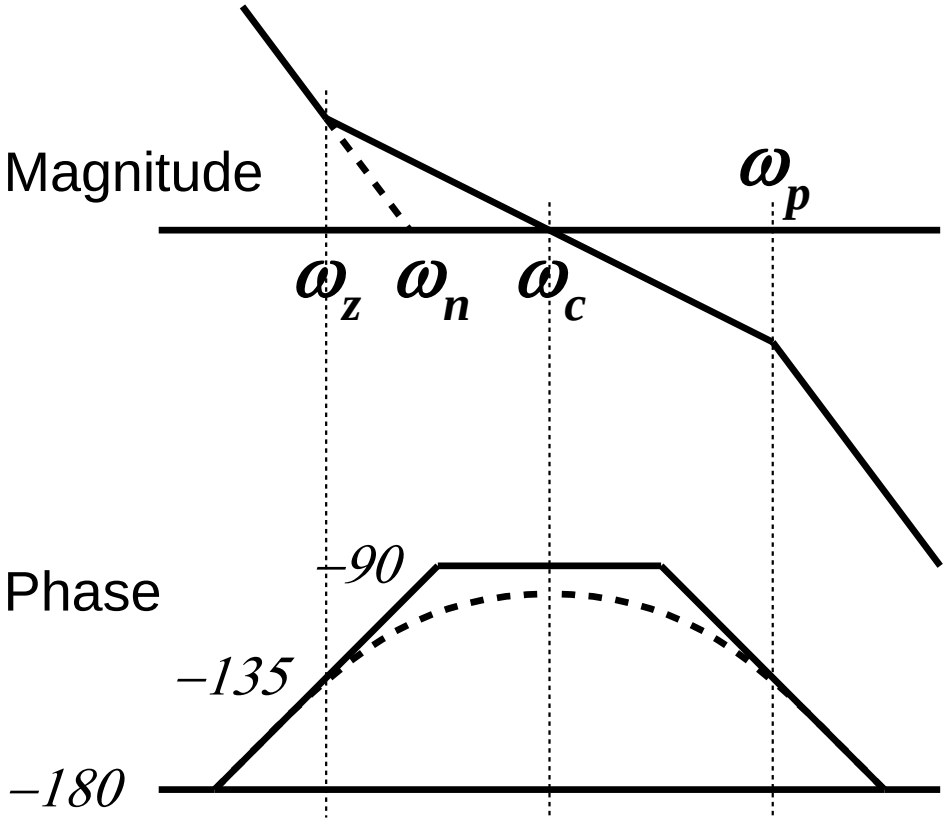
$$\phi_m = \tan^{-1}\left(\frac{\omega_c}{\omega_z}\right) - \tan^{-1}\left(\frac{\omega_c}{\omega_p}\right) \qquad \omega_c = K_D K_{VCO} / \omega_z$$

- Max phase margin at $\omega_c = \sqrt{\omega_p \omega_z} = \sqrt{b}\omega_z,\ b = \omega_p / \omega_z$

Charge Pump PLL

$$T_{ol}(s) = G(s)H(s) \approx K_D K_{VCO} \frac{(1+s/\omega_z)}{s^2(1+s/\omega_p)} = \omega_n^2 \frac{(1+s/\omega_z)}{s^2(1+s/\omega_p)}$$

- Magnitude
- Phase



- Natural frequency

$$\omega_n = \sqrt{K_D K_{VCO}} = \sqrt{\frac{IK_{vco}}{2\pi C_1 N}}$$

- Crossover frequency

$$\omega_c \approx \frac{\omega_n^{\,2}}{\omega_z}$$

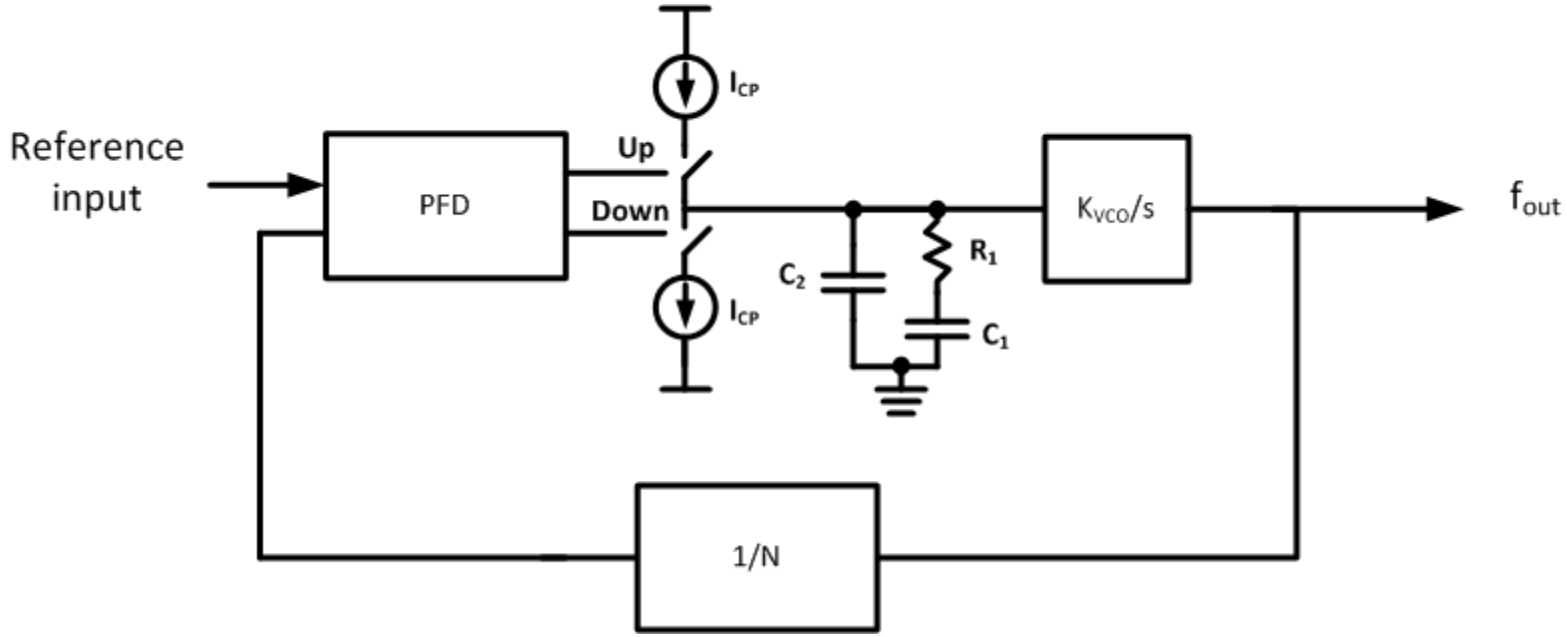
- Zero frequency

$$\omega_z = \frac{1}{R_1 C_1}$$

- Pole frequency

$$\omega_p \approx \frac{1}{R_1 C_2}$$

Charge Pump PLL



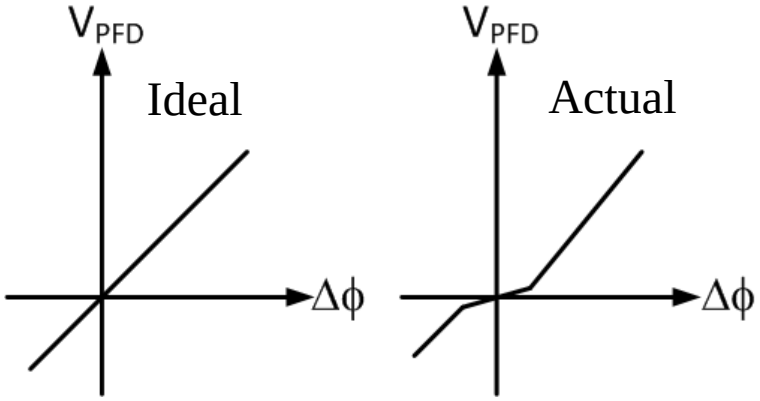
$$G(s) = N\omega_n^2 \frac{(1+s/\omega_z)}{s^2(1+s/\omega_p)}, H(s) = 1/N$$

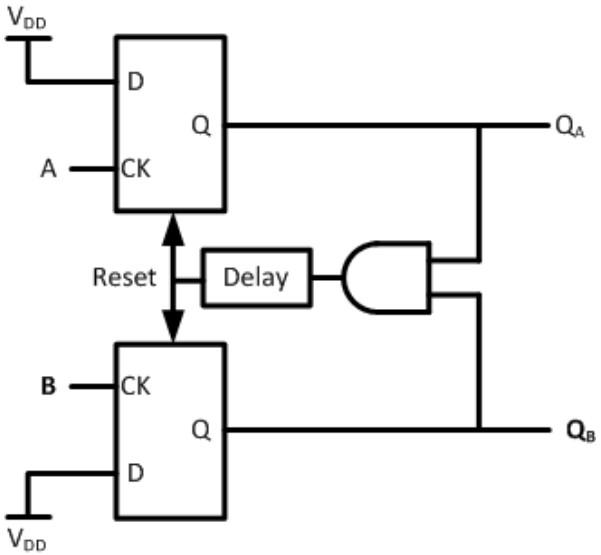
$$T_{cl}(s) = N\frac{(1+s/\omega_z)}{1+s/\omega_z + s^2/K_D K_{VCO} + s^3/\omega_p K_D K_{VCO}} \approx N\frac{(1+s/\omega_z)}{1+s/\omega_z + s^2/\omega_n^2} \quad (\omega_p >>)$$

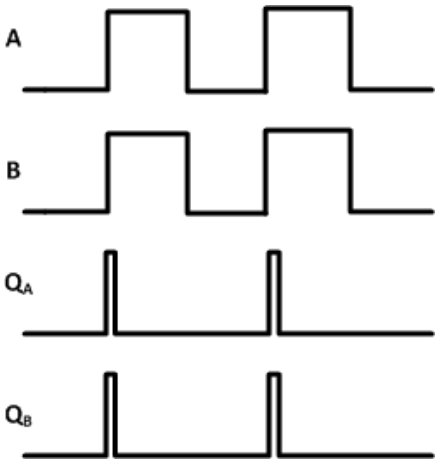
$$T_{cl}(s) = N\frac{\left(\omega_n^2 + s(\omega_n^2/\omega_z)\right)}{s^2 + s(\omega_n^2/\omega_z) + \omega_n^2}, \quad \omega_n = \sqrt{K_D K_{VCO}}, \; 2\zeta\omega_n = \omega_n^2/\omega_z = \omega_c \Rightarrow \zeta = \omega_c/2\omega_n$$

PFD Dead Zone

- When phase error approaches zero output of PFD is very narrow pulses
- Due to finite time needed for switches, charge pump doesn't respond and loop is open
  - Loop lose accuracy and will have higher noise
- Delay should be added to ensure minimum pulse out of PFD

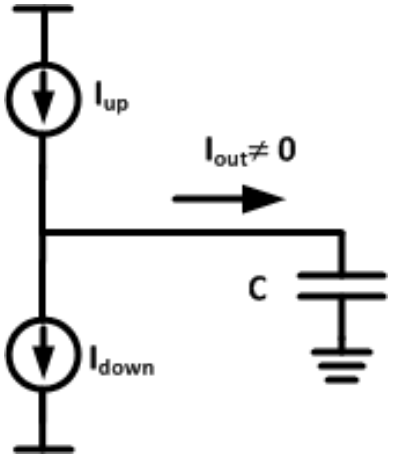


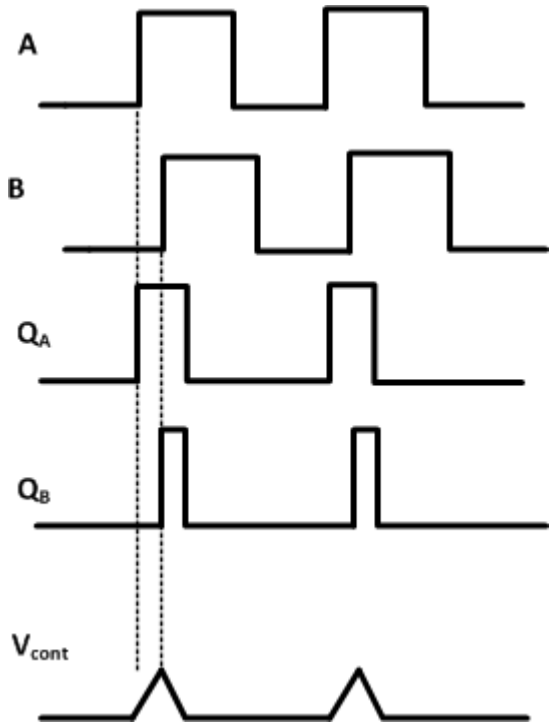




Charge Pump Circuit

- When PLL is in lock condition up and down pulses are the same
  - For a small period of time both current sources are switched ON
- Due to mismatch between up and down current, I_{out} will have a finite value $\neq 0$
- In steady state V_{cont} should be periodic, i.e. $V_{cont}(nT)=V_{cont}((n+1)T)$



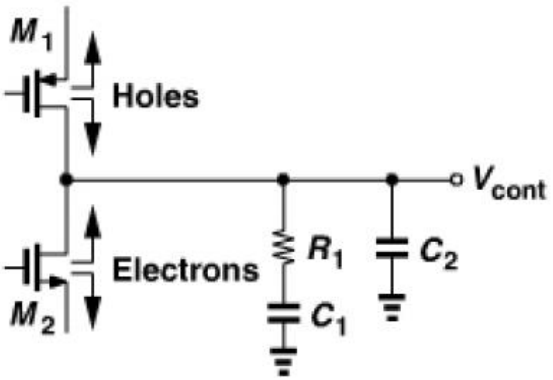


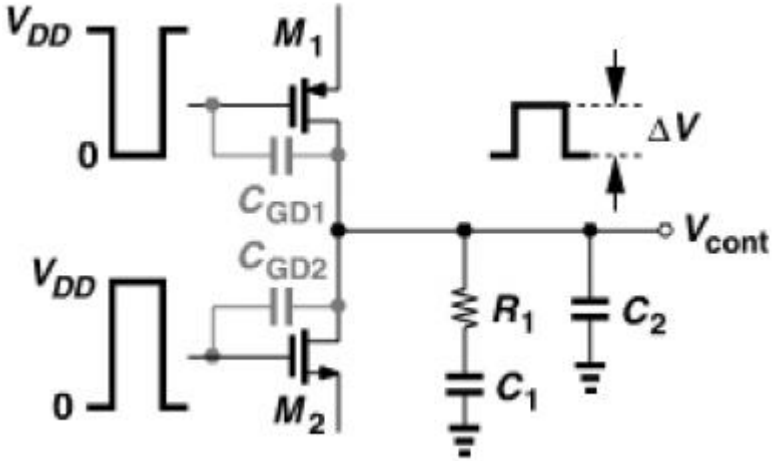
Charge Pump Circuit Design

- Current sources should have high output resistance
  - Cascode current source are commonly used
- Charge injection and charge sharing could be a problem

Charge Pump Circuit Design

- Charge sharing when devices turn ON or OFF
  - Charges on NMOS and PMOS gets to V_{cont} node
  - At different values of V_{cont}, Charges on PMOS and NMOS are different



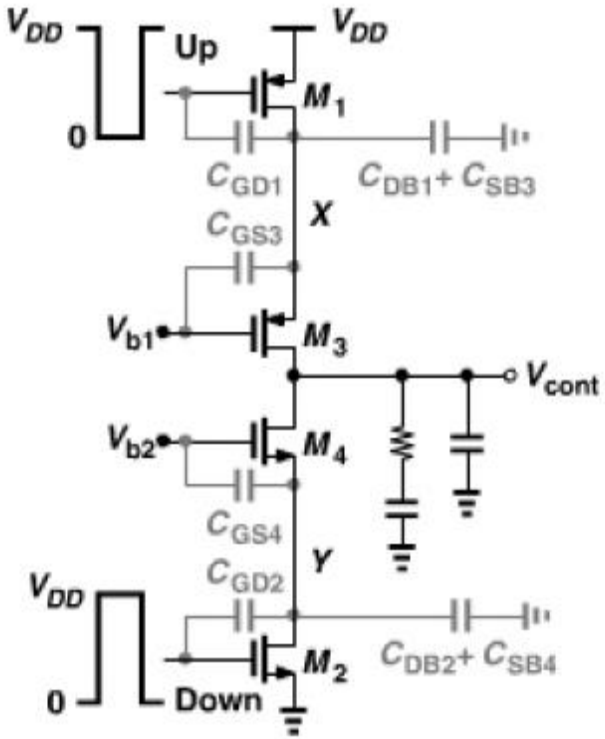


$$\Delta V = \frac{C_{GD2} - C_{GD1}}{C_{GD1} + C_{GD2} + C_2}$$

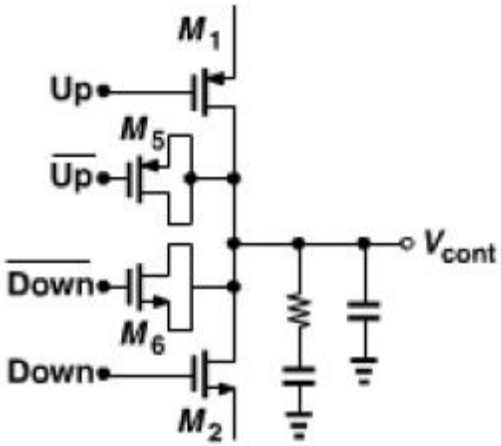
After charge sharing between C_1 and C_2 $\quad \Delta V' = \frac{C_{GD2} - C_{GD1}}{C_{GD1} + C_{GD2} + C_2 + C_1}$

Charge Pump Circuit Design

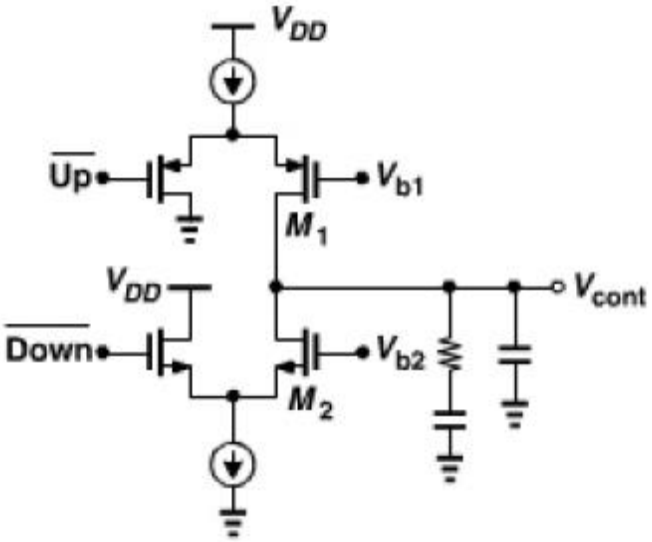
- Solutions to charge injection issue



1- Move switch away from V_{cont}



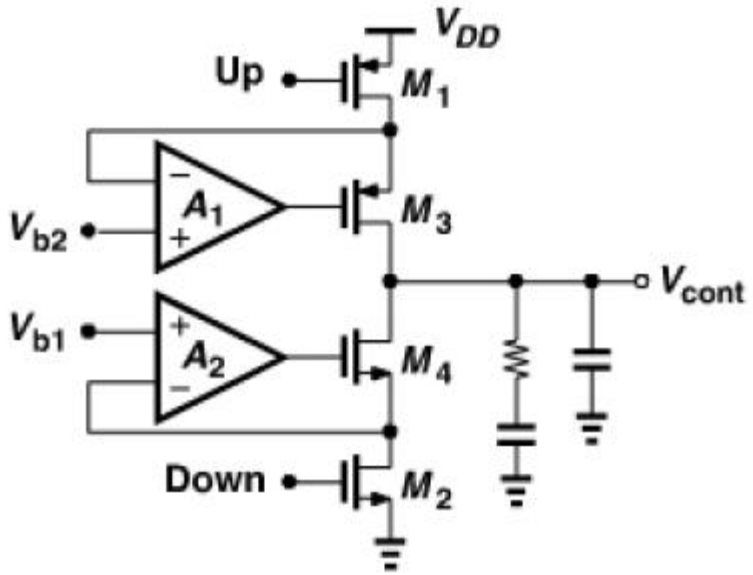
2- Use dummy switch $W_5=0.5\ W_1$



3- Use differential pair

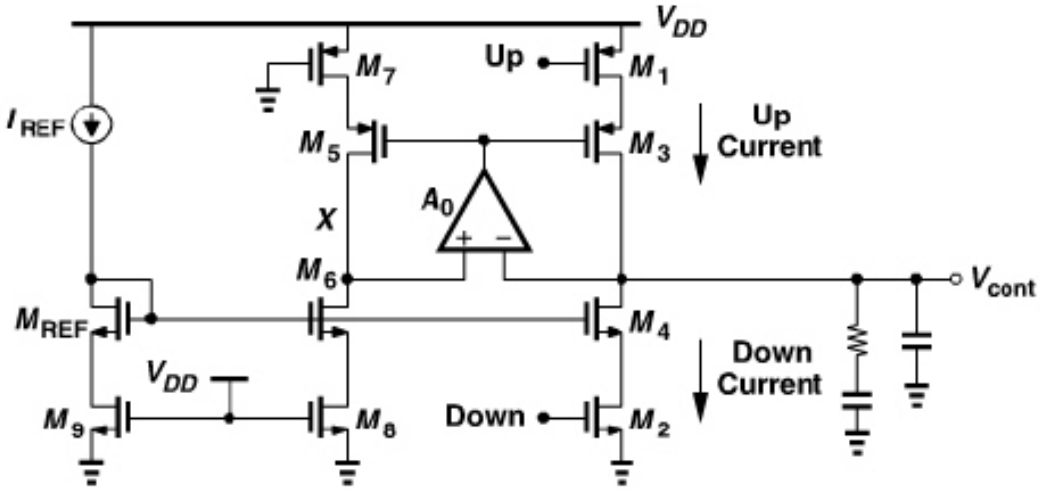
Charge Pump Circuit Design

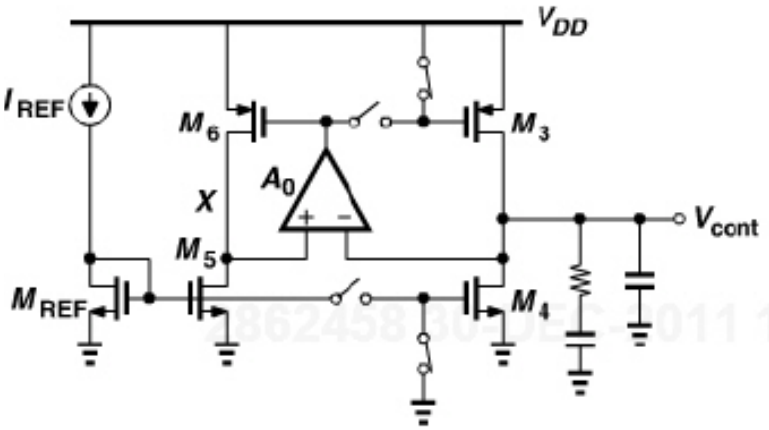
- Matching between up and down currents is very important
  - Output impedance should be very high
  - Regulated cascode current sources can be used
    - BW of amplifiers A1 and A2 should be very high



Charge Pump Circuit Design

- $V_{D6}=V_{D4}$, $V_{D5}=V_{D3}$
  - Effect of channel length modulation is eliminated

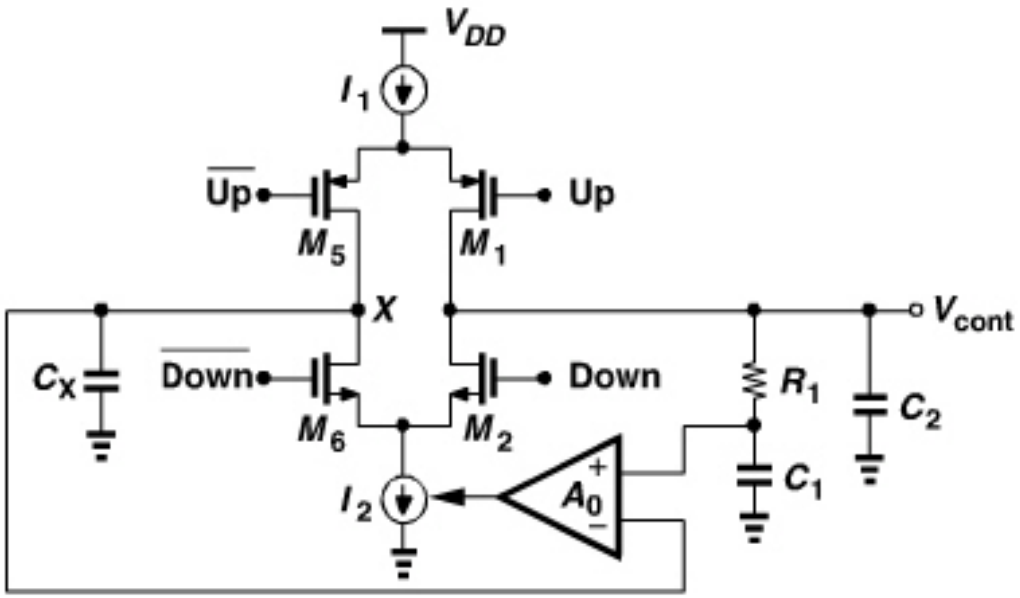




Lower Headroom required

Charge Pump Circuit Design

- In steady state $I_1=I_2$ and $V_x=V_{cont}$



Design Procedure

- How to choose f_{ref}
- If we need to generate 10MHz, 14MHz, 18MHz
  - Note that $f_{out}=N*f_{ref}$
  - F_{ref}=2MHz
  - For 10 MHz, N=5 for 14 MHz, N=7 and so on
- $f_{REF}=GCD(f_{Carrier},f_{Spacing})$

Design Procedure

$$T_{ol}(s) = \omega_n^2 \frac{(1+s/\omega_z)}{s^2(1+s/\omega_p)} \approx \frac{\left(2\zeta\omega_n s + \omega_n^2\right)}{s^2} \qquad T_{cl}(s) \approx N \frac{\left(\omega_n^2 + s(\omega_n^2/\omega_z)\right)}{s^2 + s(\omega_n^2/\omega_z) + \omega_n^2}, \quad (\omega_p >>)$$

$$\zeta = \frac{\omega_n}{2\omega_z} = \frac{\omega_c}{2\omega_n} \qquad \omega_c = \frac{\omega_n^2}{\omega_z}$$

- 3 Unknowns (ω_n, ω_z, ω_p) note that ζ is a function of ω_n, ω_z
- 3 Equations $\zeta=1$, $\omega_n^2 = \omega_z\omega_p$, $\omega_c < \omega_{REF}/10$

1. Determine the loop bandwidth
   $\omega_c = \omega_{REF}/10$
2. Choose damping factor $\zeta=1$
3. Calculate natural frequency
   $\omega_n = \omega_c/2\zeta$
4. *Calculate* $\omega_z = \omega_n/2\zeta = \omega_c/4\zeta^2$
5. *Calculate* $\omega_p = \omega_c x 4\zeta^2$ *(Remember that* $\omega_c = \sqrt{\omega_p\omega_z}$ *)*

Design Procedure

- Now we have ω_n, ω_z, ω_p

$$\omega_n = \sqrt{K_D K_{VCO}} = \sqrt{\frac{IK_{vco}}{2\pi C_1 N}} \qquad \omega_z = \frac{1}{R_1 C_1} \qquad \omega_p \approx \frac{1}{R_1 C_2}$$

- 5 unknowns and 3 Equations (I, K_{vco}, R_1, C_1, C_2)
  - Choose any 2 variables and calculate the rest
  - Use average value of N

Example

- Design PLL that generate frequencies from 2.45GHz to 2.55 GHz with 0.5 MHz channel spacing
  - F_{ref}=0.5MHz, ω_{ref}=3.14 Mrad/s (N=4900 to 5100)
  - $\omega_{c=}\omega_{ref}/10$=0.314 Mrad/s
  - $\zeta=1$
  - $\omega_n = \omega_c/2\zeta$=0.157 Mrad/s
  - $\omega_z = \omega_n/2\zeta = \omega_c/4\zeta^2$=0.0785 Mrad/s
  - $\omega_p = \omega_c x 4\zeta^2$ =1.256 Mrad/s *(Remember that* $\omega_c = \sqrt{\omega_p \omega_z}$ *)*
  - Choose I=100μA, K_{vco}=1Grad/V

$$\omega_n = \sqrt{\frac{IK_{vco}}{2\pi C_1 N}} \Rightarrow C_1 = 129PF \quad \omega_z = \frac{1}{R_1 C_1} \Rightarrow R_1 = 100k\Omega \qquad \omega_p \approx \frac{1}{R_1 C_2} \Rightarrow C_2 = 8PF$$