ECE 621
Signaling & Synchronization
Fall 2020

Topic 5
Equalization

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ICL

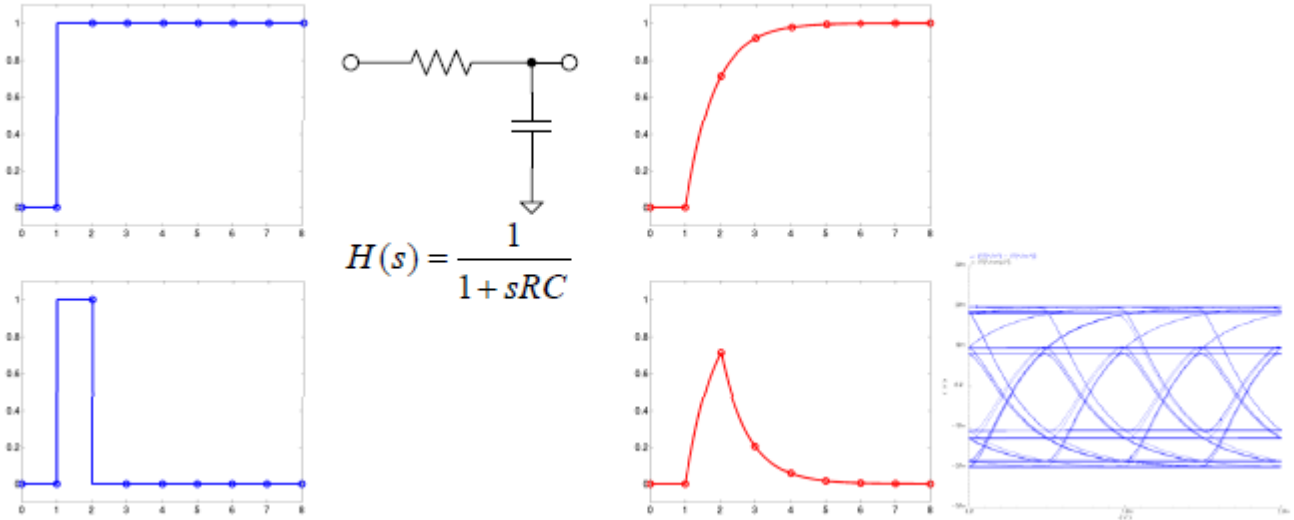
(Courtesy of K. Yang – UCLA, S. Palermo – TAMU, and E. Alon – UCB)

Outline

- **Equalization Theory and Circuits**
  - Overview
  - Classifications
- **Equalizer Implementations**
  - TX FIR
  - RX FIR
  - RX CTLE
  - RX DFE

Basic Concept (1)

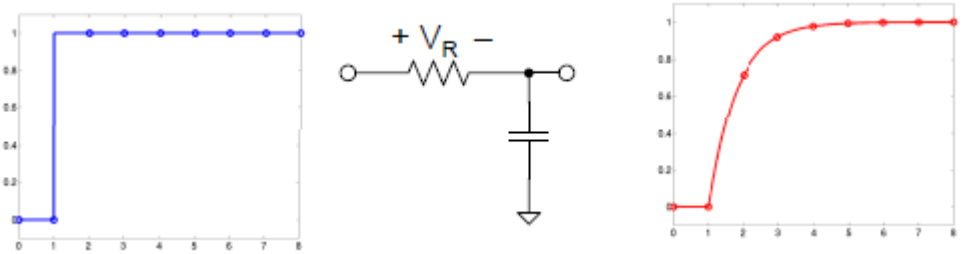
- Channel has limited bandwidth.
- A Simple model of channel: Single-pole lowpass filter



- Bandwidth limitation causes intersymbol interference (ISI)
- Can we transmit signals that exceeds the channel bandwidth?

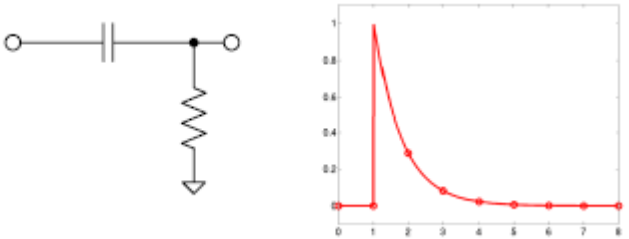
Basic Concept (2)

- **Where is the energy loss?**



- **Energy loss in R.**
- **If we add V_R back to output, we get the perfect signal.**

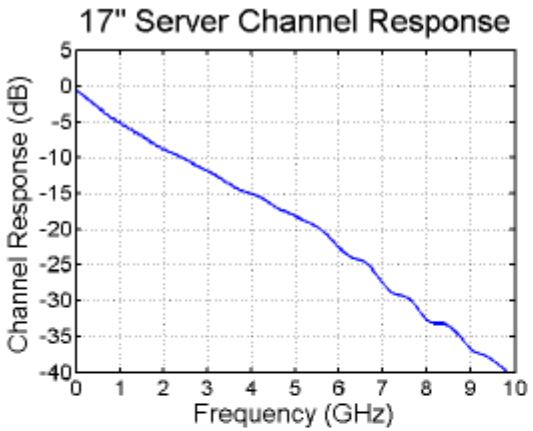
$$H(s) = \frac{sRC}{1+sRC}$$

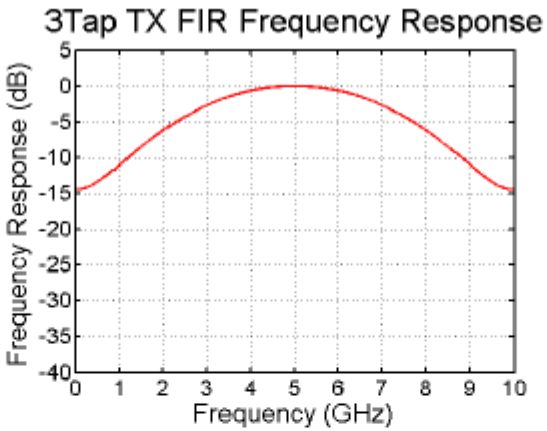


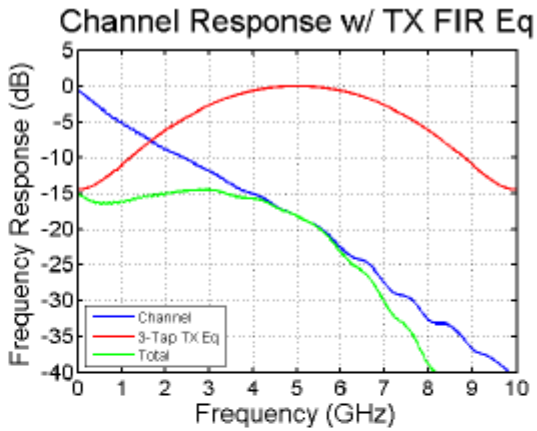
- **This circuit can help us to compensate for the lowpass filtering.**
- **What is this circuit? Highpass filter**

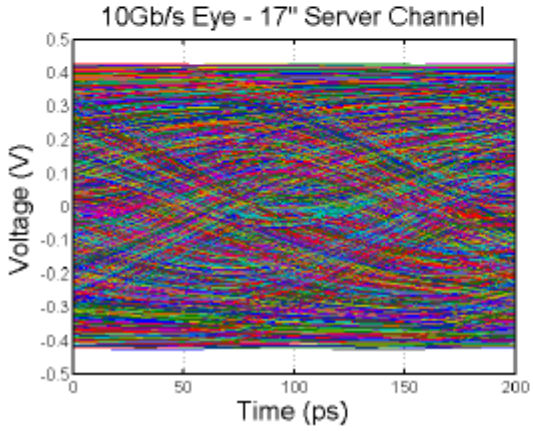
Channel Equalization

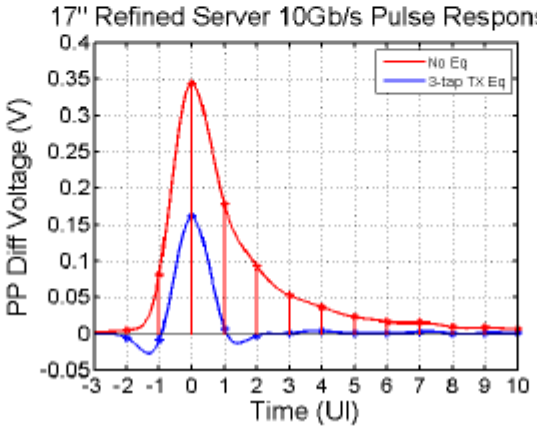
- **Equalization goal is to flatten the frequency response out to the Nyquist Frequency and remove time-domain ISI.**

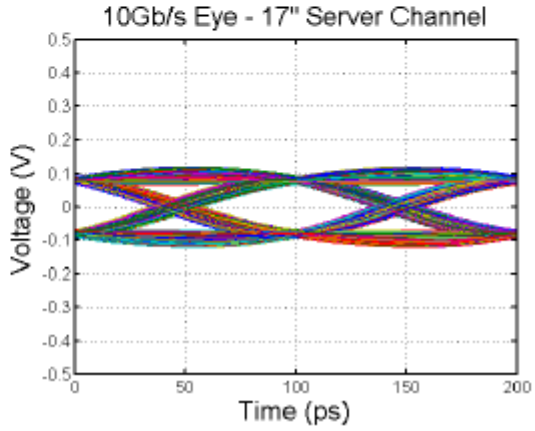










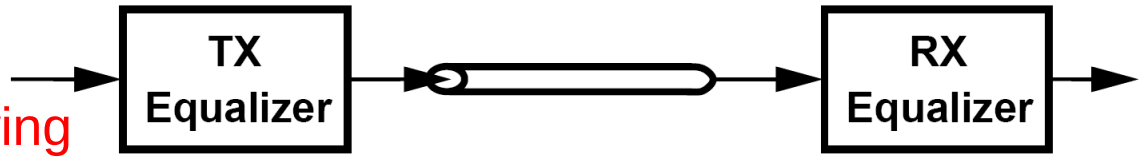


Equalizer Topologies

- **TX vs. RX Equalization**

Ease

Adaptability - Swing

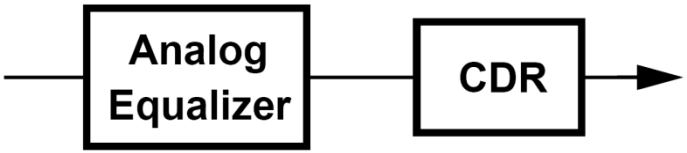


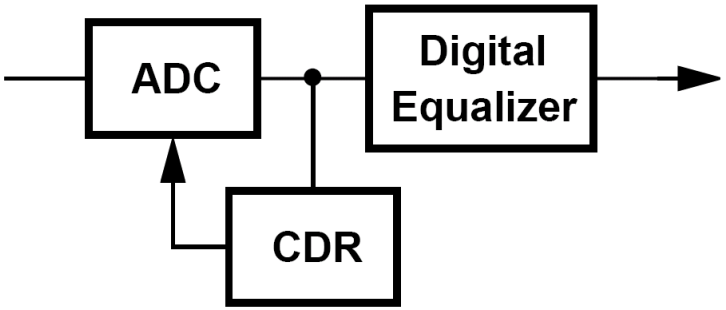
Adaptability

Noise

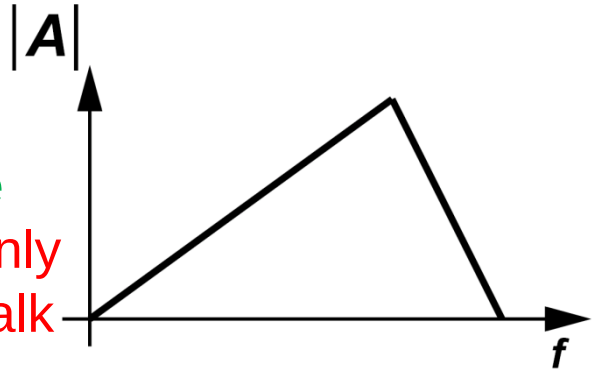
- **Digital vs. Analog**

Add/Sub V/I using GmC, RC or L





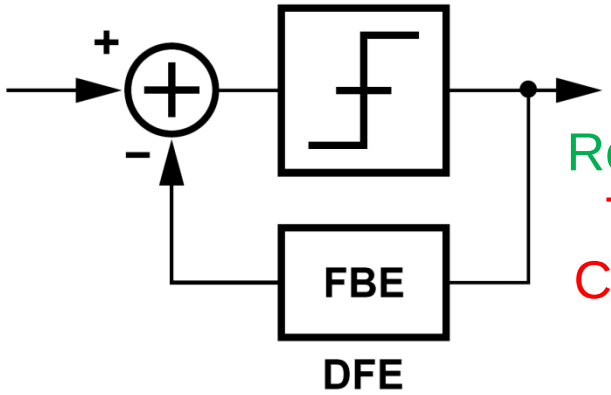
- **Linear vs. Non-Linear**



Ease

Loss Only

Crosstalk



Reflection

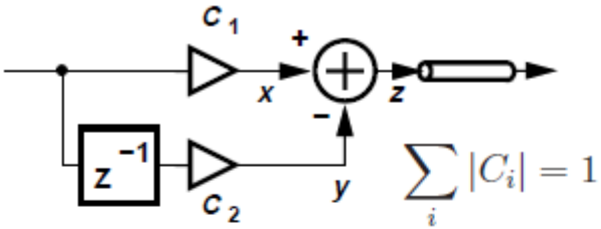
Timing

Crosstalk

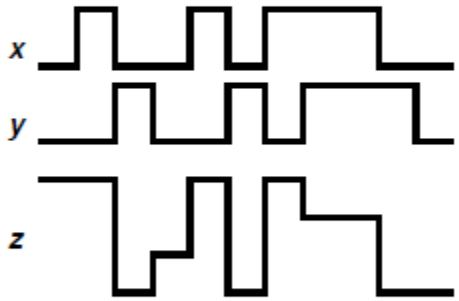
- **Continuous vs. Discrete-Time** HPF, RC or L vs. FIR, IIR or DFE

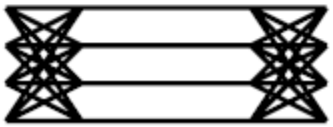
TX FIR Filter

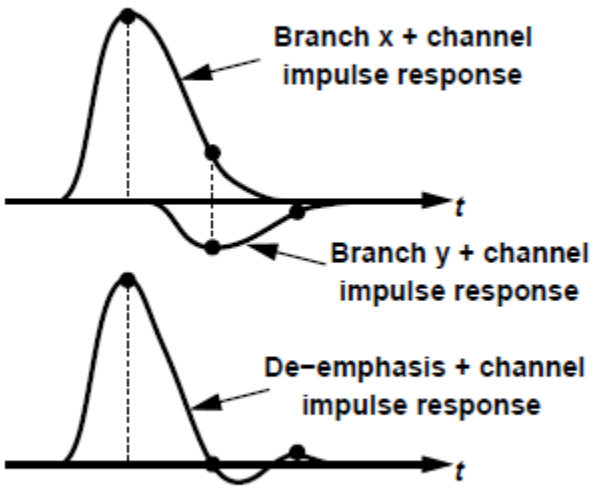
- **TX FIR filter pre-distorts transmitted pulse in order to invert channel distortion at the cost of attenuated transmit signal (de-emphasis).**



$$\sum_i |C_i| = 1$$

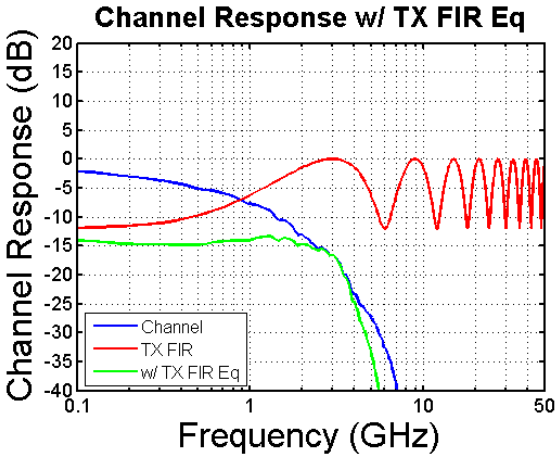


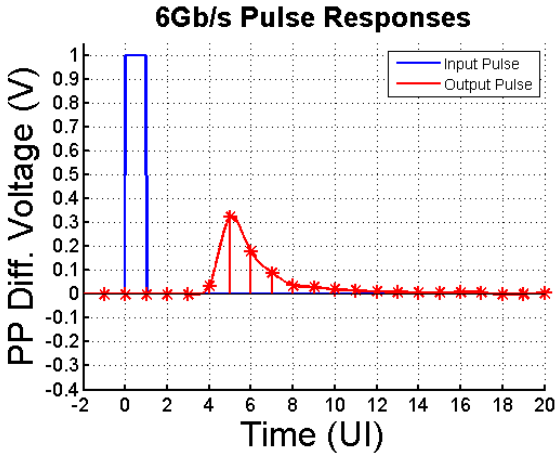


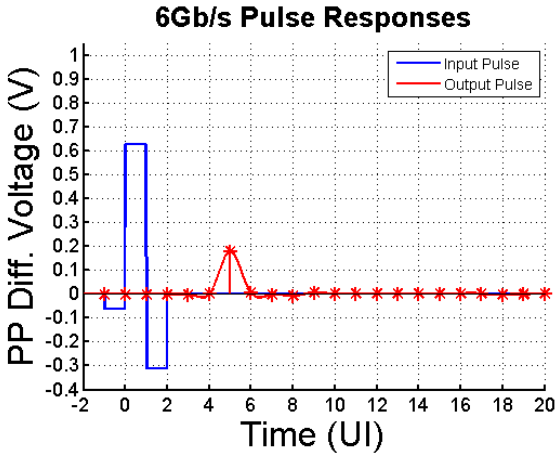


2-Tap TX FIR Example

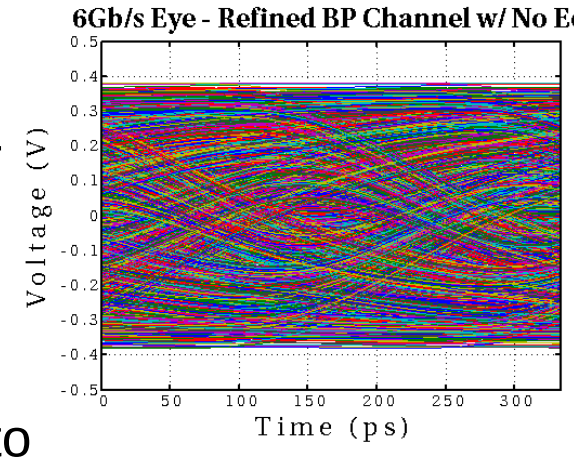
6 Gb/s TX FIR Equalization Example

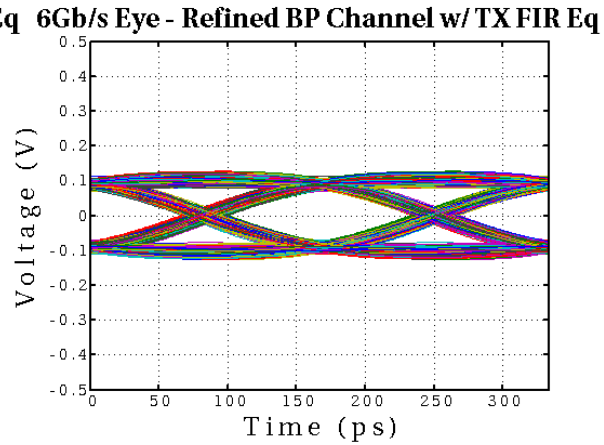






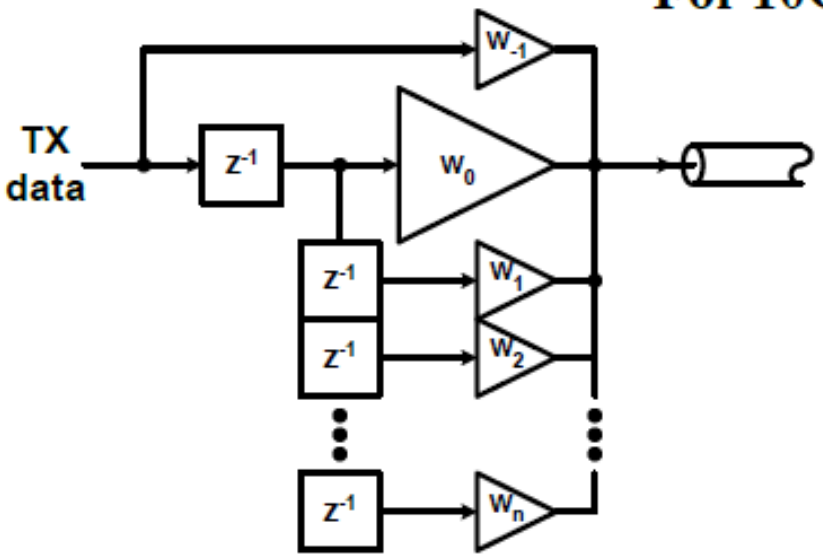
- **Pros**
  - Simple to implement
  - Can cancel ISI in pre-cursor and beyond filter span
- **Cons**
  - Attenuates low frequency content due to peak-power limitation
  - Need a “back-channel” to tune filter taps

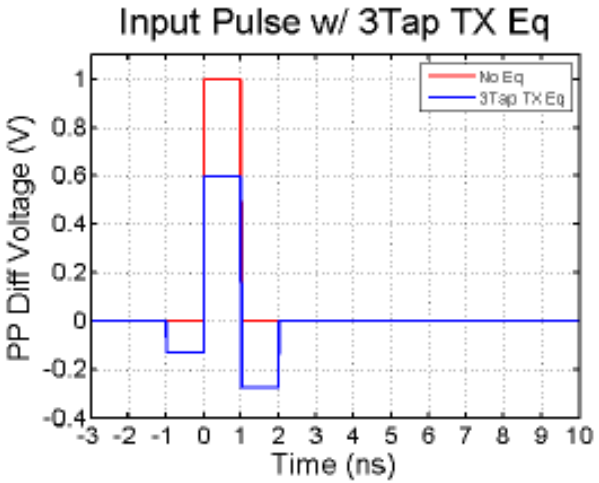




Time-Domain Representation

For 10Gbps : $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$





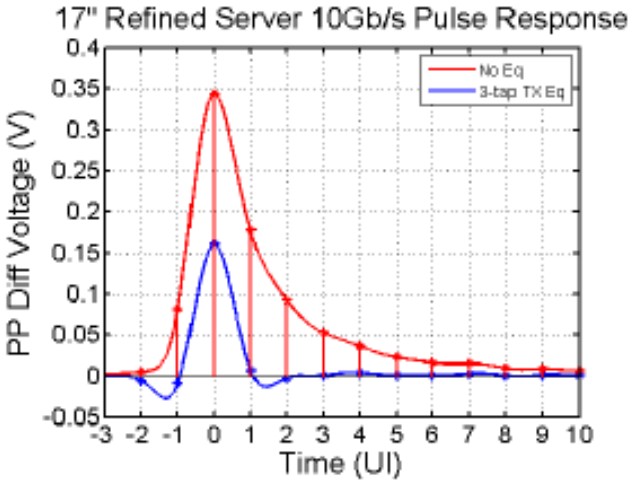
$$\mathbf{W} = [-0.131 \quad 0.595 \quad -0.274]$$

Low Frequency Response (Sum Taps)

$$[\ldots \quad 1 \quad 1 \quad 1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 0.190 \quad 0.190 \quad 0.190 \quad \ldots]$$

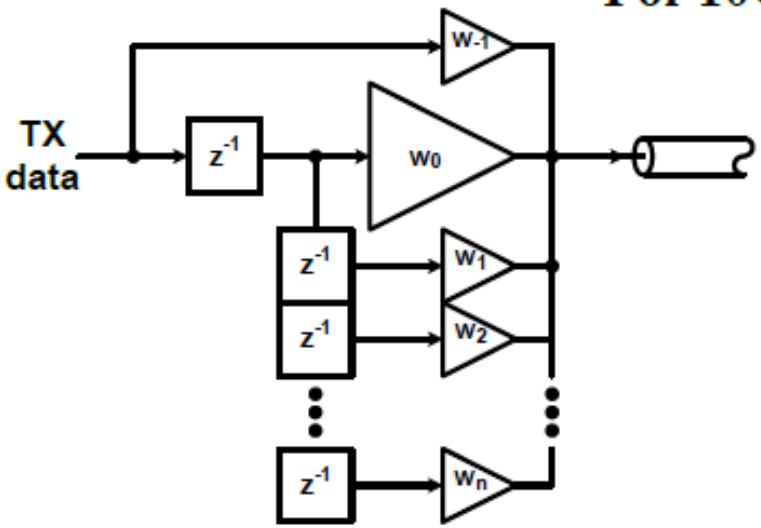
Nyquist Frequency Response (Sum Taps w/ Alternating Polarity)

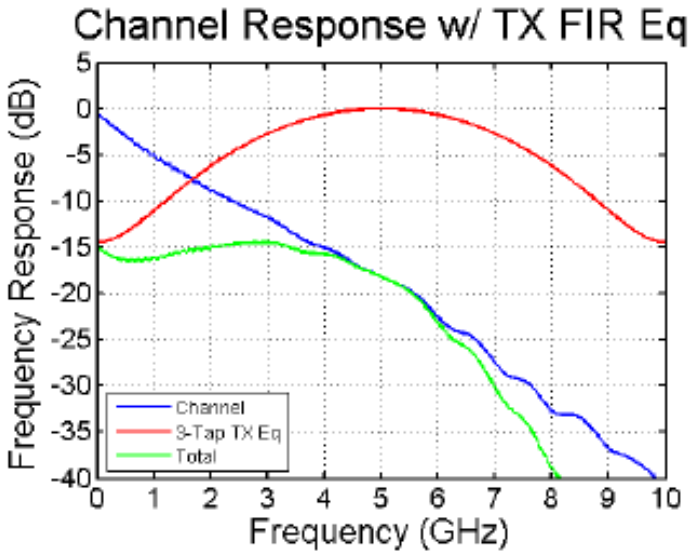
$$[\ldots \quad -1 \quad 1 \quad -1 \quad \ldots] * [-0.131 \quad 0.595 \quad -0.274] = [\ldots \quad 1 \quad -1 \quad 1 \quad \ldots]$$



Frequency-Domain Representation

For 10Gbps : $W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$





$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\text{w/ } z = e^{j2\pi fT_s} = \cos(2\pi fT_s) + j\sin(2\pi fT_s)$$

Low Frequency Response $(f = 0)$

$$z = \cos(0) + j\sin(0) = 1 \Rightarrow W(f=0) = 0.190 \Rightarrow -14.4dB$$

Nyquist Frequency Response $\left(f = \frac{1}{2T_s}\right)$

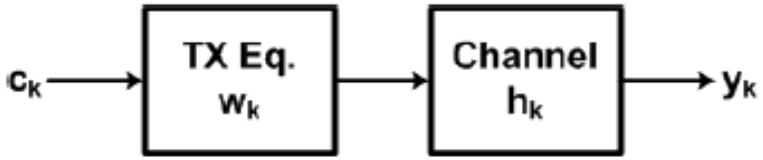
$$z = \cos(\pi) + j\sin(\pi) = -1 \Rightarrow W\left(f = \frac{1}{2T_s}\right) = -1 \Rightarrow 0dB$$

Note: Ts=Tb=100ps

- **Equalizer has 14.4dB of frequency peaking**
  - Attenuates DC at -14.4dB and passes Nyquist frequency at 0dB

TX FIR Coefficient Selection (1)

- **One approach to set the TX FIR coefficients is a Minimum Mean-Square Error (MMSE) Algorithm**



channel output vector, y
Rows = k+n+ℓ-2
where k = channel pulse model length

TX Eq "w" Matrix
Rows = n+ℓ-1 where n = tap number
Columns = ℓ = input symbol number

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \dots & 0 & 0 \\ w(1) & w(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \dots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \dots \\ c(l-1) \end{bmatrix}$$

Channel "h" Matrix
Rows = k+n+ℓ-2
Columns = n+ℓ-1

ℓ input symbols, c

TX FIR Coefficient Selection (2)

- **Total system**

$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} w(0) & 0 & 0 & \dots & 0 & 0 \\ w(1) & w(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & w(n-1) & w(n-2) \\ 0 & 0 & 0 & \dots & 0 & w(n-1) \end{bmatrix} \begin{bmatrix} c(0) \\ c(1) \\ \dots \\ c(l-1) \end{bmatrix}$$

- **Multiplying input symbols by TX Eq., wc=w*c**

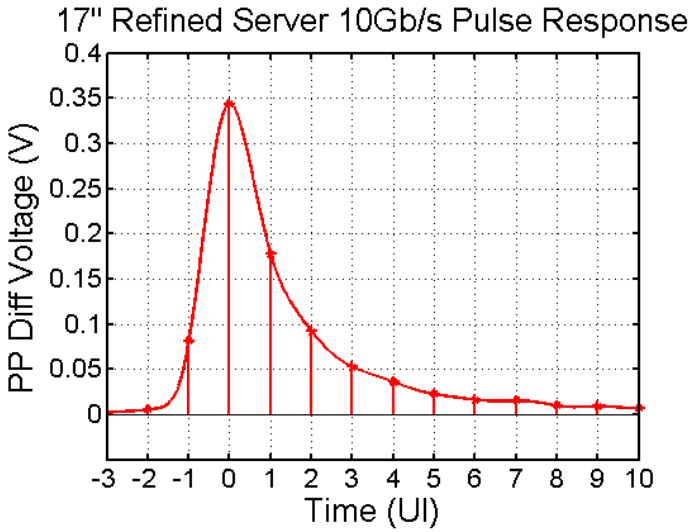
$$\begin{bmatrix} y(0) \\ y(1) \\ \dots \\ y(l+n+k-3) \end{bmatrix} = \begin{bmatrix} h(0) & 0 & 0 & \dots & 0 & 0 \\ h(1) & h(0) & 0 & \dots & 0 & 0 \\ \dots & \dots & \dots & \dots & \dots & \dots \\ 0 & 0 & 0 & \dots & h(k-1) & h(k-2) \\ 0 & 0 & 0 & \dots & 0 & h(k-1) \end{bmatrix} \begin{bmatrix} wc(0) \\ wc(1) \\ \dots \\ wc(n+l-1) \end{bmatrix}$$

- **We desire the output vector, y, to be ISI free**

$$y_{des} = \begin{cases} y_{des}(n) = 1, n = \text{Channel pre - cursor sample \#} + \text{Eq precursor tap \#} + 1 \\ y_{des}(n) = 0, n \neq \text{Channel pre - cursor sample \#} + \text{Eq precursor tap \#} + 1 \end{cases}$$

Lone-Pulse Equalization Example

- **With lone-pulse equalization, l=1 input symbols, i.e. c=[1]**



Channel pulse matrix H with 5 pre-cursor samples and 10 post-cursor samples, 3 columns for 3 eq taps

Y_{des}

Channel pre-cursor samples

$Y_{des}(5+1+1=7)=1$

Equalization pre-cursor taps

$$\begin{bmatrix}0\\0\\0\\0\\0\\1\\0\\0\\0\\0\\0\\0\\0\\0\\0\\0\end{bmatrix} = \begin{bmatrix}0.0004 & 0 & 0\\ 0.0010 & 0.0004 & 0\\ 0.0023 & 0.0010 & 0.0004\\ 0.0052 & 0.0023 & 0.0010\\ 0.0812 & 0.0052 & 0.0023\\ 0.3437 & 0.0812 & 0.0052\\ 0.1775 & 0.3437 & 0.0812\\ 0.0917 & 0.1775 & 0.3437\\ 0.0526 & 0.0917 & 0.1775\\ 0.0360 & 0.0526 & 0.0917\\ 0.0224 & 0.0360 & 0.0526\\ 0.0162 & 0.0224 & 0.0360\\ 0.0152 & 0.0162 & 0.0224\\ 0.0097 & 0.0152 & 0.0162\\ 0.0090 & 0.0097 & 0.0152\\ 0.0067 & 0.0090 & 0.0097\\ 0 & 0.0067 & 0.0090\\ 0 & 0 & 0.0067\end{bmatrix} \begin{bmatrix}w(0)\\w(1)\\w(2)\end{bmatrix} [1]$$

3-tap Eq Matrix, W

Symbol Matrix, C for "Lone Pulse"

TX FIR Coefficient Selection (3)

- **We can calculate the error w.r.t. a desired output**

$$E = Y - Y_{des} = HW_C - Y_{des} = HW - Y_{des} \text{ with pulse input}$$

- **Computing the error matrix norm²**

$$\|E\|^2 = W^T H^T HW - 2Y_{des}^T HW + Y_{des}^T Y_{des}$$

- **Differentiating this w.r.t. tap matrix taps to find taps which yield minimum error norm²**

$$\frac{d}{dW}\|E\|^2 = 2W^T H^T H - 2Y_{des}^T H = 0$$

$$W^T H^T H = Y_{des}^T H$$

- **Solving for optimum TX Eq taps, W**

$$W_{ls} = \left(H^T H\right)^{-1} H^T Y_{des}$$

- **This will yield a W matrix to produce a value of "1" at the output cursor, i.e. an FIR filter with gain**
  - Need to normalize by the total abs(tap) sum for TX FIR realization

$$W_{lsnorm}(n) = \frac{W_{ls}(n)}{\sum_{i=1}^{n} |W_{ls}(n)|}$$

TX FIR Tap Resolution

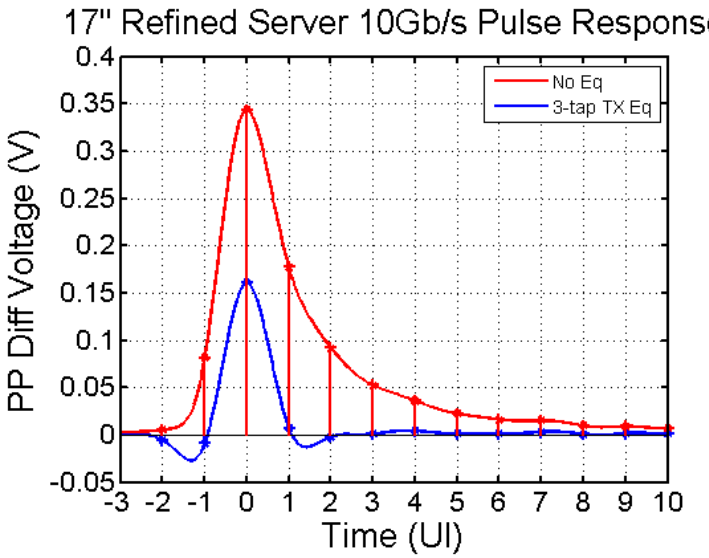
- **Using the above MMSE algorithm for the Refined Server Channel at 10Gb/s**

$$W_{ls} = \begin{bmatrix} -0.8180 \\ 3.7245 \\ -1.7184 \end{bmatrix} \xrightarrow{\text{normalizing by 6.2609}} \Rightarrow \quad W_{lsnorm} = \begin{bmatrix} -0.1307 \\ 0.5949 \\ -0.2745 \end{bmatrix}$$

$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2}$$

$$\begin{bmatrix} 1pre & main & 1post \end{bmatrix}$$

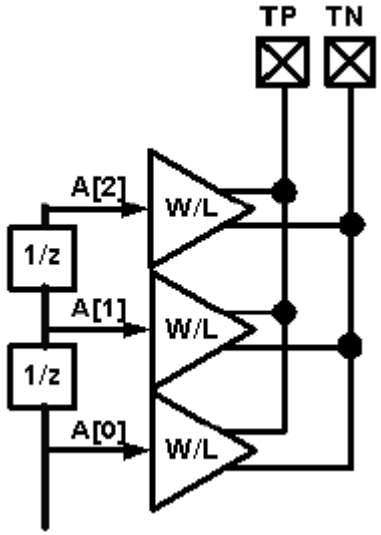
$$\begin{bmatrix} -0.131 & 0.595 & -0.274 \end{bmatrix}$$



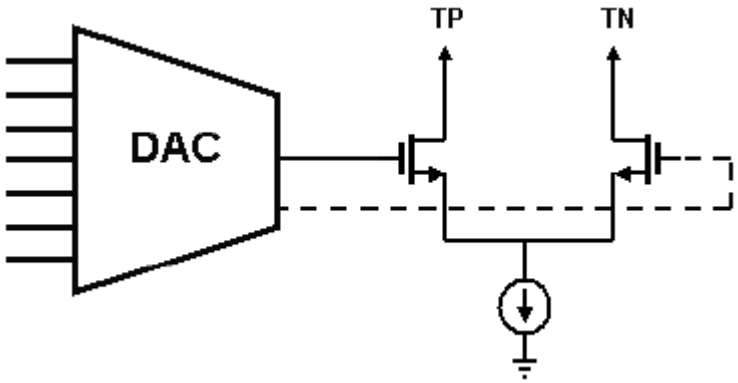
- **Generally, TX DAC resolution is limited to between 4 to 6 bits.**
- **Mapping these equalization coefficients with this resolution may impact performance.**

TX FIR Circuit Architectures

- **Direct FIR**
  - Parallel output drivers for output taps
  - Each parallel driver must be sized to handle its potential maximum current
  - Lower power & complexity
  - Higher output capacitance

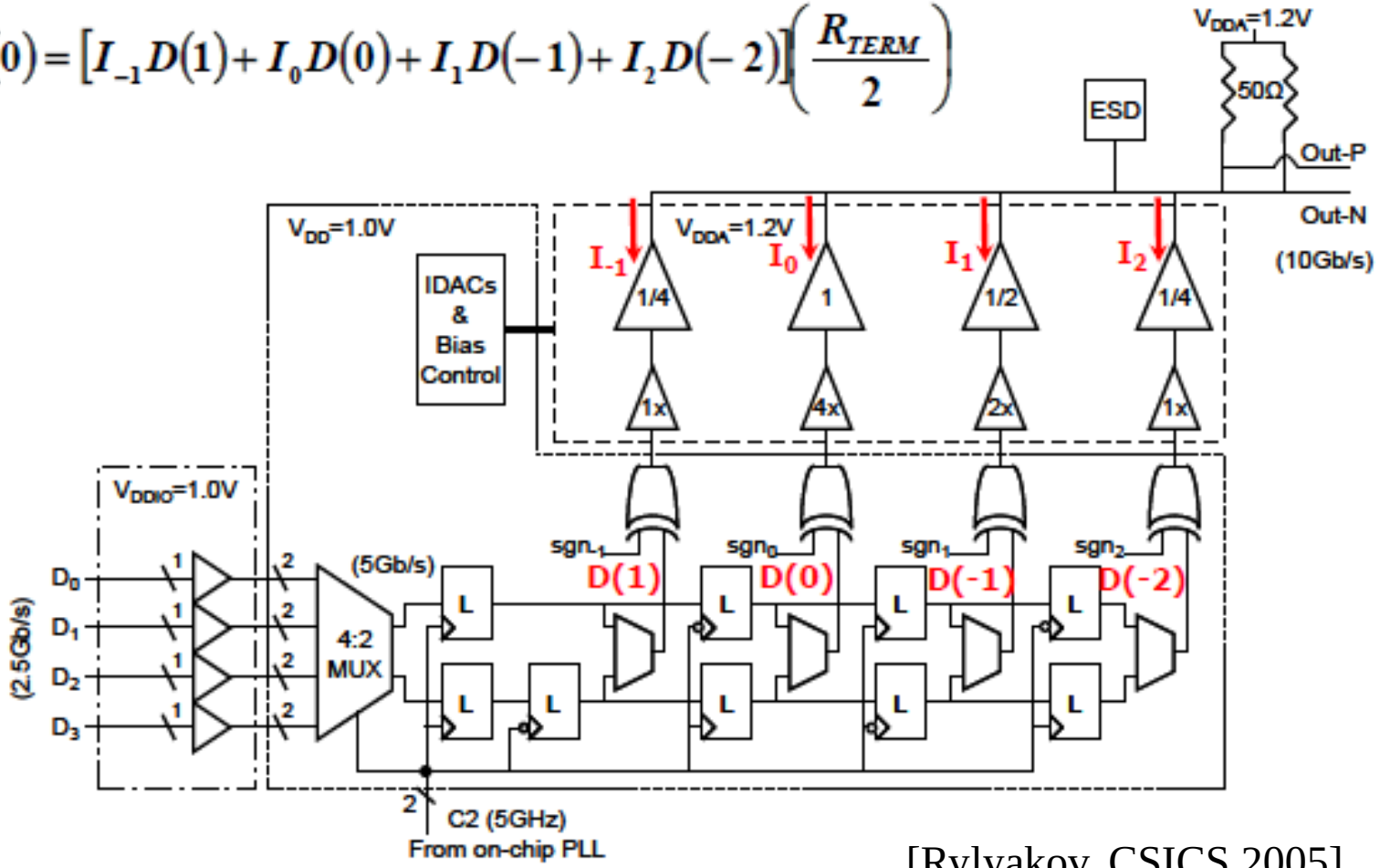


- **Segmented DAC**
  - Minimum sized output transistors to handle peak output current
  - Lowest output capacitance
  - Most power & complexity
  - Need mapping table (RAM)
  - Very flexible in equalization



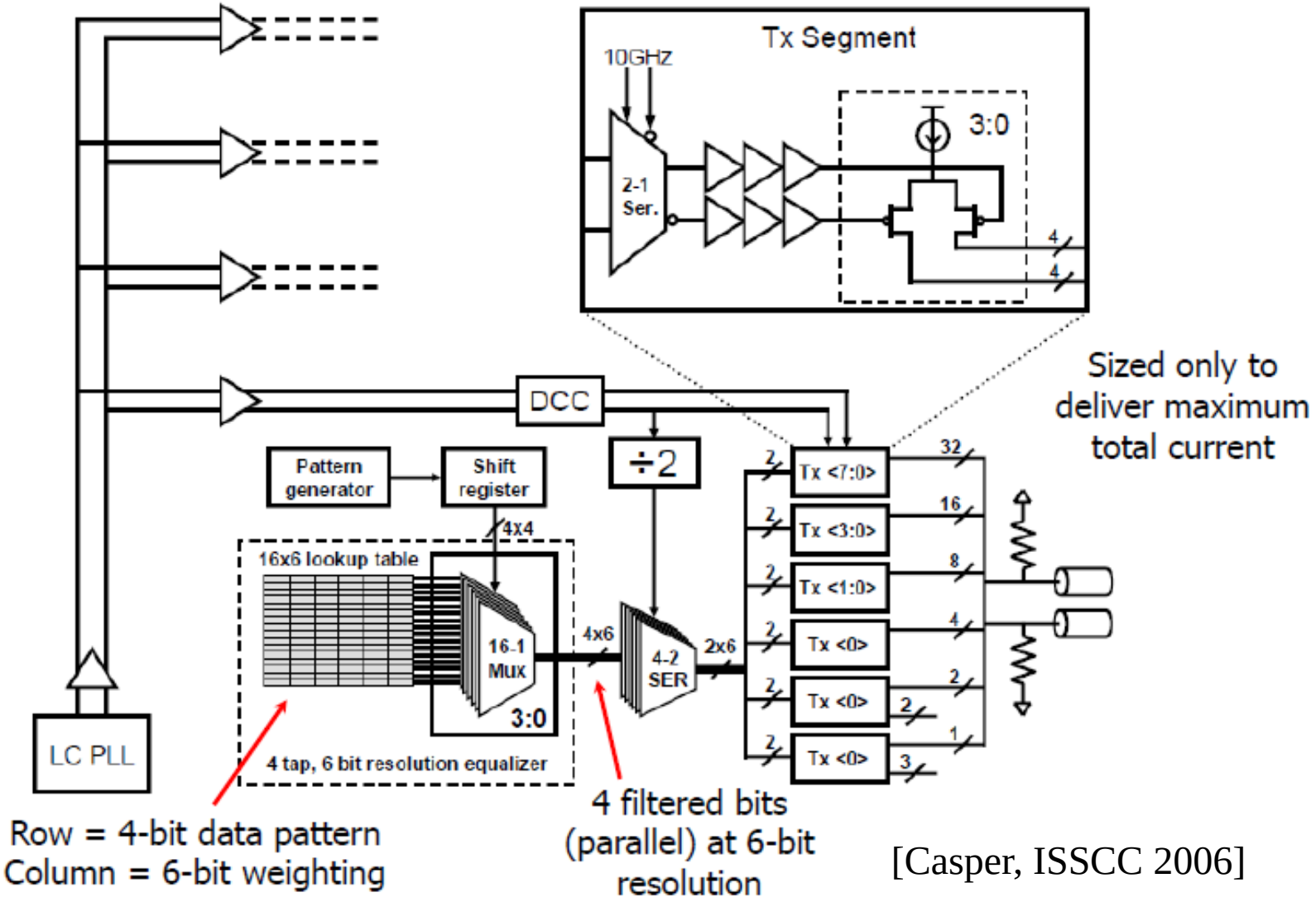
Direct FIR Example

$$V_{out}(0) = \left[I_{-1}D(1) + I_0 D(0) + I_1 D(-1) + I_2 D(-2)\right]\left(\frac{R_{TERM}}{2}\right)$$



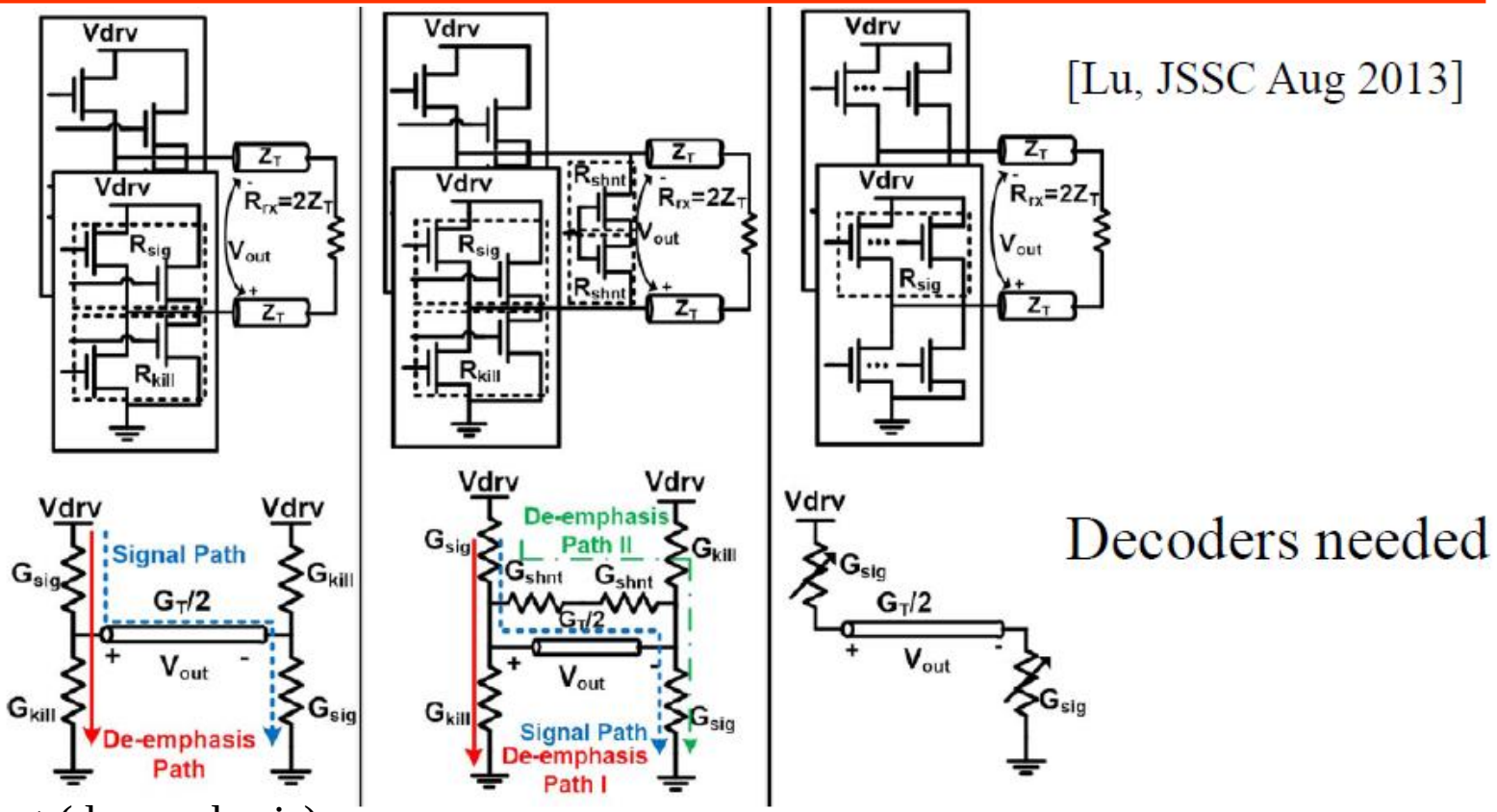
[Rylyakov, CSICS 2005]

Segmented DAC Example



[Casper, ISSCC 2006]

Pre-Emphasis in VM Drivers



- Reduce output (de-emphasis) by a path to ground in combination with the main signal path.
- Amplitude changes without impedance.
- Power loss is high.

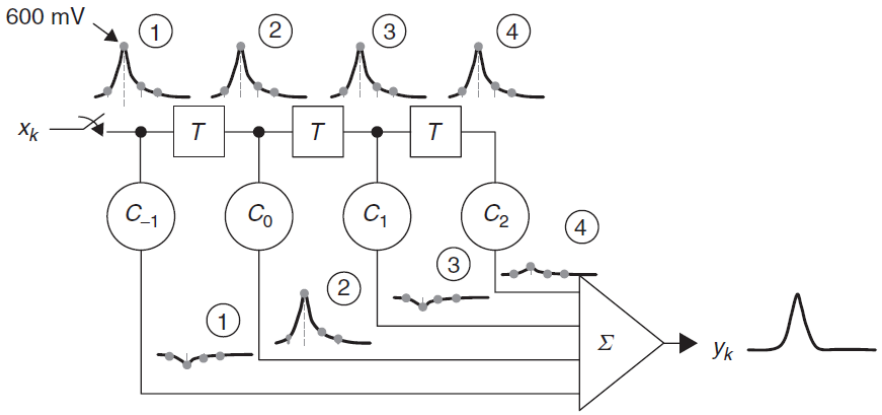
- Shunt impedance in parallel with channel
- G_{kill} can be removed completely.
- Termination is not affected.
- Power is reduced with swing.

- Power is minimum when amplitude reduces.
- But termination is corrupted.

Outline

- Equalization Theory and Circuits
  - Overview
  - Classifications
- Equalizer Implementations
  - TX FIR
  - RX FIR
  - RX CTLE
  - RX DFE

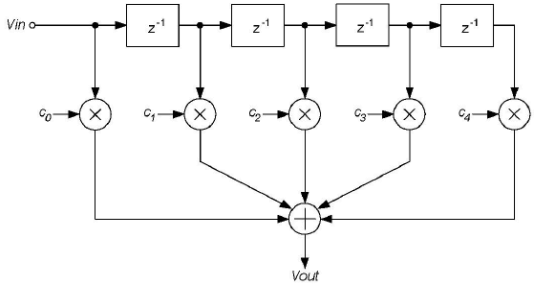
RX FIR Equalization

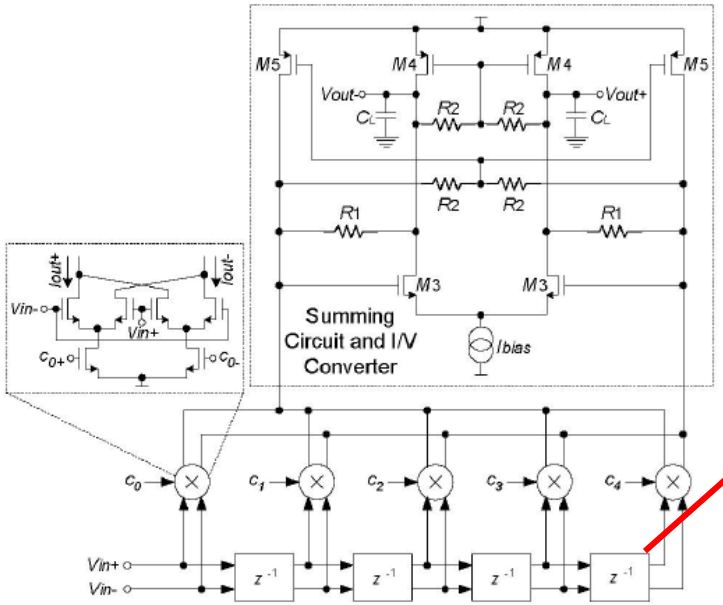


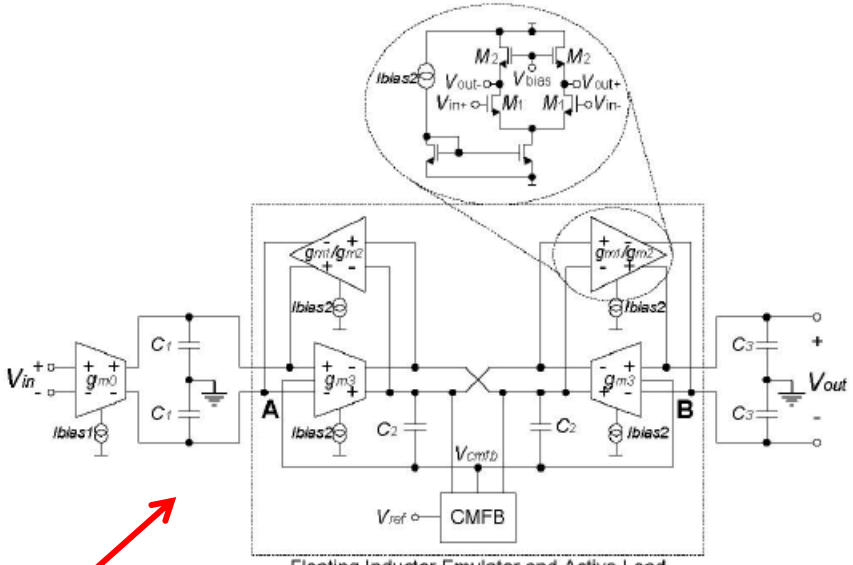
- **Delay analog input signal and multiply by equalization coefficients.**
- **Pros**
  - With sufficient dynamic range, can amplify high frequency content (rather than attenuate low frequencies).
  - Can cancel ISI in pre-cursor and beyond filter span.
  - Filter tap coefficients can be adaptively tuned without any back-channel.
- **Cons**
  - Amplifies noise/crosstalk.
  - Implementation of analog delays
  - Tap precision

Analog RX FIR Equalization Example

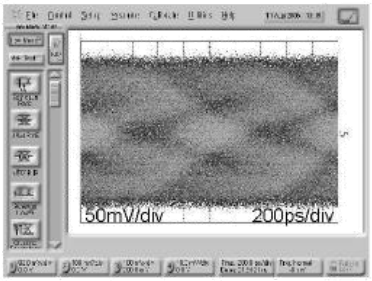
- **5-tap equalizer with tap spacing of $T_b/2$**



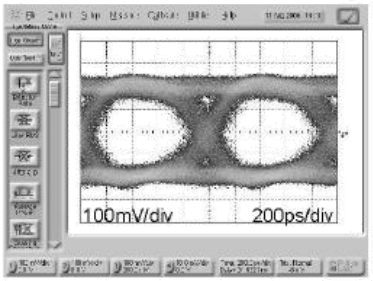




Floating Inductor Emulator and Active Load



Before Equalizer: 23meters

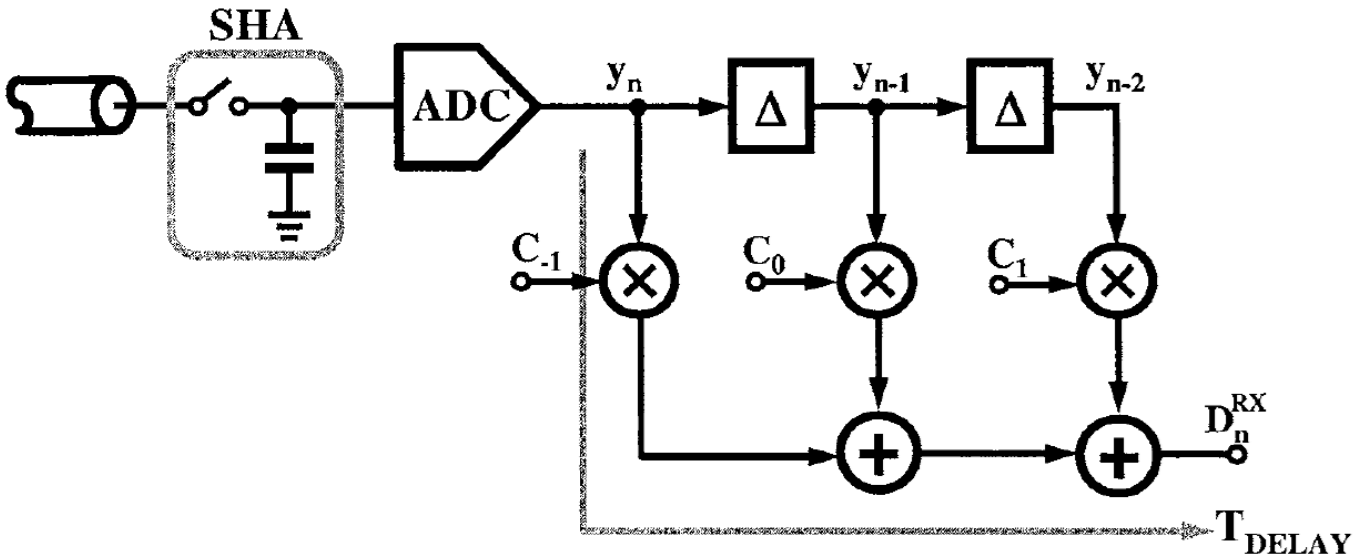


After Equalizer: 23meters

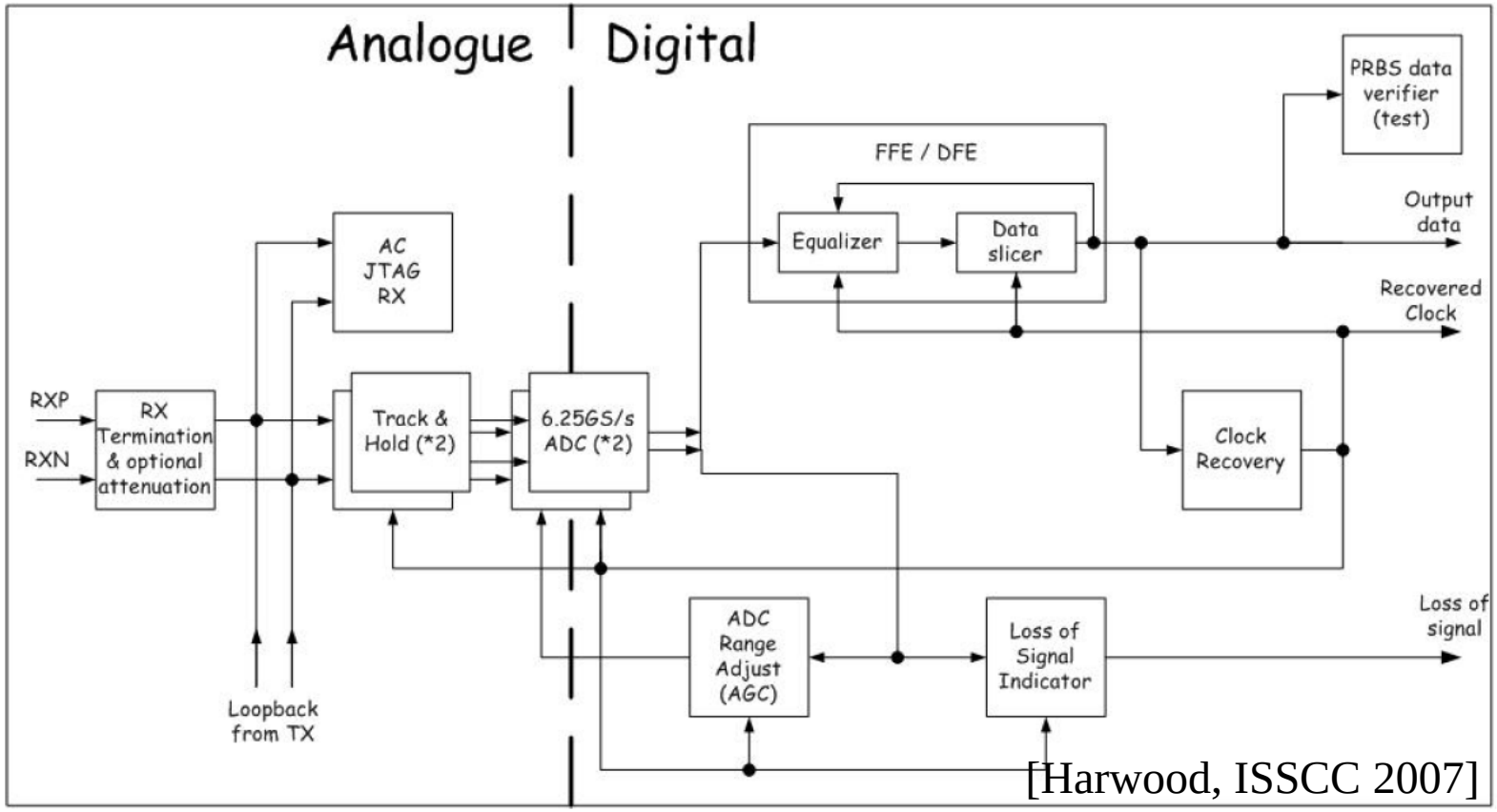
[Hernandez-Garduno, ISSCC 2007]

Digital RX FIR Equalization

- **Digitize the input signal with high-speed low/medium resolution ADC and perform equalization in digital domain**
  - Digital delays, multipliers, adders
  - Limited to ADC resolution
- **Power can be high due to very fast ADC**



Digital RX FIR Equalization Example

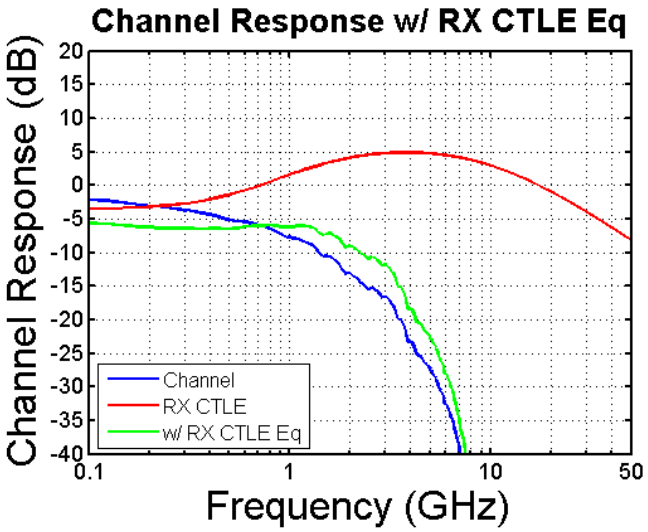


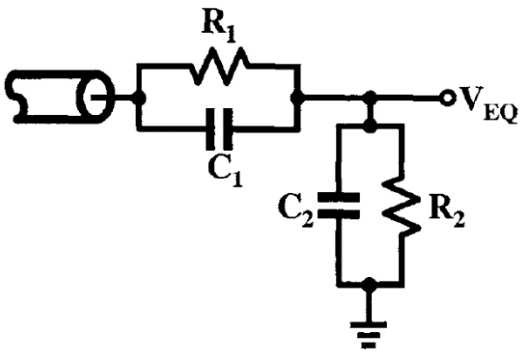
[Harwood, ISSCC 2007]

- **12.5GS/s 4.5-bit Flash ADC in 65nm CMOS**
- **2-tap FFE & 5-tap DFE**
- **XCVR power (inc. TX) = 330mW, Analog = 245mW, Digital = 85mW**

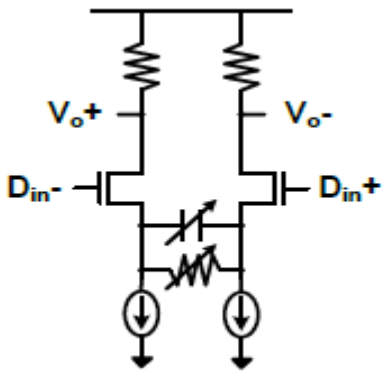
Continuous-Time Linear Equalizer (CTLE)

- **Passive R-C (or L) can implement high-pass transfer function to compensate for channel loss.**
- **Cancel both precursor and long-tail ISI.**
- **Can be purely passive or combined with an amplifier to provide gain.**





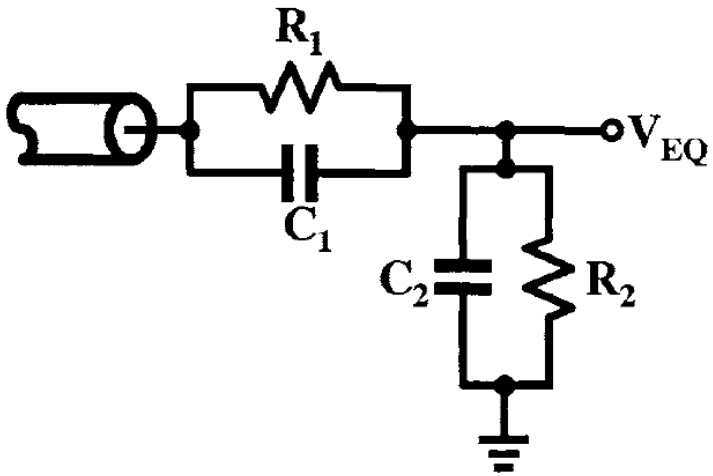
Passive CTLE



Active CTLE

Passive CTLE

- **Passive structures offer excellent linearity, but no gain at Nyquist frequency.**



$$H(s)=\frac{R_2}{R_1+R_2}\frac{1+R_1C_1s}{1+\frac{R_1R_2}{R_1+R_2}(C_1+C_2)s}$$

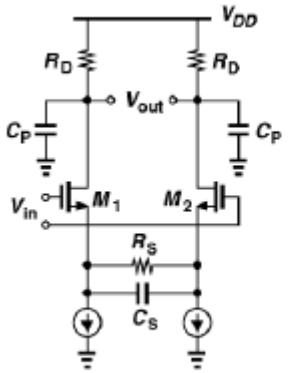
$$\omega_z=\frac{1}{R_1C_1},\qquad \omega_p=\frac{1}{\frac{R_1R_2}{R_1+R_2}(C_1+C_2)}$$

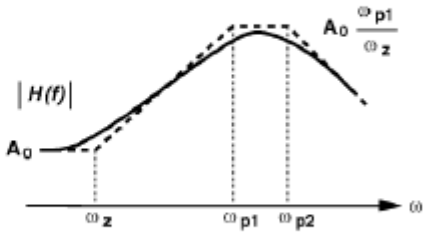
$$\text{DC gain}=\frac{R_2}{R_1+R_2},\quad \text{HF gain}=\frac{C_1}{C_1+C_2}$$

$$\text{Peaking}=\frac{\text{HF gain}}{\text{DC gain}}=\frac{\omega_p}{\omega_z}=\frac{R_1+R_2}{R_2}\frac{C_1}{C_1+C_2}$$

Active CTLE

- Input amplifier with RC degeneration can provide frequency peaking with gain at Nyquist frequency.
- Potentially limited by gain-bandwidth of amplifier.
- Amplifier must be designed for input linear range.
- Often TX eq. provides some low frequency attenuation.
- Sensitive to PVT variations and can be hard to tune.
- Generally limited to 1st-order compensation.





$$H(s) = \frac{g_m}{C_p} \frac{s + \frac{1}{R_S C_S}}{\left(s + \frac{1 + g_m R_S/2}{R_S C_S}\right)\left(s + \frac{1}{R_D C_p}\right)}$$

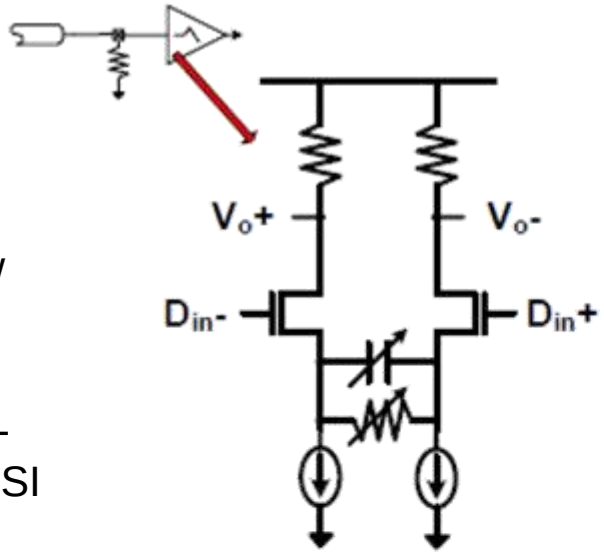
$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S}, \quad \omega_{p2} = \frac{1}{R_D C_p}$$

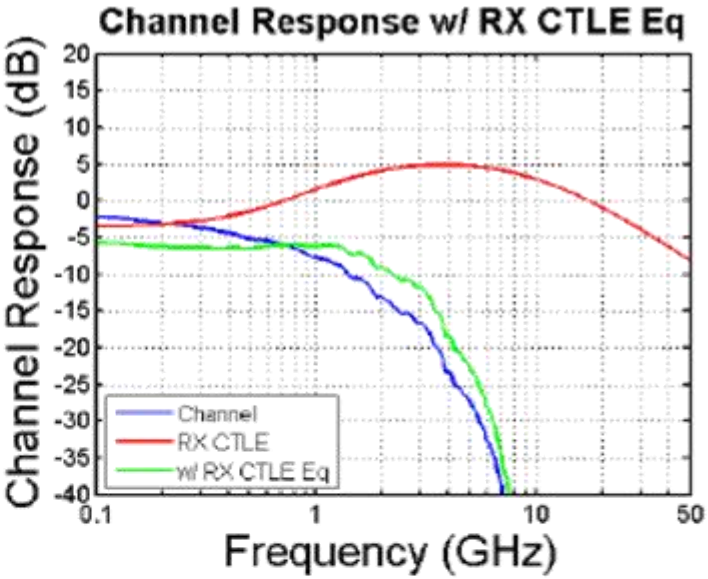
$$\text{DC gain} = \frac{g_m R_D}{1 + g_m R_S/2}, \quad \text{Ideal peak gain} = g_m R_D$$

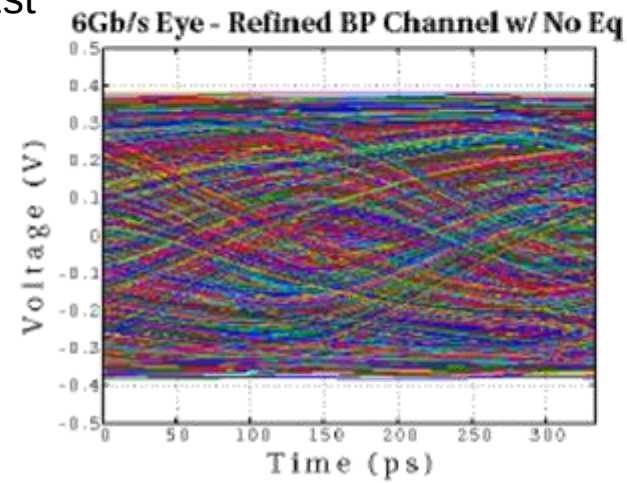
$$\text{Ideal Peaking} = \frac{\text{Ideal peak gain}}{\text{DC gain}} = \frac{\omega_{p1}}{\omega_z} = 1 + g_m R_S/2$$

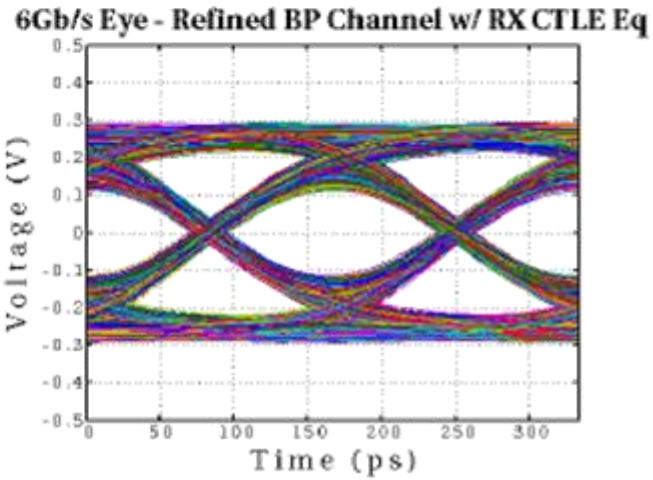
Active CTLE Example

- **Pros**
  - Provides gain and equalization with low power and area overhead
  - Can cancel both pre-cursor and long-tail ISI
- **Cons**
  - Generally limited to 1st order compensation
  - Amplifies noise/crosstalk
  - PVT sensitivity
  - Can be hard to tune



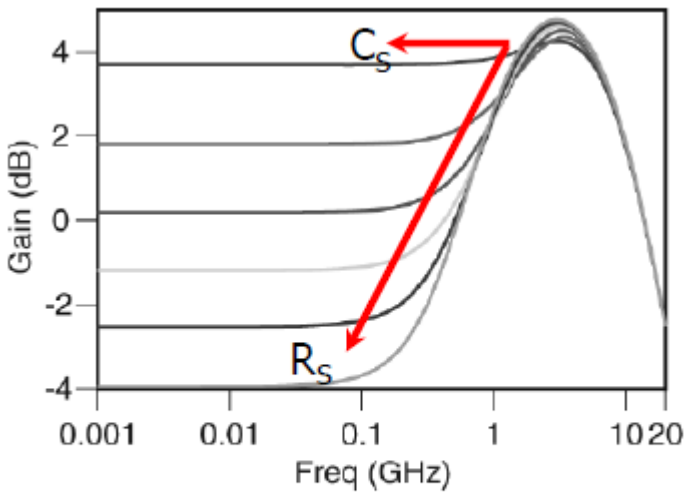






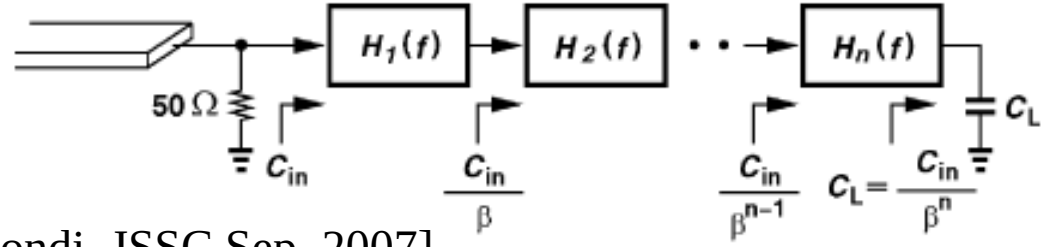
Active CTLE Tuning

- **Tune degeneration resistor and capacitor to adjust zero frequency and 1st pole which sets peaking and DC gain.**
- **Increasing C_S moves zero and 1st pole to a lower frequency w/o impacting (ideal) peaking.**
- **Increasing R_S moves zero to lower frequency and increases peaking (lowers DC gain)**
  - Minimal impact on 1st pole

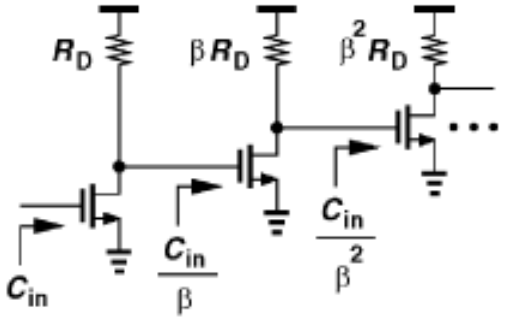


$$\omega_z = \frac{1}{R_S C_S}, \quad \omega_{p1} = \frac{1 + g_m R_S/2}{R_S C_S}$$

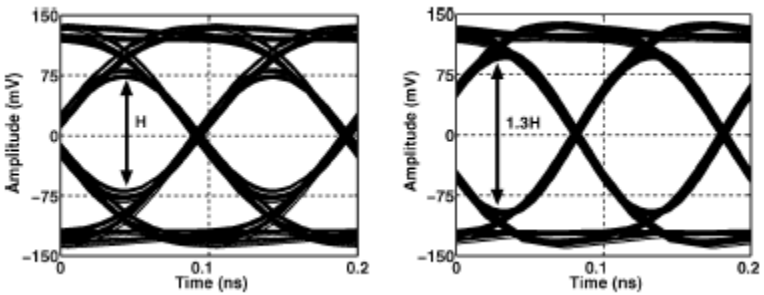
Active CTLE Cascading



[Gondi, JSSC Sep. 2007]

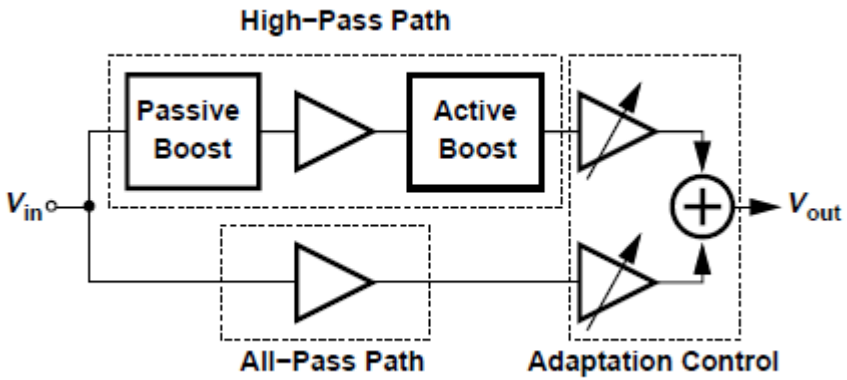


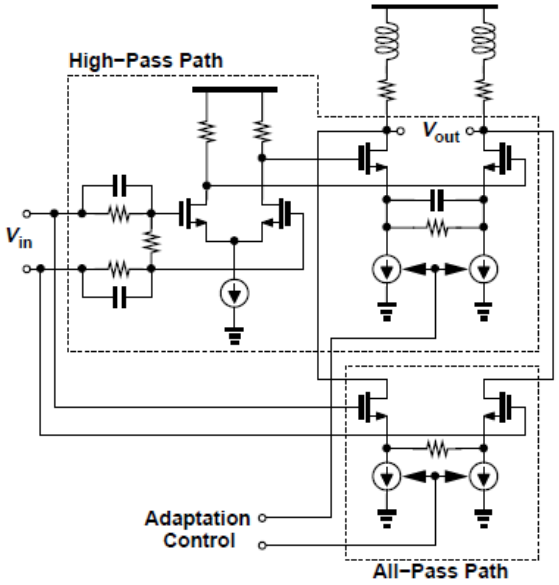
- **Multiple stages are required for higher peaking with reasonable DC gain.**
- **Some gain stages can be used.**
- **Reverse scaling provides bandwidth improvement in applications where the input impedance need not be very high.**



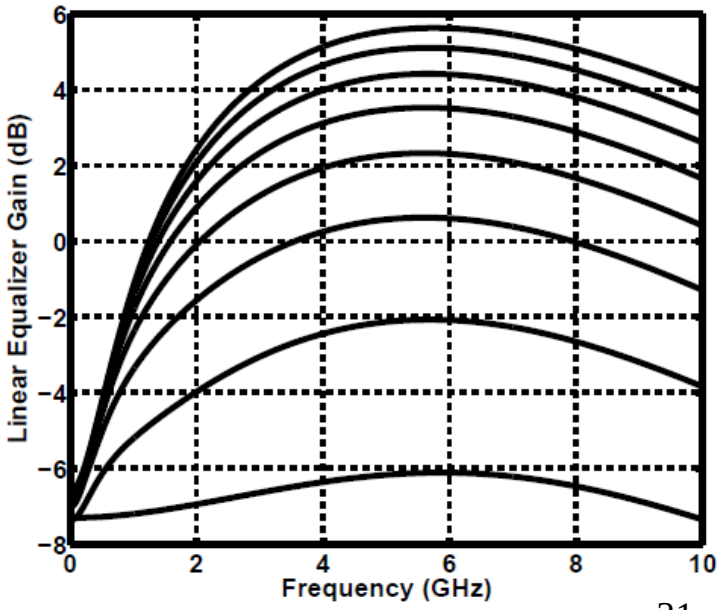
Not Scaled Scaled

Dual-Path CTLE





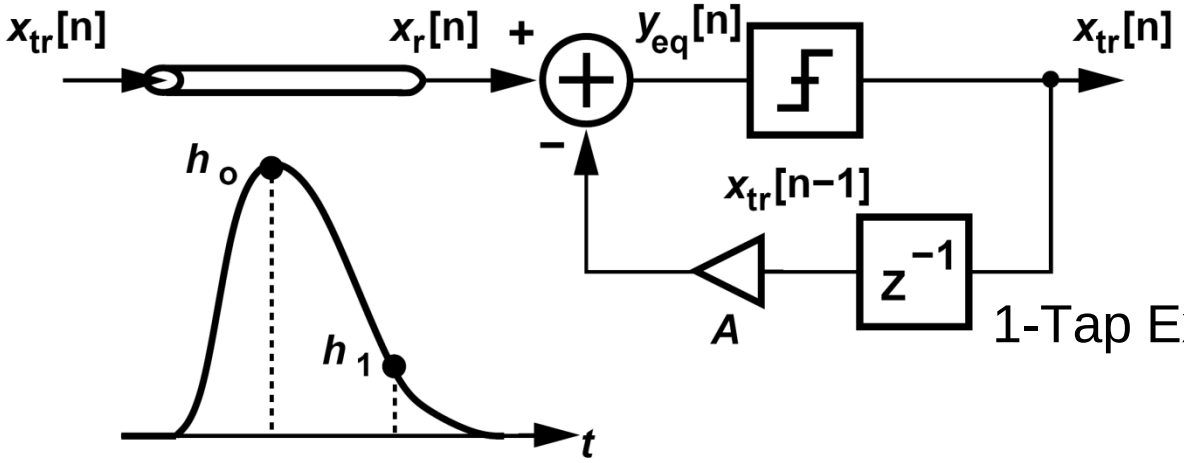
- **Adding a high-pass filter to an all-pass filter results in peaking.**
- **Phase matching between the two paths is required, especially for cascaded stages.**
- **Tuning is done by varying the relative gains.**



Outline

- Equalization Theory and Circuits
  - Overview
  - Classifications
- Equalizer Implementations
  - TX FIR
  - RX FIR
  - RX CTLE
  - RX DFE

Decision Feedback Equalizer (DFE)



1-Tap Example

$$x_r[n] = h_o x_{tr}[n] + h_1 x_{tr}[n-1]$$

$$y_{eq}[n] = x_r[n] - A x_{tr}[n-1]$$

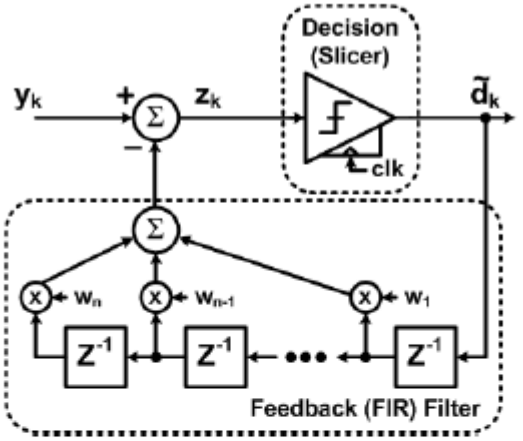
$$= h_o x_{tr}[n] + h_1 x_{tr}[n-1] - A x_{tr}[n-1]$$

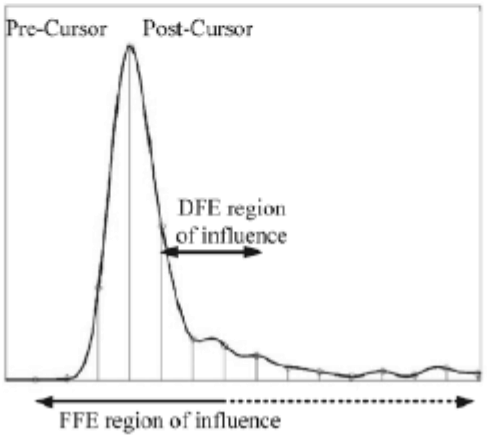
- **DFE is a non-linear equalizer.**
- **Slicer makes a symbol decision, i.e. quantizes input.**
- **ISI is then directly subtracted from the incoming signal via a feedback FIR filter.**

RX DFE Pros & Cons

- **Pros**
  - Can boost high frequency content without noise and crosstalk amplification.
  - Filter tap coefficients can be adaptively tuned without any back-channel.
  - Corrects both loss and reflections.
- **Cons**
  - Cannot cancel pre-cursor ISI.
  - Chance for error propagation
    - Low in practical links (BER=10^{-12})
  - Critical feedback timing path
  - Timing of ISI subtraction complicates CDR phase detection.
  - High power (especially, digital)

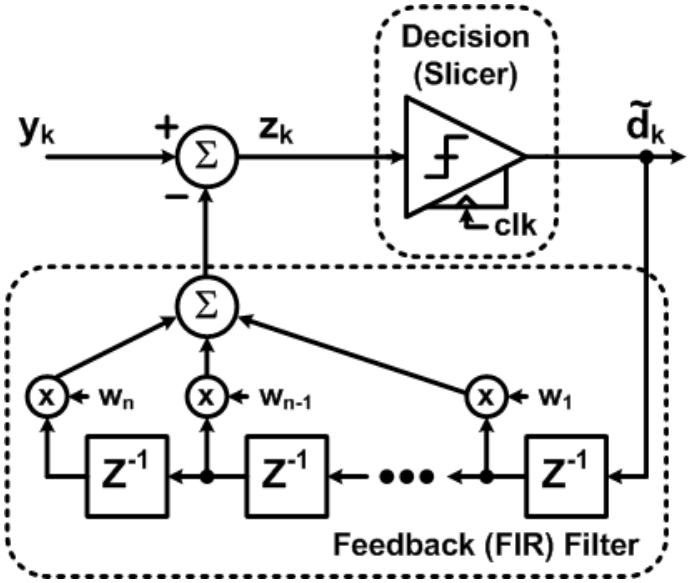
$$z_k = y_k - w_1 \tilde{d}_{k-1} \cdots - w_{n-1} \tilde{d}_{k-(n-1)} - w_n \tilde{d}_{k-n}$$



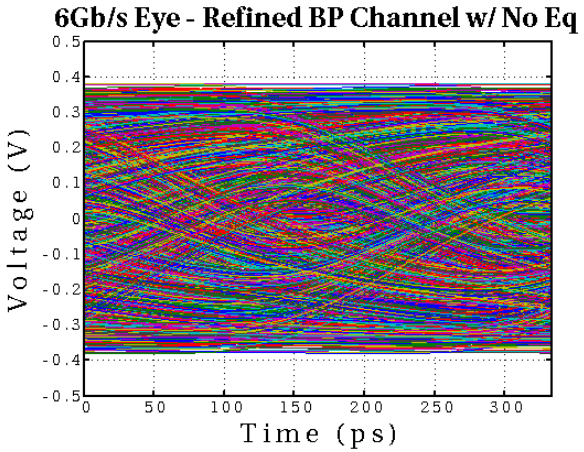


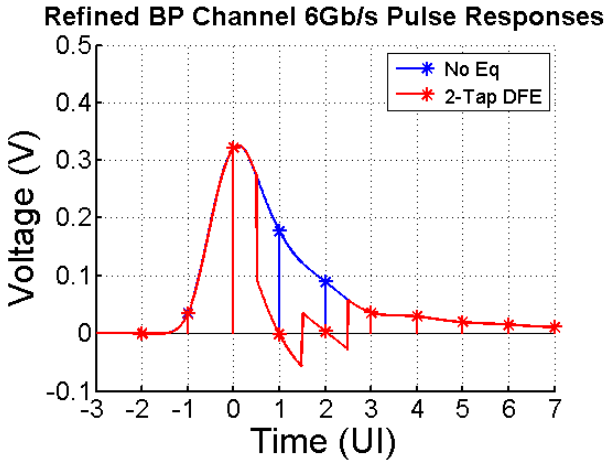
DFE Example

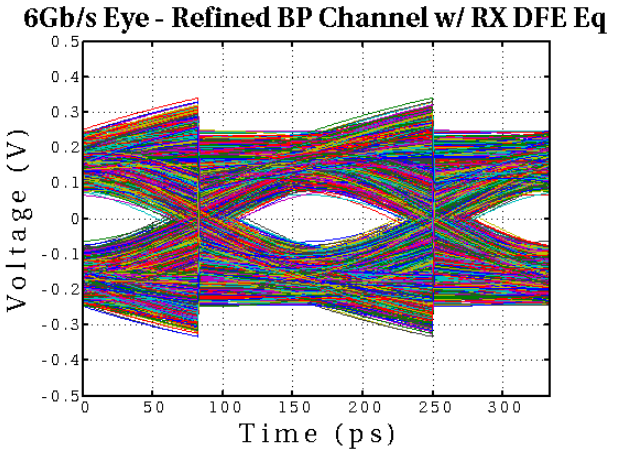
- If only DFE equalization, DFE tap coefficients should equal the unequalized channel pulse response values [a1 a2 … an].
- With other equalization, DFE tap coefficients should equal the pre-DFE pulse response values.



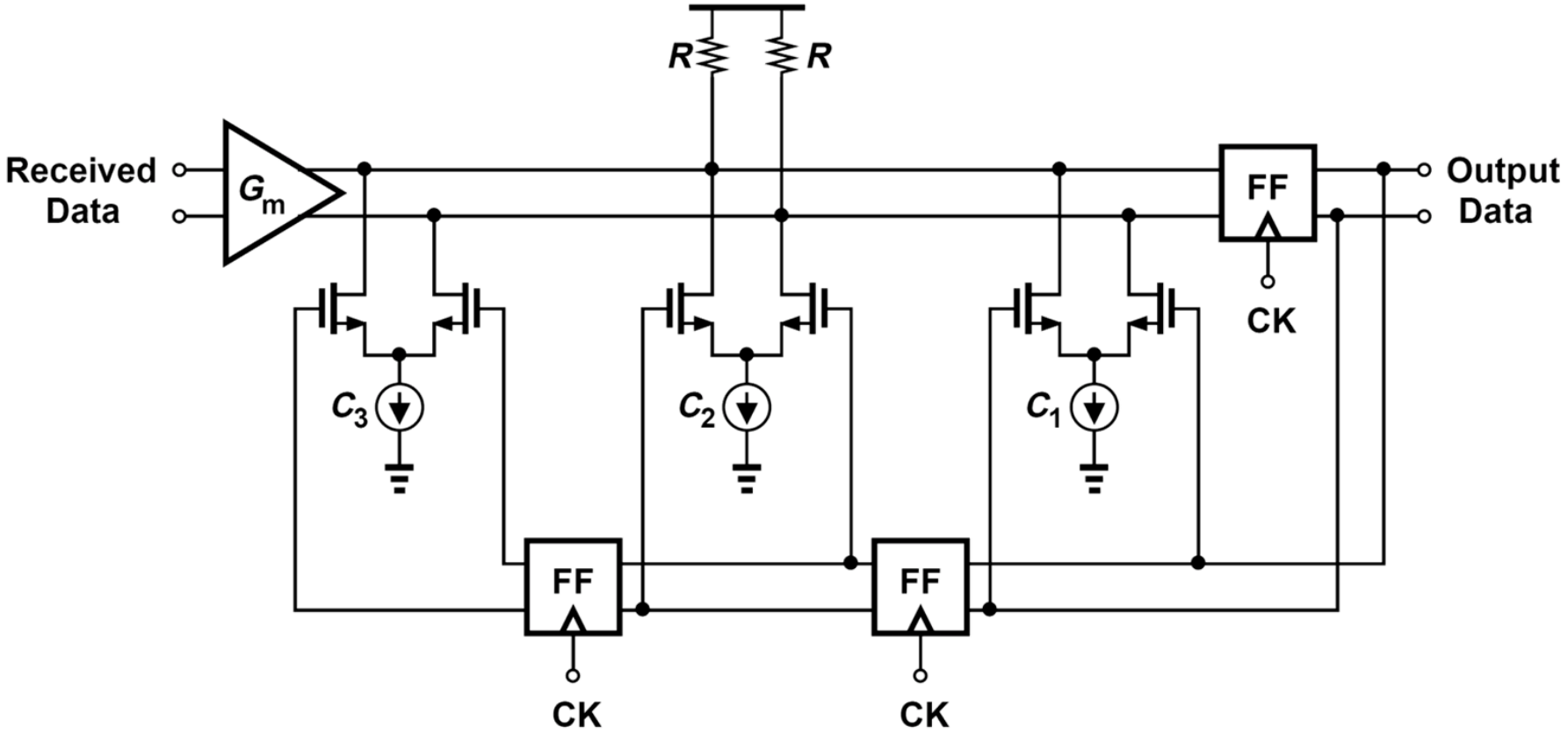
$[w_1\ w_2]=[a_1\ a_2]$







Full-Rate DFE



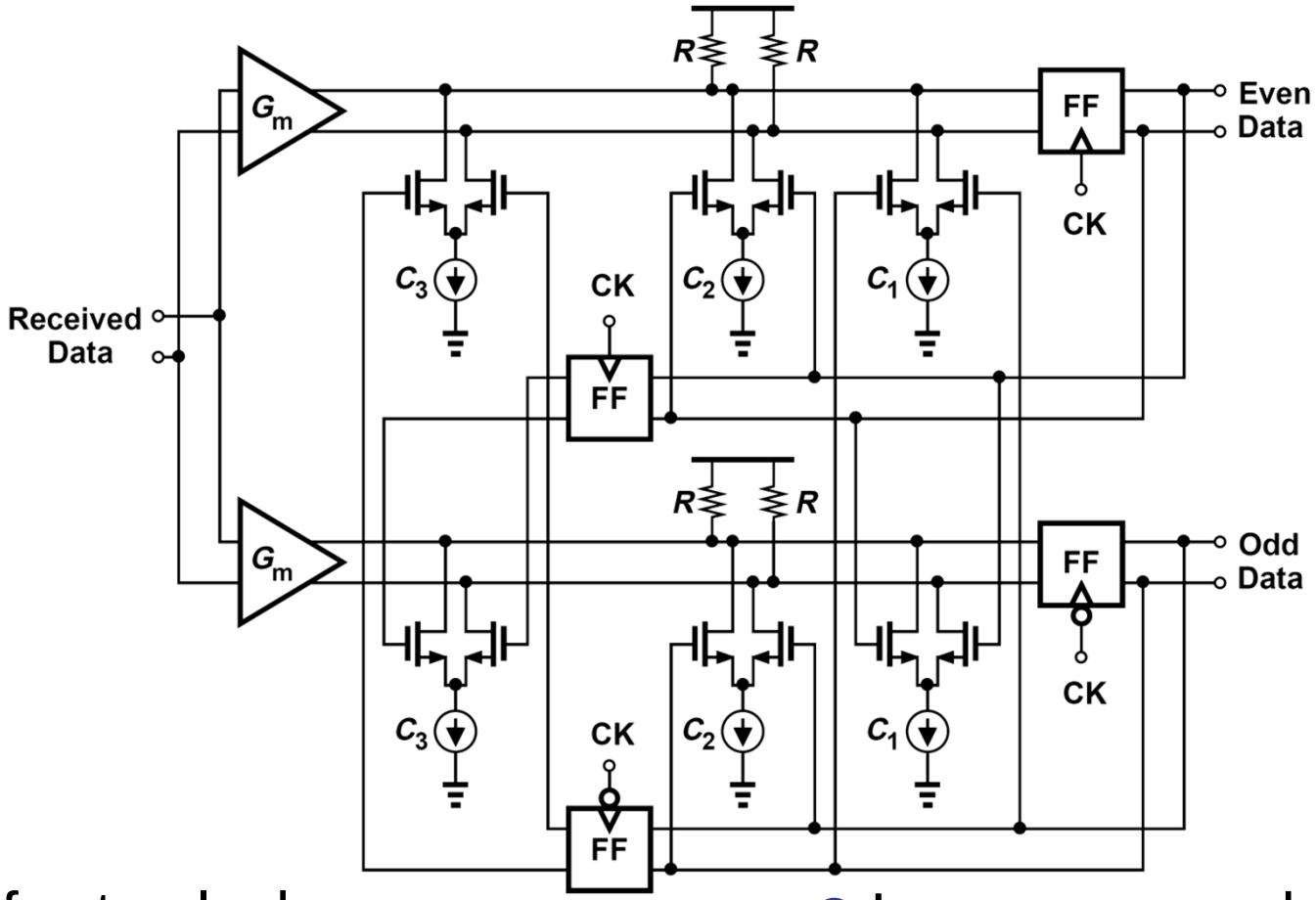
☺ Direct implementation

☺ Lowest complexity

☹ Full-rate clock

$$t_{cq} + t_{setup} + t_{FB} < UI$$

Half-Rate DFE



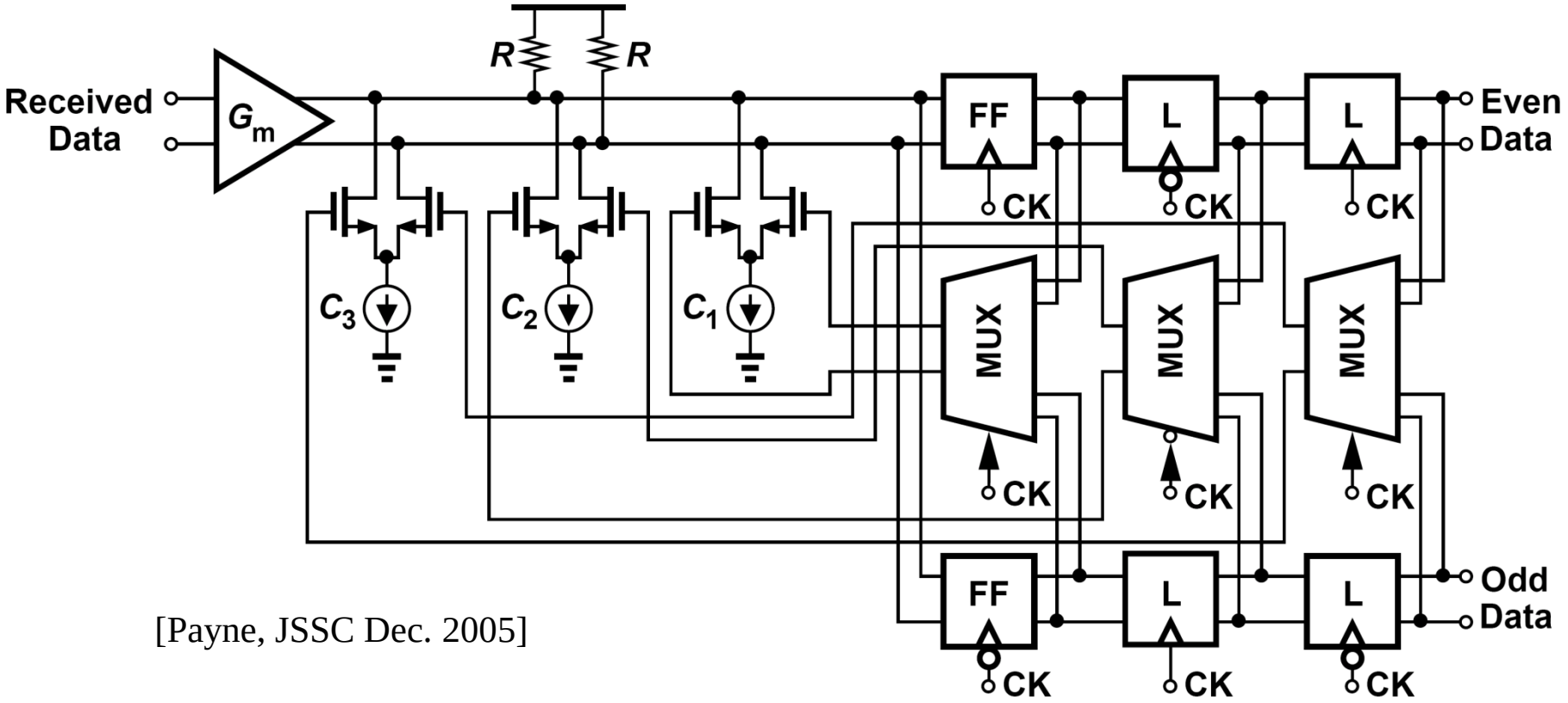
☺ Half-rate clock

☺ Relaxes FF design

☹ Large area and power

$$t_{cq} + t_{setup} + t_{FB} < UI$$

Multiplexed-Half-Rate DFE



[Payne, JSSC Dec. 2005]

- ☺ Half-rate clock
- ☺ Saves one summing node
- ☹ Larger delay

$$t_{cq,FF} + t_{setup} + t_{p,MUX} + t_{FB} < UI$$

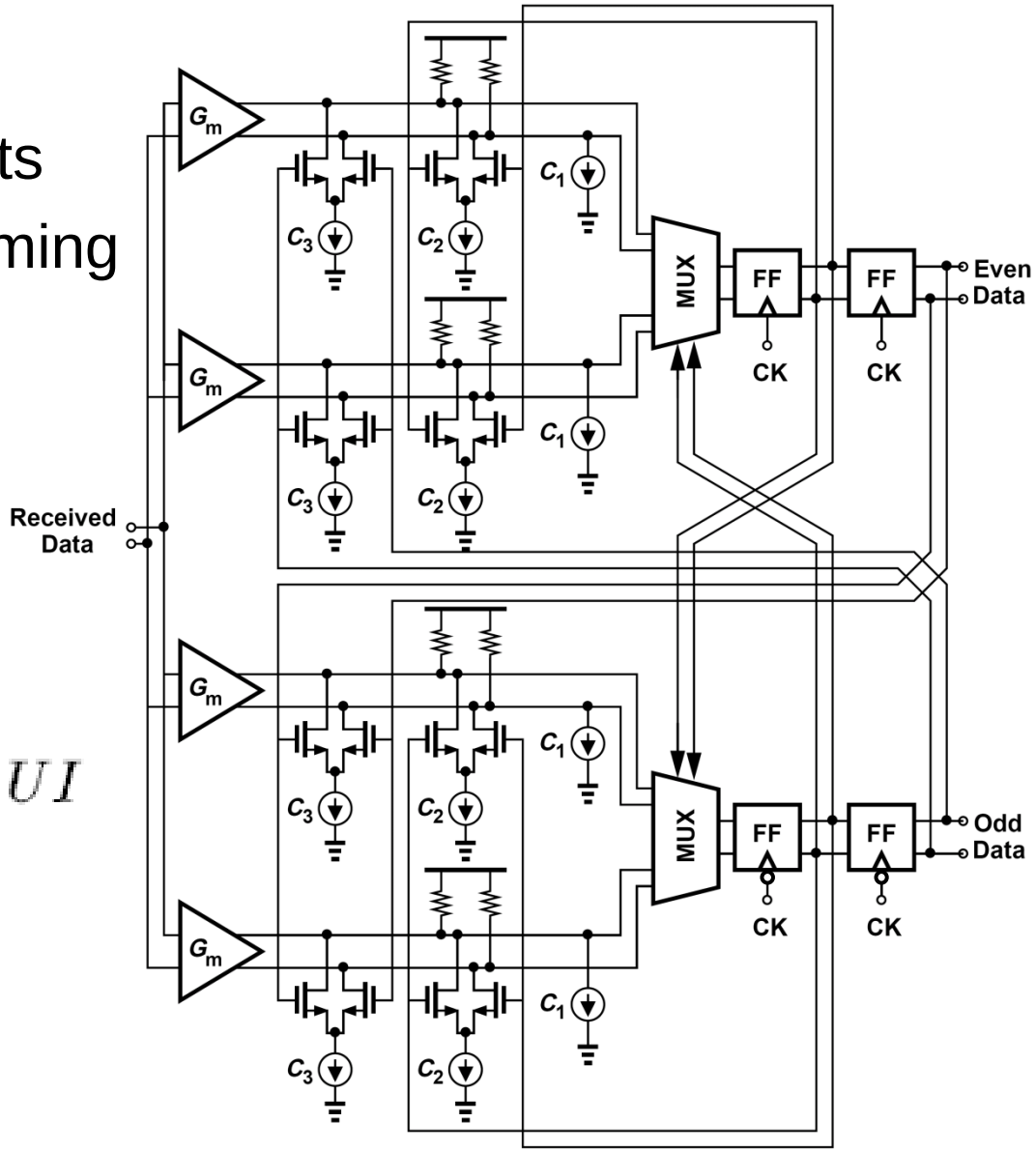
Half-Rate Loop-Unrolled DFE

- ☺ Half-rate clock
- ☺ Relaxes timing constraints
- ☺ Reduces loading at summing nodes

- ☹ High complexity
- ☹ Four summing nodes

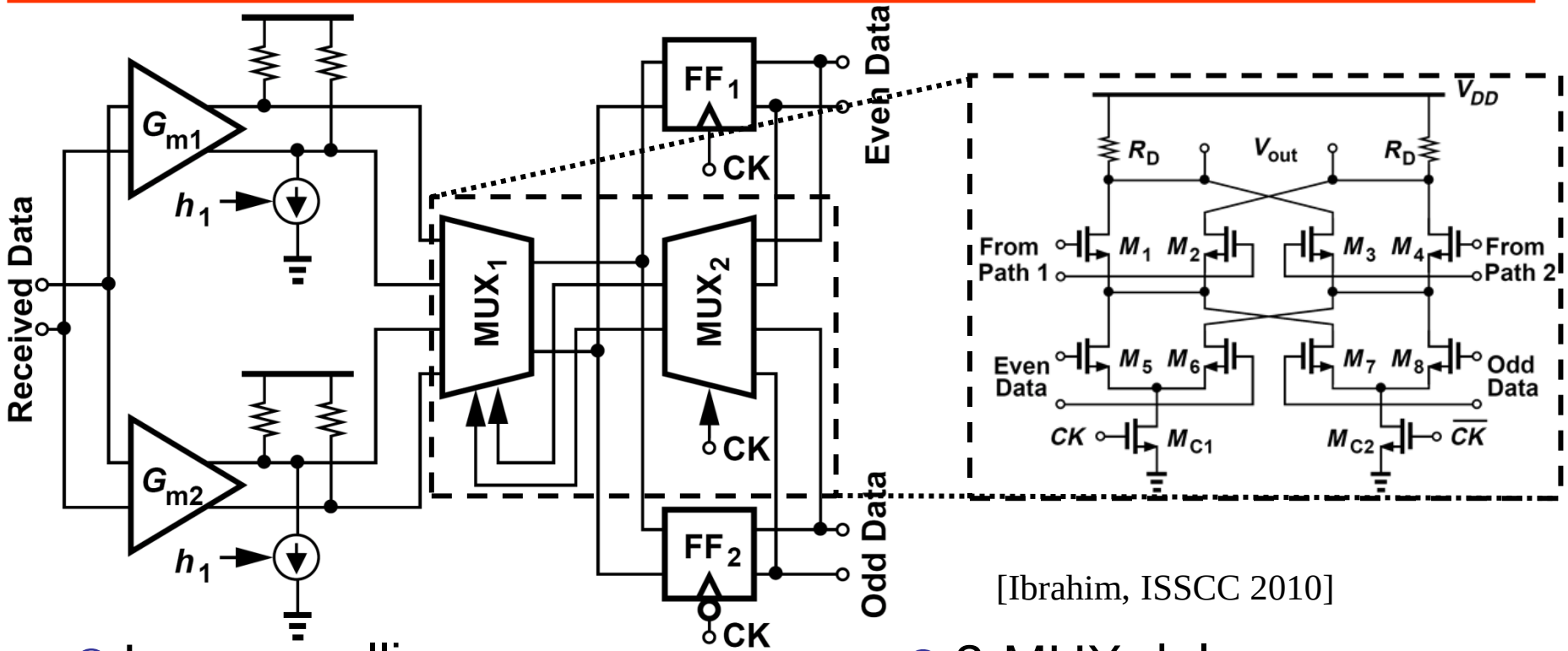
$$t_{cq,FF} + t_{setup} + t_{sq,MUX} < UI$$

- Also called, lookahead, speculative or partial response DFE.



[Bulzacchelli, JSSC Dec.2006]

HR Loop-Unrolled Multiplexed DFE

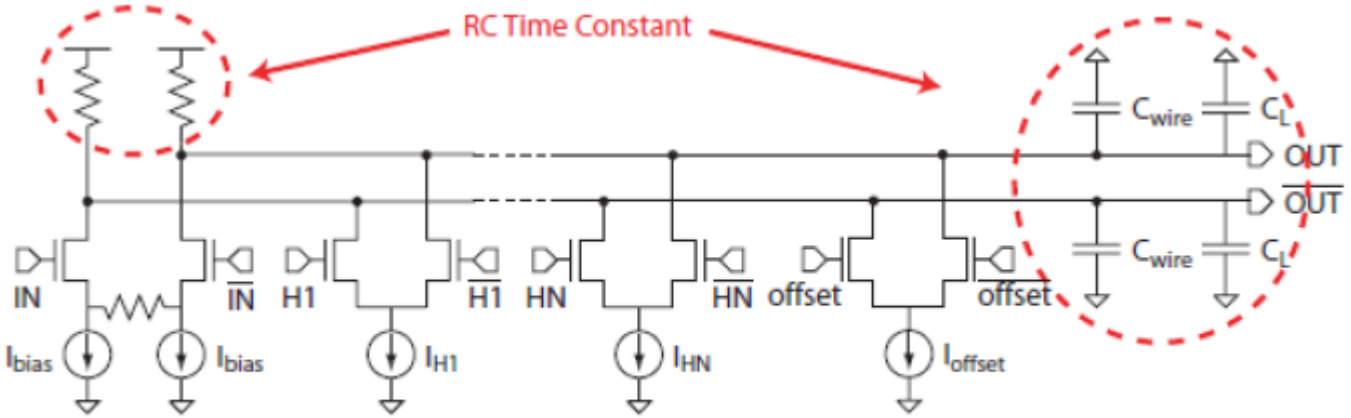


[Ibrahim, ISSCC 2010]

- ☺ Loop unrolling
- ☺ Multiplexing
- ☺ Half-rate clock
- ☺ Other taps can be readily added
- ☹ 2-MUX delay

$$t_{cq,FF} + t_{setup} + t_{sq,MUX_1} + t_{p,MUX_2} < UI$$

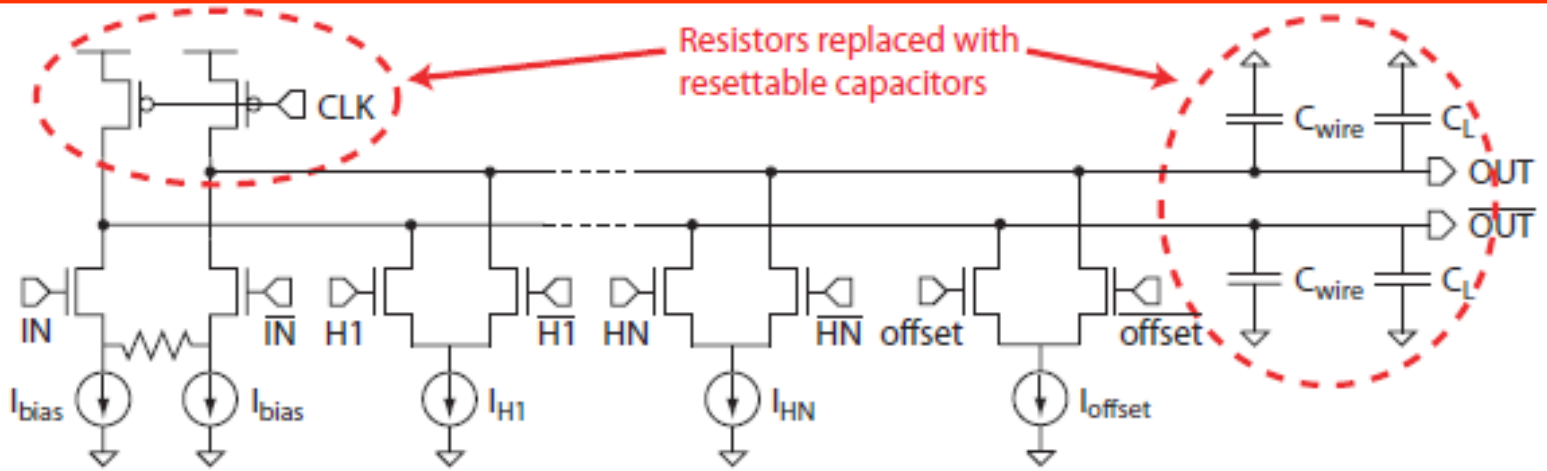
DFE Resistive-Load Summer



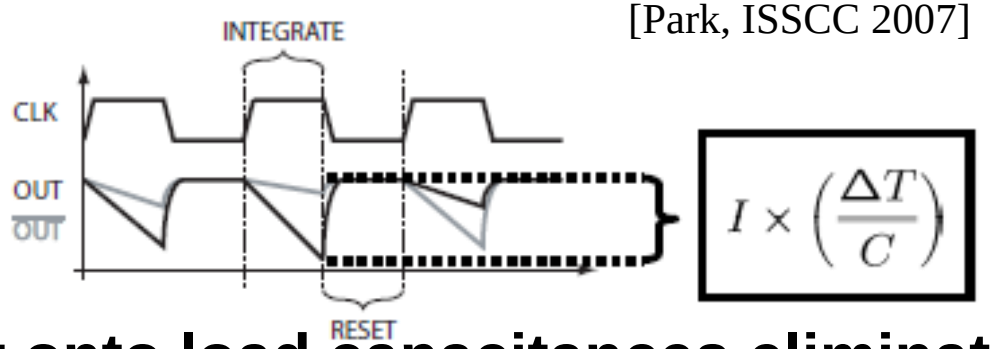
Summer Swing $= IR, \quad \tau = RC$

- **Summer performance is critical for DFE operation.**
- **Summer must settle within a certain level of accuracy (>95%) for ISI cancellation.**
- **Trade-off between summer output swing and settling time.**
- **Can result in large bias currents for input and taps.**

DFE Integrating Summer

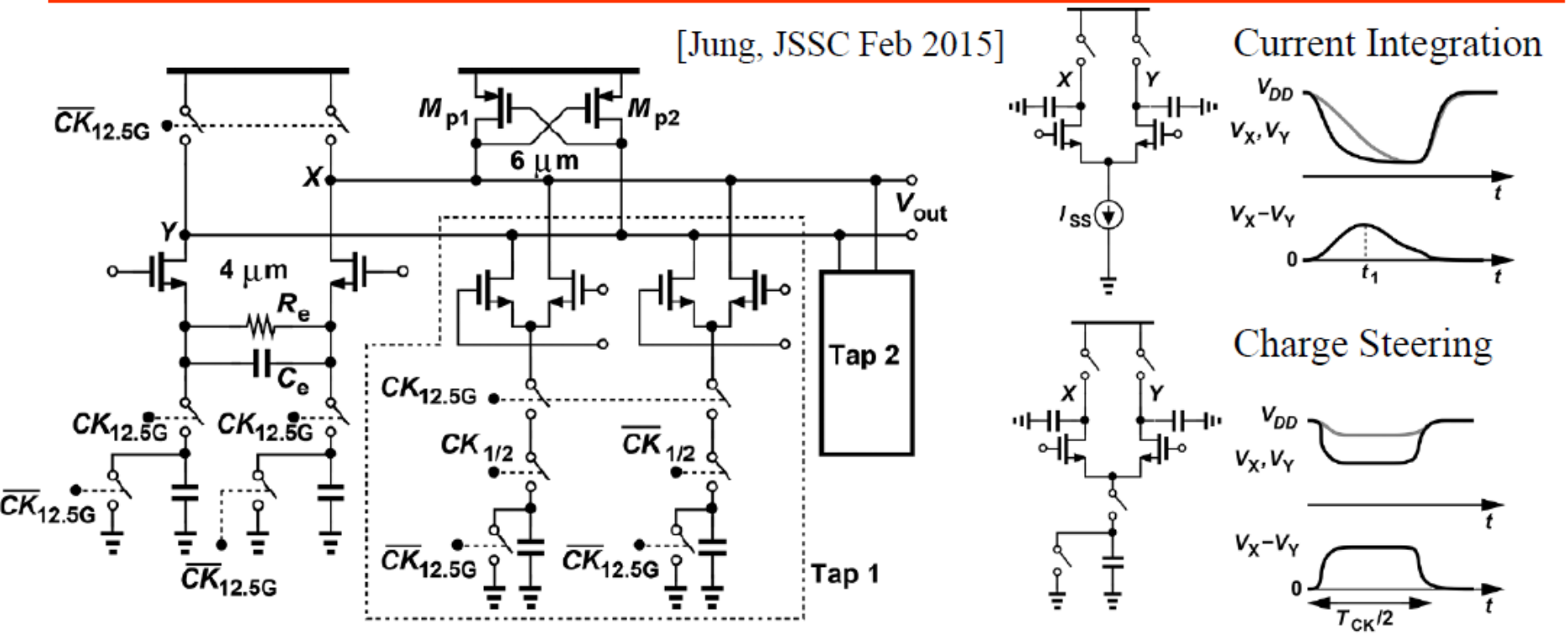


[Park, ISSCC 2007]



- **Integrating current onto load capacitances eliminates RC settling time.**
- **Since ΔT/C > R, bias current can be reduced for a given output swing.**
  - Typically a 3x bias current reduction

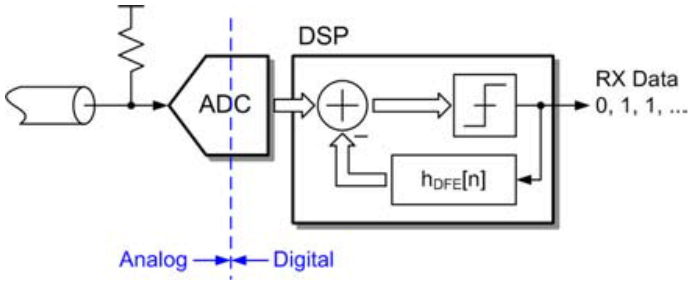
Charge-Steering Summer



- **25 Gb/s DFE with low power consumption**
- **Half-rate design so 12.5G clock is used.**
- **Multiplexed design so 6.25G clock is used to implement MUX.**

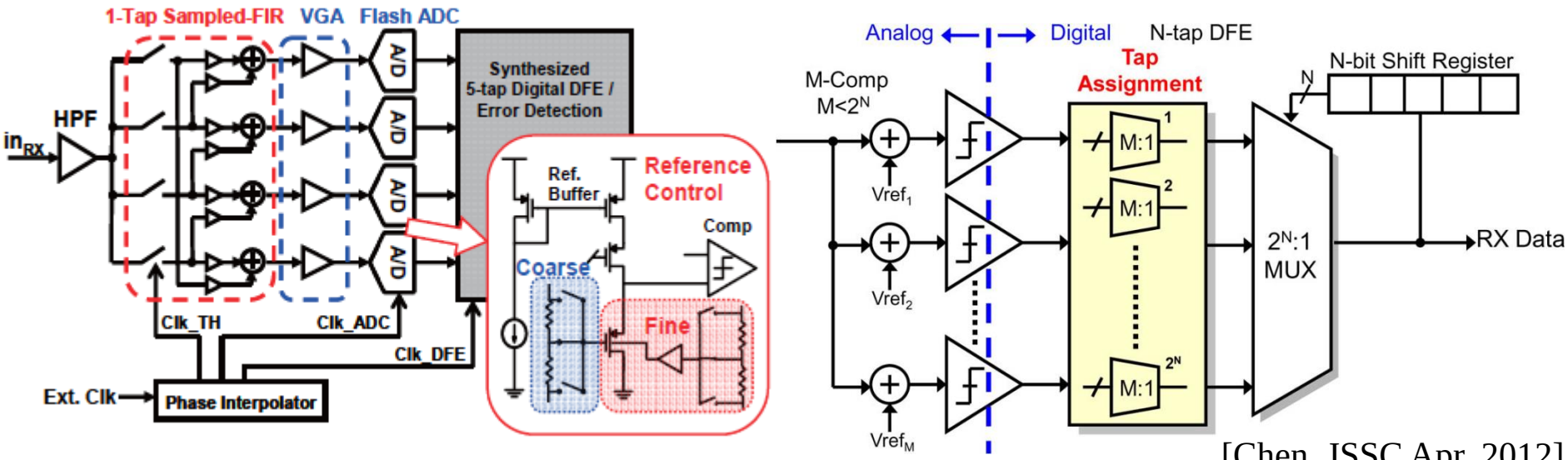
Digital Implementation

- **Similar to RX FIR, RX DFE can be implemented digitally after a high-speed ADC.**



- **Pros**
  - Ability to do both FIR and IIR and even coding all together (correct pre- & post-cursor)
  - More programmable and flexible
  - Better portability
- **Cons**
  - Requires accurate D/A or A/D
  - Very difficult to build at high-speeds
  - High resolution at multi-GS/s
  - Signal processing at multi-GHz

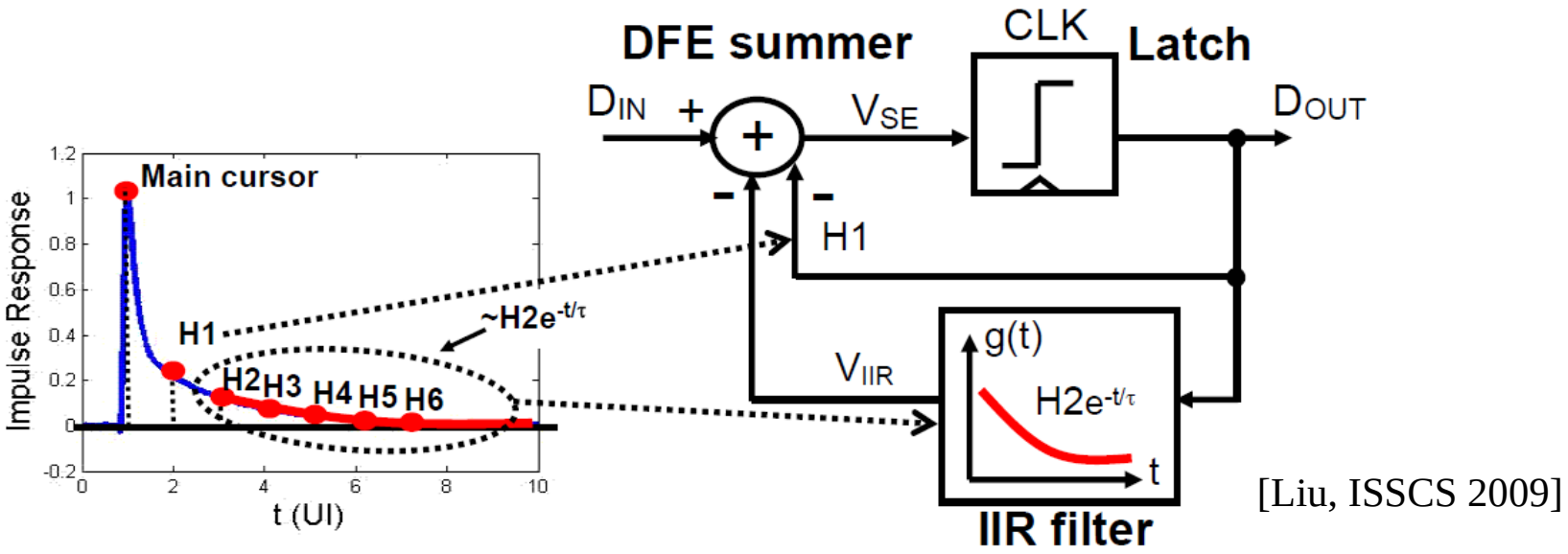
ADC-Based Equalizer Example



[Chen, JSSC Apr. 2012]

- **HPF provides a low-power pre-filtering for post-cursor ISI.**
- **FIR cancels the pre-cursor ISI at lower power than digital.**
- **A VGA (up to 10dB) buffers the signal before the ADC and provides an alternative for ADC FSR adjustment.**
- **An ADC with non-uniform quantization levels is used to reduce number of comparators.**
- **A selection-based DFE is easy to implement in digital.**

DFE with IIR Feedback

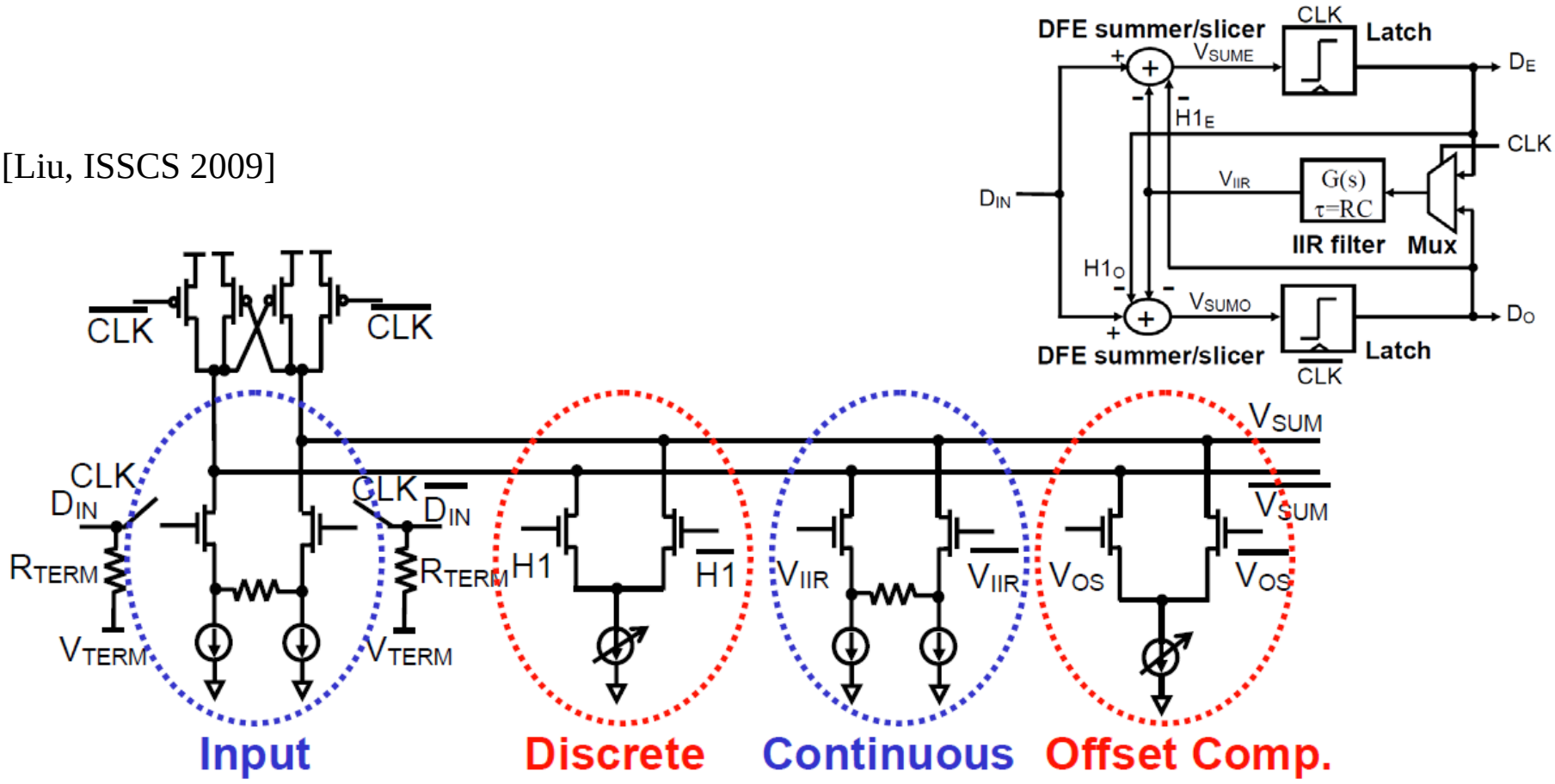


[Liu, ISSCS 2009]

- **Large 1st post-cursor H1 is canceled with normal FIR feedback tap.**
- **Smooth long tail ISI from 2nd post-cursor and beyond is canceled with low-pass IIR feedback filter.**
- **Note: channel needs to be smooth (not many reflections) in order for this approach to work well.**

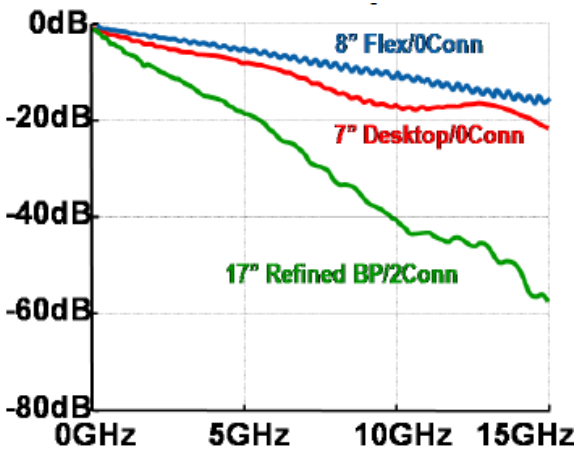
Merged Summer & Partial Slicer

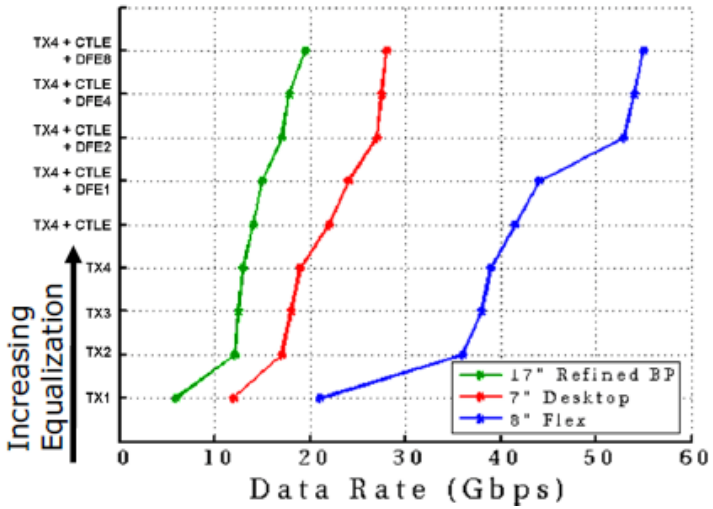
[Liu, ISSCS 2009]



- **Integrating summer with regeneration PMOS devices to realize partial slicer operation.**

Equalization Effectiveness





- **Some observations**
  - Big initial performance boost with 2-tap TX eq.
  - With only TX eq., not much difference between 2 to 4-tap.
  - RX equalization, particularly DFE, allows for further performance improvement
    - Caution – hard to build fast DFEs due to critical timing path