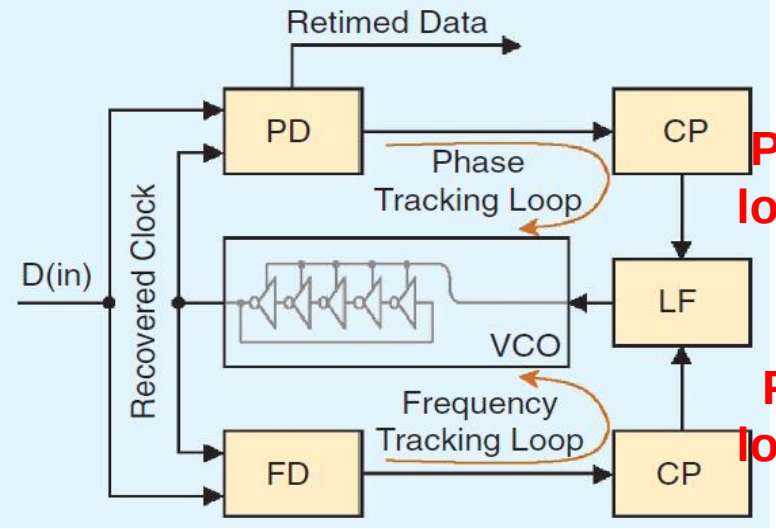
Clock and Data Recovery: Architectures

Lecture 10

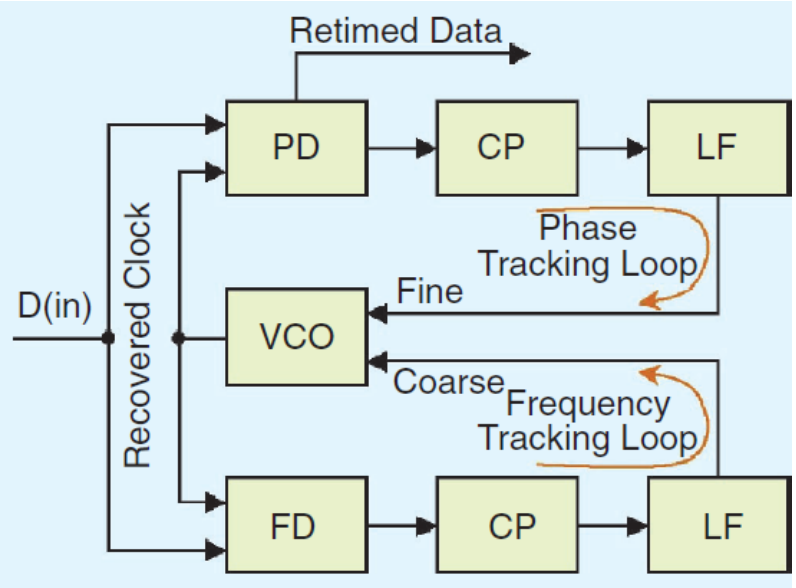
Reference-less PLL-based CDRs



- The freq. detector (FD) provides an output proportional to the frequency error between D_{in} & VCO output → no need for external clock frequency
- At start-up, the FD drives the VCO frequency close to D_{in} then PD takes over to lock on D_{in} phase:
- **Aided Acquisition** allows increasing loop locking range without sacrificing the VCO ripple (or increasing f_{BB})
- The PD & FD may interfere during transferring over to the PD mode, also FD might be confused with long CIDs→ control voltage ripple or failure/false lock

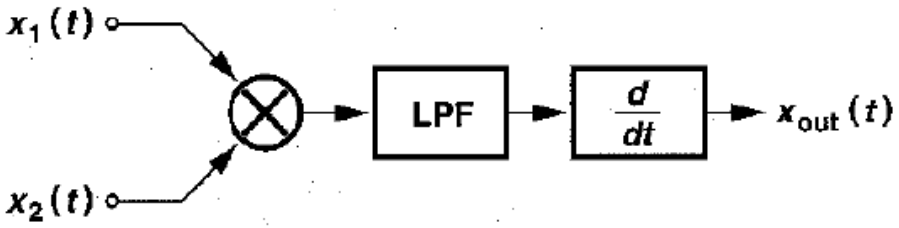
[Ref]: "Architectures for Multi-Gigabit Wire-Linked Clock and Data Recovery," IEEE Circ. & Sys. Magazine, 2008

Reference-less PLL-based CDRs (Cont'd)



- Each loop can drive it own CP & loop filter
- Frequency tracking is typically necessary at power up or to track slow temperature drift → speed is not important
- Loop BW of frequency tracking loop should be << BW of phase tracking loop
- Large BW of phase tracking loop improves CDR jitter tolerance
- Disadvantage: large area → Could combine using analog & digital loop filters

Frequency Detectors (Quadri-correlator)

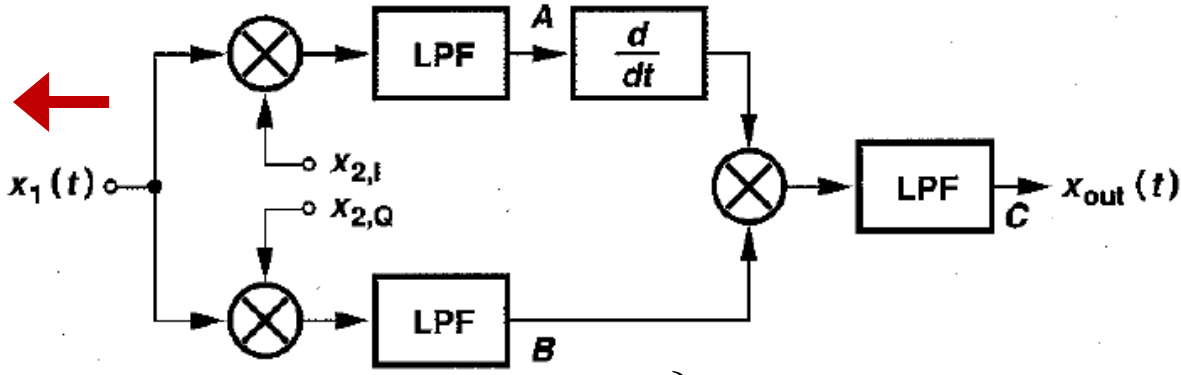


$$X_{out}(t) = \frac{d}{dt}\left(\frac{A_1 A_2}{2}\cos(\omega_1 - \omega_2)t\right)$$

$$= -\frac{A_1 A_2}{2}(\omega_1 - \omega_2)\sin(\omega_1 - \omega_2)t$$

$$X_A(t) = \frac{A_1 A_2}{2}\cos(\omega_1 - \omega_2)t$$

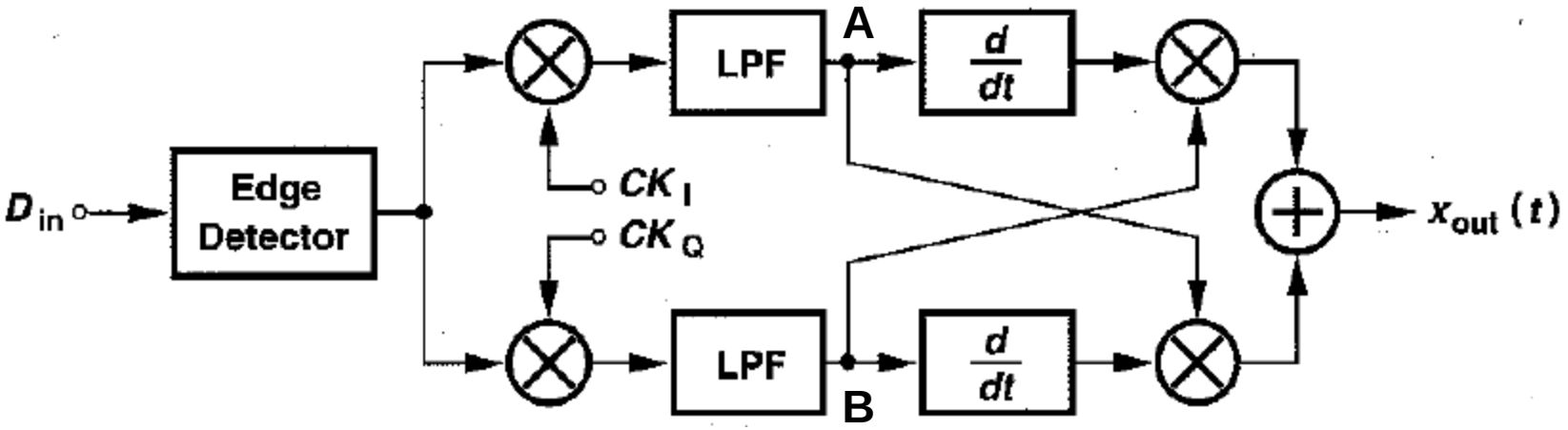
$$X_B(t) = \frac{A_1 A_2}{2}\sin(\omega_1 - \omega_2)t$$



$$X_{out}(t) = LPF\left\{-\left(\frac{A_1 A_2}{2}\right)^2(\omega_1 - \omega_2)\times\left(\frac{1}{2} - \frac{\cos 2(\omega_1 - \omega_2)t}{2}\right)\right\}$$

- $X_1(t)$ has to have a spectral line at f_b → Edge detector
- Close to lock, the component at $2(\omega_1-\omega_2)$ may cause a large ripple at the output

Random Data Balanced Quadri-correlator



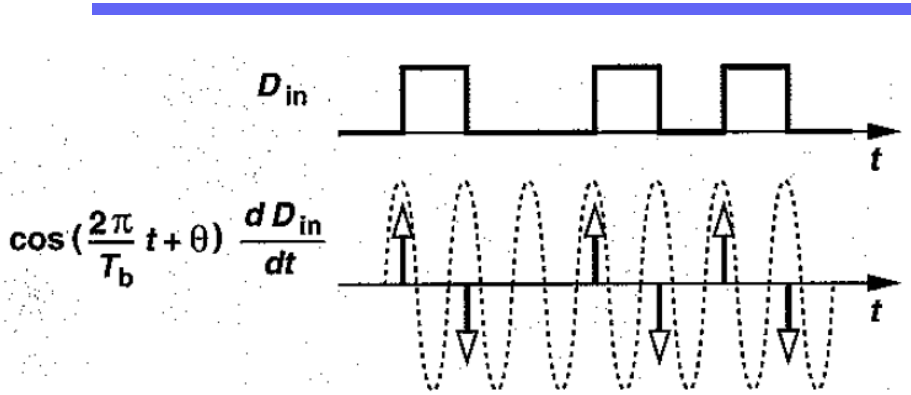
$$X_A(t) = \frac{A_1 A_2}{2}\cos(\omega_1 - \omega_2)t$$

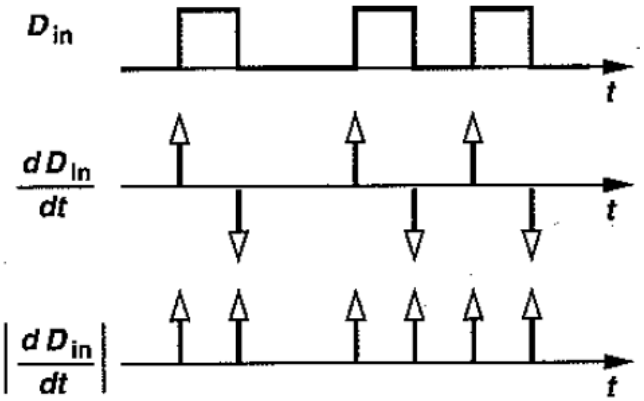
$$X_B(t) = \frac{A_1 A_2}{2}\sin(\omega_1 - \omega_2)t$$

$$X_{out}(t) = -\left(\frac{A_1 A_2}{2}\right)^2(\omega_1 - \omega_2)\times\sin^2(\omega_1 - \omega_2)t - \left(\frac{A_1 A_2}{2}\right)^2(\omega_1 - \omega_2)\times\cos^2(\omega_1 - \omega_2)t$$

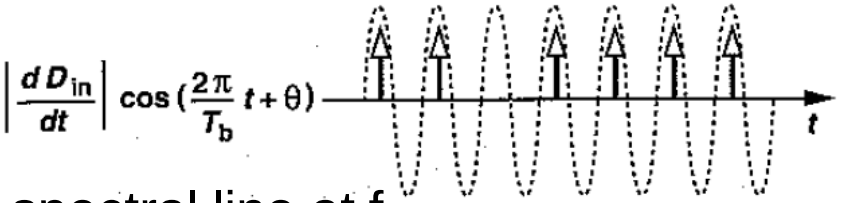
- The balanced quadri-correlator suppresses the component at $2(\omega_1-\omega_2)$ improving the lock behavior

Creating a Spectral line at f_b (Edge Detection)



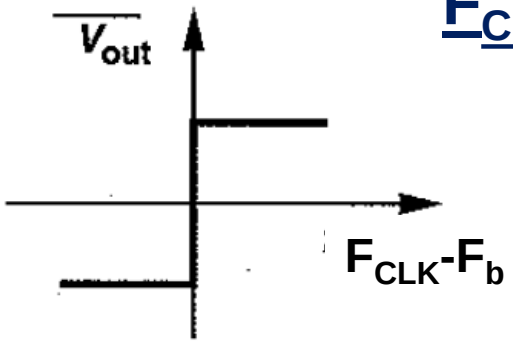


Differentiation is a linear operation:
will not create a spectral line

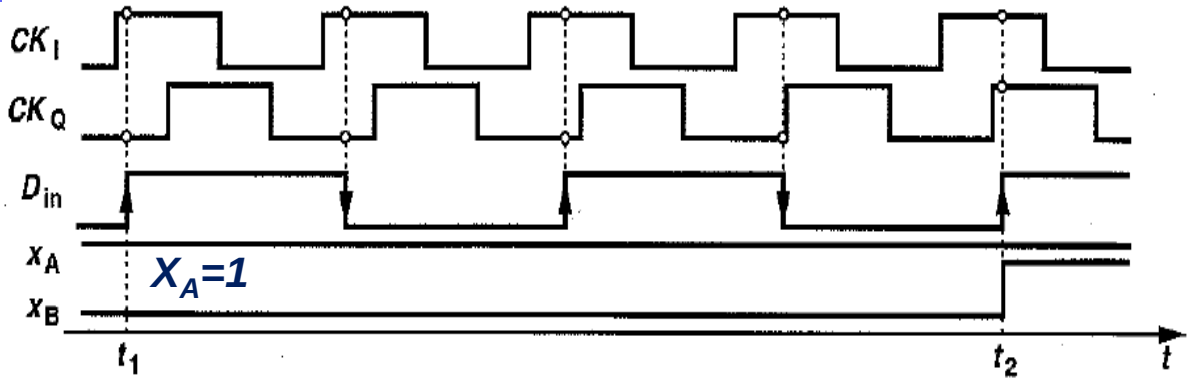


- Random data D_{in} doesn't include a spectral line at f_b
- Differentiating D_{in} still produces 0 when correlated with $\cos(\omega_b t+\theta)$ → No Edge detection
- If the –ve impulses are converted to +ve impulses the correlation will yield a non-zero value
- Differentiation & Rectification produces a spectral line at f_b →Edge detection

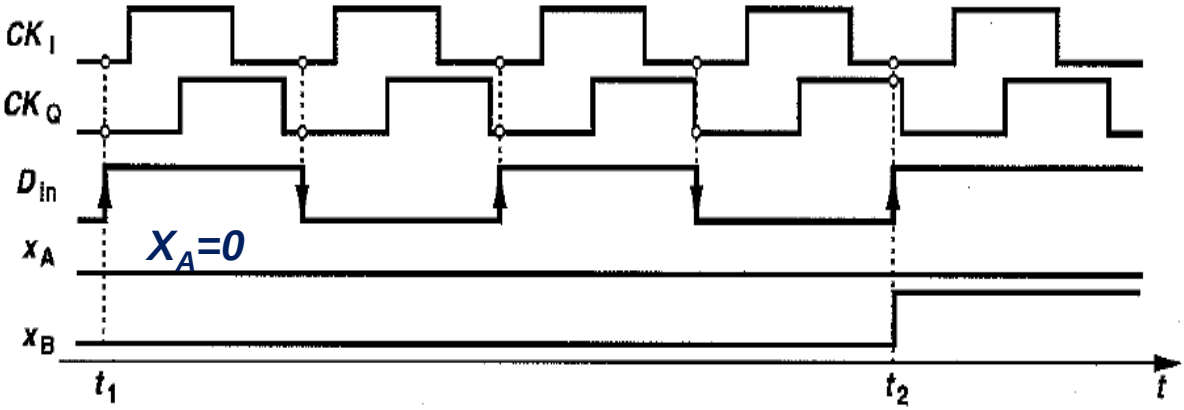
Digital Quadri-correlator



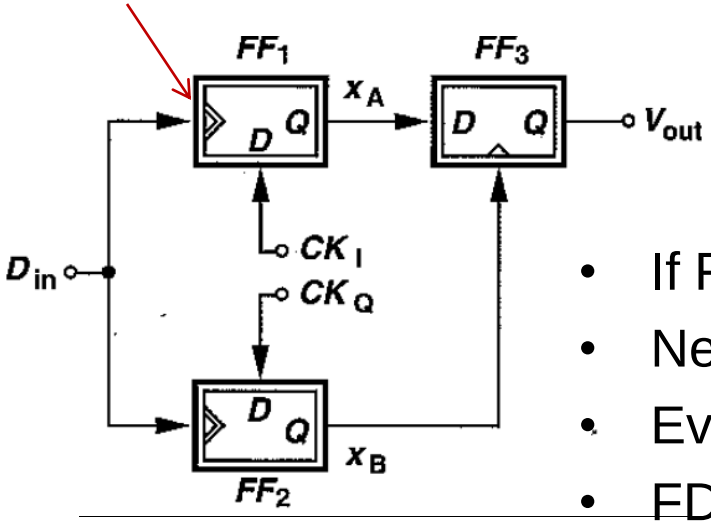
$F_{CLK}>F_b$



$F_{CLK}<F_b$

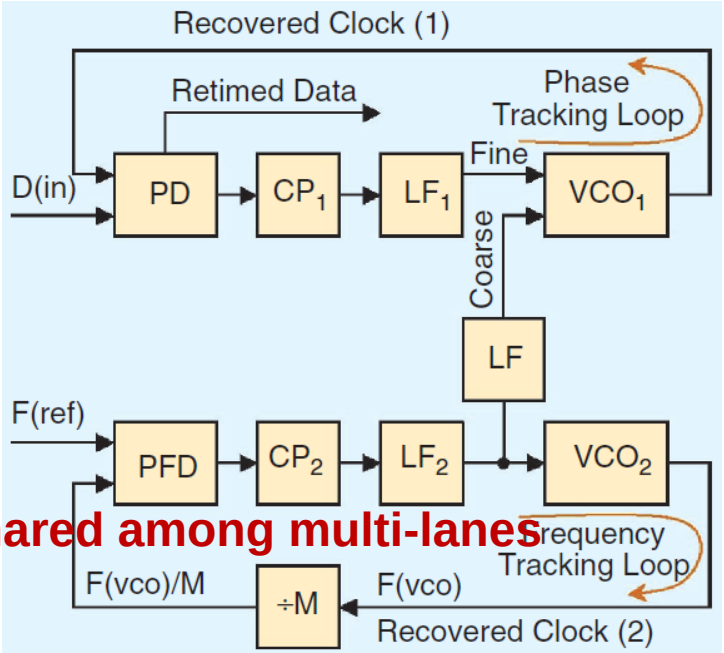


Double edge sampling FF



- If $F_{CLK}>F_b$, at $t=t_1$ X_A samples a 1 & X_B samples 0
- Next sampling occurs at $t=t_1+T_{CLK}+\Delta$
- Eventually, X_B will sample a 1 resulting in $V_{out}=1$
- FD exhibits a bang-bang characteristics

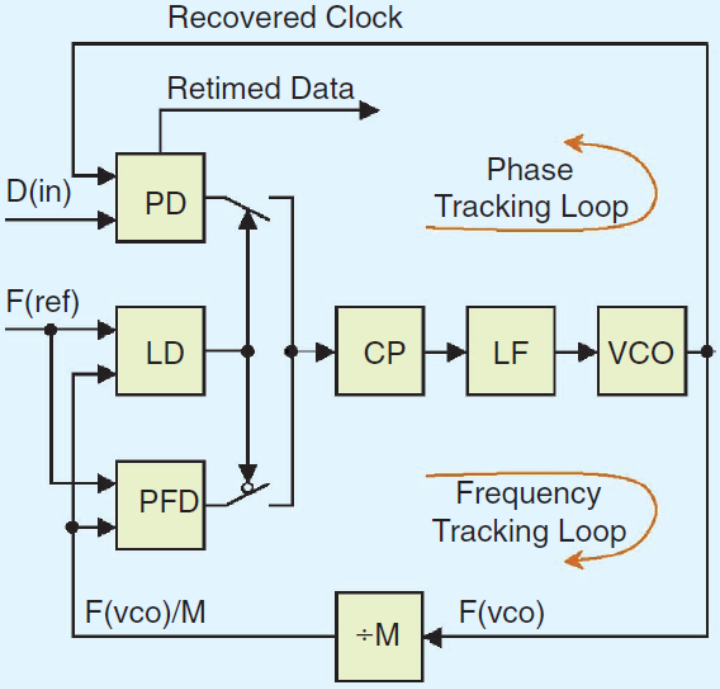
PLL-based CDRs with External Reference Clock



- *Advantages:*
  - ✓ *Availability of separate VCO_2 control → faster acquisition time for phase locking*
- *Disadvantages:*
  - X *Sensitive to mismatches between VCO_1 & VCO_2 ($f_1 \neq f_2$)*
  - X *If the Tx has finite frequency offset the 2 VCOs will be running at different frequencies → frequency pulling*

- Freq. tracking loop locks VCO_2 output to F_{ref}*M
- VCO_2 control voltage is applied to VCO_1 (VCO_2 is a replica of VCO_1)
- This centers VCO_1 around the input data rate & allows the phase tracking loop to lock the phase of VCO_1 to D_{in}
- The gain of the phase tracking loop must be (fine step) << the gain of the frequency tracking loop (coarse step)

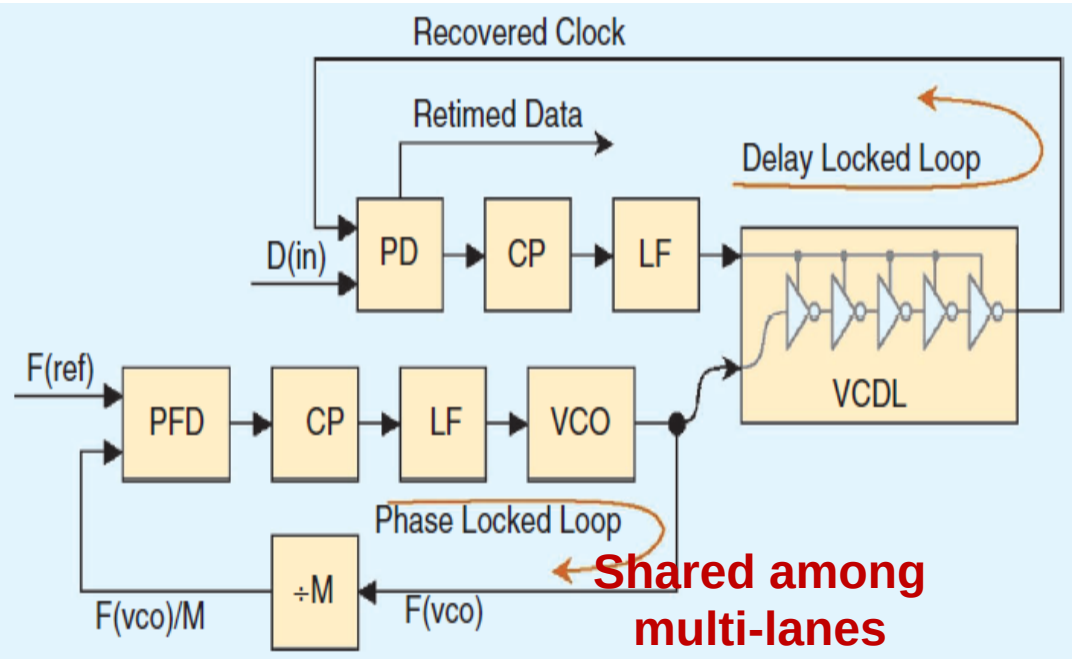
PLL-based CDRs with External Reference Clock



- *Advantages:*
  - ✓ *Eliminates the extra CP, LF, & VCO → no mismatch issues*
- *Disadvantages:*
  - X *Transition from freq. to phase tracking loops might cause disruption to VCO control causing freq. shift → failure to lock or ripple on VCO control*

- A lock detector (LD) can be used to sequentially switch between the freq. & phase tracking loops
- When the LD senses that the difference between F_{ref} and F_{vco}/M is small it switches to the phase tracking loop

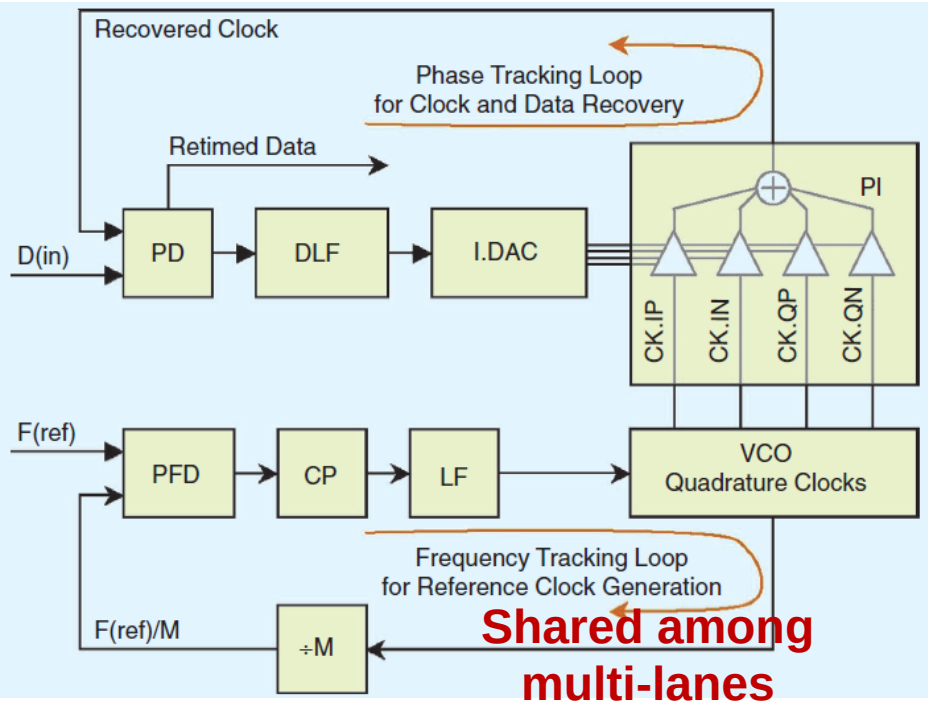
Delay Lock Loop (DLL)-based CDR



- *Advantages:*
  - ✓ *VCDL directly alters the clk phase → no freq. to phase integration (1 less pole): more stable*
  - ✓ *Faster locking*
  - ✓ *No jitter accumulation*
- *Disadvantages:*
  - X *Limited capture range*

- Freq. tracking loop provides a high speed clk instead of a voltage
- Phase tracking loop uses a voltage-controlled delay line (VCDL) to lock to the phase of D_{in}
- F_{ref}*M must be the same as the input data rate, suitable for source-synchronous applications (chip-to-chip)

Phase Interpolator (PI)-based CDR



- *Advantages:*
  - ✓ *Increases system stability*
  - ✓ *Faster locking*
  - ✓ *No jitter accumulation*
  - ✓ *No jitter peaking (if loop latency is small)*
  - ✓ *Can operate over limited range of frequency offset*
- *Disadvantages:*
  - X *Need to deliver quadrature clks across the chip*

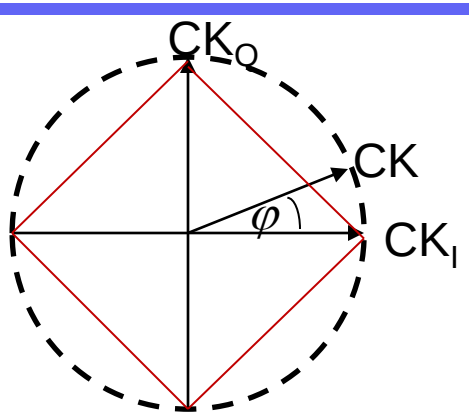
- Similar to the DLL, but uses a digital loop filter DLF, current DAC, PI
- Output of the I-DAC is a current α to DLF output → controls how much gain is assigned to the I-clk & Q-clk to control the recovered clk phase

Ideal Phase Interpolation

Starting with 2 quadrature clocks, with amplitude A:

$CK_I = Acos(\omega t)$

$CK_Q = Acos(\omega t - 90) = Asin(\omega t)$



For any desired angle φ, <u>with fixed amplitude A</u>:

$CK = Asin(\omega t - \varphi)$

$CK = Asin(\omega t)cos(\varphi)$- $Acos(\omega t)sin(\varphi)$

$CK = A_I CK_Q + A_Q CK_I$ (phase interpolation)

$A_I = cos(\varphi)$ & $A_Q = sin(\varphi)$ → $A_I^2 + A_Q^2 = 1$ for constant amplitude (circle)

$$\varphi = tan^{-1}\left(\frac{A_Q}{A_I}\right)$$

In practice, most designs use a simpler implementation which results in $A_I + A_Q = 1$ → diamond shape

Jitter of Digital PI-based CDRs

- In CDRs with digital loop filters dithering jitter is proportional to the feedback loop delay and phase resolution of the PI
- Dithering jitter is the main source of the deterministic jitter in PI CDRs
- A decimation filter that counts early or late decisions of the phase detector is employed to reduce the dithering jitter

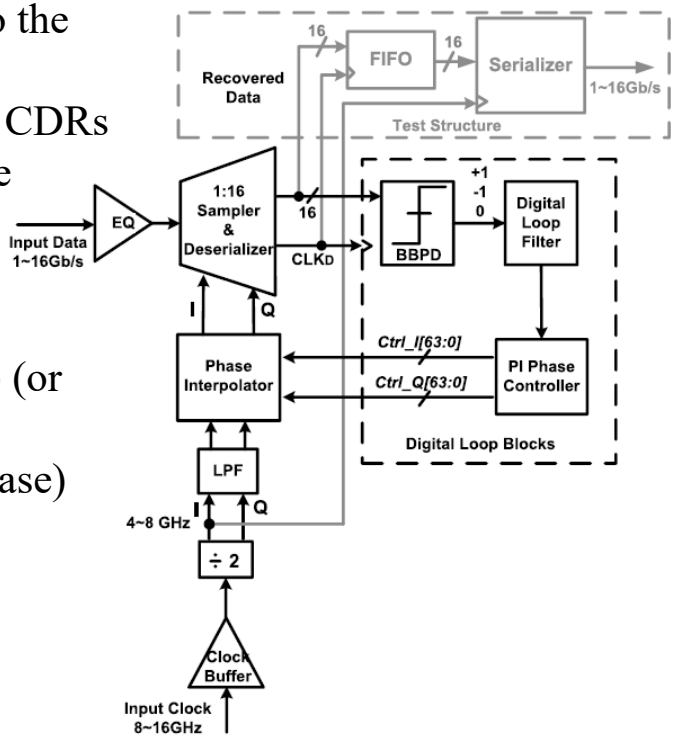
$$\theta_{\text{dither}} = 2 \cdot m \cdot K_{\text{DLL}} \cdot K_{\text{PI}}$$

m is the loop latency in the control loop (in UI), K_{PI} is the phase step (or resolution) of the PI, and K_{DLL} is the decimation filtering factor

- Slew rate SR (maximum rate at which the loop updates the PI phase) defines its tracking capability

$$\text{SR} = \frac{\text{Phase step}}{\text{Phase update period}} = K_{\text{PI}} \cdot f_{\text{update}} \cdot K_{\text{DLL}}$$

where f_{update} is the clock frequency of the digital CDR control blocks



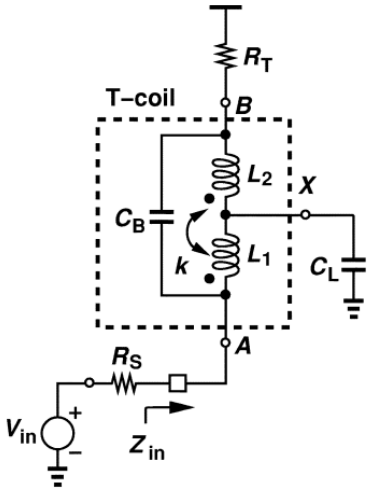
- SR should be > the phase changing rate caused by input sinusoidal jitter A_{mod}

$$A_{\text{mod}} < \frac{\text{SR}}{2\pi \cdot f_{\text{jitter}}} = \frac{K_{\text{PI}}}{2\pi} \cdot \frac{f_{\text{update}} \cdot K_{\text{DLL}}}{f_{\text{jitter}}}$$

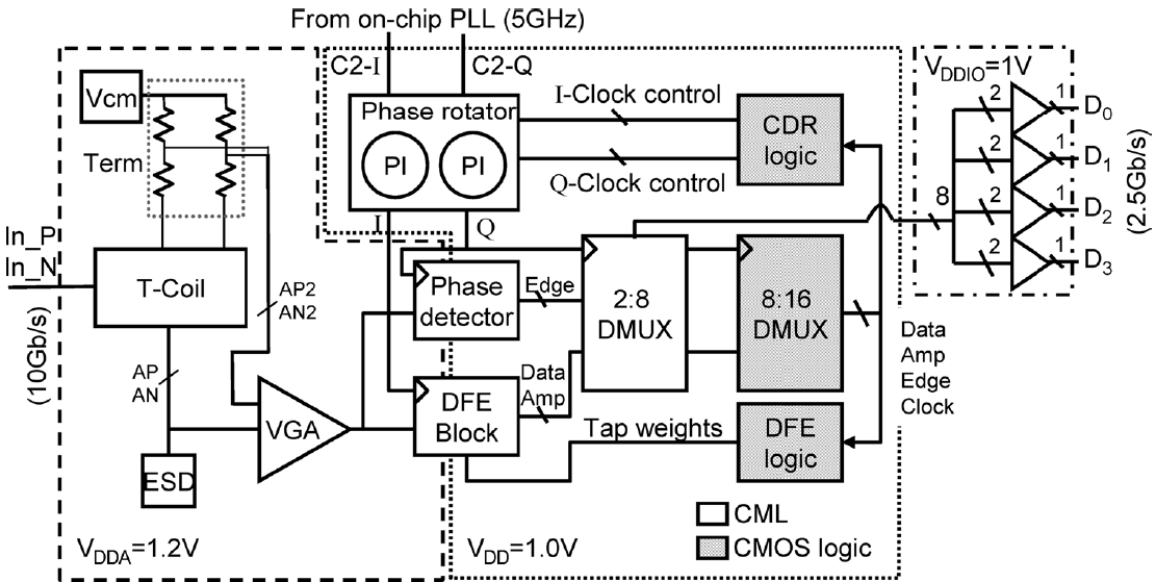
where f_{jitter} is the frequency of the jitter modulated on the incoming data

G. Wu et al., "A 1–16 Gb/s All-Digital Clock and Data Recovery With a Wideband High-Linearity Phase Interpolator," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 24, no. 7, pp. 2511-2520, July 2016.

JSSC 2006: A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology



Proper choice of T-coil parameters provides BW~2.2/$R_L C_L$

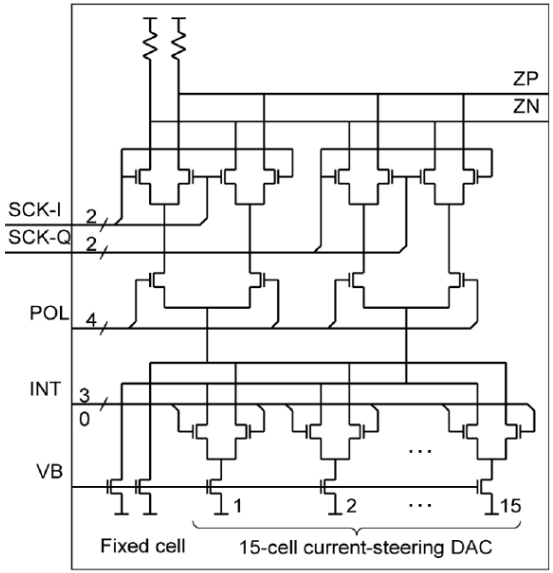


- Phase interpolation (PI) by phase rotators controlled by a digital CDR loop generates the I & Q and clocks used to sample the centers and edges of the data bits
- Half-rate CDR logic converts the data and edge samples into early and late signals which are digitally filtered to generate INC/DEC signals that control the PI
- Digital PI must be precise not to degrade the timing of the recovered clock

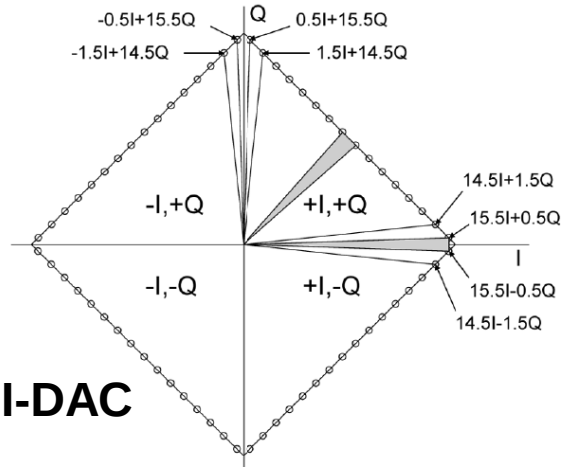
J. F. Bulzacchelli et al., "A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology," in IEEE Journal of Solid-State Circuits, vol. 41, no. 12, pp. 2885-2900, Dec. 2006.

JSSC 2006: A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology

- The phase rotator is driven by two differential quadrature clock phases
- The circuit selects the quadrant then interpolates to generate 16 phases per quadrant for a total of 64 on a 360^{o} (2 UI) circle



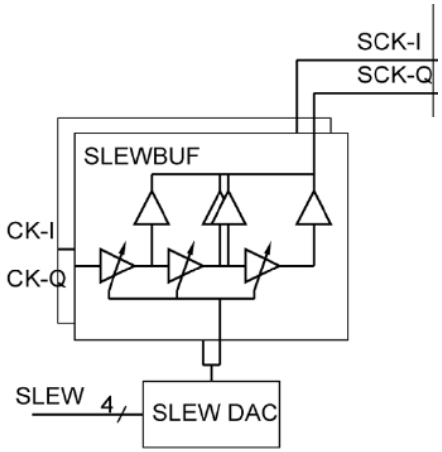
PI

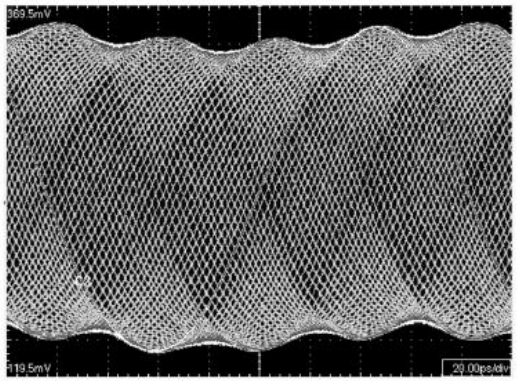


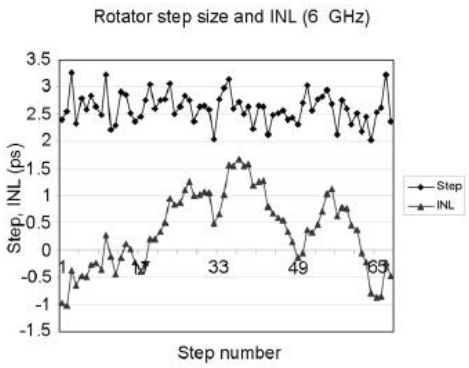
I-DAC

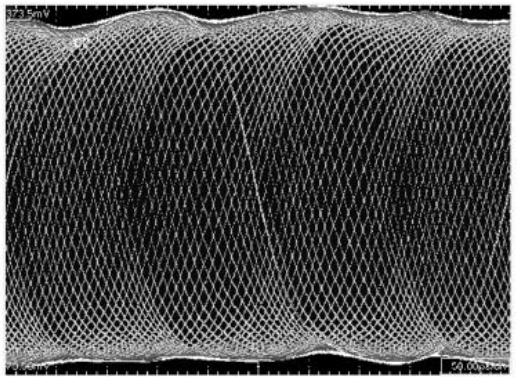
- The interpolator uses a current-steering DAC as tail currents
- Rotator has a diamond-shaped, due to constant total interpolator tail current → non uniform angles close to quadrant edges
- The current-steering DAC has 2 fixed cells of half-size → 0.5:15.5 to 15.5:0.5
- Fixed cells improve rotator settling time
- 15 steering DAC cells are not uniform; the largest cells are switched near the quadrant boundaries

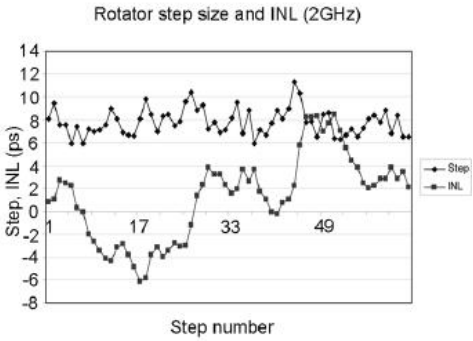
A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology: JSSC 2006





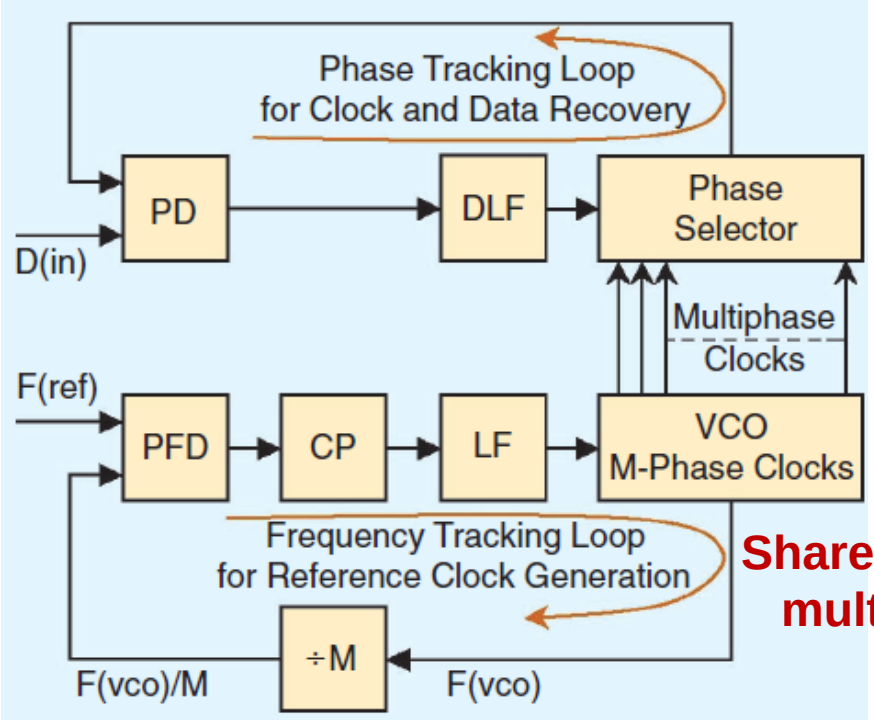






- Slew-rate-control buffers are required to ensure the signals going to the PI are sinusoidal for proper interpolation
- PI step scales with data rate since it is 360/no. of states:
  - At 2GHz step =2.7ps
  - At 6 GHz step=8ps
- Amplitude variation is periodic, CDR samplers not sensitive to amplitude variation

Phase Interpolator (PI)-based CDR



Shared among multi-lanes

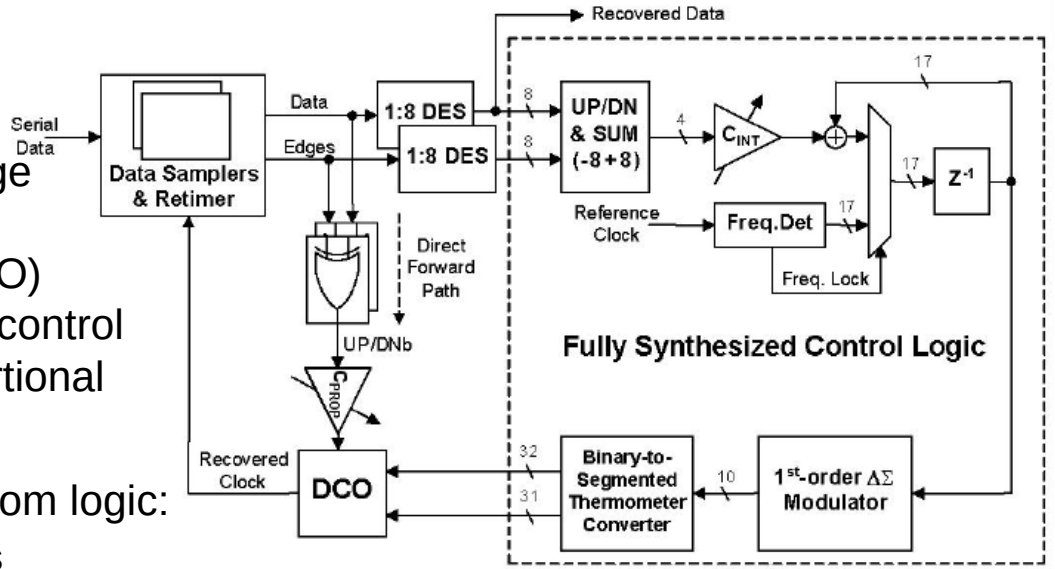
- I-DAC and PI replaced with a phase selector → All digital implementation (more robust to PVT variations)
- Discrete phase steps
- Independent phase & frequency tracking loops → simplifies loop BW/stability Requirements

All Digital PLL-based CDRs

- In deep submicron technologies Analog CDRs suffer from :
  - Insufficient voltage headroom
  - Large area occupied by integral loop capacitor
    - Design sensitive to leakage currents
- All digital CDRs:
  - Easy porting between process nodes
  - Offers easy method to program loop behavior K_{prop} & K_{int} → settling, bandwidth, stability, jitter tolerance…

ISSCC 2007: All-Digital CDR with a 10-bit Monotonic DCO

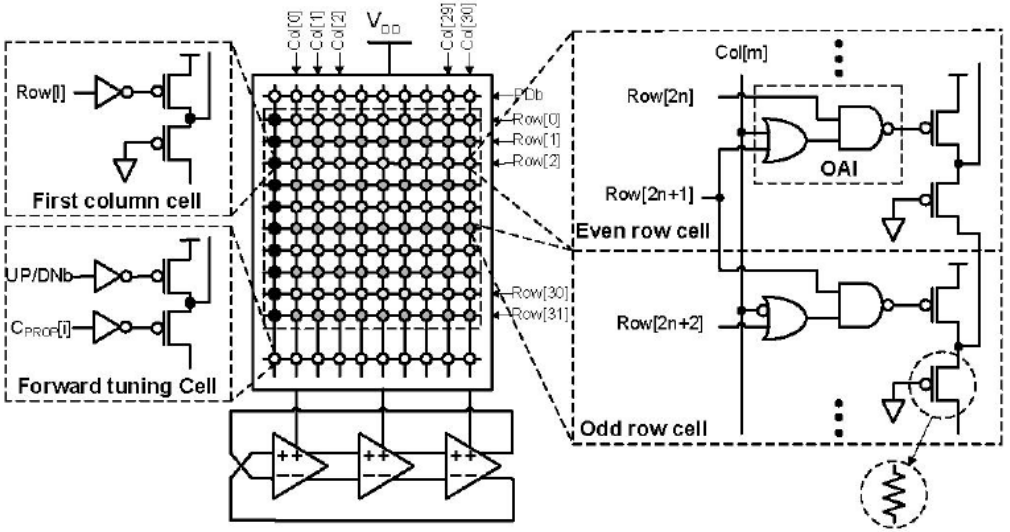
- The CDR consists of:
  - Bang-band phase detector
  - 1:8 de-serialiers for data and edge samples
  - Digitally controlled oscillator (DCO)
- High speed UP/Down signals directly control the DCO frequency to form the proportional path



- The integral path is formed by the custom logic:
  - Generates low speed UP/Down signals
  - 17 bit Loop integrator synthesized using a digital IIR filter
  - A digital 1st order delta-sigma modulator converts the 17 bit frequency code to a dithered 10 bit DCO code
  - To guarantee the monotonicity of the DCO the 10 bits control code is converter to a segmented thero-mometer code (32 + 31) bits.
- Frequency detection is also done by the custom logic block
- DSM (delta-sigma modulator) improves the resolution by dithering (17→10 bits)

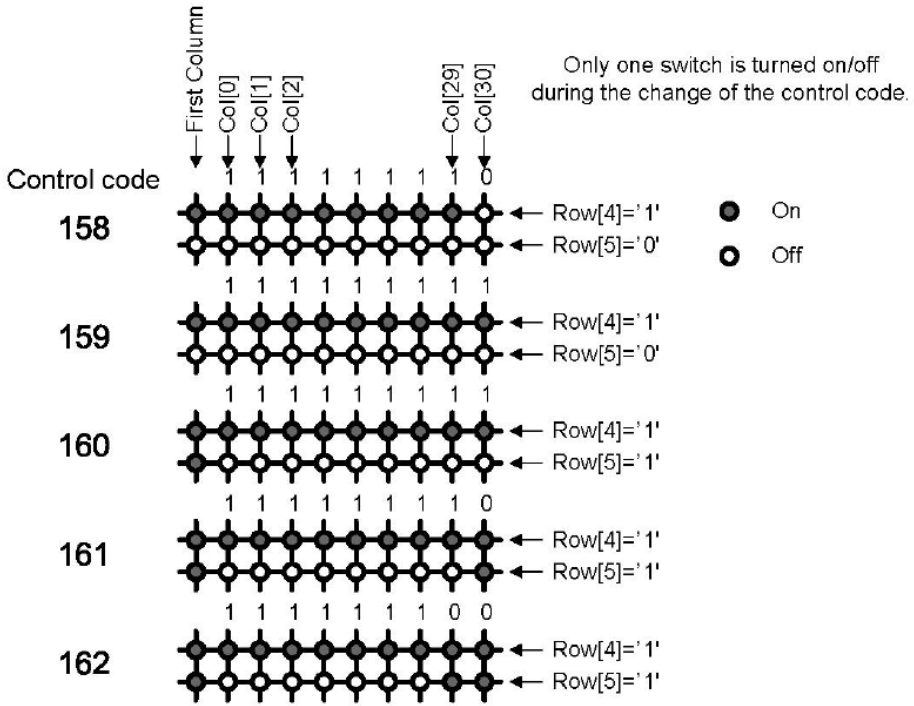
D. -H. Oh, D. -S. Kim, S. Kim, D. -K. Jeong and W. Kim, "A 2.8Gb/s All-Digital CDR with a 10b Monotonic DCO," 2007 IEEE International Solid-State Circuits Conference. Digest of Technical Papers, 2007, pp. 222-598

ISSCC 2007: All-Digital CDR with a 10-bit Monotonic DCO



- DCO is a ring oscillator with the supply connected through a digitally controlled resistor
- Resistor is made up of 1024 PMOS transistor switches that control the DCO frequency
- A segmented thermometer (32 rows & 31 columns) control is used for switching to prevent glitches during the code transitions
  - Full thermometer would require 1024 control line
- The DCO tuning steps (fstep=f_{n+1}/f_n) should be constant to maintain the same loop stability, bandwidth across different data rates
- Equally spaced tuning steps mean that the frequency increases exponentially → not easy to achieve
- PMOS transistors are inserted between the rows to produces an overall resistance change close to an exponential, frequency can be tuned exponentially

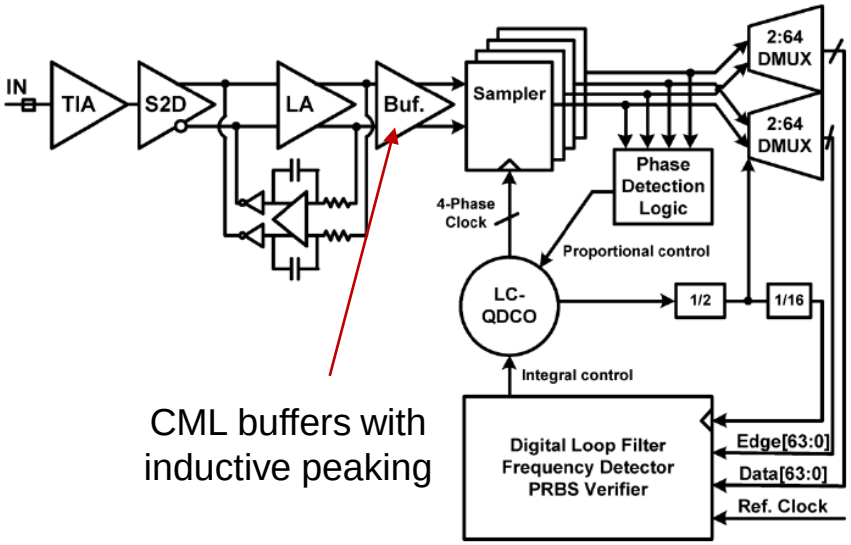
ISSCC 2007: All-Digital CDR with a 10-bit Monotonic DCO



- A cell in an **even** row is turned on when the corresponding column **code is 1** and a cell in an **odd** row is turned on when the corresponding column **code is 0**
- A cell in the **first column** is turned on when the corresponding row **code is 1**
- DCO has 16 tuning cells for the 2-b forward path that receive the proportional path UP/DN signal

JSSC 2015: 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery

- Optical front-end consists of TIA, a single-to-differential converter (S2D), an limiting amplifier (LA) with DC offset cancellation
- Output buffers are necessary to drive the large capacitive load of the samplers
- CDR employs a half rate architecture with 2 data and 2 edge samplers (4-phase clock) for phase detection

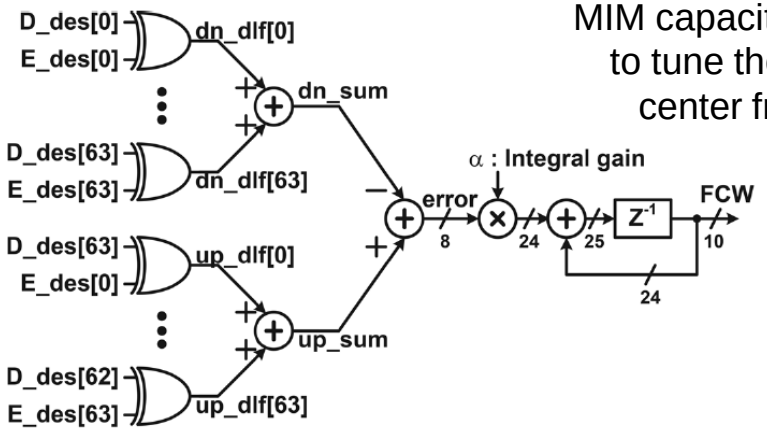


CML buffers with inductive peaking

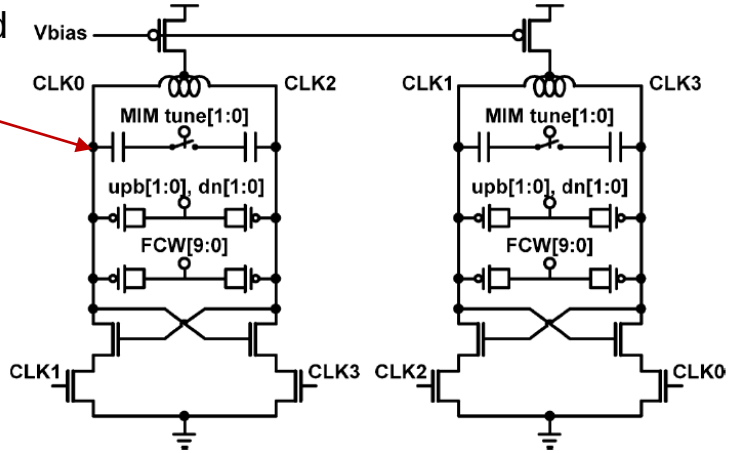
- This is followed by a 2 to 64 bit de-multiplexers that generate the 64-bit parallel data and edge information Data[63:0] & Edge[63:0]
- The proportional high speed pulses are feed directly to the LC-QDCO (quadrature digitally controlled oscillator)
- The integral path is implemented using a low speed ($F_b/64$) 64-bit parallel digital phase detector & loop filter
- Frequency detection is also done in the digital

S. -H. Chu et al., "A 22 to 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery in a 65 nm CMOS Process," in IEEE Journal of Solid-State Circuits, vol. 50, no. 11, pp. 2603-2612, Nov. 2015.

JSSC 2015: 26.5 Gb/s Optical Receiver With All-Digital Clock and Data Recovery

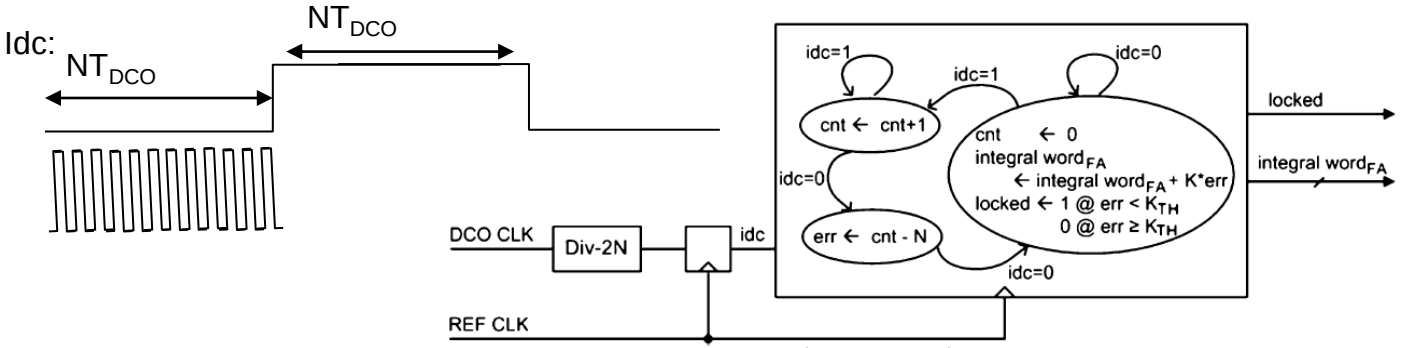


MIM capacitors are used to tune the oscillator center frequency



- The DLF XOR incoming demultiplexed data and edge samples to generate the up/down signals
- The integral path control is generated by a 24 bit integrator (which replaces the large analog loop filter) → Integral path gain is determined digitally by the integral gain α
- Upper 10 bit of the 24 bit integrated error are used for the frequency control word FCW[9:0]
- 2 coupled symmetrical LC oscillators are used to generate the quadrature half-rate clocks with proportional/integral varactor banks to tune the DCO frequency
- To eliminate glitches 8 MSBs of the 10 bit FCW as 4 bit row and 4 bit column codes and these are converted to two 15 bit thermometer codes, which represent a 30 bit coarse-tuning code
- The two LSBs of the FCW are for fine-tuning the LC-QDCO code
- The proportional varactor bank consists of binary weighted PMOS capacitors (selectively activated for the proportional gain control)

JSSC 2011: All-Digital CDR With 1.0-ps Period Resolution DCO and Adaptive Proportional Gain



$$err = N\left(\frac{f_{ref}}{f_{DCO}} - 1\right) + a \quad \ldots \quad (-2 < a > 2)$$

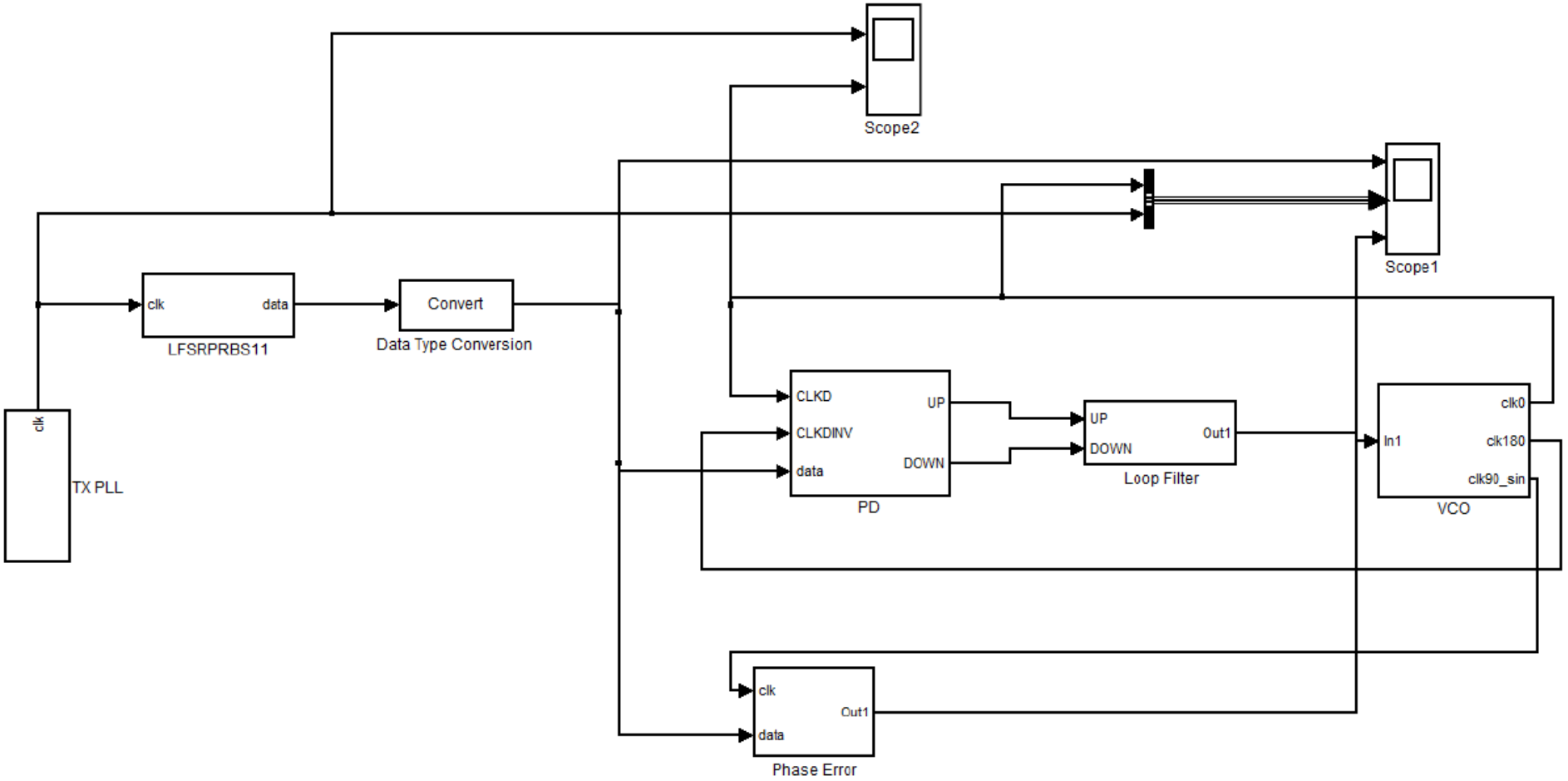
- Frequency acquisition can be performed using a FSM with a digital frequency comparator
- The number of rising reference clock edges are counted during "N" DCO output clocks and subtracting this value from N
- The FSM runs using f_{ref}, and the enable/disable signal is generated via f_{DCO}
- The result is equal to the product of the frequency error and N
- The integral word is changed by an amount proportional to the measured frequency error
- Once the measured frequency error has declined below a predetermined value, the integral word is then controlled by the DLF
- of the main phase-locking loop

H. Song, D. -S. Kim, D. -H. Oh, S. Kim and D. -K. Jeong, "A 1.0–4.0-Gb/s All-Digital CDR With 1.0-ps Period Resolution DCO and Adaptive Proportional Gain Control," in IEEE Journal of Solid-State Circuits, vol. 46, no. 2, pp. 424-434, Feb. 2011.

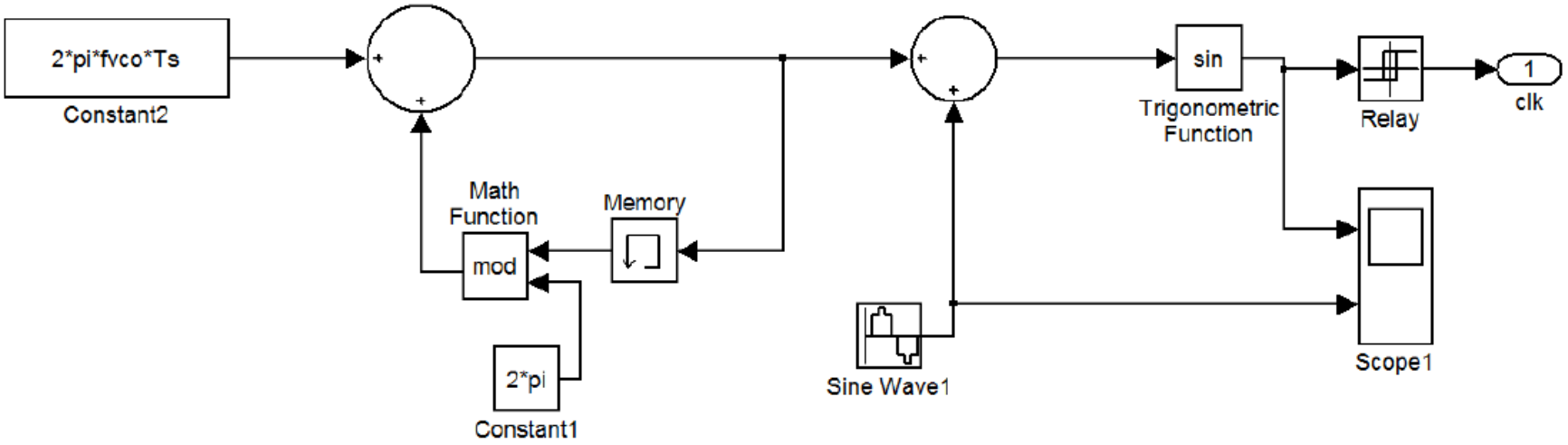
CDR SIMULINK DESIGN EXAMPLE:

FULL RATE ALEXANDER PD BASED CDR WITH ANALOG CP/LOOP FILTER

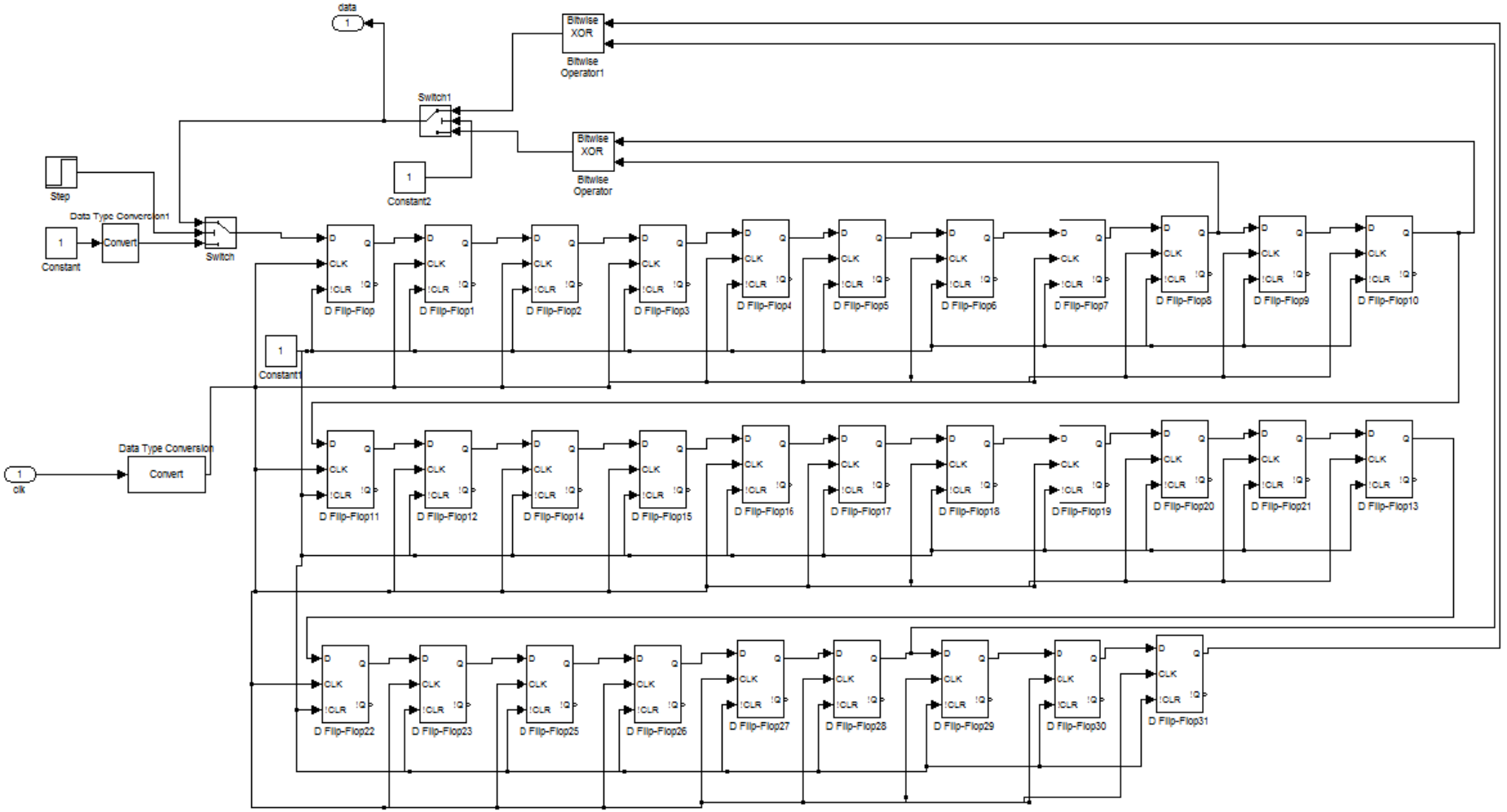
Block Diagram of CDR with PRBS Generator



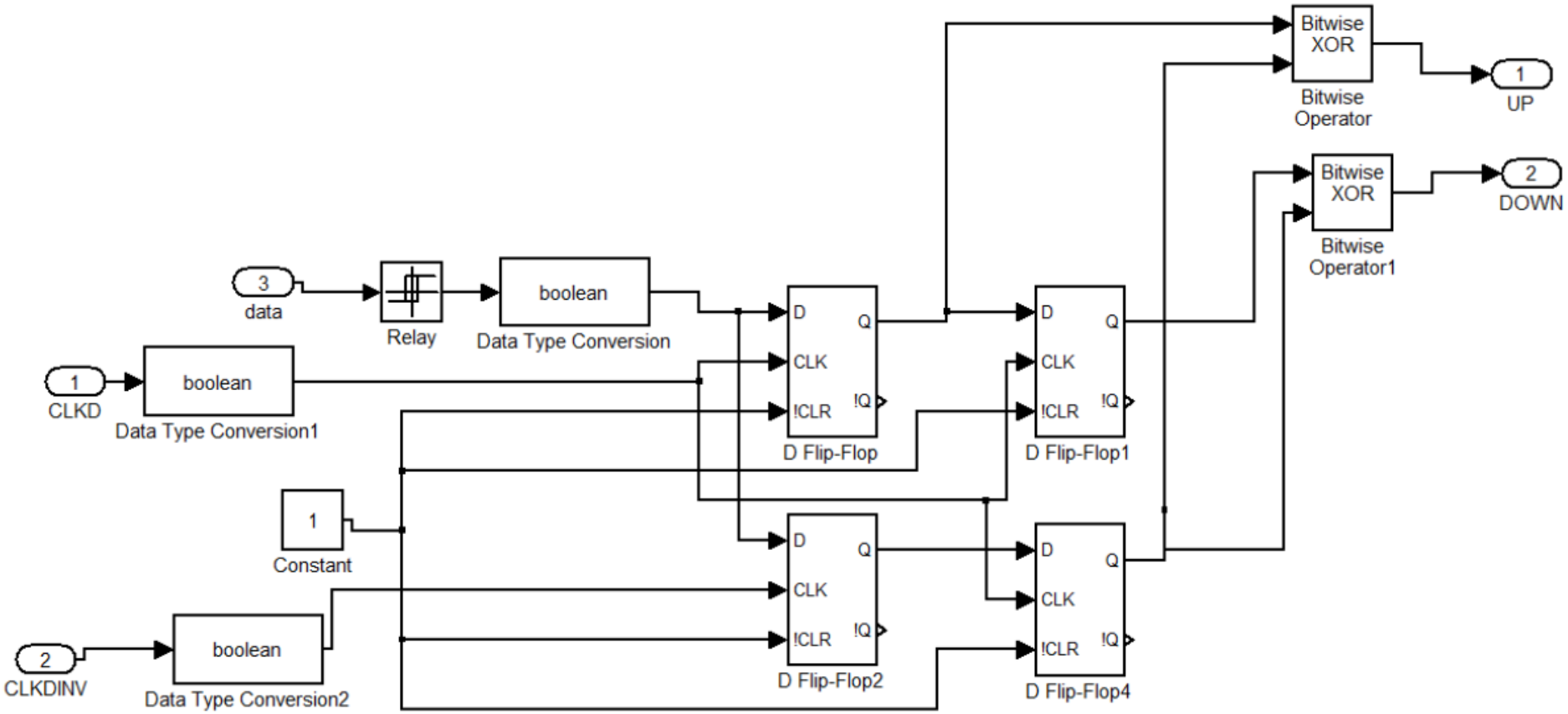
Tx CLK Model with Sinusoidal Jitter



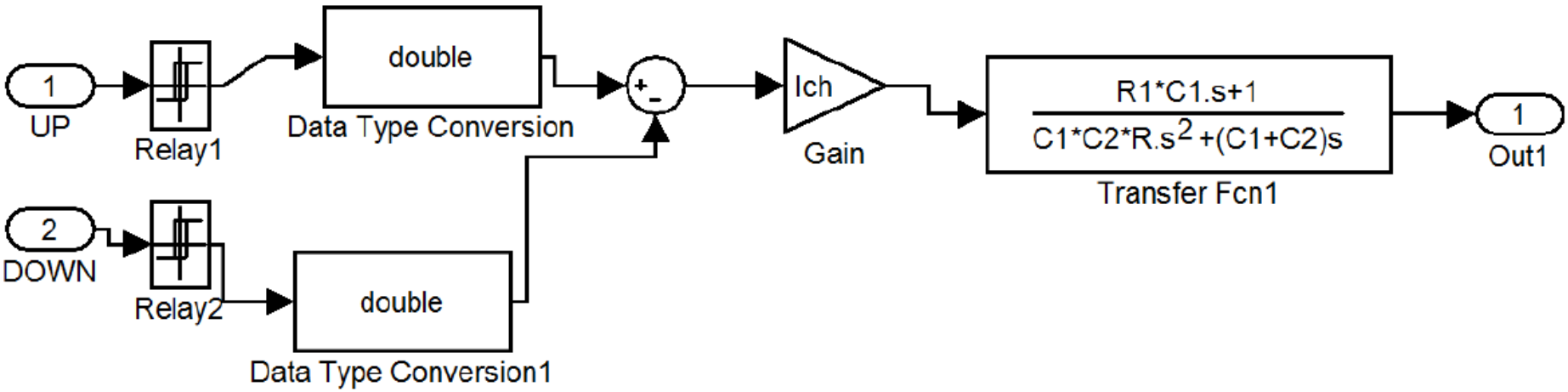
PRBS Generator



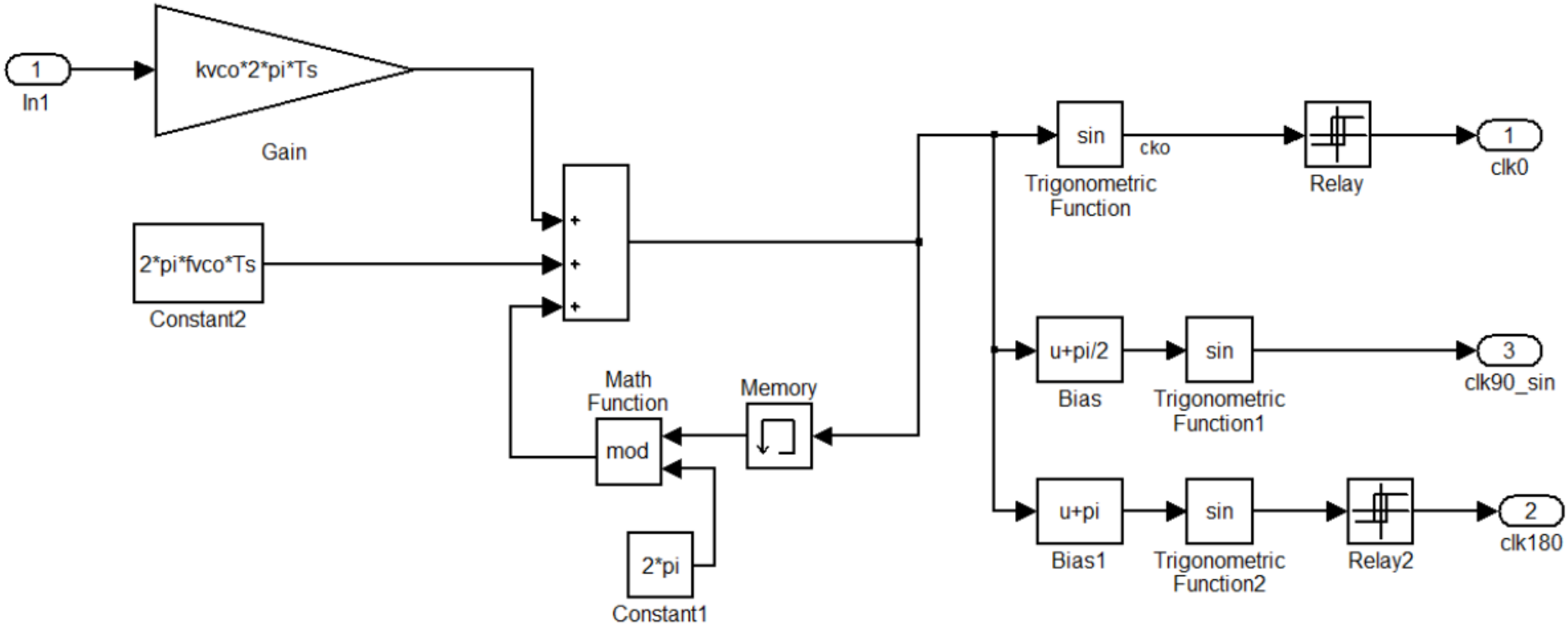
Phase Detector



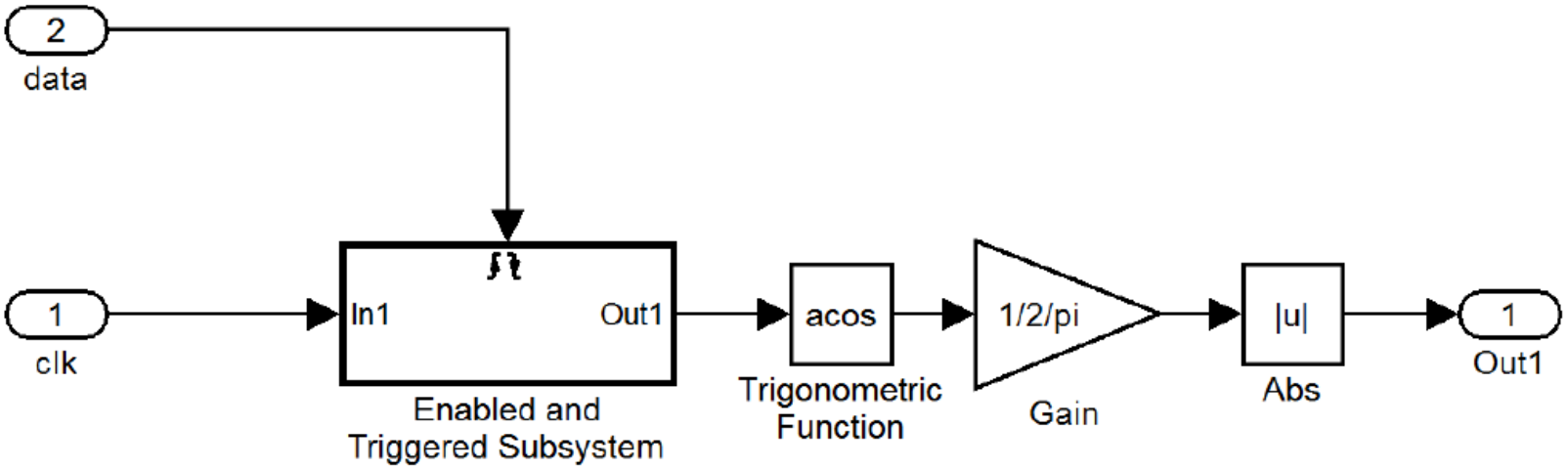
Loop Filter Model



CDR VCO Model



Phase Error Calculation Block



Simulation Results