ECE 621
Signaling & Synchronization
Fall 2020

Topic 3
TX Circuitry

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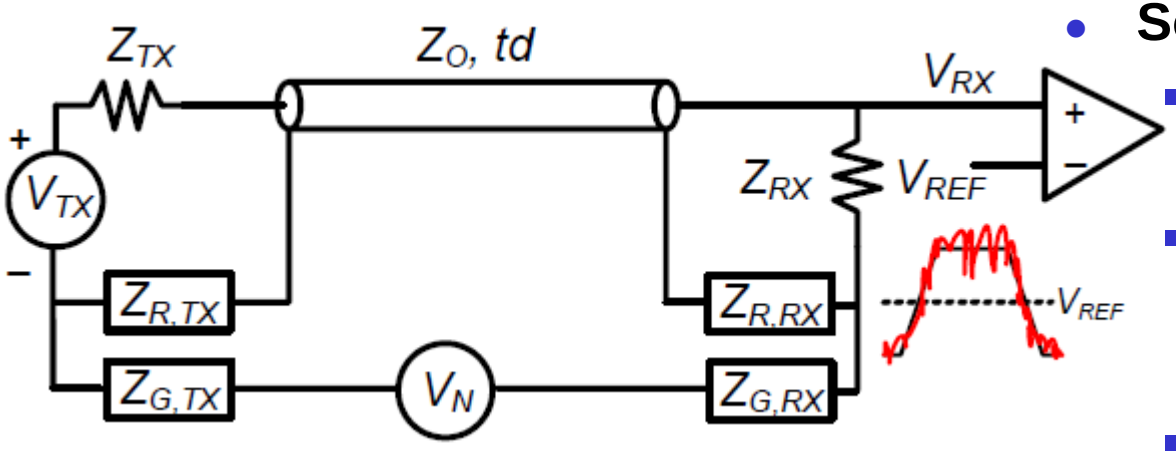
ICL

(Courtesy of S. Pamarti – UCLA, S. Palermo – TAMU, and E. Alon – UCB)

Outline

- **Signaling Basics**
  - Single-ended vs. differential
  - Voltage-mode vs. current-mode
- **Termination Circuits**
  - On-Chip vs. off-chip
  - AC vs. DC coupled
  - Active vs. passive
- **TX Driver Circuits**
  - Large swing drivers
  - Small swing drivers
  - Pre-drivers
- **Multiplexing**
  - Multiplexing depth
  - Multiplexing circuits

Single-Ended Signaling

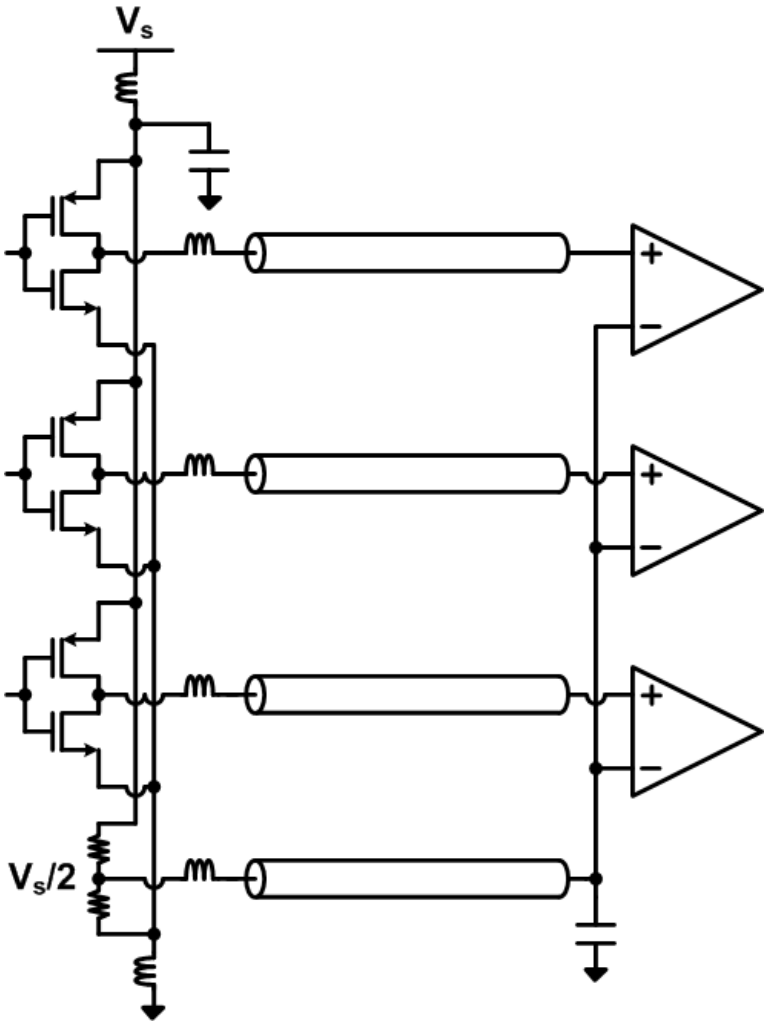


- **Sources of signal corruption**
  - Return-path impedances, $Z_{R,TX}$ and $Z_{R,RX}$
  - Supply coupling impedances, $Z_{G,TX}$ and $Z_{G,RX}$
  - Supply mismatch and noise, V_N

- **Clean reference (V_{REF}) generation is very difficult**
  - Tx and Rx grounds could be different.
  - The difference, V_N, has a significant high frequency content because of supply noise generated by high speed switching.
- **We can use an additional line to send the reference signal**
  - Matching becomes a problem.

SE Signaling for Multiple Links

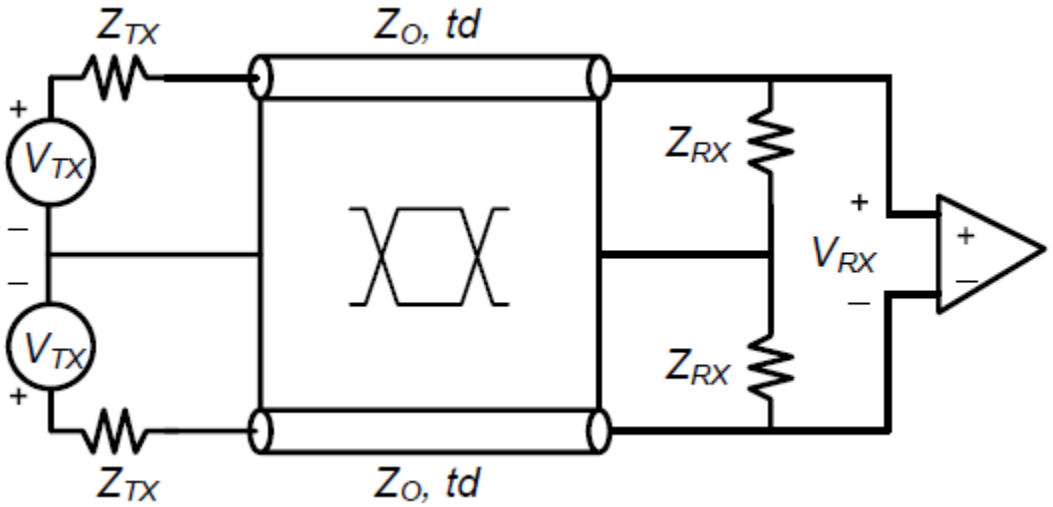
- **Finite supply impedance causes significant Simultaneous Switching Output (SSO) noise.**
  - Imagine many TXs switching at the same time
- **Necessitates large amounts of decoupling capacitance for supplies and reference voltage**
  - Decap limits I/O area more than circuitry
- **Is it still used? Why?**



Classic Debate

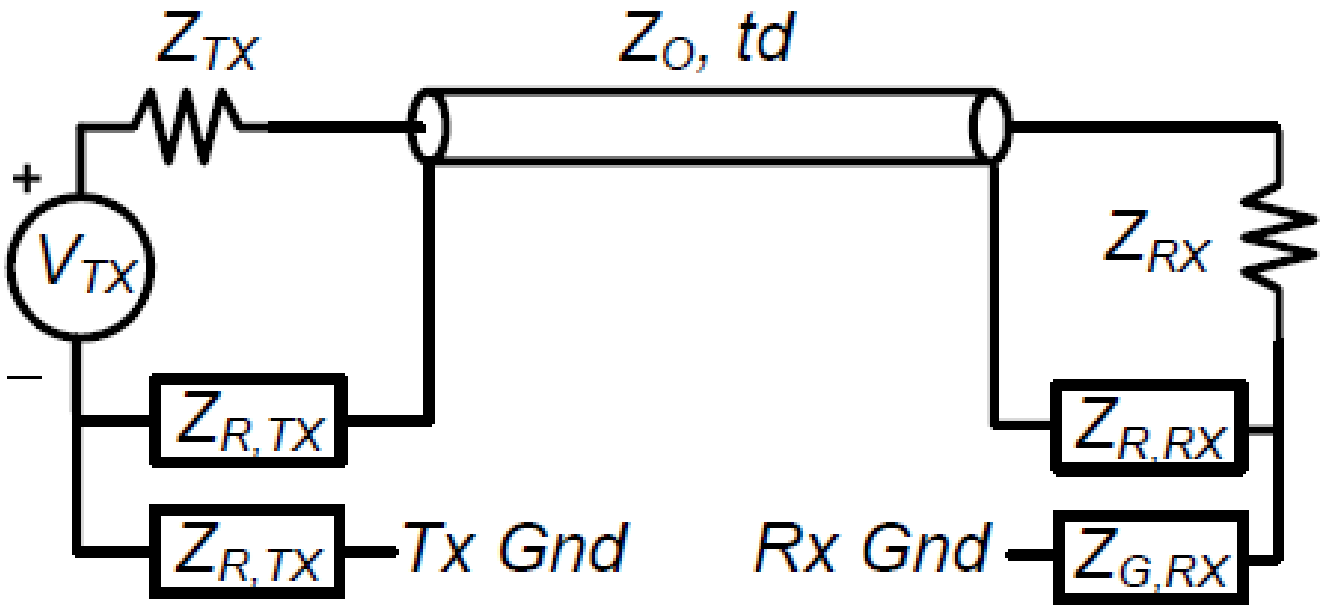
- **Area constraints mandates single ended.**
- **“Differential must be twice as fast as single ended in order to win”**
- **Reality more complicated**
  - Ex: SSO mandates the use of more ground and supply pins for SE
  - i.e. higher supply to signaling pin ratio in SE
- **Differential is a lot easier to build and get right the first time.**
- **SE can be built to work but needs more care and is more painful.**
- **Differential links can possibly save power.**

Differential Signaling



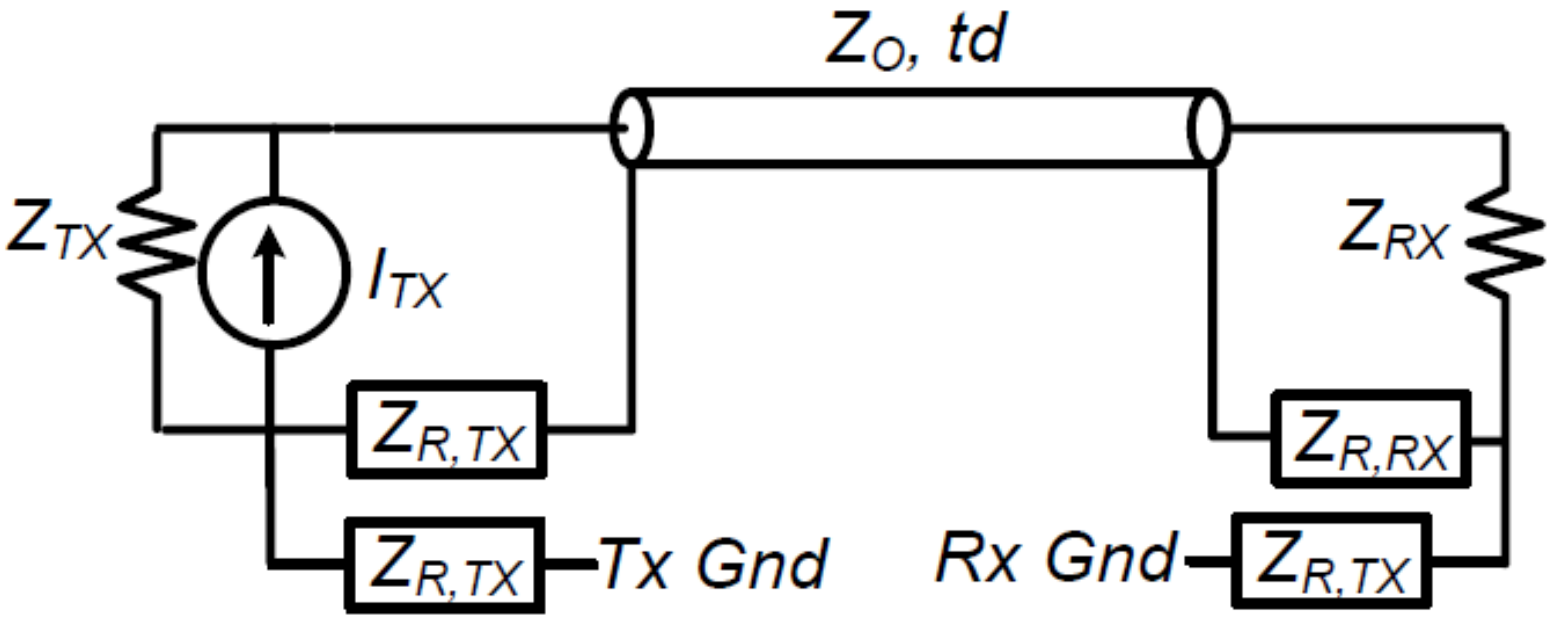
- Use of two transmission lines per I/O link
- No reference voltage is used to extract data. ☺
- Swing is twice as large as SE signaling. ☺
- No return path corruption ☺
- Minimum self-induced power supply noise ☺
- Matching between lines is crucial ☹
- Low pin/wire utilization is becoming a problem. ☹

Voltage-Mode Signaling



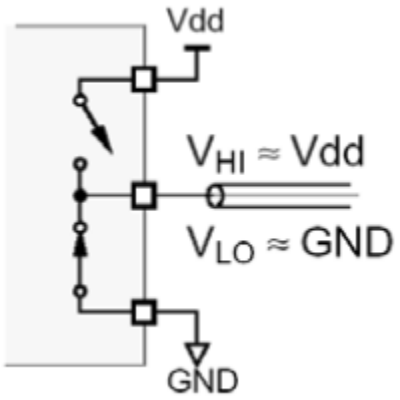
- **Output Impedance is low.**
- **Older systems used $Z_{TX} << Z_o$.**
- **Newer Systems use $Z_{TX} = Z_o$ to minimize reflections.**
- **Thevenin-equivalent series termination**

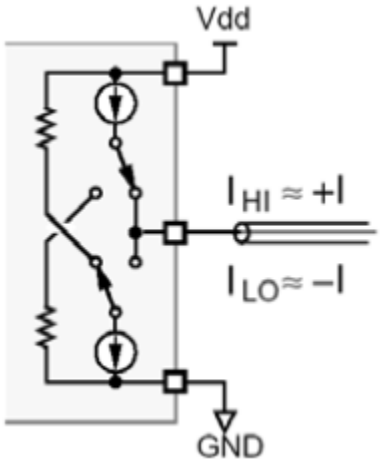
Current-Mode Signaling

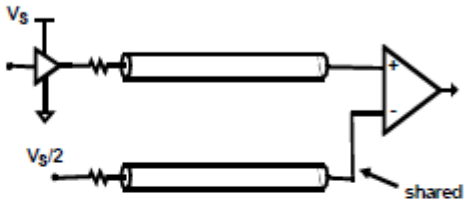
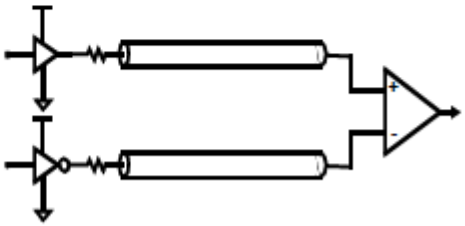
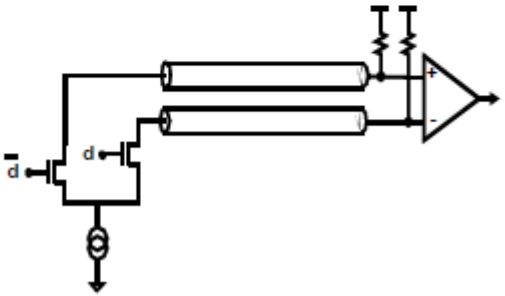


- **Output Impedance is high.**
- **Older systems used $Z_{TX} >> Z_o$.**
- **Newer Systems use $Z_{TX} = Z_o$ to minimize reflections.**
- **Norton-equivalent parallel termination**

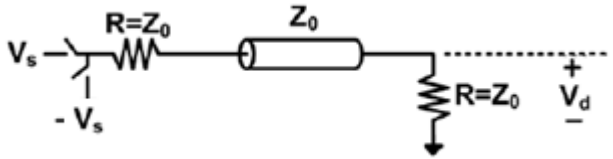
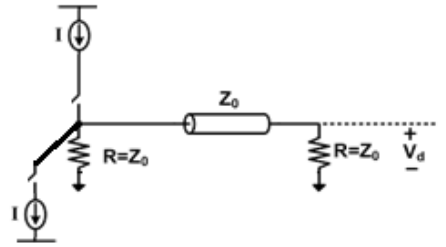
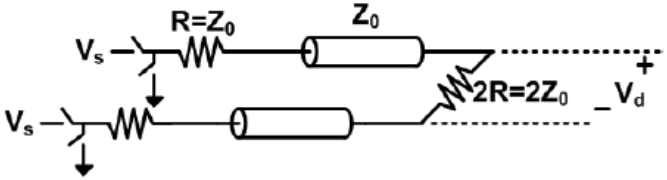
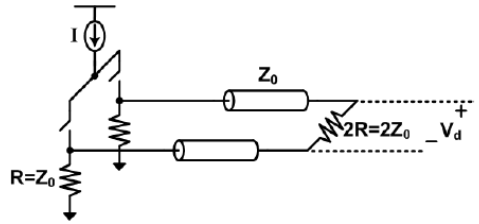
Old "Voltage-Mode" vs. "Current-Mode"





	"Low Impedance"	*"High Impedance"*
Single Ended		
Differential		

Gb/s "Voltage-Mode" vs. "Current-Mode"

	Voltage-Mode	Current-Mode
Single-Ended	 $V_{d,1} = (V_s/2)$ $V_{d,0} = -(V_s/2)$ $V_{d,pp} = V_s$ $I = (V_s/2R)$ $\boldsymbol{I = \frac{V_{d,pp}}{2R}}$	 $V_{d,1} = (I/2)R$ $V_{d,0} = -(I/2)R$ $V_{d,pp} = IR$ $\boldsymbol{I = \frac{V_{d,pp}}{R}}$
Differential	 $V_{d,1} = (V_s/2)$ $V_{d,0} = -(V_s/2)$ $V_{d,pp} = V_s$ $I = (V_s/4R)$ $\boldsymbol{I = \frac{V_{d,pp}}{4R}}$	 $V_{d,1} = (I/4)(2R)$ $V_{d,0} = -(I/4)(2R)$ $V_{d,pp} = IR$ $\boldsymbol{I = \frac{V_{d,pp}}{R}}$

Voltage-Mode vs. Current-Mode Summary

Driver/Termination	Current Level	Normalized Current Level
Current-Mode/SE	$V_{d,pp}/Z_0$	1x
Current-Mode/Diff	$V_{d,pp}/Z_0$	1x
Voltage-Mode/SE	$V_{d,pp}/2Z_0$	0.5x
Voltage-Mode/Diff	$V_{d,pp}/4Z_0$	0.25x

- **An ideal voltage-mode driver with differential RX termination enables a potential 4x reduction in driver power.**
- **Finally, since TL has both voltage and current, terminology can mean**
  - Whether or not the termination is high
  - How termination is set
  - What sets the output swing (supply or current source)

Outline

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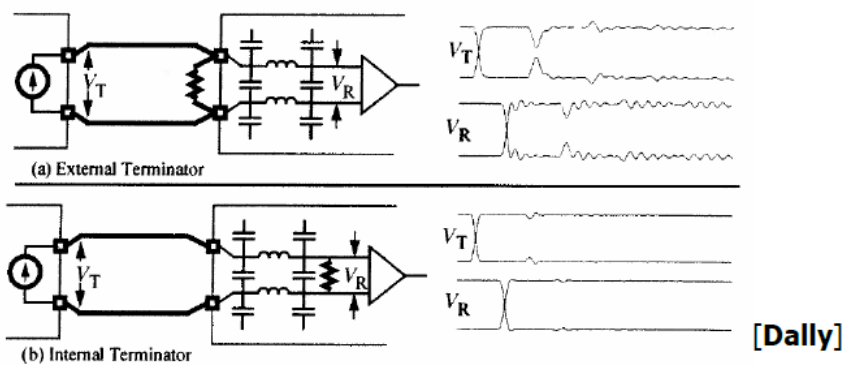
On-Chip vs. Off-Chip Termination



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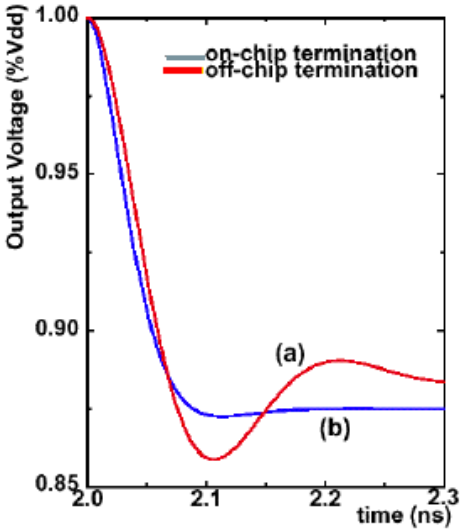
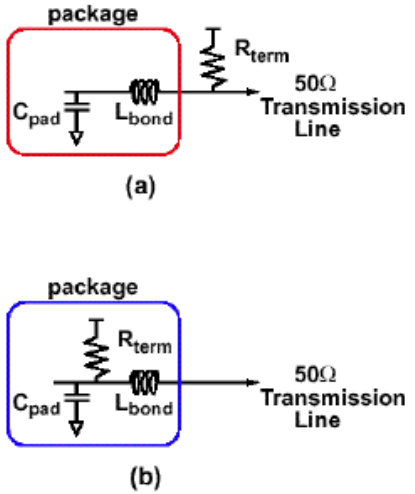
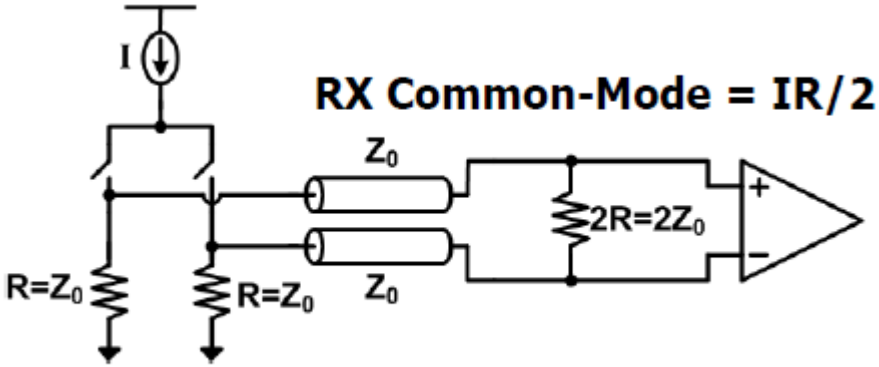




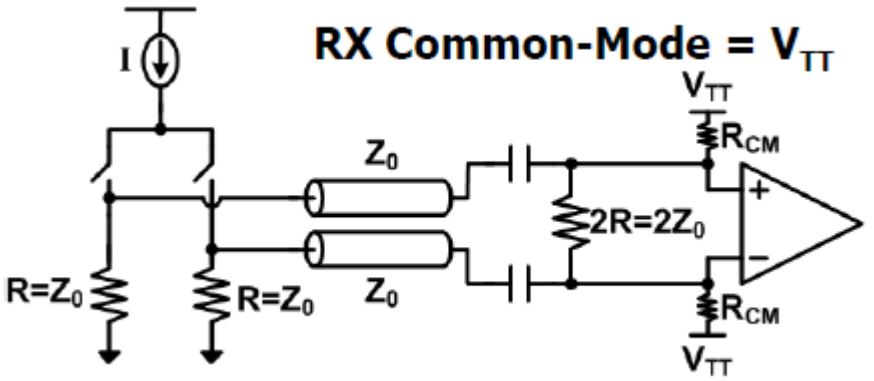
- **Package parasitics act as an unterminated stub which sends reflections back onto the line.**
- **On-chip termination makes package inductance part of transmission line.**
- **But on-chip termination needs control.**

AC vs. DC-Coupled Termination

- DC coupling allows for uncoded data.
- RX common-mode set by transmitter signal level.



- AC coupling allows for independent RX common-mode level.
- Data must be coded because of channel's low frequency cut-off.



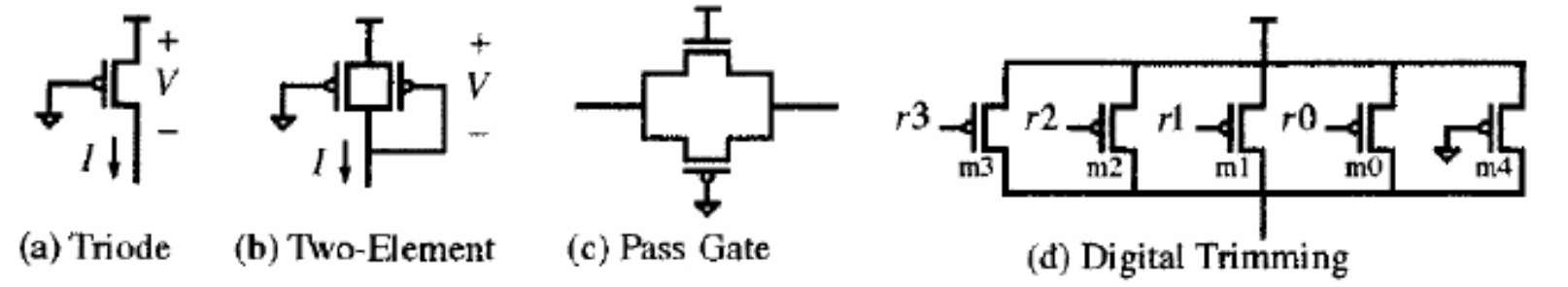
Passive Termination

- **Choice of integrated resistors involves trade-offs in manufacturing steps, sheet resistance, parasitic capacitance, linearity, and ESD tolerance.**
- **Integrated passive termination resistors are typically realized with unsilicided poly, diffusion, or n-well resistors.**
- **Poly resistors are typically used due to better linearity, but they typically vary +/-30% over process and temperature.**

Resistor Options (90nm CMOS)

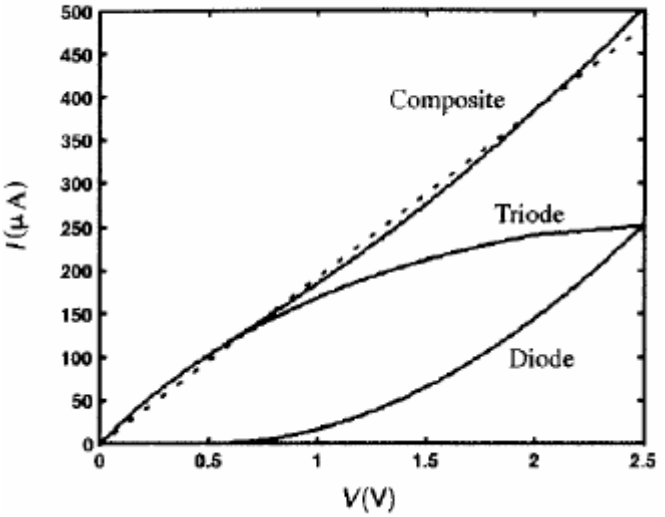
Resistor	Poly	N-diffusion	N-well
Sheet R (Ω/sq)	90±10	300±50	450±200
VC1(V^{-1})	0	10^{-3}	$8x10^{-3}$
Parasitic Cap	2-3fF/um^2 (min L poly)	0.9fF/um^2 (area), 0.04fF/um (perimeter)	0.2fF/um^2 (area), 0.7fF/um (perimeter)

Active Termination



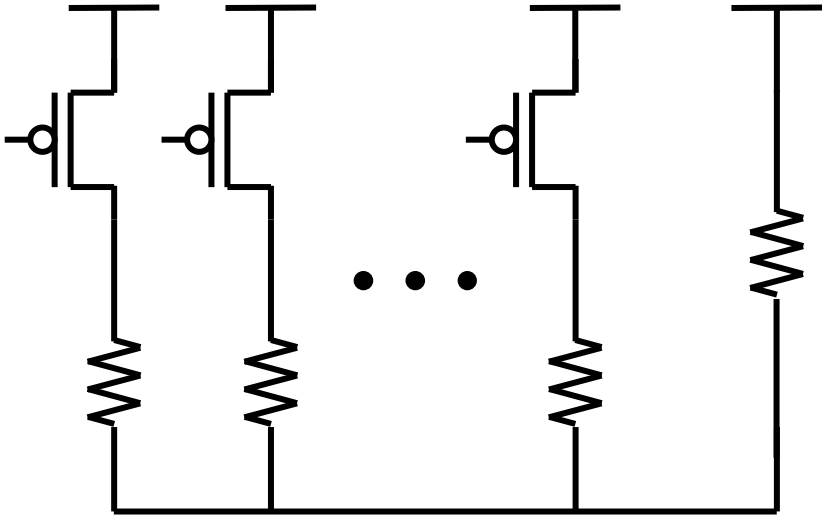
- **Transistors must be used for termination in CMOS processes with no resistors.**
- **Triode-based FET works well for low-swing (<500 mV)**
  - Adding a diode-connected FET increases linear range.

[Dally]



- **Pass-gate structure allows for differential termination.**
- **Not ESD robust, needs adjustment loop (Analog or Digital), and adds extra capacitance.**

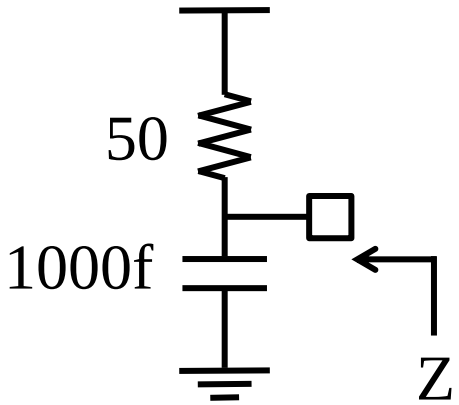
Combination of Active and Passive

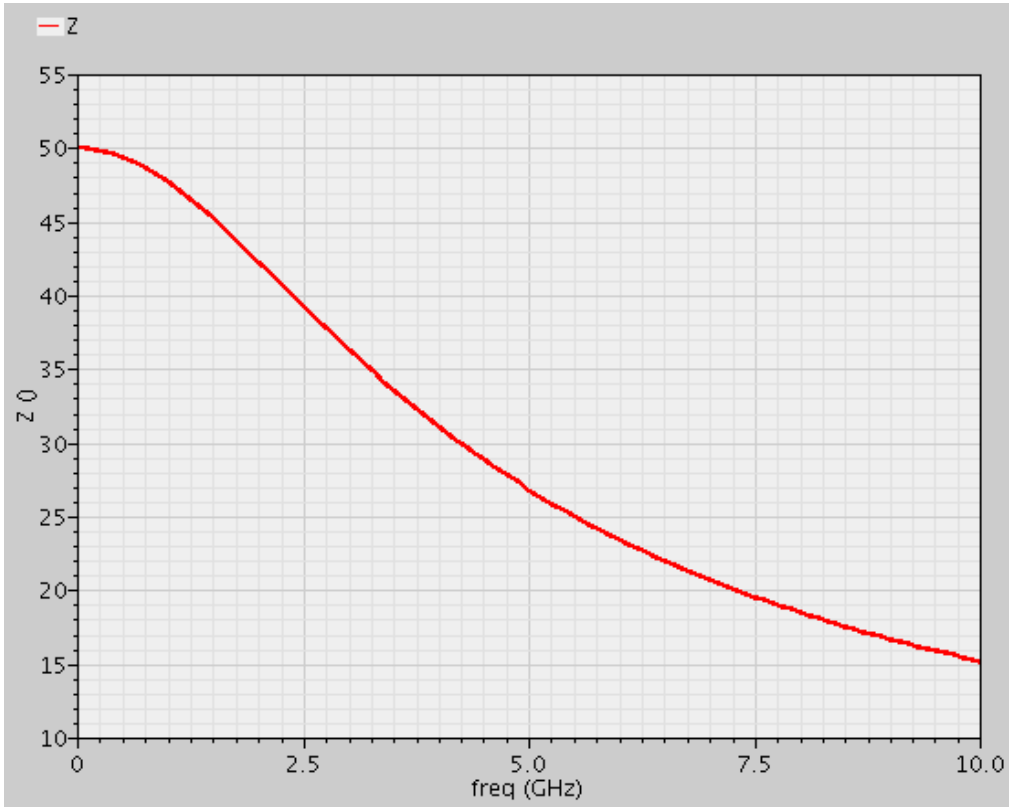


- **Fixed resistor and digitally-controlled resistor to account for variations**
- **Better ESD robustness and linearity**
- **Device capacitances are partially shielded.**
- **But adjustment loop is still required.**

Termination Capacitance

- **Many parasitic caps: ~500 fF ESD and pads and ~500 fF driver.**
- **This gives a BW of ~ 6 GHz for double-terminated links.**



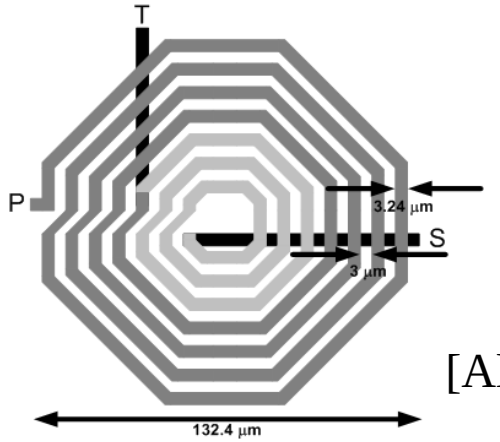


T-Coils

- **Old technology recently used in bandwidth extension and ESD capacitance compensation.**

[Schmatz JSSC Dec. 2008]

- **T-coil consists of two mutually coupled inductor and a bridged capacitor.**



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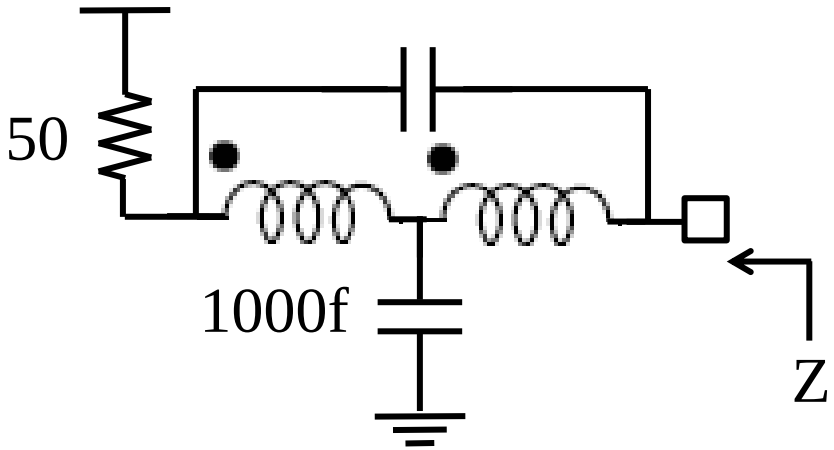
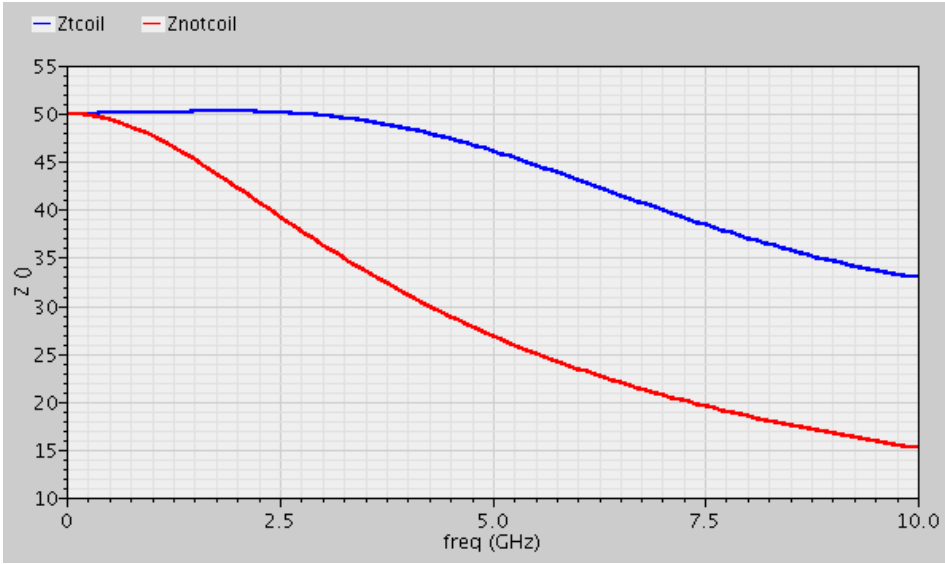
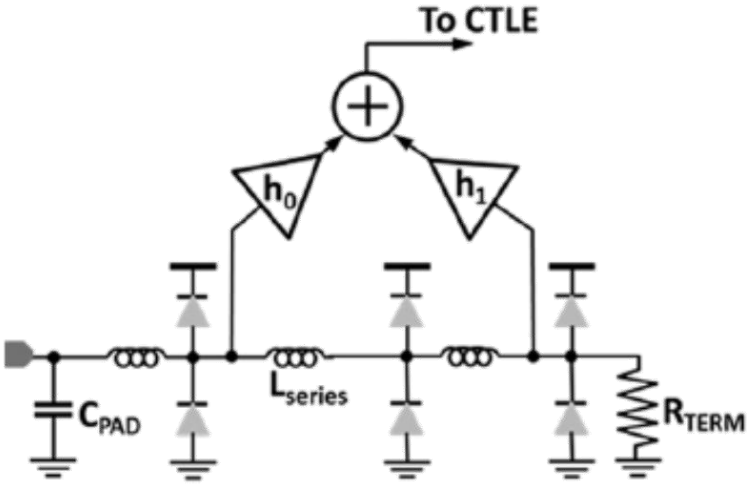
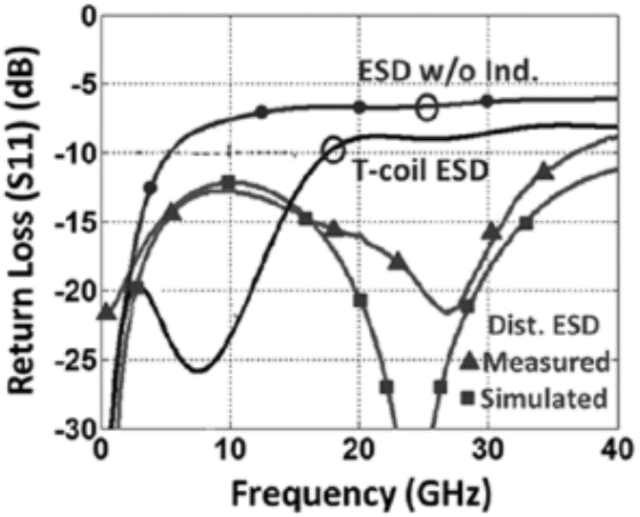




Distributed ESD

- At higher data rates (ex 40 Gb/s), even T-coil Extension is not enough.
- Distributed ESD is a possible solution.
- More on-chip inductors are used but with smaller values.
- Delay through transmission line sections can help implement equalizers at RX side.
- Impedance of inductors at ESD events is negligible (low-frequency events).





[Navid, JSSC Apr. 2015]

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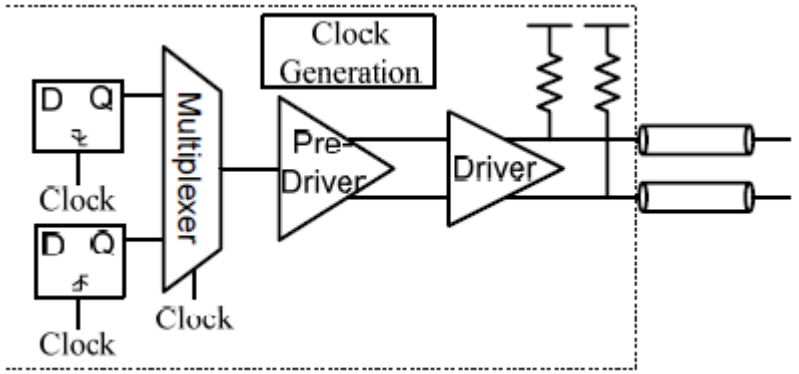
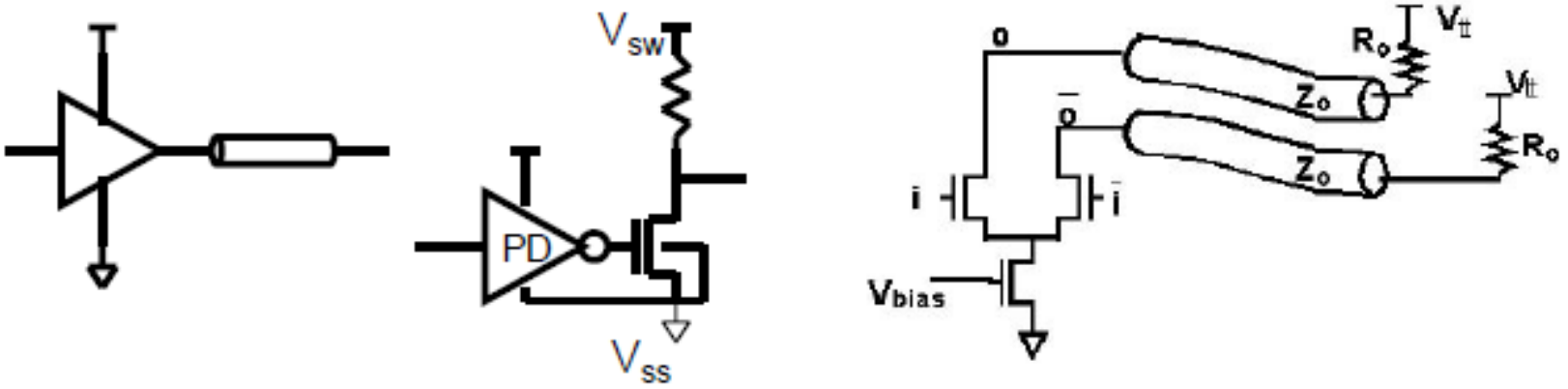
Conceptual I/O Transmitter

- **Multiplexers and Synchronizers**
  - To facilitate data exchange between sources and the link
- **Driver**
  - Generates signals suitable for signaling
- **Pre-driver**
  - Condition the driver e.g., level shifting etc.



- **Goals**
  - High bit rate
  - Low power consumption
  - Low noise, free of unnecessary time-domain spikes
  - Low coupling to other links

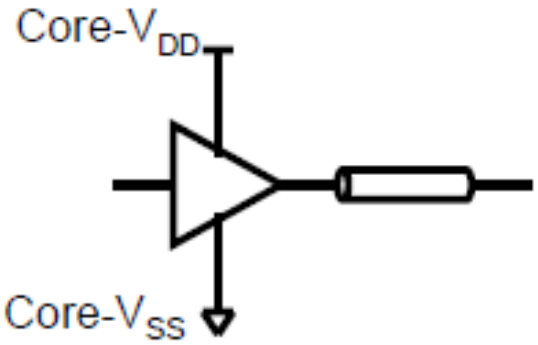
Main Driver Circuit Choices



- **Single Ended or Differential**
- **Voltage mode or current mode**
- **On-chip or off-chip supplies**
- **Source termination**

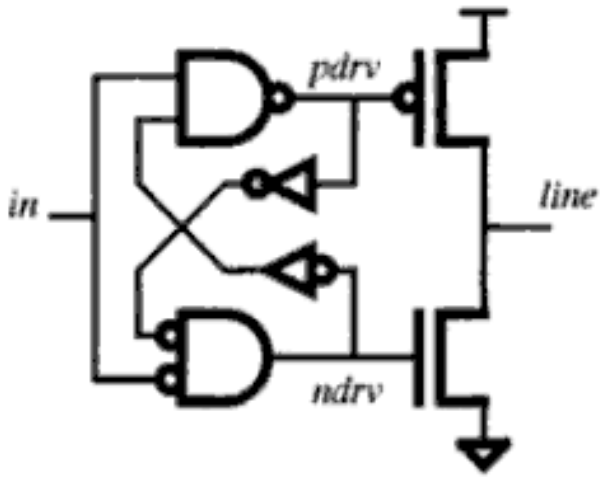
- **Each choice has an implication on signal fidelity, power consumption, noise coupling, and data rate.**

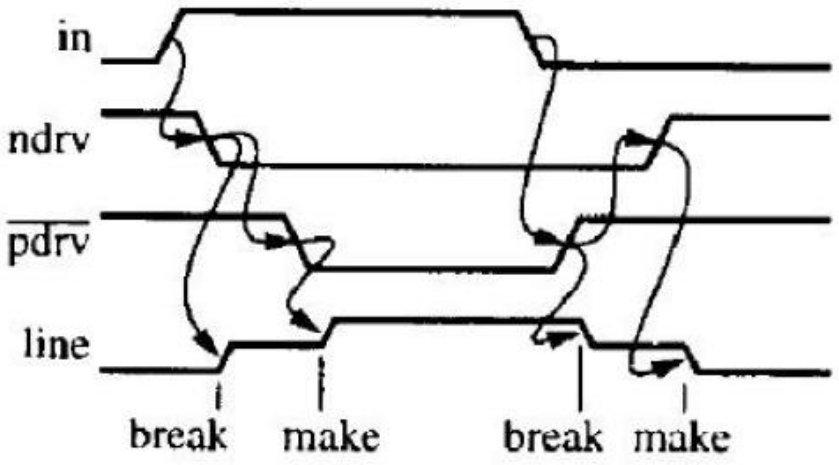
A Very Simple Large Swing Driver



- **Characteristics**
  - Push-pull architecture
  - Large signal amplitude, $V_{swing} = V_{DD}$
- **Supply noise contribution is very large.**
  - V_{DD} on chip can be very noisy
- **Reflections are significant due to lack of source termination**
- **Large crowbar current**
  - Causes significant power consumption

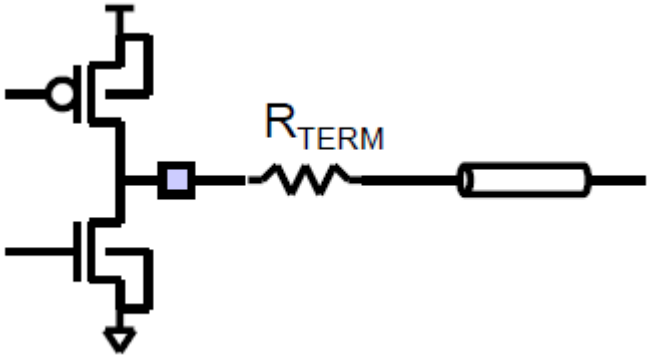
Another Simple Large Swing Driver





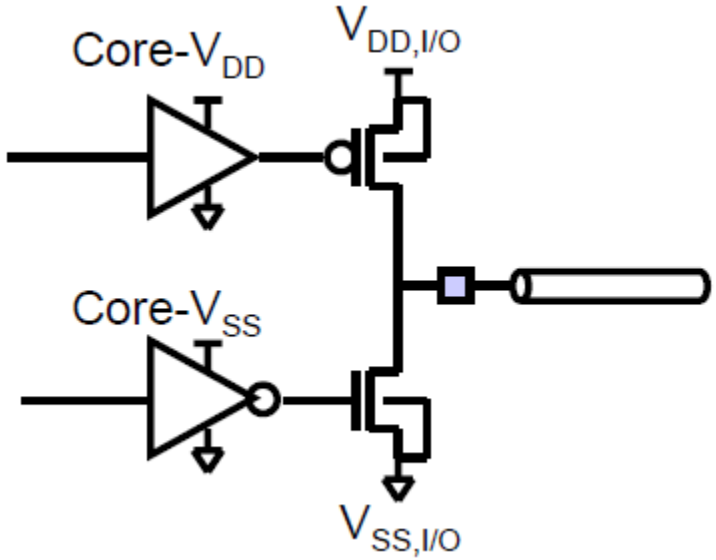
- **Break-before-make connection**
  - Ensures that NMOS and PMOS are not simultaneously ON, even for short duration
- **Supply noise, reflection problems remain**
- **These are mainly legacy I/Os**
  - Good for low data rate, generic interfaces with other ICs

Source Terminated Large Swing Driver



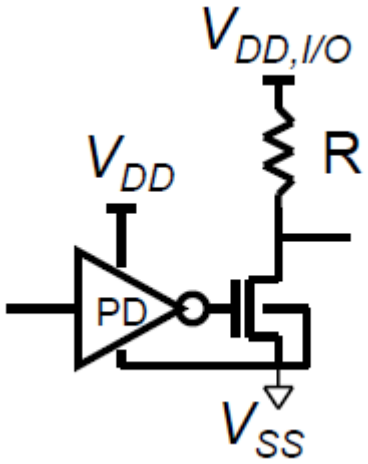
- **Add a resistance in series to provide source termination.**
  - Prevents some reflection
- **Actual source impedance is a series combination of R_{TERM} and Z_{NMOS} or Z_{PMOS}.**
  - Increase NMOS and PMOS sizes to maintain switching speed performance.
- **Difficult to terminate precisely**
  - Transistor impedance varies with region of operation and PVT corners.

Dedicated Driver Supplies



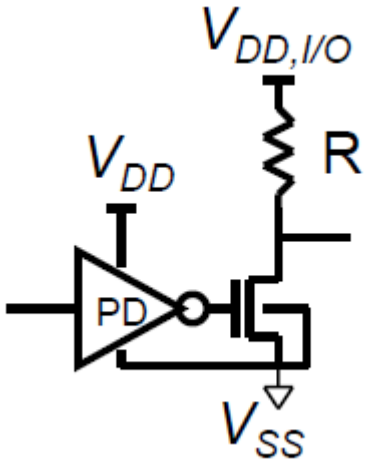
- **V_{SWING} = $V_{DD,I/O}$ > Core-V_{DD} is possible.**
  - I/O signals are better protected from noise on core supplies.
- **The driver supplies could be on-chip or off-chip.**
- **Large DC driver currents are possible**
  - Depends on relation between Core-V_{DD} and $V_{DD,I/O}$

A Very Simple Low Swing Driver



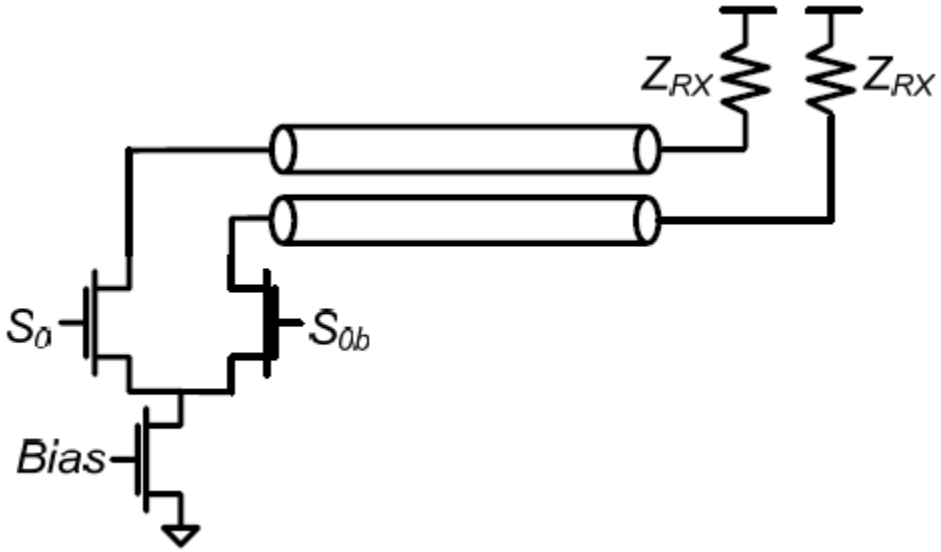
- **Replace the pull-up PMOS with a resistance.**
  - Signal swings between $V_{DD,I/O}$ and $V_{DD,I/O} - I_{DS}R$
- **Pull-up time constant is determined by R.**
  - Small R results in quick pull-up.
- **Received signal is smaller than with large swing drivers.**
  - Threatens receiver margins and could increase BER.
- **More susceptible to variations in R and I_{drv}.**

Why Low Swing Drivers?



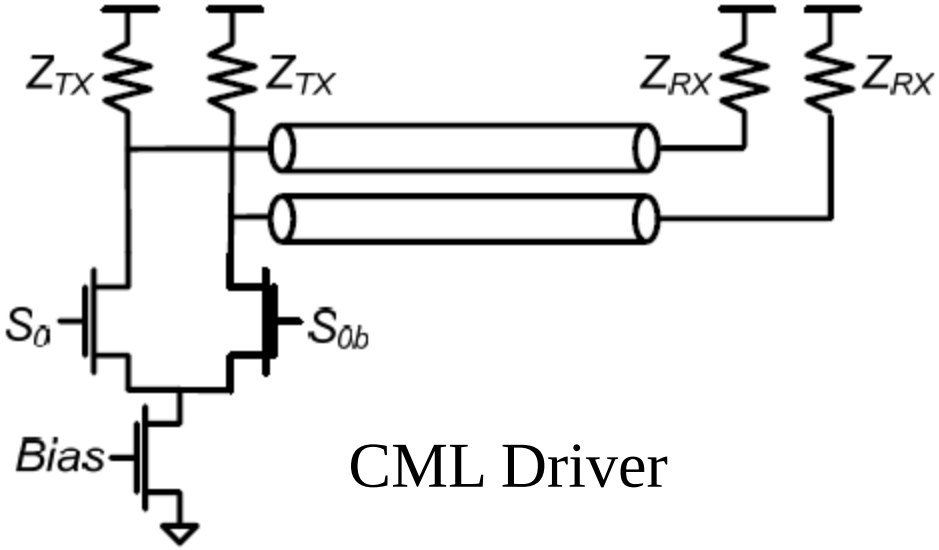
- **Higher speed**
  - Devices switch faster.
  - Smaller devices and hence lower capacitance
- **Better linearity**
  - Driver transistor stays in a single region of operation when ON.
- **Lower power**
  - Power is proportional to swing e.g. $0.5C_LV^2f$

Low Swing Differential Drivers



- **Differential pair steers the current into a differential I/O link.**
- **High output impedance can cause reflection problems on the source side.**
- **Pre-driver works hard**
  - Currents need to be steered completely.

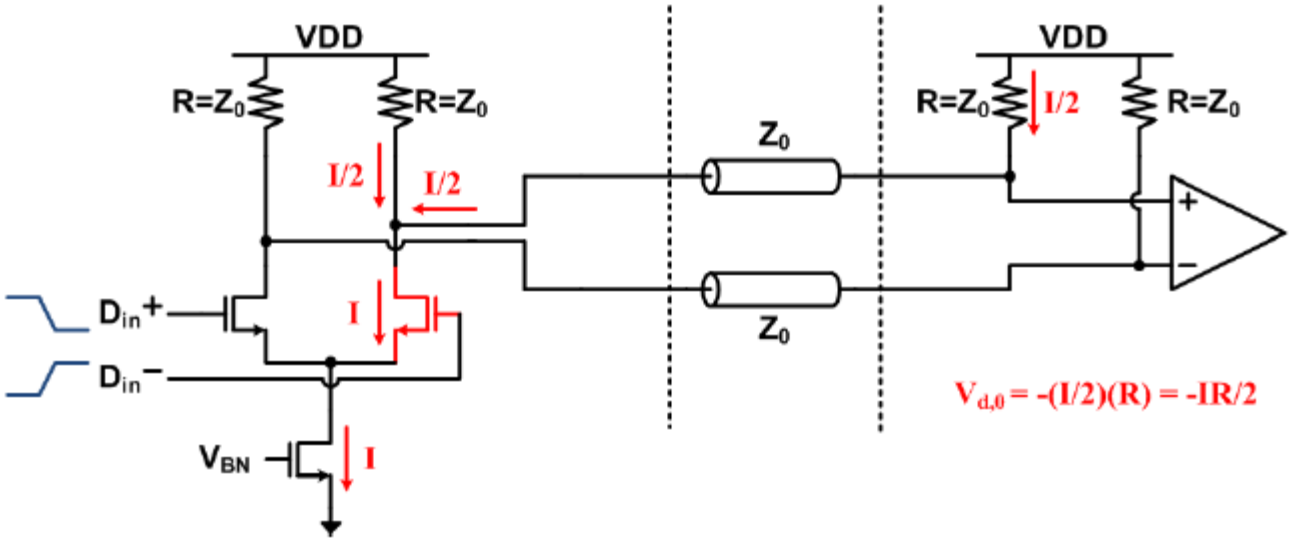
Terminated Low Swing Differential Drivers



CML Driver

- **Z_{TX} are actual termination resistors.**
  - Driver is based on current mode logic. [Mizuno JSSC Jun. 1996]
  - Triode PMOS could be used instead.
  - Additional power consumption
- **Doubly terminated differential signaling is popular among very high speed signaling.**

Current-Mode Logic (CML) Driver



- **Used in most high-performance serial links.**
- **Low voltage operation relative to push-pull driver**
  - High output common-mode keeps current source saturated.
- **Can use DC or AC coupling**
- **Differential pp RX swing is ±IR/2 with double termination**

CML Power Consumption

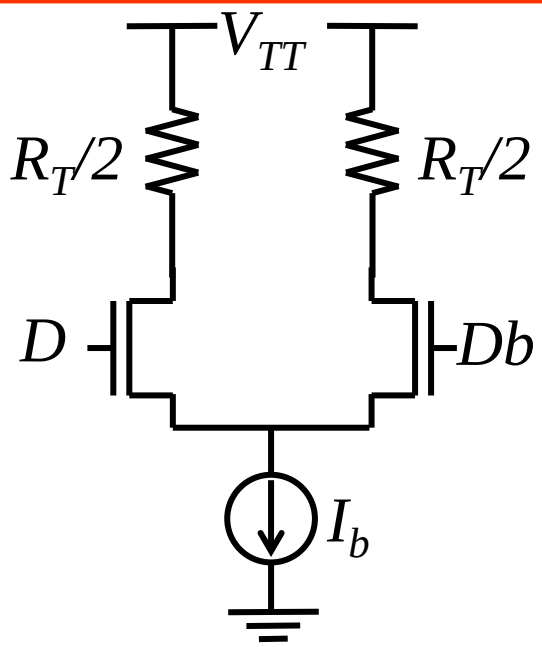
$$P = I_b V_{TT}$$

$$V_{SW,diff} = I_b R_T$$

$$V_{SW,amp} = \frac{I_b R_T}{2}$$

$$I_b = \frac{2V_{SW,amp}}{R_T}$$

$$P = V_{SW,amp} V_{TT} \frac{2}{R_T}$$



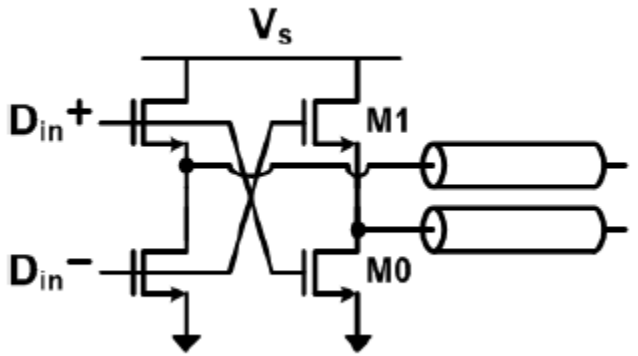
$$V_{TT,min} = 2V_{DSAT} + V_{SW,amp}$$

$$P_{min} = {V_{SW,amp}}^2 \left(1 + \frac{2V_{DSAT}}{V_{SW,amp}}\right) \frac{2}{R_T}$$

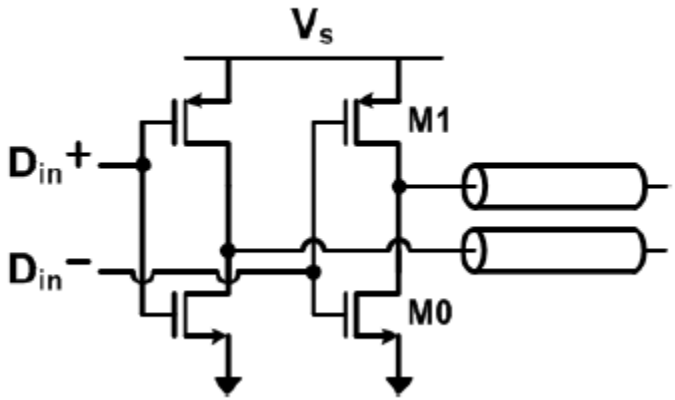
Lower Power Using Voltage-Mode Drivers

- Voltage-mode driver implementation depends on output swing requirements.
- For low-swing (<400-500mVpp), an all NMOS driver is suitable.
- For high-swing, CMOS driver is used.

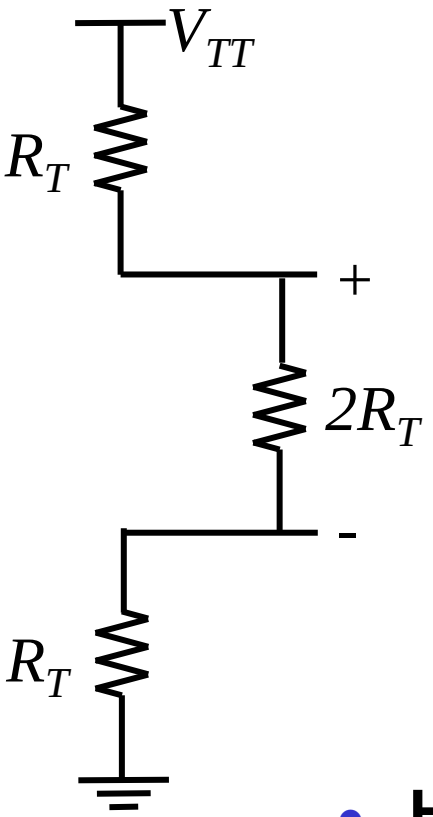
Low-Swing Voltage-Mode Driver



High-Swing Voltage-Mode Driver



VM Driver Power Consumption



$$V_{SW,amp} = \frac{V_{TT}}{2}$$

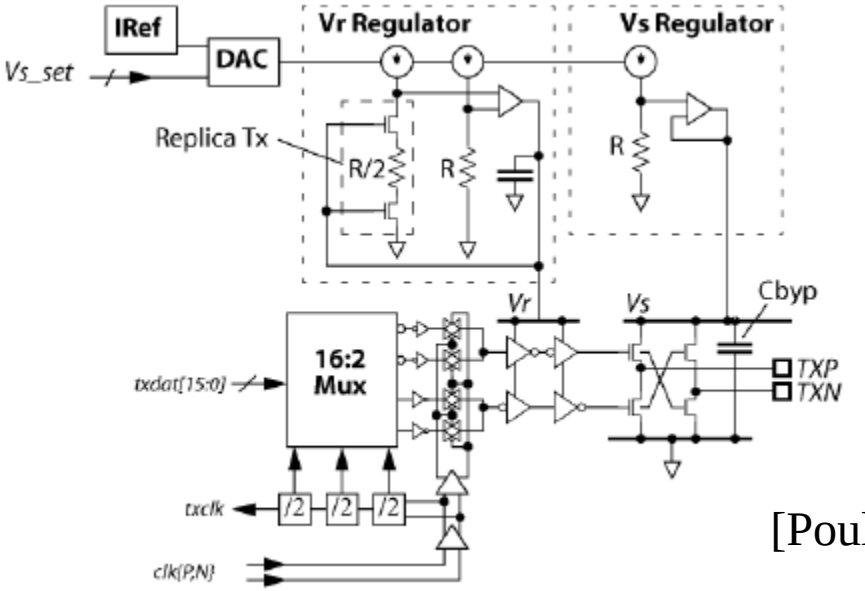
$$I_{V_{TT}} = \frac{V_{TT}}{4R_T}$$

$$P = V_{SW,amp} V_{TT} \frac{1}{2R_T}$$ ¼ CML

$$P = V_{SW,amp}{}^2 \frac{1}{R_T}$$

- **However**
  - Termination is set by devices
  - Impedance control loops are complicated
  - Matching pull-up and pull-down is difficult.

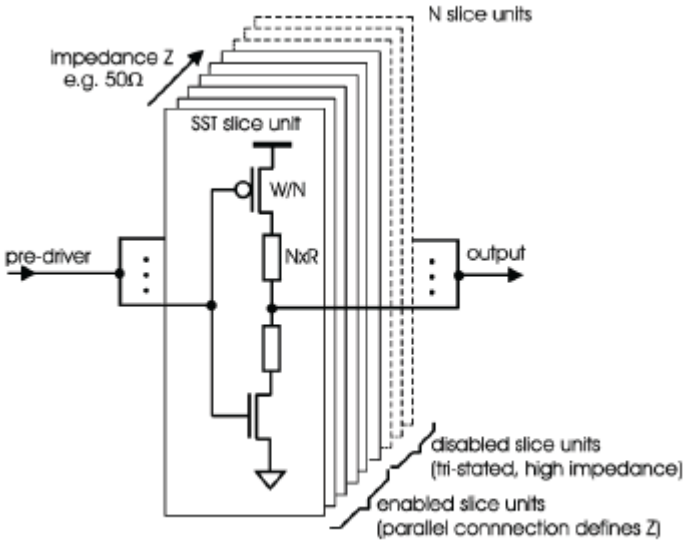
Low-Swing VM Driver Example



[Poulton JSSC Dec. 2007]

- A linear regulator sets the output stage supply, V_S.
- Termination is implemented by output NMOS transistors.
- To compensate for PVT and varying output swing levels, the pre-driver supply is adjusted with a feedback loop.
- The top and bottom output stage transistors need to be sized differently, as they see a different V_{DSAT}.

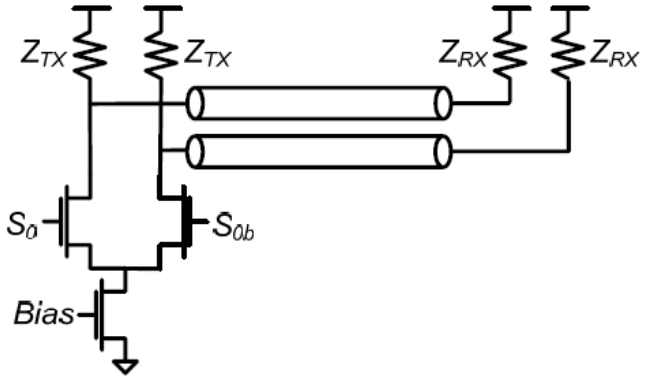
High-Swing VM Driver Example

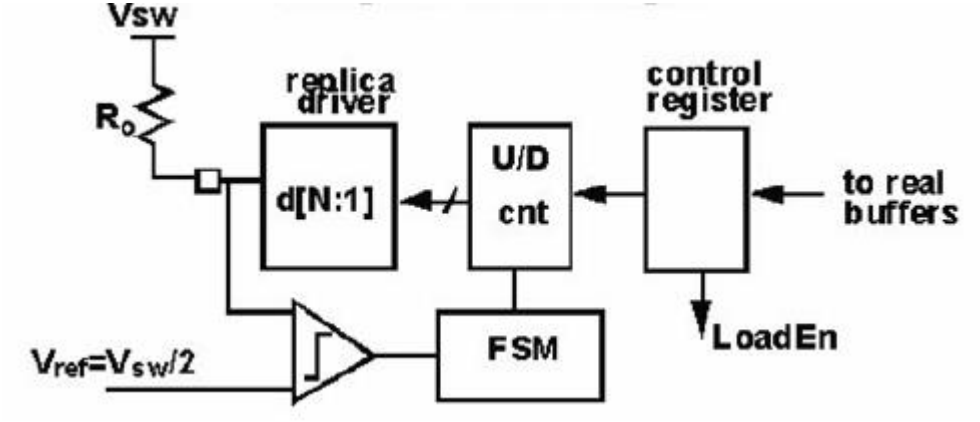


[Kossel JSSC Dec. 2008]

- **High-swing voltage-mode driver termination is implemented with a combination of output driver transistors and series resistors.**
- **To meet termination resistance levels (50 Ω), large output transistors are required.**
  - Degrades potential power savings.

TX Swing Control





- **Uncertainty in R_{TERM} and I_B can degrade output swing**
  - In low-swing drivers, this could be a big problem.
- **Extend R_{TERM} control to control the swing too.**
- **Control is done in two steps**
  - Impedance control
  - I-control by adaptively changing bias current.
- **Typically, a replica driver is used.**

TX Slew-Rate Control

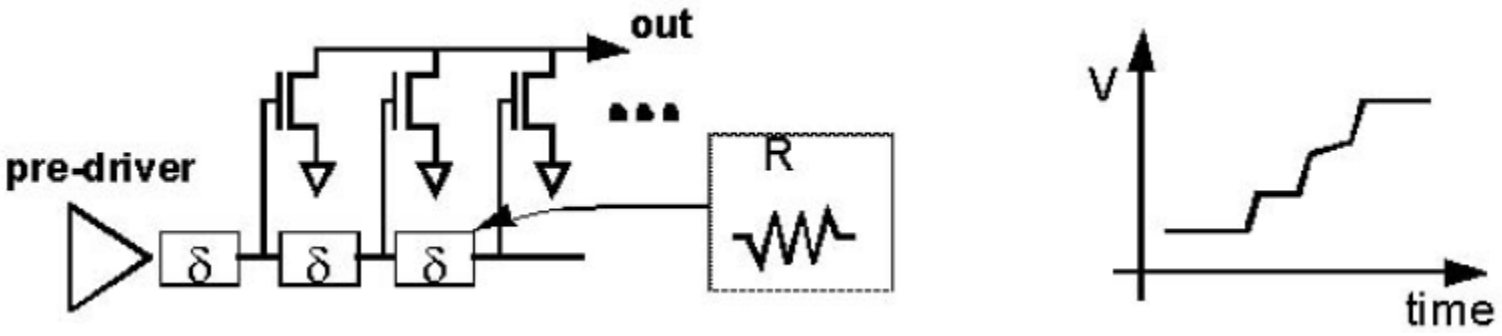
- **Output transition times should be controlled.**
  - Too Slow
    - Limits maximum data rate
  - Too fast
    - Can excite resonant circuits, resulting in ISI due to ringing
    - Cause excessive cross-talk because of large di/dt

- **Slew rate control reduces reflections and cross-talk.**

- **Controlling pre-driver is an effective means of controlling driver output slew-rate.**

Slew-Rate Control Implementation

- **Idea**
  - Break the driver into segments.
  - Turn on each segment sequentially.
- **Delay element**
  - Transistor-based doesn't track PVT changes well.
  - Use poly resistor that is relatively constant.
  - Use a timing element to sequentially time the switching.

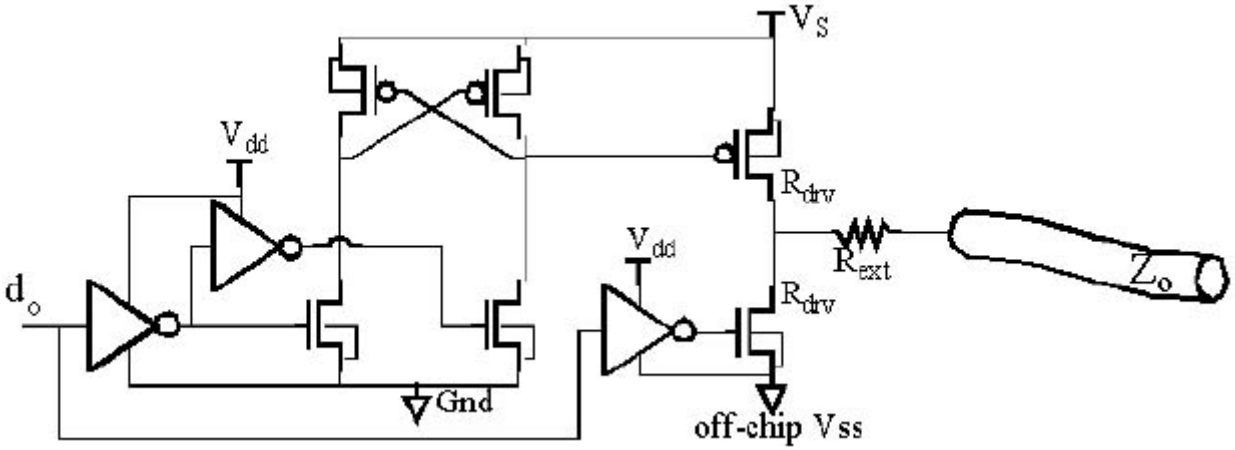


Pre-Drivers

- **Pre-drivers are needed for**
  - Capacitance driving
  - Level shifting
  - Timing control
  - Transient waveform improvement
  - Up and down impedance matching

- **A pre-driver is similar to the driver but with much lower current.**

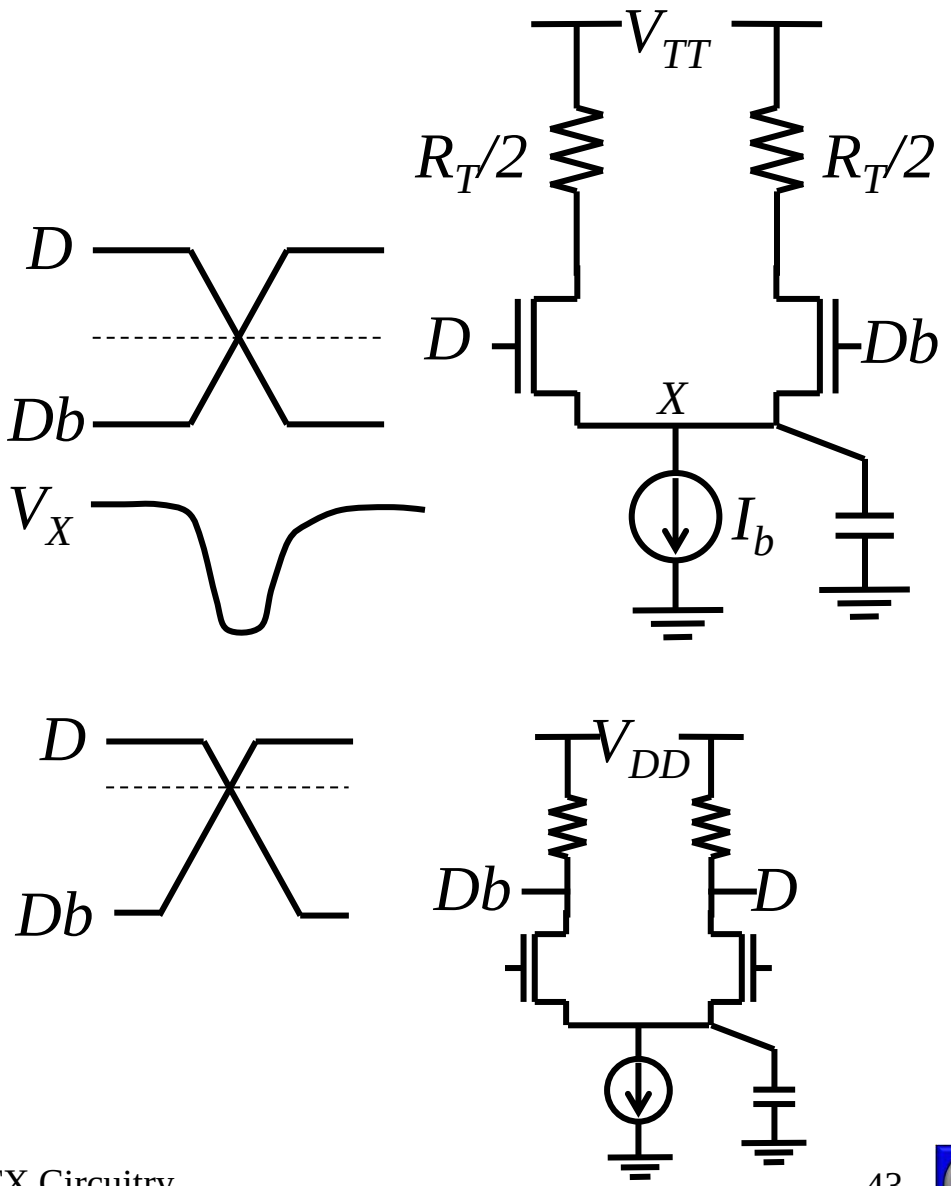
Pre-Driver Level Shifting



- **If swing $V_s > V_{dd}$, the pre-driver needs to level shift the output**
  - If not, the PMOS will not shut off completely when needed.
- **Level shifting can be achieved by a "pump" circuit.**
- **Reliability issues**
  - Cross-coupled PMOS devices need to have their wells tied to external voltage.

Pre-Drivers for CML

- **Ideal waveforms for the CML driver will cause big drops on the tail current voltage and current.**
- **This affects overall performance.**
- **Skewed inverters can be used as pre-drivers.**
- **CML pre-drivers can be used as well to have a smaller input swing.**
  - Low current

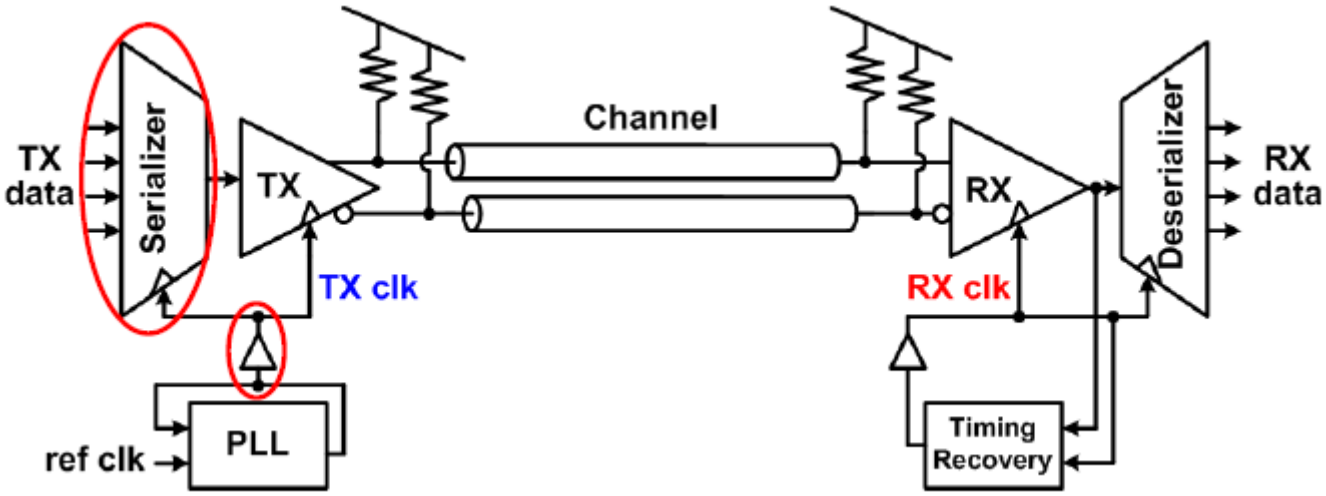


Outline

- **Signaling Basics**
  - Single-ended vs. differential
  - Voltage-mode vs. current-mode
- **Termination Circuits**
  - On-Chip vs. off-chip
  - AC vs. DC coupled
  - Active vs. passive
- **TX Driver Circuits**
  - Large swing drivers
  - Small swing drivers
  - Pre-drivers
- **Multiplexing**
  - Multiplexing depth
  - Multiplexing circuits

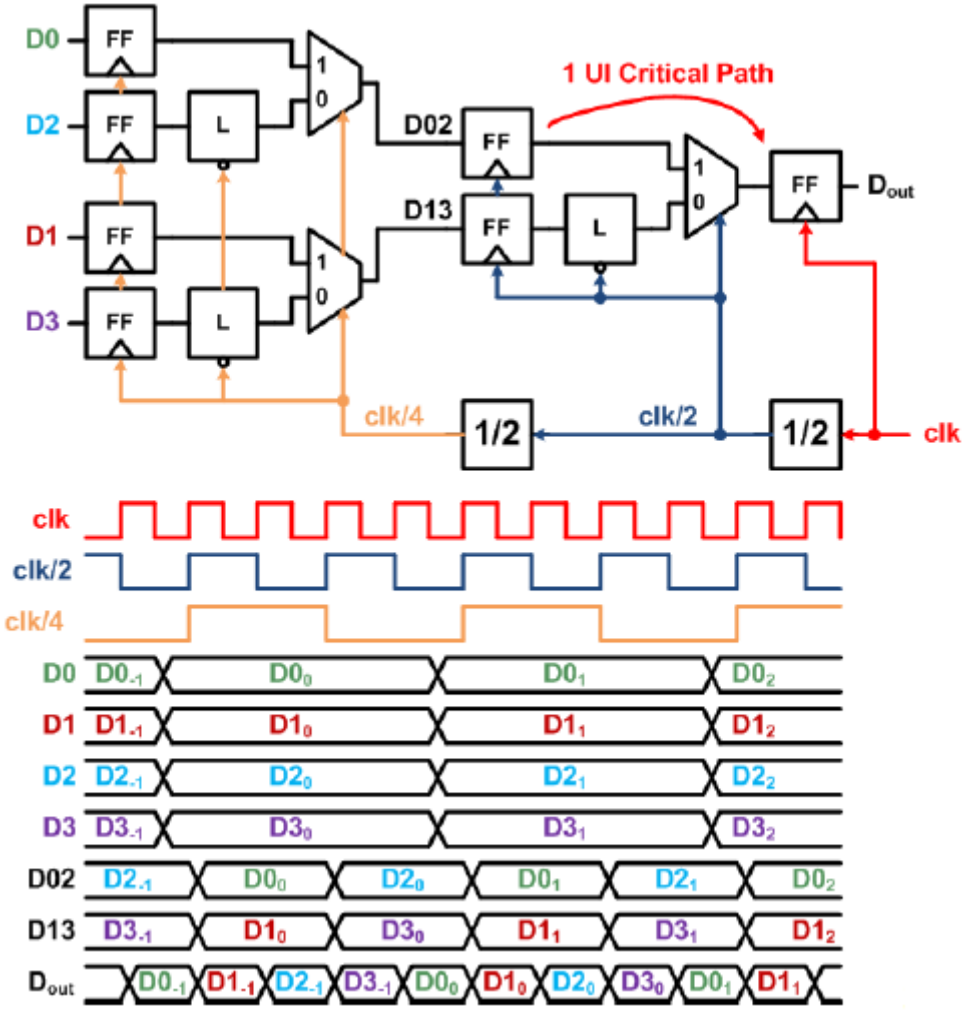
TX Circuit Speed Limitations

- High-speed links can be limited by both the channel and the circuits.
- Clock generation and distribution is key circuit bandwidth bottleneck.
- Multiplexing circuitry also limits maximum data rate.



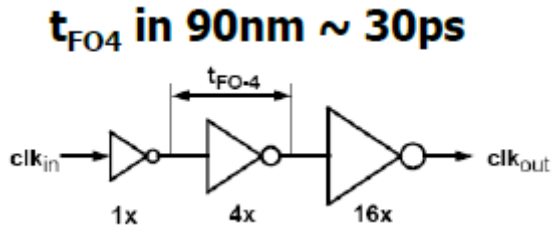
Full-Rate Multiplexing

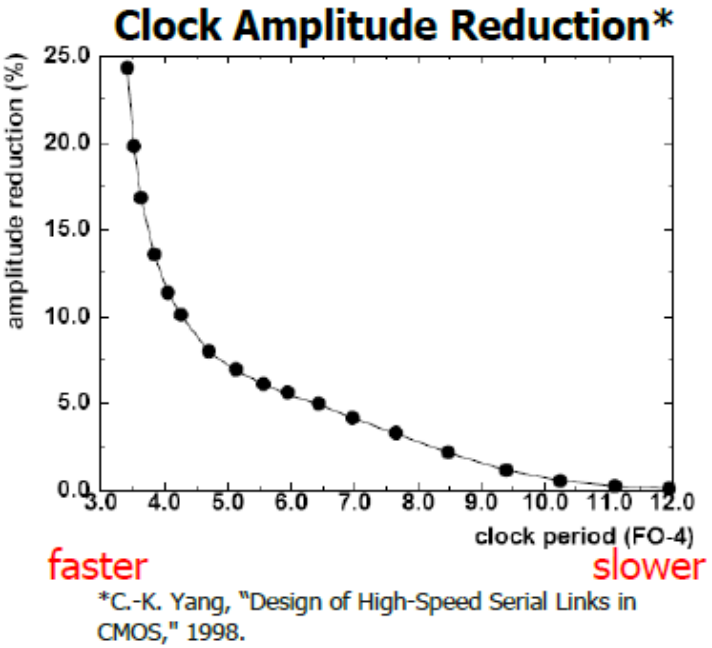
- **Tree-mux architecture with cascaded 2:1 stages is often used.**
- **Full-rate architecture relaxes clock duty-cycle, but limits max data rate.**
  - Needs to generate and distribute high-speed clock.
  - Needs to design high-speed flip-flop.
- **CML logic is sometimes used in last stages.**
  - Minimize CML to save power.



Clock Distribution Speed Limitations

- **Max clock frequency that can be efficiently distributed is limited by clock buffers ability to propagate narrow pulses.**
- **CMOS buffers are limited to a min clock period near 8FO4 inverter delays.**
  - About 4GHz in typical 90nm CMOS
  - Full-rate architecture limited to this data rate in Gb/s.
- **Need a faster clock, use faster clock buffers.**
  - CML
  - CML w/ inductive peaking

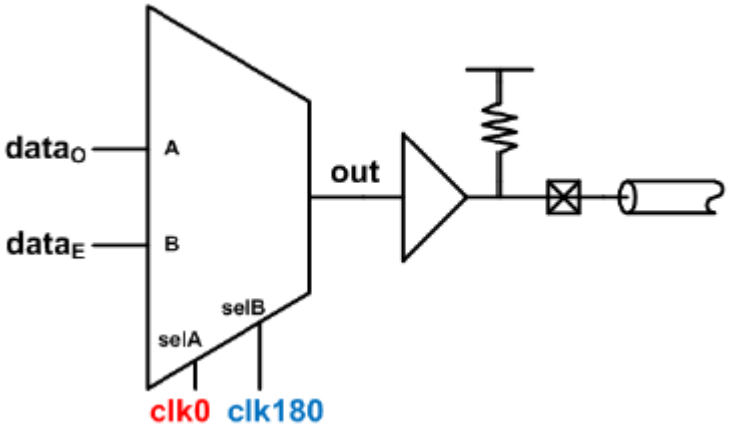


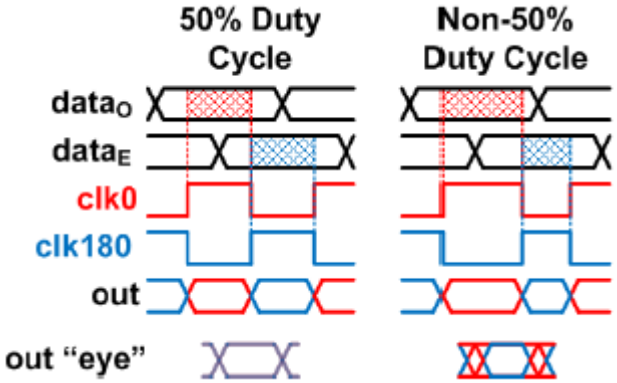


*C.-K. Yang, "Design of High-Speed Serial Links in CMOS," 1998.

Multiplexing Techniques – ½ Rate

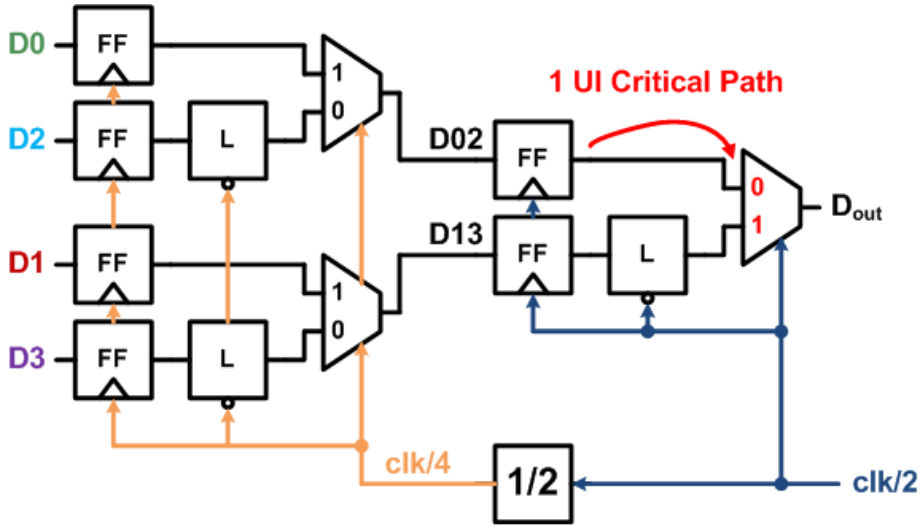
- **Full-rate architecture is limited by maximum clock frequency to 8FO4 T_b.**
- **To increase data rates eliminate final retiming and use multiple phases of a slower clock to mux data.**
- **Half-rate architecture uses 2 clock phases separated by 180° to mux data.**
  - Allows for 4FO4 T_b
  - 180° phase spacing (duty cycle) critical for uniform output eye

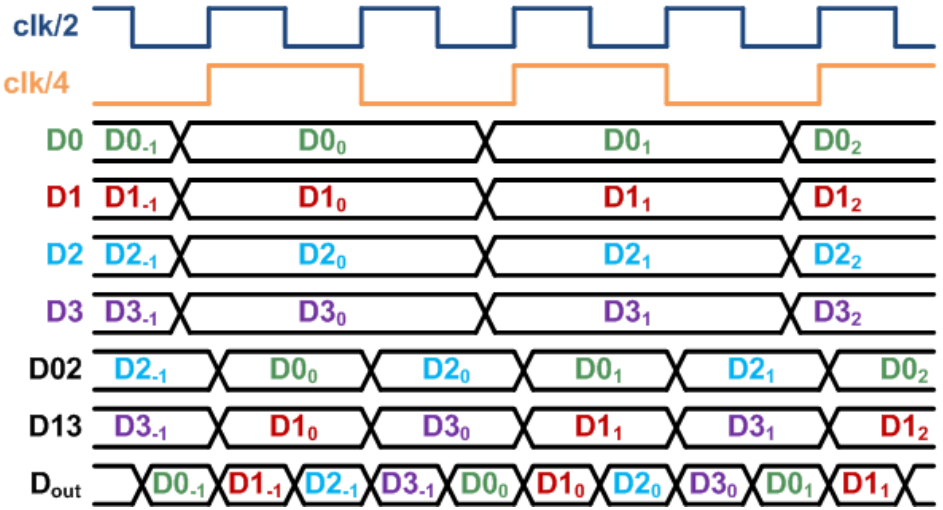




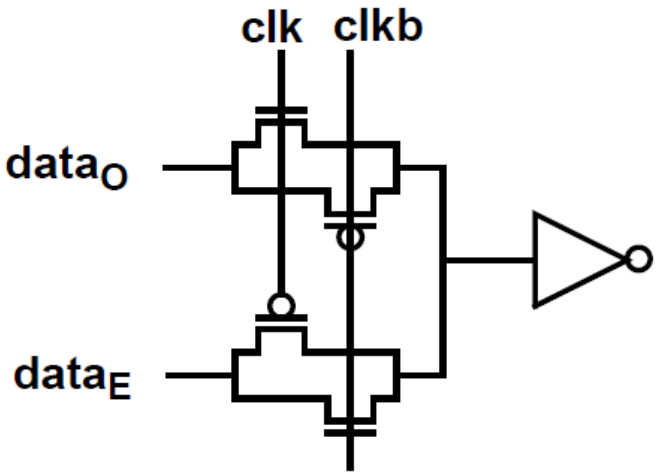
Half-Rate Multiplexing Timing Waveforms

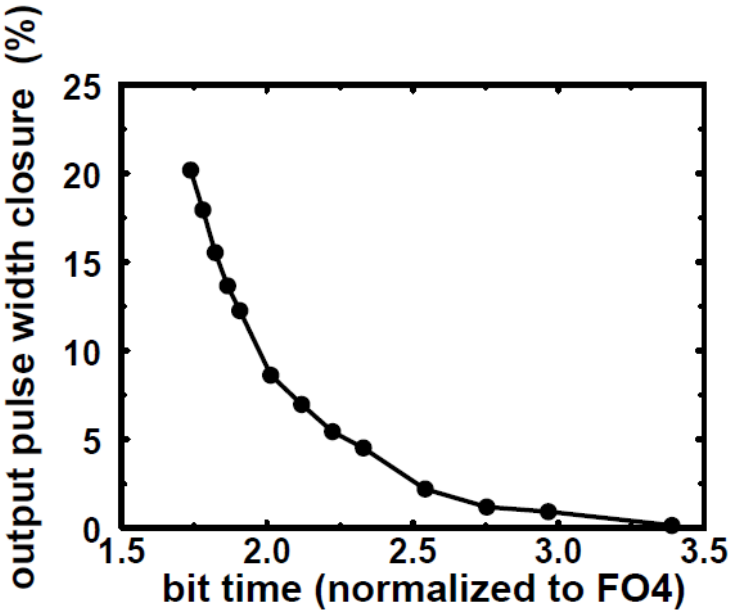
- **Half-rate architecture eliminates high-speed clock and flip-flop.**
- **Output eye is sensitive to clock duty cycle.**
- **Critical path no longer has flip-flop setup time.**





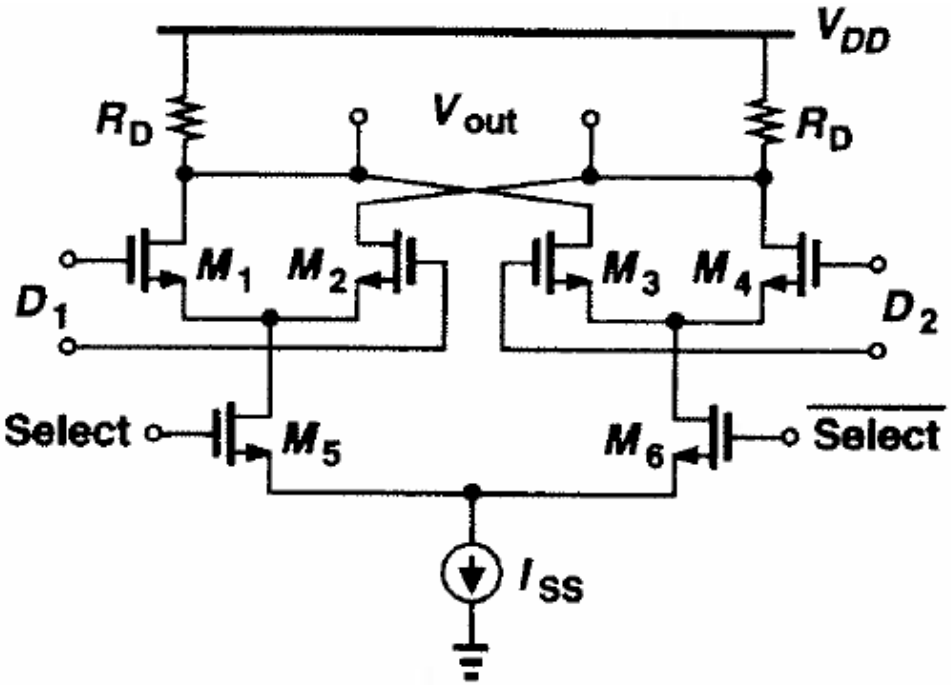
2:1 CMOS Multiplexer





- **2:1 CMOS mux is able to propagate a minimum pulse near 2FO4 Tb.**
- **However, with a ½-rate architecture it is still limited by clock distribution to 4FO4 Tb.**
  - 8Gb/s in typical 90nm

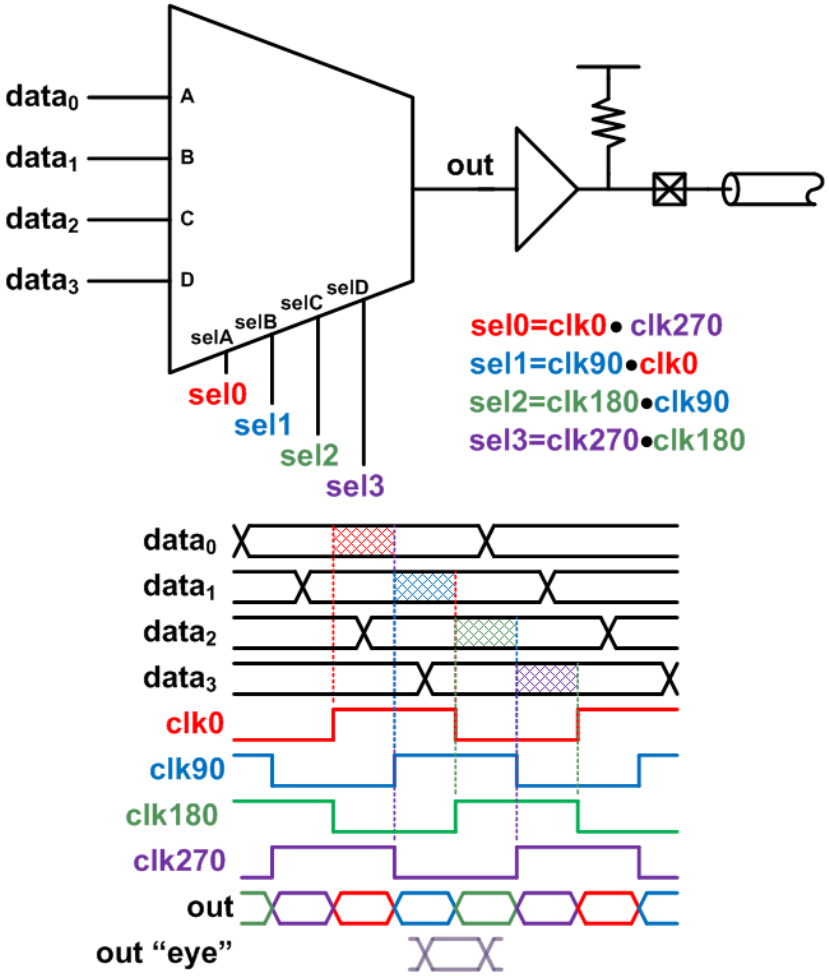
2:1 CML Multiplexer



- CML mux can achieve higher speeds due to reduced self-loading factor.
  - Cost is higher power consumption that is independent of data rate (static current).

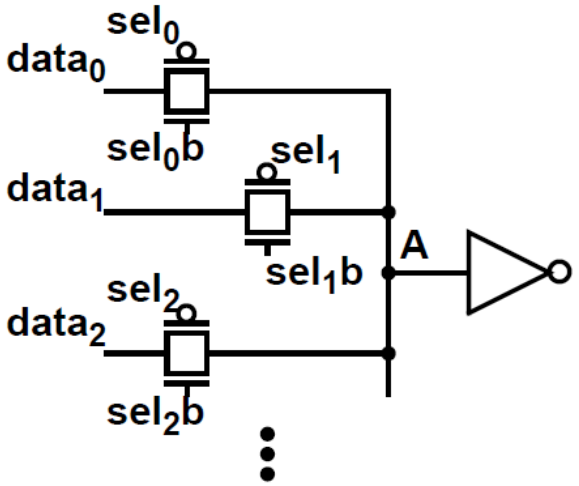
Increasing Multiplexing Factor – ¼ Rate

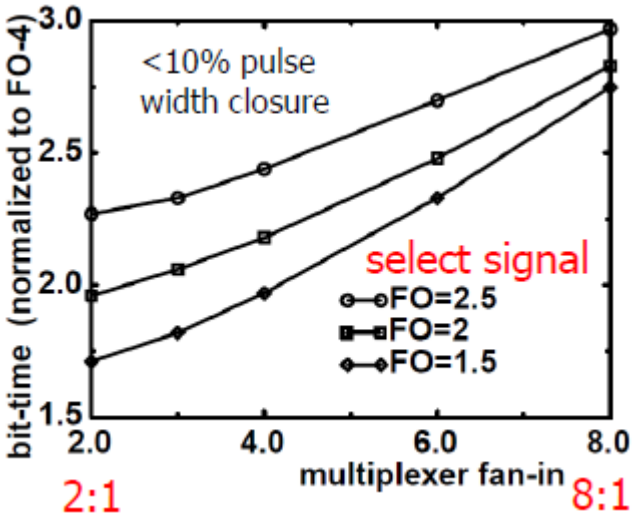
- **Increase multiplexing factor to allow for lower frequency clock distribution.**
- **¼-rate architecture**
  - 4-phase clock distribution spaced at 90° allows for 2FO4 Tb.
  - 90° phase spacing and duty cycle critical for uniform output eye.



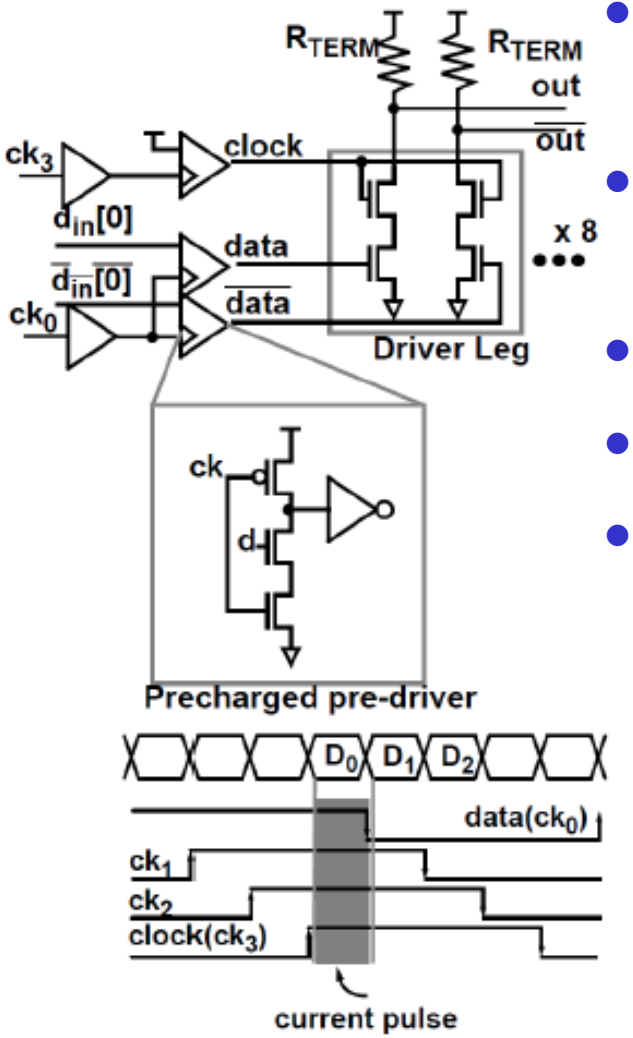
Mux Speed vs. Fan-in

- **Higher fan-in muxes run slower due to increased cap at mux node.**
- **1/4-rate architecture**
  - 4:1 CMOS mux can potentially achieve 2FO4 Tb with low fanout.
    - An aggressive CMOS-style design has potential for 16Gb/s in typical 90nm CMOS
- **1/8-rate architecture**
  - 8-phase clock distribution spaced at 45° allows for 1FO4 Tb
  - No way a CMOS mux can achieve this!!

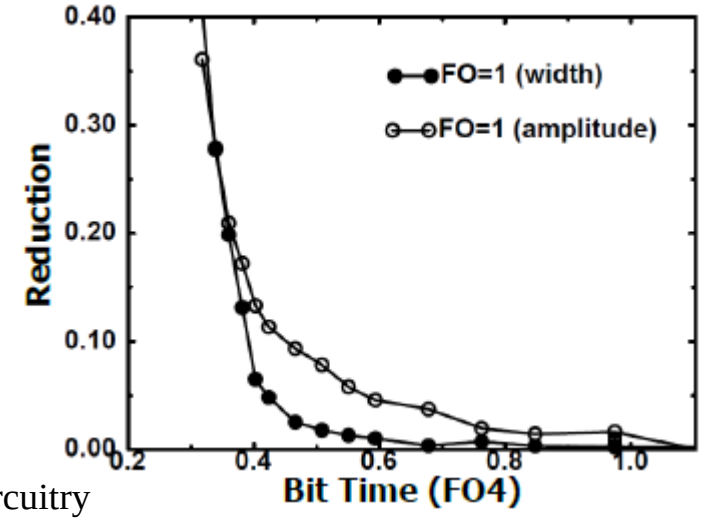




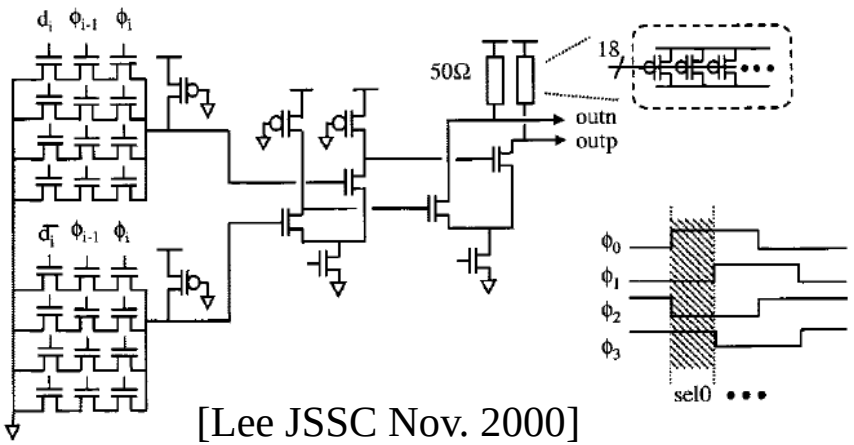
Current-Mode Output-Multiplexed



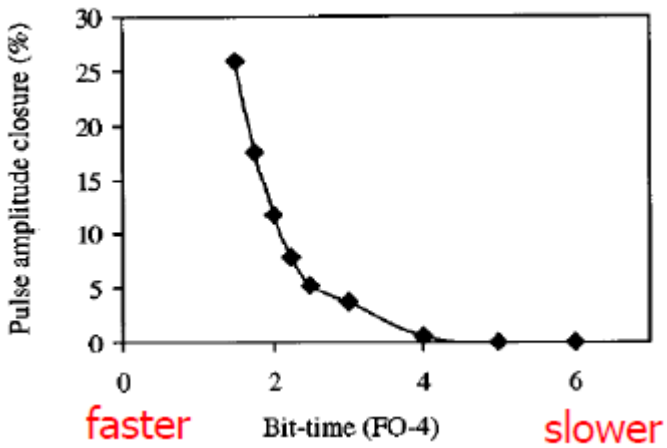
- 8:1 current-mode mux directly at output pad.
- Makes sense if output time constant smaller than on-chip time constant.
- Very sensitive to clock phase spacing.
- Yang achieved 6Gb/s in 0.35µm CMOS.
- Equivalent to 33Gb/s in 90nm CMOS (now channel (not circuit) limited)



Current-Mode Input-Multiplexed

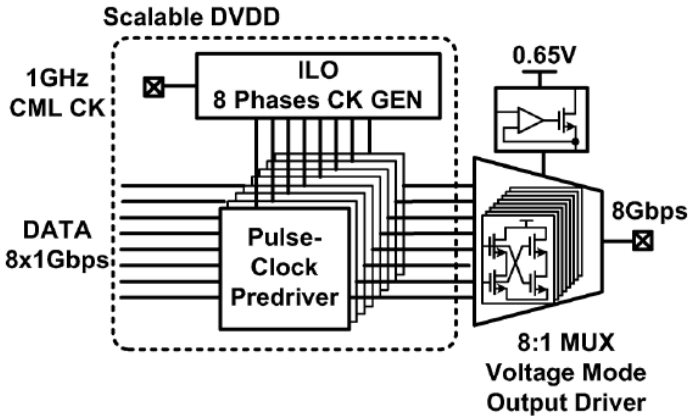


[Lee JSSC Nov. 2000]

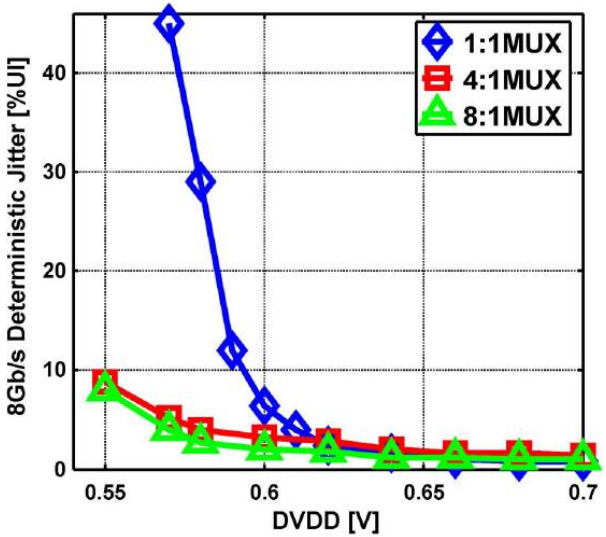


- **Reduces output capacitance relative to output-multiplexed driver**
  - Easier to implement TX equalization
- **Not sensitive to output stage current mismatches**
- **Reduces power due to each mux stage not having to be sized to deliver full output current**

Voltage-Mode Output-Multiplexed



[Song, JSSC May 2013]



- **8:1 voltage-mode mux directly at output pad.**
- **Makes sense if output time constant smaller than on-chip time constant.**
- **Allowed running from lower supply with lower jitter performance.**
- **Song achieved 6.4Gb/s in 65nm CMOS with only 0.3 pJ/bit excluding clocking power.**