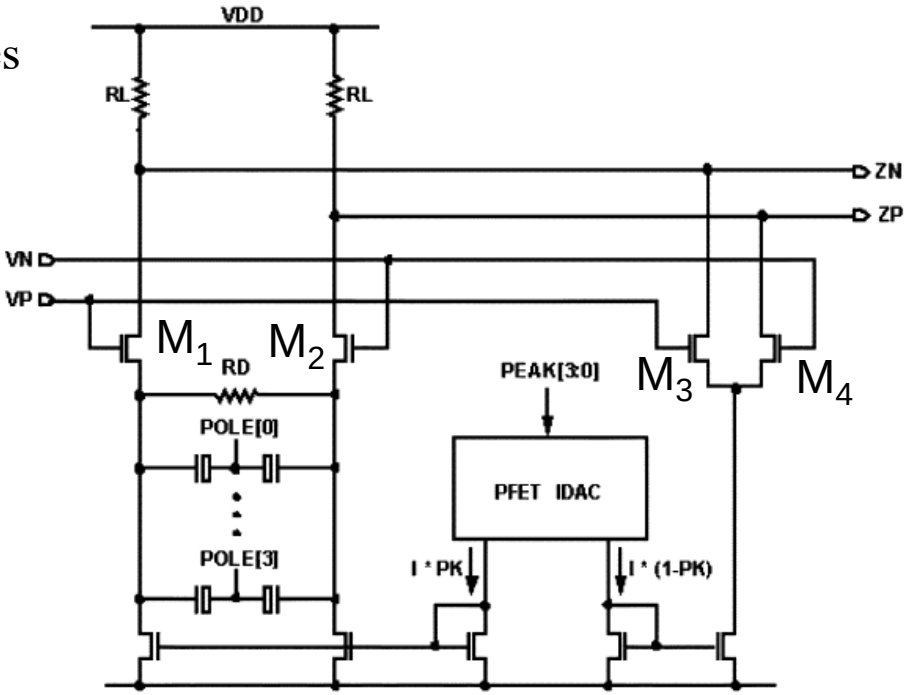
High-Speed Wire Line Receivers

Lecture 6

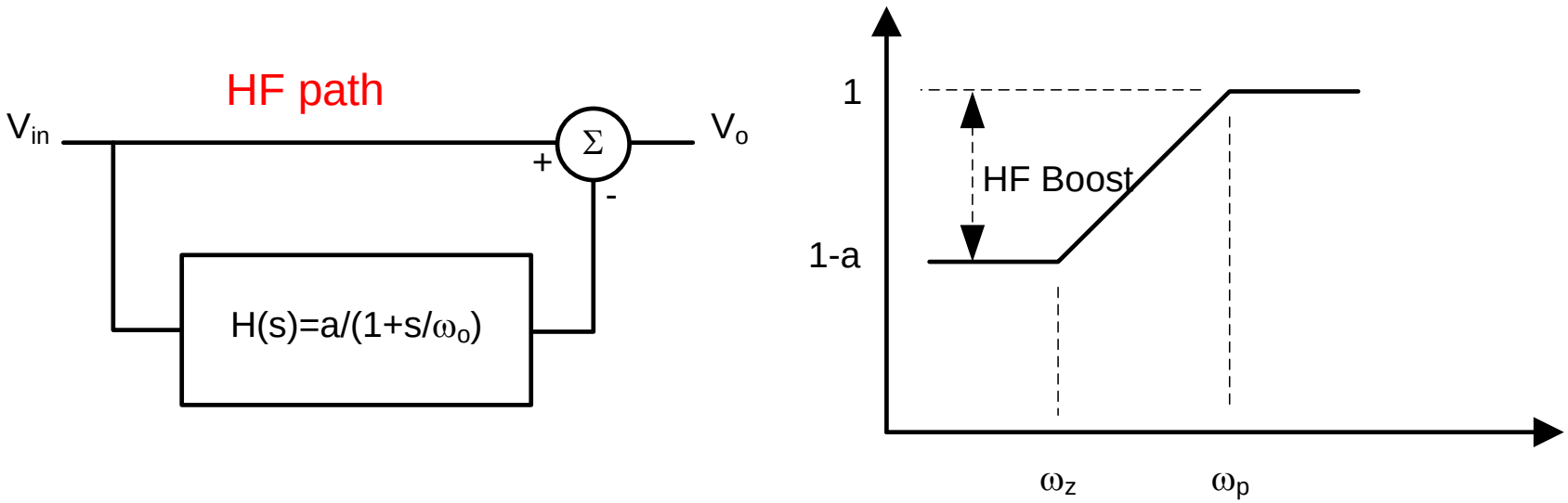
JSSC 2005: 6.4-Gb/s CMOS SerDes core with FFE and DFE

- The CTLE is a combination of the responses of two amplifiers
- M1 & M2 have a fixed peaking determined by R_D and $g_{m1,2}$ and M3 & M4 has no peaking
- The combined peaking level is adjusted by controlling the ratio of the tail currents to two amplifiers
- The IDAC ensures a fixed total current for both amplifiers → CTLE output common-mode is always fixed
- The frequency at which the peak occurs, referred to here as the pole position, is adjusted by the degeneration capacitor



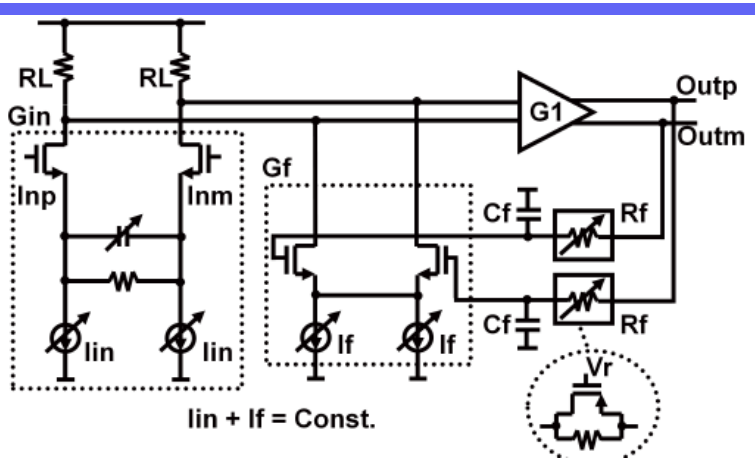
$$\frac{V_o}{V_{in}} = \frac{R_L}{1/g_{m1,2} + (R_D/2)//(1/sC_{pole})} + g_{m3,4}R_L$$

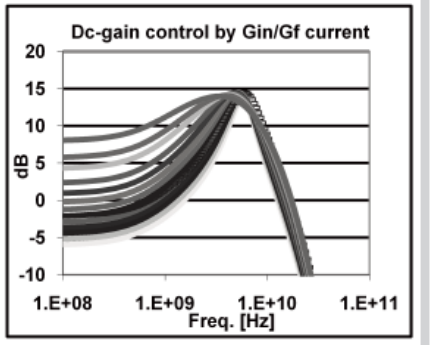
Alternative CTLE Architectures

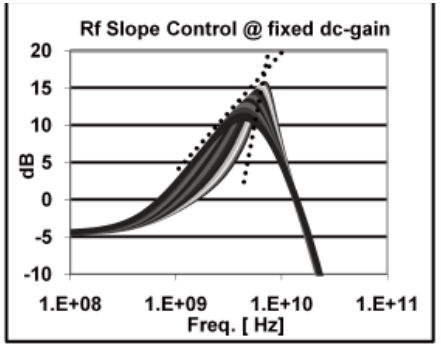


- A CTLE could have two parallel path: a DC path and a HF path
- $H_T(s)=(1-a+s/\omega_o)/(1+s/\omega_o)$
- DC gain= 1-a, HF gain= 1
- The CTLE has a zero at $\omega_z=\omega_o(1-a)$, and a pole at ω_o
- If 0<a<1, then the circuit provides HF boost = 1/(1-a)

ISSCC 2010: A 12Gb/s 39dB Loss-Recovery Receiver





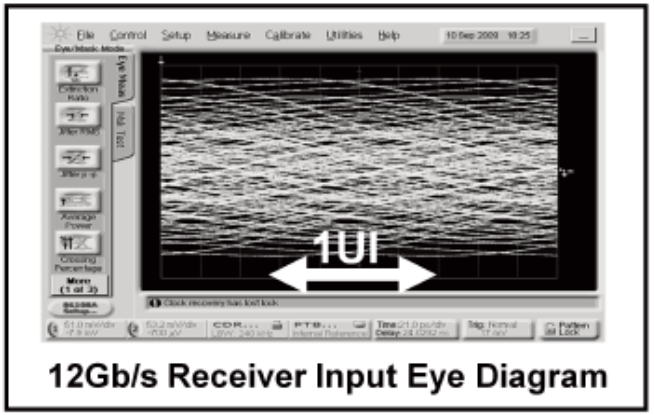


- The first-stage G_{in} drives a second stage made of the amplifier G_1 in the forward path and the Rf-Cf low-pass filter followed by Gf in the feedback path
- RC degeneration creates the first zero
- RC filter in the feedback path introduces a second zero to help shape the frequency response
- Switching the current from G_{in} to G_f affects the low-frequency gain
- The variable resistor Rf controls the filter slope

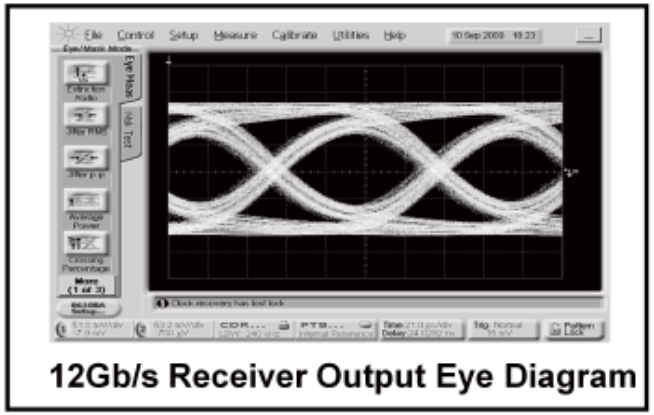
$$V_o = \frac{R_L}{1/g_{m,in} + (R/2)//(2/sC_{pole})} V_{in} \times G_1 - V_o \frac{1/sC_f}{R_f + 1/sC_f} g_{m,f} R_L \times G_1$$

M. Pozzoni et al., "A 12Gb/s 39dB loss-recovery unclocked-DFE receiver with bi-dimensional equalization," 2010 IEEE International Solid-State Circuits Conference - (ISSCC), 2010, pp. 164-165, doi: 10.1109/ISSCC.2010.5434006.

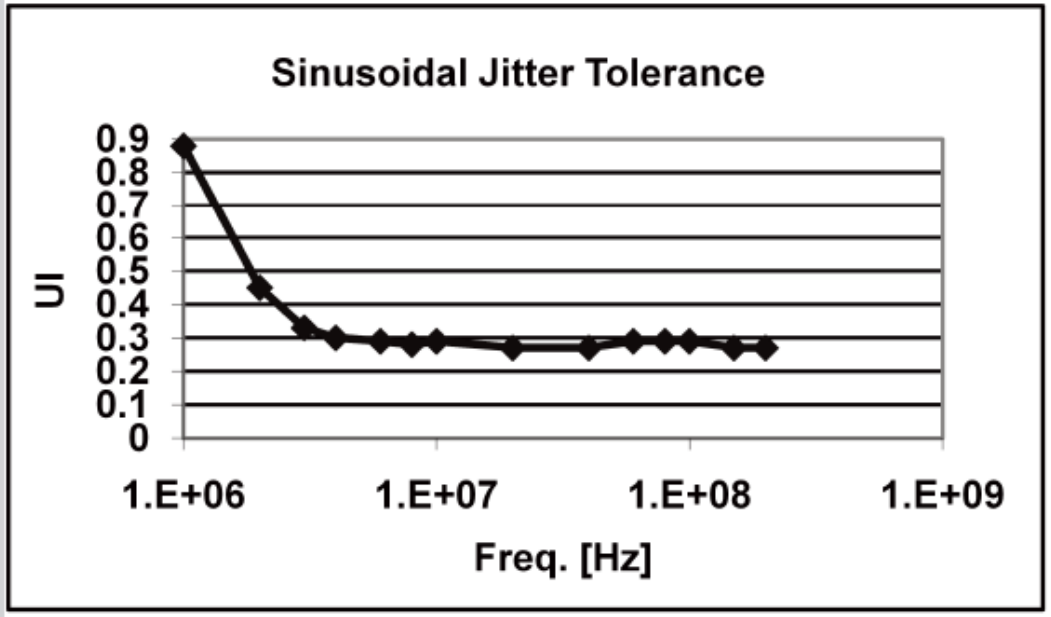
ISSCC 2010: A 12Gb/s 39dB Loss-Recovery Receiver

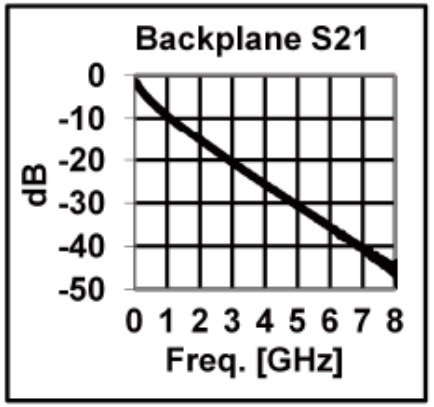


12Gb/s Receiver Input Eye Diagram

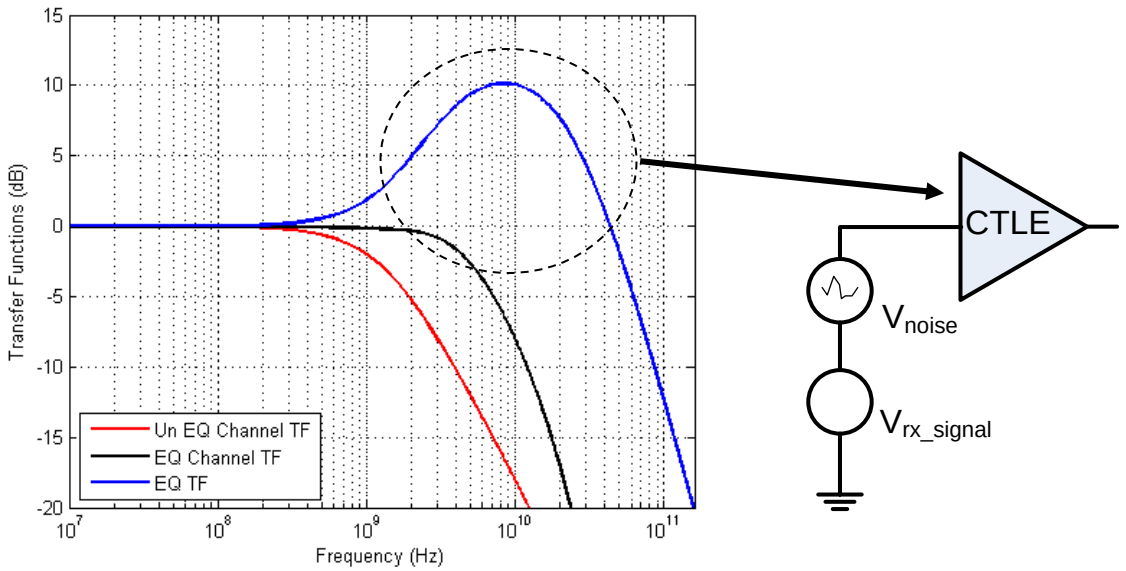


12Gb/s Receiver Output Eye Diagram



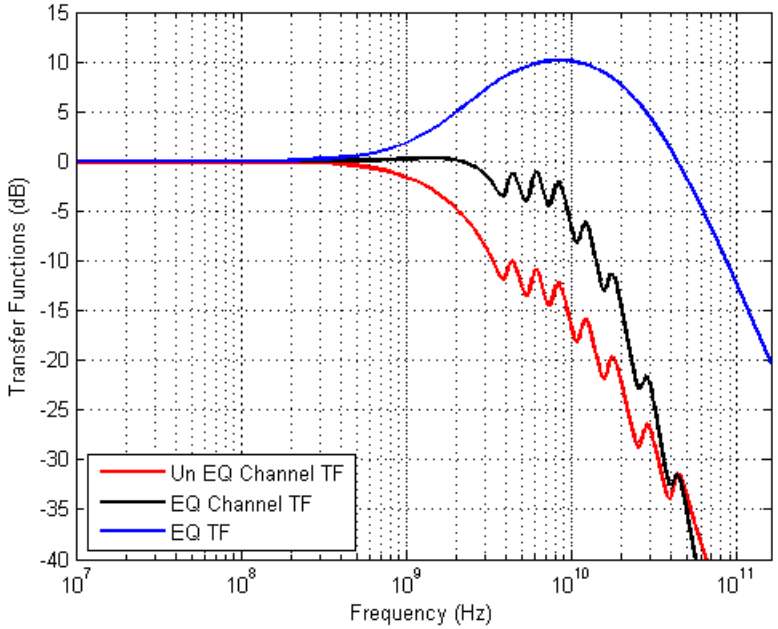


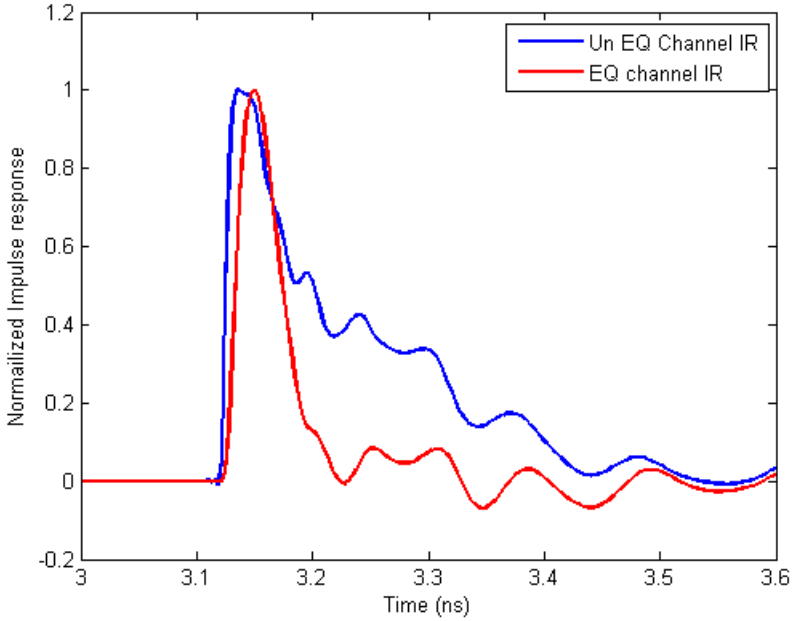
CTLE Drawbacks



- One of the main draw backs of CTLEs → it amplifies noise along with the signal
- This includes thermal noise and cross-talk
- A CTLE alone is usually insufficient for very long backplanes (>20dB of loss at the Nyquist frequency)
- Impact of channel reflections on the received signal is not easily cancelled using a CTLE which usually has a generic boost profile.
- It is important to use more sophisticated equalization techniques → DFEs

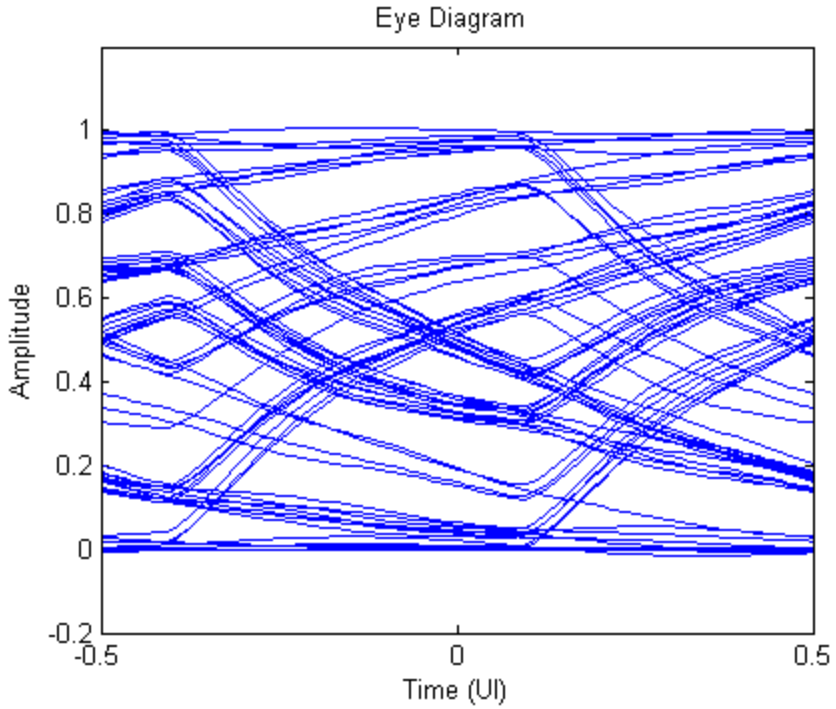
Un Equalized vs. Equalized Channel Response For Channel with Reflections

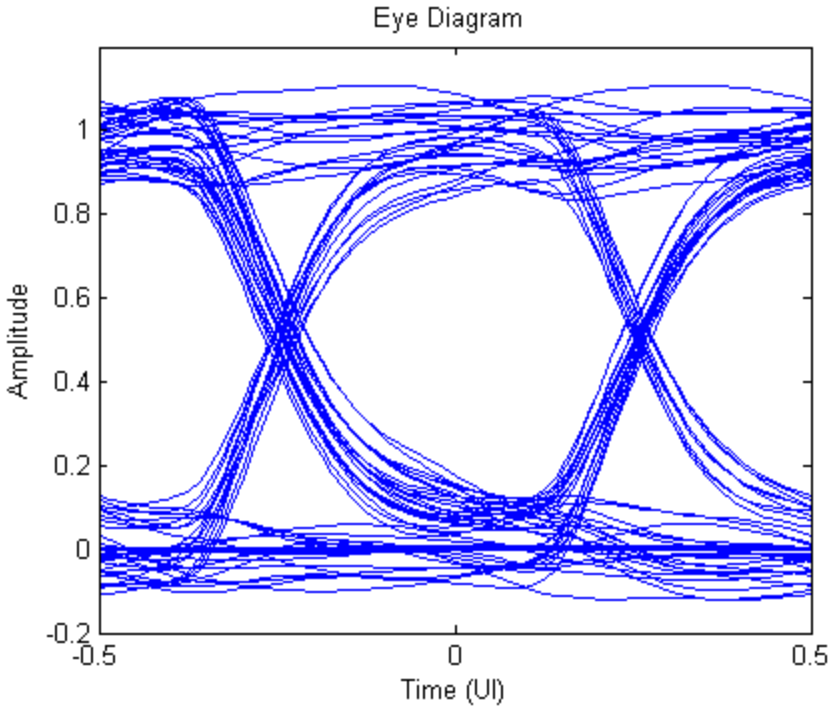




- Channel has 13dB loss at Nyquist (5GHz)
- The combined EQ stages provide up to 9.5dB of boost at Nyquist
- The channel impulse response shows significant pulse spreading before equalization
- Reflections result in residual ISI that is not easily cancelled by a CTLE

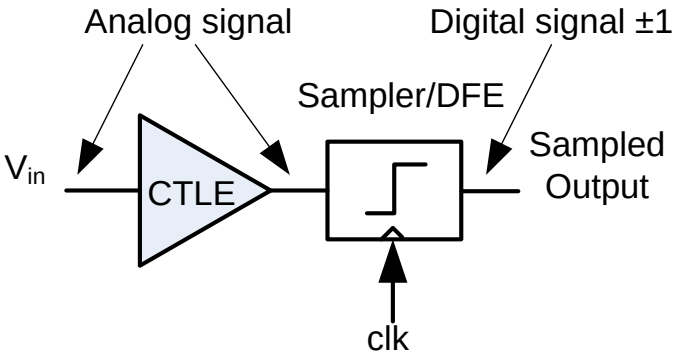
10Gbps Eye diagrams before & after the CTLE For Channel with Reflections

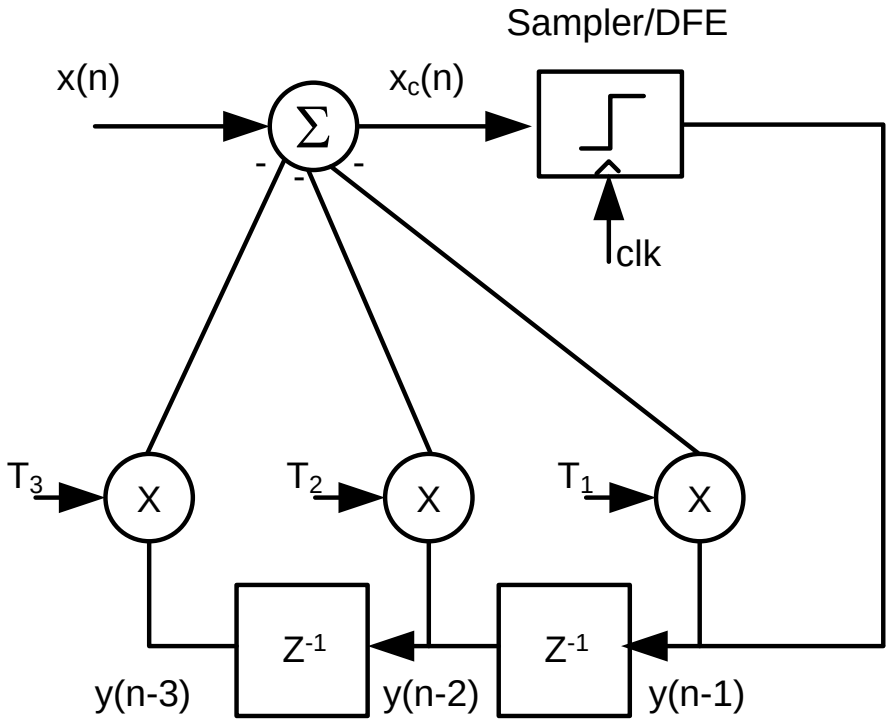




- Reflections result in partial closure for the vertical/horizontal eye openings

Decision Feedback Equalizer (DFE)

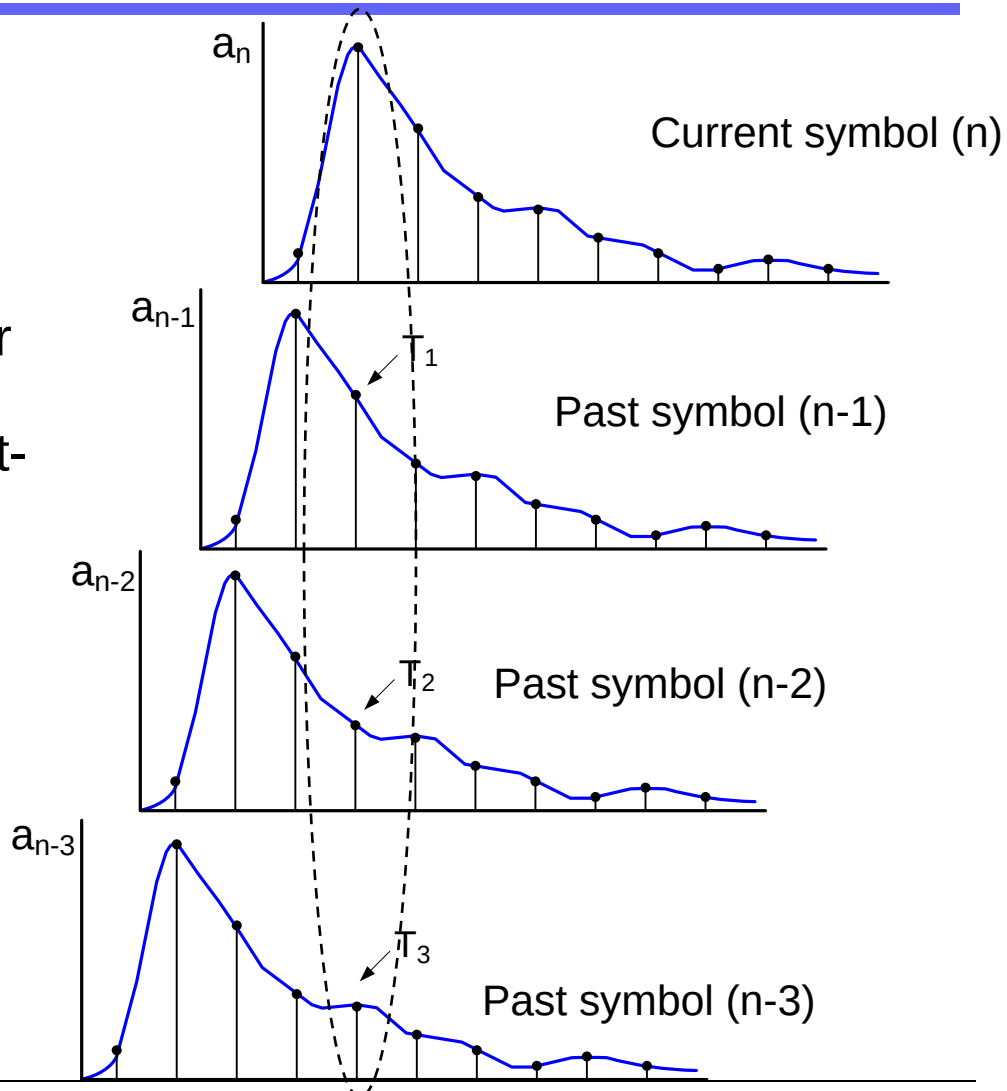




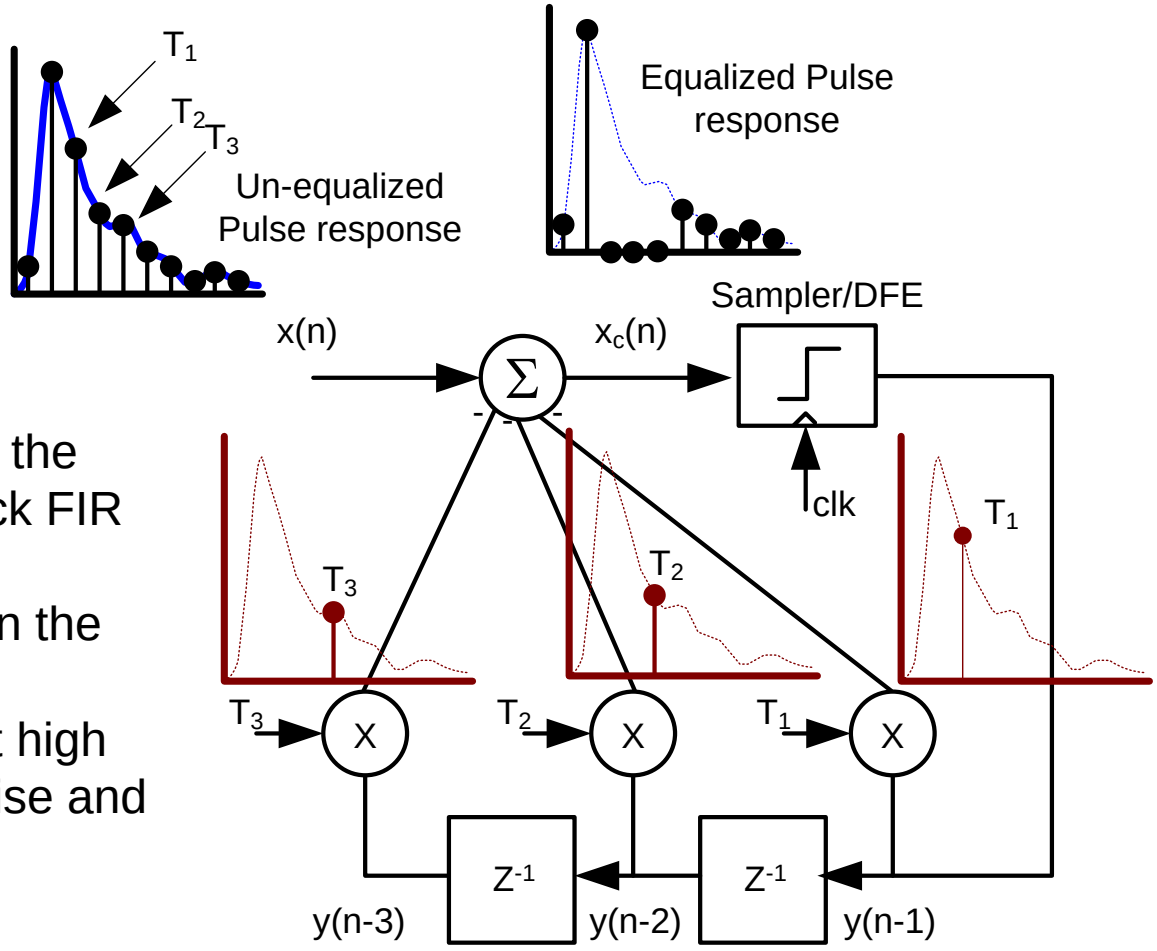
- For low loss channels, the eye opening after the CTLE is reasonable and a sampler could be used to digitize the signal for the clock and data recovery
- If additional equalization is required a DFE is used to cancel residual ISI and near by reflections (why not far reflections?)
- A DFE is a **non-linear** equalizer which uses the past decisions to correct for post-cursor ISI before taking its new decisions

Inter Symbol Interference

- The transmitted symbols 0s and 1s are represented by $a_n = \pm 1$
- Past symbols add post-cursor ISI to the main-cursor
- The eye closure can be directly calculated if the post-cursor ISI terms are known
- If a_n and a_{n-1} have opposite polarity (i.e. a transition bit) the ISI terms subtract from the main cursor



3-Tap DFE Operation



- ISI is directly subtracted from the incoming signal via a feedback FIR filter
- Sampler takes the decision on the corrected signal $x_c(n)$
- Unlike CTLE, DFE Can boost high frequency content without noise and crosstalk amplification
- Cannot cancel pre-cursor ISI

DFE (Cont'd)

- The analog equalized signal of the DFE can be expressed as:

$$x_c(n) = x(n) - \sum_{k=1}^{N} T_k y(n-k)$$

- N is the number of DFE taps, and T_k are the DFE tap weights
- Optimum DFE tap weights/polarities are unknown a priori and are determined via adaptive algorithms
- The decision y(n) is made based on the equalized signal $x_c(n)$

$$y(n) = \mathrm{sgn}(x_c(n)) = \mathrm{sgn}(x(n) - \sum_{k=1}^{N} T_k y(n-k))$$

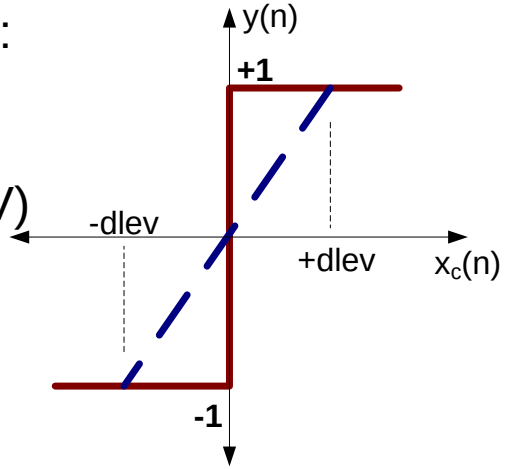
- The DFE input x(n) is an analog signal whereas, it's output y(n) is a digital signal ±1
- Hence the **non-linear** nature

DFE HF Boost Calculation

- DFE is a non linear equalizer, however with some approximations one can analyze it in a linear fashion
- The comparator sign function can be linearized as follows:

$$y(n) = x_c(n) / dlev$$

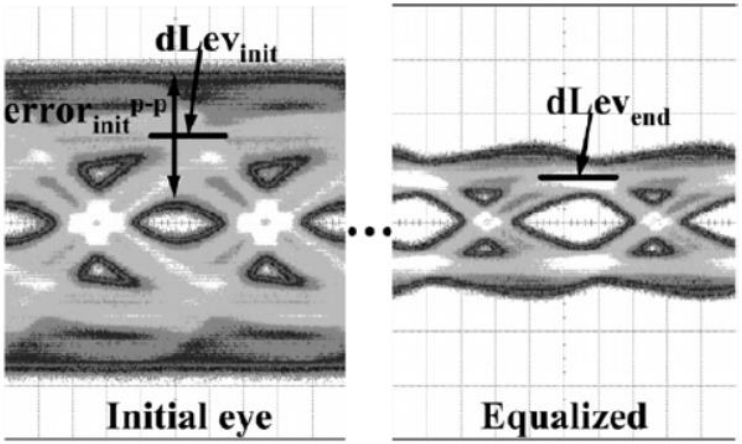
where *dlev* is the average signal level **after equalization** in (V)



$$x_c(n) \approx x(n) - \sum_{k=1}^{N} T_k x_c(n-k) / dlev$$

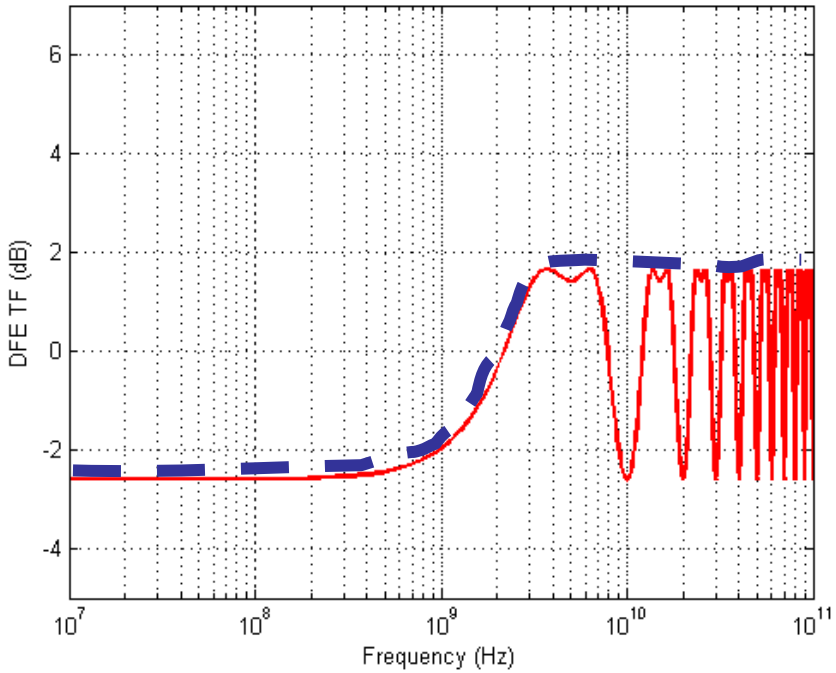
$$H_c(z) = \frac{1}{1 + \sum_{k=1}^{N} T_k z^{-k} / dlev}$$

where T_k is the actual tap weights in (V)



DFE HF Boost Calculation

- *Problem*: For a 2-tap DFE the normalized taps T_1=0.25 & T_2=0.1 Calculate the high frequency boost at Nyquist



- Solution:

$-z(f=F_N)=e^{j\omega Tb}=e^{j(2\pi Fb/2)Tb}=-1 \rightarrow H_c(f=f_N)=\frac{1}{1-T_1+T_2}$

$-z(f=0)=1 \rightarrow H_c(f=0)=\frac{1}{1+T_1+T_2}$

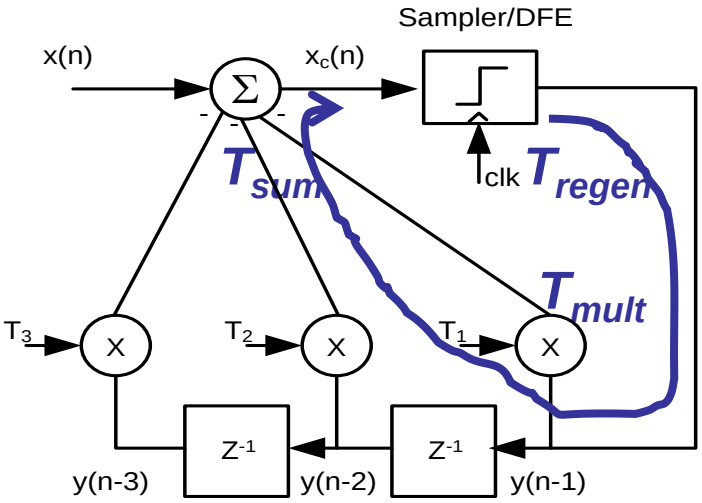
DFE HF Boost Calculation

$$H_c(f=0)=\frac{1}{1+T_1+T_2}=-2.6dB$$

$$H_c(f=f_N)=\frac{1}{1-T_1+T_2}=1.4dB$$

- Boost at Nyquist = 4dB
- Note that the DFE provides **a positive boost value for the HF** portion of the signal but at the same time it **attenuates the DC** portion of the signal
- This implies that there is a limit on how much boost can be obtained from a DFE since it eventually reduces the amplitude of the non-transition bits → similar to Tx pre-emphasis

DFE Feedback loop latency

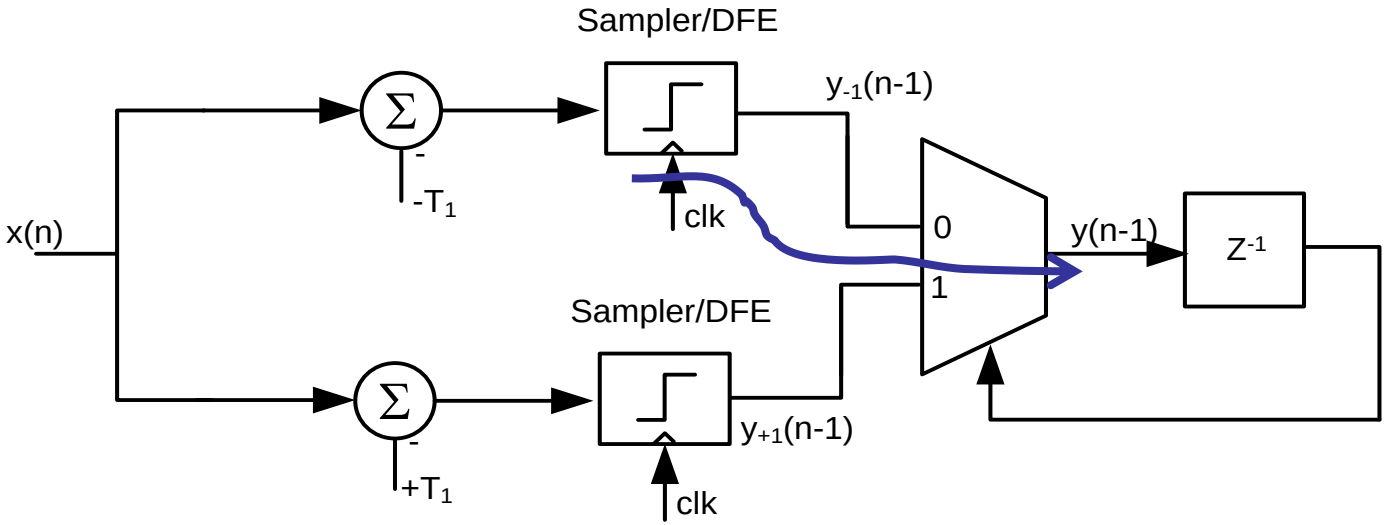


- Once the DFE comparator takes a decision it has to propagate through the multiplier and the summer and be ready before the next clock edge

$$T_{regen} + T_{mult} + T_{sum} + T_{setup} < T_{clk}$$

- T_{setup} is the comparator setup time, and $T_{regen}=T_{ck\text{-}Q}$
- For 10Gbps, the sum of these delays has to be less than 100ps
- Consequent taps don't have the same tough timing constraint due to the relaxed T_{regen}
- Capacitance at the summing node limits the maximum number of DFE taps

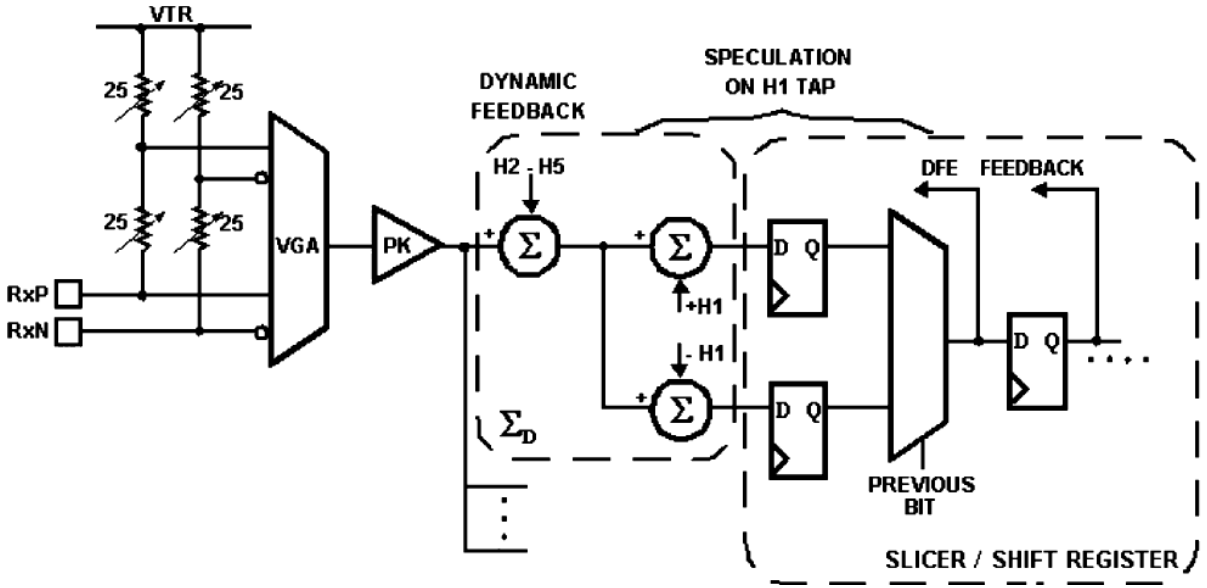
1-Tap DFE Feedback loop Unrolling



$$T_{regen} + T_{mux} + T_{setup} < T_{clk}$$

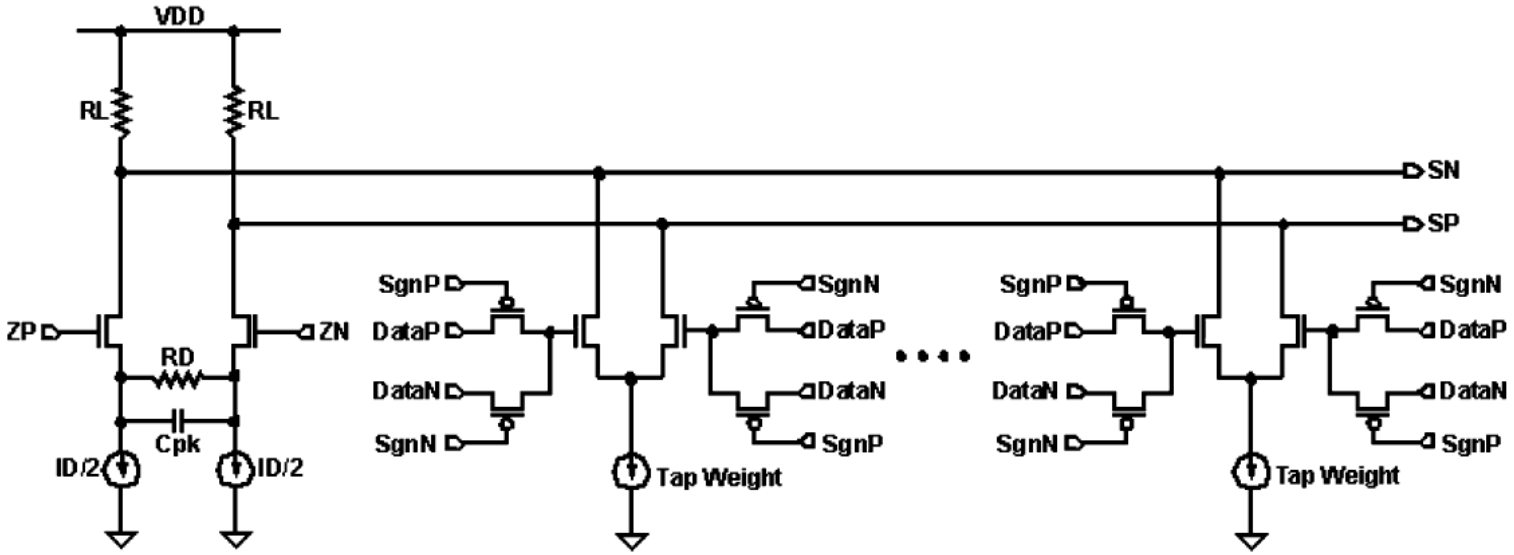
- 2 decisions are made a priori; one with an offset $+T_1$ and the other with $-T_1$
- After the following bit decision settles the MUX output automatically selects the correct output
- Eliminates T_{mult} *and* T_{sum} → allows operating at higher speeds
- *Also,* T_{setup} in this case is much smaller →since the comparator is not resolving a small signal as in previous case
- Double the area, and double the loading on the CTLE output

JSSC 2005: 6.4-Gb/s CMOS SerDes core with FFE and DFE



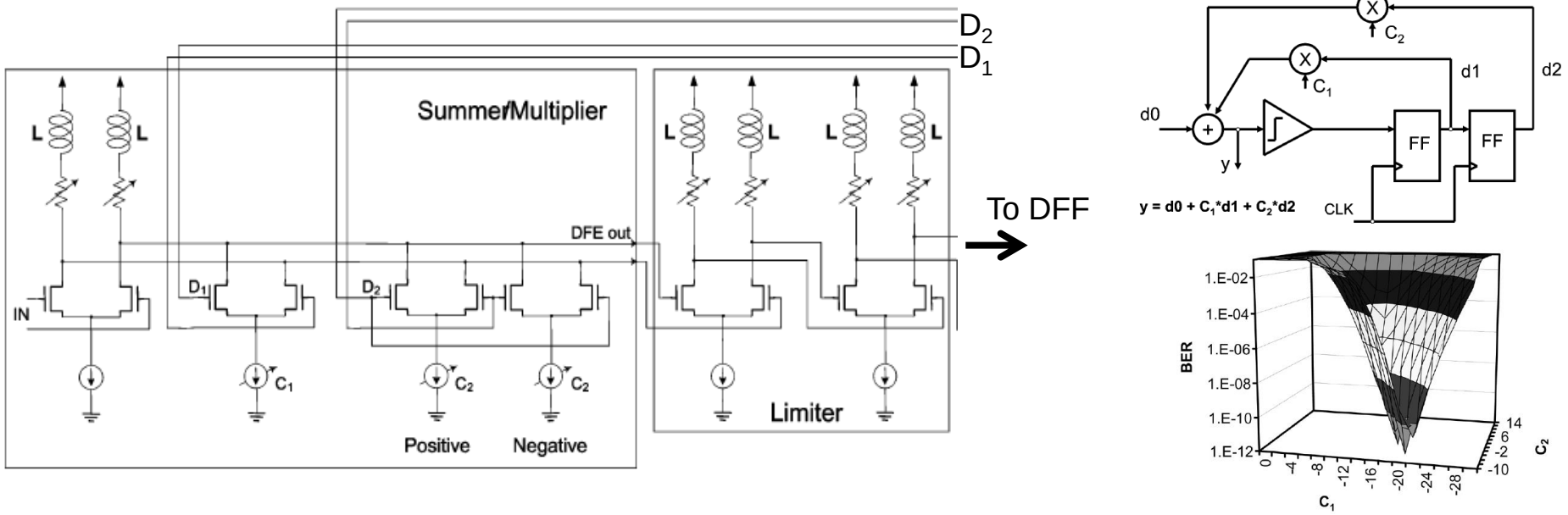
- The DFE uses a speculative approach for the first feedback tap & dynamic feedback for taps two through five
- The speculative DFE feedback sums both + and - first feedback tap weights with the received signal
- Both values are then sliced to a binary value
- The correct slicer output is selected by the previously detected data bit value

JSSC 2005: 6.4-Gb/s CMOS SerDes core with FFE and DFE



- The DFE correction is added to the signal by pulling weighed currents from either the +ve/-ve leg of a differential amplifier output using switched current cells
- The tail current sources in the switched current cells set the desired tap weight
- Pass gates are used to XOR(or multiply) the data value with the tap weight sign
- A small amount of capacitive degeneration is used to extend the bandwidth of the summers while minimizing power

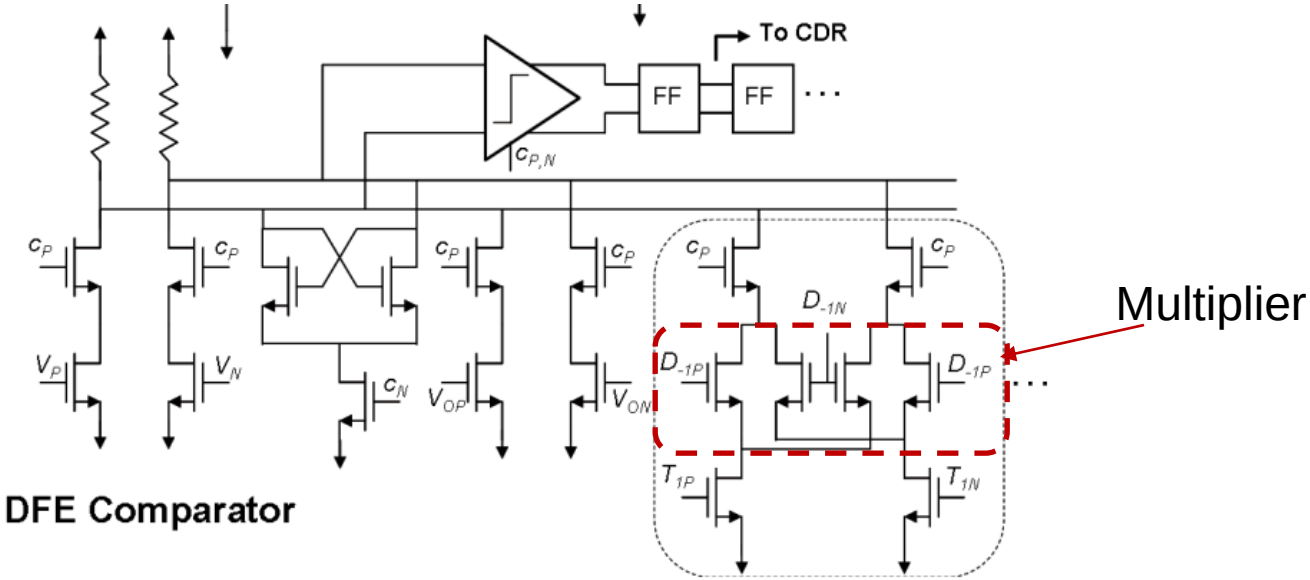
JSSC 2007: 10-Gb/s Receiver With Adaptive Optical Dispersion Equalizer in 0.13-μm CMOS



- Polarity switches are removed from the feedback loop to minimize delay around the DFE loop → higher speed operation
- C_1 is always assumed negative to minimize capacitance at the summation node
- The polarity of C2 can be reversed by switching on/off the appropriate differential pair
- A high gain stage is added before the sampler to increase the eye opening
- The least mean square (LMS) algorithm is used to iteratively update the DFE coefficient

A. Momtaz et al., "A Fully Integrated 10-Gb/s Receiver With Adaptive Optical Dispersion Equalizer in 0.13um CMOS," in IEEE Journal of Solid-State Circuits, vol. 42, no. 4, pp. 872-880, April 2007.

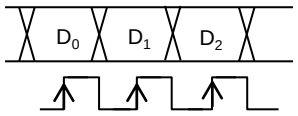
ISSCC 2011: multi-standard-compliant transceiver in 40nm digital CMOS technology



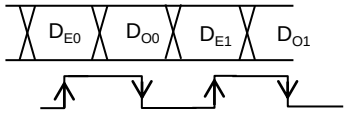
- DFE comparators can use a common-source topology to allow operating from a low supply voltage
- An identical branch is added for comparator offset cancelation
- DFE tap branches use a scaled version of the main comparator: tap 1 branch being ½ the main branch, & taps 2 to 5 being ¼ the main branch
- Scaling helps reduce the summing node capacitance & DFE power consumption
- The differential voltage T_{1P}-T_{1N} determines the DFE tap weight

M. Ramezani et al., "An 8.4mW/Gb/s 4-lane 48Gb/s multi-standard-compliant transceiver in 40nm digital CMOS technology," 2011 IEEE International Solid-State Circuits Conference, 2011, pp. 352-354.

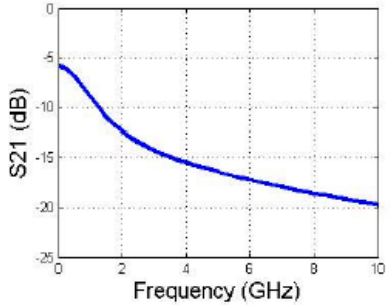
ISSCC 2009: Serial I/O with DFE-IIR Equalization

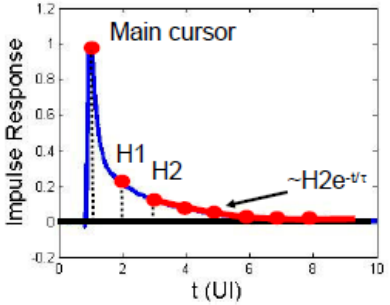


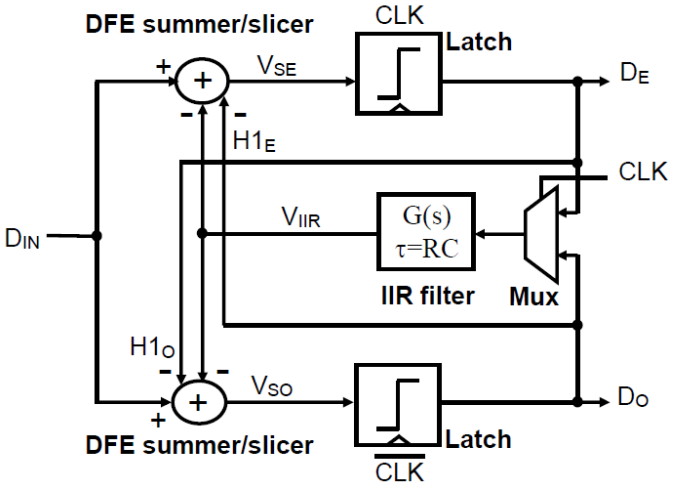
Full rate CDR $T_{clk}=T_b$



Half rate CDR $T_{clk}=T_b/2$



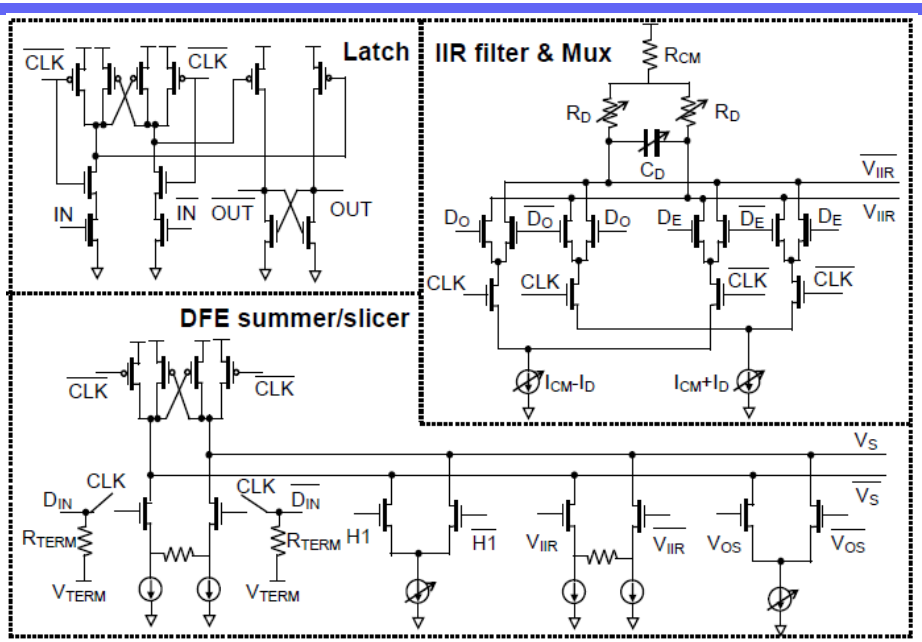




- Half rate DFEs/CDRs allow operating the VCO at ½ the data rate at the expense of using 2 DFE samplers (Even & ODD)
- For Channels with a very long tail, A DFE requires many taps to be effective (power and area penalty)
- 1st DFE tap (H1) is feed back directly to cancel the large first ISI post-cursor
- The two half-rate outputs are multiplexed and fed back to a full-rate CT-IIR filter G(s)
- G(s) matches the exponentially decaying tail of the channel impulse response using a single feedback tap

Yong Liu, Byungsub Kim, T. O. Dickson, J. F. Bulzacchelli and D. J. Friedman, "A 10Gb/s compact low-power serial I/O with DFE-IIR equalization in 65nm CMOS," 2009 IEEE International Solid-State Circuits Conference - Digest of Technical Papers, 2009, pp. 182-183.

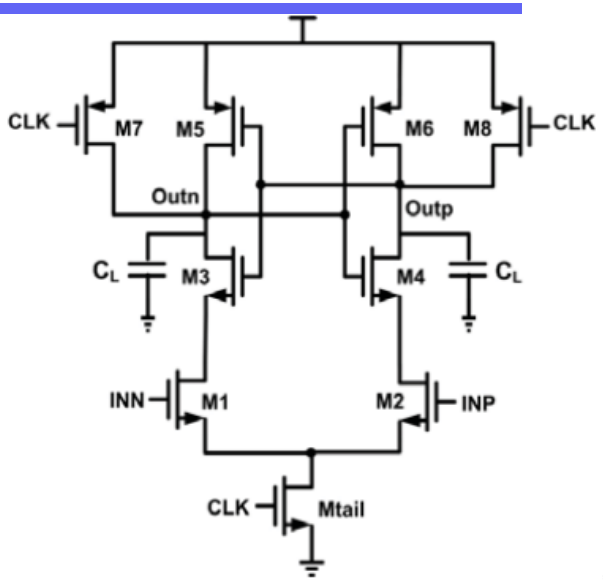
ISSCC 2009: Serial I/O with DFE-IIR Equalization

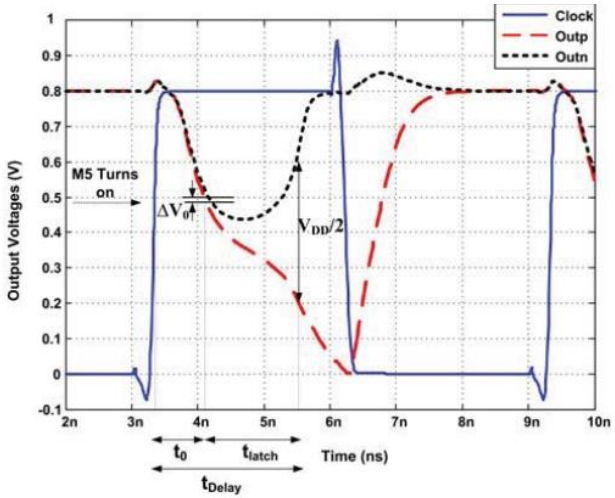


- The integrating summer output current is injected into a resettable PMOS latch
- The output of the merged summer/slicer stage is further regenerated by a two-stage latch
- The CT-IIR filter with integrated MUX adopts a fully differential structure
- G(s) has adjustable time-constant via changing R_D & C_D, & amplitude via I_D & R_D
- The IIR filter output is fed to a G_m that is matched to the input G_m
- An additional G_m is added for comparator offset cancelation
- Clocked Mux provides addition UI delay to start at 2nd tap ISI precursor

STRONG ARM LATCH COMPARATOR

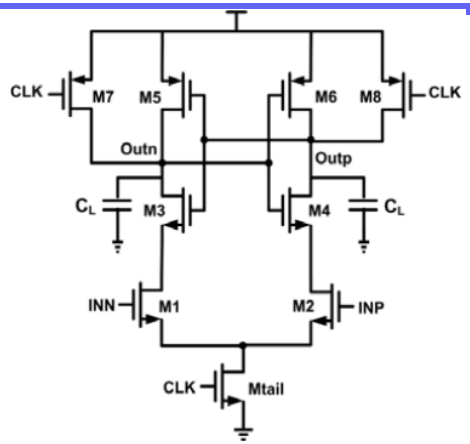
- When (CLK = 0) the comparator operates in the reset phase
- When CLK=V_{DD}, the circuit operates in the regenerative phase M_{tail} turns ON, while $M_{7,8}$ turn OFF
- Output voltages (Outp, Outn), which were pre-charged to VDD, start to discharge with different discharging rates depending on the corresponding input voltage (INN/INP)
- Assuming $V_{INP} > V_{INN}$, Outp discharges faster than Outn
- Hence Outp, falls down to $V_{DD}-|V_{thp}|$ before Outn, M5 will turn on initiating the latch regeneration caused by back-to-back inverters (M3-M6)
- Outn pulls to VDD and Outp discharges to ground

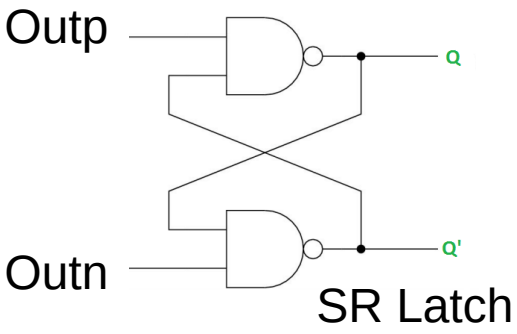




S. Babayan-Mashhadi and R. Lotfi, "Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 2, pp. 343-352, Feb. 2014.

STRONG ARM LATCH COMPARATOR

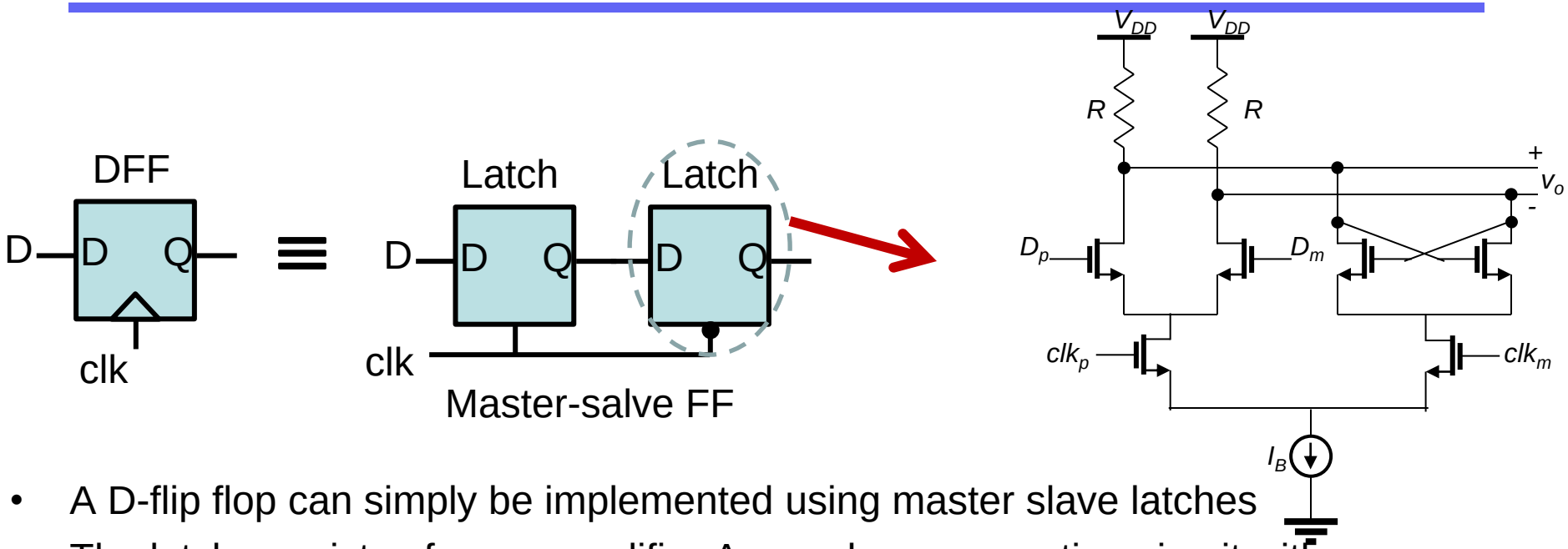




- Needs to be followed by an R-S latch to form a D-flip flop
- RS latch holds output data during latch pre-charge phase (CLK=0)
- Strong-Arm flip-flop has the advantage of no static power dissipation and full CMOS output levels
- M_1 and M_2 are usually the dominant contributors to the comparator mismatch
- The Strong ARM latch draws high transient currents from the supply
- Differential Kickback current appears at the input due to the unequal rate of drop of the latch outputs which couples to the inputs through C_{GDMN1} & C_{GDMN2}
- CM kickback noise currents is a lot worse due to the turn ON/OFF of Mtail which couples the CLK to the inputs through $C_{GDMtail}$ & $C_{GSMN1,2}$

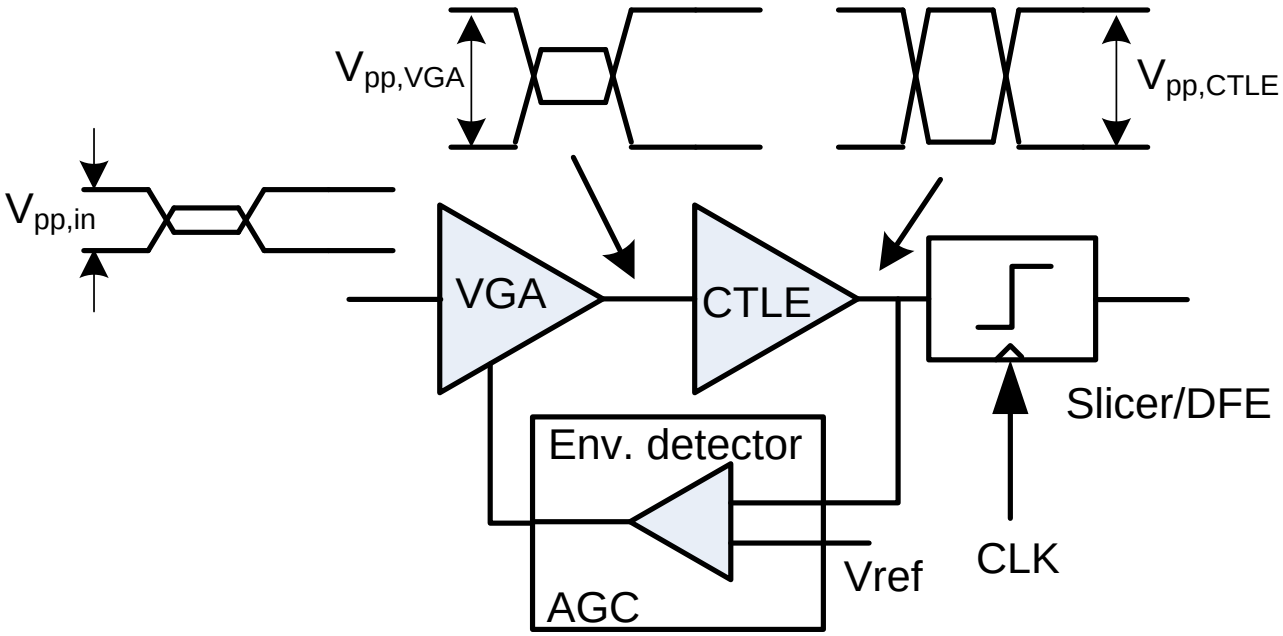
B. Nikolic, V. G. Oklobdzija, V. Stojanovic, Wenyan Jia, James Kar-Shing Chiu and M. Ming-Tak Leung, "Improved sense-amplifier-based flip-flop: design and measurements," in IEEE Journal of Solid-State Circuits, vol. 35, no. 6, pp. 876-884, June 2000.

High-Speed CML Samplers/Flip-Flops



- A D-flip flop can simply be implemented using master slave latches
- The latch consists of a pre-amplifier A_{pre} and a regeneration circuit with a re-generation time constant τ_{reg}
- In track mode, clk is high and the output tracks the input with a gain A_{pre}, if input large enough the output will saturate at $v_{o\text{-}p}=V_F=I_BR$
- In the latch (regeneration) mode, the positive feedback results in an exponential increase in the output $v_o \propto v_{initial}\exp(+t/\tau_{reg})$
- Until the current is fully steered and $v_{o\text{-}p}=V_F=I_BR$

Automatic Gain Control Loop



- The AGC loop is responsible for adjusting the VGA gain to achieve a constant swing at either the VGA or CTLE output
- It consists of an envelope detector which compares the long-term average peak-to-peak swing of the signal with a reference generated from the band-gap
- The AGC loop has a slow response, so even if it encountered an under equalized eye it rejects the HF information and will only see the outer eye peak-to-peak
- During boost calibration, if the CTLE DC gain changes the AGC loop must be allowed enough time to adjust the signal amplitude

DFE Tap weight Adaptation

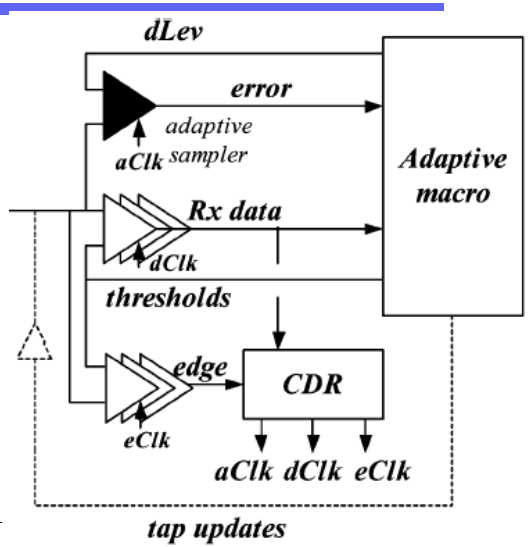
- Adaptive algorithms for DFE tap weights:
  - Sign-sign LMS is typically used (derivative of the well-known least-mean square (LMS) algorithm)
  - Sign based zero forcing (ZF)
- An extra sampler is added for adaptation using SS-LMS
- Updates for the tap coefficients are based only on the sign of the data and the measured error

$$T_{n+1}^{k} = T_{n}^{k} + \mu \; x \; sign(e_n) \; x \; sign(y_{n-k})$$

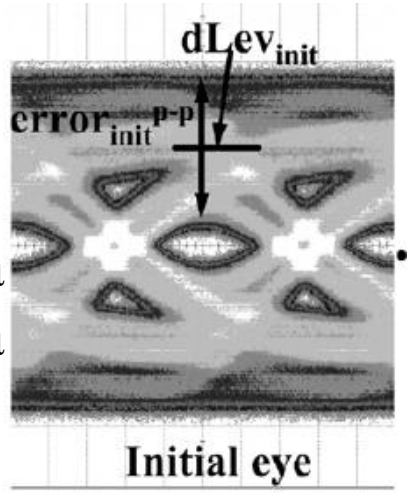
where n is the time instant, k is the tap index, μ is the adaptation loop gain

- y_n is the received data and e_n is the error of the received signal with respect to the desired data level dlev

$$e_n = x_c(n) - dlev \quad \text{if} \quad x_c(n)>0$$



- For any **X01** transition if e_n is -ve (under-equalized) T^1 increments by μ
- For any **0X1** transition if e_n is -ve (under-equalized) T^2 increments by μ



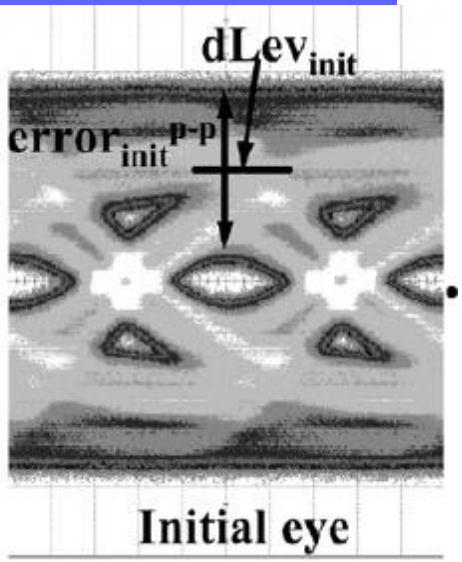
V. Stojanovic et al., "Autonomous dual-mode (PAM2/4) serial link transceiver with adaptive equalization and data recovery," in IEEE Journal of Solid-State Circuits, vol. 40, no. 4, pp. 1012-1026, April 2005.

DFE Tap weight Adaptation (Cont'd)

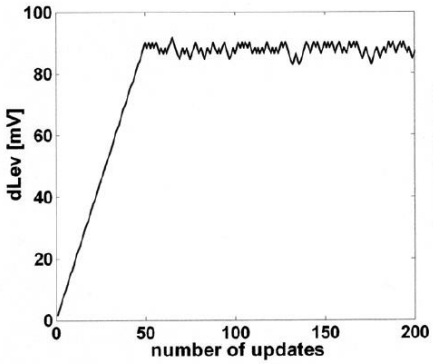
- dlev can be detected using an analog peak detector or a second loop can be created to track the signal level dlev

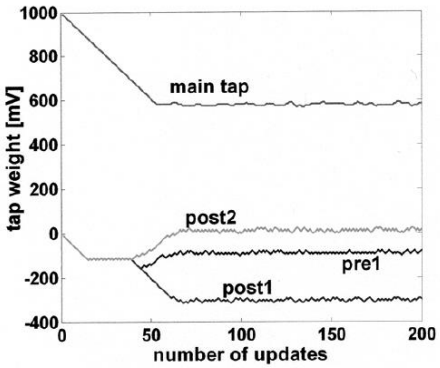
$$dlev_{n+1} = dlev_n + \mu \; x \; sign(e_n)$$

$$e_n = x_c(n) - dlev \quad \text{if} \quad x_c(n)>0$$



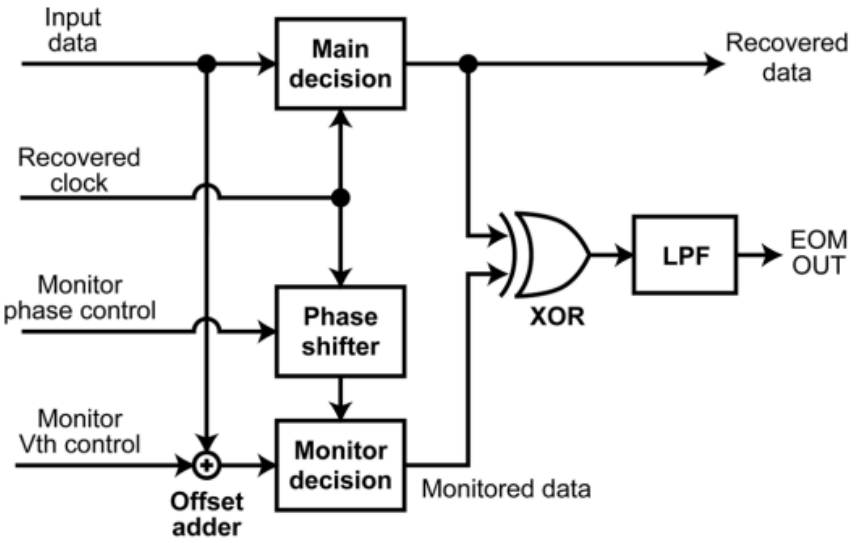
- For any **1** transition if e_n is +ve *dlev* increments by μ
- For any **1** transition if e_n is -ve *dlev* decrements by μ
- Typically, the *dlev* adaptation loop should settle first before the DFE tap weights start adaptation
- Depending on the DFE implementation the value of dlev might need to be re-adjusting for each change in the tap weights
- Dlev can also be used by the AGC for VGA gain control





On-chip Eye Opening Monitor (EOM)

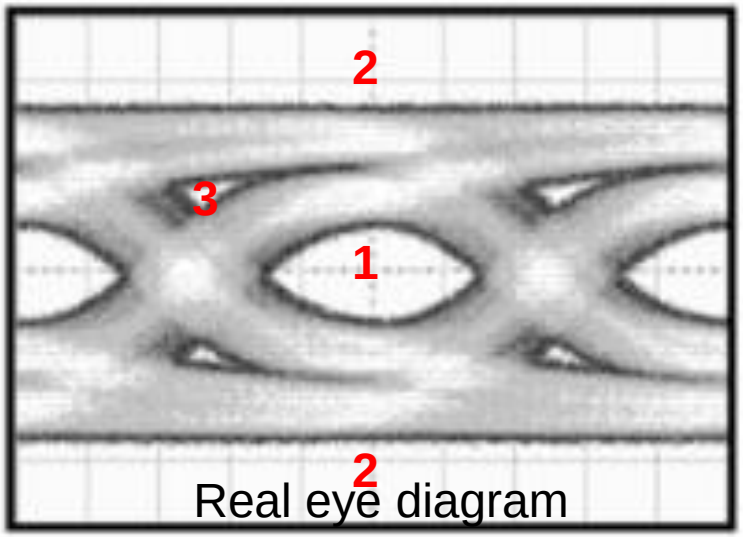
- Integrating an on-chip eye opening monitor (EOM) gives valuable information that can be used for:
  - Adjusting CDR sampling point
  - Optimizing Rx CTLE/DFE equalization
- EOM can be created by the same sampler used for DFE tap adaptation
- Sampler needs to have both variable voltage timing offsets



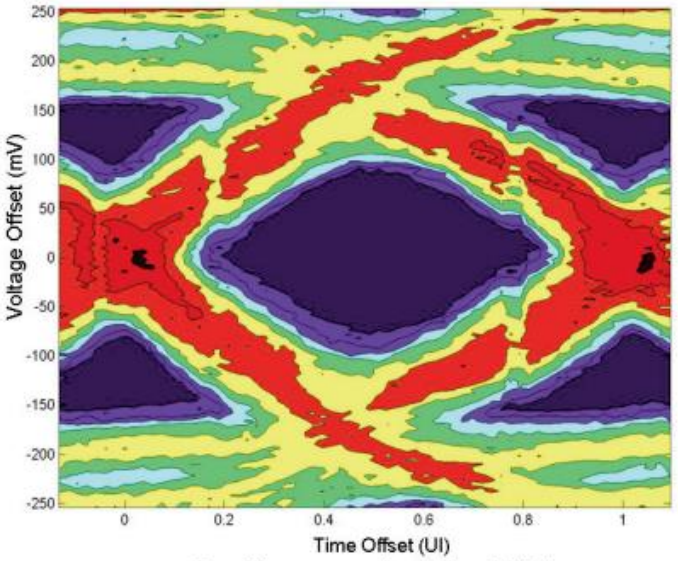
- The output of this sampler is compared with the main data sampler via an XOR and the BER can be calculated by accumulating the number of errors
- The voltage and timing offset of the monitor comparator are swept to produce a 2-D plot for BER

H. Noguchi, N. Yoshida, H. Uchida, M. Ozaki, S. Kanemitsu and S. Wada, "A 40-Gb/s CDR Circuit With Adaptive Decision-Point Control Based on Eye-Opening Monitor Feedback," in IEEE Journal of Solid-State Circuits, vol. 43, no. 12, pp. 2929-2938, Dec. 2008.

On-chip Eye Opening Monitor (EOM)



Real eye diagram



On-chip eye monitor after CTLE

- If the samples of both comparators are in:
  - Region (1), the XOR outputs a “LOW” → low BER
  - Region (2), the XOR outputs a very high BER of 0.5 (assuming 1s and 0s are equally probable)
  - Region (3), the XOR outputs a BER of 0.25
  - The gradient of the 2-D BER plot provides a re-created eye diagram using the on-chip eye monitor

M. Ramezani et al., "An 8.4mW/Gb/s 4-lane 48Gb/s multi-standard-compliant transceiver in 40nm digital CMOS technology," 2011 IEEE International Solid-State Circuits Conference, 2011, pp. 352-354.

LV-OIF-11G-SR Receiver specifications (JESD204B standard)

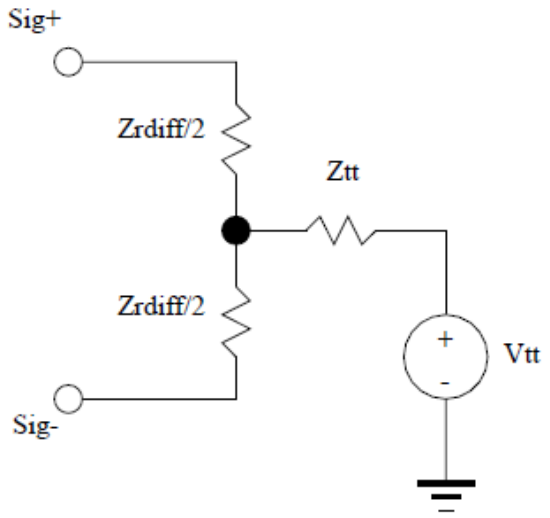


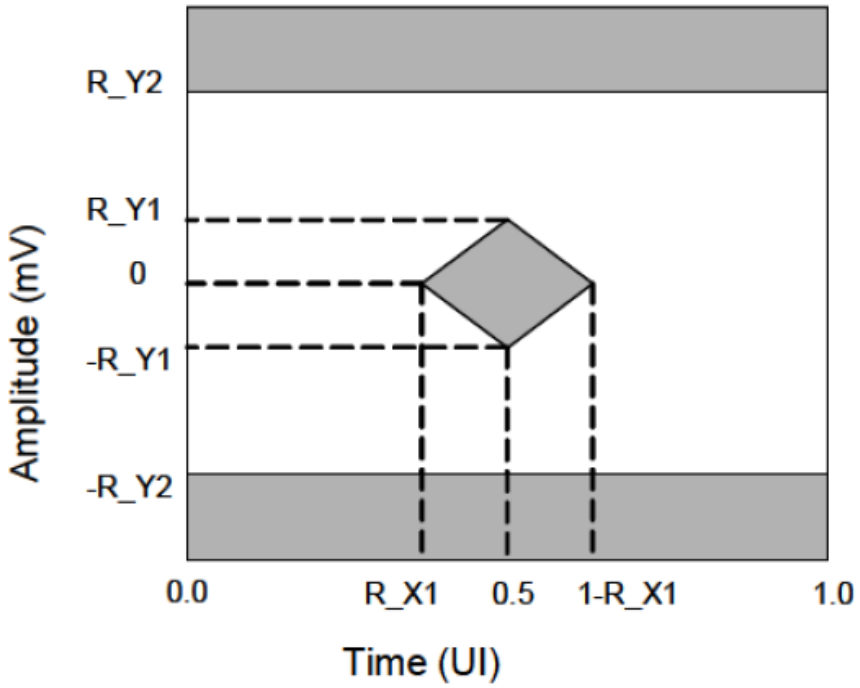
Figure 5 — Line termination at Receiver

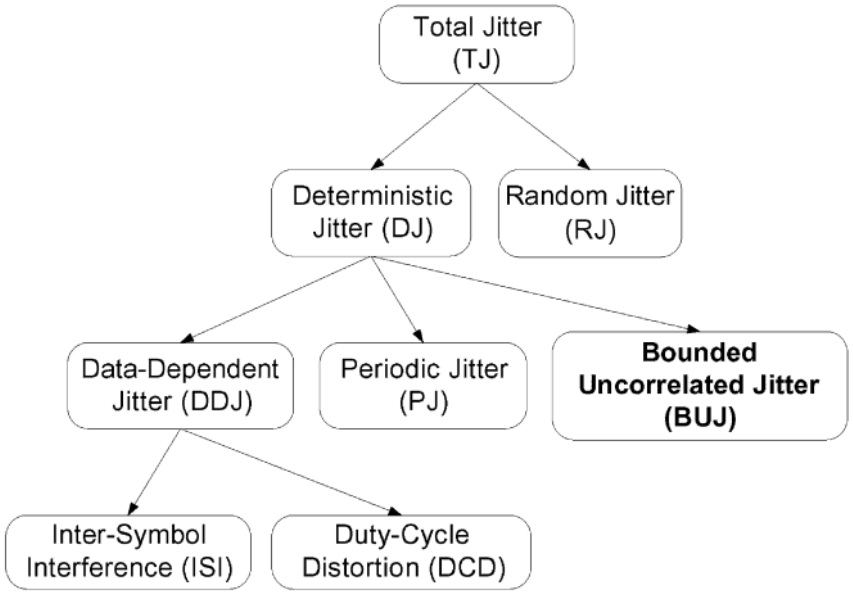
Table 7 — General Differential Input DC and AC Characteristics for LV-OIF-11G-SR – based operation

Symbol	Parameter	Conditions	Min	Max	Units
Vtt	Termination Voltage	Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 1).	1.2 – 8%	1.2 + 5%	V
		Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 2).	1.0 – 8%	1.0 + 5%	V
		Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 3).	0.8 – 8%	0.8 + 5%	V
Vrcm	Input Common Mode Voltage	Applies only to AC coupling	-0.05	1.85	V
		Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 1).	720	Vtt – 10	mV
		Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 2).	535	Vtt + 125	mV
		Required only if DC-compliance is claimed. Line Termination circuit of Figure 5 with parameters as per (Note 3).	475	Vtt + 105	mV
R_Vdiff	Input Differential Voltage		110	1050	mVppd
Ztt	Vtt Source Impedance	At DC.	-	30	Ω
Zrdiff	Receiver Differential Impedance	At DC.	80	120	Ω
RLrdiff	Differential Input Return Loss	From 100 MHz to 0.75*baud rate relative to 100Ω.	8		dB
RLrcm	Common Mode Input Return Loss	From 100 MHz to 0.75*baud rate relative to 100Ω.	6		dB

NOTE 1 Vtt = 1.2V Nominal
NOTE 2 Vtt = 1.0V Nominal
NOTE 3 Vtt = 0.8V Nominal

LV-OIF-11G-SR Receiver specifications (JESD204B standard)





R_X1 (UI)	1-R_X1 (UI)	R_Y1 (V)	R_Y2 (V)	R_SJ-hf (p-p UI)	R_SJ-max (p-p UI)	R_BHPJ (p-p UI)	TJ (p-p UI)
0.35	0.65	0.055	0. 525	0.05	5	0.45	0.70

NOTE 1 R_SJ-hf = Receive Sinusoidal Jitter, High Frequency
NOTE 2 R_SJ-max = Receive Sinusoidal Jitter, Maximum
NOTE 3 R_BHPJ = Receive Bounded High Probability Jitter – Breakdown is 0.25 UIpp Uncorrelated, 0.20 UIpp Correlated
NOTE 4 R_X1 = TJ / 2.
NOTE 5 Unit Interval (UI) is specified in Table 6. However, for baud-rates greater than 11.1 Gsym/sec, UI shall be 90.09ps.
NOTE 6 Total Jitter (TJ) includes high-frequency sinusoidal jitter (R_SJ-hf)
NOTE 7 The Gaussian Jitter (GJ) portion of the Total Jitter (TJ) is defined with respect to a BER of 1e-15 (Q=7.94).