ECE 621
Signaling and Synchronization
Fall 2020

Topic 6
Timing Basics

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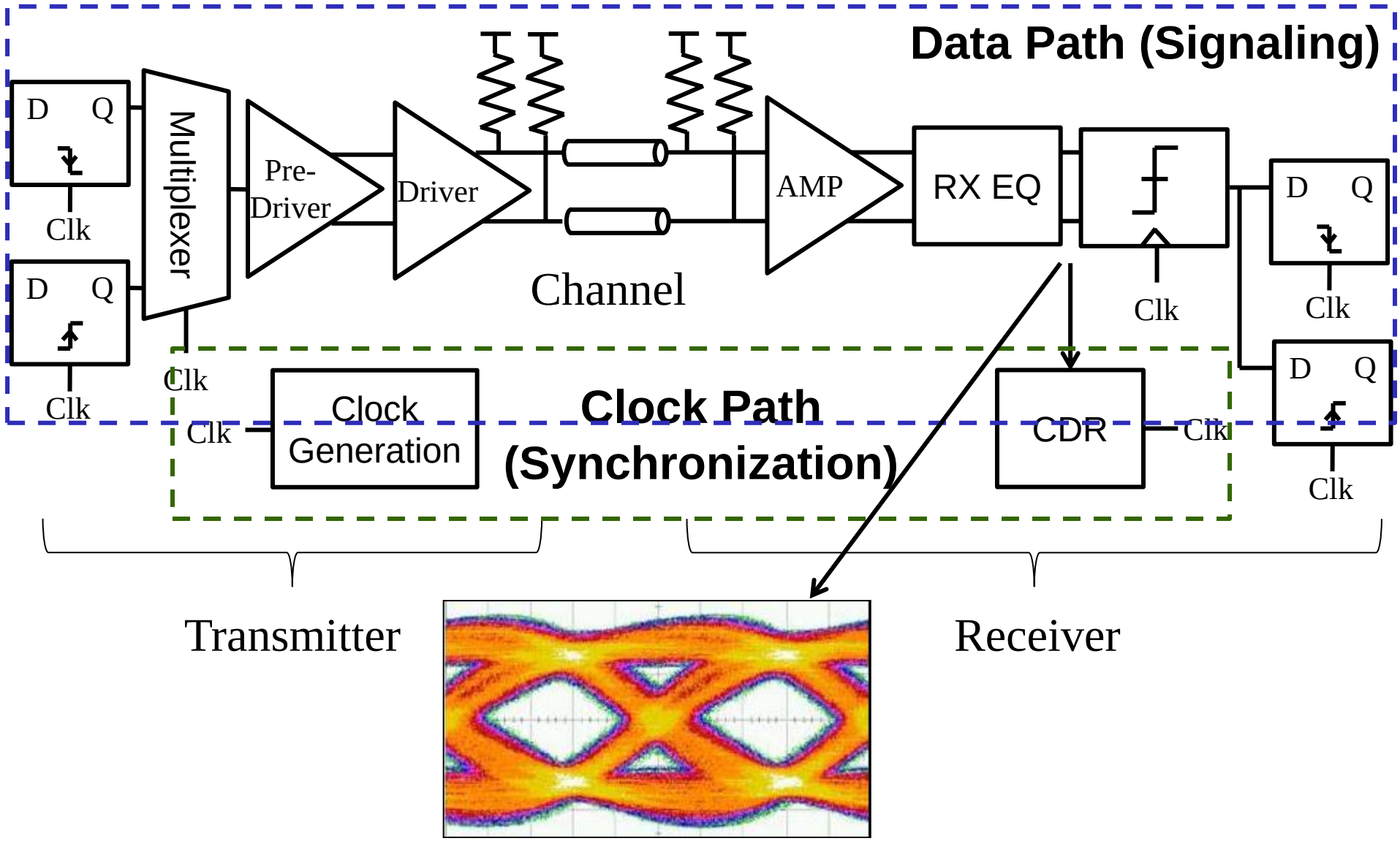
ICL

(Courtesy of S. Pamarti & K. Yang – UCLA, S. Palermo – TAMU, and E. Alon – UCB)

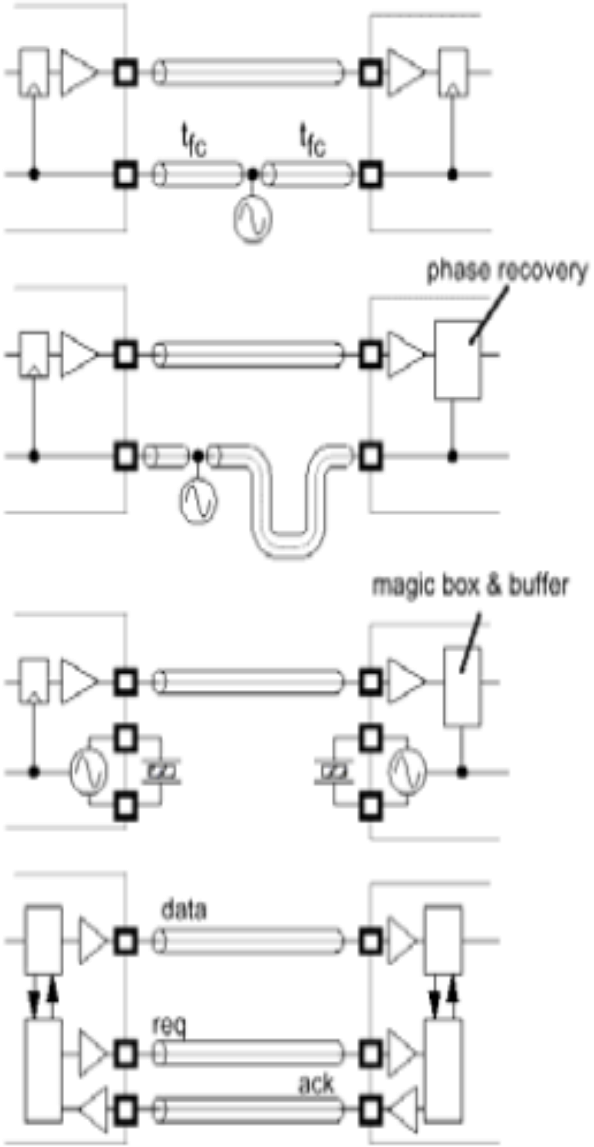
Outline

- **Clocking Types**
  - Common Clock
  - Forwarded Clock
  - Embedded Clock
- **Jitter Analysis**
  - Jitter Definitions
  - Jitter Categories
  - Dual Dirac Jitter Model
  - System Jitter Budgeting

The Need for Synchronization



Clocking Types



- **Synchronous**
  - Every Participant gets same frequency and phase.
  - Conventional busses, memories
- **Mesochronous**
  - Every participant gets same frequency but unknown phase. Requires a way to recover the phase.
  - Fast memories/busses, interconnection networks
- **Plesiochronous**
  - Every participant gets nearly the same frequency, slowly drifting phase. CDR needed
  - Widely used in high-speed links
- **Asynchronous**
  - Dispense with clocks altogether, use (e.g.) request/acknowledge 4-phase handshake to ensure correct sequencing of events.
  - Embedded systems

I/O Clocking Architectures

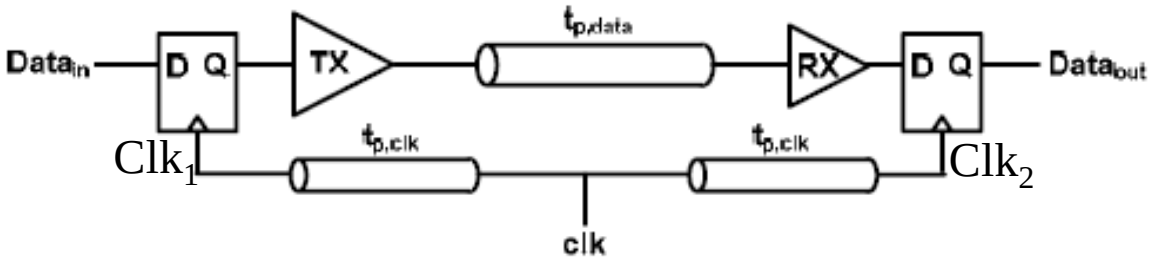
- **Three basic I/O architectures**
  - Common Clock (Synchronous)
  - Forwarded Clock (Source Synchronous)
  - Embedded Clock (Clock Recovery)

- **These I/O architectures are used for varying applications that require different levels of I/O bandwidth.**

- **A processor may have one or all of these I/O types,**

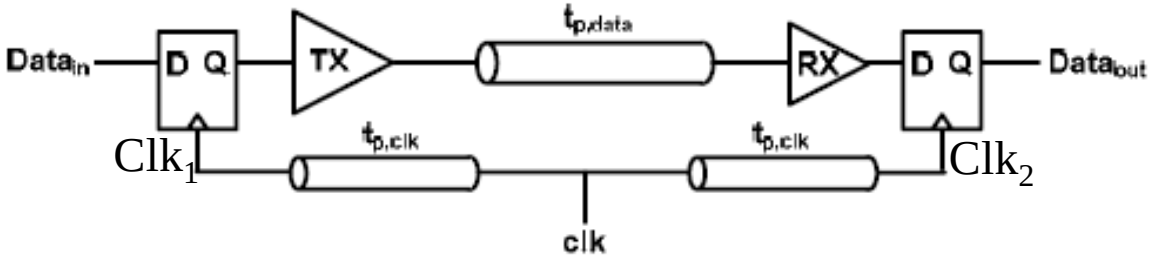
- **Often the same circuitry can be used to emulate different I/O schemes for design reuse.**

Synchronous Clocking Challenges

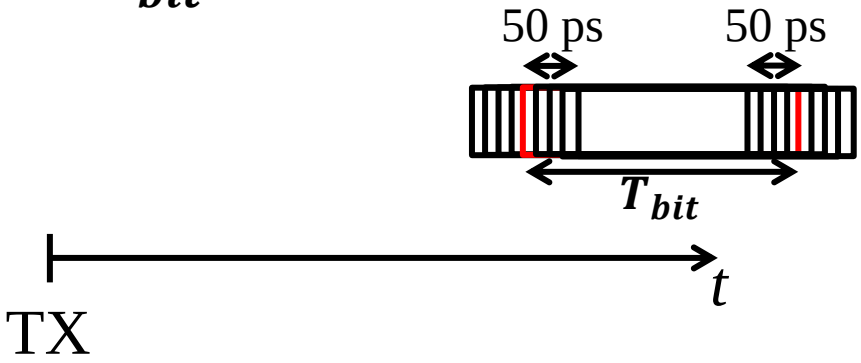


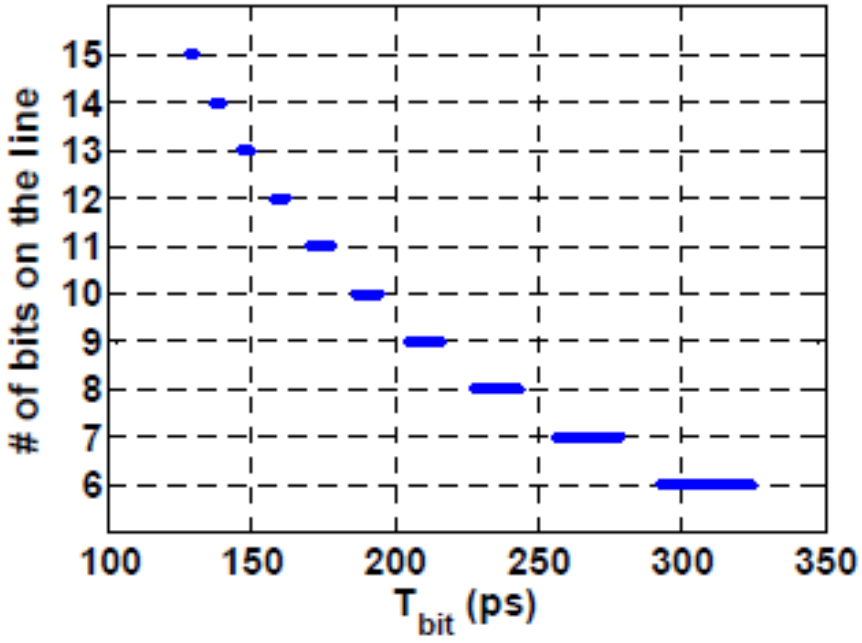
- $t_{cq} + t_{TX} + t_{p,data} + t_{RX} + t_{setup} < T_{bit} \rightarrow$ **Large T_{bit}**
- **This is wrong as we actually have multiple bits on line ($t_{p,data}/T_{bit}$)**
- **Factors affecting correct sampling by Clk_2**
  - Clock Skew
  - Clock Jitter
  - Waveform shape

An Example



- $t_{p,data} = 2ns, t_{cq} + t_{TX} + t_{RX} + t_{setup} = 0$
- **Assume square bits and $t_{skew+jitter} = \pm 50ps$**
- T_{bit} **= ?**

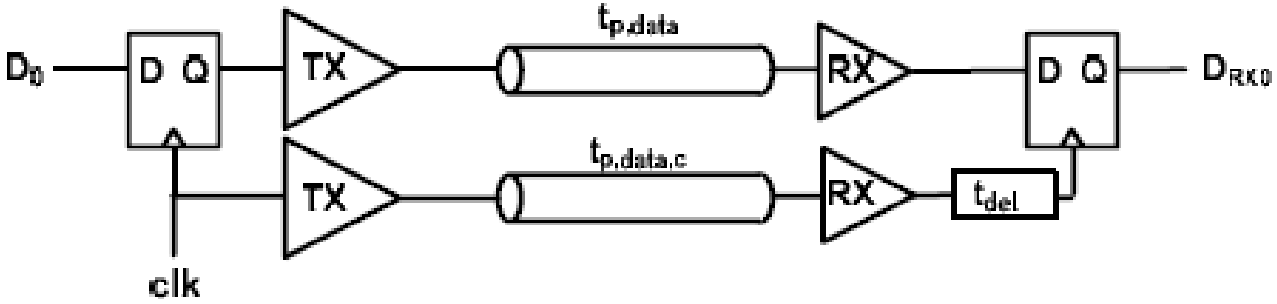




Common Clock I/O Limitations

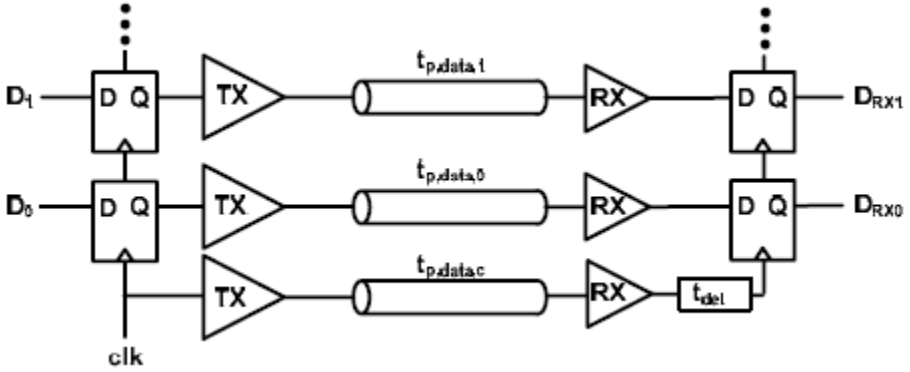
- Difficult to control clock skew and propagation delay
- Need to have tight control of absolute delay to meet a given cycle time
- Sensitive to delay variations in on-chip circuits and board routes
- Hard to compensate for delay variations due to low correlation between on-chip and off-chip delays
- While commonly used in on-chip communication, offers limited speed in I/O applications.

Source Synchronous Clocking

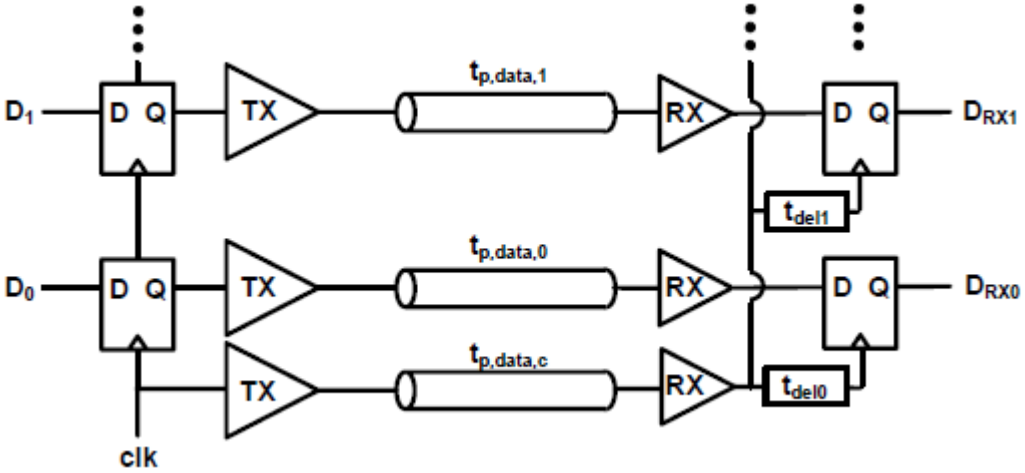


- **Clock is sent along with the data to ease phase recovery.**
- **Falling edge receives data. $t_{del} = \frac{T_{bit}}{2}$.**
- **Key idea is to match clock and data paths.**
- **Don't need a PLL (only recovering phase), DLL is just fine.**

Multiple Source Synchronous Links



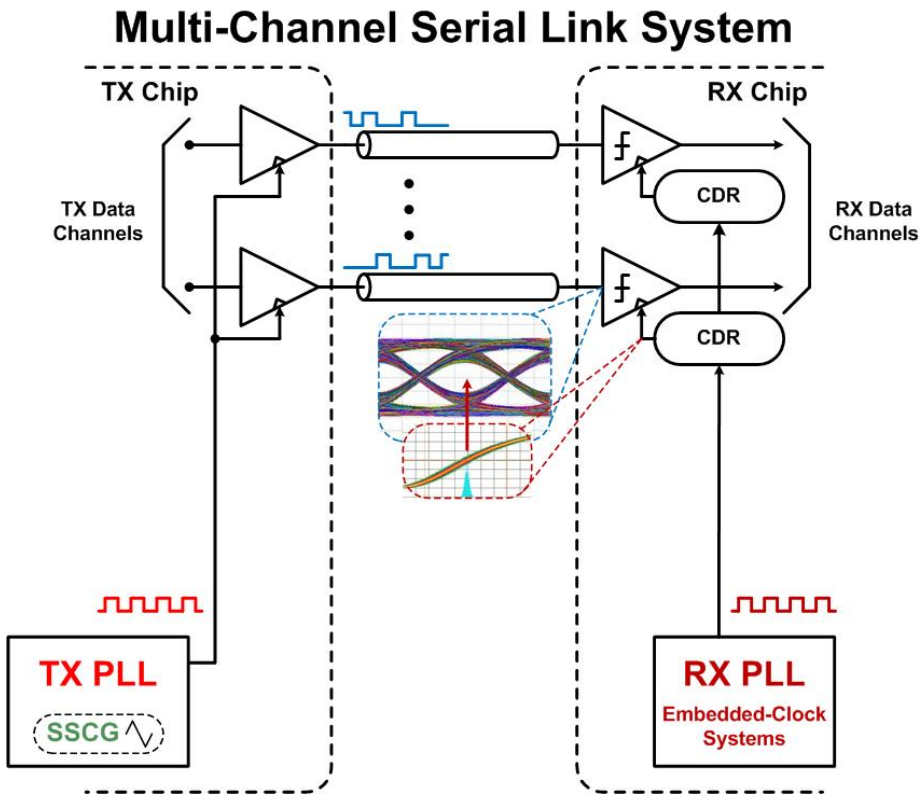
- To reduce overhead, clock link is shared.
- Matching become a problem.



The Use of CDR

- **CDR = Clock and Data Recovery**
  - Recovers clock phase and/or frequency based on data itself.
  - If phase only, needs a frequency reference.
- **Several advantages vs. fixed timing**
  - Don’t have to match delays/paths (mesochronous).
  - Allows separate crystals (plesiochronous).
- **But, CDR isn’t free**
  - And places some requirements on data.

List of Circuits Needed



Spread-Spectrum Clock Generator

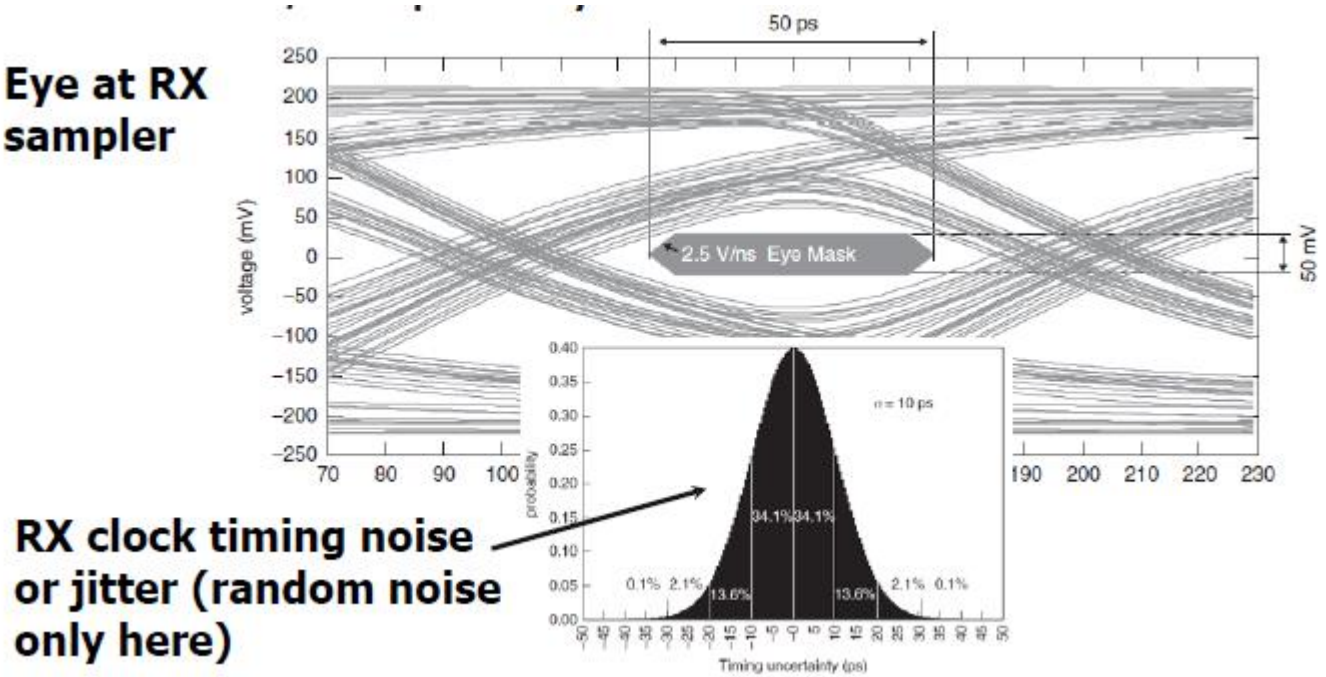
- **TX PLL**
- **TX Clock Distribution**
- **CDR**
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL & Local DLL/PI
  - Local Phase-Rotator PLLs
  - Global PLL requires RX clock distribution to individual channels

Outline

- Clocking Types
  - Common Clock
  - Forwarded Clock
  - Embedded Clock
- **Jitter Analysis**
  - Jitter Definitions
  - Jitter Categories
  - Dual Dirac Jitter Model
  - System Jitter Budgeting

Eye Diagram and Spec Mask

- **Links must have margin in both the voltage AND timing domain for proper operation.**
- **For independent design (interoperability) of TX and RX, a spec eye mask is used.**



Jitter Definitions

- **Jitter can be defined as "the short-term variation of a signal with respect to its ideal position in time"**
- **Jitter measurements**
  - Period Jitter (J_{PER})
    - Time difference between measured period and ideal period
    - The easiest and most direct measurement to make
  - Cycle to Cycle Jitter (J_{CC})
    - Time difference between two adjacent clock periods
    - Of interest because it shows the instantaneous dynamics a clock-recovery PLL.
  - Accumulated Jitter (J_{AC}) (Time Interval Error TIE)
    - Time difference between measured clock and ideal trigger clock
    - For this measurement to be performed, the ideal edges must be known or estimated.
    - It shows the cumulative effect that even a small amount of period jitter can have over time.

Jitter Statistical Parameters

- **Mean Value**
  - Can be interpreted as a fixed timing offset or “skew”.
  - Generally not important, as usually can be corrected for.
- **RMS Jitter**
  - Useful for characterizing random component of jitter
- **Peak-to-Peak Jitter**
  - Function of both deterministic (bounded) and random (unbounded) jitter components
  - Must be quoted at a given BER to account for random (unbounded) jitter

Deterministic jitter (DJ)

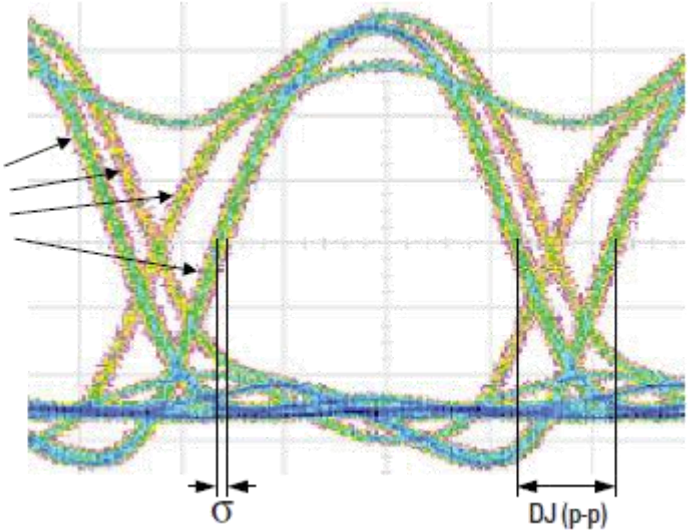
Determines the trajectory of each logic transiton

DJ (p-p)

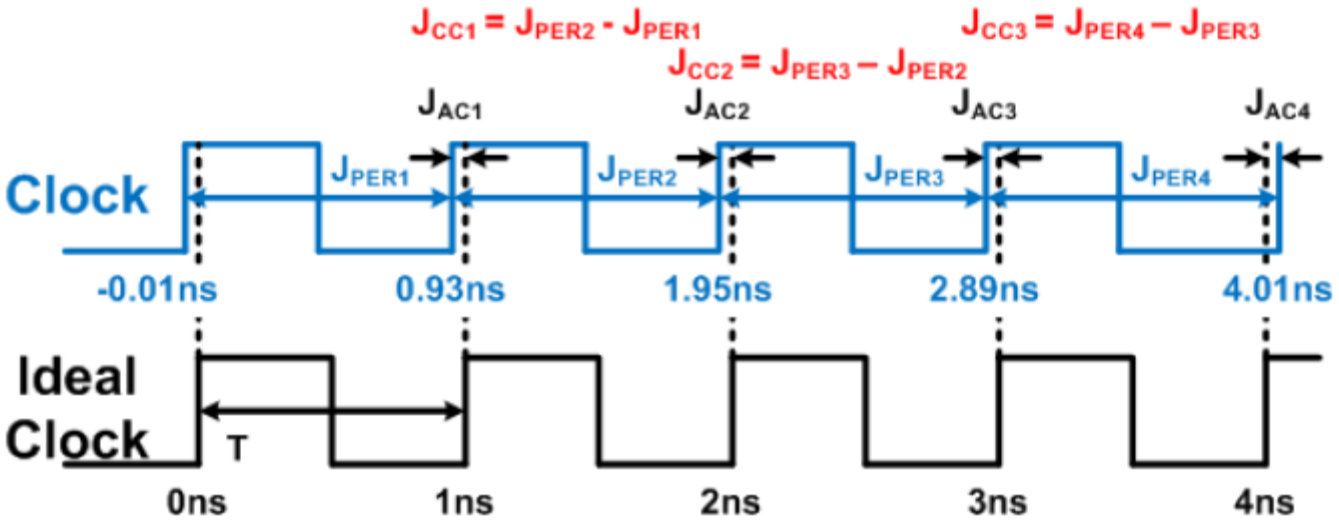
Random jitter (RJ)

Smears each trajectroy according to the same Gaussian distribution

σ



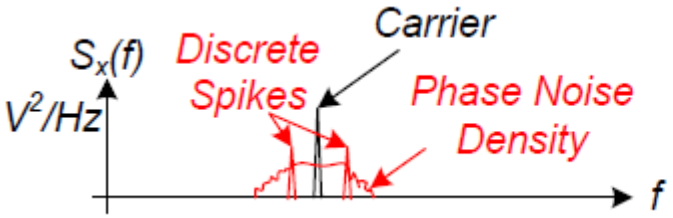
Jitter Calculation Examples



n	1	2	3	4	Mean	RMS	PP
J_{PER}	-0.06	0.02	-0.06	0.12	0.005	0.085	0.18
J_{CC}	0.08	-0.08	0.18	-	0.06	0.131	0.26
J_{AC}	-0.07	-0.05	-0.11	0.01	-0.055	0.05	0.12

- **J_{PER} = time difference between measured period and ideal period**
- **J_{CC} = time difference between two adjacent clock periods**
- **J_{AC} = time difference between measured clock and ideal trigger clock**

Phase Noise



$$x(t) = A\cos\left(\omega_0 t + \phi(t)\right)$$

- **Widely used in wireless communication circuit design**
- **$\emptyset(t)$ is the phase noise**
  - Measured indirectly by measuring the power spectrum of x(t).
  - Spectrum analyzers or dedicated phase noise measurement equipment are used.
- Low noise assumption → |Φ(t)| << 2π

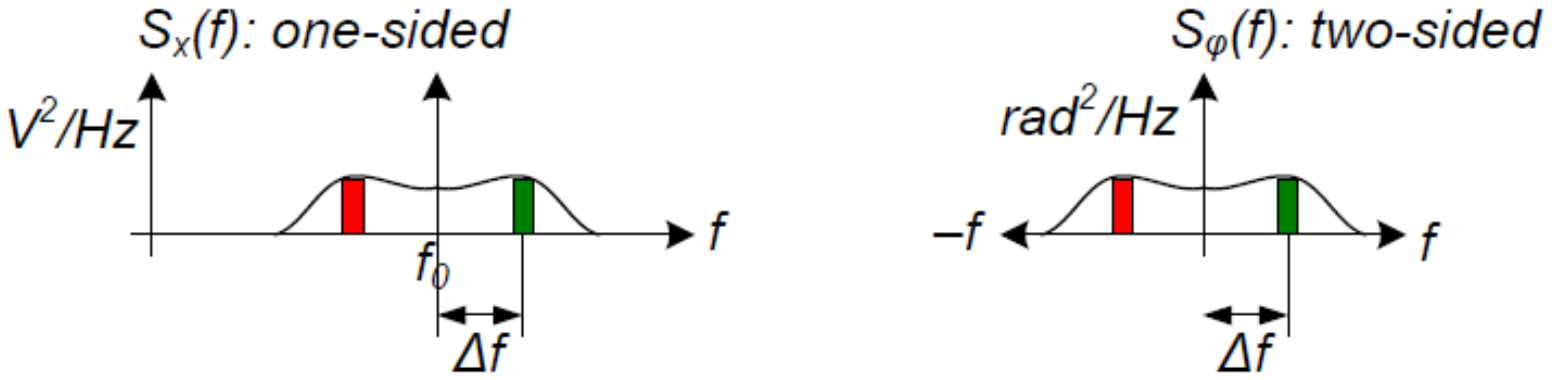
$$x(t) \approx A\cos(\omega_0 t) - \phi(t) A\sin(\omega_0 t)$$

$$S_x^{(1)}(f) = A^2\pi\delta\left(2\pi f - 2\pi f_0\right) + \frac{A^2}{2} S_\phi^{(2)}\left(f - f_0\right)$$

One-sided PSD

Two-sided PSD

Phase Noise PSD

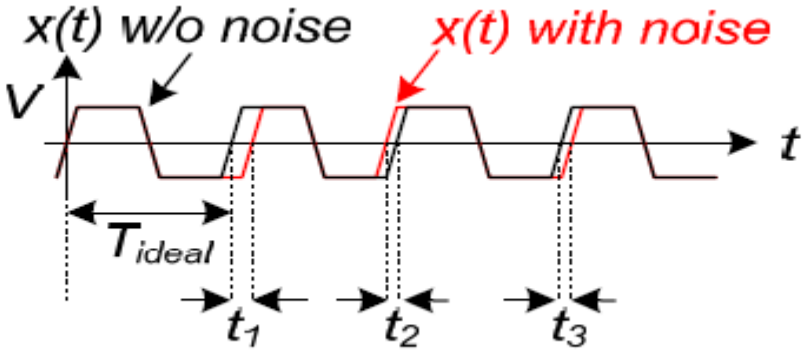


$$L(f_0 + \Delta f) \triangleq 10 \log_{10} \left| \frac{\text{Power of } x(t) \text{ in } 1Hz \text{ at } f_0 + \Delta f}{\text{Power of carrier}} \right|$$

$$= 10 \log_{10} S_\phi^{(2)}(\Delta f) \ \frac{dBc}{Hz}$$

Important Note: The PSD of the phase noise is two-sided in this expression

Phase Noise and Jitter



$$x(t) = \mathrm{sgn}\left(\cos\left(\omega_0 t + \phi(t)\right)\right)$$

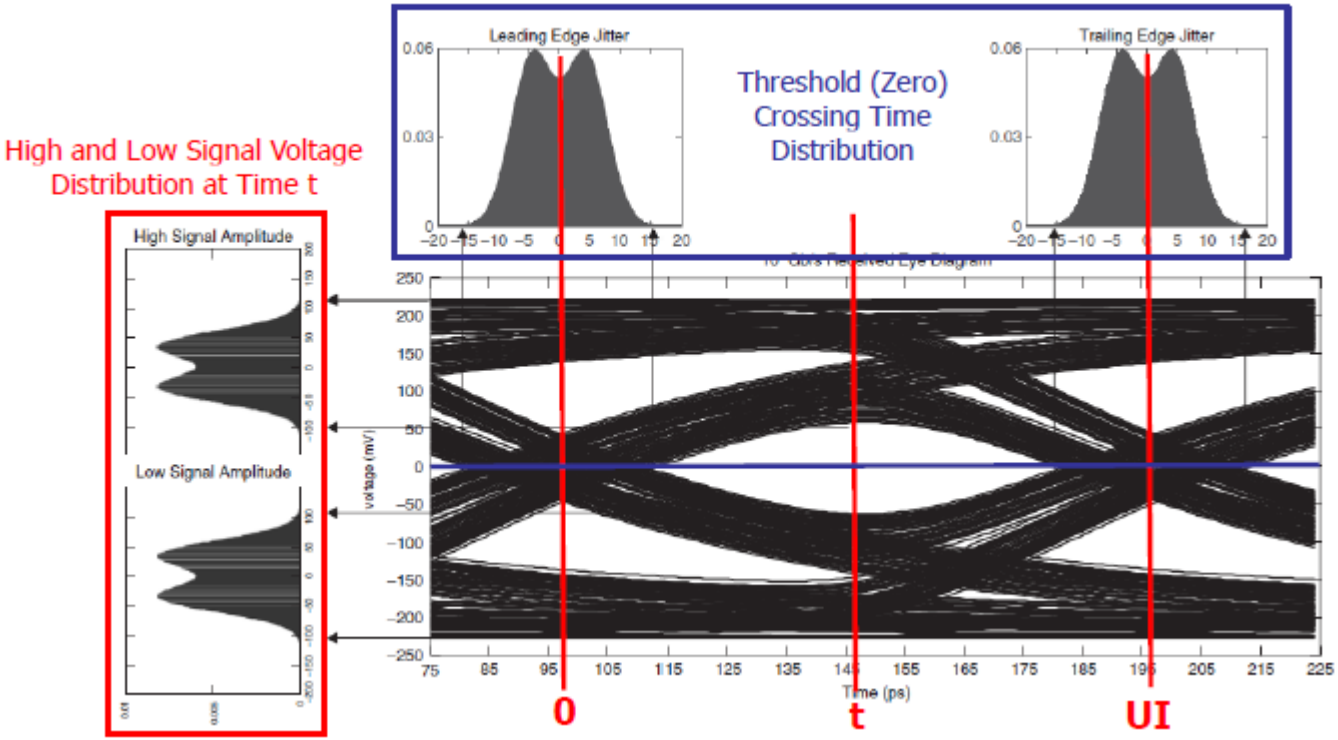
$$t_n \approx -\left(\frac{\phi(nT_{ideal})}{2\pi}\right) T_{ideal},$$

$$\text{where } T_{ideal} = \frac{2\pi}{\omega_0}$$

- **Jitter is a scaled, sampled version of the phase noise.**
  - The phase noise is small: $|\Phi(t)| << 2\pi$
  - The phase noise does not change too much over t_n

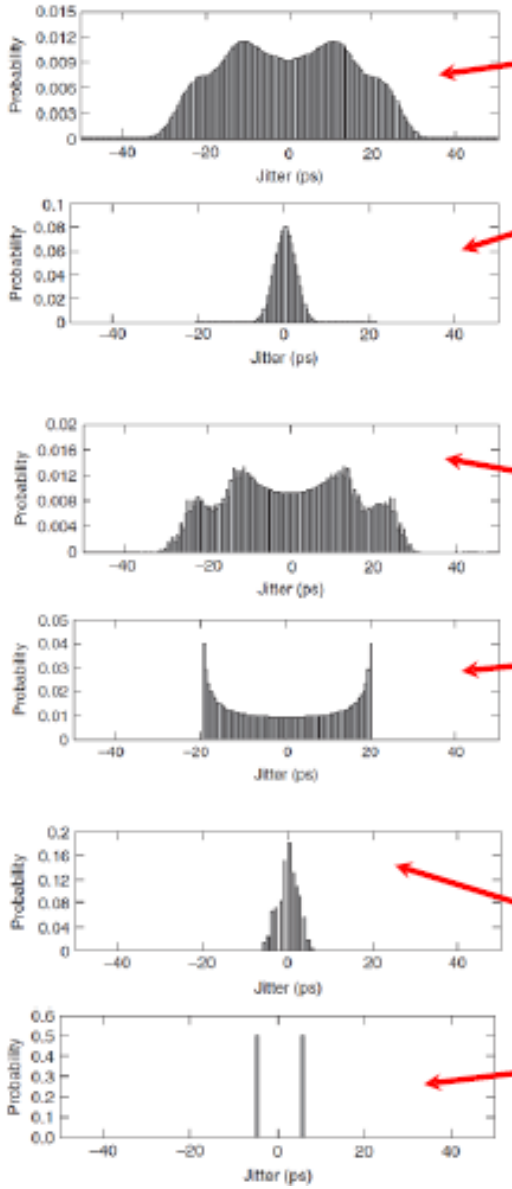
- **Often, we're only concerned about the mean, root mean square (r.m.s.) and peak-to-peak values of jitter.**

Jitter Histogram



- **Used to extract the jitter PDF**
- **Consists of both deterministic and random components**
- **Need to decompose these components to accurately estimate jitter at a given BER**

Jitter Categories



Total Jitter

Random Jitter (RJ)

Characteristics
- Unbounded, Gaussian distributed
- Key parameters: $\mu = 0$, σ_{RMS}
- Sources: Device noise (shot, flicker, thermal)

Deterministic Jitter (DJ)

Characteristics
- Bounded, peak-to-peak
- Key parameters: Maximum pk-pk jitter
- Sources: Losses, reflections, t_r/t_f mismatch, spread spectrum clocking, crosstalk

Sinusoidal Jitter (SJ)

Data Dependent Jitter (DDJ)

Intersymbol Interference (ISI)

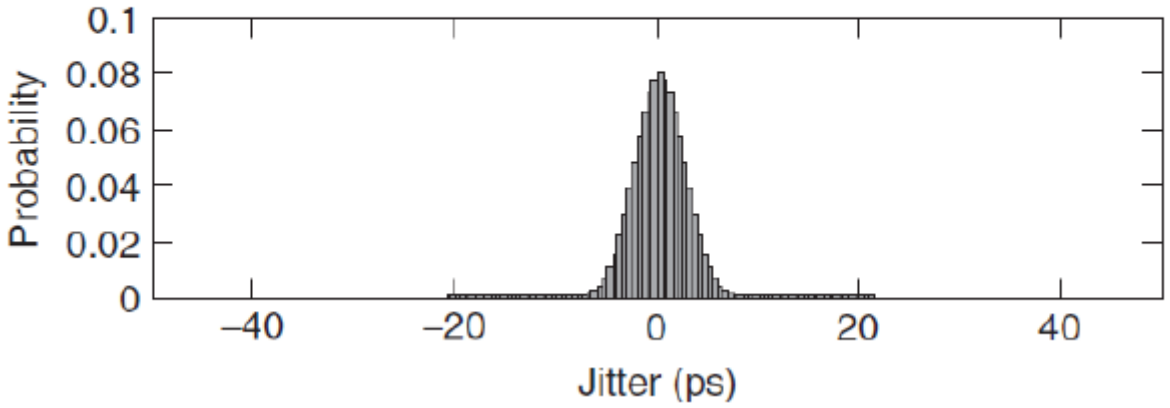
Duty Cycle Distortion (DCD)

Bounded Uncorrelated Jitter (Crosstalk)

Random Jitter (RJ)

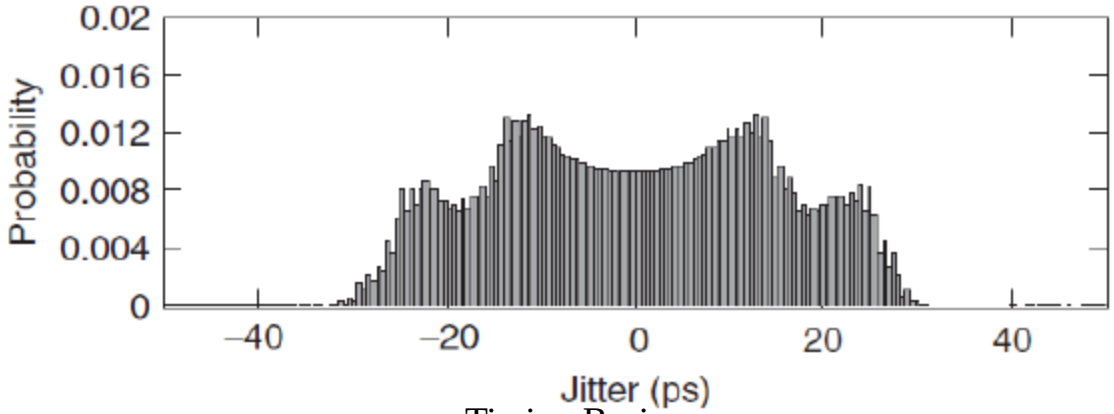
- **Unbounded and modeled with a Gaussian distribution.**
  - Assumed to have zero mean value.
  - Characterized by the rms value, σ_{RJ}.
  - Peak-to-peak value must be quoted at a given BER.
- **Originates from device noise.**
  - Thermal, shot, flicker noise

$$RJ(t) = \frac{1}{\sqrt{2\pi}\sigma_{RJ}} e^{\frac{-t^2}{2\sigma_{RJ}^2}}$$



Deterministic Jitter (DJ)

- **Bounded with a peak-to-peak value that can be predicted.**
- **Caused by transmission-line losses, duty-cycle distortion, spread-spectrum clocking, crosstalk.**
- **Categories**
  - Sinusoidal Jitter (SJ or PJ)
  - Data Dependent Jitter (DDJ)
    - Intersymbol Interference (ISI)
    - Duty Cycle Distortion (DCD)
    - Bounded Uncorrelated Jitter (BUJ)



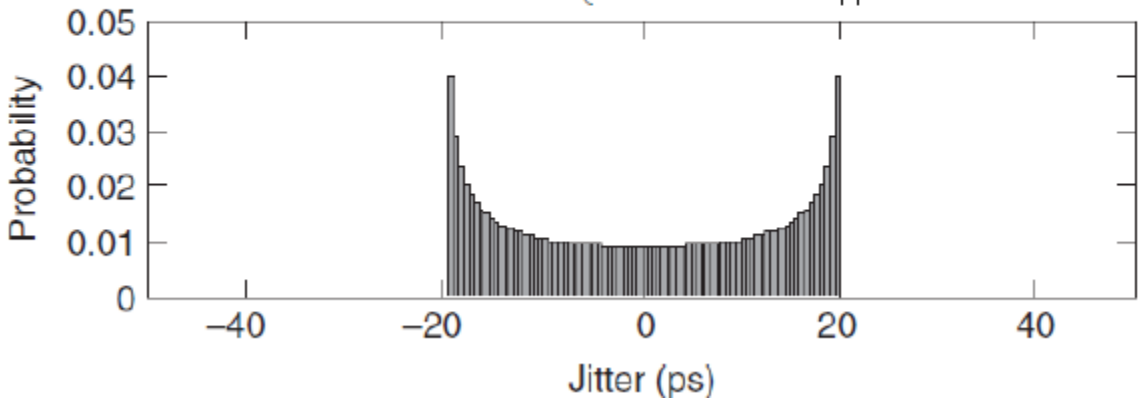
Sinusoidal or Periodic Jitter (SJ or PJ)

- **Repeats at a fixed frequency due to modulating effects.**
  - Spread spectrum clocking.
  - PLL reference clock feedthrough.
- **Can be decomposed into a Fourier series of sinusoids.**

$$SJ(t) = \sum_i A_i \cos(\omega_i t + \theta_i)$$

- **The jitter produced by an individual sinusoid is**

$$PDF_{SJ}(t) = \begin{cases} \dfrac{1}{\pi\sqrt{A^2 - t^2}} & A > |t| \\ 0 & A \le |t| \end{cases}$$



Data Dependent Jitter (DDJ)

- **Data dependent jitter is correlated with either the transmitted data pattern or aggressor (crosstalk) data patterns.**

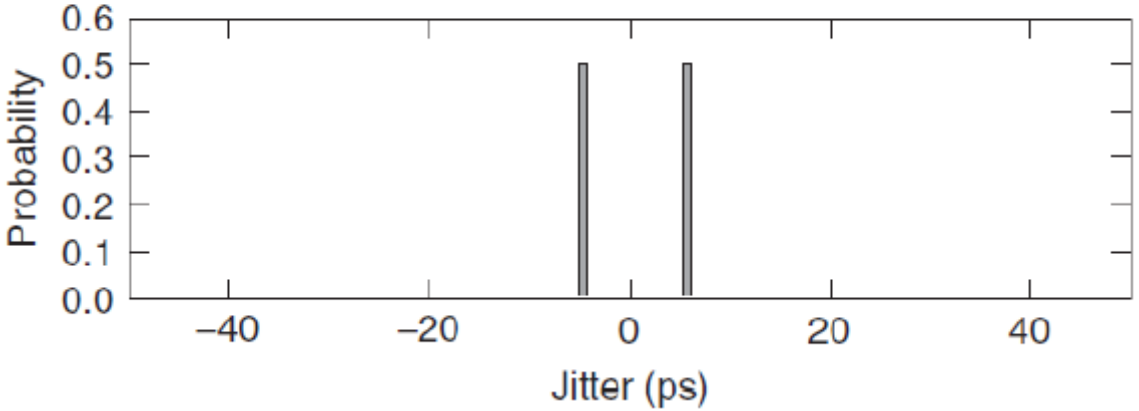
- **Caused by phenomena such as phase errors in serialization clocks, channel filtering, and crosstalk.**

- **Categories**
  - Duty Cycle Distortion (DCD)
  - Intersymbol Interference (ISI)
  - Bounded Uncorrelated Jitter (BUJ)

Duty Cycle Distortion (DCD)

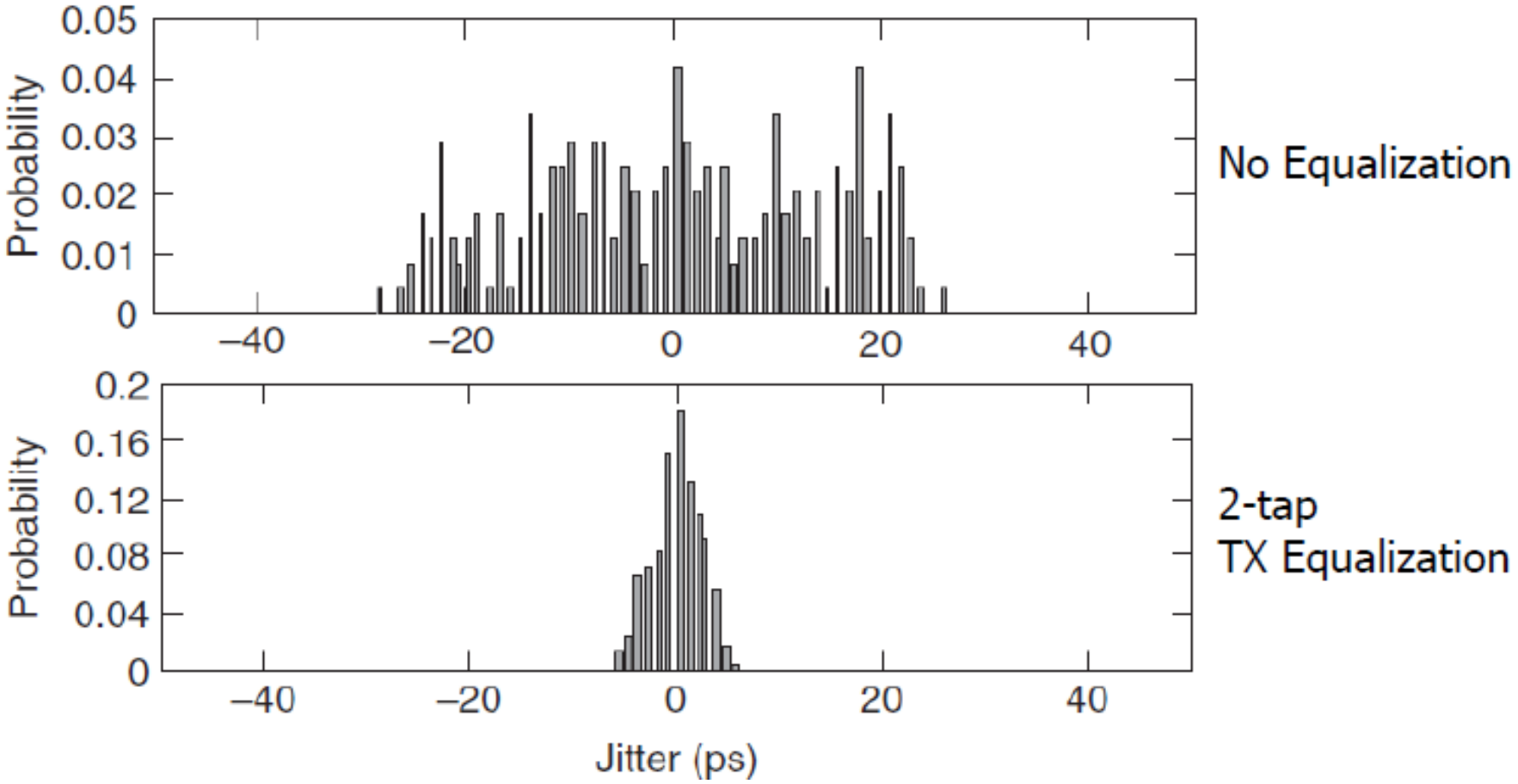
- Caused by duty cycle errors in TX serialization clocks and rise/fall delay mismatches in post-serialization buffers.
- Resultant PDF from a peak-to-peak duty cycle distortion (α_{DCD}) is the sum of two delta functions.

$$PDF_{DCD}(t) = \frac{1}{2}\left[\delta\left(t - \frac{\alpha_{DCD}}{2}\right) + \delta\left(t + \frac{\alpha_{DCD}}{2}\right)\right]$$



Intersymbol Interference (ISI)

- **Caused by channel loss, dispersion, and reflections.**
- **Equalization can improve ISI jitter.**



Bounded Uncorrelated Jitter (BUJ)

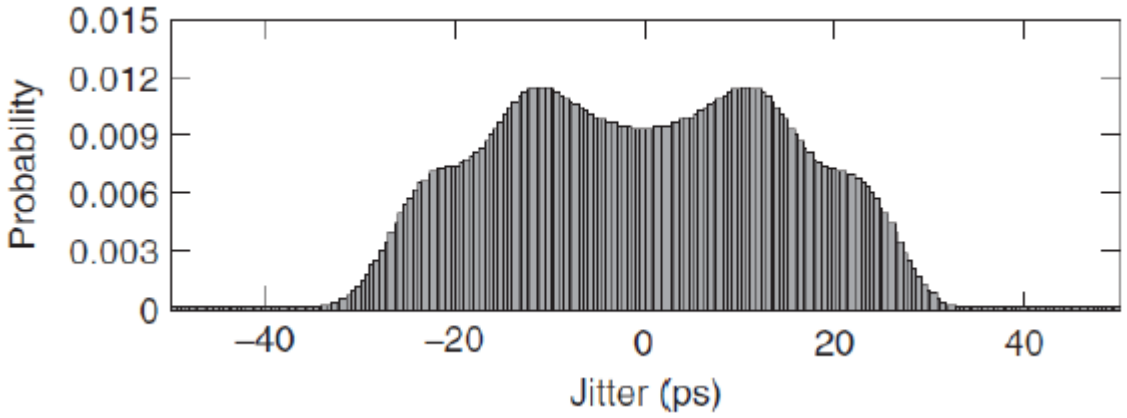
- Not aligned in time with the data stream.
- Most common source is crosstalk.
- Classified as uncorrelated due to being correlated to the aggressor signals and not the victim signal or data stream.
- While uncorrelated, still a bounded source with a quantifiable peak-to-peak value.

Total Jitter (TJ)

- **The total jitter PDF is produced by convolving the random and deterministic jitter PDFs.**

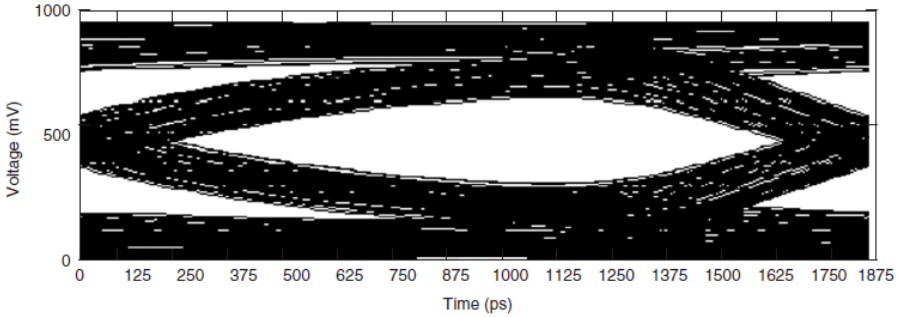
$$PDF_{TJ}(t) = PDF_{RJ}(t) * PDF_{DJ}(t)$$

where $PDF_{DJ}(t) = PDF_{SJ}(t) * PDF_{DCD}(t) * PDF_{ISI}(t) * PDF_{BUJ}(t)$

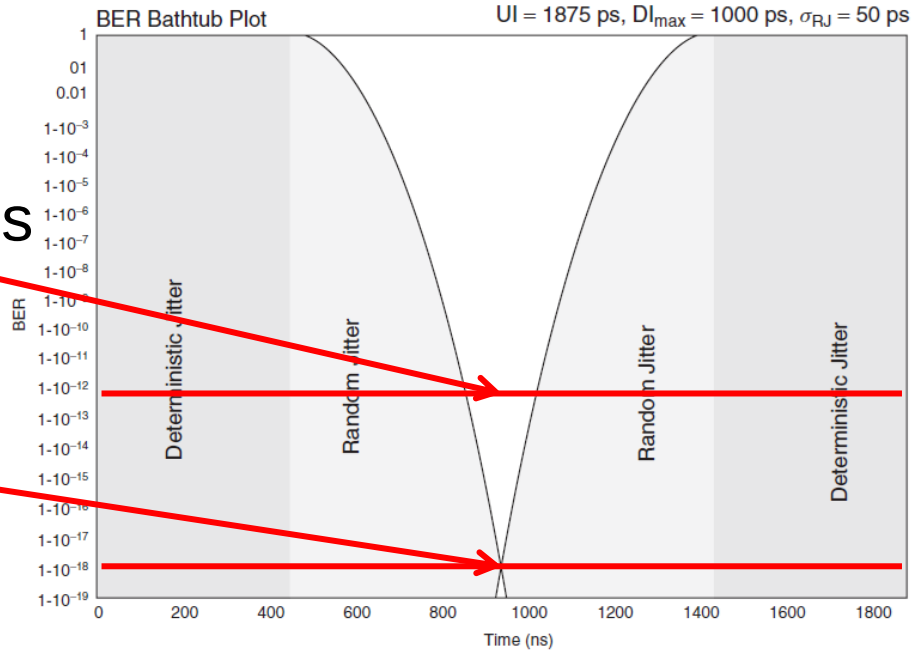


Jitter and Bit Error Rate

- **Jitter consists of both deterministic and random components**



- **Total jitter must be quoted at a given BER**
  - At BER=10^{-12}, jitter ~1675ps and eye width margin ~200ps
  - System can potentially achieve BER=10^{-18} before being jitter limited.



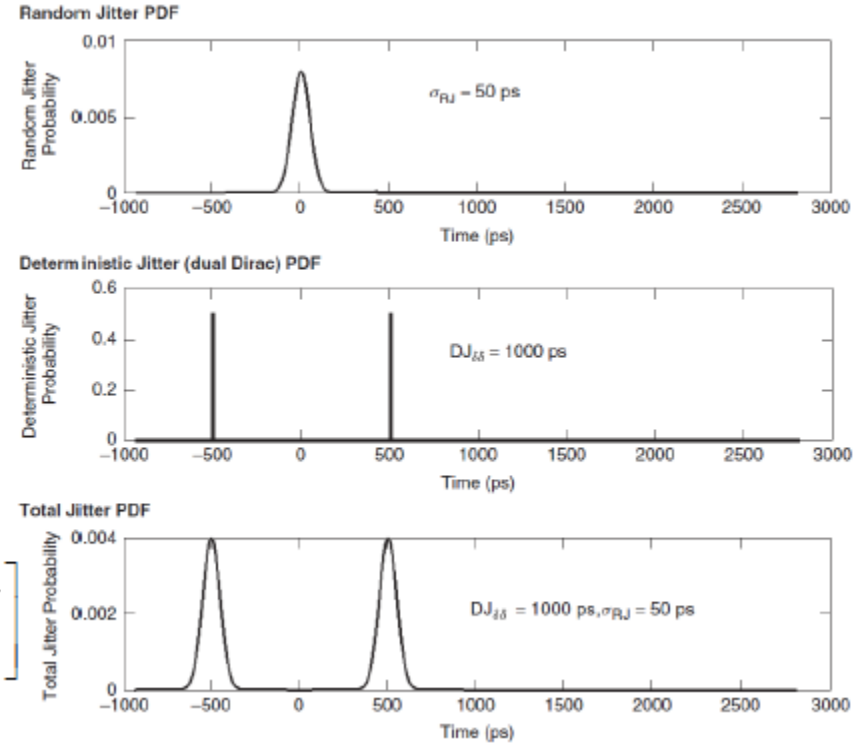
Dual Dirac Jitter Model

- **For system-level jitter budgets, the dual Dirac model approximates the complex total jitter PDF and allows for the budgeting of deterministic and random jitter components.**

$$RJ(t) = \frac{1}{\sqrt{2\pi}\sigma_{RJ}} e^{\frac{-t^2}{2\sigma_{RJ}^2}}$$

$$DJ(t) = \frac{\delta(t - DJ_{\delta\delta}/2)}{2} + \frac{\delta(t + DJ_{\delta\delta}/2)}{2}$$

$$TJ(t) = RJ(t) * DJ(t) = \frac{1}{2\sqrt{2\pi}\sigma_{RJ}} \left[e^{\frac{t - DJ_{\delta\delta}/2}{2\sigma_{RJ}^2}} + e^{\frac{t + DJ_{\delta\delta}/2}{2\sigma_{RJ}^2}} \right]$$



System Jitter Budget

- **For a system to achieve a minimum BER performance**

$$UI \geq DJ_{\delta\delta}(sys) + Q_{BER}\sigma_{RMS}(sys)$$

- **The convolution of the individual deterministic jitter components is approximated by linear addition of the terms.**

$$DJ_{\delta\delta}(sys) = \sum_i DJ_{\delta\delta}(i)$$

- **The convolution of the individual random jitter components results in a root-sum-of-squares system rms value.**

$$\sigma_{RMS}(sys) = \sqrt{\sum_i \sigma^2_{RMS}(i)}$$

Example – PCI Express System

$$DJ_{\delta\delta}(sys) = DJ_{\delta\delta}(TX) + DJ_{\delta\delta}(channel) + DJ_{\delta\delta}(RX) + DJ_{\delta\delta}(clock)$$

$$\sigma_{RMS}(sys) = \sqrt{\sigma^2_{RMS}(TX) + \sigma^2_{RMS}(channel) + \sigma^2_{RMS}(RX) + \sigma^2_{RMS}(clock)}$$

TABLE 13-2. PCI Express 2.5-Gb/s Jitter Budget at 10^{-12} BER

Component	Term	σ_{RJ} (ps)	$DJ_{\delta\delta}$ (ps)	TJ (ps)
Reference clock	TJ_{clock}	4.7	41.9	108
Transmitter	TJ_{TX}	2.8	60.6	100
Channel	$TJ_{channel}$	0	90	90
Receiver	TJ_{Rx}	2.8	120.6	~~147~~ 160
Linear TJ				458
RSS TJ	6.15 * 14.069 =	86.5	313.1	399.6

TABLE 13-1. Q_{BER} as a Function of the Bit Error Rate

BER	Q_{BER}	BER	Q_{BER}	BER	Q_{BER}
1×10^{-3}	6.180	1×10^{-10}	12.723	1×10^{-17}	16.987
1×10^{-4}	7.438	1×10^{-11}	13.412	1×10^{-18}	17.514
1×10^{-5}	8.530	1×10^{-12}	14.069	1×10^{-19}	18.026
1×10^{-6}	9.507	1×10^{-13}	14.698	1×10^{-20}	18.524
1×10^{-7}	10.399	1×10^{-14}	15.301	1×10^{-21}	19.010
1×10^{-8}	11.224	1×10^{-15}	15.882	1×10^{-22}	19.484
1×10^{-9}	11.996	1×10^{-16}	16.444	7.7×10^{-24}	20.000

[Hall]

Jitter Measurement

RJ D Jitter Separation with an Agilent Infiniium Real Time Scope.mp4

https://www.youtube.com/watch?v=ui53SkVEWDA