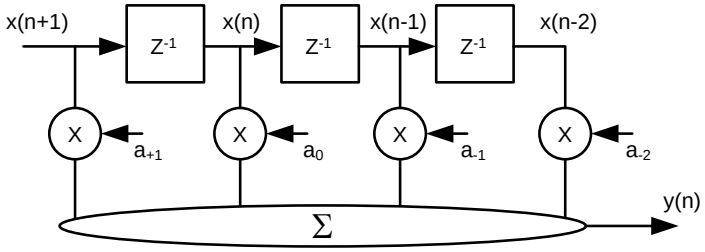
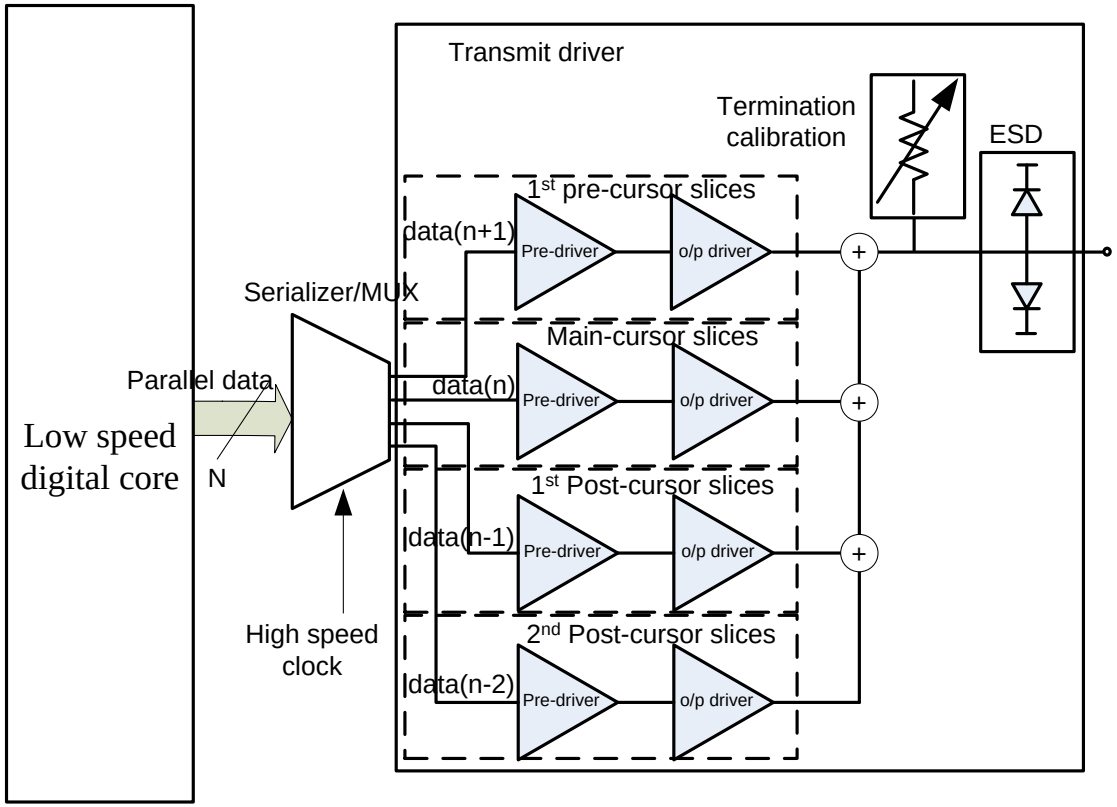
High-Speed Wire Line Transmitters

Lecture 4

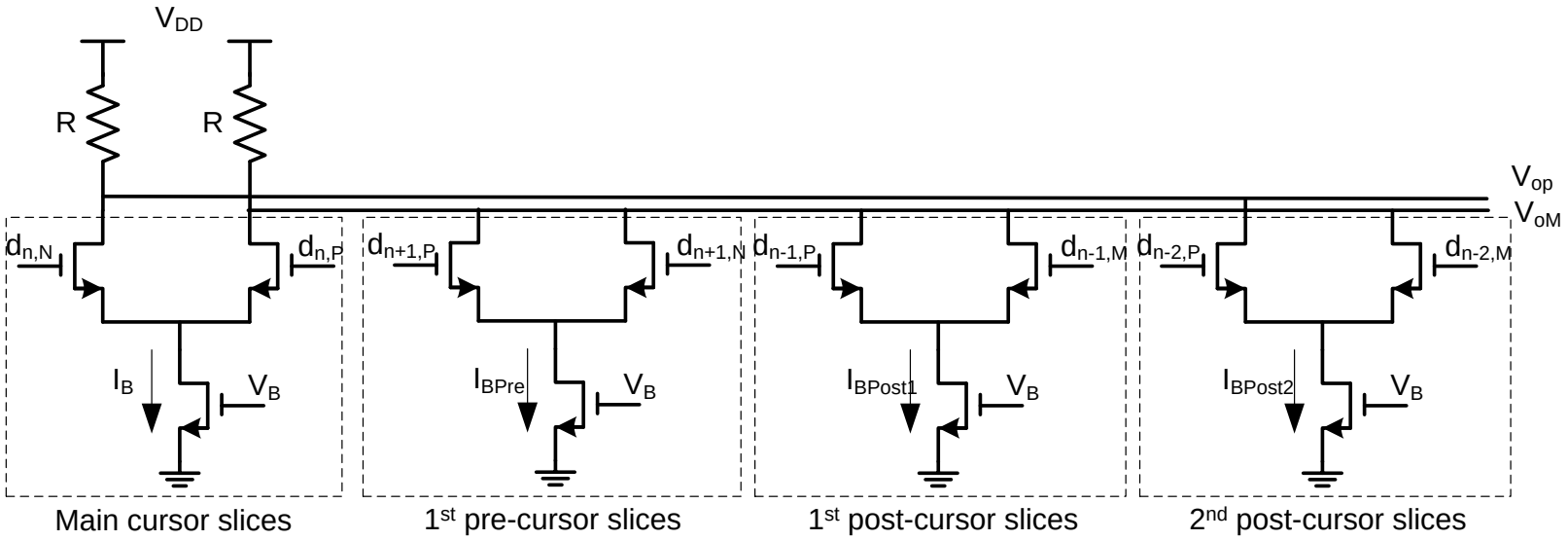
Tx FFE Implementation





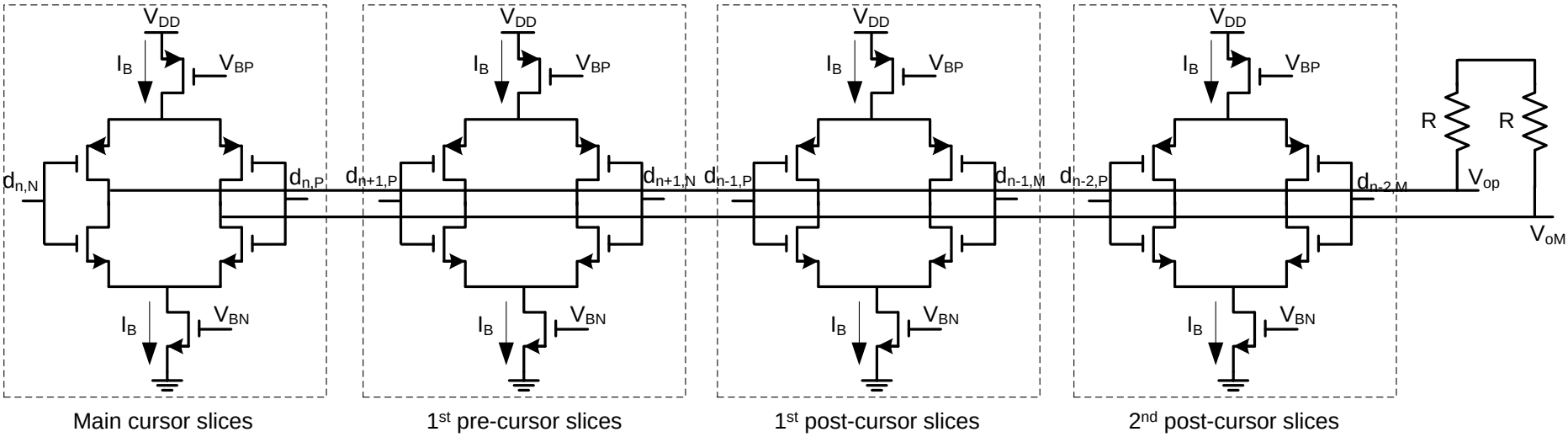
- Main, delayed and future data values are already available at the parallel interface
- The serializer block can produce the 4 required signals for a 4-tap FIR
- The number of slices assigned to each data cursor will determine the relative tap strength

CML Tx FFE Implementation



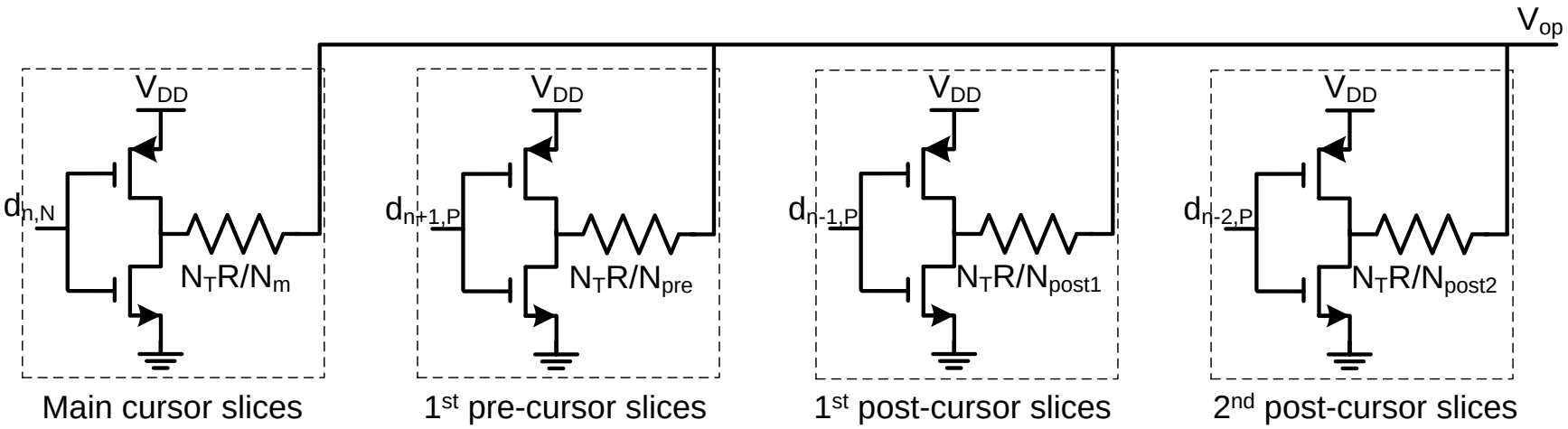
- Summation is done in the current domain
- The polarity of the delayed and future date is reversed for negative FFE taps, if positive taps are required that can be achieved be reversing the polarities in the serializer
- The relative strength of each cursor can be tuned by controlling the current sources, but changing the current in one branch entails changing the current of the main cursor to achieve a constant swing.
- Coarse control over pre-emphasis can be achieved by changing the number of slices assigned to each tap

H-bridge Tx FFE Implementation



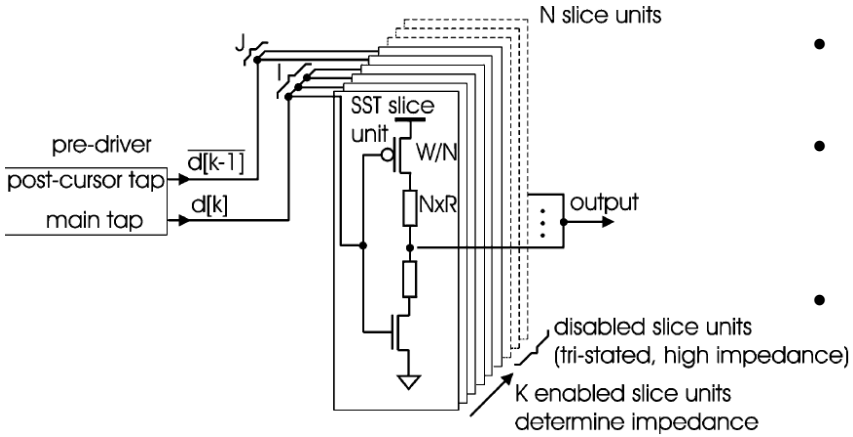
- Similar to CML summation takes place in the current domain before flowing in the differential 100Ohm termination resistor
- No. of slices assigned to each tap and bias current allow both coarse and fine tuning respectively

SST Tx FFE Implementation



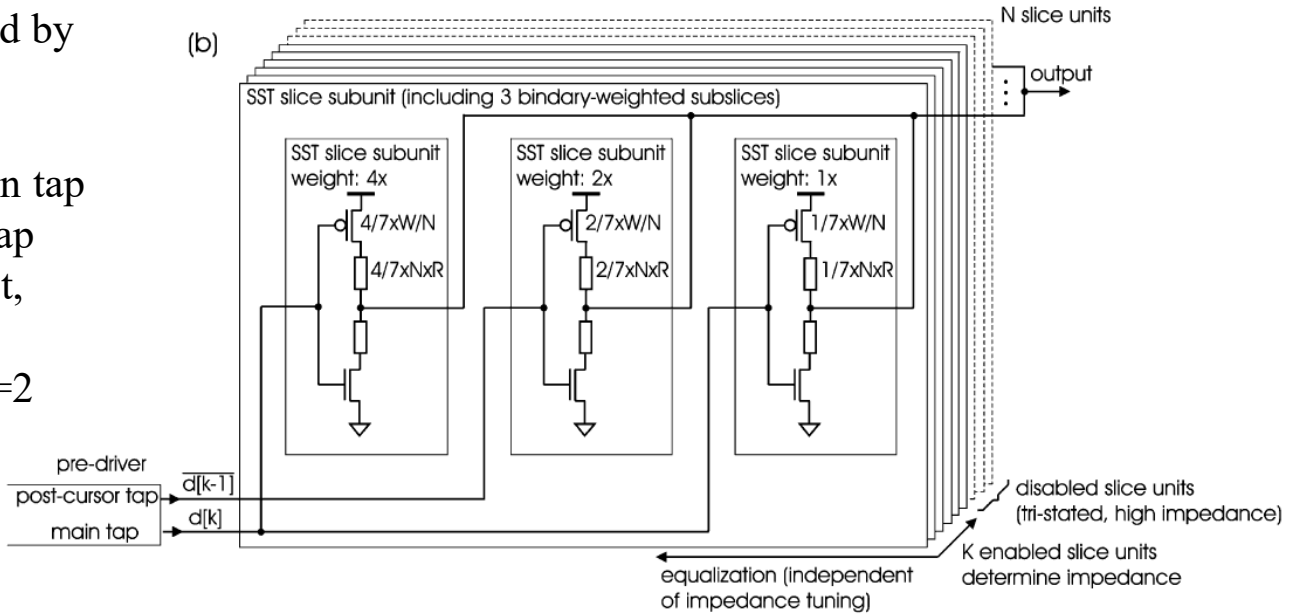
- Summation has to take place in voltage mode
- The driver is divided into many slices each having a termination equal to N_TR, where N_T is the total number of slices
- If no pre-emphasis is required, all slices are assigned to the main cursor and no voltage division takes place
- When Tx pre-emphasis is needed some slices are distributed among different cursors according to the required FFE tap weights
  - For transition bits (considering only the 1st post-cursor) the slices add together and the full V_{DD} swing is achieved
  - For non transition bits the 1st post cursor slices would have a different polarity and a potential divider is created lowering the swing
- The resolution of pre-emphasis is a function of the total number of full slices. Note that half slices can be used to improve the resolution

JSSC 2008: 8Gb/s High-swing SST Transmitter in 65nm Bulk CMOS



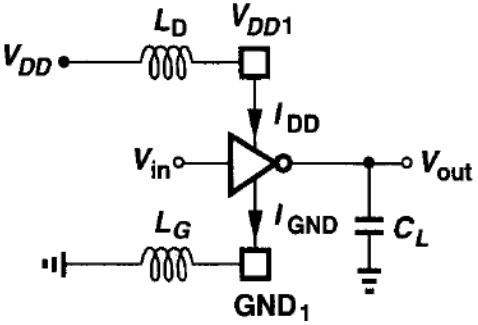
- The problem is that the transmitter impedance cannot be tuned independently of the equalization setting
- A change in the number of parallel connected slice units also affects the number of slice units assigned to the main and post-cursor taps
- The individual slice units are composed of three binary-scaled SST stages → the selected equalization setting is maintained independently of the value of K

- Nominal impedance is obtained by connecting K out of N slice in parallel
- I slices are assigned to the main tap and J units to the post-cursor tap
- If K=8, and we need 6dB boost, then:
- $20\log_{10}(1-J)/K=6$, i.e. I=6 & J=2



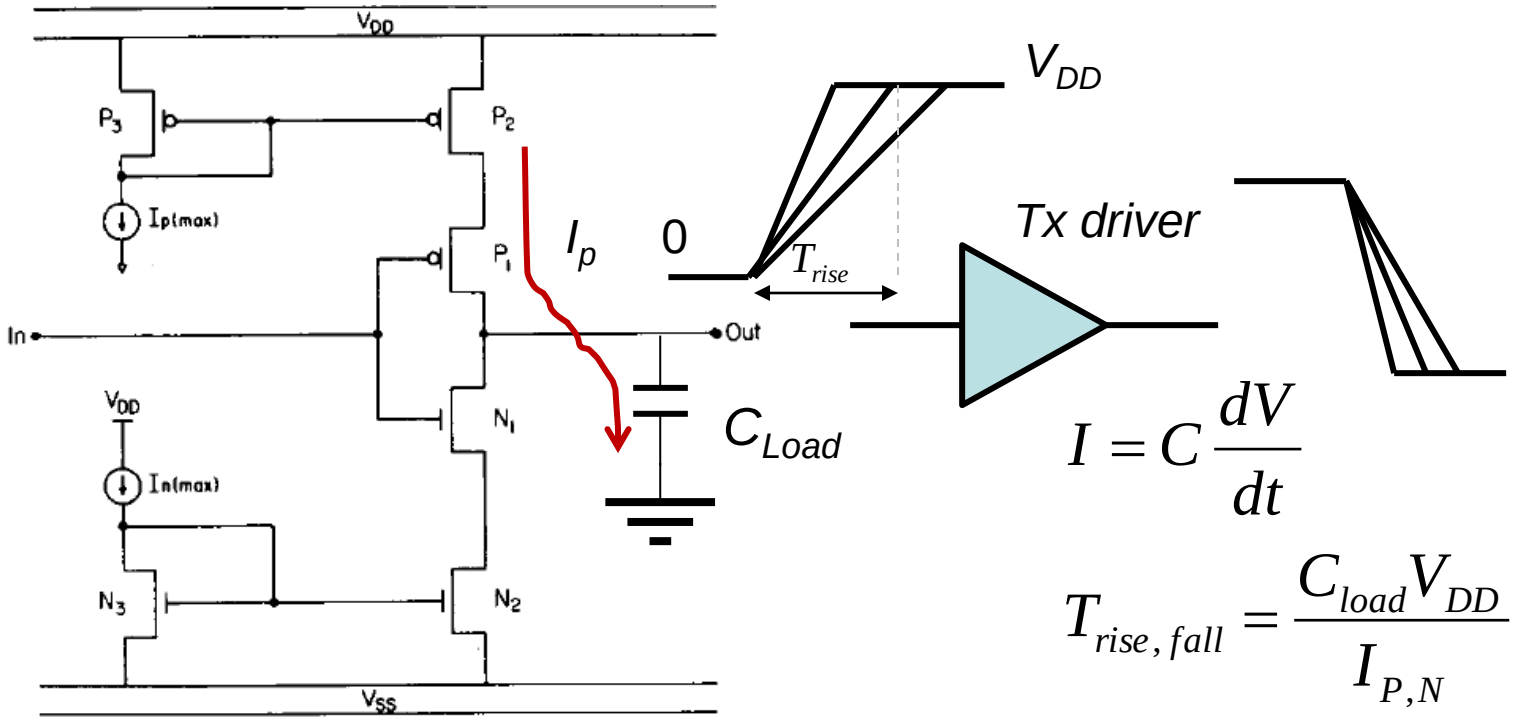
Pre-driver

- Pre-drivers are necessary to drive the large transistors of the output stage



- Common pre-driver implemented as:
  - CMOS buffers
    - Simpler implementation
    - Zero static power consumption,
    - During switching of the CMOS buffers a current kick is generated which can result in ripples on the supply voltage, problematic for large package inductance (Ldi/dt)
    - This supply ripple can be a major source DDJ
  - CML buffers
    - Static power consumption is non-zero
    - When buffer is switching the total current it is drawing from the supply remains constant resulting in less ripples on the supply voltage
- Pre-drivers can also be used to control the o/p driver slew rate:
  - Slew rate control can be achieved by changing the rise/fall time of the output of the pre-driver, for example current starved inverters for CMOS buffers

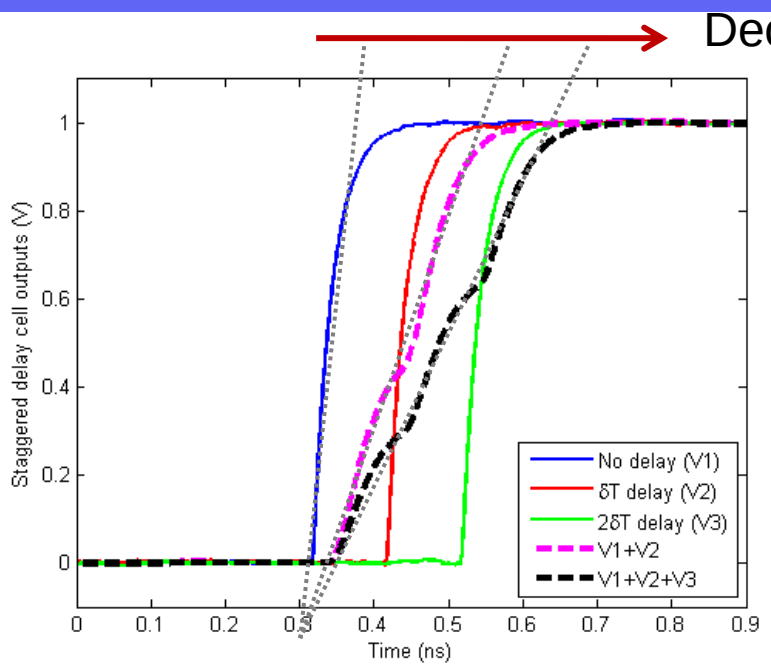
Slew Rate Control by Current Starving



- Driver slew rate is spec depending on the standard to reduce EMI
- By controlling the bias currents $I_{P,N}$ we can adjust the rise/fall time of the pre-driver, which will affect the rise/fall time of the Tx output driver

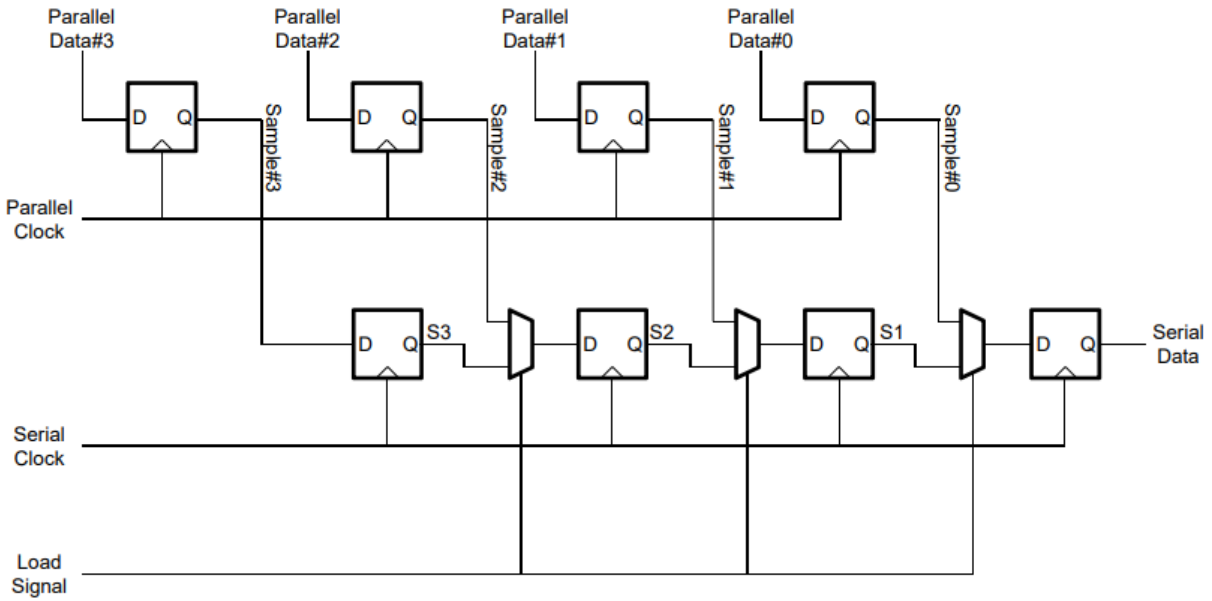
R. Senthinathan and J. L. Prince, "Application specific CMOS output driver circuit design techniques to reduce simultaneous switching noise," in IEEE Journal of Solid-State Circuits, vol. 28, no. 12, pp. 1383-1388, Dec. 1993.

Slew Rate Control by Staggering



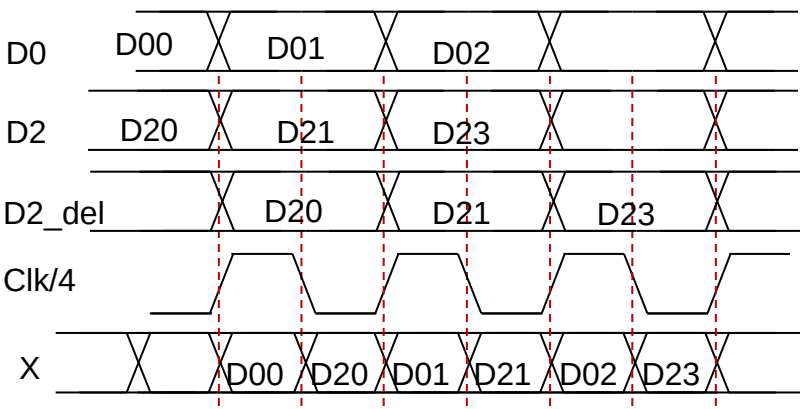
- To achieve more tuning range for slew rate, coarse control can be achieved by combing the output of staggered delay cells in the pre-driver
- The coarse control bits can be used to select how many (relative weight) and which delayed signals are added in order to adjust the slew rate
- The output driver bandwidth limitation smoothes out the discrete steps generated by adding the delayed waveforms assuming that they are relatively close

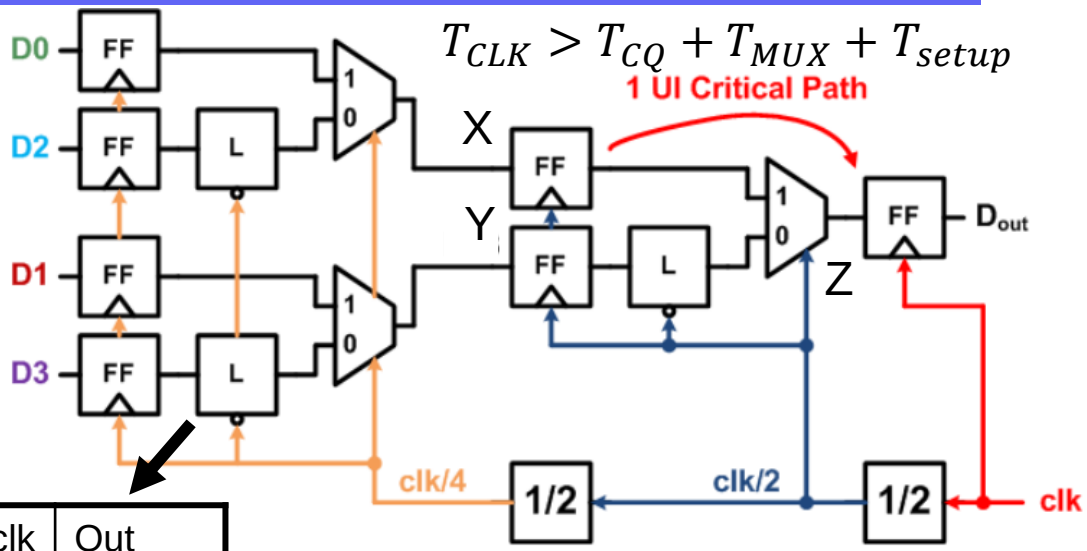
DFF-based Serialzer/Mux

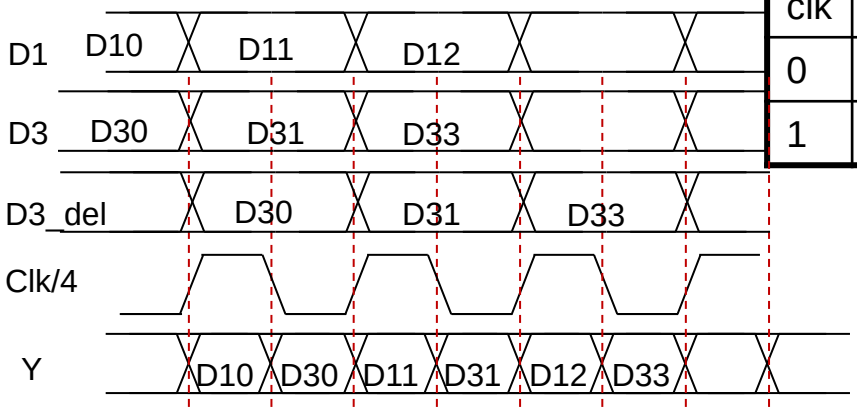


- Can use simple DFF based parallel-load serial shift out register as a serilaizer
- Suitable for low frequency applications
- Requires running N flip flops using the high-speed serial clock
  - Power consumption and area penalty due to multiple high speed DFF
  - High capacitive load on high Tx speed clock
- Requires very good synchronization between parallel load signal and high-speed clock

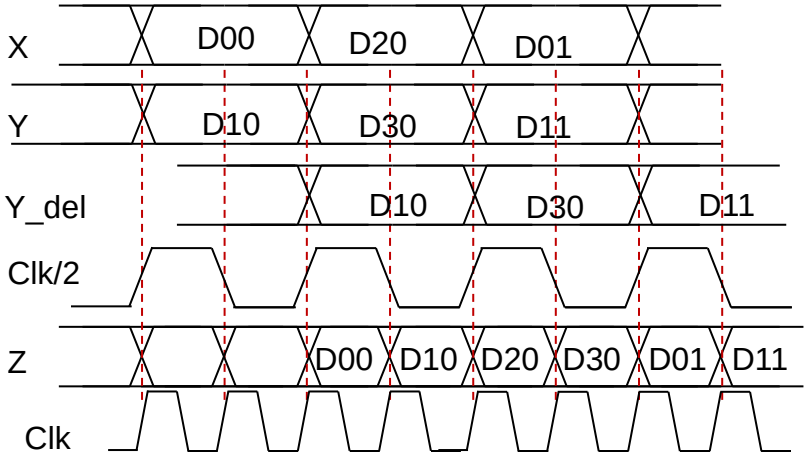
Full-rate Serializer Using 2:1 Mux







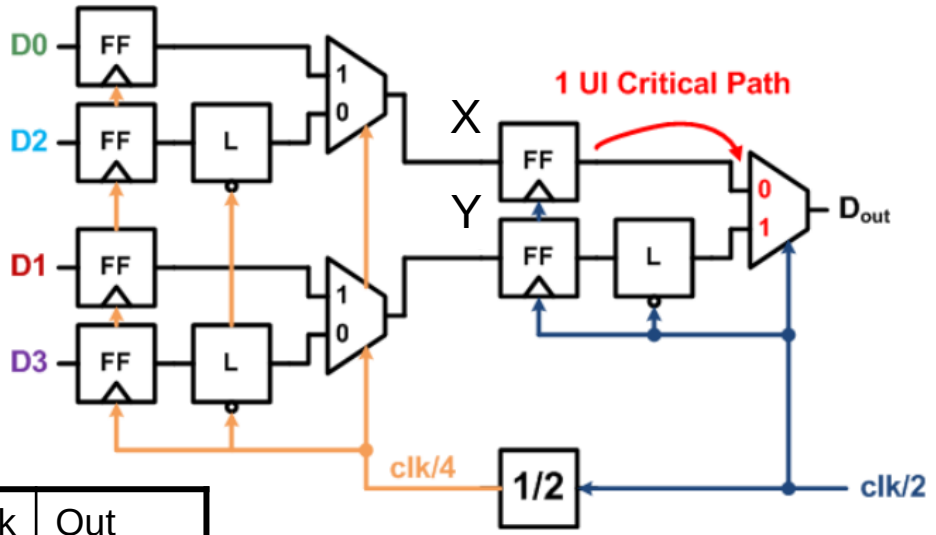
clk	Out
0	Track
1	Latch



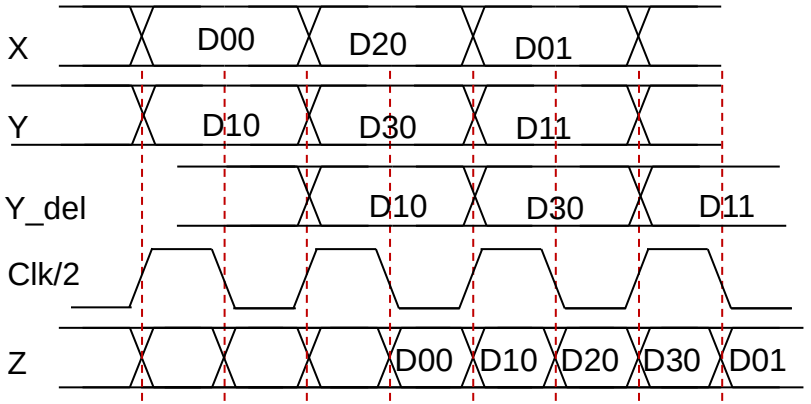
- Final Flip flop samples serial data at full rate → high speed sampler

Half-rate Serializer Using 2:1 Mux

- Half-rate architecture eliminates high-speed clock and flip-flop
- Output data changes on both +ve & -ve clock edges → sensitive to clock duty cycle distortion
- Critical path no longer has flip-flop setup time
- Final mux control is swapped to prevent output glitches

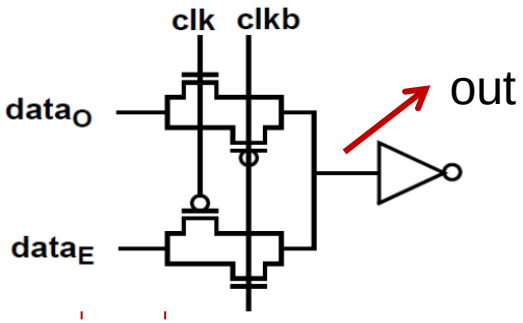


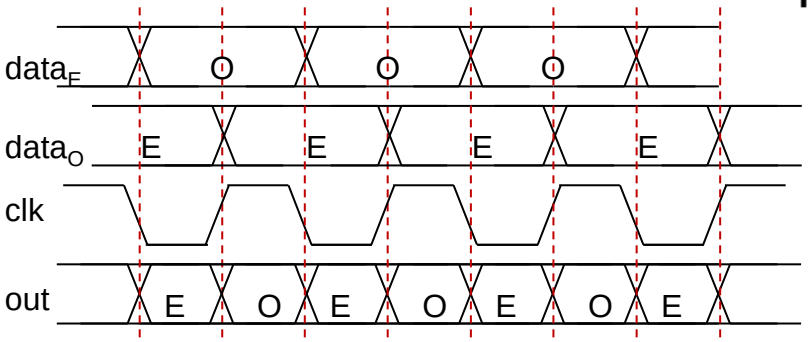
clk	Out
0	Track
1	Latch

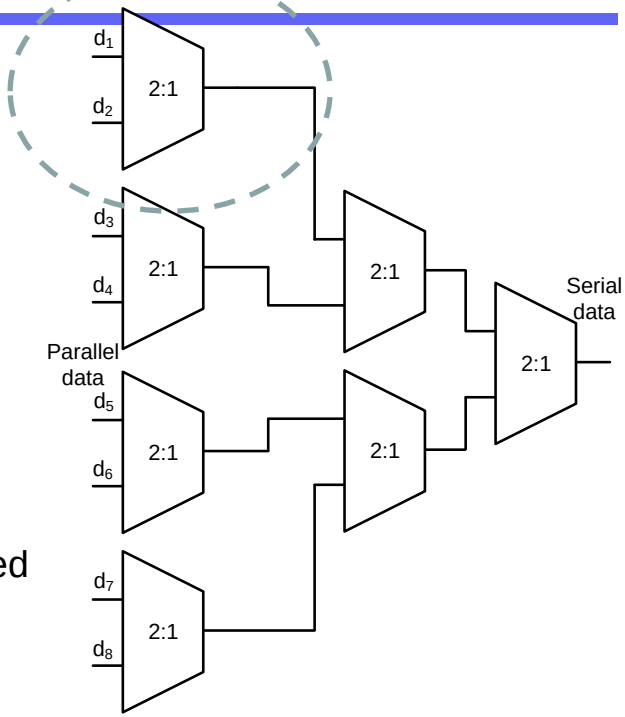


Serializers: Transmission Gate MUX

clk	out
0	$data_E$
1	$data_O$

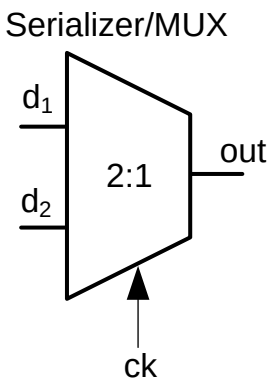




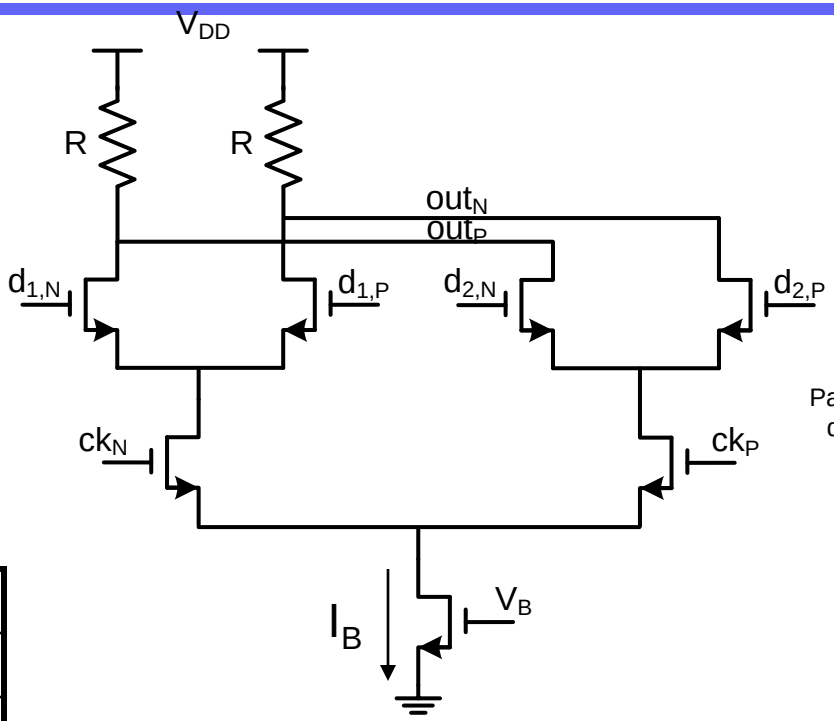


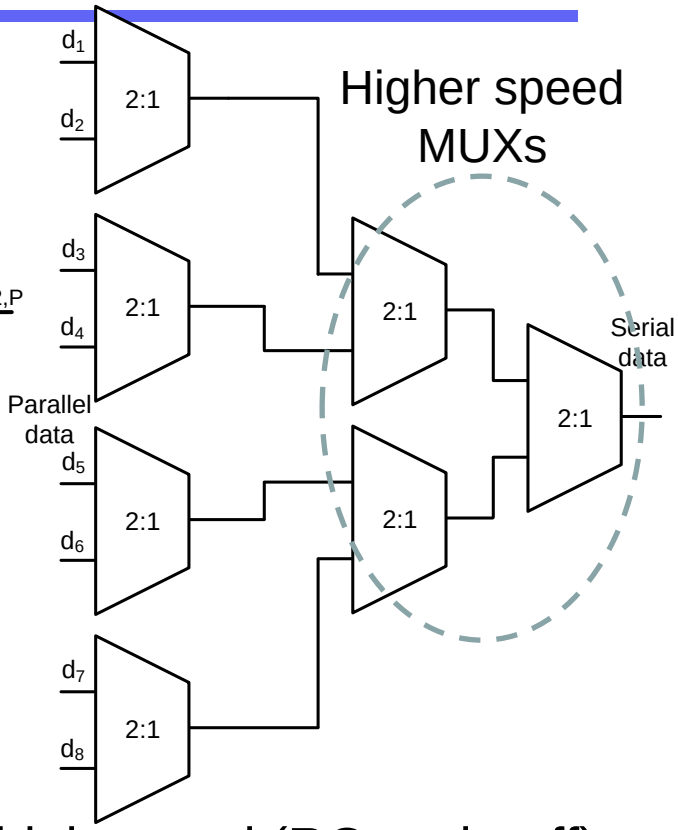
- The serializer/MUX block is basically a parallel to serial converter
- It receives the parallel bits from the digital core and converts it into the high speed serial stream, for example 16:1
- A modular approach to do this is by designing a 2:1 MUX and then go from 16:8, 8:4, 4:2 and finally from 2:1
- As speed increases the Tgate size needs to increased to reduce R_{ON} until the Tgate capacitance start to dominate

Serializers: CML-based



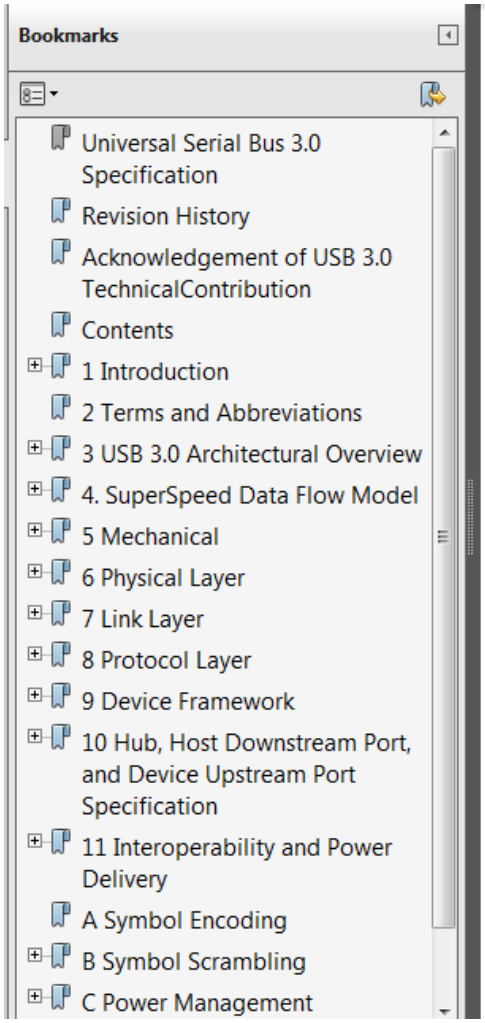
clk	Out
0	d1
1	d2





- Transmission-gate MUXs are not suitable for high speed (RC trade-off)
- High speed MUXs usually use a CML-based topology
- To increase swing & maintain BW used small R and increase current
- Inductive peaking can be used to extend the circuit BW further

Sample Spec. Document: USB 3.0



Universal Serial Bus 3.0 Specification

(including errata and ECNs through May 1, 2011)

Hewlett-Packard Company

Intel Corporation

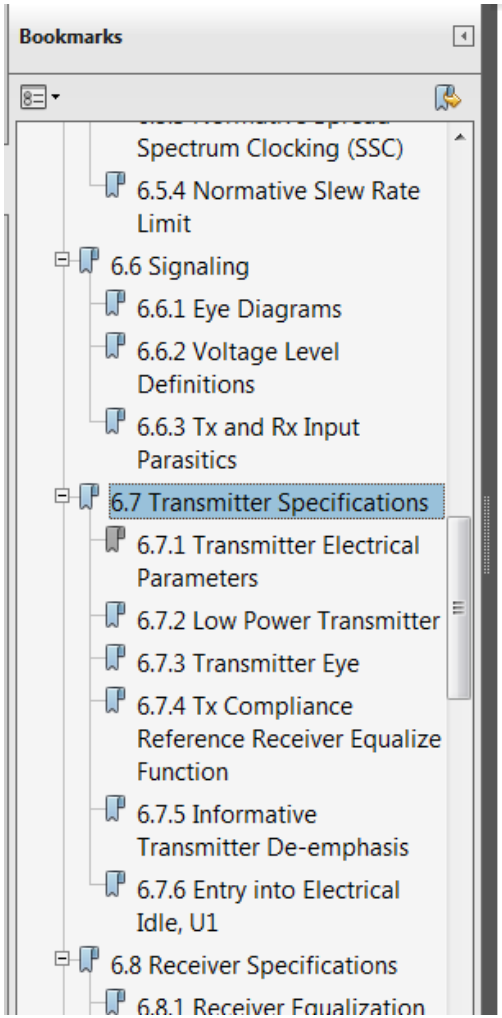
Microsoft Corporation

NEC Corporation

ST-Ericsson

Texas Instruments

Sample Spec. Document: USB 3.0 (Cont'd)



6.7 Transmitter Specifications

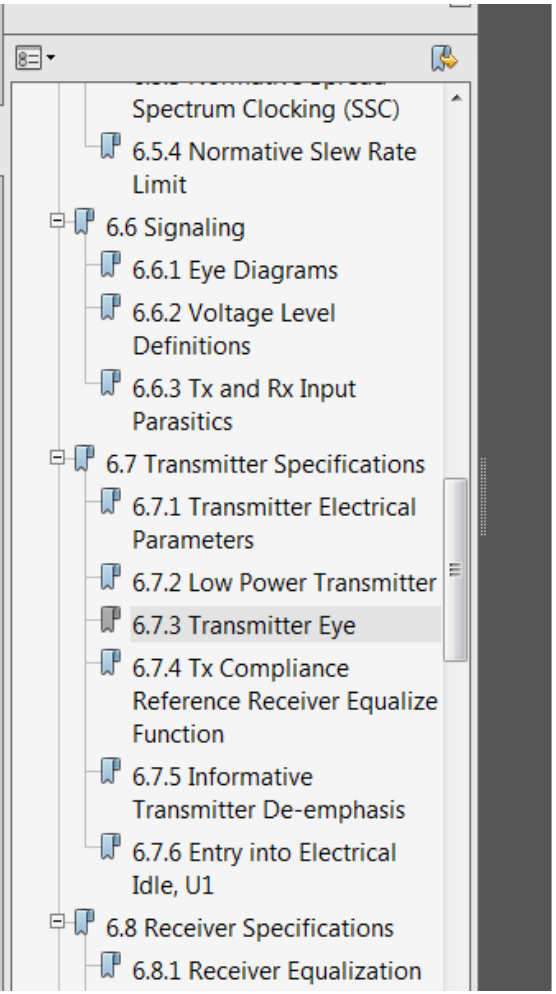
6.7.1 Transmitter Electrical Parameters

Peak (p) and peak-peak (p-p) are defined in Section 6.6.2.

Table 6-10. Transmitter Normative Electrical Parameters

Symbol	Parameter	5.0 GT/s	Units	Comments
UI	Unit Interval	199.94 (min) 200.06 (max)	ps	The specified UI is equivalent to a tolerance of ±300 ppm for each device. Period does not account for SSC induced variations.
$V_{TX-DIFF-PP}$	Differential p-p Tx voltage swing	0.8 (min) 1.2 (max)	V	Nominal is 1 V p-p
$V_{TX-DIFF-PP-LOW}$	Low-Power Differential p-p Tx voltage swing	0.4 (min) 1.2 (max)	V	Refer to Section 6.7.2. There is no de-emphasis requirement in this mode. De-emphasis is implementation specific for this mode.
$V_{TX-DE-RATIO}$	Tx de-emphasis	3.0 (min) 4.0 (max)	dB	Nominal is 3.5 dB
$R_{TX-DIFF-DC}$	DC differential impedance	72 (min) 120 (max)	Ω	
$C_{AC-COUPLING}$	AC Coupling Capacitor	75 (min) 200 (max)	nF	All Transmitters shall be AC coupled. The AC coupling is required either within the media or within the transmitting component itself.

Sample Spec. Document: USB 3.0 (Cont'd)



6.7.3 Transmitter Eye

The eye mask is measured using the compliance data patterns (CP0 for DJ and CP1 for RJ) as described in Section 6.4.4. Eye height is measured for 10^6 consecutive UI. Jitter is extrapolated from 10^6 UI to 10^{-12} BER,

Table 6-12. Normative Transmitter Eye Mask at Test Point TP1

Signal Characteristic	Minimal	Nominal	Maximum	Units	Note
Eye Height	100		1200	mV	2, 4
Dj			0.43	UI	1,2,3
Rj			0.23	UI	1,2,3, 5
Tj			0.66	UI	1,2,3

Notes:

1. Measured over 10^6 consecutive UI and extrapolated to 10^{-12} BER.
2. Measured after receiver equalization function.
3. Measured at end of reference channel and cables at TP1 in Figure 6-14.
4. The eye height is to be measured at the maximum opening (at the center of the eye width ± 0.05 UI).
5. The Rj specification is calculated as 14.069 times the RMS random jitter for 10^{-12} BER.

The compliance testing setup is shown in Figure 6-14. All measurements are made at the test point (TP1), and the Tx specifications are applied after processing the measured data with the compliance reference equalizer transfer function described in the next section.