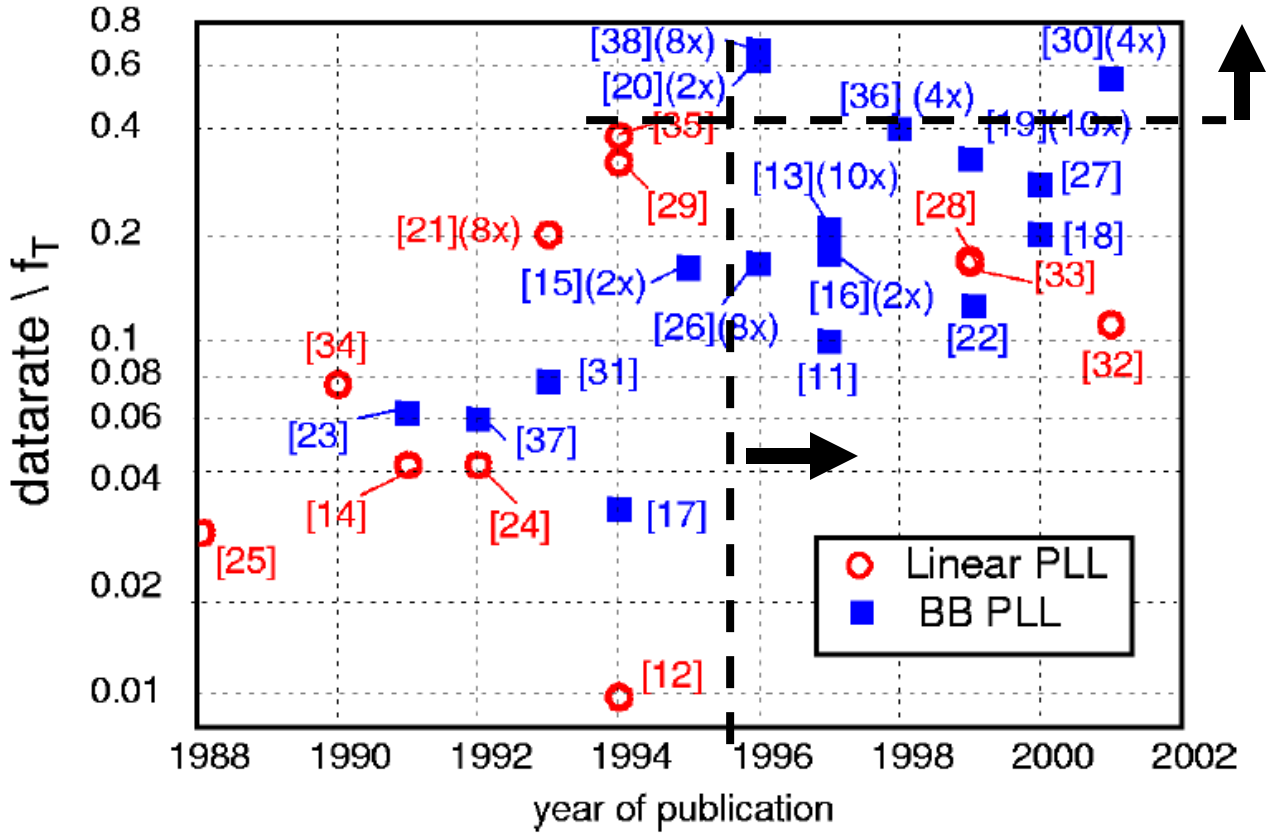
# Clock and Data Recovery

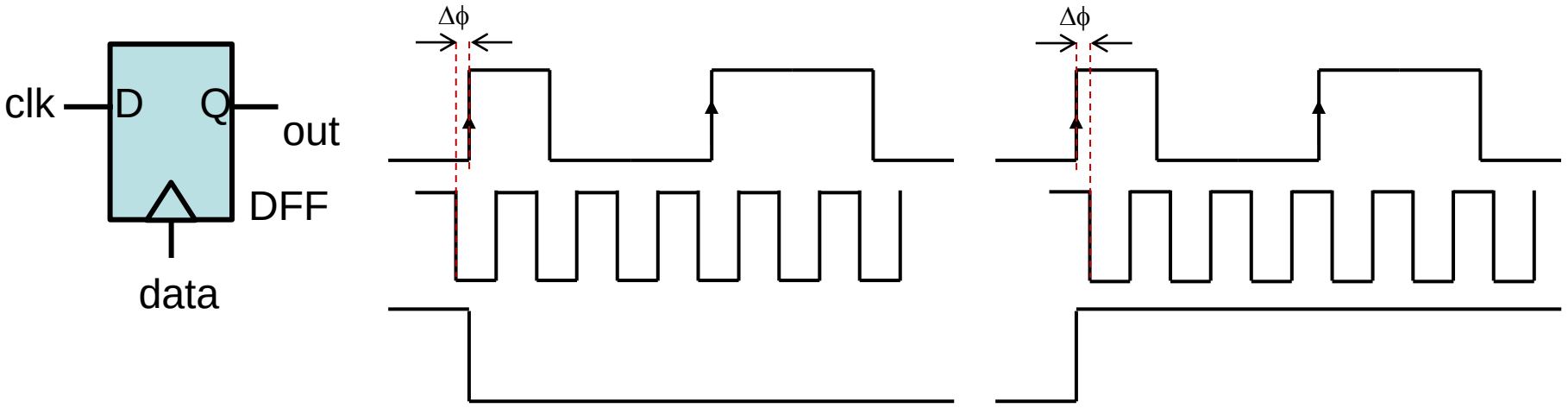
*Lecture 9*

# Linear versus Multi-Phase Non-linear CDRs



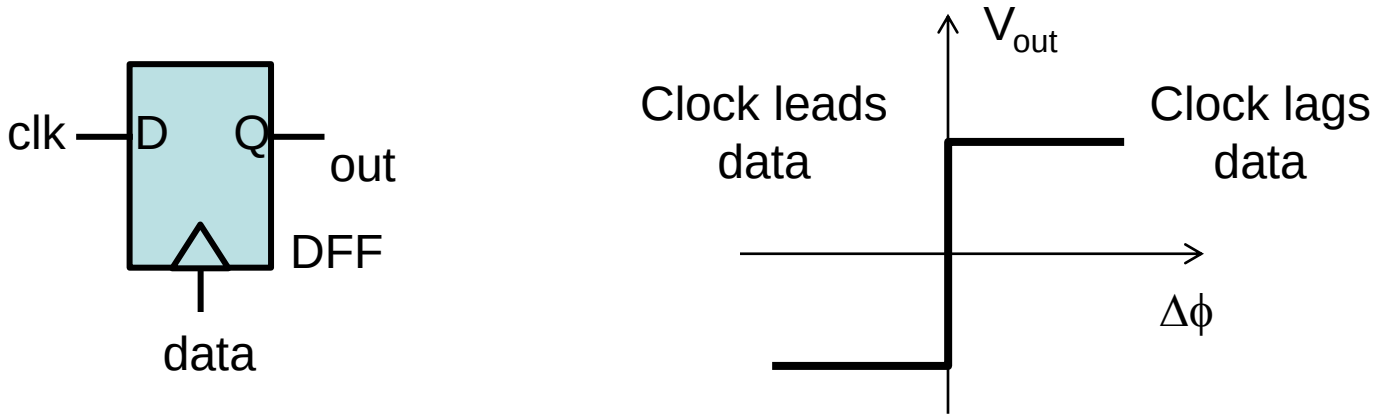

- The majority of the current designs (up to 2002) employ multi phase sampling and Bang-Bang phase detectors
- CDRs operating at speeds > $0.4f_T$ use BB phase detectors

# D Flip-flop as a Non-Linear PD



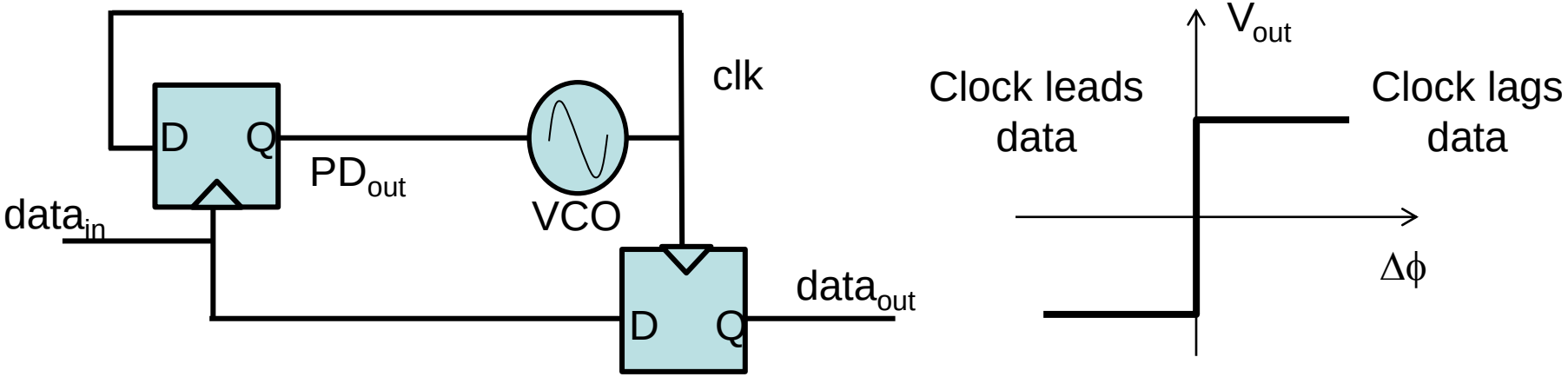

- Each rising edge of the data samples the clock
- If the clock leads the data: the flip-flop will always samples the low level of the clock producing a zero
- If the clock lags the data: the flip-flop will always sample a one
- The PD output can only take one of 2 values depending on weather the data leads or lags the clock
- Thus the output indicates the **polarity** of the phase difference between the data and clock

# D Flip-flop as a Non-Linear PD



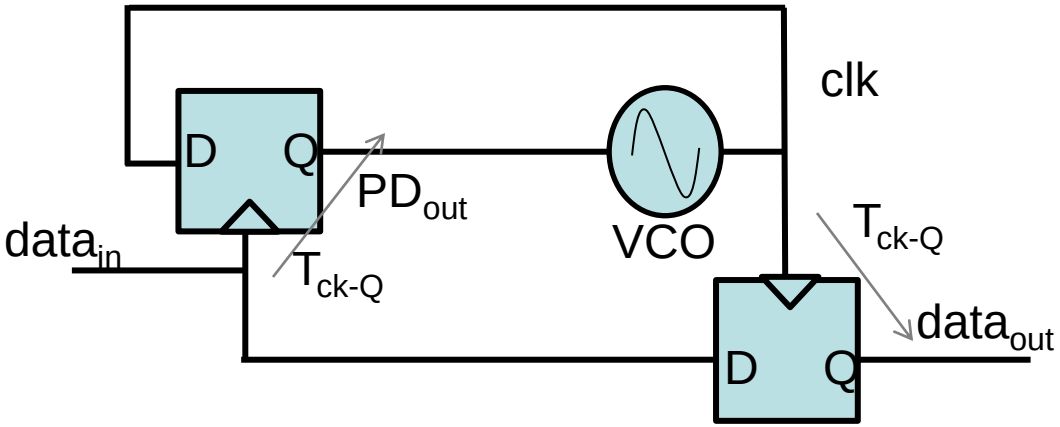

- The DFF PD exhibits nonlinear behavior with very high gain close to $\Delta\phi$=0 and zero gain otherwise
- This behavior is called a “bang-bang” characteristic, where the output jumps from one extreme to another with a slight shift in the input phase
- The BB PD signal can be used to derive the VCO control voltage in a CDR:
  - If the clock leads the data: the negative output will reduce the VCO frequency
  - If the clock lags the data: the positive output will reduce the VCO frequency

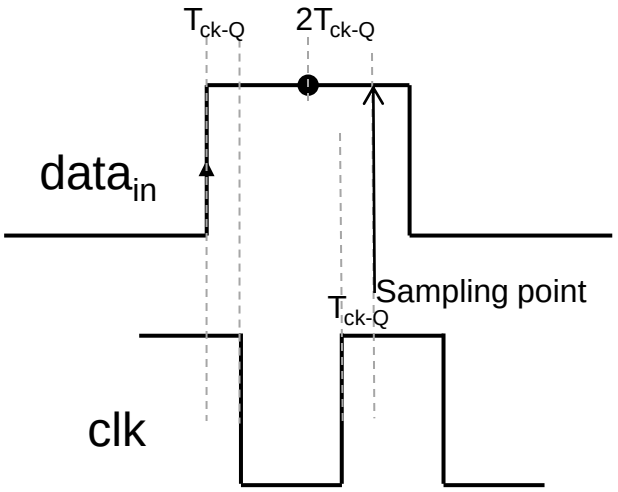
# First Order CDR Using DFF PD




- In a 1st order bang-bang CDR the binary PD output is used to derive the VCO directly
- <u>If the clock lags the data:</u> the PD will continue to generate a “1” running the VCO at the faster frequency ($f_{nom}+f_{BB}$) until the phase of the clock accumulates enough phase and catches up with the data reducing the phase error to zero
- <u>Under lock condition:</u> the PD will continue oscillating between “1” and “-1” with equal probabilities (meta-stability region)
- Another DFF is needed to re-time the data with the recovered clock (VCO clock)

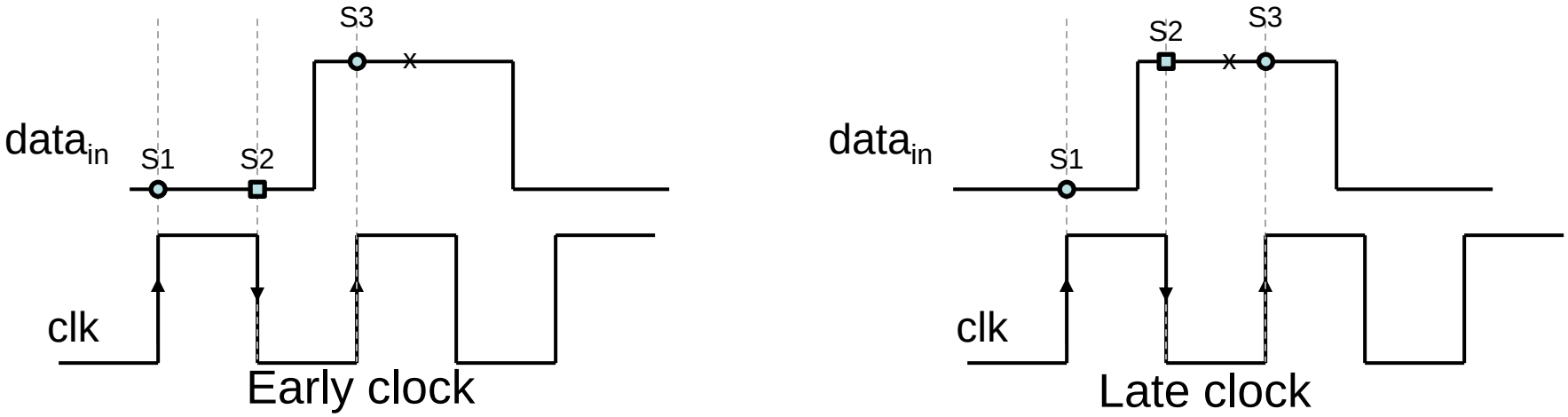
# First Order CDR Using DFF PD




- Drawbacks of this simple CDR:
  - If the CDR is under lock condition and the data contains long CIDs, the PD will continue to produce +1 (or -1) forcing the VCO frequency to run at a the high (or the low) frequency for a long time causing the clock to drift from the data "creating large amount of jitter" → Jitter accumulation
  - If DFF exhibit a finite $T_{ck-Q}$, then after the CDR locks, the clock will lag the data by $T_{ck-Q}$ whereas the output flip flop samples the data with the clock. This will results in a shift (or skew) of $2T_{ck-Q}$ away from the center of the eye

# Alexander Phase Detector




- To avoid the skew problem, it is desired to sample the date with the recovered clock
- Using the 3 samples S1-S3 taken at 3 consecutive edges the PD can tell:
  - if a data transition is present, if no transition is present all the 3 samples would have the same value
  - If the clock leads or lags the data
    - If the clock leads the data (Early): then (S1=S2)≠S3
    - If the clock lags the data (Late): then S1≠(S2=S3)

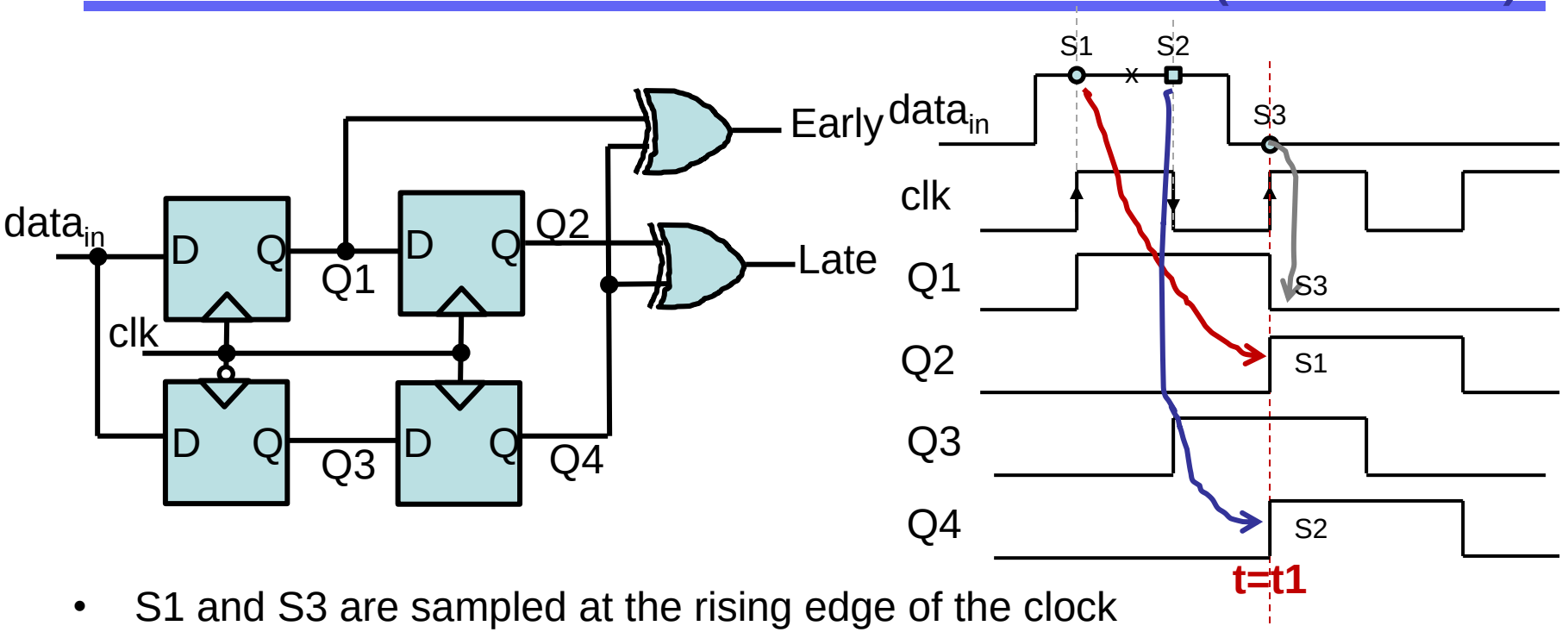
# Alexander Phase Detector (Cont'd)

- **Early=S2⊕S3**
- **Late=S1⊕S2**
- Late=Early=0→ no transition
- ⊕ means an XOR operation

| S1 | S2 | S3 | Late | Early | Transition |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X |
| 0 | 0 | 1 | 0 | 1 | √ |
| 0 | 1 | 0 | - | - | Imp. |
| 0 | 1 | 1 | 1 | 0 | √ |
| 1 | 0 | 0 | 1 | 0 | √ |
| 1 | 0 | 1 | - | - | Imp |
| 1 | 1 | 0 | 0 | 1 | √ |
| 1 | 1 | 1 | 0 | 0 | X |

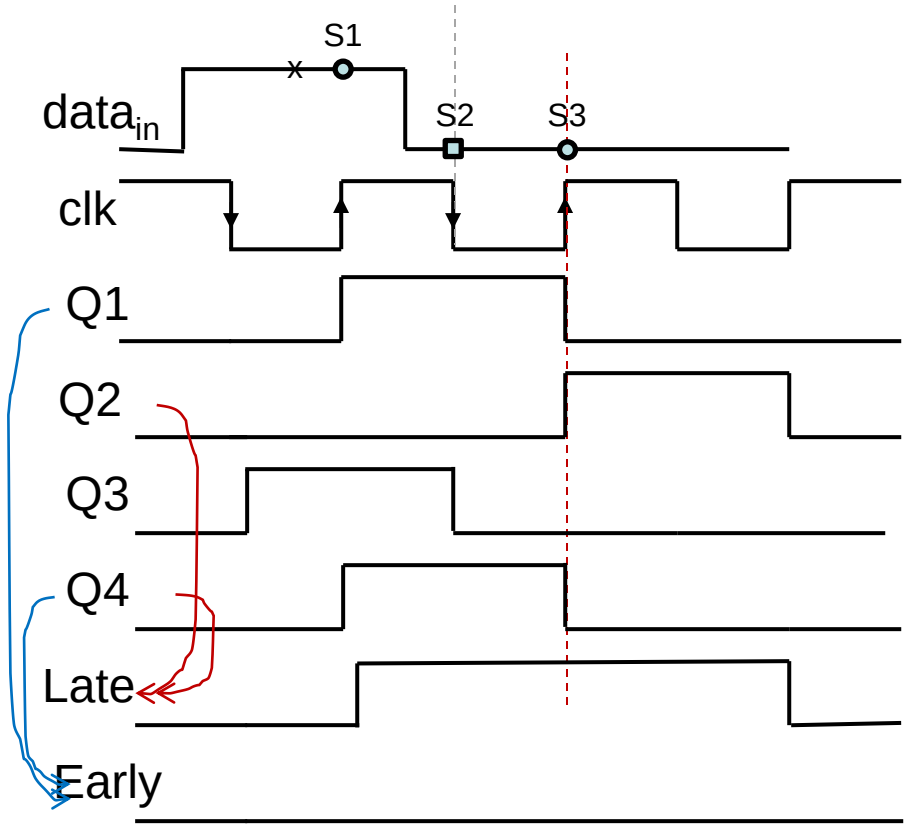
- Note: The Alexander Phase detector does not provide details about how much early or late is the clock
- The Alexander PD only provides the polarity information, hence it is a nonlinear "or bang-bang" phase detector

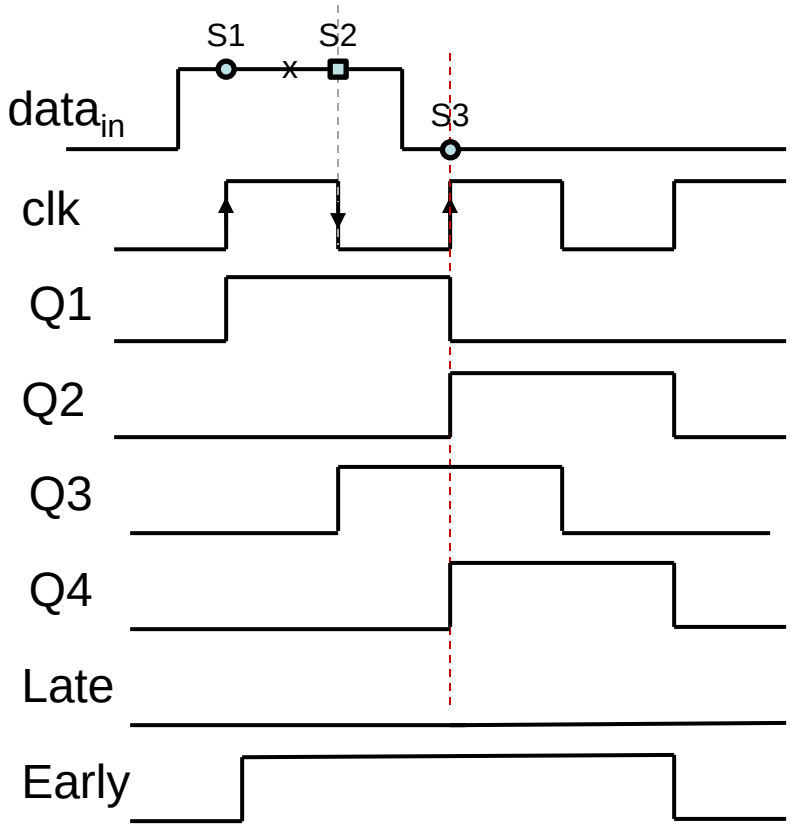
# Alexander Phase Detector (Cont'd)




- S1 and S3 are sampled at the rising edge of the clock
- The 2nd rising clock edge delays S1 by 1 clock cycle and is stores it at Q2
- S2 is sampled at the falling edge of the clock and the following rising edge delays it by 0.5 a clock cycle and stores it at Q4
- All the required samples are synchronized at t1 and are valid for 1 full clock cycle for comparison

# Alexander Phase Detector (Cont'd)



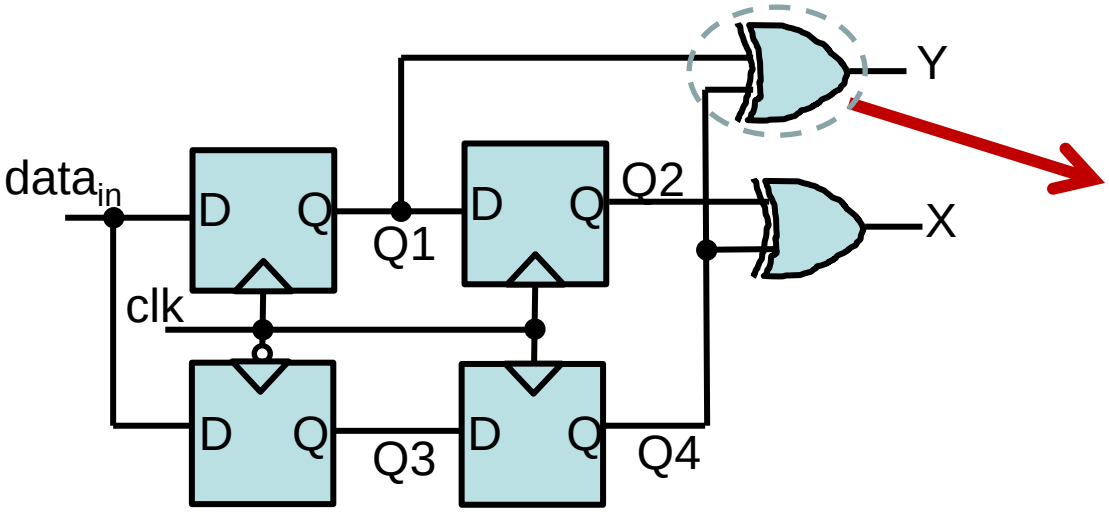

Late clock $\Delta\phi<0$
Late=1 & Early =0
Late-Early=+ve

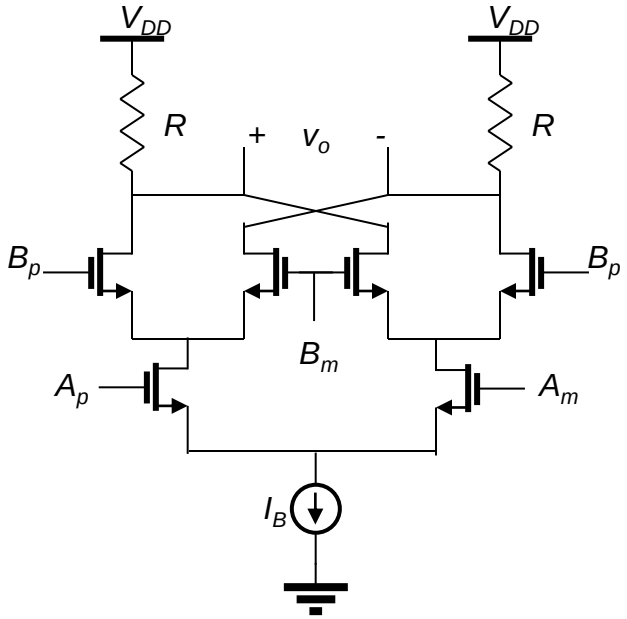
Early clock $\Delta\phi>0$
Late=0 & Early=1
(Late- Early)=-ve

# Alexander Phase Detector (Cont'd)

- The Early-Late pulses can be used to derive the VCO control voltage to slowdown/speed up the VCO
- The Alexander PD has a very high gain around $\Delta\phi=0$ (bang-bang PD)
- Advantages of Alexander PD:
  - PD automatically re-times the data at Q1 and Q2
  - In the absence of data transitions the PD generates no output pulses leaving the output at zero "tri-state PD". This will ensure the VCO control voltage is undisturbed, and will not result in VCO freq. drift as in binary DFF PDs

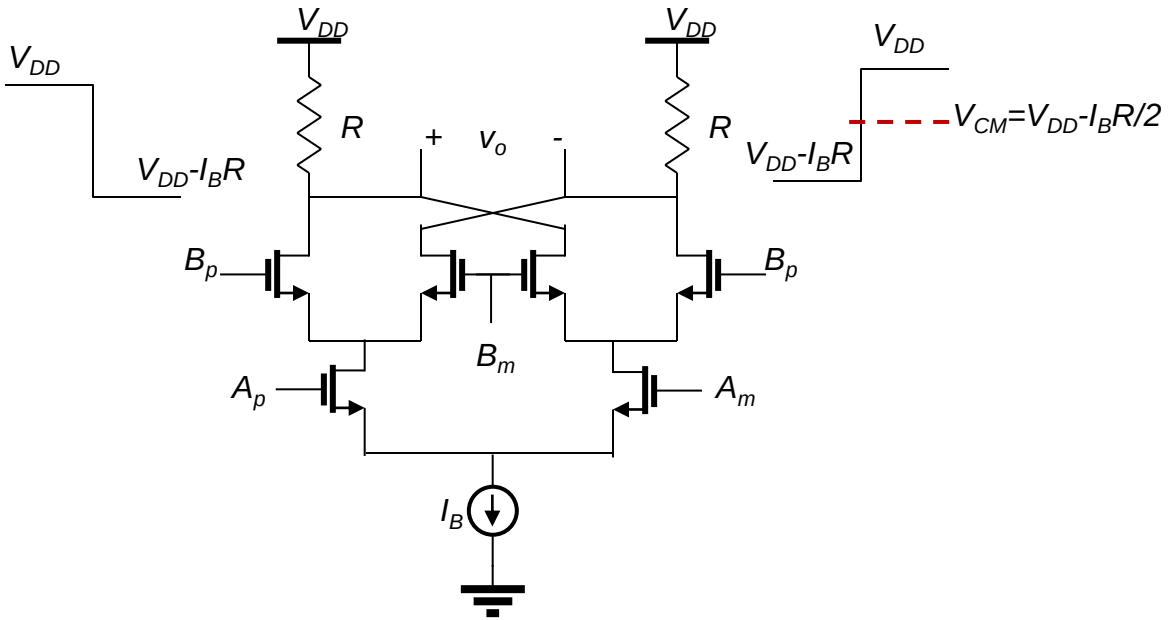
# Alexander Phase Detector (Cont'd)




- Advantages of Alexander PD (Cont'd):
  - ✓ When the CDR locks the sample S2 will always co-inside with the zero crossing resulting in meta-stability. In this case, if the edge FF can't resolve the edge samples the PD output will be near zero resulting in no updates to the VCO control voltage
  - ✓ The Alexander phase detector has very high gain close to lock which eliminates the need for a charge pump and eliminates the need to amplify very short pulses in linear PDs

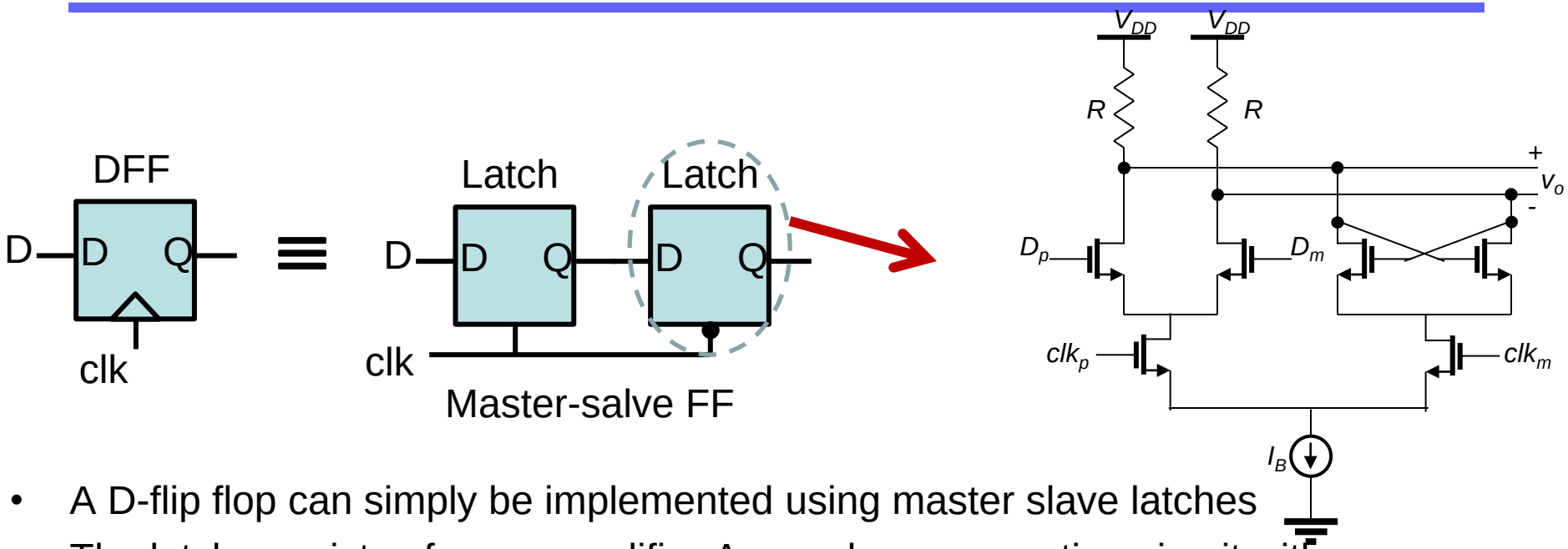
# High-Speed CML XOR




| A | B | Y |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

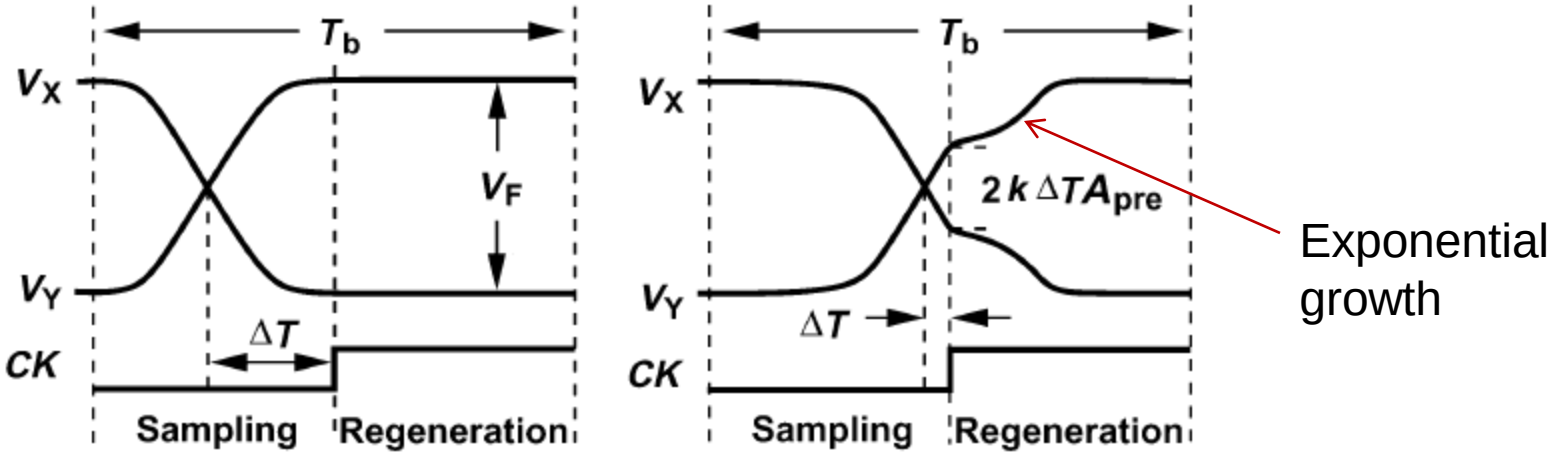
- Differential swing (p-p)=$2I_BR$ is determined by the load resistors and the bias current, which also sets the output common mode level
- Speed is mainly determined by the RC product at the output node
- To increase the speed and maintain the bandwidth the bias current must be increase → consume more power (or use inductive peaking techniques)

# High-Speed CML Samplers/Flip-Flops



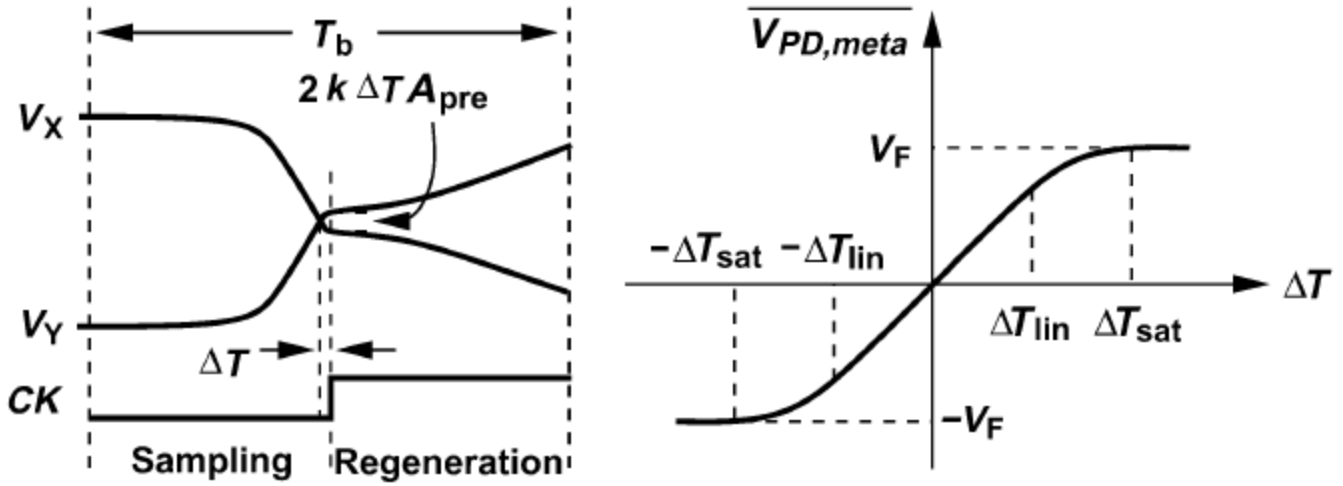

- A D-flip flop can simply be implemented using master slave latches
- The latch consists of a pre-amplifier $A_{pre}$ and a regeneration circuit with a re-generation time constant $\tau_{reg}$
- In track mode, clk is high and the output tracks the input with a gain $A_{pre}$, if input large enough the output will saturate at $v_{o\text{-}p}=V_F=I_BR$
- In the latch (regeneration) mode, the positive feedback results in an exponential increase in the output $v_o \propto v_{initial}\exp(+t/\tau_{reg})$
- Until the current is fully steered and $v_{o\text{-}p}=V_F=I_BR$

# High-Speed Latches




- Assume that the differential input changes with a slope of 2k, and the latch has sufficient BW such that its output follow the input with the same slope
- If the phase difference between the data and clk, $\Delta T$, is large the signal reaches $I_B R$ in the sampling mode and is held constant in latch mode
- If $2k\Delta TA_{pre} < V_F$, the circuit regeneratively amplifies the sampled level providing $V_{oPD,avg} < V_F$

# High-Speed Latches (Cont'd)




- If $\Delta T$ is sufficiently small the regeneration in Tb/2 doesn't amplify $2k\Delta TA_{pre}$ to $V_F$ leading to $V_{oPD,avg} << V_F$

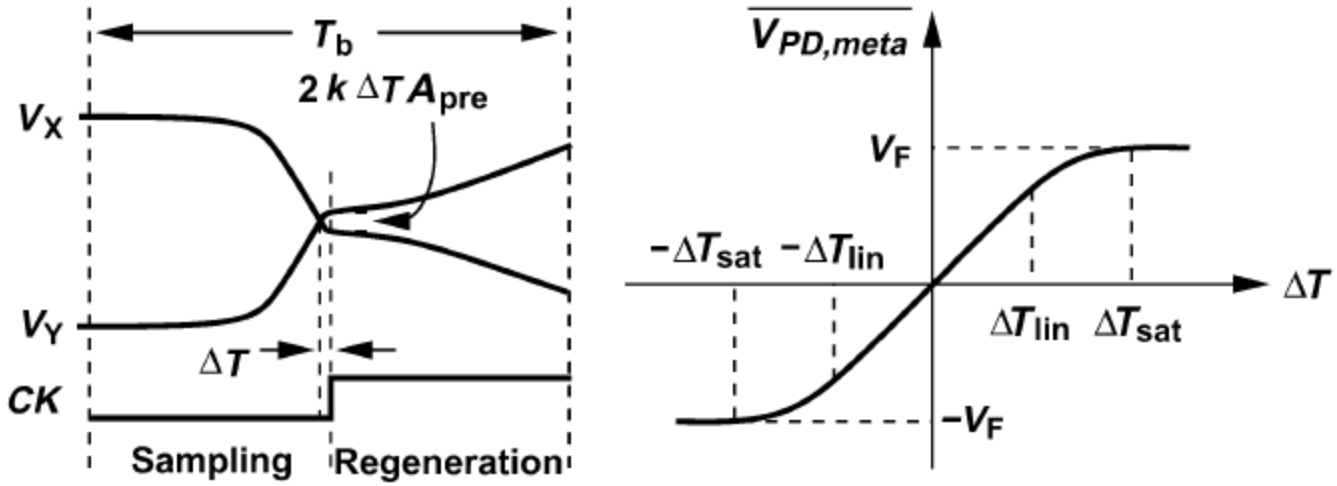
$$v_{oPD,avg} = \frac{1}{T_b}\int_0^{T_b/2} 2k\Delta TA_{pre}\exp\left(t/\tau_{reg}\right)dt = 2k\Delta TA_{pre}\frac{\tau_{reg}}{T_b}\exp\left(T_b/2\tau_{reg}\right)$$

- The average output is linearly proportional to $\Delta T$, as long as the final value at $T_b/2 < V_f$:

$$\Delta T_{lin} = V_F/2kA_{pre}\exp\left(T_b/2\tau_{reg}\right)$$

***[Ref]: "Analysis and Modeling of Bang-Bang Clock and data recovery circuit", JSSC Sept. 2004***

# High-Speed Latches (Cont'd)

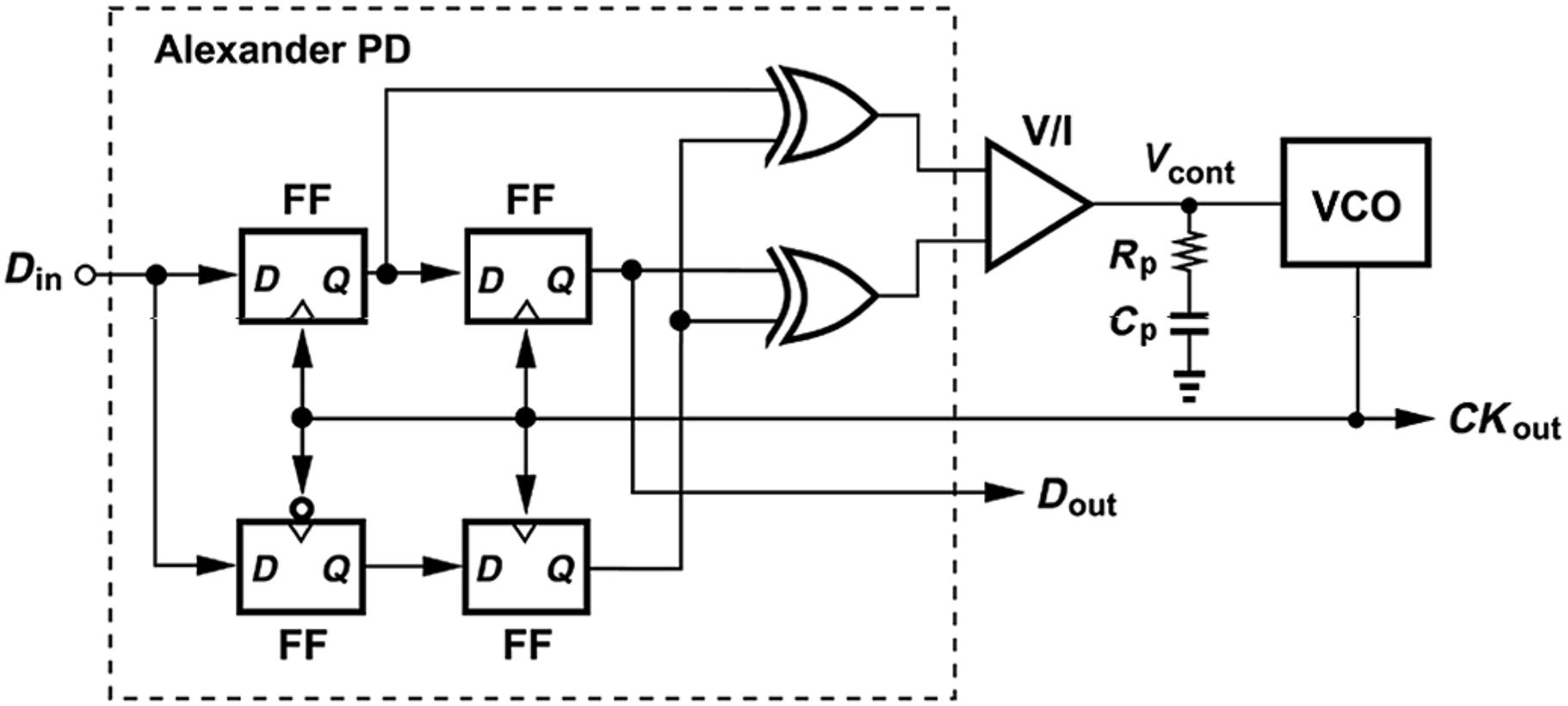



- For phase differences > $\Delta T_{lin}$, the slope of the characteristics starts to drop reaching zero when the pre-amplified values reaches $V_F$:

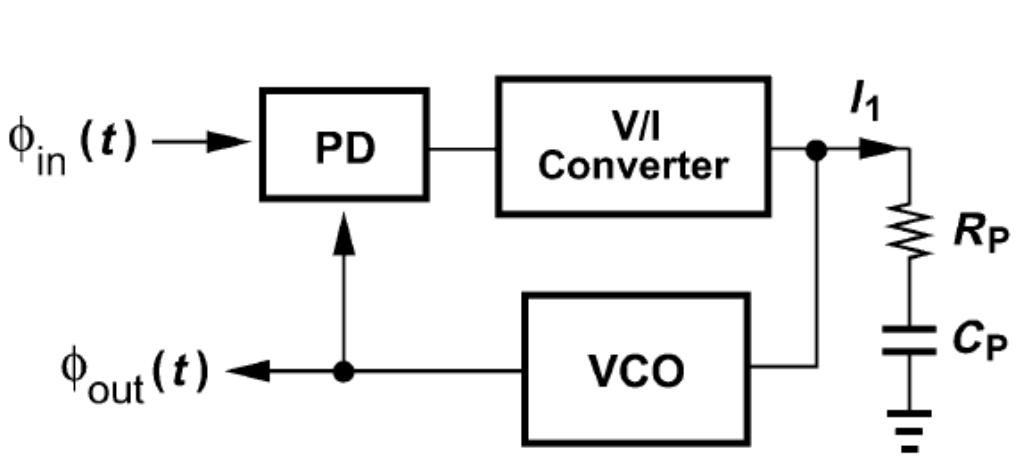
$$\Delta T_{sat} = V_F / 2kA_{pre}$$

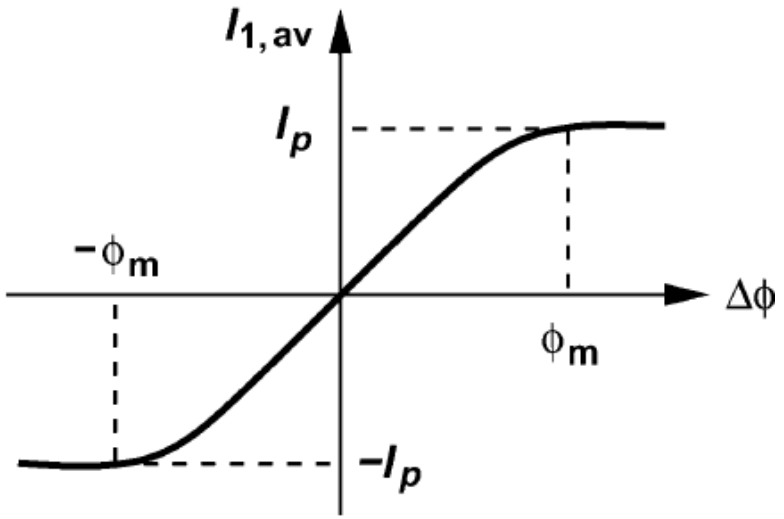
- For small values of input jitter, i.e. small $\Delta T$, a BB-CDR can be analyzed in a similar fashion to linear CDRs
- As the input jitter starts to increase the loop starts to become heavily nonlinear and the loop needs to be analyzed differently

# CDR Based on Alexander PD



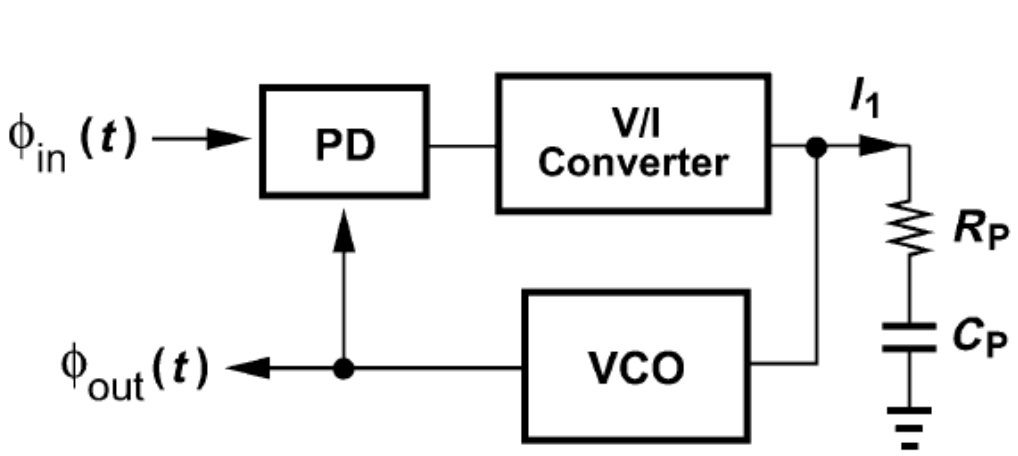
# Analysis of BB-PD CDRs

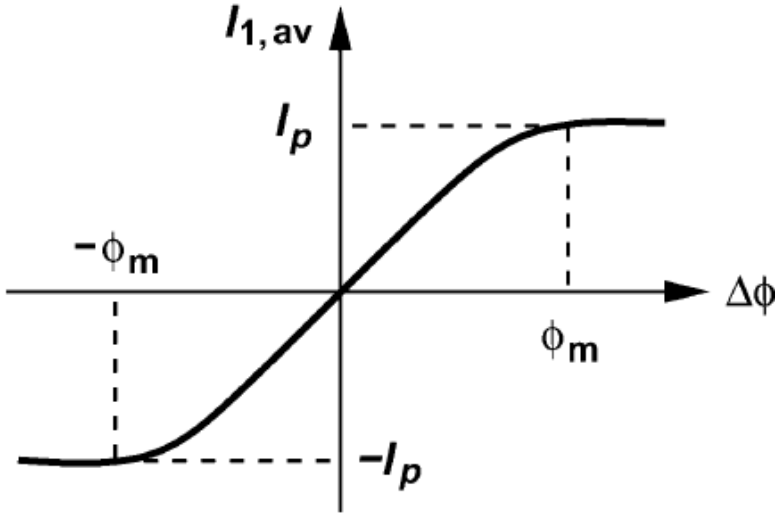



- BB-PD is follower by a V/I converter and a loop filter before the VCO
- BB phase detectors are non-linear and theoretically they provide very high gain in the vicinity of $\Delta\phi=0$
- However, the actual BB-PD exhibits a finite gain for small phase differences $|\Delta\phi|< \phi_m$ before it saturates, due to:
  - the meta-stability of the DFFs
  - the random jitter on the recovered clock

# Jitter Transfer of BB CDRs



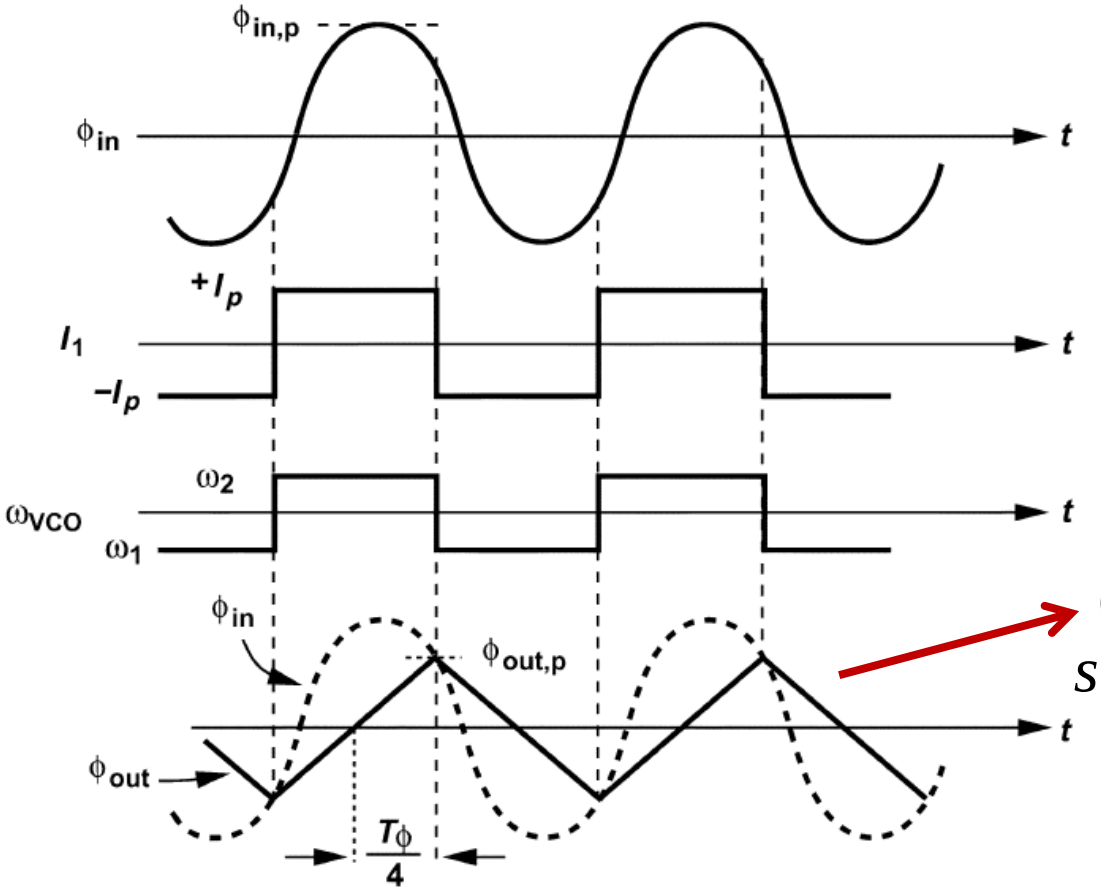

- To analyze jitter transfer, assume the input data phase $\phi_{in}(t)$ varies according to the following equation: $\phi_{in}(t)= \phi_{in,p}\cos(\omega_\phi t)$
- If $\phi_{in,p} < \phi_m$ then the PD operates in the *linear region* resulting in a standard second-order low-pass response for the loop "similar to linear PD CDRs"
- Indicating that the $\phi_{out}$ tracks $\phi_{in}$ as long as $\omega_\phi$ is less than the loop BW

***[Ref]: "Analysis and Modeling of Bang-Bang Clock and data recovery circuit", JSSC Sept. 2004***

# Jitter Transfer of BB CDRs (Cont'd)

- As $\phi_{in,p}$ exceeds $\phi_m$ the difference $\Delta\phi$ *may* exceed $\phi_m$ leading to nonlinear operation
- For low jitter frequencies $\omega_\phi$, $\phi_{out}$ tracks $\phi_{in}$ i.e. $\phi_{out}/\phi_{in}$~1, which makes $|\Delta\phi|<\phi_m$
- As the jitter frequency increases so does $\Delta\phi$, requiring the PD to pump more current in the loop filter, but the V/I current saturates beyond the linear region leading to *slewing*
- Assume $\phi_{in,p}>>\phi_m$ , such that $\Delta\phi$ changes polarity in every half cycle of $\omega_\phi$, and $I_1$ keeps jumps between $+I_p$ and $-I_p$
- Since the loop capacitor is typically very large its voltage is ~ constant and the VCO control voltage tracks $\pm I_p R$

# Jitter Transfer of BB CDRs (Cont'd)




CDR is slewing

$$slope = K_{VCO} I_P R$$

- A square wave on the VCO control voltage leads to a triangular wave on the VCO output phase

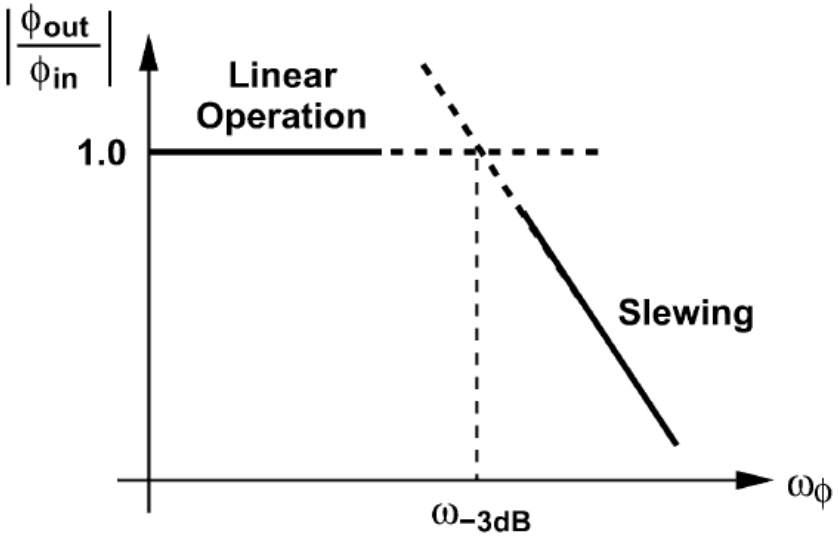
# Jitter Transfer of BB CDRs (Cont'd)

- The peak value of the output phase $\phi_{out}$ occurs after its integration for $T_\phi/4$, where $T_\phi=2\pi/\omega_\phi$:

$$\phi_{out,p} = \frac{K_{VCO} I_P R T_\phi}{4}$$

- Hence, the jitter transfer is obtained by dividing with the input jitter peak value:

$$\left| \frac{\phi_{out,p}}{\phi_{in,p}} \right| = \frac{\pi K_{VCO} I_P R}{2\phi_{in,p}\omega_\phi}$$




- The jitter transfer rolls of with a slope of -20dB/dec
- However, the jitter transfer is a function of the amplitude of the input jitter $\phi_{in,p}$
- As the jitter frequency decreases the CDR stops slewing and enters into the linear region $\phi_{out}=\phi_{in}$

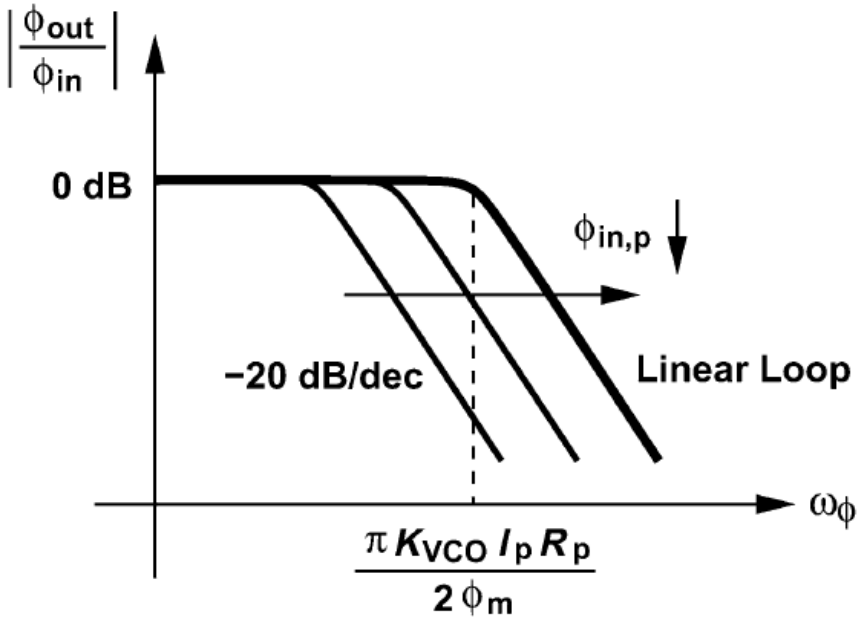
# Jitter Transfer of BB CDRs (Cont'd)

- Extrapolating the 2 regions we can get an expression for the 3dB BW of the loop:

$$\omega_{3dB} = \frac{\pi K_{VCO} I_P R}{2\phi_{in,p}}$$

- It is possible to approximate the entire jitter transfer as:

$$\frac{\phi_{out}}{\phi_{in}}(s) = \frac{1}{1 + s/\omega_{3dB}}$$

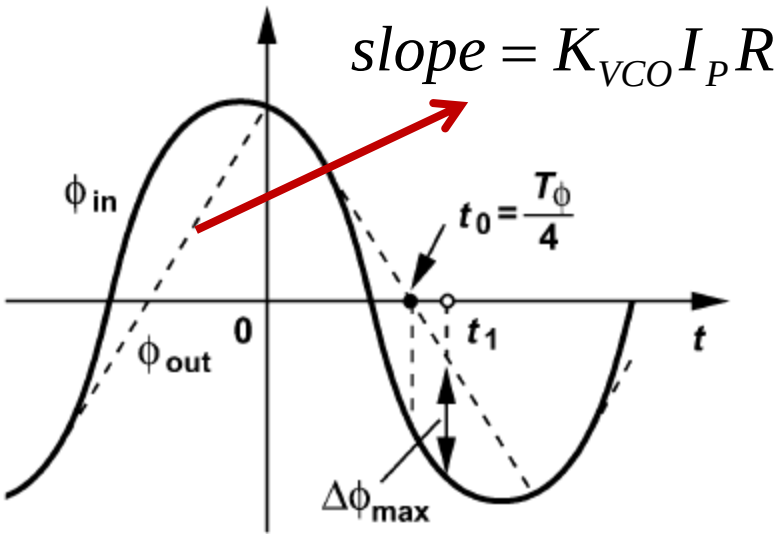



- The BB-CDR loop BW is a function of the input jitter amplitude $\phi_{in,p}$
- The jitter transfer approaches that of the linear loop as $\phi_{in,p}$ decreases

# Jitter Tolerance in BB CDRs

- JTOL is the maximum input jitter that CDR can tolerate without increasing BER for different jitter frequencies
- Phase error $\Delta\phi_{max}$ approaches $\pi$ (0.5UI) for BER to rapidly increase
- CDR has to be slewing in order for errors to occur

$$\phi_{in} = \phi_{in,p}\cos\left(\omega_\phi t + \delta\right)$$




- $\Delta\phi_{max}$ occurs at $t_1 \approx$ ($\Delta\phi$ at $t_0 \approx T_\phi/4$) (approx. simplifies the analysis)
- CDR has to be slewing in order for errors to occur

$$\Delta\phi_{\max} \approx \Delta\phi(t_o) = \left|\phi_{in,p}\cos\left(\omega_\phi \times T_\phi/4 + \delta\right)\right|$$

- $\phi_{in}(t)$ and $\phi_{out}(t)$ have the same at t= 0:

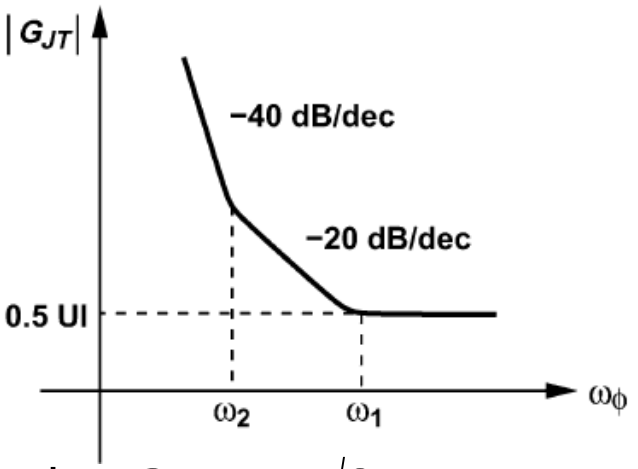
$$K_{VCO} I_P R T_\phi/4 = \phi_{in,p}\cos\left(\delta\right)$$

# Jitter Tolerance in BB CDRs (Cont'd)

$$\Delta\phi_{\max} \approx \frac{1}{2\omega_\phi}\sqrt{4\omega_\phi^2\phi_{in,p}^2 - \pi^2 K_{VCO}^2 I_P^2 R^2} = \pi$$

- Equating $\Delta\phi_{max}$ to $\pi$ results in the maximum tolerable input jitter

$$|G_{JT}| = \pi\sqrt{1+\frac{K_{VCO}^2 I_P^2 R^2}{4\omega_\phi^2}}$$




- For low values of $\omega_\phi$, $G_{JT}$ drops by 20dB/dec
- For higher values of $\omega_\phi$, $G_{JT}$ approaches $\pi$ (0.5UI)
- The corner frequency can be calculate by equating $G_{JT}$ to $\pi\sqrt{2}$

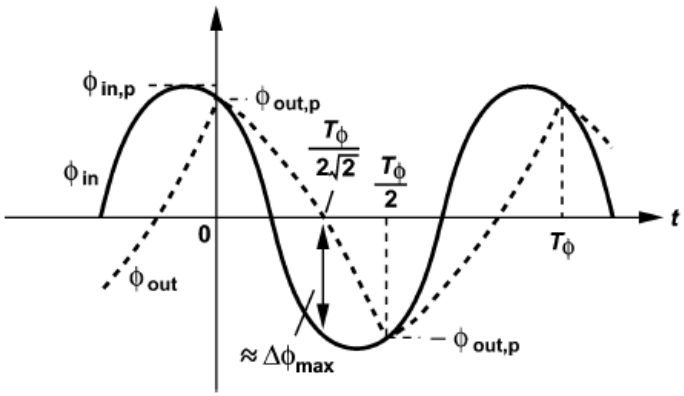
$$\omega_1 = K_{VCO} I_P R/2$$

- Our analysis has assumed linear slewing, i.e. the voltage across the capacitor was assumed constant and the change in the control voltage is due to $I_P R$

# Jitter Tolerance in BB CDRs (Cont'd)

- For jitter frequencies lower than 1/RC nonlinear slewing starts to take place, and the voltage across the capacitor starts to yield a parabolic shape for $\phi_{out}(t)$
- For sufficiently low jitter frequencies we can neglect the effect of the linear term compared to the parabolic term
- Performing the analysis in a similar method results in:

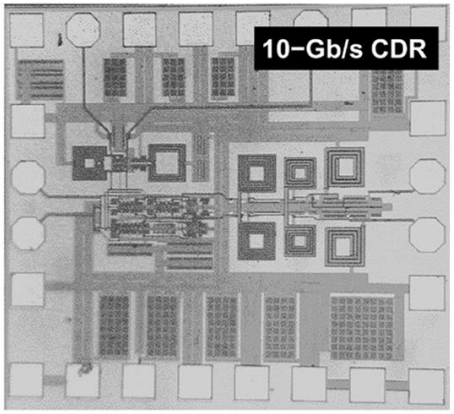
$$\left|G_{JT}\right| = 1.26\frac{K_{VCO}I_P\pi^2}{4C_p\omega_\phi^2}$$

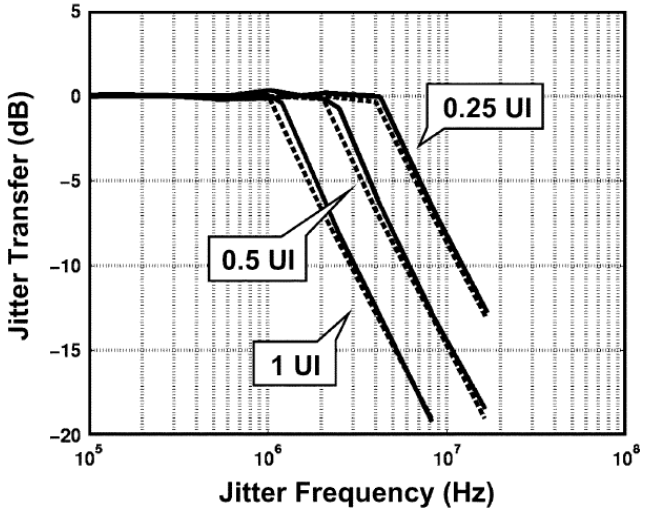


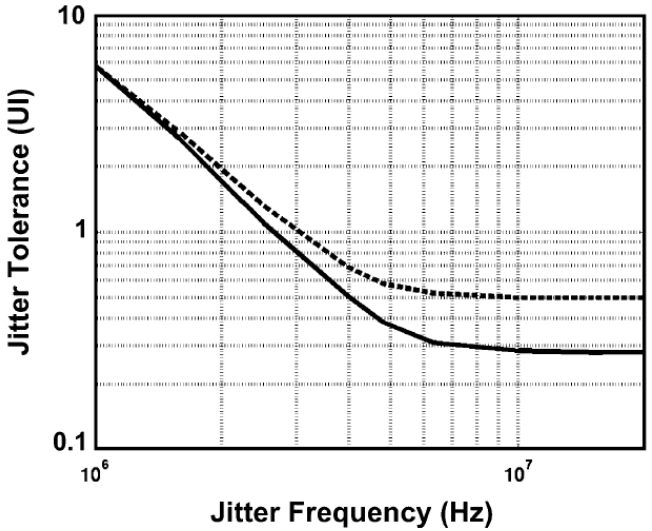

- $G_{JT}$ drops by 40dB/dec, and the corner frequency between the 2 regions can be found by extrapolating the 2 equations

$$\omega_2 = 0.63\pi/RC_p$$

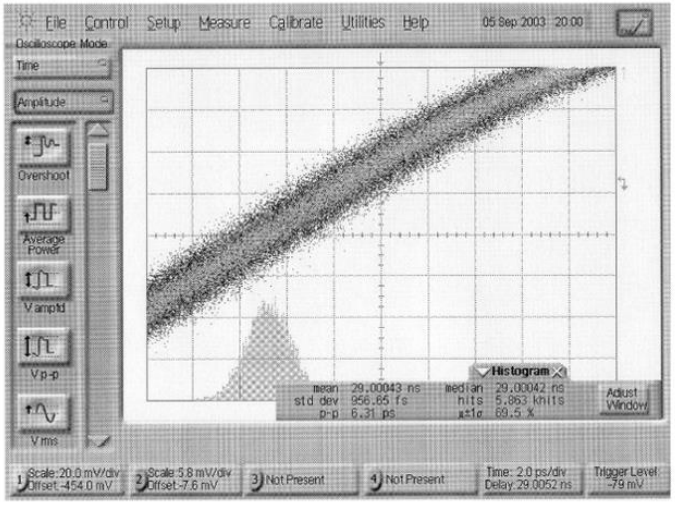
# JSSC 2004: 10Gb/s Alexander PD CDR



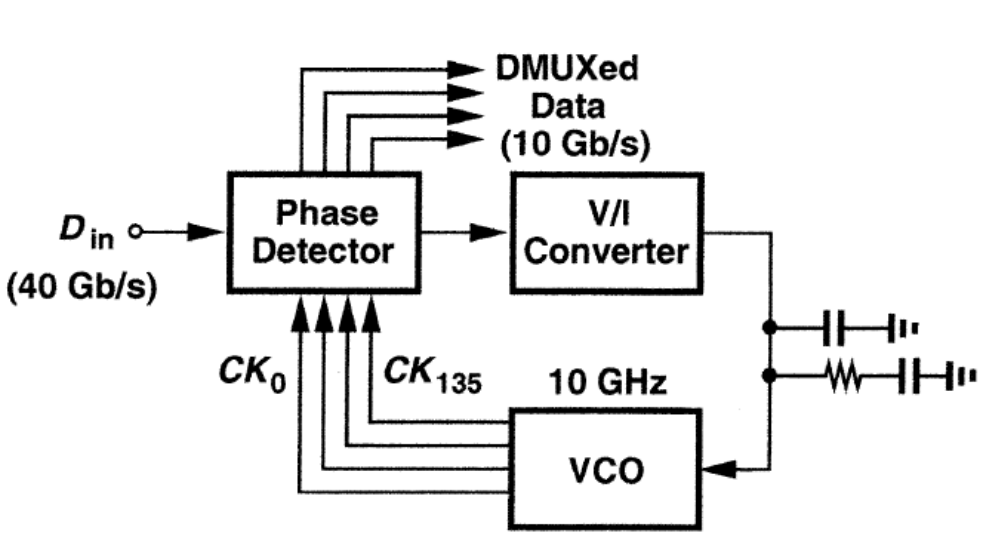



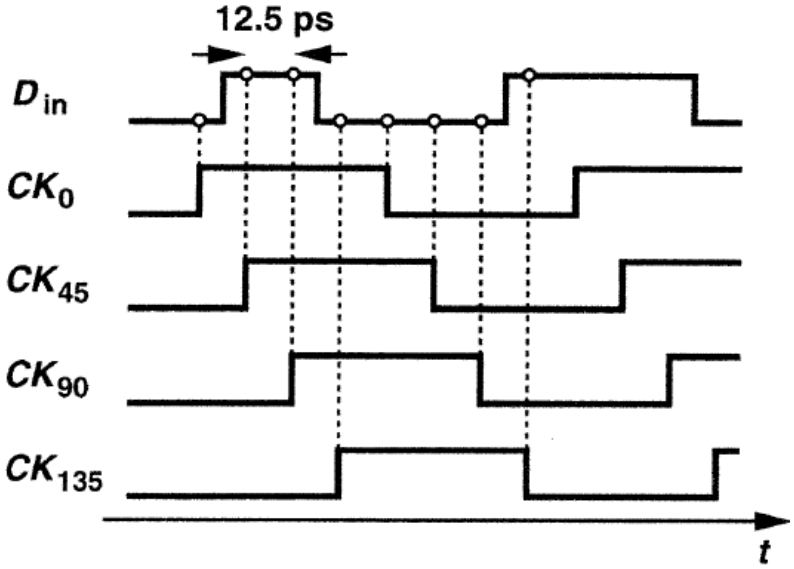




- 10Gb/s measurements show the bandwidth of the jitter transfer inversely scales linearly with input jitter
- Measured high frequency jitter tol. is worse than 0.5UI (theoretical limit)
- Recovered clock jitter histogram gives jitter pp and rms values



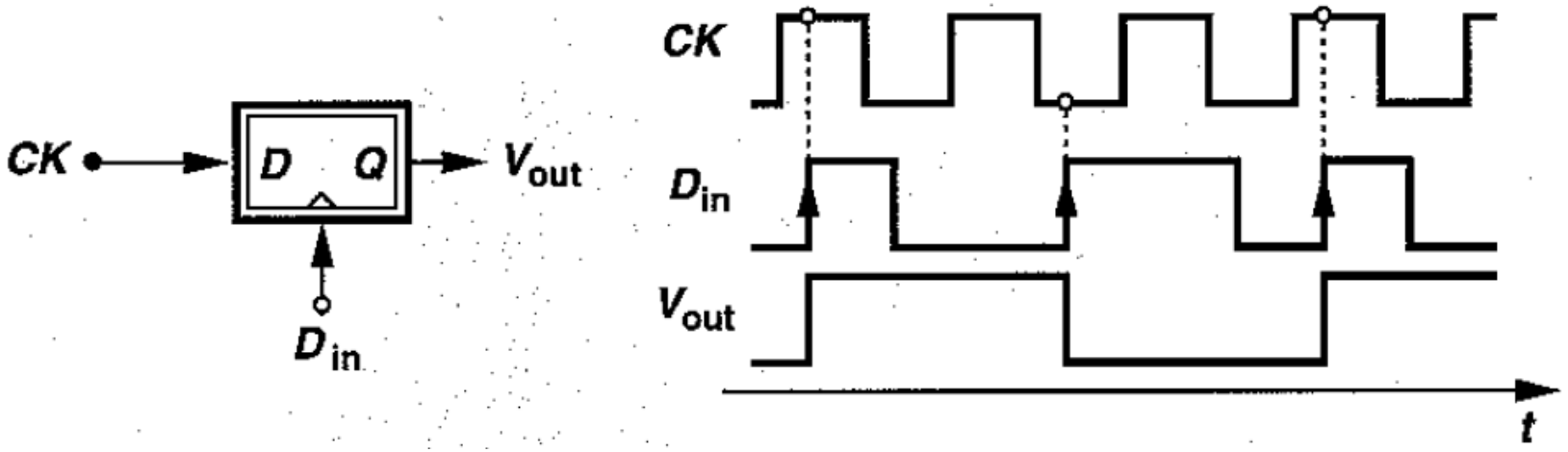
# Half-Rate Phase Detectors



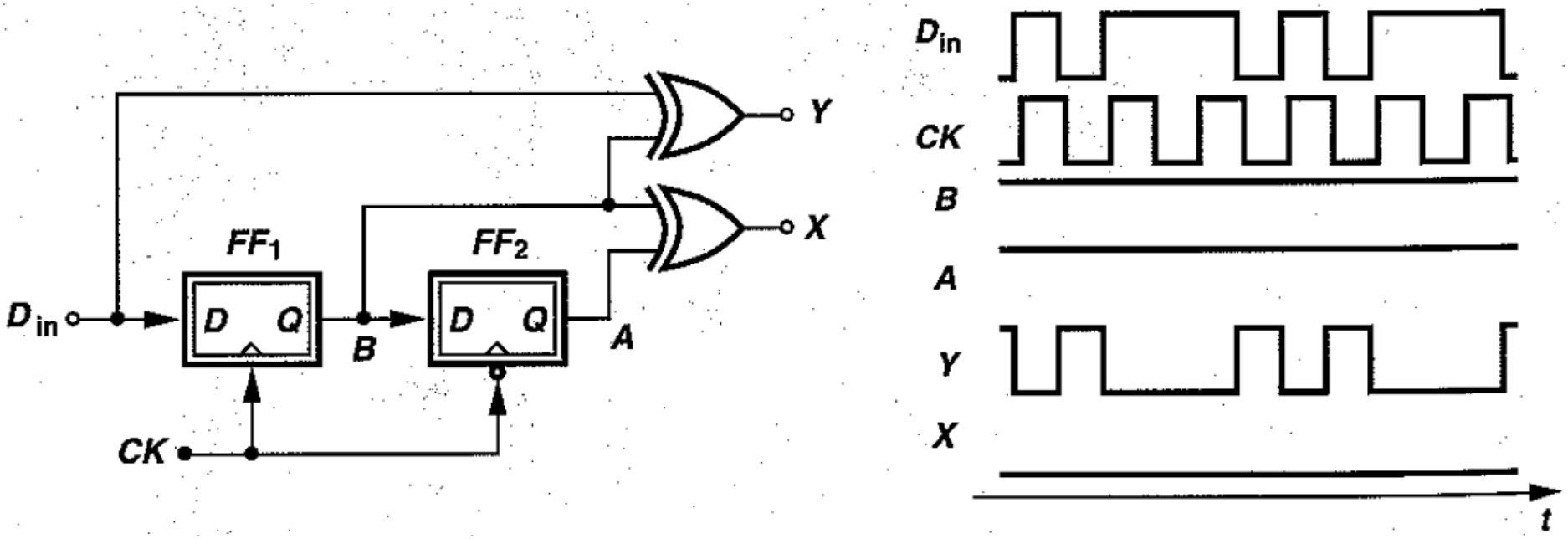

- Oscillators are hard to design at very high frequencies with a wide tuning range and good jitter performance
- CDRs can sense full-rate data but employ a VCO running at a fraction of the speed (half-rate, quarter-rate,…)
- This also relaxes the speed requirement on the PDs (extra area!)
- Picture shows a quarter rate architecture with a VCO running at 10GHz to receive a 40Gbps signal

# Failure of DFF as a Half-rate PD



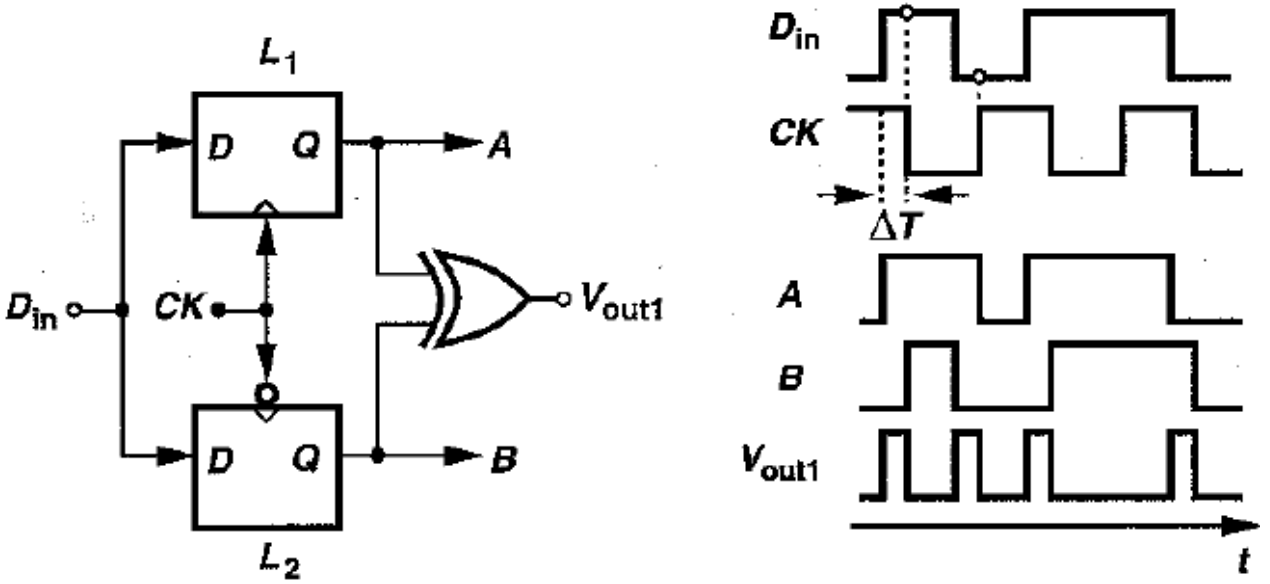

- A DFF sensing a half-rate clock with a constant phase difference relative to the full-rate data results in both positive and negative pulses at the PD output
- DFF can't work as a half-rate PD

# Failure of Hogge PD as a Half-rate PD



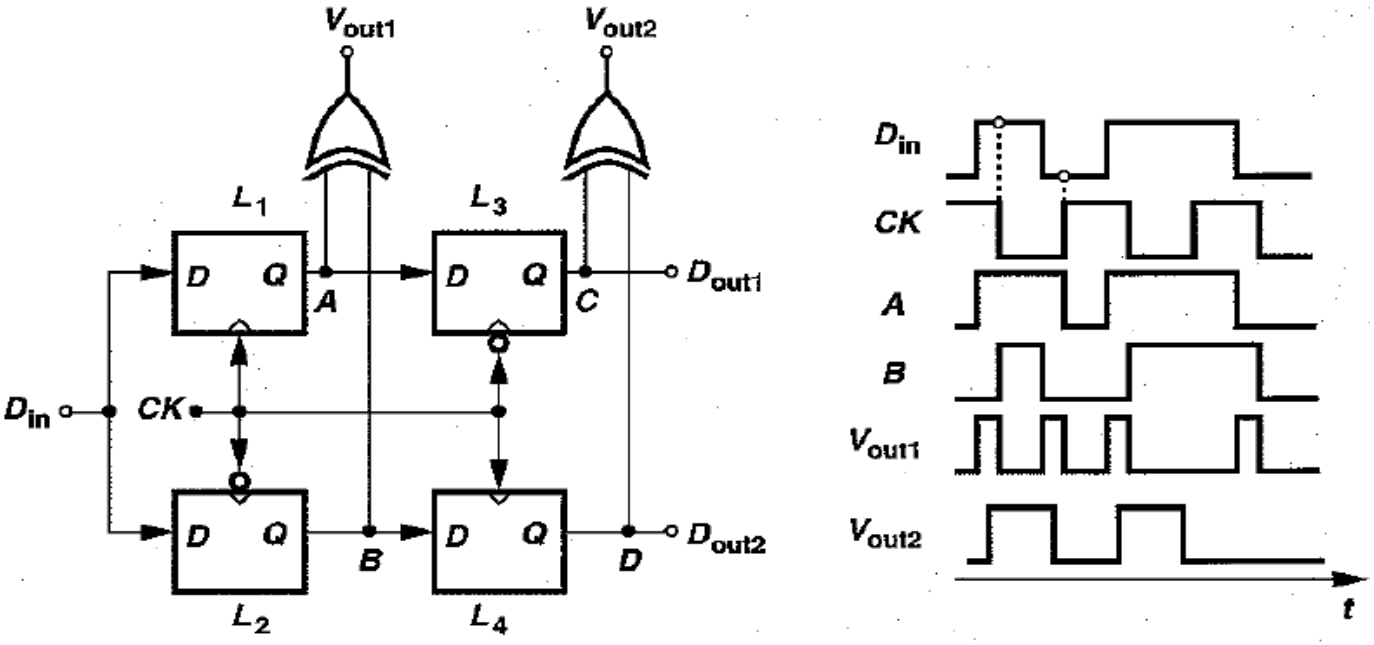

- Since half of the clock transitions are absent, the clock can continue to sample a high (or a low) level failing to detect data transitions
- The proportional and reference pulses are invalid
- Date transitions can be detected if both clock edges of the half rate clock are used to sample the data!

# Half-rate Hogge Phase Detector




- Each latch is transparent for half of the clock cycle passing data transitions to its output and is latched on the other half cycle
- L1 is transparent when CK is high→$L_1$ produces a pulse $T_{ck}/2+\Delta T$ wide
- L2 is transparent when CK is low→$L_2$ produces a pulse $T_{ck}/2-\Delta T$ wide
- A XOR B produces pulses $\Delta T$ wide on each data transition

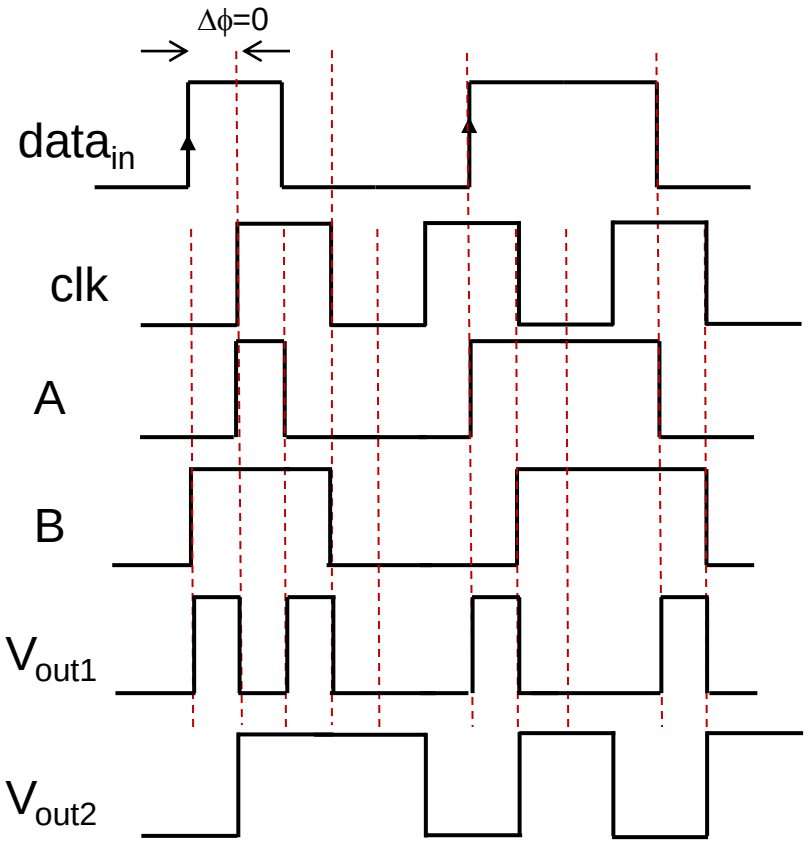
# Half-rate Hogge Phase Detector (Cont'd)



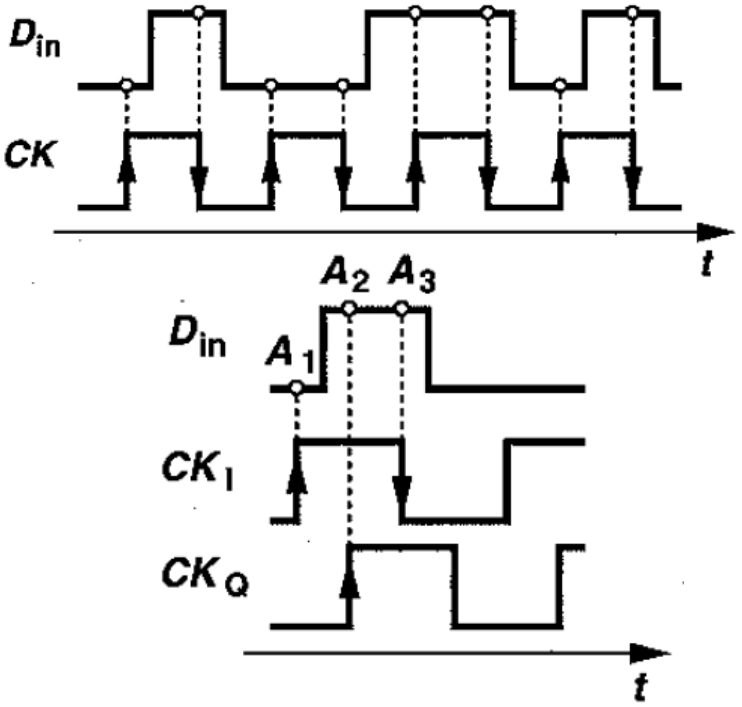

- A complete Hogge PD must generate reference pulses to uniquely represent the phase error for any data transition density
- The two additional latches L3 & L4 together with L1 & L2 respectively form a master slave flip-flop
- If there is a data transition C XOR D generates a pulse $T_{ck}/2$ wide →reference pulses

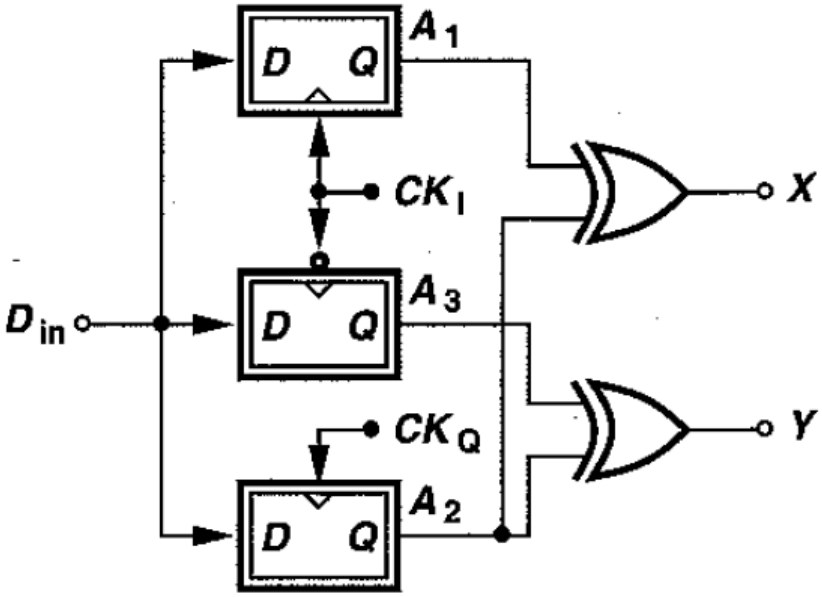
# Half-rate Hogge Phase Detector (Cont'd)

- At lock conditions, the clock is aligned to the center of the data eye
- Then the proportional pulses are $T_{CK}/4$ wide (reference pulses are $T_{CK}/2$)
- The output of the reference XOR has to be scaled down by a factor of 2 in the charge pump to correctly align the clock and data
- The half rate PD provides retimed and also de-multiplexed data by 2
- The outputs are available as 2 data streams at L3 and L4



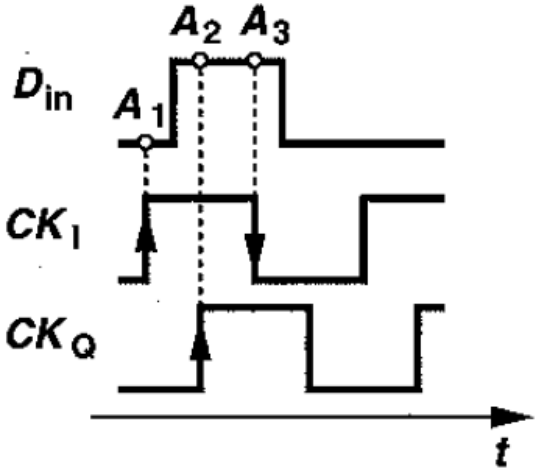
# Half-rate Alexander Phase Detector

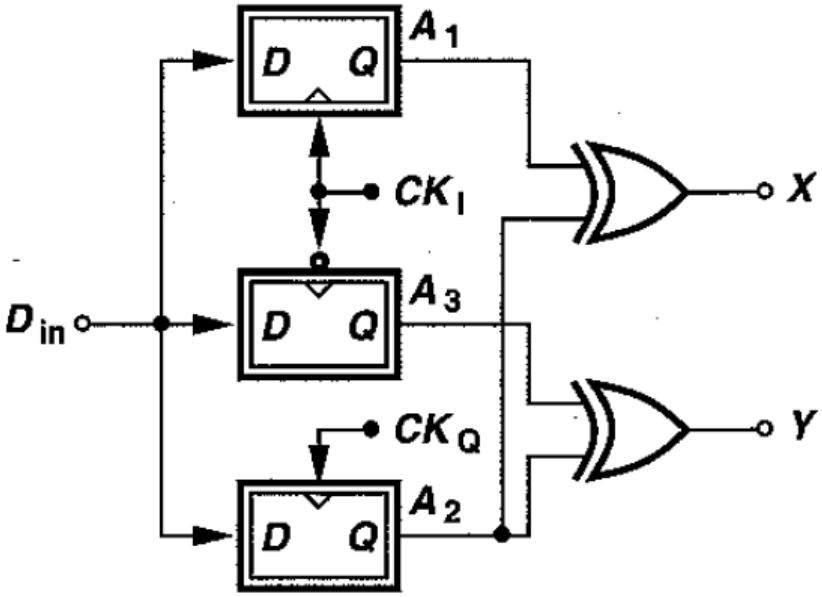



- Alexander phase detector already requires sampling on both edges for full-rate operation (for data and edge information)
- It must employ additional clock phases to operate in half-rate mode
- The data must be sampled using an in-phase $CK_I$ and edge samples using a quadrature clock $CK_Q$

# Half-rate Alexander Phase Detector (Cont'd)




- A1, A2, & A3 represent the consecutive samples in the full-rate PD
- The 2 XORs produce the up and down pulses
- Under lock condition, the rising edge of $CK_Q$ occurs at the data zero crossing
- Additional re-timing latches are usually required to eliminate the skew between A1-A3 by delaying A1 by $T_{CK}/2$ and A2 by $T_{CK}/4$