/testbench/Reset [[]													I	
/testbench/Clk _[-						-			_				
/testbench/Proccessor/PC/PC_Out	0	1	<u> </u>	2		3	†	4	<u> </u>	5		6		7
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/testbench/Proccessor/RF/Read_Addr_1	0	13		8		13	†	0						-
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/testbench/Proccessor/ALU/OP1	0			13		34		13						
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