Technical Note

DDR SDRAM Point-to-Point Simulation Process

Introduction

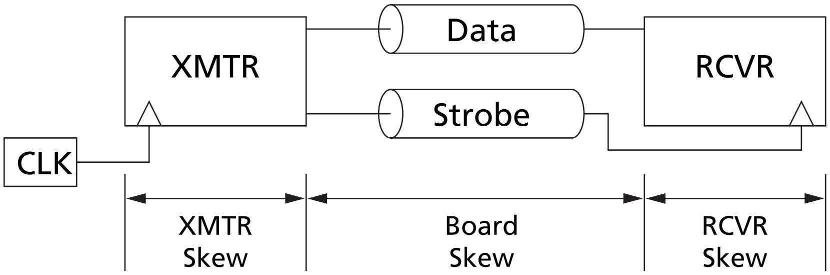
This technical note covers rarely addressed areas of the DDR SDRAM point-to-point simulation process:

1. Signal integrity
2. Board skew and the contributing factors
3. Return path discontinuities

As bus speeds have increased, signal integrity analysis has become more important. A detailed model of the design reduces the total cost of the development because it ensures system functionality from the start. A model maximizes performance while reducing test and debug time. Signal integrity analysis brings a better product to market sooner.

Moving from a synchronous-based architecture to a source-synchronous architecture eliminates the flight-time delay that restricts speed. DDR SDRAM devices use a bidirectional strobe as a data clock to eliminate flight-time delays. In a source-synchronous architecture such as DDR, the board skew is a major limiter of speed (see Figure 1). The goal of signal integrity analysis is to minimize skew.

Figure 1: Source-Synchronous Bus



Signal Integrity Process

The signal integrity process can be divided into two categories: performance requirements and assumptions. The performance requirements include items such as the timing budget and number of loads. The assumptions include more of the board-level components such as topology and lossy lines. Once the performance requirements and assumptions are determined, the design is ready to be simulated using the models provided by Micron.

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Performance Requirements

The overall timing budget determines the data-valid window, including the skew for the board. Table 1 illustrates a typical top-level timing budget. The timing budget starts with the full cycle time allowed, in this case a 7.5ns clock, which equals a 3.75ns cycle time. It is then split up for the setup and hold portions. The transmitter and receiver skews can be obtained from the device data sheet.

For example, the transmitter skew during a READ command from a DDR SDRAM device can be obtained from the timing parameters ^{t}DQSQ and ^{t}QH. Subtract the transmitter skew from the available bit time to determine the maximum data-valid window available before the board skew is factored in. The receiver skew in the example represents the required data-valid window by the DDR SDRAM controller.

The components that make up the board-skew budget have to include ISI, VREF noise, path length mismatch, crosstalk, CIN mismatch, and termination resistor tolerance.

Table 1: Top-Level Timing Budget Example

Component	Setup	Hold	Units	Comments
Total budget	1,875	1,875	ps	266 MHz period = 3.75ns half period
Transmitter skew	-790	-790	ps	Vendor data sheet
Receiver skew	-500	-500	ps	Vendor data sheet
Board skew budget	585	585	ps	Skew available for the board

We will cover all of the components in the board-level skew in detail in the Assumptions section of this document.

Another performance requirement is voltage margin. Voltage margin is the amount of margin between the required logic levels and the actual levels detected by the device. It is defined by the supply voltage and the logic input levels (see Figure 2). Signal transitions must pass through the AC input logic level and stay within at least the DC/AC region to be valid. For DDR devices, the input level is VREF ±150mV, and the AC level is VREF ±300mV. As show in Figure 3, both the skew and logic levels are used to determine the data-valid window. The AC level is referenced at the beginning of the eye where the signal switches, and it must pass through the AC level to latch.

Figure 2: DDR Input Logic Levels

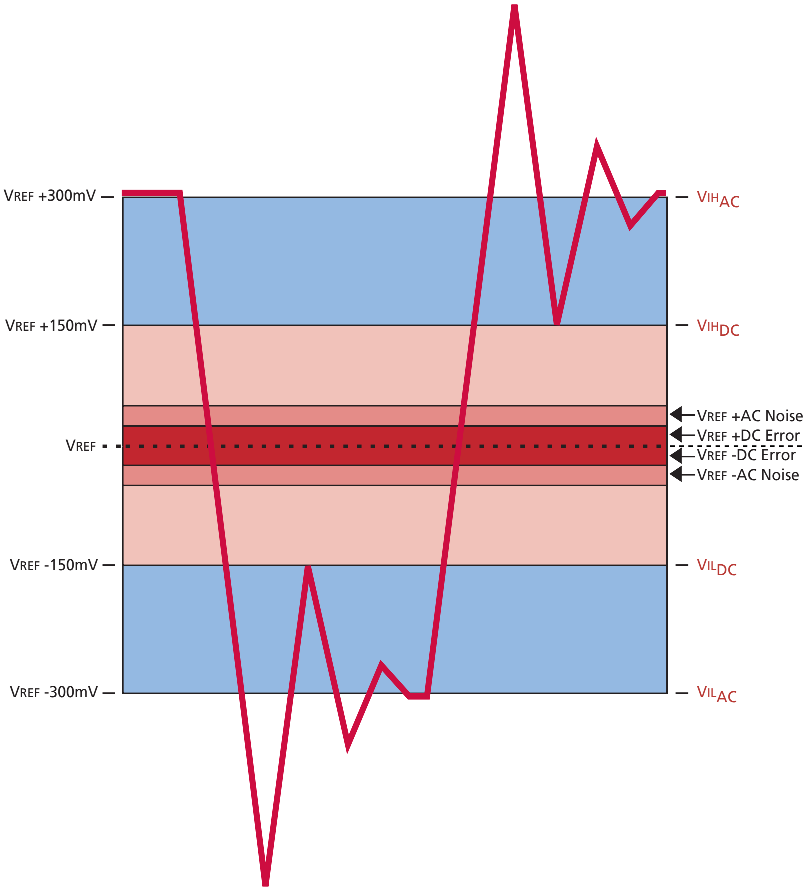
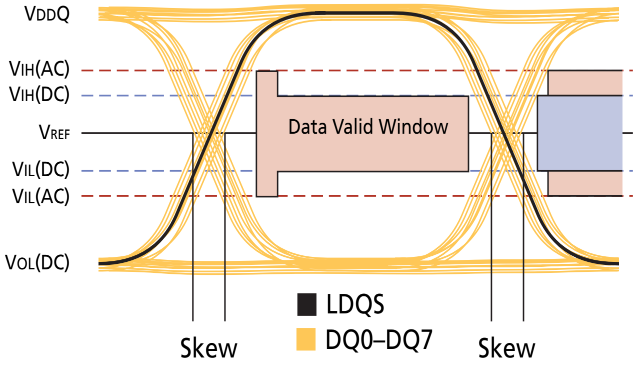


Figure 3: DC Data-Valid Window Showing Voltage Margins



Assumptions

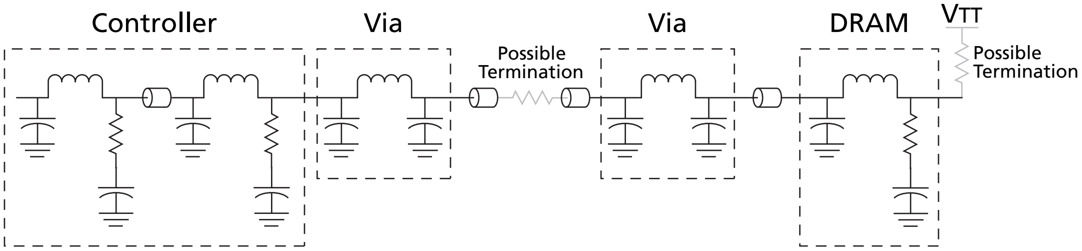
Assumptions in the signal integrity process are typically based on a combination of previous experience, current industry practice, and recent research. Staying aware of industry practices and current research helps avoid incorrect assumptions. Examples of assumptions include via effects and lossy transmission lines. Figure 4 illustrates a typical point-to-point circuit model. This model includes drivers, receivers, package parasitic for both the DDR SDRAM and the ASIC, vias, possible termination, and transmission lines.

Micron provides both SPICE and IBIS models for all of its DDR SDRAM devices on its Web site. SPICE models are transistor-level models and tend to be more accurate than IBIS models, but they are slower. IBIS models are behavior-based models that are fast, but they may not reproduce lab failures. The package parasitics need to be included in the models and should always be used for simulation.

When it comes to receiver models, the choices include a SPICE model, an IBIS model, or a lumped capacitor model. The lumped capacitor model offers a good approximation to the SPICE or IBIS options at the speeds that DDR SDRAM runs. This model saves time and is an industry standard in modeled DDR systems. In most cases, the time saved using a lumped capacitor model is worth the slight loss in accuracy.

The traces or transmission lines are created from a combination of trace impedance, delay, physical constants, and the sectional geometry. While single line models are used for most simulation, coupled models need to be used to simulate the effects of crosstalk. Lossy lines should also be used when simulating DDR SDRAM systems for the most accurate results; they tend to match lab data better than lossless lines.

Figure 4: Typical Point-to-Point Circuit



Using via models improves the accuracy of the models without affecting the simulation time. Industry-accepted values can be found in multiple sources, including Johnson and Graham’s *High-Speed Digital Design*. To prevent adding skew, the number of vias must match across the byte lane. For a high-speed bus, all circuit components should be included in the simulation to ensure accuracy.

Simulation

The main purpose of simulation is to ensure that all of the signals meet the bus specification before hardware is built. It is also used to optimize the design and to obtain numbers for the timing budget. Simulation, which takes place throughout the design cycle, can be separated into three categories that clarify the simulation goals:

1. Sizing to determine the basic layout
2. Sensitivity analysis to fine-tune the design prior to building hardware
3. Design verification once the hardware is built

The typical simulation process starts with gathering all of the required performance data: speed, desired loading, bus specification, assumed topology, and PVT (process, voltage, and temperature) conditions. Once the performance requirements are established, a circuit model is built and the initial sizing simulations are performed to see if the received signals meet the established requirements. The signals should be checked at all of the receiver locations. A pseudo-random bit pattern should be included as a minimum to check the data eye for the sizing measurements. The pattern should include several cycles switching at a maximum and minimum rate to fill in the spectral content of the source—a one-cycle “high” in the middle of a long “low” or a one-cycle “low” in the middle of a long “high,” for example. Bit patterns can be much more extensive; these are merely minimum requirements. A good pattern will cover a 2^5 bit sequence and its complement. In other words, the eye diagram source should have a pulse train containing every pattern in a 5-bit truth table, followed by an exact complement of the first pulse train. The eye diagram can be obtained by overlaying the signals.

If the initial sizing simulations meet the established requirements, you can move on to sensitivity analysis and creating the timing budget. If the sizing simulation does not meet the established requirements, some modifications to the design are required. A few of the key aspects to look at include topology, termination, loading, and drive strength. Once changes are made, the simulation can be run again to ensure that all of the established requirements are met. The initial sizing will help determine the functional layout, while the sensitivity analysis will test the layout over a wide range of operating conditions.

Sensitivity analysis is used to test the design over a wide range of operating conditions. It locates problems and optimizes system performance. The variables included in sensitivity analysis are topology, termination scheme, board impedance, loading, and PVT (process, voltage, and temperature) conditions. Topology variation will help determine the effects of possible routing variations and mismatch in the trace lengths. The termination scheme should also be varied to account for the tolerance in the resistors. Trace impedance tolerance must be accounted for during the simulation process. Loading is not as important in point-to-point simulation, but the worst-case variations must be accounted for in the simulation process. The loading variations from pin to pin can introduce skew. Corner-testing PVT conditions ensures that the designs work under all operating temperatures. The worst-case corners include fast or slow process, high or low temperature, and high or low voltage.

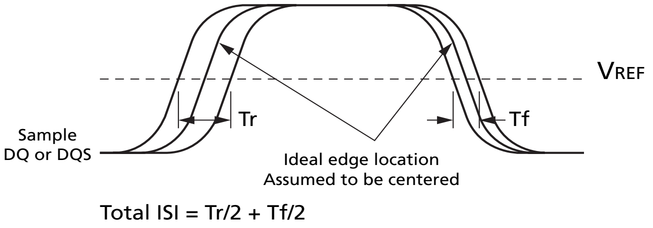
Board Skew

The components that make up the board-skew budget include ISI, VREF noise, path length mismatch, crosstalk, CIN mismatch, and termination resistor tolerance. When looking at the individual elements of the board skew, variations must be made for both the DQ pins and the DQS to cover all the corners.

ISI

Although ISI is caused by cycling the bus faster than it can settle, reducing bus speed is certainly not a preferred ISI reduction technique. ISI may cause both strobe and data edges to move; therefore, both strobe and data ISI must be included in the timing budget. For timing budget purposes, the total ISI is split equally between setup and hold as shown in Figure 5. The total ISI is defined as Tr/2 + Tf/2, with Tr and Tf measured at VREF. To keep ISI to a minimum, the termination and layout must be optimized. To minimize ISI, repeat sizing and sensitivity analysis until an optimal solution is found.

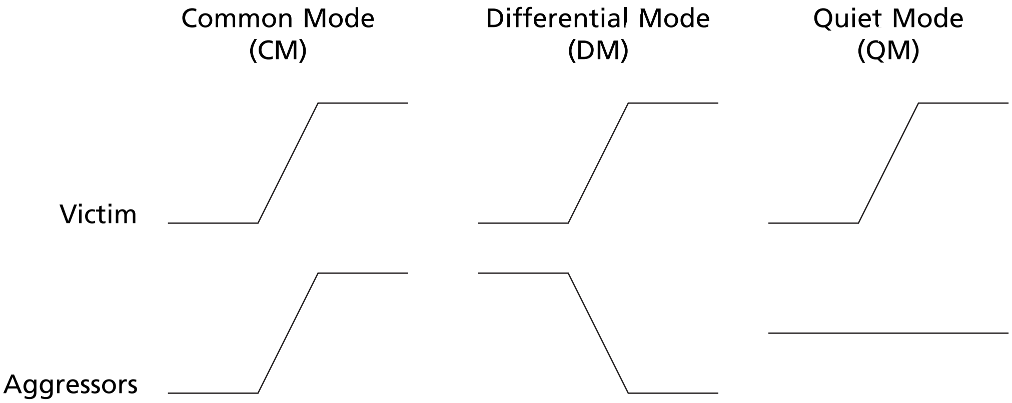
Figure 5: ISI



Crosstalk

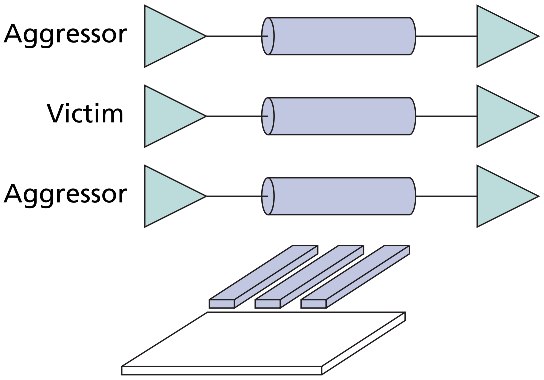
Coupling on the board and in the package between adjacent traces causes jitter, which causes crosstalk. Crosstalk can cause both strobe and data edges to move; therefore, both strobe and data crosstalk must be included in the timing budget. Two types of crosstalk need to be addressed: 1) the aggressor firing at the same time as the victim, and 2) the aggressor not firing at the same time as the victim. The first type of crosstalk is seen between common signals such as DQ pins. The common signal coupling causes the victim's edge to speed up or slow down, resulting in jitter. The second type of crosstalk includes coupling between a DQ pin and an address pin. It is difficult to account for in a timing budget and should be avoided through routing and layout. Never route the DQ pins adjacent to the address and control lines.

Figure 6: Switching Aggressor Conditions When Simulating Crosstalk



When simulating crosstalk, the victim bit should switch under three aggressor conditions: common mode, differential mode, and quiet mode (see Figure 6). The skew between the victim's edge and the aggressor's edge accounts for the crosstalk component in the timing budget. Crosstalk needs to be simulated for both the DQ lines and the DQS line. Figure 7 illustrates a coupled circuit net used to simulate crosstalk. Although three coupled circuits are shown, a worst-case crosstalk scenario typically contains five circuits: a victim and two neighbors on each side.

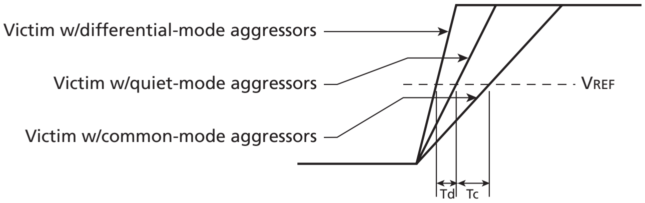
Figure 7: Coupled Circuit



The jitter caused by crosstalk should be measured at VREF rather than at the movement of a single edge using pseudo-random victim/aggressor bit patterns. The quiet mode pattern gives the nominal case with no crosstalk. The differential mode typically causes the victim's signal to speed up. The common mode causes the victim's signal to lay over (see Figure 8). After simulating both the rising and falling edges under all aggressor patterns, enter the largest value of Td or Tc into the timing budget. Entering Td + Tc into the timing budget would be overly pessimistic, since it's physically impossible for a victim bit to have common-mode aggressors one cycle, followed by differential-mode aggressors on the next cycle.

To minimize crosstalk, the bits that switch on the same clock edge should be routed together. This will help to avoid near-end crosstalk. Sensitive lines, such as the strobes, should be isolated or routed next to a signal that rarely switches.

Figure 8: Crosstalk Effects


Victim w/differential-mode aggressors
Victim w/quiet-mode aggressors
Victim w/common-mode aggressors
VREF
Td
Tc

VREF Noise

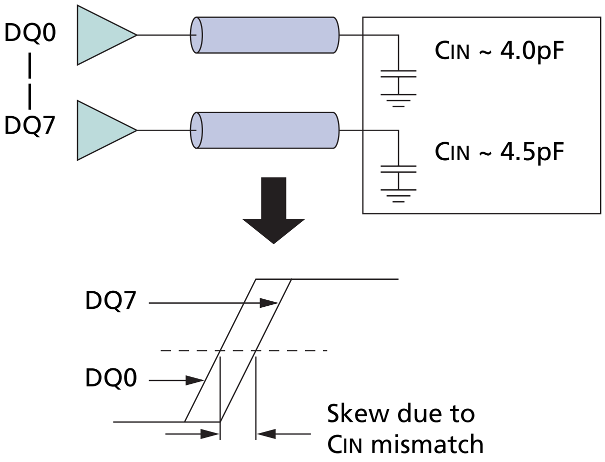
Reference-plane noise and crosstalk are the two major contributors to VREF noise that causes strobe-to-data skew. To calculate the worst-case skew, use the worst-case receiver-edge rate and the VREF noise limits found in the device data sheet. Both strobe and data should be included in the timing budget. For example, with a 0.5V/s edge rate and ±50mV VREF noise, there are 200ps of strobe-to-data skew.

Minimizing VREF noise is an extremely important aspect of DDR SDRAM design. When laying out VREF, the trace should be as wide as possible to reduce the inductance on the line with 15 to 20 mils of spacing from adjacent signals. VREF should also be decoupled to both VDDQ and VSSQ, with balanced decoupling capacitors as close to the chip as possible. Shielding VREF with a VDDQ or VSSQ pin can also help reduce noise on the VREF pin.

CIN and Termination Resistor Mismatch

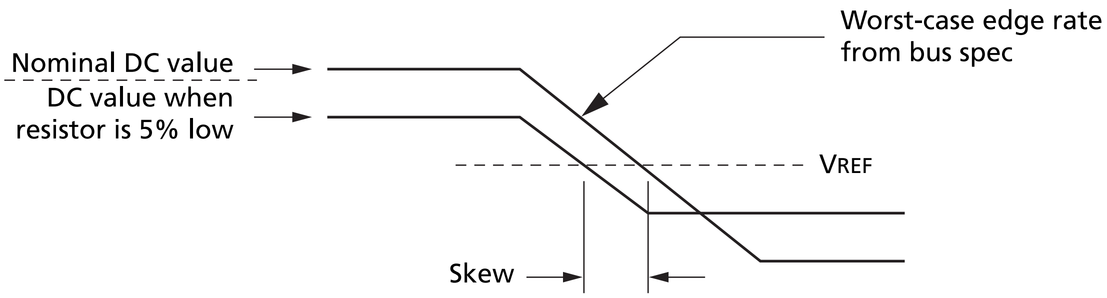
The skew associated with CIN mismatch is derived from simulation and the delta C found in the data sheet specification. The MIN and MAX capacitance are used to determine data-to-data and data-to-DQS skew. Both the driver and the receiver need to be considered for the CIN mismatch. Figure 9 depicts the skew resulting from CIN mismatch and the associated circuit diagram for simulation purposes.

Figure 9: CIN Mismatch



Skew caused by termination mismatch can be hand-calculated or obtained from simulation if more accurate numbers are needed. To hand-calculate the skew from termination mismatch, determine the DC values with the resistance at each tolerance point. Using the edge rate, determine the time required to rise/fall from DC levels to VREF at each tolerance point, and calculate the skew from the difference in times required to rise/fall (see Figure 10).

Figure 10: Skew From CIN Mismatch



Trace Length Mismatch

The trace-length mismatch only affects the byte lane between the DQS pins and the associated DQ pins. Byte lane-to-byte lane mismatch is not as important for putting together the timing budget. The trace tolerances are typically determined by the layout of the design and the manufacture of the PCB. Calculate the skew by multiplying the distance between the shortest and longest trace in the byte lane by the propagation delay of the trace. The propagation delay associated with a microstrip trace is approximately 165ps, and the delay associated with a stripline is approximately 180ps, assuming an FR4 substrate. The propagation delay can vary depending on the deltaic constant of the PCB and the impedance of the trace.

Table 2: Timing Budget

Component	Setup	Hold	Units	Comment
Total skew	1,875	1,875	ps	266 MHz period = 3.75ns per half cycle
Transmitter skew	-790	-790	ps	Vendor data sheet
Receiver skew	-500	-500	ps	Vendor data sheet
ISI	-105	-105	ps	Simulation
Crosstalk	-165	-165	ps	Simulation
VREF noise	-200	-200	ps	Calculation from spec
Termination resistor tolerance	-20	-20	ps	Simulation
Path length mismatch	-30	-30	ps	Calculation from spec
CIN mismatch	-50	-50	ps	Simulation
Remainder	15	15	ps	Margin

The skew associated with the trace length mismatch is the final element needed to complete the timing budget. Table 2 lays out a basic timing budget covering all of the board-skew variables discussed earlier to determine the margin in the design.

Verification

Simulation methodology tends to bond design with worst-case performance numbers, producing a pessimistic timing budget that shows little to no margin. This does not guarantee failure, just risk. It is highly unlikely that all terms will be worst case in a system. To avoid being overly pessimistic, worst-case assumptions can be replaced with statistical distributions during sensitivity analysis. The statistical distributions are developed through lab verification, providing trust in the simulations.

Verifying all simulated conditions is impractical, but there are a few key areas to focus on to gain trust in the simulation. Simulations cannot account for all board effects, so some differences will exist. The key items to verify are DC levels, edge rate, over-shoot, jitter, eye aperture, and the general shape of the wave.

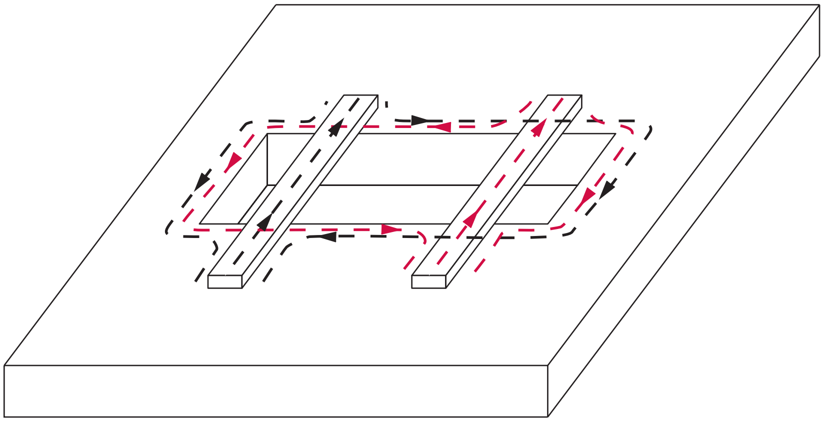
During the verification phase of the design, it is important to use good measurement techniques. Concentrate on the speed of the scope and loop inductance of the probes. Also concentrate on where the measurements are taken. The sample rate and speed of the oscilloscope should be at least two times the speed of the signals being measured. The fast sample rate helps capture single-time events. The speed and sample rate apply to both the scope and the probes. Loop inductance associated with the probe is caused by long ground wires used for differential probes. The ground wires need to be kept as short as possible to achieve the most accurate measurements, even if it makes it more difficult to take the measurement. Measurements should be taken as close to the receiver as possible. Moving away from the receiver can attenuate the signal due to the stub between the probe and the pad. Simulating at the probe point can be useful for verification.

During the verification process, performance testing should be done to determine the robustness of the design. This would include environmental testing and voltage guard band. Both of the MIN and MAX voltage corners should be tested, along with variations in VREF. This validates the design over the vast operating conditions.

Return Path Discontinuities

Return path discontinuities include such things as holes or splits in the reference planes that could divert the return current path. High-speed return current wants to flow directly under the signal line but cannot when the plane has a split or a slot (see Figure 11).

Figure 11: Split Return Path



Return path discontinuities are becoming increasingly more important as bus speeds increase and should not be ignored. Simulating the effects of return path discontinuities is difficult, and in most cases it is better to avoid them if at all possible. Figure 11 illustrates overlapping return currents, which can increase the amount of crosstalk in the system. Again, avoid return path discontinuities if at all possible—even if it requires more time to design and route the board.

Conclusion

Every design requires tradeoffs, and in most cases the major tradeoff is electrical performance versus cost. Through the signal integrity process and simulation, the design can be optimized for both performance and cost.

While going through the signal integrity process, there are a few key points to remember covering the design tradeoffs. The more accurate the models, the longer the simulation takes. A good example of this was discussed earlier on the lump capacitor use. The lump capacitor is not as accurate as the SPICE model, but in most cases it is good enough and saves time in simulation. Edge rates are an area that need special attention. When designing a driver, you want the edge rate to be just fast enough to have some margin. The faster the edge rate, the more noise in the system with less sensitivity to VREF noise. Slower edge rates have an opposite effect. Increasing the loading escalates the ISI and requires a stronger buffer, which adversely affects SSO and crosstalk. Stack-up is a big factor in the tradeoff between performance and cost. Increasing the number of layers typically reduces system noise and simplifies routing but increases cost. The ground plane also tends to be a quieter reference, so it's generally more advantageous to route high-speed signals referencing ground and not power. The detailed models help ensure functional systems from the start, maximizing performance while reducing test and debug time, bringing a better product to market sooner.

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