Project Drawing Numbers
 Raw PCB 100-0321329-A1 Raw PCB
Gerber Files
PCB Design Files
Assembly Drawing
Fab Drawing
Fab Drawing
PCB Film
Bill of Materials
Schematic Design Files
Functional Specification
PCB Layout Guidelines
Assembly Rework 110-0321329-A1 120-0321329-A1 130-0321329-A1 130-0321329-A1 140-0321329-A1 150-0321329-A1 160-0321329-A1 170-0321329-A1 180-0321329-A1 210-0321329-A1 220-0321329-A1 320-0321329-A1 Altera FMC Note: The Parallel NOR flashes are LPC+ updated from JTAG REFOLK XZ CLKIN x2 MAX10 x32 NOR Flash 10M08SAU169 FPP x16 PFL JTAG Chain x40@933MHz MAX10 Micro-USB EMIF 10M08SAU169 On-Board USB Interface 2.0 USB Blaster™ II USB3.1 TX/RX-A/B Super Speed XCVR x1 Cyclone® 10 GX MUX/DRV USB3.1 Type-C DP/DM USB2.0 ULPI PHY GigE PHY 10CX220YF780E5G SGMII RJ45 88E1111 QSPI TX/RX SFP+ XCVR x1 TX/RX SFP+ XCVR x1 LVCMOS XCVR x4 PCI>> **Os cillators** LVDS 50M, 100M, **EXPRESS** x4 XCVRs programmable

NOTES:

REV DATE	PAGE	DESCRIPTION
0.1		initial schematic
0.2		Released schematic, R406=22K, R343=1.2K
0.3		Released schematic, BoM Change: Install Y2(Si570) and U7(Si53307)

PAGE	DESCRIPTION	PAGE	DESCRIPTION
1	01 - Title, Note, Block Diagram	24	24 - INTERFACE - USB3.1
2	02 - Clock Diagram	25	25 - INTERFACE - USB2.0
3	03 - Power Tree Diagram	26	26 - INTERFACE - GIGE - 1
4	04 - I2C JTAG Chain Diagram	27	27 - INTERFACE - GIGE - 2
5	05 - C10GX BANK CSS - Config	28	28 - SYS MAX10 - CTRL
6	06 - C10GX BANK1C/1D - XCVR	29	29 - SYS MAX10 - UBII
7	07 - C10GX BANK2K - EMIF	30	30 - CFG MAX10 - FPP
8	08 - C10GX BANK2J - EMIF	31	31 - CFG MAX10 - PFL
9	09 - C10GX BANK3A - FMC LVDS	32	32 - CFG PFL FLASH
10	10 - C10GX BANK3B - FMC LVDS	33	33 - LED & PB & SW
11	11 - C10GX BANK2A - FPP/GPIO	34	34 - POWER - INPUT
12	12 - C10GX BANK2L - GPIO	35	35 - POWER - 12V to 0.9V
13	13 - C10GX POWER	36	36 - POWER - 12V to 3.3V
14	14 - C10GX PWR Filter	37	37 - POWER - 12V to 5V
15	15 - C10GX GND	38	38 - POWER - 3.3V to 0.95V
16	16 - CLOCK - SI570/Si5332	39	39 - POWER - 3.3V to 1.5V
17	17 - CLOCK - SI5340	40	40 - POWER - 3.3V to 1.8V
18	18 - EMIF-DDR3-1	41	41 - POWER - 3.3V to VADJ
19	19 - EMIF-DDR3-2	42	42 - POWER - CURRENT SENSE
20	20 - INTERFACE - PCIe	43	43 - POWER - Fast Discharge
21	21 - INTERFACE - SFP+		
22	22 - INTERFACE - FMC - 1		
23	23 - INTERFACE - FMC - 2		



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Size | Decument Number

 Size
 Document Number
 Rev A1

 B
 6XX-44528R
 A1

 Date:
 Sunday, November 19, 2017
 Sheet
 1
 of
 43

3

DDR3

256Mx40

Buttons

Switches

LEDs

EPCQ-L For Config

256Mbit

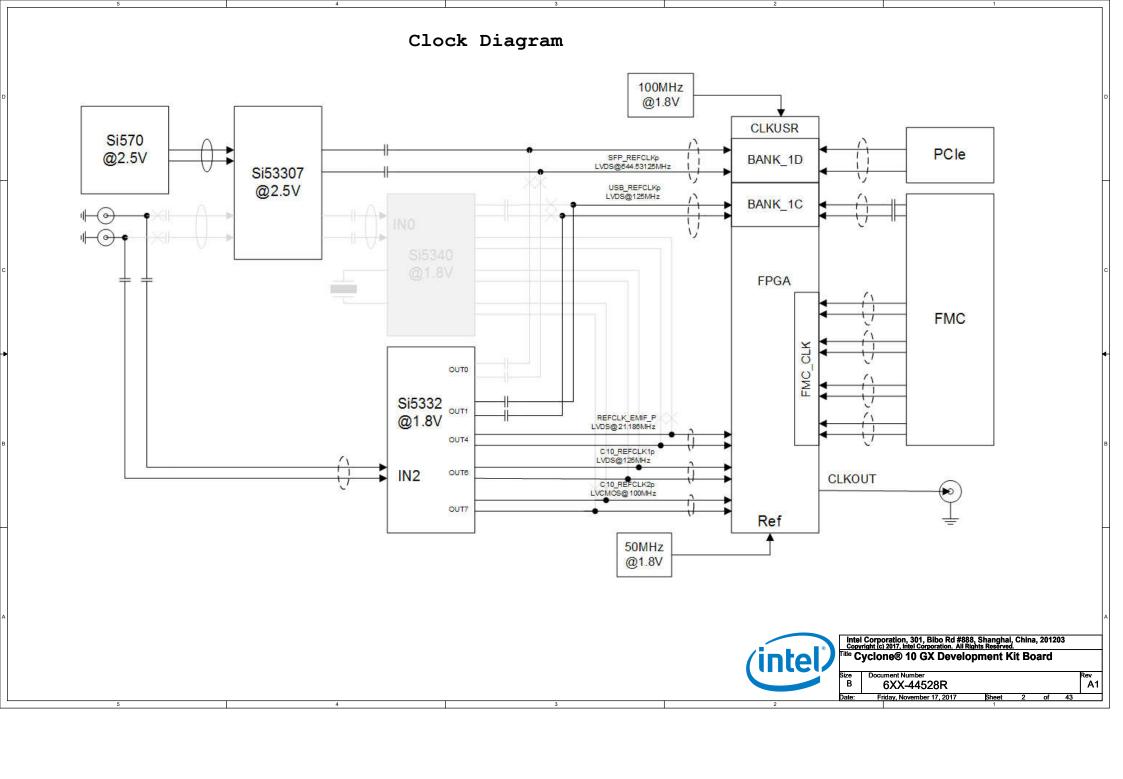
QSPI Flash For NIOS

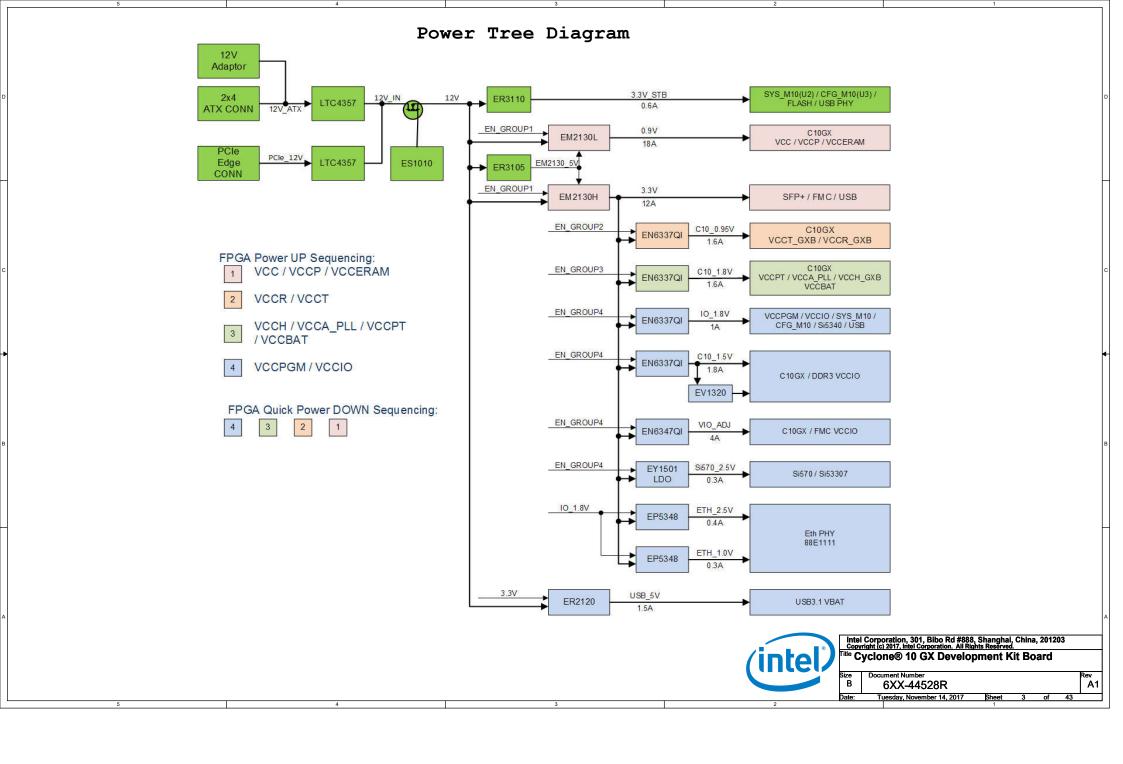
SMA CLK

OUT

SMA CLK

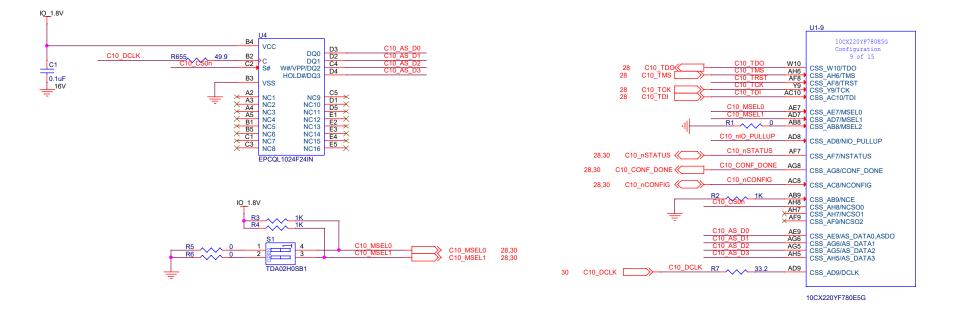
IN





I2C / JTAG Chain Diagram TMP512A EM2130 EM2130 LTC2497 3.3V 0.9V I/V/T-Sense I-Sense (110_0000) (110_0110) (001_0100) (101_1100) PMBUS @3.3V I2C SYS M₁₀ Dongle HDR4x1 (101_0000) CFG M10 HDR2x5 I2C @3.3V For C10GX @3.3V Si5340 Si5332 Si570 C10 JTAG (110_1010) (111_0100) (110_0110) FX2 BUS@3.3V @1.8V C10GX I2C @2.5V 12C@1.8V Level **FPGA USB CFG USB PHY** Shifter CY7C68013 @1.8V PD[3:0](JTAG) SYS M₁₀ @3.3V SFP+0 10 M10 JTAG (101_0000) Expander CFG M10 @3.3V $(101 \ 0001)$ (010_0000) HDR2x5 For SYS M10 Level I2C @3.3V I2C @1.8V Shifter **FMC JTAG** FMC @3.3V SFP+1 10 (101_0000) Expander (101_0001) (010_0000) C10GX Level I2C @3.3V 12C **FPGA** Shifter **USB 3.1** Level @3.3V 12C Switch @1.8V Shifter (110_0111) Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. Title Cyclone® 10 GX Development Kit Board **FMC** @3.3V 'intel' Level 12C DT Card @1.8V Shifter (User Def) Size B 6XX-44528R A1 Friday, November 17, 2017 Sheet

C10GX BANK CSS - Config



0.9V R519 1K,DNI	C10_nIO_PULLUP	IQ
R16 10K R18 10K R20 1K	C10_TDO C10_TMS C10_TRST	
R21 10K	C10_TDI C10_TCK	

IQ	1.8V		
	R10	10K	C10_nSTATUS
	R11	10K	C10_CONF_DONE
	R12	10K	C10_nCONFIG
	R13	10K	C10_CS0n
	R14	10K	C10_AS_D0
	R15	10K	C10_AS_D1
	R17	10K	C10_AS_D2
	R19	10K	C10_AS_D3

Configuration Scheme	V _{CCPGM} (V)	Power-On Reset (POR) Delay	Valid MSEL[20]
JTAG-based configuration	=	-	Use any valid MSEL pin settings below
AS (x1 and x4)	1.8	Fast	010
		Standard	011
PS and	1.2/1.5/1.8	Fast	000
FPP (x8, x16, and x32)		Standard	001

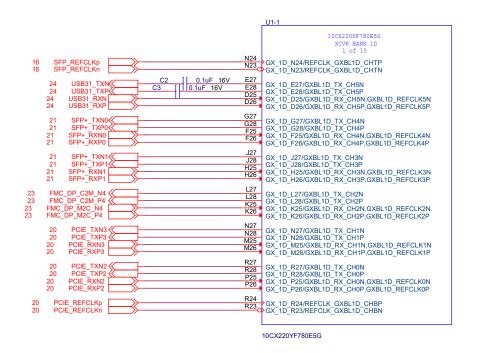
Note: MSEL2 is fixed '0', MSEL1 and MSEL0 are '0' when corresponding switch is ON

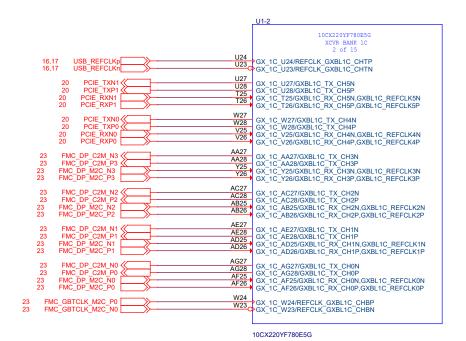


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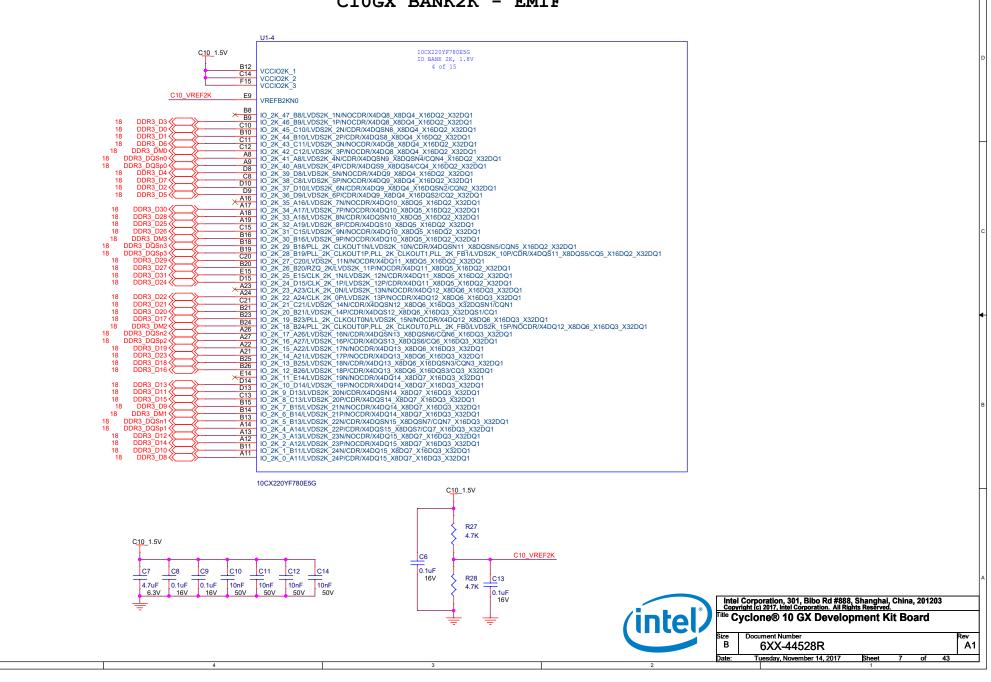
C10GX BANK1C/1D - XCVR



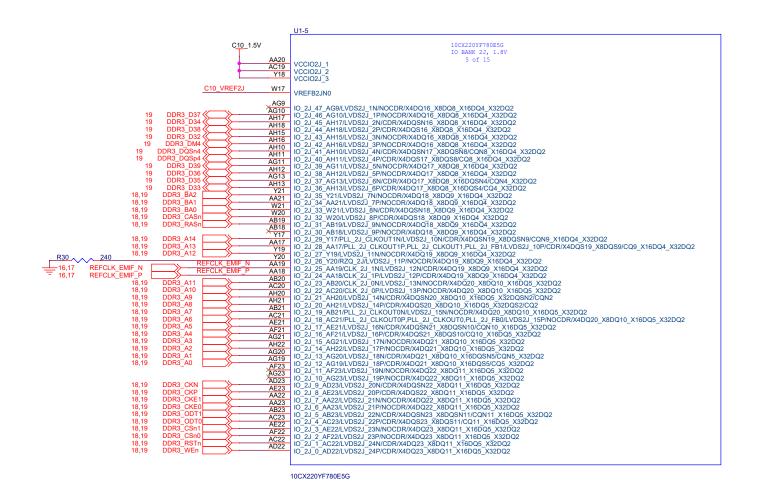


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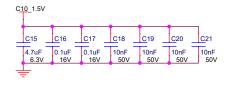
C10GX BANK2K - EMIF

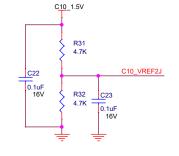


C10GX BANK2J - EMIF











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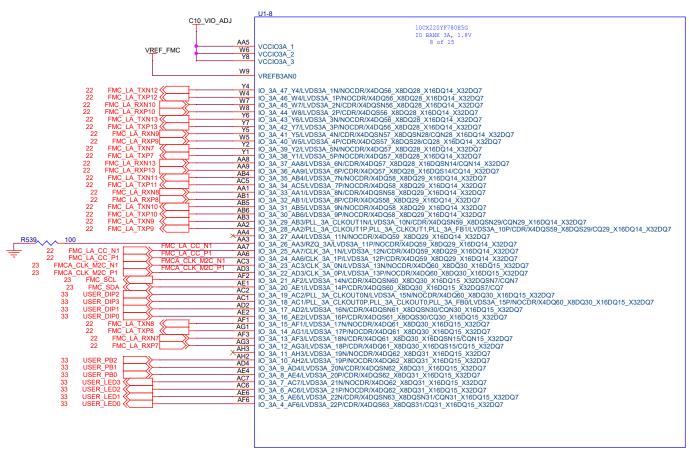
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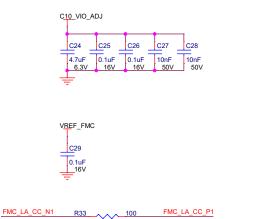
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A1

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C10GX BANK3A - FMC LVDS





FMCA_CLK_M2C_N1 R34 100 FMCA_CLK_M2C_P1

10CX220YF780E5G



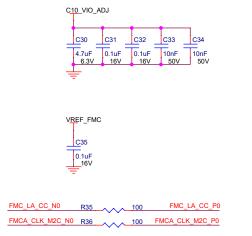
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6XX-44528R Tuesday, November 14, 2017 Sheet of

A1

C10GX BANK3B - FMC LVDS



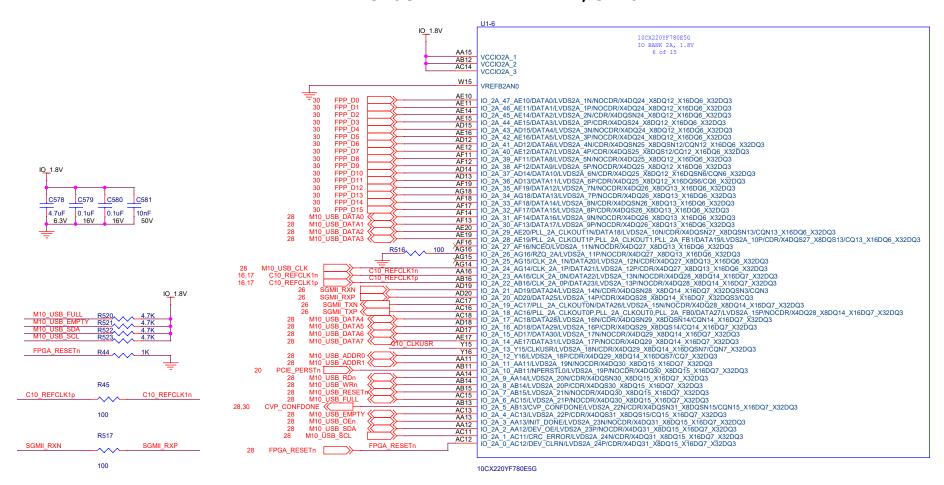


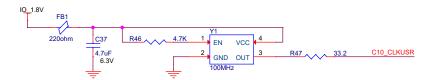


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В A1 6XX-44528R Tuesday, November 14, 2017 Sheet 10 of

C10GX BANK2A - FPP/GPIO





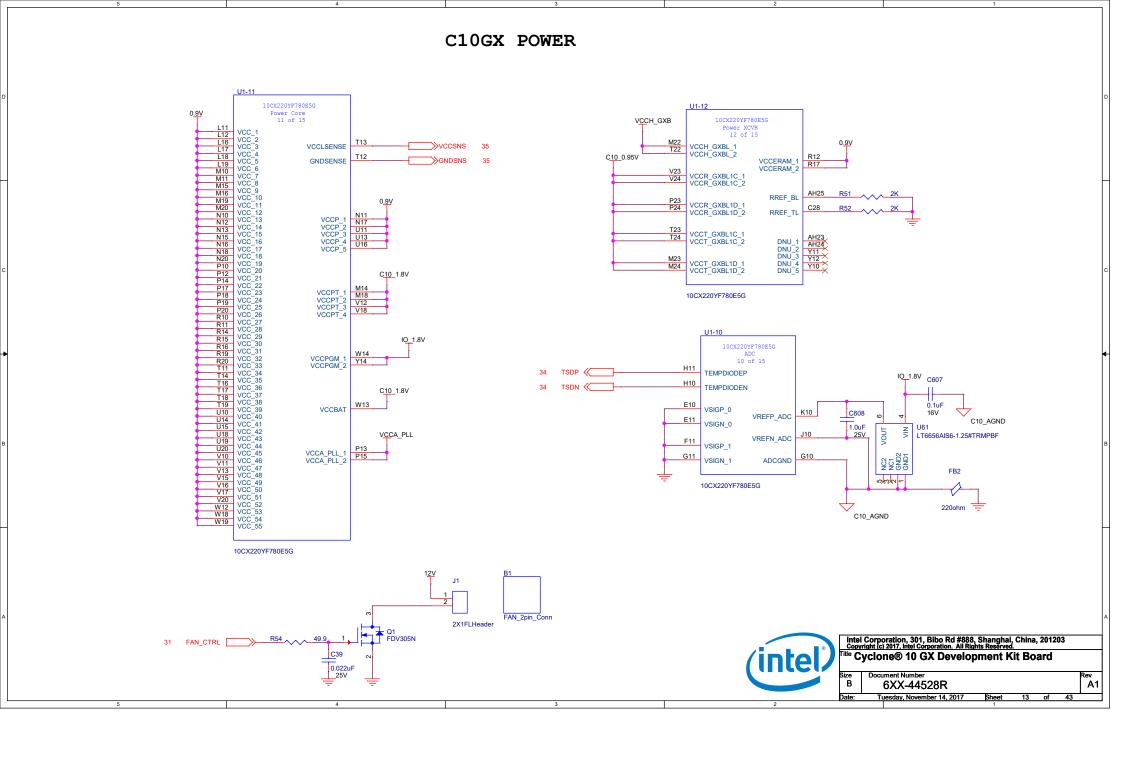


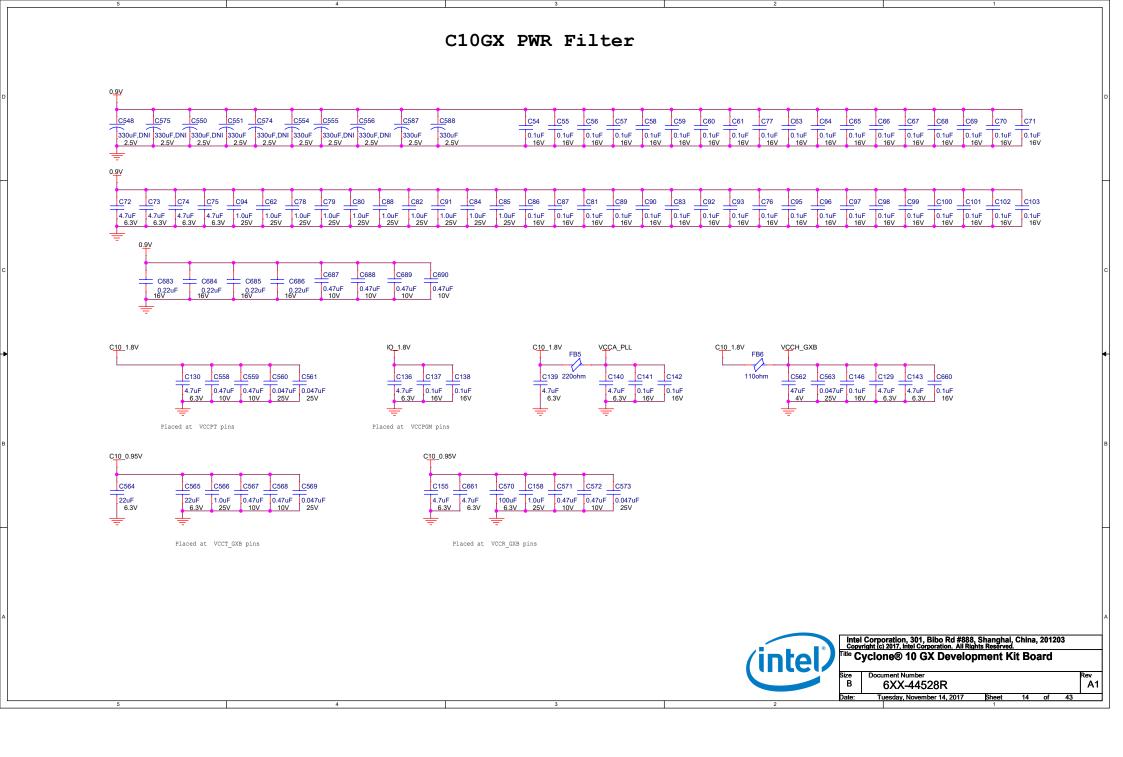
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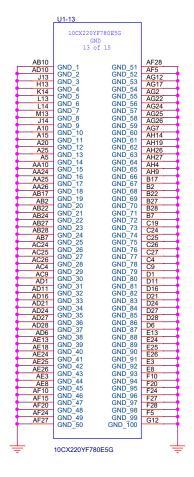
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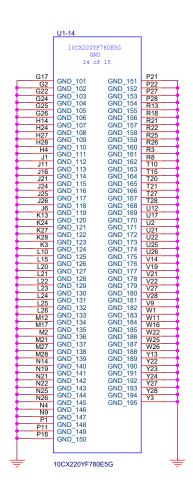
C10GX BANK2L - GPIO IO 1.8V 10CX220YF780E5G IO BANK 2L, 3V 3 of 15 VCCIO2L_ VCCIO2L_2 VCCIO2L 3 K16 VREFB2LN0 IO_1.8V U58 25 25 25 25 25 25 25 25 USB NXT VCC C10_QSPI_D0 DQ0/SI ВЗ C582 DQ1/SO VSS USB D6 C4 D4 USB_D7 DQ2/W# USB DO DNU6 DQ3 16V USB_D1 10 2L 41 F18/DIFFIO2L 4N/NOCDR/X4DQSN1 X8DQSN0/CQN0 X16DQ0 X32DQ0 DNU7 C10_QSPI_CLK B2 H18 IO_2L_40_F17/DIFFIO2L_4P/NOCDR/X4DQS1_X8DQS0/CQ0_X16DQ0_X32DQ0 DNU8 USB_D2 DNU9 D1 × 25 25 USB DIR **DNU10** A4 D5 × DNU11 RESET#/DNU3 25 21 21 21 21 21 VBUS_DET IO_2L_36_G20/DIFFIO2L_6P/NOCDR/X4DQ1_X8DQ0_X16DQS0/CQ0_X32DQ0 X A3 X A5 DNU12 E3 × E4 × DNU1 DNU13 SEP SCI SFP SDA DNI 12 DNI 114 SFP INT 0 DNU4 DNU15 E5 X B1 DNU5 DNU16 SFP_INT_1 USB_SCL IO 2L 32 D23/DIFFIO2L 8P/NOCDR/X4DQS2 X8DQ1 X16DQ0 X32DQ0 24 IO 2L 31 F22/DIFFIO2L 9N/NOCDR/X4DQ2 X8DQ1 X16DQ0 X32DQ0 IS25WP256D-RHLE USB SDA 24 R37 _____ 33.2 C23 IO_2L_26_F21/RZQ_2L/DIFFIO2L_11PNOCDR/X4DQ3_X8DQ1_X16DQ0_X32DQ0 IO_2L_26_G23/CLK_2L_1N/DIFFIO2L_12N/NOCDR/X4DQ3_X8DQ1_X16DQ0_X32DQ0 IO_2L_24_F23/CLK_2L_1P/DIFFIO2L_12PNOCDR/X4DQ3_X8DQ1_X16DQ0_X32DQ0 C10_REFCLK2n IO_1.8V 16,17 IO_2L_23_H23/CLK_2L_0N/DIFFIO2L_13N/NOCDR/X4DQ4_X8DQ2_X16DQ1_X32DQ0 C10 CLK50M C10_QSPI_RESETn R509 USB_PWEN USB_RESETn C10 QSPI CSn R510 10K CLK_OUT R504 33.2 J22 C10_QSPI_D0 21 SFP SCL 1 SFP SDA K19 IO_2L_15_K20/DIFFIO2L_17N/NOCDR/X4DQ5_X8DQ2_X16DQ1_X32DQC USB_SW_INTn_1.8V USB_ID_1.8V | IO_2L_14_K19/DIFFIO2L_17P/NOCDR/X4DQ5_X8DQ2_X16DQ1_X32DQ0 | IO_2L_13_K22/DIFFIO2L_18N/NOCDR/X4DQ5_X8DQ2_X16DQ5N1/CQN1_X32DQ0 PCIE WAKEN D18 IO_2L_12_K23/DIFFIO2L_18P/NOCDR/X4DQ5_X8DQ2_X16DQS1/CQ1_X32DQ0 PCIE_SMBCLE PCIE SMBDAT IO 2L 11 D18/DIFFIO2L 19N/NOCDR/X4DQ6 X8DQ3 X16DQ1 X32DQ0 | D_2L 11 D18/DIFFIO2L 19N/NOCDR/X4DQ6 X8DQ3 X16DQ1 X32DQ0 | D12L 10_D19/DIFFIO2L=9P/NOCDR/X4DQ6 X8DQ3 X16DQ1 X32DQ0 | D2L 9 E17/DIFFIO2L 20N/NOCDR/X4DQSN6 X8DQ3 X16DQ1 X32DQ0 | D2L 8 E16/DIFFIO2L 20P/NOCDR/X4DQSN6 X8DQ3 X16DQ1 X10DQ0 X10DQ0 | D2L 8 E16/DIFFIO2L 20P/NOCDR/X4DQ0 X10DQ0 X10DQ0 X10DQ0 X10DQ0 X10DQ0 X10DQ0 X10DQ0 X10DQ0 ETH_RESETn_C10 ETH_INTn_C10 ETH MDIO C10 4 C10_QSPI_CLK IO 2L 7 F19/DIFFIO2L 21N/NOCDR/X4DQ6 X8DQ3 X16DQ1 X32DQ0 ETH_MDC_C10≪ D17 IO_2L_2_C17/DIFFIO2L_23P/NOCDR/X4DQ7_X8DQ3_X16DQ1_X32DQ0 IO_1.8V 10CX220YF780E5G C584 C585 0.1uF 0.1uF 4.7uF 16V 6.3V 16V CLK OUT LTI-SASF546-P26-X1 R50 C10 REFCLK2p C10_REFCLK2n 100,DNI Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. Fitte Cyclone® 10 GX Development Kit Board В A1 6XX-44528R Tuesday, November 14, 2017 Sheet of

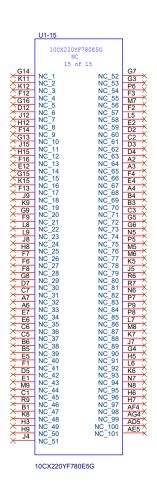




C10GX GND









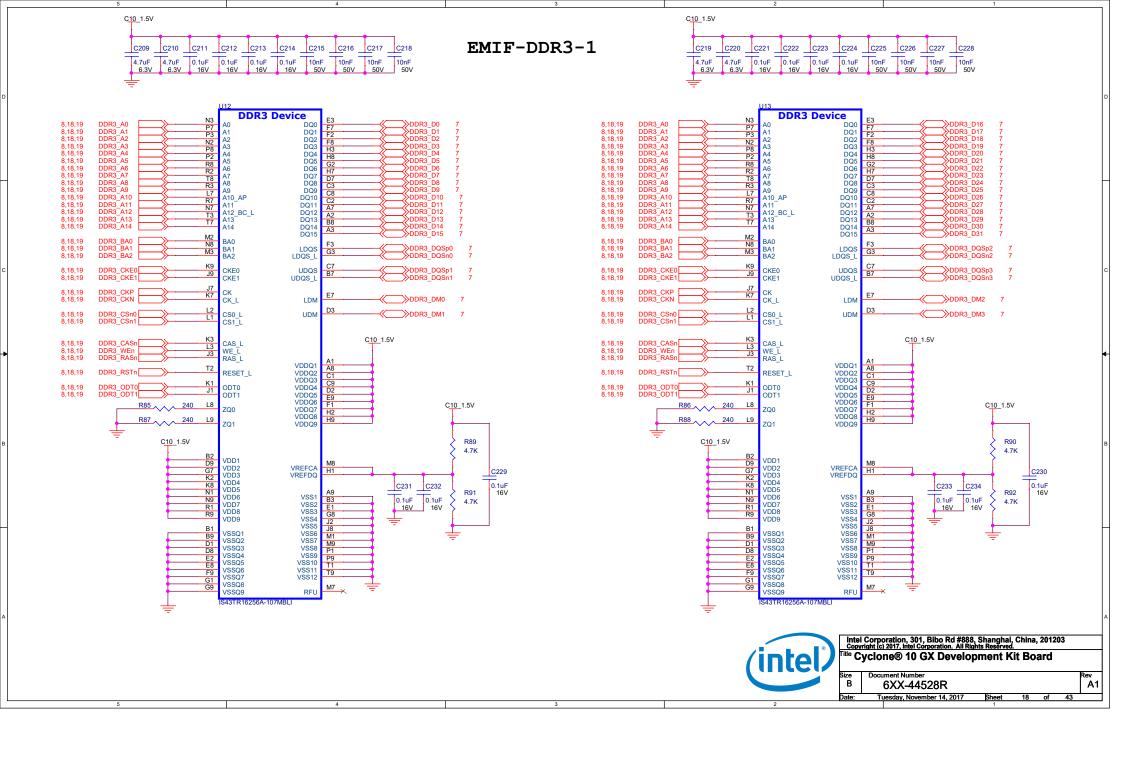
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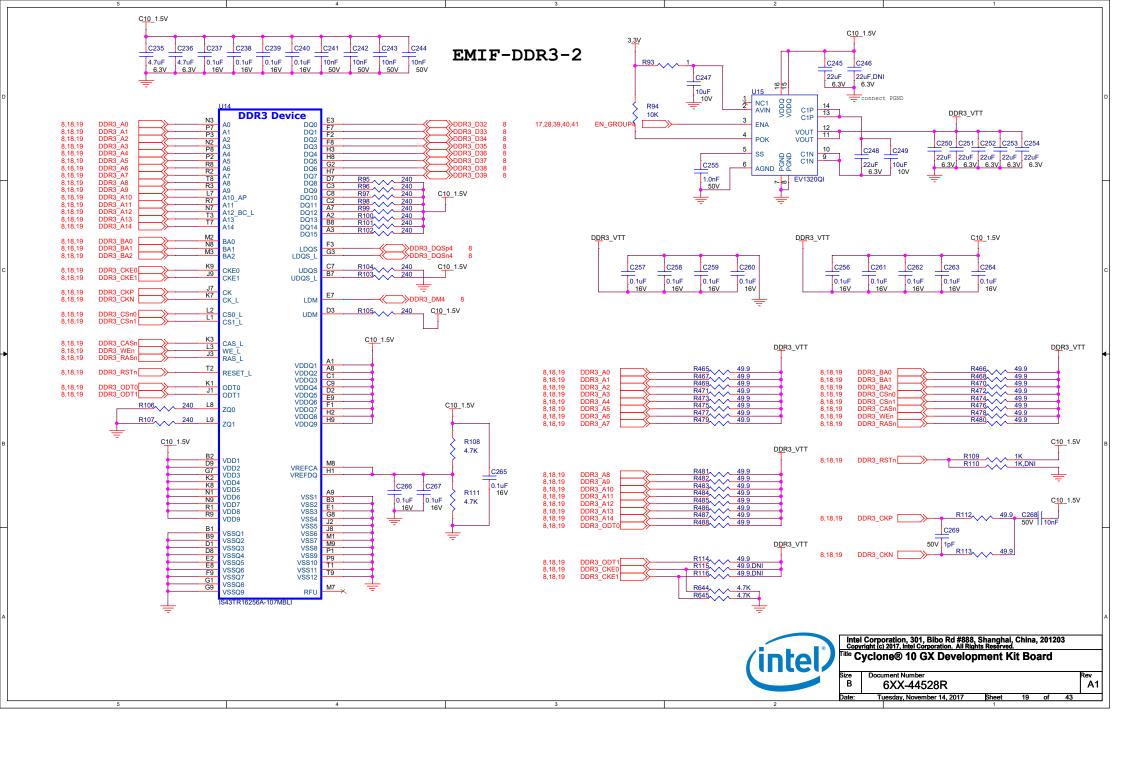
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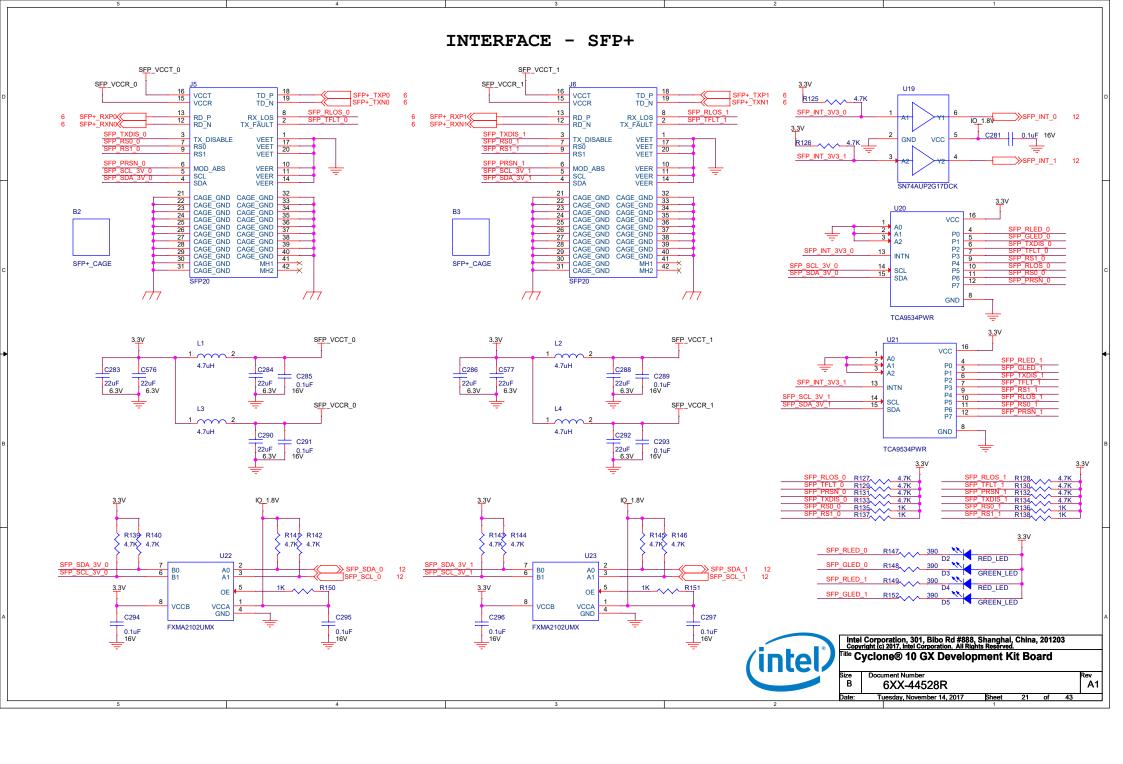
CLOCK - SI570/Si5332 SI570_2.5V FR9 I2C Address = "110 0110" Freq=644.53125MHz PN=570FAA000759DG C163 C164 220ohm 0.1uF 4.7uF 16V 6.3V 4.7uF SI570_2.5V ≱ NC VCC SI570_OE C165 0.1uF R56 OE GND nOUT OUT C166 0.1uF CLK I2C SCL 2.5V CLK I2C SDA 2.5V SDA SCL U7 Si570 C167 0.1uF CLKIN0_P SFP REFCLKn CLKINO N Q0n C168 0.1uF LTI-SASF546-P26-X1 S<u>I57</u>0_2.5V 0.1uF,DNI C170 0.1uF CLKIN1 P CLKIN1_N C171 0.1uF EXT_REF1n R611 C172 FB10 SI570_2.5V CLKBUF SEL IO_1.8V R60 10K CLK_SEL VDD C173 C174 220ohm R612 S<u>I57</u>0_2.5V CLKBUF_SEL 4.7K VDDO 0.1uF LTI-SASF546-P26-X1 1 OuF IO 1.8V 25V FB25 16V GND1 TDA02H0SB1 SFOUT0 GND2 SFOUT1 EPAD 220ohm,DNI Si53307-B-GM FB11 SI570_2.5V EXT REF P C546 0.1uF C175 C176 220ohm IO_1.8V U9 EXT_REF_N 0.1uF C547 0.1uF 1.0uF CLK I2C SCL 2.5V 16V 25V B0 B1 CLK_I2C_SDA IO_1.8V SI570 2.5V OE IO_1.8V VCCA VCCB 1.0uF 25V <u>C</u>182 C183 ___C641 C642 0.1uF FXMA2102UMX IO_1.8V 0.1uF 16V 4.7uF 6.3V 4.7uF ____6.3V I2C Address = "110_1010" PN=Si5332AC08493-GM2 25V 1 VDD_DIG VDDO0 14 OUT0 13 OUT0B SFP REFCLKD C646 0.1uF,DNI VDDA 156.25MHz LVDS VDD_XTAL 0.1uF.DNI VDD01 SCLK 12 SUSB_REFCLKp OUT1 OUT1B 10 19 INPUT1 20 INPUT2 31 INPUT3 32 INPUT4 36 INPUT5 37 INPUT6 INPUT7 C649 0.1uF SUSB_REFCLKn R613 0,DNI R614 0,DNI VDDO2 22 21 × 24 × 23 × IO_1.8V SI5340 INSEL0 OUT2 OUT2B C652 C650 C651 C653 SI5340_INSEL1 SI5340_RSTn SI5340_INTn OUT3 1.0uF 1.0uF 1.0uF 1.0uF OUT3B 25V 25V 25V 25V VDDO3 OUT4 EXT_REF_P REFCLK_EMIF_P REFCLK_EMIF_N 8,17 8,17 21.186MHz LVDS CLKIN 2 OUT4 26 OUT4B 30 R617_____49.9 CLKIN_2B C654[0.1uF OUT5 OUT5B 29 × CLKIN 3 CLKIN_3B EXT_REF_N VDDO4 11,17 125MHz LVDS Y8 OUT6 OUT6B XIN/CLK1 25.00MHz XOUT Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. VDD05 C10_REFCLK2p C10_REFCLK2n 12,17 12,17 100MHz, LVCMOS OUT7 OUT7B Title Cyclone® 10 GX Development Kit Board GNDPAD Si5332A-C-GM2R Size B 6XX-44528R A1 Friday, November 17, 2017 Sheet 16 of

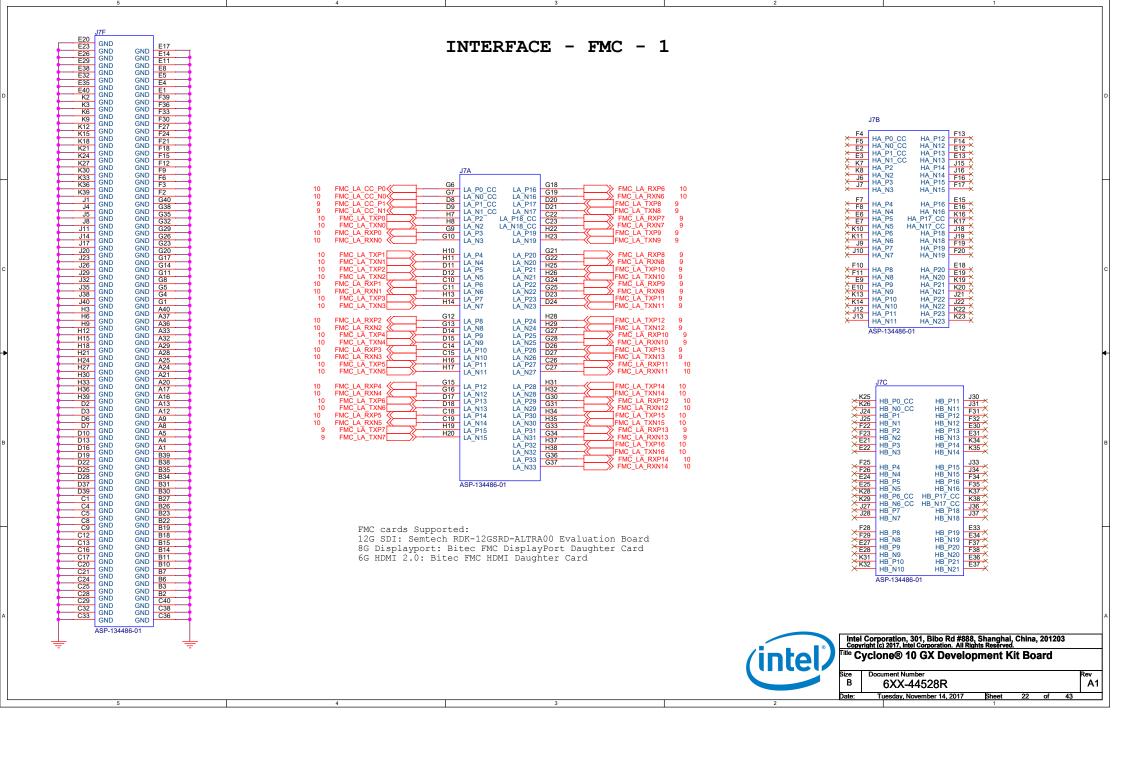
CLOCK - SI5340 IO_1.8V FB12 SI570_2.5V FB24 IO_1.8V C185 220ohm C187 ___C188 C186 SI5340 INTn 220ohm 4.7uh 6.3V 4.7uF 4.7uF 1.0uF 1.0uF 6.3V 25V 25V 3.3V Use Default VCCTO=1.8V IO_1.8V I2C Address = "111_0100" SI5340_RSTn FB13 SI5340_I2CSEL U10 3<u>.3V</u> C189 220ohm,DNI CLK_I2C_SDA C609 C610 C611 C612 C195 C196 FB14 1.0uF 25V VDD VDDO0 VDDO1 32 26 39 40 1.0uF 25V 1.0uF 25V CLK_I2C_SCL 23 29 1.0uF 25V 1.0uF 25V 4.7uF VDD 6.3V VDDS VDD01 C190 220ohm C197 C198 SI5340_A0 R72 1K 8 VDD VDDA 4.7uF 1.0uF 1.0uF 6.3V SI5340 A1 25V 25V 9 VDDA 0,DNI 0,DNI >REFCLK_EMIF_P >REFCLK_EMIF_N 8,16 233.25MHz LVDS OUT0 OUT0B 13 SDA_SDIO 14 SCLK 15 A1_SDO A0_CSB R541 SI5340_OEN CLK_I2C_SDA CLK_I2C_SCL 16,30 16.30 6,16 6,16 OUT1 125MHz LVDS C200 0.1uF,DNI 12 I2C SEL OEB IO_1.8V 37 IN_SEL0 17 RSTB R77 \\ 10K C10_REFCLK1p R627 0,DNI R78 10K SI5340_RSTn C10_REFCLK1n 11,16 EXT REF1p 43 44 10 1N0 1N0 1N0 1N0 1N0 C613 0.1uF R543 49.9 R628 0,DNI R629 0,DNI 10 IN1 N 10 IN1 N 11 IN2 N 11 IN2 N C10_REFCLK2p 12,16 12,16 OUT3 SI5340_INSEL1 EXT REF1n OUT3B TDA02H0SB1 41 FBIN FBIN N INTRB 27 28 X ≫SI5340_INTn 6 XA 7 XB LOS_XAXB _____Y3 R79 390 3.3V X2 RED LED SI570 2.5V 48.00MHz 45 ePAD RSVD U8 Si5340A-A-GM,DNI 9 10 VIN1 POK C178 C177 VIN2 4.7uF 4.7uF 6.3V VOUT1 IO_1.8V C179 S R64 C180 C181 VOUT2 FB16 2.61K 82pF 4.7uF 4.7uF 50V 6.3V 6.3V 220ohm 19,28,39,40,41 EN GROUP4 EN VFB R83 4.7K EN VCC C207 R66 R84 33.2 4.7uF GND OUT >C10 CLK50M 4./uF 6.3V 50.0MHz EPAD 649 SS GND 10nF 50V EY1501DI-ADJ 3.3V_STB U11 FB15 VDD R81 33.2 R82 33.2 >CFG_M10_CLK >SYS_M10_CLK R80 VV 220ohm 4.7K OE CLKr C205 C206 Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. 4.7uF 0.1uF GND NC 6.3V 16V Title Cyclone® 10 GX Development Kit Board ÷ 510MCA50M0000AAGR Size B 6XX-44528R A1 Tuesday, November 14, 2017 Sheet





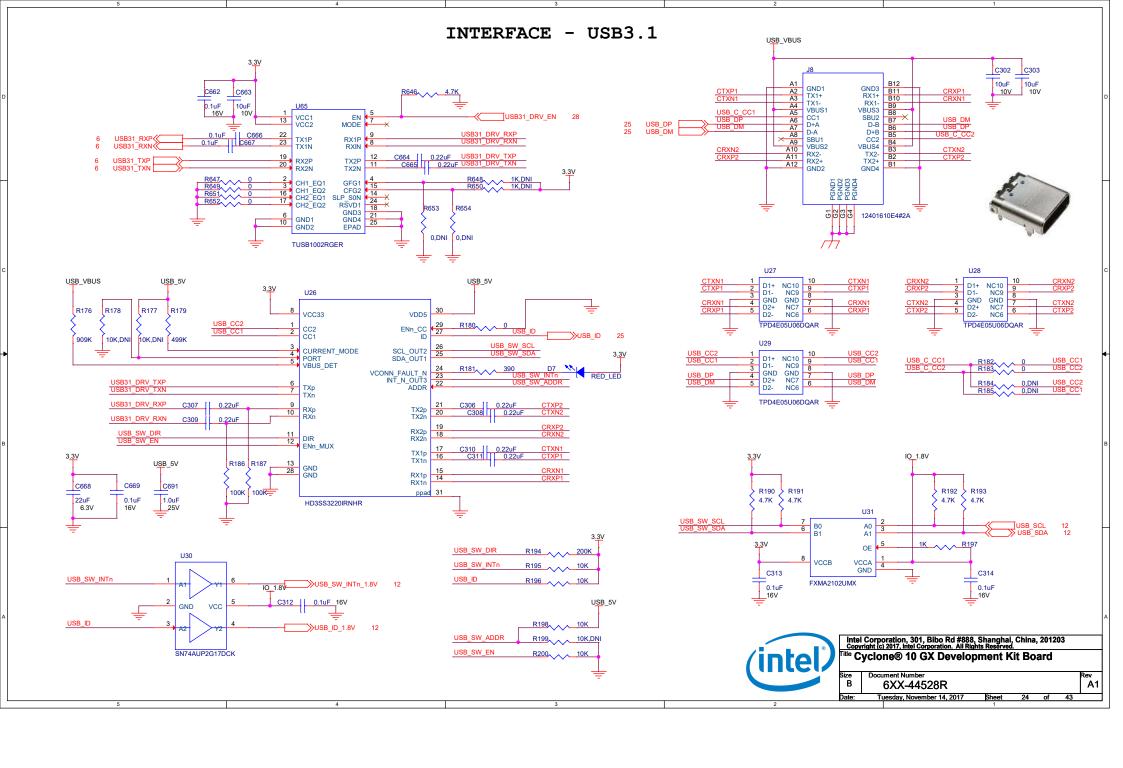
INTERFACE - PCIe PCIE_PRSNT2n_x1 PRSNTn PCIE_12V PCIE_12V PRSNT1 N A1 A2 +12V A3 +12V A3 +12V A3 H A2 H A2 H A3 H A4 H A6 H A6 H A6 H A6 H A7 PRSNTn B1 +12V B3 +12V +12V B4 GND B6 GND SMCLK PCIE_3.3V PCIE_SMBCLK_HOST PCIE_3.3V U17 R117 20K B7 SMDAT GND B8 GND +3_3V B10 JTAG TRSTN +3_3VAUX >PCIE_PERSTn 11 PCIE_WAKEn_HOST R118 0,DNI B11 +3_3v/... WAKE_N R657 33.2 >>PCIE PERSTn HOST C270 0.1uF 16V GND B12 RSVD1 B13 GND B14 PETOP B16 PETON B17 B18 PRSNTO PCIE_PERSTn_HOST1 R658 33.2 GND REFCLK+ REFCLK-GND A16 PCIE_WAKEn_HOST >PCIE_WAKEn 12 PCIE_RXN0 < PER0P PCIE PRSNT2n x1 PER0N GND B18 PRSNT2_N_X1 GND A18 B19 PET1P B20 PET1N B21 GND B23 GND B23 GND B24 PET2P B25 GND B26 GND B27 GND B27 GND B27 GND B27 GND SN74AUP2G17DCK RSVD2 A20 × GND A21 PER1P A22 PCIE_RXP1 & PCIE_RXN1 & C273 0.1uF 16V C274 0.1uF 16V PER1P PER1N A23 GND A25 PER2P A26 PER2N A27 GND A28 GND A20 PCIE RXP2 PCIE_RXN2 C275 0.1uF 16V 3.3V IO_1.8V PCIE_TXP2 PCIE_TXN2 B26 GND B27 PET3P B28 PET3N GND S30 RSVD3 B31 RSVD3 PCIE_RXP3 (PCIE_RXN3 (GND A29 PER3P A30 PER3N A31 C277 0.1uF 16V C278 0.1uF 16V R120 R121 R122 > R123 PCIE_PRSNT2n_x4 - 20K → 20K 4.7K > 4.7K GND RSVD4 A31 B32 PNG. PRSNT2_N_X4 U18 PCIE_SMBCLK_HOST PCIE_SMBDAT_HOST PCIE_Bracket_X4 PCIE_SMBCLK A1 > PCIE_SMBDAT 3.3V OE PCIe Bracket Holes Board Holes VCCB VCCA SCREW1 SCREW2 GND C279 C280 FXMA2102UMX 0.1uF 0.1uF 1 MT2 MT4 1 € _16V SCREW SCREW BKT1 PCB1 PCle Bracket C615 1000pF C616 1000pF Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. 1000V 1000V Title Cyclone® 10 GX Development Kit Board Size B 6XX-44528R A1 Friday, November 17, 2017 Sheet 20 of

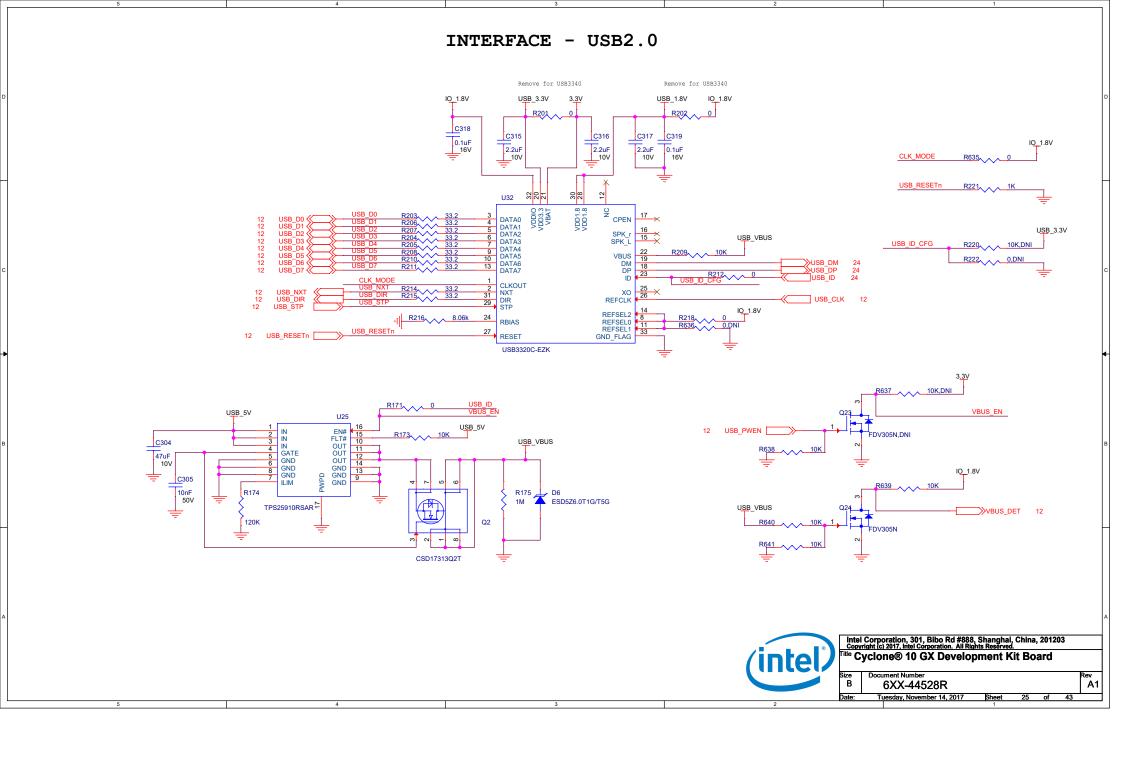




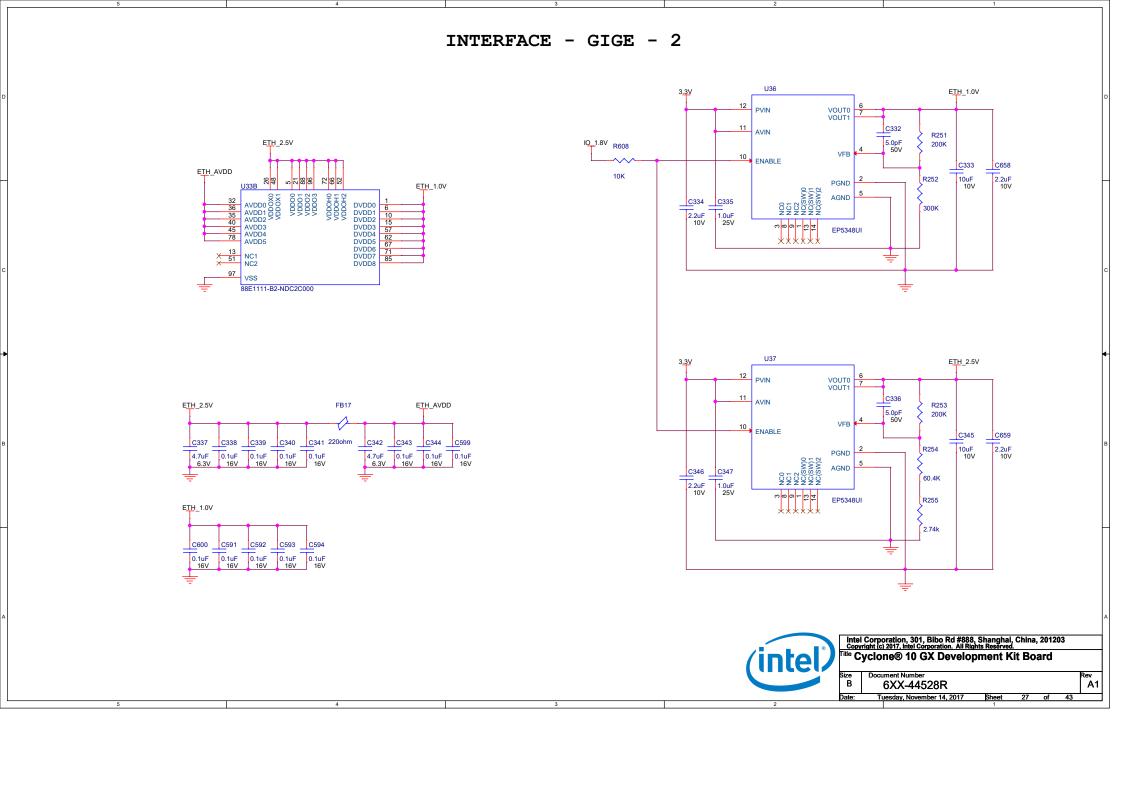
INTERFACE - FMC - 2 3.3V J7E VIO ADJ VREF FMC J7D D32 F39 R153 FMC_DP_C2M_P0 FMC_DP_C2M_N0 FMC_DP_C2M_P1 >FMC_DP_M2C_P0 FMC_DP_M2C_N0 >FMC_DP_M2C_P1 >FMC_DP_M2C_N1 3P3VAUX VADJ DP0 M2C P VADJ A22 DP0_C2M_N A23 DP1_C2M_P A26 DP1_C2M_P DP2_C2M_P DP0_C2M_N DP0_M2C_N D40 C39 D36 R154 DP1_M2C_P DP1_M2C_N DP2_M2C_P 3P3V VAD.I C298 C299 3P3V 3P3V VAD.J A6 FMC_DP_M2C_P2 FMC_DP_M2C_N2 FMC_DP_M2C_N2 FMC_DP_M2C_N3 FMC_DP_M2C_N3 FMC_DP_M2C_P4 D38 VREF FMC 0.1uF 0.1uF A27 DP2 C2M N A30 DP3 C2M P DP3 C2M P DP3 C2M N DP4 C2M P DP4 C2M N DP2_M2C_N A10 FMC_DP_C2M_N2 FMC_DP_C2M_P3 3P3V VIO B M2C 12V J39 1K 16V 16V VIO_B_M2C DP3_M2C_N A10 DP3_M2C_N A11 FMC_DP_C2M_N3 FMC_DP_C2M_P4 C35 DP3_M2C_P A14 DP4_M2C_P A15 H1 × R155 0,DNI 12P0V VREF B M2C C37 FMC_DP_C2M_N4 FMC_DP_M2C_N4 12P0V VREF_A_M2C DP4_M2C_N A38 DP5_C2M_P B36 DP5_C2M_N DP5 M2C P DP5_M2C_N A19 B16 FMC_PG_C2M FMC_PG_M2C D1 B36 DP5 C2M N B37 DP6 C2M P B32 DP7 C2M P B33 DP7 C2M P B28 DP7 C2M N B29 DP8 C2M N B24 DP8 C2M N B24 DP9 C2M N B25 DP9 C2M N DP5_MZC_N DP6_M2C_P DP6_M2C_N DP7_M2C_P DP7_M2C_N B13 × DP7_M2C_N B8 × PG C2M PG M2C 28 FMC_PRSNT 《 PRSNT_M2C_L D34 FMC_TRST DP7_M2C_P DP7_M2C_N B8 TRST FMC_SDA_3.3V 28 28 DP8_M2C_P B9 FMC_TMS FMC_TDO FMC_TDI TMS FMC SCL 3.3V C30 DP8_M2C_r DP8_M2C_N B4 × DP9_M2C_P B5 × SCL TDO TDI CLK2_BIDIR_P CLK2_BIDIR_N DP9_C2M_N DP9_M2C_N × K5 TCK J2 CLK2_BIDIR_N CLK3_BIDIR_PCLK0_M2C_P C595 0.1uF 16V FMC_GBTCLK_M2C_P0 FMC_GBTCLK_M2C_N0 FMCA_CLK_M2C_P0 FMCA_CLK_M2C_N0 10 10 GBTCLK0_M2C_P GBTCLK0_M2C_N GBTCLK1_M2C_P GBTCLK1_M2C_N CLK3_BIDIR_NCLK0_M2C_N CLK1_M2C_P FMCA CLK M2C P1 × B1 G3 CLK_DIR CLK1_M2C_N XCVR input reference clock requires AC C34 B40 × ASP-134486-01 coupled, so capacitors are used here in case the FMC card doesn't have the AC coupling GAN RES0 D35 GA1 ASP-134486-01 VIO_ADJ VIO_ADJ 3.3V R524 R525 R158 R159 R160 R161 > 4.7K > 4.7K > 4.7K > 4.7K > 4.7K > 4.7K U59 U24 FMC_PRSNT FMC_SCL_3.3V FMC_SDA_3.3V A0 A1 >FMC_PRSN_1V8 A0 FMC_SCL 10K FMC_RSV A1 <u>3.3</u>V 3.3V 1K R165 OE OE FMC_TMS VCCA GND VCCB VCCB VCCA GND C597 C300 C301 C598 FXMA2102UMX FXMA2102UMX FMC_RSV 0.1uF 0.1uF 0.1uF U.1∟ 16V J.1u 16V 0.1uF 16V FMC_TCK R167____1K

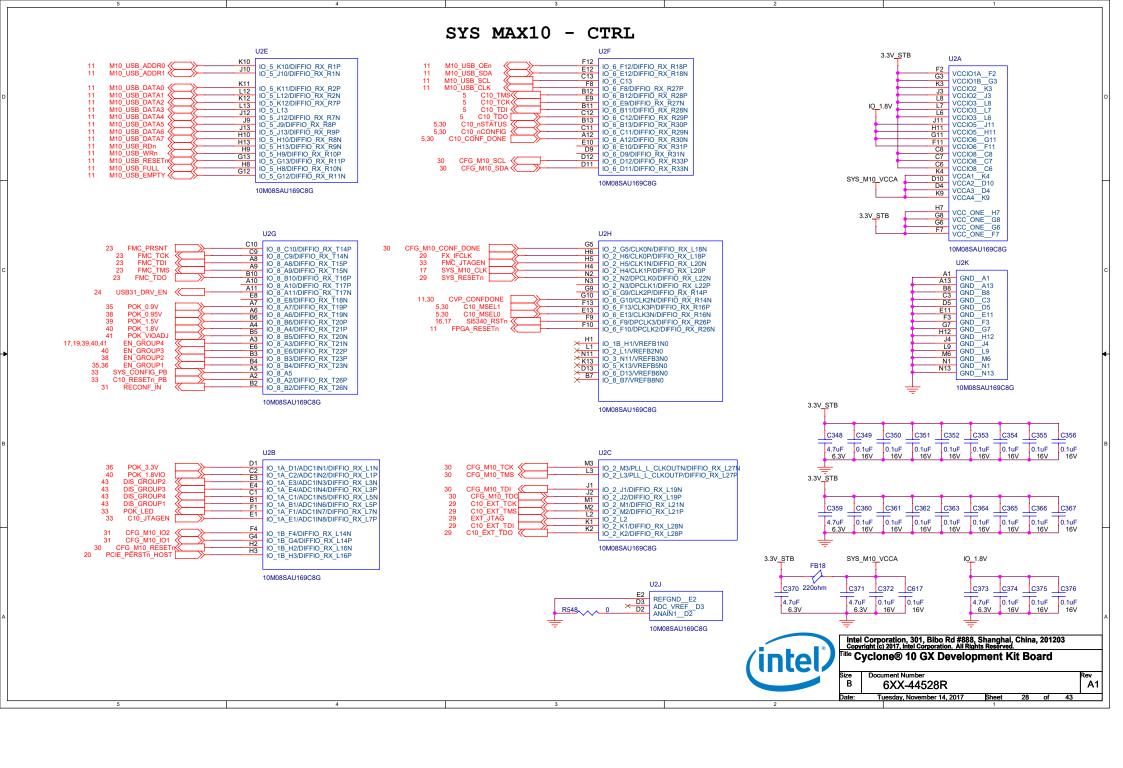


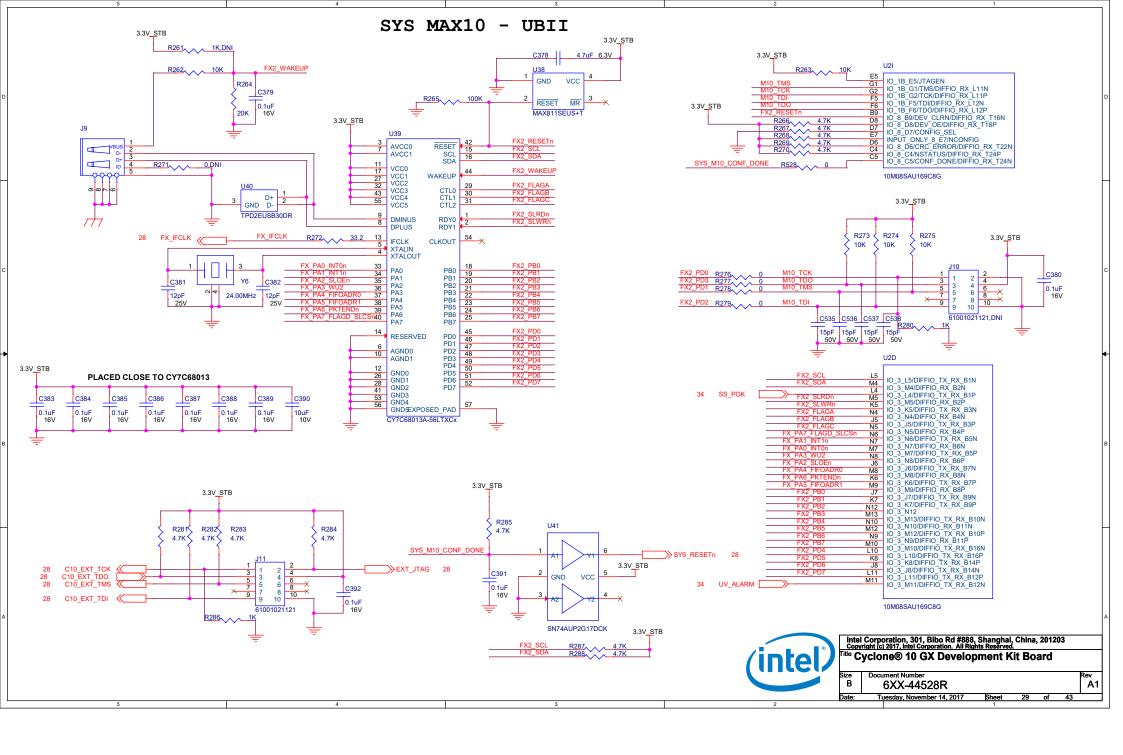


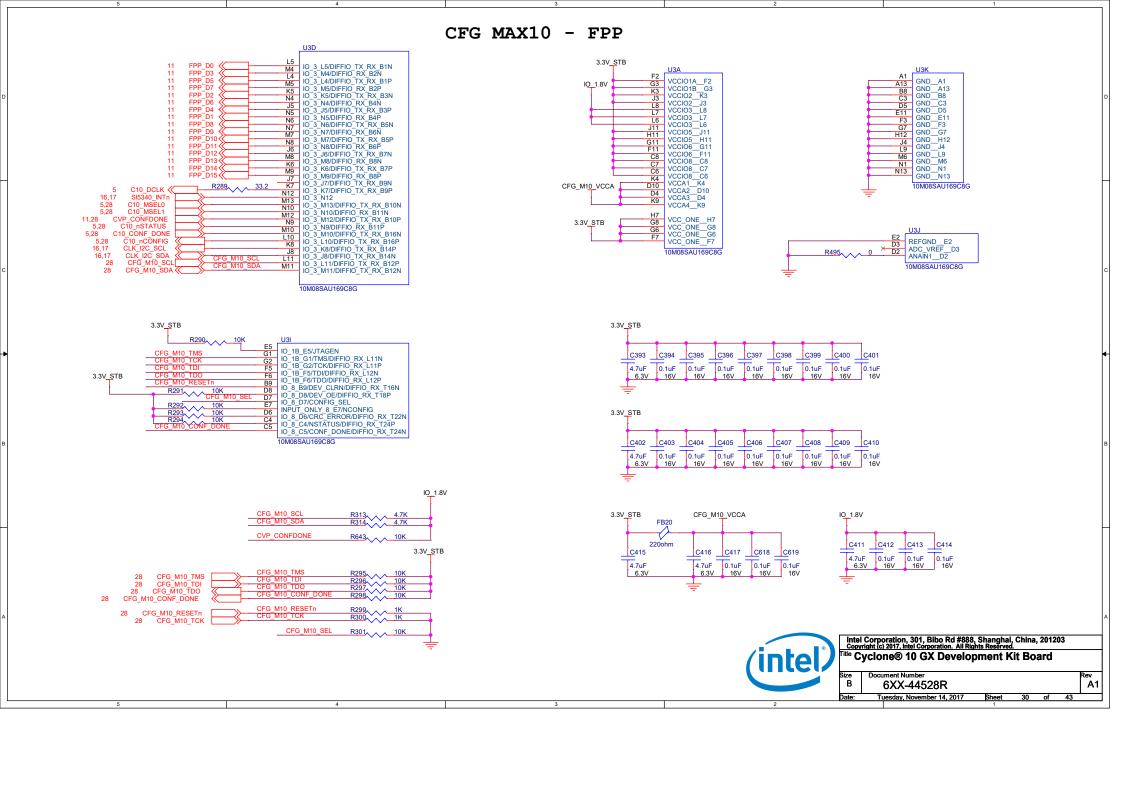


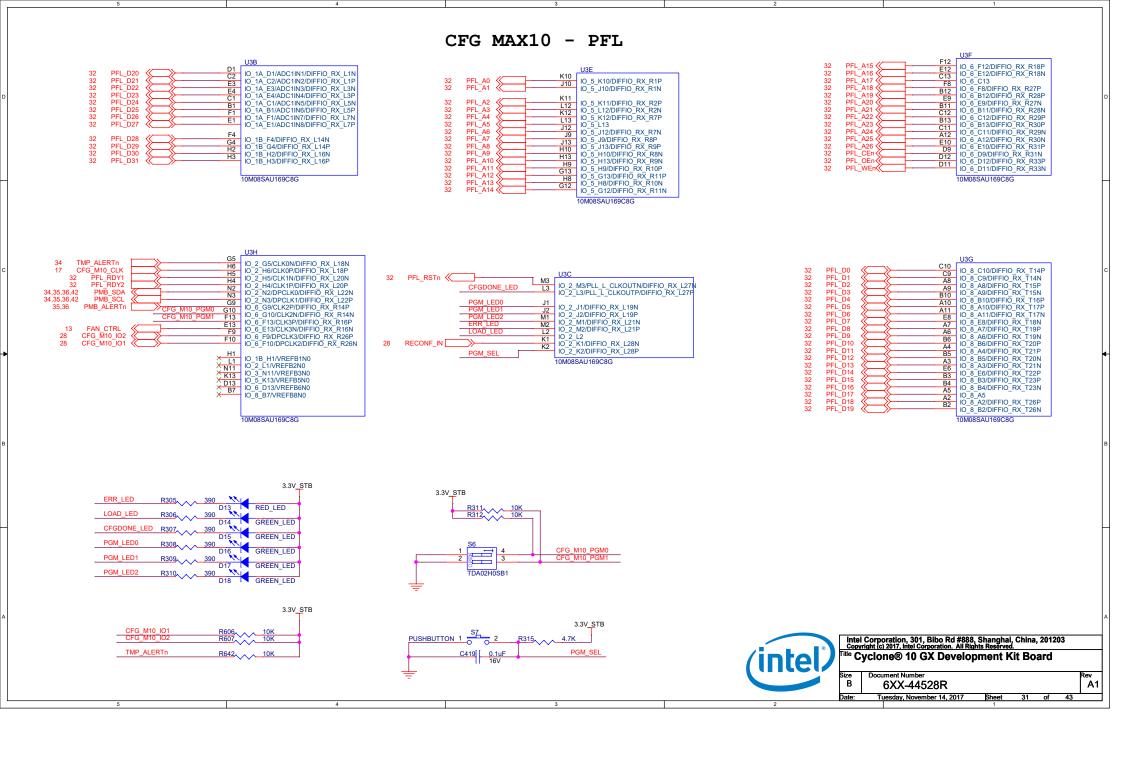
INTERFACE - GIGE - 1 ETH 2.5V GTX_CLK 4 IO 1.8V COMA ETH_RESETn RESET_N TX_CLK TX_EN TX ER 65 64 63 ETH_2.5V CONFIG0 R226 R227 R228 R229 CONFIG1 TXD0 > 4.7K > 4.7K > 4.7K > 4.7K 61 CONFIG2 CONFIG3 TXD1 TXD2 U34 RJ1 ETH_2.5V CONFIG4 TXD3 ETH_MDC ETH_LED_10 ETH_LED_RX ETH_MDC_C10 12 ETH_MDIO_C10 12 CONFIG5 TXD4 B0 A0 58 CONFIG6 VCC В1 12 TXD5 A1 ETH_MDI0_P TYD6 ETH_2.5V TD0_P ETH_MDI0_N ETH_MDI1_P MDI0 P TXD7 OE 31 MDI0_F 33 MDI0_N MDI1_P MDI1_N MDI2_P RXCLK 2 X VCCB VCCA ETH_MDI1_N TD1_P GND C322 C323 RX_ER ETH_MDI2_N ETH_MDI3_P 41 MDI2_P MDI2_N FXMA2102UMX RXD0 RXD1 RXD1 RXD2 PXD2 PXD2 PXD2 RXD2 0.1uF 0.1uF J.1€ 16V 42 MDI3_P MDI3_N TD2_P TD2_N ETH MDI3 N RXD2 RXD3 RXD4 RXD5 RXD5 RXD6 RXD7 RXD7 RXD7 GND GND GND MDIO ETH_MDC ETH_INTn 25 MDIO MDC INT_N × 38 HSDAC_P ___ CRS 84 X HFJ11-1G02E 30 × 56 R231 4.99K RSET COL ETH_2.5V IO_1.8V - S_CLK_P S_CLK_N S_IN_P S_IN_N S_OUT_P - S_OUT_N SEL_FREQ × 22 125CLK ETH 25MHz SGMII_TXN XTAL1 R232 R233 R234 R235 SGMII_RXP XTAL2 4.7K > 4.7K 4.7K > 4.7K S_OUT_N VSSC 47 49 TRST TCK TDI TDO TDO U35 LED_TX 68 69 FD FX 70 R236 TRST_N ETH LED RX ≫ETH_INTn_C10 12 __ETH_RESETn_C10 A0 LED DUPLEX ETH_LED_1000 ETH_LED_100 LED LINK1000 ETH_2.5V 1K R237 OE TMS LED LINK100 ETH_LED_10 LED_LINK10 VCCA GND VCCB 88E1111-B2-NDC2C000 C327 C326 FXMA2102UMX 0.1uF 0.1uF 16V ______0.1u. _____16V ETH 2.5V ETH_2.5V ETH_MDI0_P ETH_MDI0_N ETH_MDI1_P 49.9 C328 10nF 50V ETH_2.5V ETH_LED_TX D8 M GREEN LED R239 49.9 R240 R241 49.9 C329 R242 49.9 C330 R244 49.9 C330 R245 49.9 C331 10nF 50V R490 EN VCC GREEN LED ETH_MDI2_N ETH_MDI3_P 10nF 50V ETH_25MHz GND OUT ETH_LED_1000 D10 M GREEN LED R246 25.00MHz 10nF 50V GREEN LED R249 220 R248 49.9 ETH_LED_10 D12 CREEN LED R250 Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. Title Cyclone® 10 GX Development Kit Board Document Number Size B 6XX-44528R A1 Tuesday, November 14, 2017 Sheet 26 of



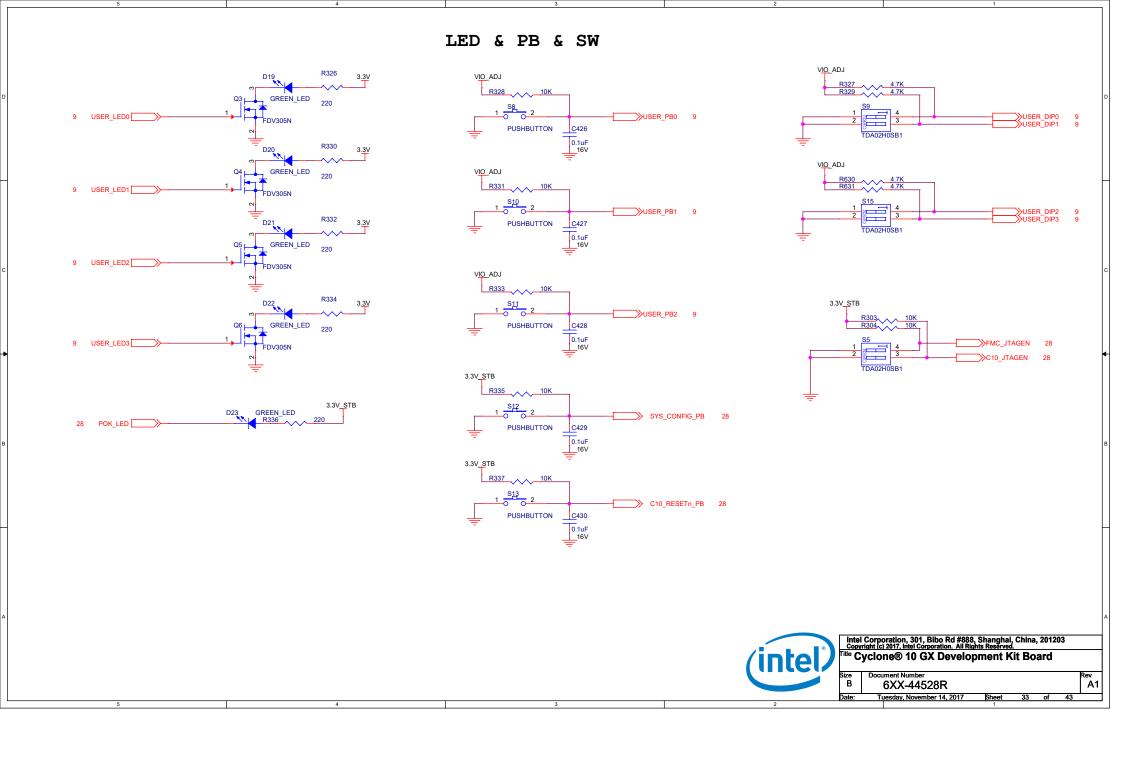


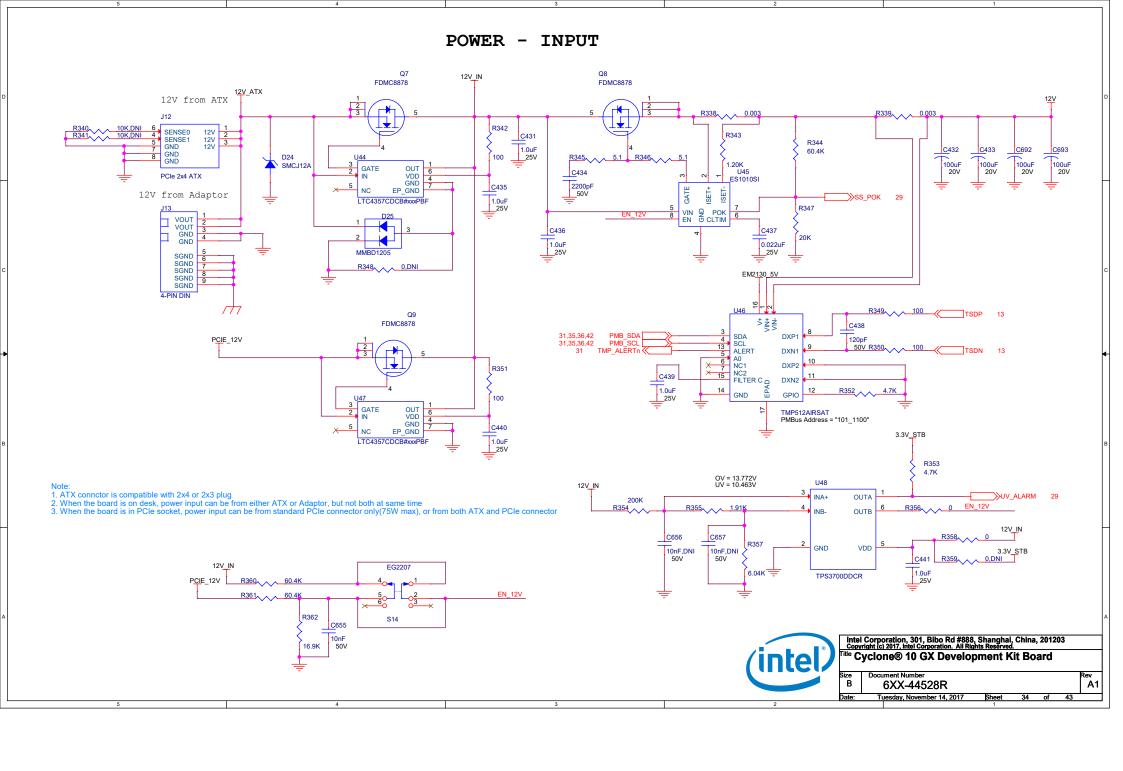


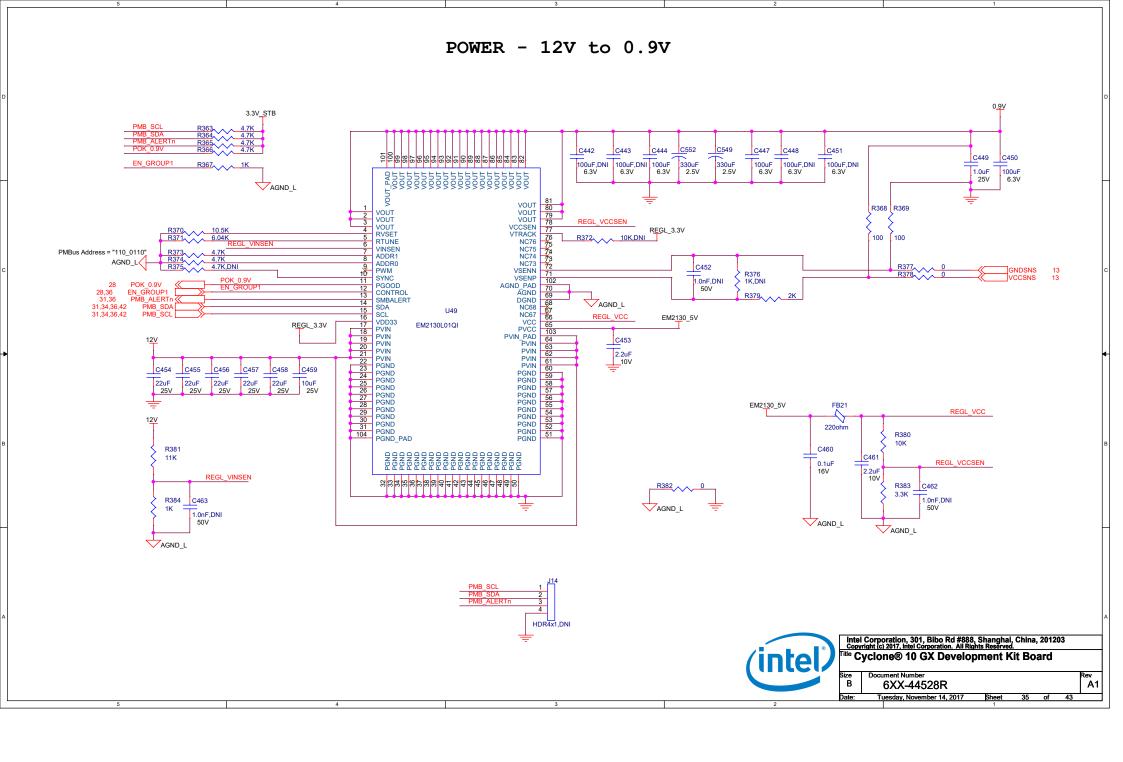




CFG PFL FLASH U42 U43 FLASH FLASH E3 H3 E4 H4 31,32 31,32 31,32 31,32 31,32 31,32 31,32 PFL_A0 PFL_A1 PFL_A2 PFL_A3 PFL_A4 PFL_A5 PFL_A6 31,32 31,32 31,32 D0 D1 D2 D3 D4 D5 D6 D7 D0 D1 D2 D3 D4 D5 D6 D7 31 31 31 31 31 31 31 31 31 31 31 31 31 31 E4 PFL_A1 PFL_A2 PFL_A3 PFL_A5 PFL_A6 PFL_A7 PFL_A8 PFL_A9 PFL_A10 PFL_D1 PFL_D2 PFL_D3 PFL_D4 PFL_D5 PFL_D6 PFL_D7 PFL_D10 PFL_D20 PFL_D21 31,32 31,32 31,32 H6 31,32 31,32 31,32 PFL_A7 PFL_A8 PFL_A9 PFL_A10 PFL_A11 31,32 31,32 31,32 31 31 F3 PFL_D8 PFL_D9 PFL_D10 PFL_D11 PFL_D12 PFL_D13 PFL_D14 PFL_D15 D8 G3 D9 F4 31 31 31 31 31 31 31 31 PFL D24 31 D8 D9 31,32 31,32 31,32 31,32 PFL_D25 PFL_D26 PFL_D27 31 31 31 31 31,32 31,32 D10 G4 D11 F5 D12 G6 D13 F6 D10 D11 D12 D13 G4 F5 G6 F6 G7 PFL_A12 PFL_A13 31,32 31,32 PFL_A12 PFL_A13 31,32 31,32 31,32 31,32 31,32 31,32 PFL_A14 PFL_A15 PFL_A16 PFL_A17 PFL_A18 PFL_A14 PFL_A15 PFL_A16 PFL_A17 PFL_A18 31 31 31 31,32 PFL D29 31,32 31,32 31,32 31,32 D14 D14 >PFL_D31 D15/A-1 D15/A-1 A4 A4 RY/BY# >>PFL_RDY1 RY/BY# >>PFL_RDY2 PFL_A19 31,32 PFL_A19 G5 PFL_A19 PFL_A20 PFL_A21 PFL_A22 PFL_A23 PFL_A24 PFL_A25 PFL_A19 PFL_A20 PFL_A21 PFL_A22 PFL_A23 PFL_A24 PFL_A25 PFL_A26 31,32 31,32 31,32 31,32 VCC1 31,32 31,32 VCC1 3.3V_STB 3.3V_STB D8 F1 VCCQ1 31,32 31,32 VCCQ1 VCCQ2 VCCQ2 G8 A24 B1 A25(512M) 31,32 31,32 31,32 31,32 31,32 A24 E8 H2 G8 A24 B1 A25(512M) GND1 GND2 GND1 GND2 H2 H7 31,32 A26(1G) A26(1G) GND3 GND3 B5 RESET# G2 CE# A5 OE# F7 WE# B4 WP# B5 C RESET# G2 C CE# A5 C OE# F7 WE# B4 C WP# Α1 Α1 NC1 NC2 NC3 NC7 NC8 RFU1 31,32 31,32 31,32 31,32 NC1 NC2 NC3 NC7 NC8 RFU1 RFU2 31,32 31,32 31,32 PFL_RSTn PFL_CEn A1 X A8 X D1 X H1 X H8 X C1 X E1 X G1 X PFL_RSTr PFL_CEn PFL_OEn PFL WEr 31,32 3.3V_STB 3.3V_STB R316 4.7K R318 4.7K R317 4.7K R319 4.7K RFU2 RFU3 RFU3 MT28EW01GABA1LPC-0SIT MT28EW01GABA1LPC-0SIT 3.3V_STB 3.3V_STB PFL_CEn R320 4.7K PFL_OEn R321 C420 C421 C422 C423 C424 C425 PFL_WEn R322 4.7uF 0.1uF 0.1uF 16V 0.1uF 16V 0.1uF 4.7uF PFL_RDY1 R323, 6.3V 16V 16V 6.3V PFL_RDY2 R324 PFL_RSTn R325 4.7K Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. Title Cyclone® 10 GX Development Kit Board Document Number Size B 6XX-44528R A1 Tuesday, November 14, 2017 Sheet 32 of

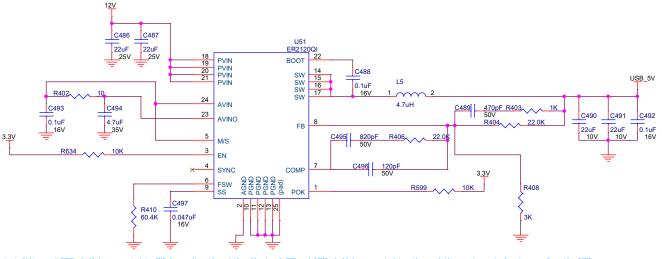




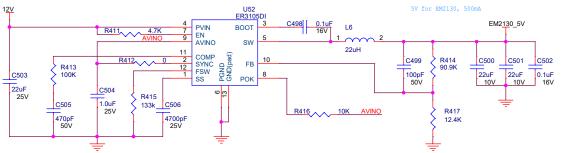


POWER - 12V to 3.3V 3.3V 3.3V_STB POK 3.3V R385 4.7K C464 C465 C466 C467 C468 C469 C470 C471 C472 C473 100uF 100uF 330uF 100uF 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 6.3V 1.0uF 25V VOUT 80 79 VOUT 2 VOUT R388 R387 VOUT REGH_VCCSEN 0 0 4 VOUT VCCSEN REGH_3.3V R391 10K,DNI 6 RTUNE 7 VINSEN NC76 NC75 PMBus Address = "110_0000" 8 ADDR1 R393 0 R394 4.7K,DNI NC74 AGND_H NC73 9 PWM C474 VSENN R395 11 SYNC PGOOD VSENP POK_3.3V 1.0nF,DNI 1K POK_3.3V EN_GROUP1 AGND_PAD 50V 28,35 CONTROL ĀĠND 13 CONTROL SMBALERT SDA R396 3.3V PMB ALERT DGND AGND_H NC68 U50 PMB_SCL 31.34.35.42 SCL NC67 REGH_VCC 16 SCL VDD33 EM2130 5V 177 VDD32 18 PVIN 19 PVIN 20 PVIN 21 PVIN 22 PVIN 22 PVIN 23 PGND 25 PGND 26 PGND 27 PGND 28 PGND 29 PGND 29 PGND 20 PGND 21 PGND 21 PGND 22 PGND 23 PGND 26 PGND 27 PGND 28 PGND 29 PGND 20 PGND 20 PGND 20 PGND 21 PGND 22 PGND 23 PGND 26 PGND 27 PGND 28 PGND 29 PGND 20 PGND 2 VCC REGH_3.3V EM2130H01QI C670 C671 PVCC 103 PVIN PAD 22uF 12V 22uF C475 PVIN 6.3V 6.3V 6.3V PVIN PVIN 2.2uF 10V PVIN 60 59 58 57 56 55 54 53 52 51 C476 C477 C478 C479 C480 C481 PGND PGND PGND 22uF 22uF 22uF 25V 25V 25V 22uF 10uF 25V 25V 25V PGND **PGND** EM2130_5V FB22 PGND PGND REGH VCC 1<u>2V</u> PGND 220ohm 104 PGND PAD PGND R397 **PGND** 10K C482 R398 C483 < 11K REGH_VCCSEN 0.1uF 2.2uF 16V 10V REGH VINSEN R400 C484 AGND_H 3.3K R401 C485 1.0nF,DNI 50V 1.0nF,DNI AGND_H AGND_H AGND_H 3.3V_STB C678 C673 C674 C675 C676 C677 C679 C680 C681 C682 U62 3.3V for Sys Control MAX10 1<u>2V</u> ER3110DI 22uF 22uF 22uF C620 0.1uF 3.3V_STB 6.3V PVIN BOOT R549 4.7K EN AVINO SW 22uH COMP C621 R552 C622 C623 C624 C625 C626 PGND GND(par SYNC FB R550 R609 90.9K FSW SS 0.1uF 22uF 27pF 50V 22uF C627 100K POK 6.3V 6.3V 16V 6.3V 6.3V 22uF 25V C628 R553 Intel Corporation, 301, Bibo Rd #888, Shanghai, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. 1.0uF 133k,DNI R555 C629 C630 25V R554 10K AVINO_1 Title Cyclone® 10 GX Development Kit Board 470pF 4700pF 50V 25V 20K Size B 6XX-44528R A1 ÷ Tuesday, November 14, 2017 Sheet 36 of

POWER - 12V to 5V

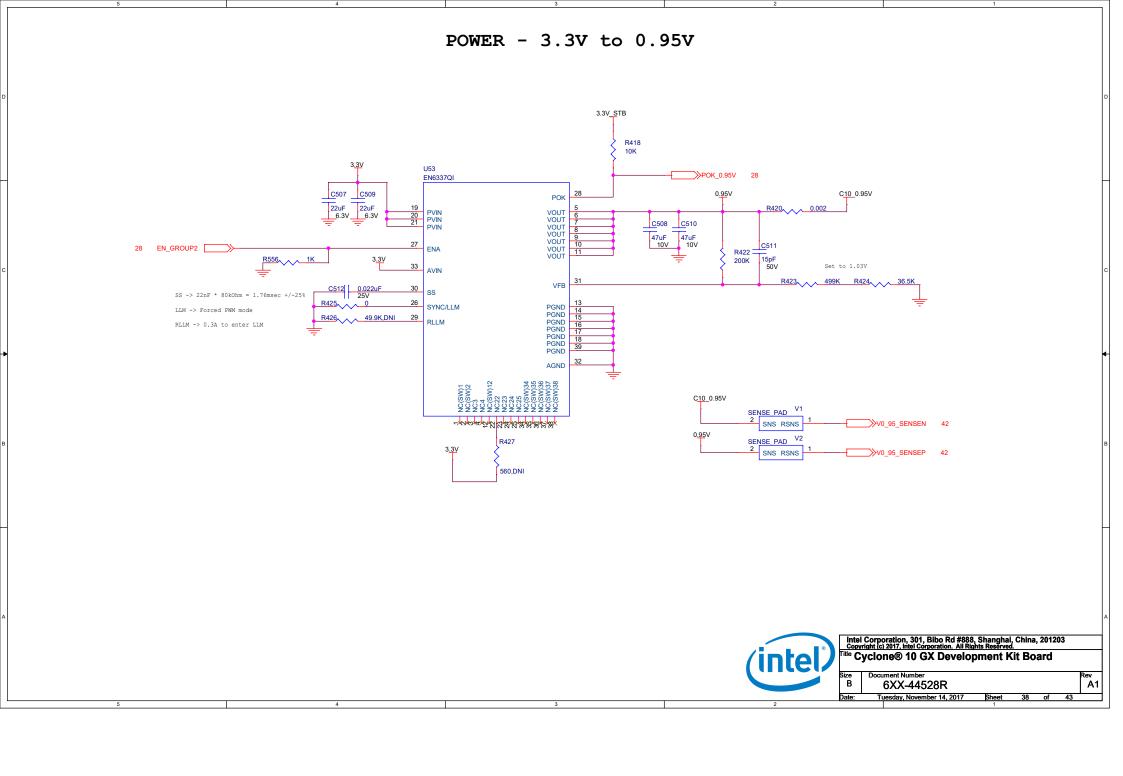


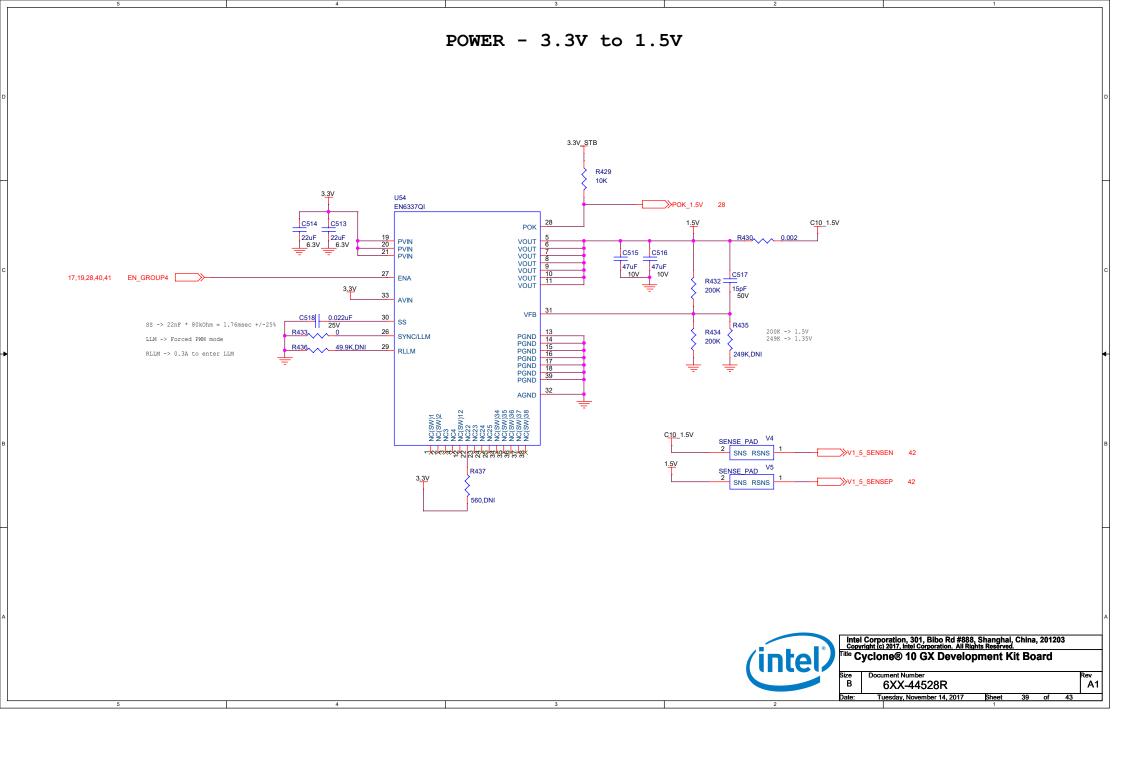
GND of input/output filter and PGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area



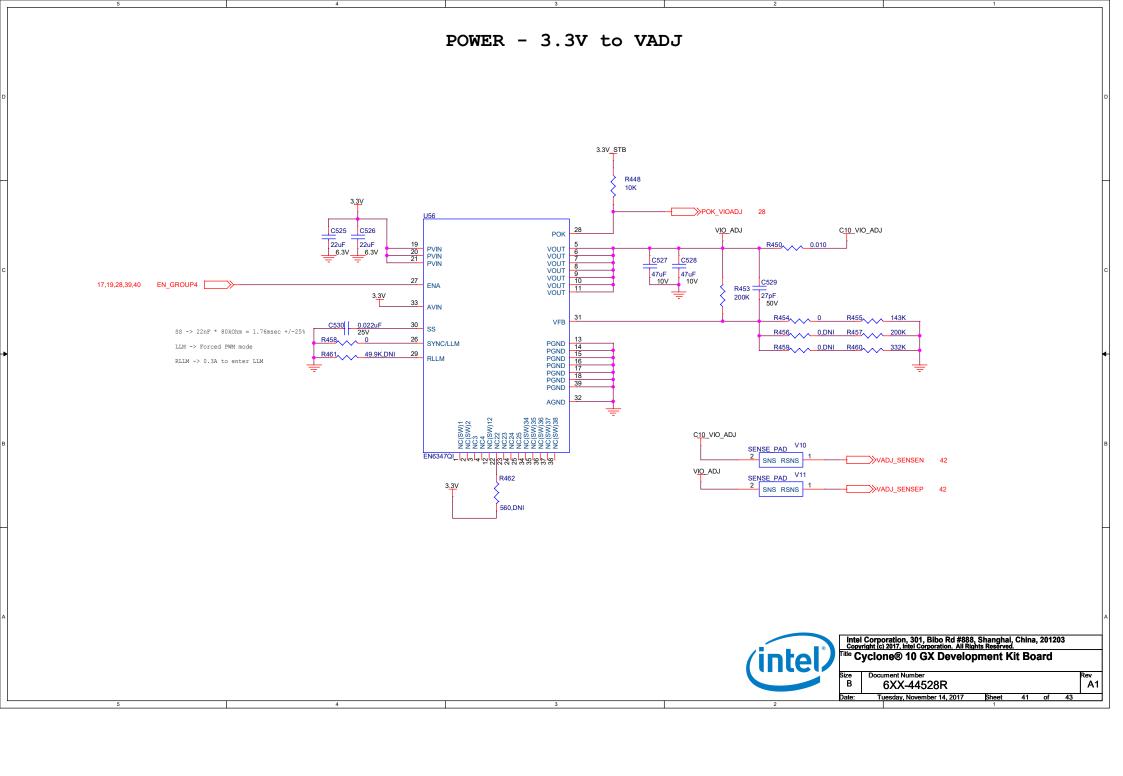
GND of input/output filter and FGND shall be connected to GND layer directly, while all signal GND and AGND shall be connected together and then go to a single via away from the PGND area







POWER - 3.3V to 1.8V U55 3.3V_STB EN6337QI C519 C520 POK 22uF 6.3V = 6.3V 1<u>.8V</u> C10_1.8V 20 PVIN 21 PVIN VOUT VOUT R440 0.002 VOUT VOUT VOUT PVIN C521 ____C522 C523 R443 47uF 10V 28 EN_GROUP3 ENA 47uF 10V VOUT 15pF 50V 200K R442 33 AVIN VFB SS $SS \rightarrow 22nF * 80kOhm = 1.76msec +/-25%$ R445 R444 0 SYNC/LLM **PGND** LLM -> Forced PWM mode PGND 49.9K,DNI RLLM PGND RLLM -> 0.3A to enter LLM 143K PGND PGND PGND PGND 3<u>.3V</u> AGND R447 C10_1.8V SENSE PAD V7 2 SNS RSNS >V1_8_SENSEN 560.DNI 1.8V SENSE_PAD_V8 SNS RSNS >V1_8_SENSEP 3.3V_STB 3.3V U60 EN6337QI C601 POK ≫POK_1.8VIO 22uF 6.3V 19 20 21 1.8VIO IO_1.8V VOUT VOUT VOUT PVIN PVIN PVIN R530 0.010 VOUT C603 C604 C605 VOUT 27 R533 17.19.28.39.41 EN_GROUP4 ENA 47uF 10V 47uF 15pF 50V 200K VOUT 3<u>.3</u>V 10V 33 AVIN VFB $SS \rightarrow 22nF * 80kOhm = 1.76msec +/-25%$ R536 26 SYNC/LLM PGND PGND LLM -> Forced PWM mode R537 49.9K,DNI 29 RLLM PGND RLLM -> 0.3A to enter LLM 143K PGND PGND PGND 3<u>.3</u>V AGND R538 IO_1.8V SENSE PAD V15 2 SNS RSNS >>IO1_8_SENSEN 560.DNI Intel Corporation, 301, Bibo Rd #888, Shanghal, China, 201203 Copyright (c) 2017, Intel Corporation. All Rights Reserved. 1.8VIO SENSE_PAD V16 Title Cyclone® 10 GX Development Kit Board SNS RSNS >>IO1_8_SENSEP Size B 6XX-44528R A1 Tuesday, November 14, 2017 Sheet



POWER - CURRENT SENSE

