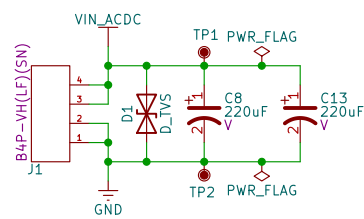
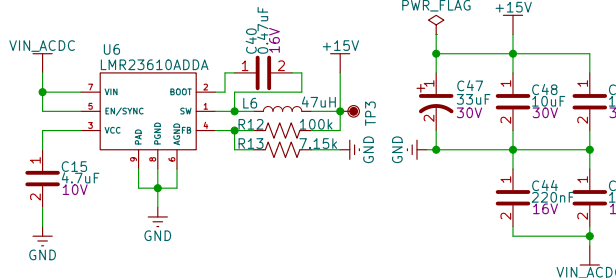


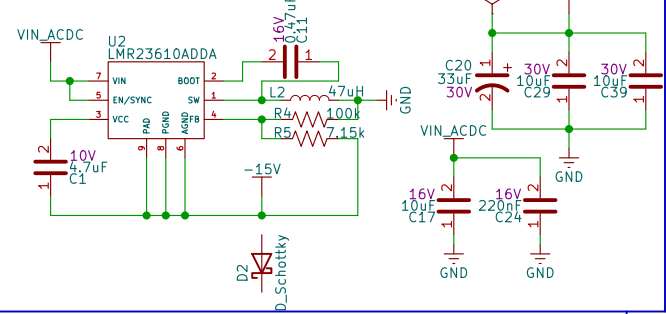
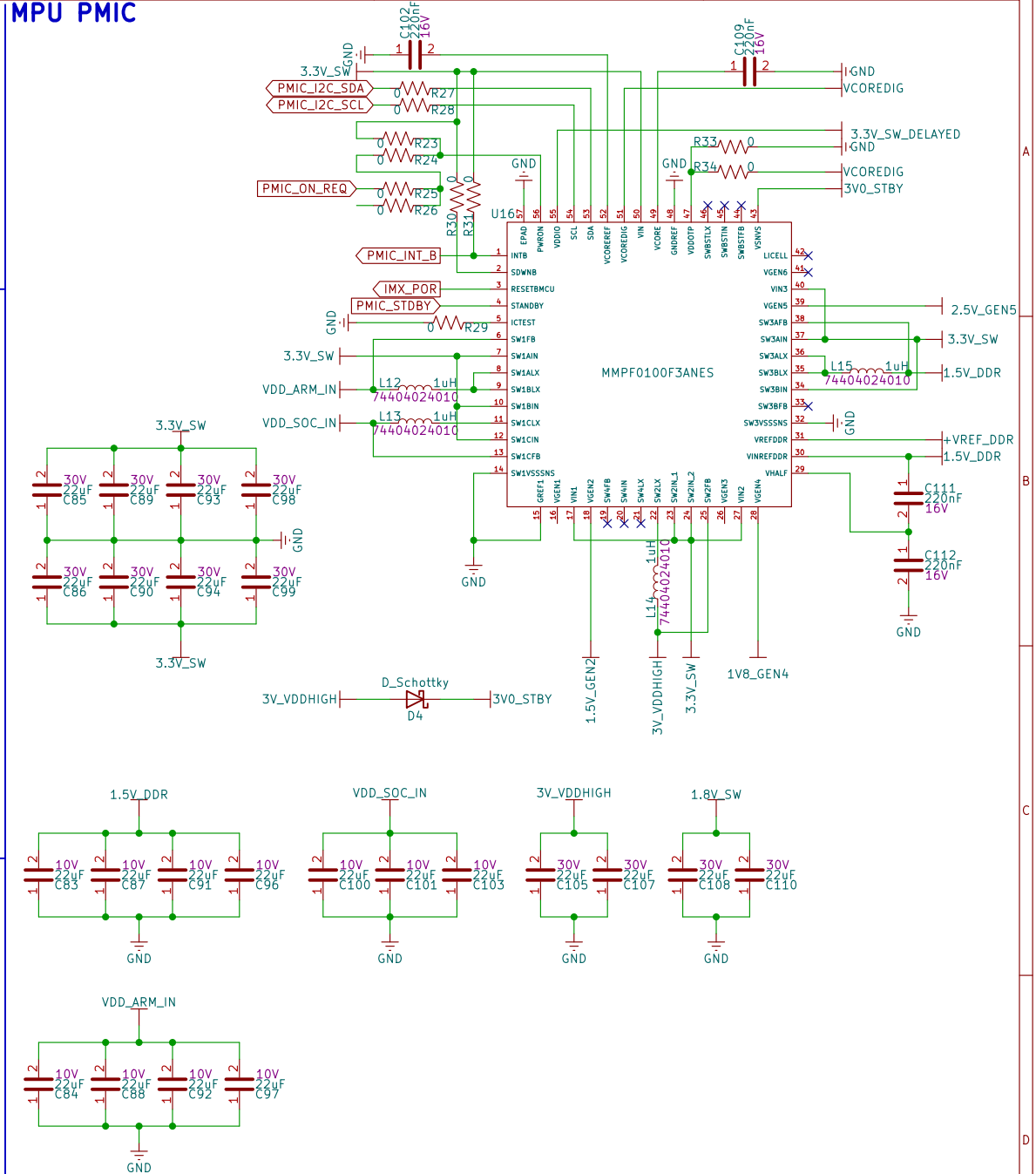
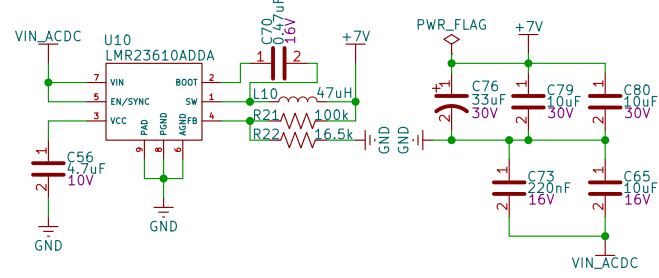
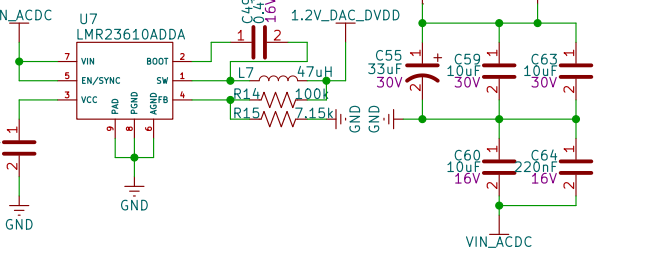
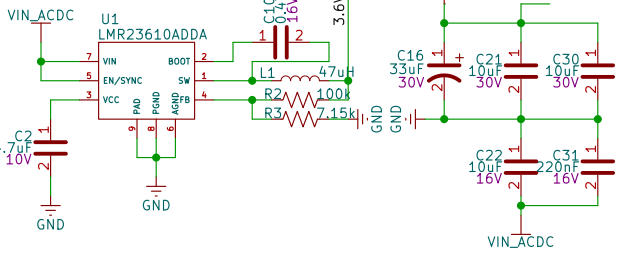
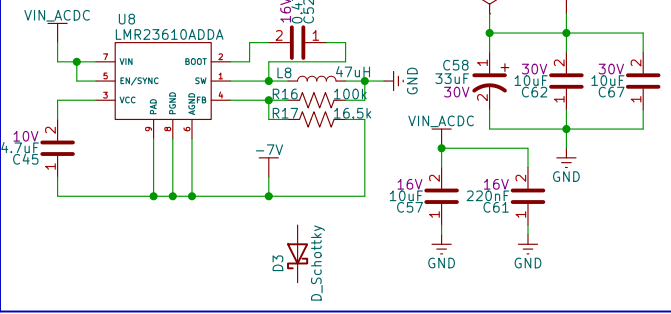
[illegible]

15V 1A SMPS

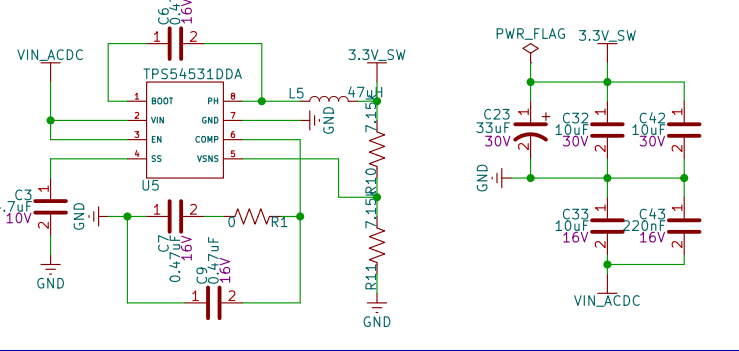
The diagram shows a 15V 1A SMPS circuit. The input is VIN_ACDC, which is filtered by capacitor C15 (4.7uF, 10V) and connected to the VIN pin of U6. The EN/SYNC pin is connected to VIN, and the VCC pin is connected to the +15V output. The GND pin is connected to ground. The BOOT pin is connected to the SW pin through a 47uH inductor L6. The SW pin is connected to the output filter network consisting of capacitor C40 (330uF, 10V) and resistor R12 (100k). The output is also connected to a 7.15k resistor R13 to ground. The output is labeled +15V and GND TP3. A PWR_FLAG pin is shown connected to the +15V output. The output is also connected to a filter network with capacitors C47 (330uF, 30V), C48 (100uF, 30V), C54 (10uF, 30V), C44 (220nf, 16V), and C36 (10uF, 16V). The input of this second filter network is connected to the +15V output, and its output is connected to the VIN_ACDC input of the next stage.



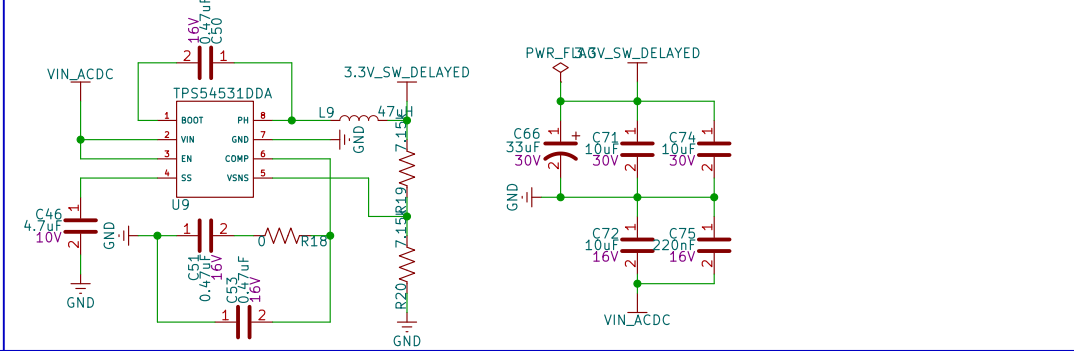
7V 1A SMPS

[illegible]

3.3V 5A PMIC_VIN

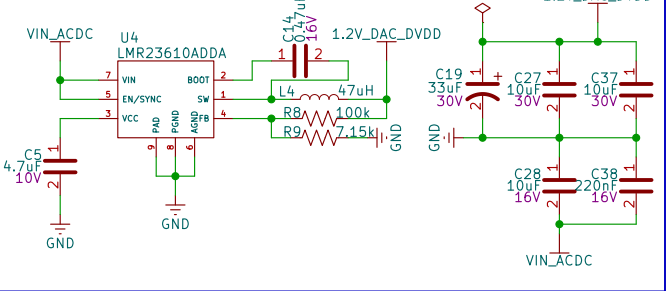


3.3V 5A PERIPHERALS SMPS



FPGA VCC CORE

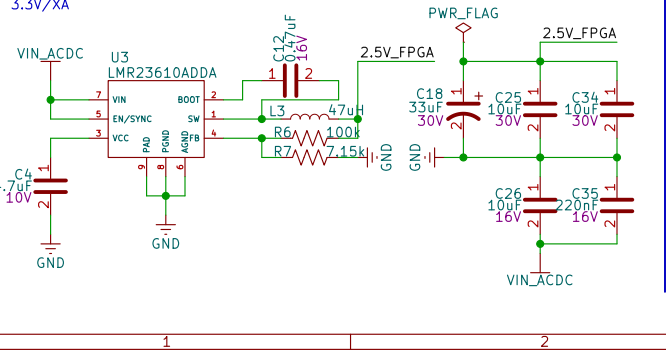
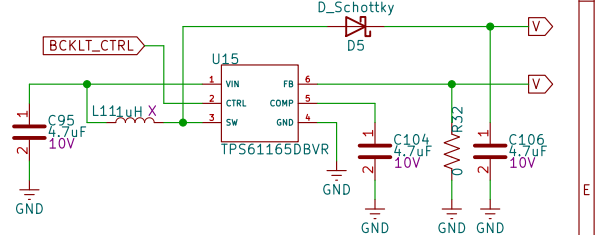
The schematic diagram illustrates the FPGA VCC CORE circuit. It features a buck converter (U4, LMR23610A) that steps down the input voltage (VIN_ACDC, 4.7V) to the output voltage (1.2V_DAC_DVDD). The circuit includes a 47uH inductor (L4) and a 100k resistor (R8) for the feedback network. The output is filtered by a 33uF capacitor (C19) and a 10uF capacitor (C27). The output is also connected to a 1.2V_DAC_DVDD input. The circuit is powered by a 4.7V input (VIN_ACDC) and a 1.2V output (1.2V_DAC_DVDD).



POWER SUPPLIES TREE

```
graph TD; VIN_ACDC --> SW1[SW]; SW1 --> P15V[+15V]; VIN_ACDC --> SW2[SW]; SW2 --> P15V[+15V]; VIN_ACDC --> SW3[SW]; SW3 --> P7V[+7V]; VIN_ACDC --> SW4[SW]; SW4 --> P7V[+7V]; VIN_ACDC --> SW5[SW]; SW5 --> P12V_DAC_DVDD[1.2V_DAC_DVDD]; VIN_ACDC --> SW6[SW]; SW6 --> LDO1[LDO]; LDO1 --> P33V_DAC_AN[3.3V_DAC_AN]; SW6 --> LDO2[LDO]; LDO2 --> P12V_DAC_CLK[1.2V_DAC_CLK]; SW6 --> LDO3[LDO]; LDO3 --> P12V_DAC_VDD[1.2V_DAC_VDD]; VIN_ACDC --> SW7[SW]; SW7 --> P33V_SW[3.3V_SW]; SW7 --> SW8[SW]; SW8 --> P_VDD_ARM_IN[VDD_ARM_IN];
```

The diagram illustrates the power supply tree for the system. It starts with VIN_ACDC at the top, which branches into several paths. The first path goes through a switch (SW) to a +15V supply. The second path also goes through a switch (SW) to a +15V supply. The third path goes through a switch (SW) to a +7V supply. The fourth path goes through a switch (SW) to a +7V supply. The fifth path goes through a switch (SW) to a 1.2V_DAC_DVDD supply. The sixth path goes through a switch (SW) to a 3.3V_DAC_AN supply, a 1.2V_DAC_CLK supply, and a 1.2V_DAC_VDD supply. The seventh path goes through a switch (SW) to a 3.3V_SW supply, which then branches into a VDD_ARM_IN supply.

[illegible]

ETHERNET

ETHERNET

MCIMX6S8DV10AD

RGMIIL_RX_CTL D22 RGMII_RX_CTL
RGMII_RXD3 D23 RGMII_TD0
RGMII_RXD2 B24 RGMII_TD1
RGMII_RXD1 B23 RGMII_TD2
RGMII_RXD0 C24 RGMII_TD3
RGMII_RXC B25 RGMII_RXC
RGMII_TX_CTL C23 RGMII_TX_CTL
RGMII_RXD0 A24 RGMII_RXD0
RGMII_RXD1 E21 RGMII_RXD1
RGMII_RXD0 F20 RGMII_RXD0
RGMII_TXC C22 RGMII_TXC
RGMII_TXC D21 RGMII_TXC

U17K

3.3V_SW-DELAYED
FerriteBead
F89
ETH_VDDA
GND
C377 10V
C378 10V
C379 10V
C380 10V
C381 10V
C382 10V
C383 10V
C384 10V
C385 10V
C386 10V
C387 10V
C388 10V
C389 10V
C390 10V
C391 10V
C392 10V
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C531 10V
C532 10V
C533 10V
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C538 10V
C539 10V
C540 10V
C541 10V
C542 10V
C543 10V
C544 10V
C545 10V
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C562 10V
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C566 10V
C567 10V
C568 10V
C569 10V
C570 10V
C571 10V
C572 10V
C573 10V
C574 10V
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C580 10V
C581 10V
C582 10V
C583 10V
C584 10V
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C616 10V
C617 10V
C618 10V
C619 10V
C620 10V
C621 10V
C622 10V
C623 10V
C624 10V
C625 10V
C626 10V
C627 10V
C628 10V
C629 10V
C630 10V
C631 10V
C632 10V
C633 10V
C634 10V
C635 10V
C636 10V
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C665 10V
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C668 10V
C669 10V
C670 10V
C671 10V
C672 10V
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C709 10V
C710 10V
C711 10V
C712 10V
C713 10V
C714 10V
C715 10V
C716 10V
C717 10V
C718 10V
C719 10V
C720 10V
C721 10V
C722 10V
C723 10V
C724 10V
C725 10V
C726 10V
C727 10V
C728 10V
C729 10V
C730 10V
C731 10V
C732 10V
C733 10V
C734 10V
C735 10V
C736 10V
C737 10V
C738 10V
C739 10V
C740 10V
C741 10V
C742 10V
C743 10V

U17D
MCIMX6S8DV0M10AD

LCD_RESET

D

24 X1 CSIO_MCLK
21 X1 CSIO_PIXCLK
20 X2 CSIO_VSYNC
19 X3 CSIO_DATA_EN
18 X4 CSIO_DATA4
17 X2 CSIO_DATA5
16 X4 CSIO_DATA6
15 X3 CSIO_DATA7
14 X6 CSIO_DATA8
13 X5 CSIO_DATA9
12 X4 CSIO_DATA10
11 X3 CSIO_DATA11
10 X2 CSIO_DATA12
9 X4 CSIO_DATA13
8 X4 CSIO_DATA14
7 X6 CSIO_DATA15
6 X4 CSIO_DATA16
5 X3 CSIO_DATA17
4 X6 CSIO_DATA18
3 X6 CSIO_DATA19

CS

LCD_RGB_B0B8

E

23 X3 CSLCLKOM
22 X3 CSLCLKOP
21 X4 CSLD0M
20 X3 CSLD0P
19 X1 CSLD1M
18 X3 CSLD1P
17 X1 CSLD2M
16 X2 CSLD2P
15 X2 CSLD3M
14 X1 CSLD3P
13 X4 CSLREXT

MIPI CSI

DSI0_D0
DSI0_D1
DSI0_D2
DSI0_D3
DSI0_D4
DSI0_D5
DSI0_D6
DSI0_D7
DSI0_D8
DSI0_D9
DSI0_D10
DSI0_D11
DSI0_D12
DSI0_D13
DSI0_D14
DSI0_D15
DSI0_D16
DSI0_D17
DSI0_D18
DSI0_D19
DSI0_D20
DSI0_D21
DSI0_D22
DSI0_D23
DSI0_D24
DSI0_D25
DSI0_D26
DSI0_D27
DSI0_D28
DSI0_D29
DSI0_D30
DSI0_D31

MIPI DSI

LCD_CLK
LCD_HSYNC
LCD_VSYNC
LCD_ENABLE
LCD_B0
LCD_B1
LCD_B2
LCD_B3
LCD_B4
LCD_B5
LCD_B6
LCD_B7
LCD_G0
LCD_G1
LCD_G2
LCD_G3
LCD_G4
LCD_G5
LCD_G6
LCD_G7
LCD_R0
LCD_R1
LCD_R2
LCD_R3
LCD_R4
LCD_R5
LCD_R6
LCD_R7

USB

U17C
MCIMX6S8DVM10AD

JTAG_TCK H5 JTAG_TCK R45 49.9
JTAG_TMS C3 JTAG_TMS R46 49.9
JTAG_TDI G5 JTAG_TDI R47 49.9
JTAG_TDO G6 JTAG_TDO R48 49.9
JTAG_RST C2 JTAG_RST R49 49.9
JTAG_MOD H6 JTAG_MOD R50 49.9
IMX_RST C11 IMX_RST R51 49.9
BOOT_MODE0 C12 BOOT_MODE0 R52 49.9
BOOT_MODE1 F12 BOOT_MODE1 R53 49.9
TEST_MODE F12 TEST_MODE R54 49.9
TAMPER F11 TAMPER R55 49.9
PMIC_STBY_REQ F11 PMIC_STBY_REQ R56 49.9
PMIC_ON_REQ D11 PMIC_ON_REQ R57 49.9
CLK1_P D7 CLK1_P R58 49.9
CLK1_N C7 CLK1_N R59 49.9
CLK2_P D5 CLK2_P R60 49.9
CLK2_N C5 CLK2_N R61 49.9
XTAL_I A7 XTAL_I R62 49.9
XTAL_O B7 XTAL_O R63 49.9
RTC_XTAL_I D9 RTC_XTAL_I R64 49.9
RTC_XTAL_O C9 RTC_XTAL_O R65 49.9

3.3V_SW_DELAYED

24MHz

32.768kHz

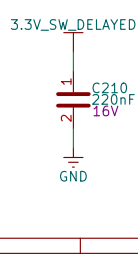
C157 10uF
C158 10uF
C159 10uF
C164 10uF

R45 49.9
R46 49.9
R47 49.9
R48 49.9
R49 49.9
R50 49.9
R51 49.9
R52 49.9
R53 49.9
R54 49.9
R55 49.9
R56 49.9
R57 49.9
R58 49.9
R59 49.9
R60 49.9
R61 49.9
R62 49.9
R63 49.9
R64 49.9
R65 49.9

JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_RST
JTAG_MOD
IMX_RST
BOOT_MODE0
BOOT_MODE1
TEST_MODE
TAMPER
PMIC_STBY_REQ
PMIC_ON_REQ
CLK1_P
CLK1_N
CLK2_P
CLK2_N
XTAL_I
XTAL_O
RTC_XTAL_I
RTC_XTAL_O

2

3



Sheet: /MPU/		
File: MPU.kicad_sch		
Title:		
Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.99.0-11430-ge61b1f03bb8)		Id: 3/7

Sheet: /MEMORY/
File: MEMORY.kicad_sch

Title:

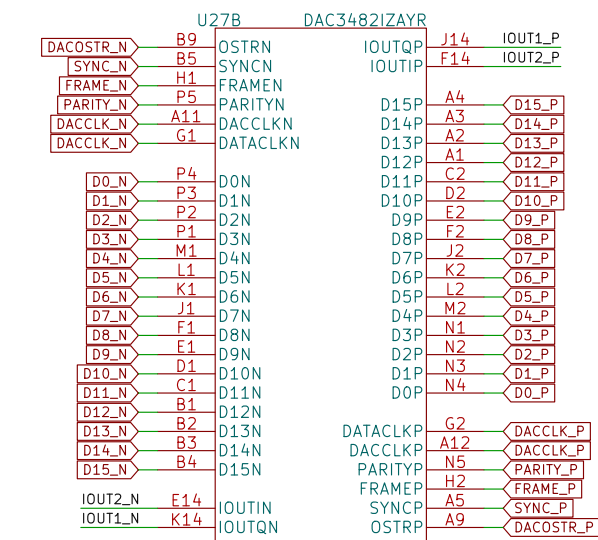
Size: A3 Date: Rev: 4/7
KiCad E.D.A. kicad (5.99.0-11430-ge61b1f03b8)

File: MEMORY.kicad_sch

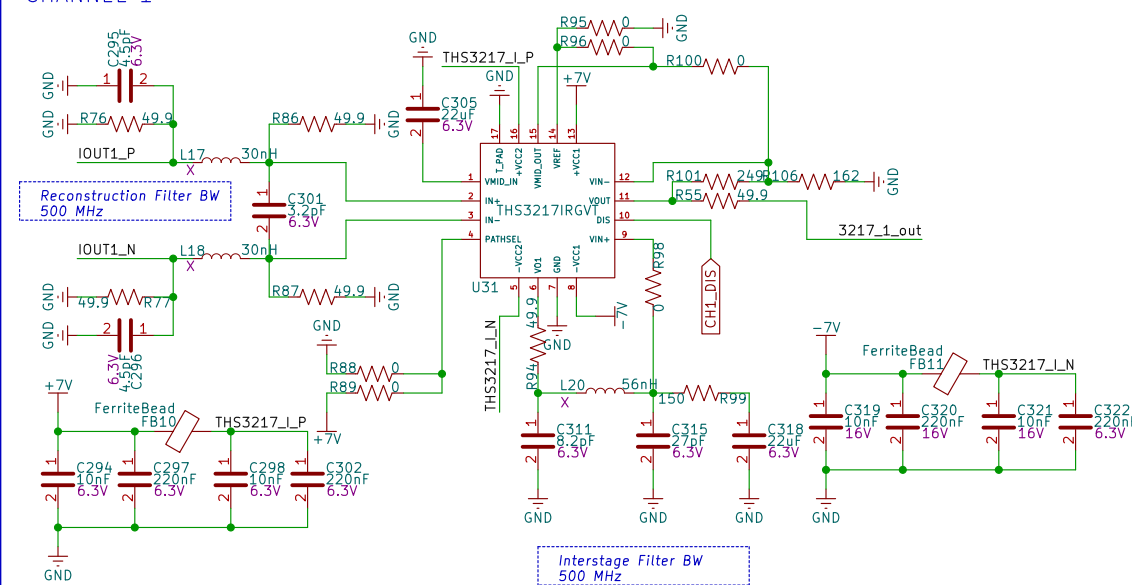
Size: A3	Date:	Rev:
----------	-------	------

	7	8
--	---	---

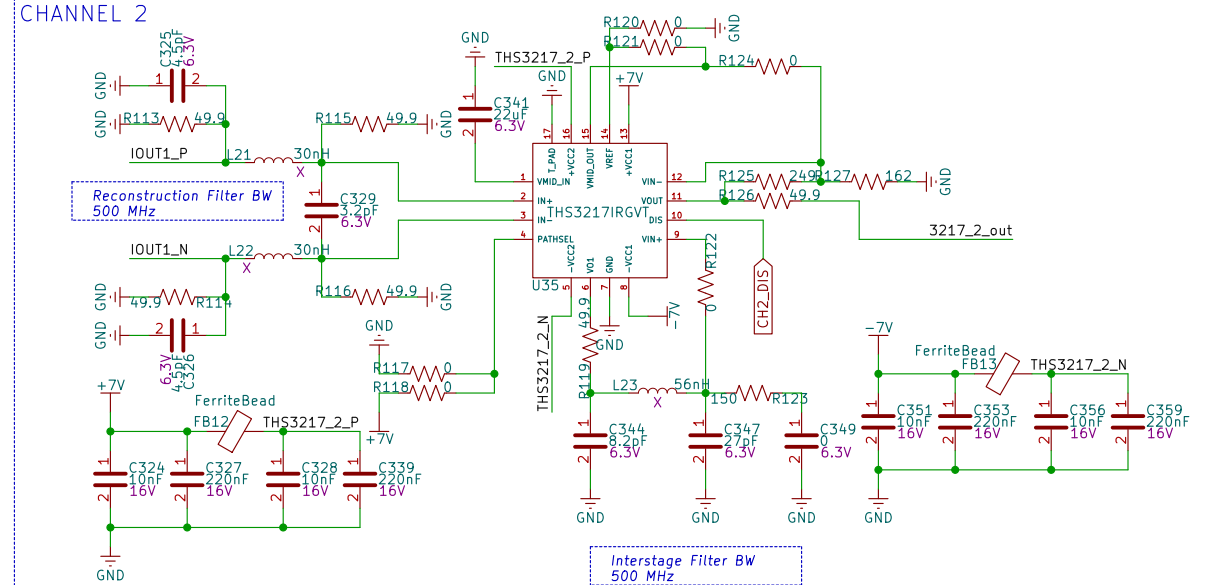
DAC I/O



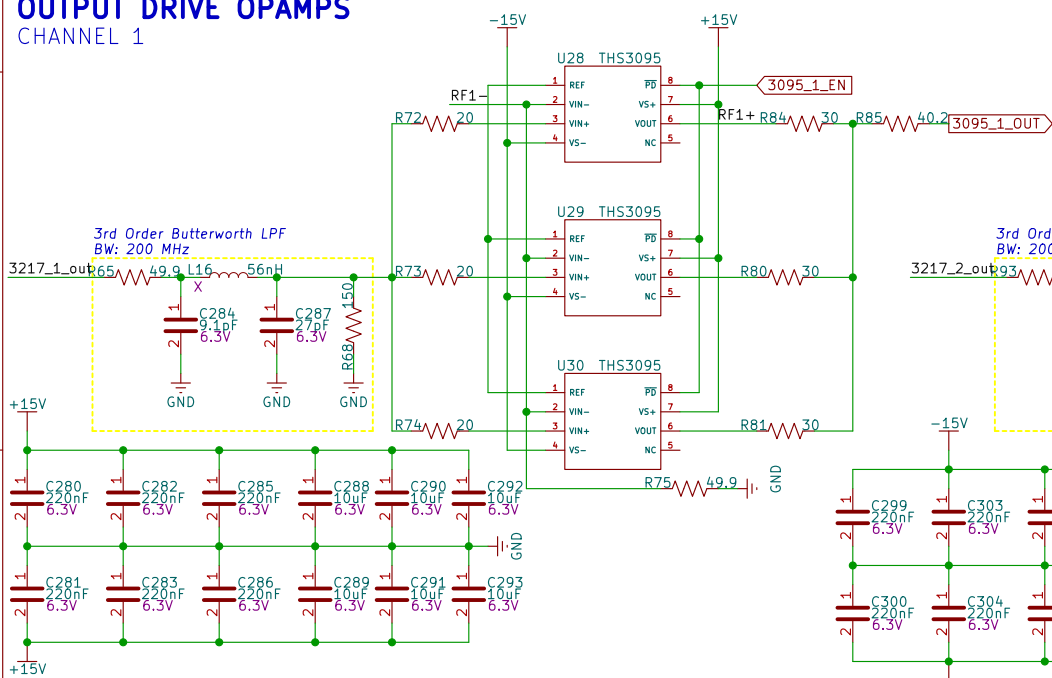
DIFFERENTIAL TO SINGLE ENDED CHANNEL 1



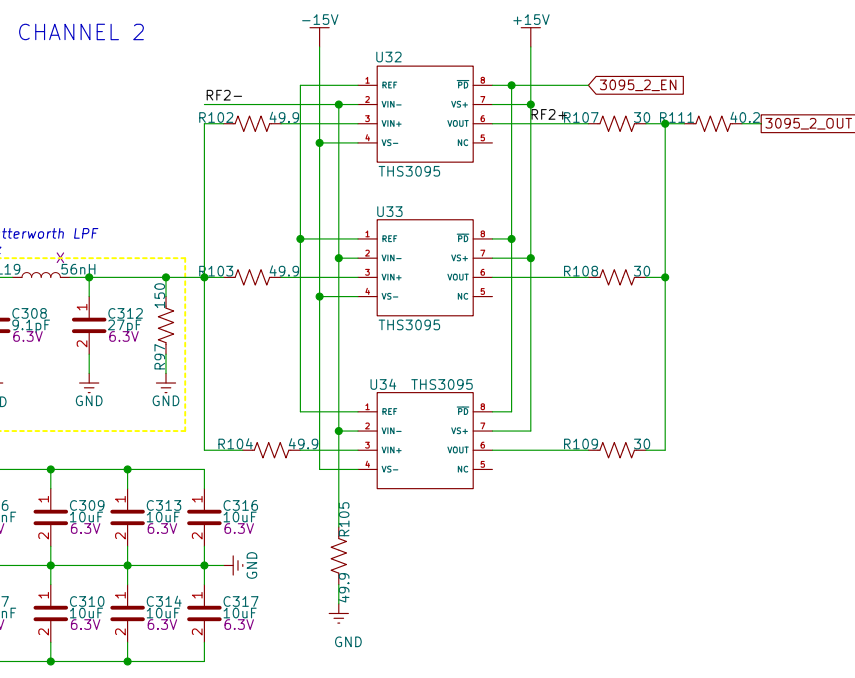
CHANNEL 2



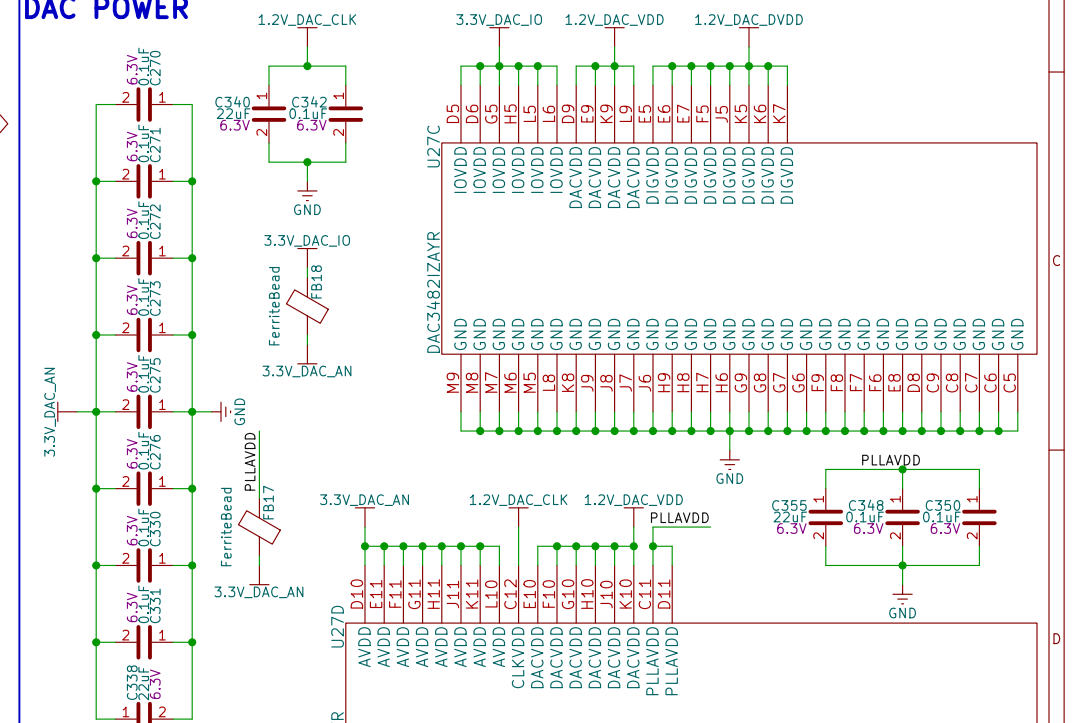
OUTPUT DRIVE OPAMPS



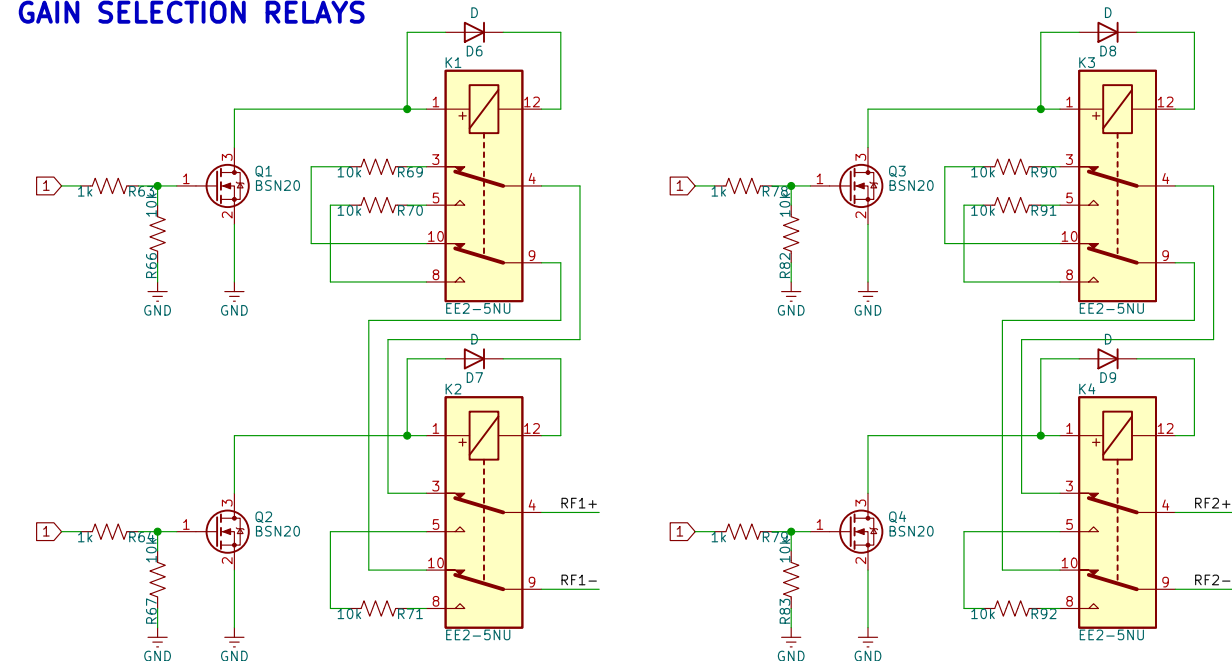
CHANNEL 2



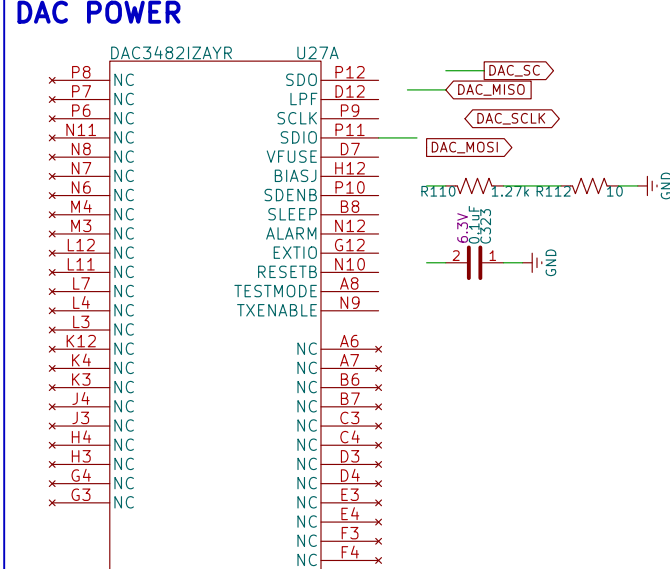
DAC POWER



GAIN SELECTION RELAYS



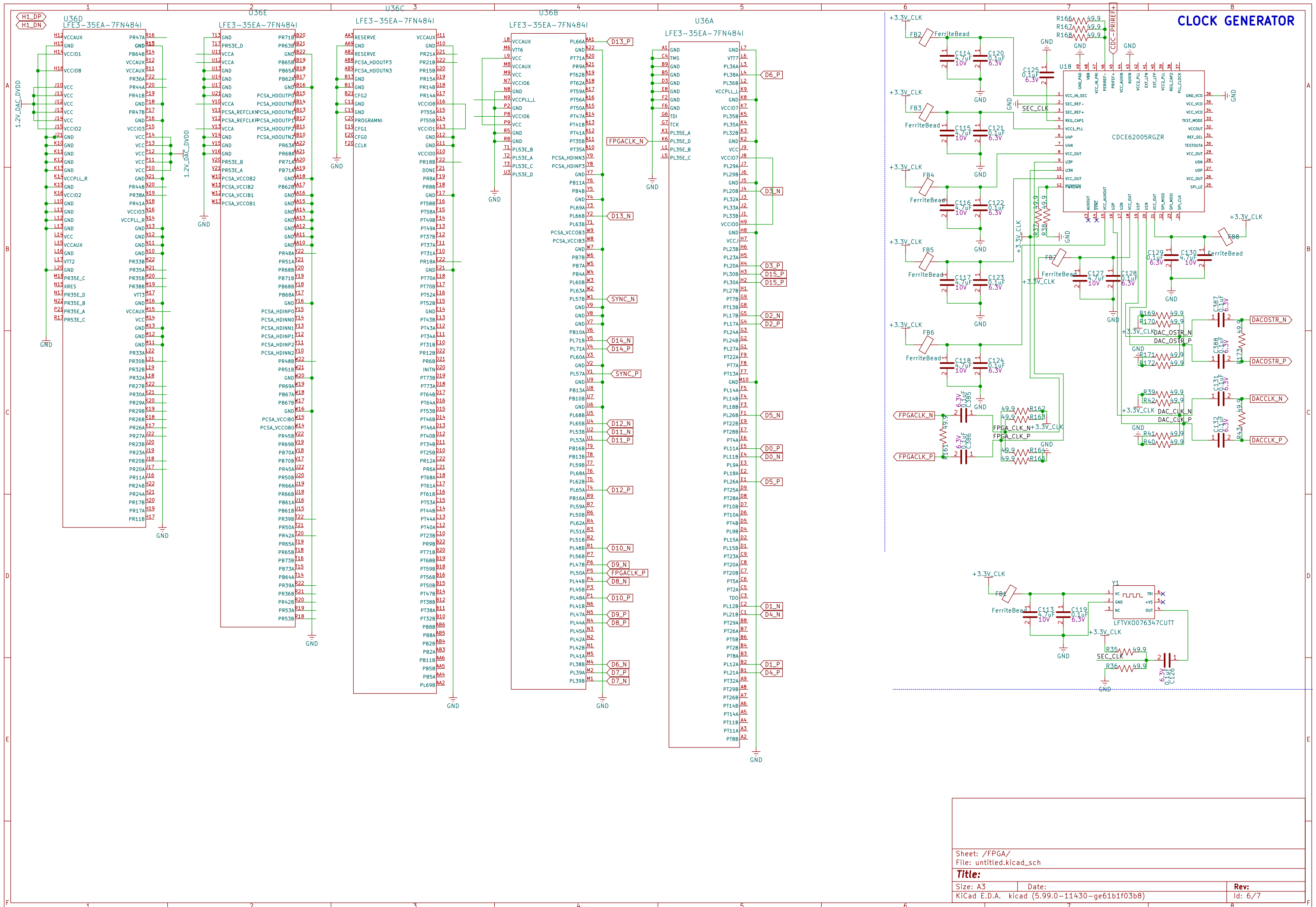
DAC POWER



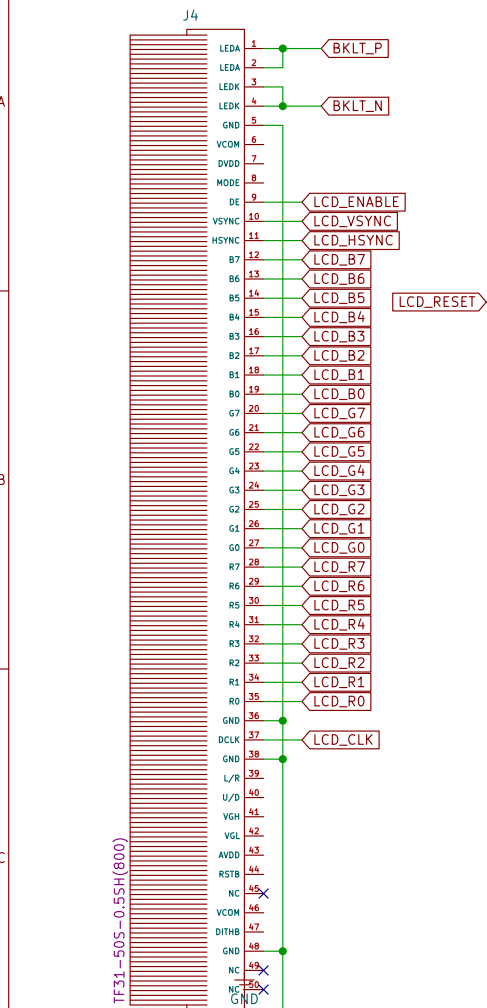
POWER SUPPLIES SUMMARY			
NET NAME	TYPE	VOLT	CURRENT
3.3V_DAC_AN	LINEAR	3.3V	100mA
3.3V_DAC_IO			
1.2V_DAC_CLK			
1.2V_DAC_VDD	LINEAR	1.2V	125mA
1.2V_DAC_DVDD	SWITCHING	1.2V	500mA

Sheet: /DAC/
File: DAC.kicad_sch

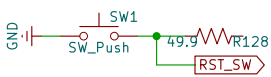
Title:		
Size: A3	Date:	Rev:
KiCad E.D.A. kicad (5.99.0-11430-ge61b1f03b8)		Id: 5/7



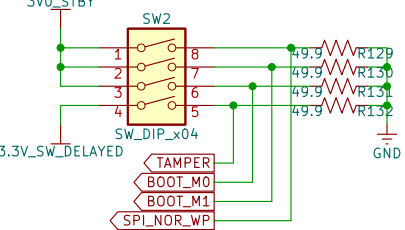
LCD INTERFACE



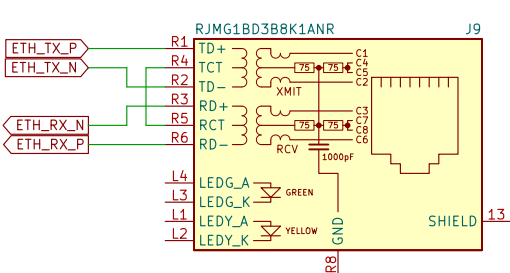
FORCED MPU REBOOT



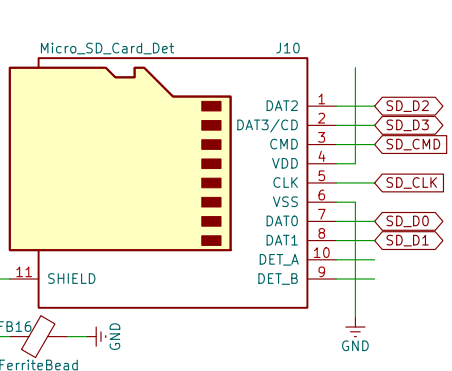
BOOT&SPI CNTRL



ETHERNET



SD CARD

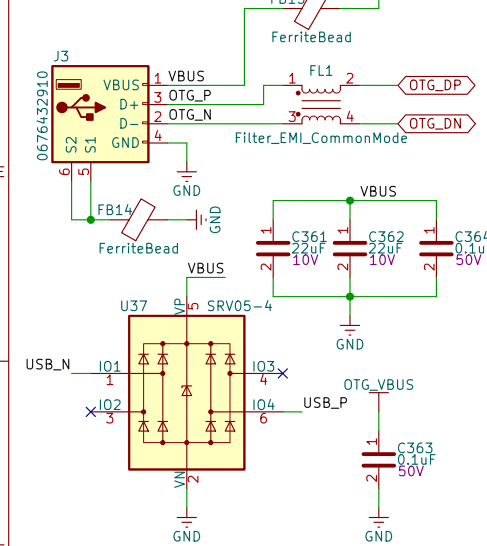


ON/OFF SWITCH

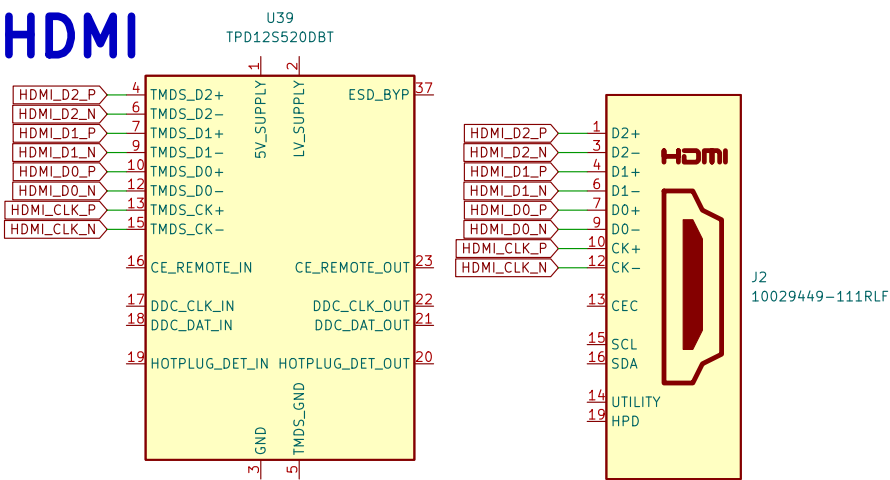
TOUCH I2C



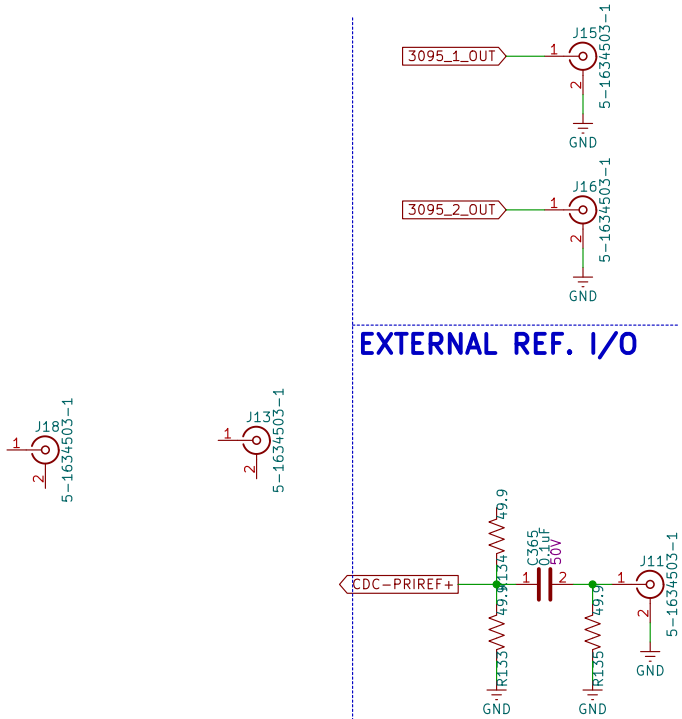
USB OTG



HDMI



BNC CONNECTORS



EXTERNAL REF. I/O