Module_4x5
Module_4x5.SchDoc

CPLD
CPLD.SchDoc

PWR0
PWR0.SchDoc

PCIE_CONN
PCIE_CONN.SchDoc

FTDI
FTDI.SchDoc

PWR1
PWR1.SchDoc

FMC
FMC.SchDoc

SD
SD.SchDoc

FMC_PWR
FMC_PWR.SchDoc

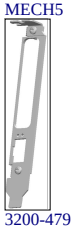
ETHERNET
ETHERNET.SchDoc

USB
USB.SchDoc

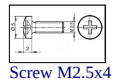
FireFly
FireFly.SchDoc

SFP_SATA
SFP_SATA.SchDoc

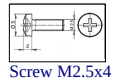
MECH5



3200-479

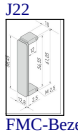


Screw M2.5x4



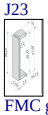
Screw M2.5x4

J22



FMC-Bezel

J23

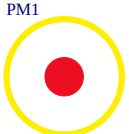


FMC gasket

Screw M2.5x6

Screw M2.5x6

PM1

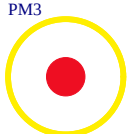


FIDU-DOT - small

PM2

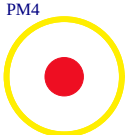
FIDU-DOT - small

PM3



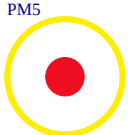
FIDU-DOT - small

PM4



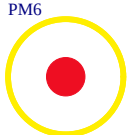
FIDU-DOT - small

PM5



FIDU-DOT - small

PM6



FIDU-DOT - small

Serial1
Serial
Serialnumber 6,3 x 6.3mm

LOGO1
TE Logo PRINT Layer
LOGO PRINT

Assembly variant	default
Created by	MR
Modified by	MR
Modified at	2019-09-24
SVN Revision	9225 [Locally Modified]

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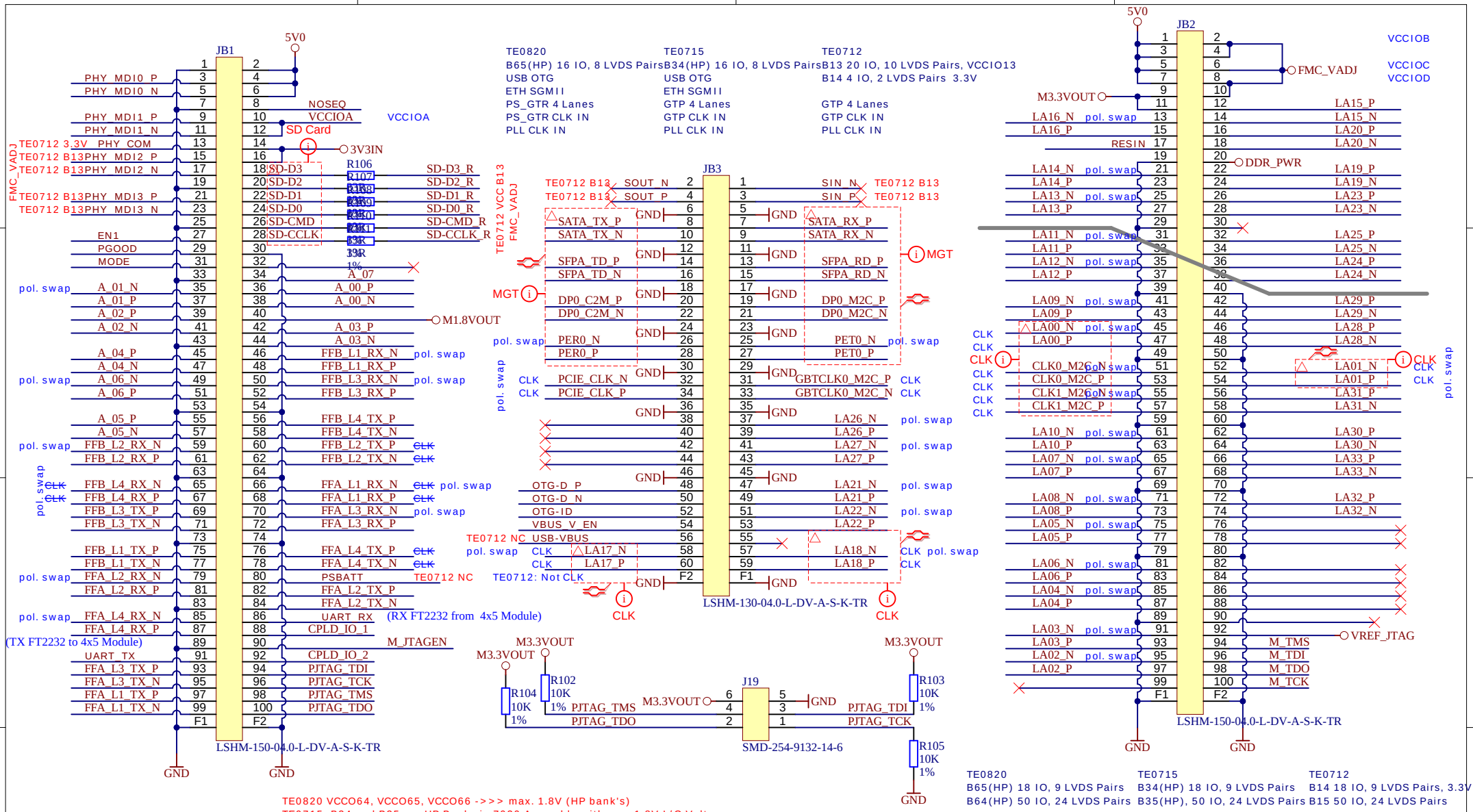
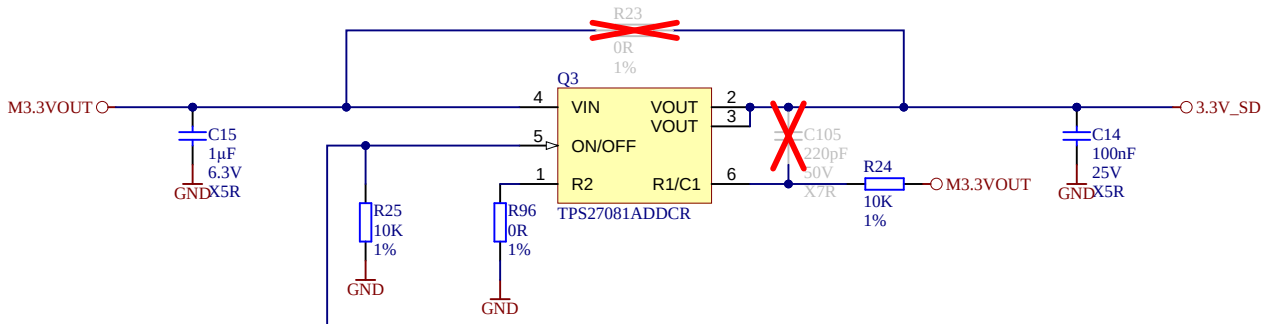
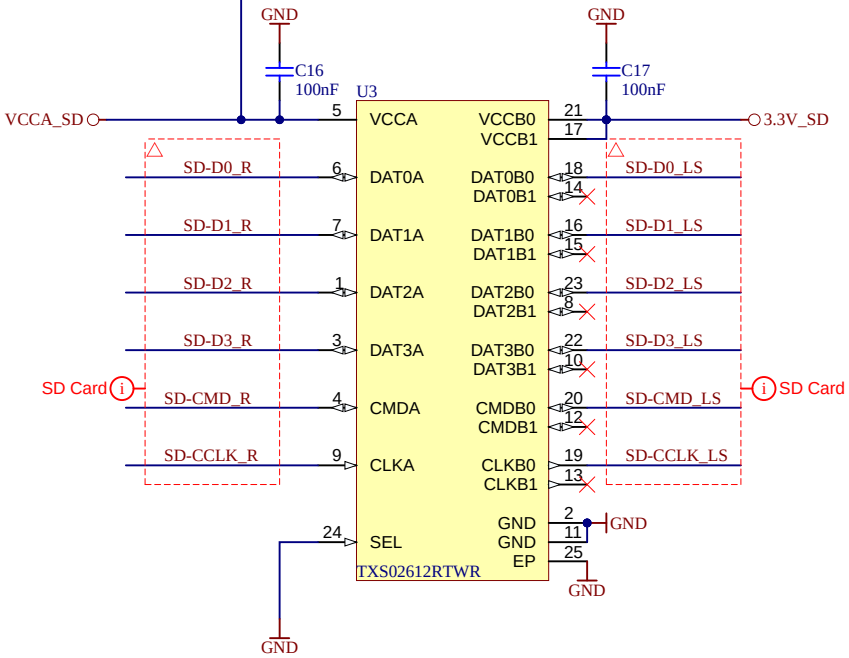
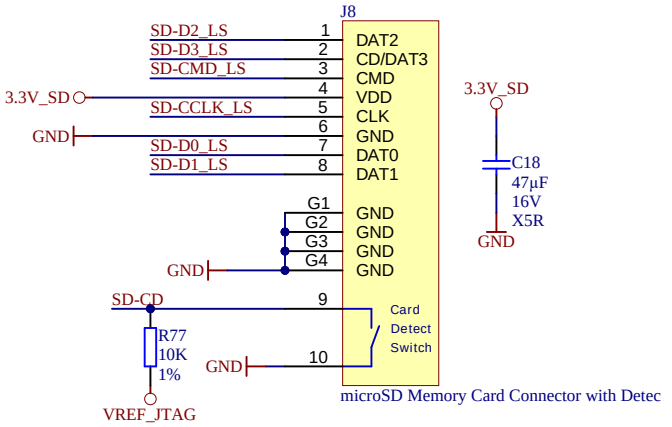
Title: TEF1002 - MAIN			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page1 of 18
Filename: TEF1002.SchDoc			



Title: TEF1002 - 4x5 Module			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page2 of 18
Filename: Module_4x5.SchDoc			







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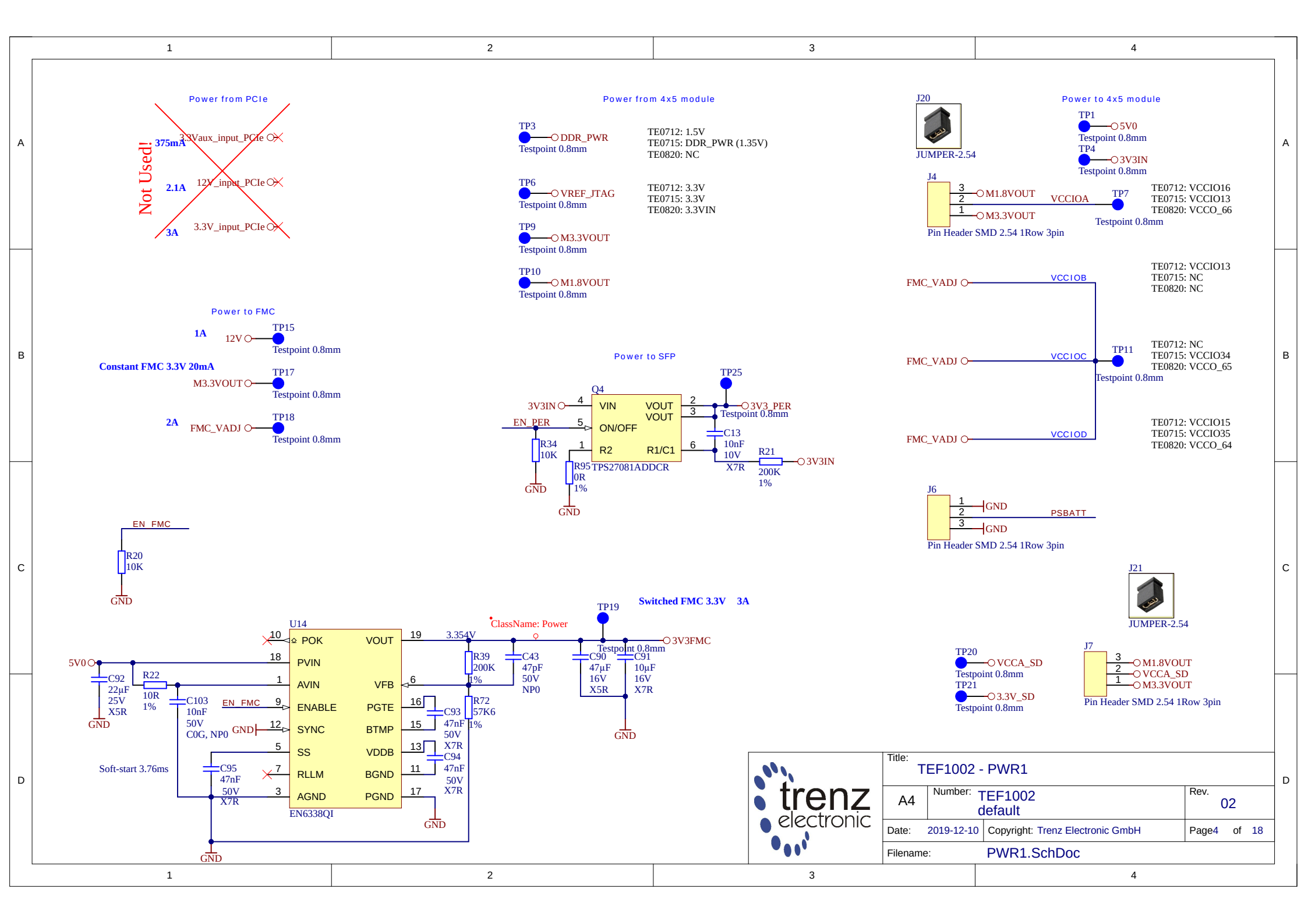
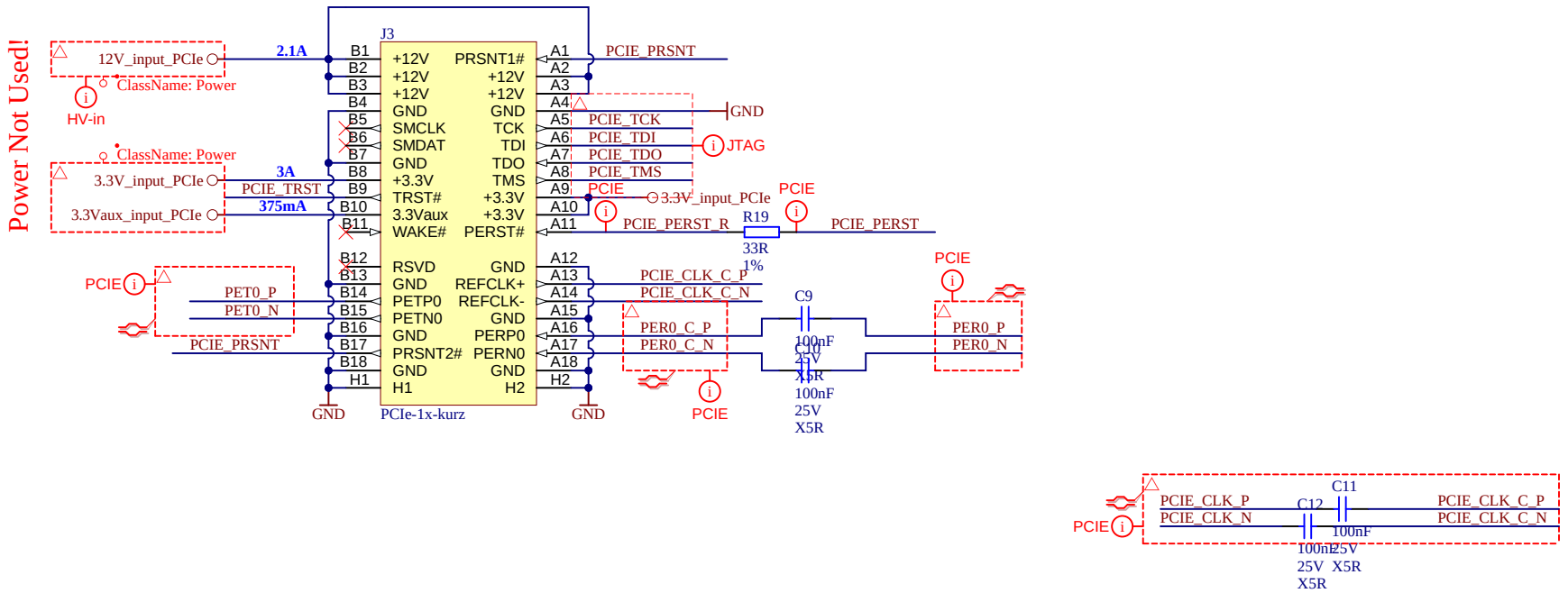
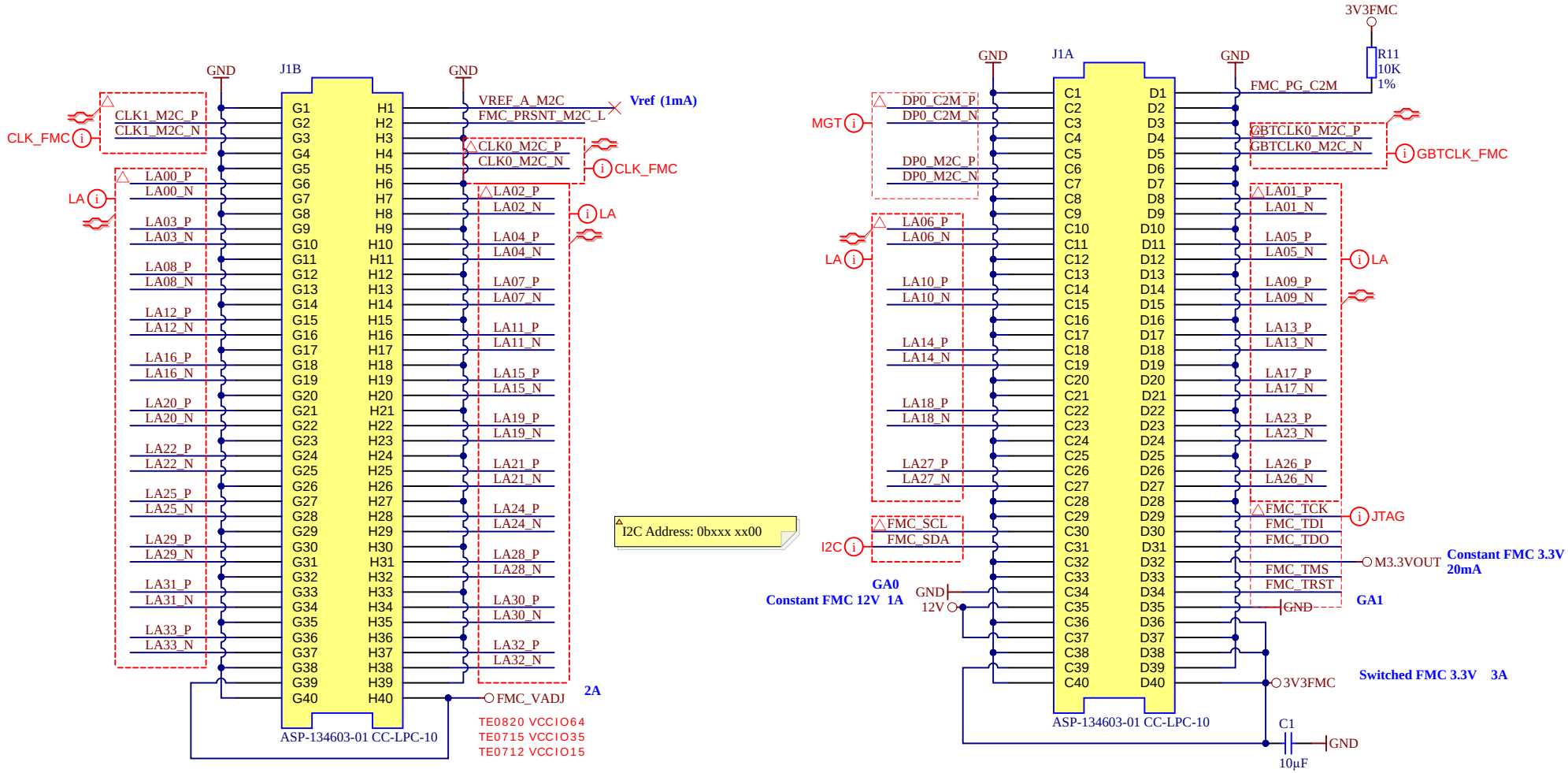
Title: TEF1002 - SD			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page3 of 18
Filename: SD.SchDoc			

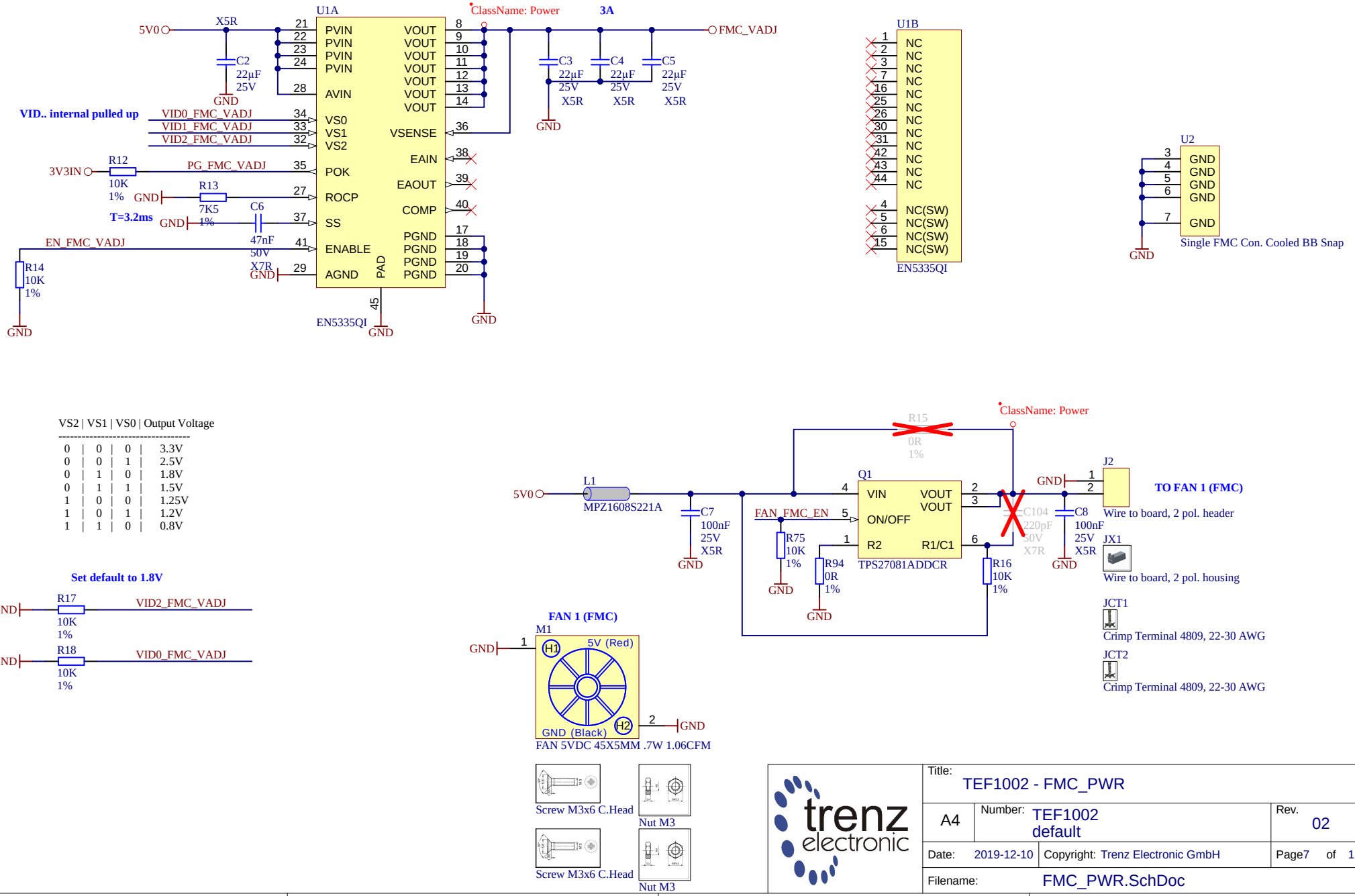

Power from PCIe
Not Used!
375mA
3.3Vaux_input_PCIe
2.1A
12V_input_PCIe
3A
3.3V_input_PCIe
Power from 4x5 module
TP3
DDR_PWR
Testpoint 0.8mm
TE0712: 1.5V
TE0715: DDR_PWR (1.35V)
TE0820: NC
TP6
VREF_JTAG
Testpoint 0.8mm
TE0712: 3.3V
TE0715: 3.3V
TE0820: 3.3VIN
TP9
M3.3VOUT
Testpoint 0.8mm
TP10
M1.8VOUT
Testpoint 0.8mm
J20
JUMPER-2.54
Power to 4x5 module
TP1
5V0
Testpoint 0.8mm
TP4
3V3IN
Testpoint 0.8mm
J4
M1.8VOUT
VCCIOA
M3.3VOUT
TP7
Testpoint 0.8mm
Pin Header SMD 2.54 1Row 3pin
TE0712: VCCIO16
TE0715: VCCIO13
TE0820: VCCO_66
Power to FMC
1A
12V
TP15
Testpoint 0.8mm
Constant FMC 3.3V 20mA
M3.3VOUT
TP17
Testpoint 0.8mm
2A
FMC_VADJ
TP18
Testpoint 0.8mm
FMC_VADJ
VCCIOB
TE0712: VCCIO13
TE0715: NC
TE0820: NC
FMC_VADJ
VCCIOC
TP11
Testpoint 0.8mm
TE0712: NC
TE0715: VCCIO34
TE0820: VCCO_65
FMC_VADJ
VCCIOD
TE0712: VCCIO15
TE0715: VCCIO35
TE0820: VCCO_64
Power to SFP
Q4
3V3IN
EN_PER
VIN
ON/OFF
R2
VOUT
VOUT
R1/C1
TPS27081ADDCR
TP25
3V3_PER
Testpoint 0.8mm
C13
10nF
10V
X7R
R21
200K
1%
3V3IN
R34
10K
R95
0R
1%
GND
J6
GND
PSBATT
GND
Pin Header SMD 2.54 1Row 3pin
EN_FMC
R20
10K
GND
Switched FMC 3.3V 3A
U14
POK
PVIN
AVIN
ENABLE
SYNC
SS
RLLM
AGND
VOUT
VFB
PGTE
BTMP
VDDB
BGND
PGND
EN6338QI
ClassName: Power
3.354V
TP19
Testpoint 0.8mm
3V3FMC
R39
200K
1%
C43
47pF
50V
NP0
C90
47µF
16V
X5R
C91
10µF
16V
X7R
R72
57K6
1%
C93
47nF
50V
X7R
C94
47nF
50V
X7R
5V0
C92
22µF
25V
X5R
R22
10R
1%
C103
10nF
50V
C0G, NP0
Soft-start 3.76ms
C95
47nF
50V
X7R
GND
J21
JUMPER-2.54
TP20
VCCA_SD
Testpoint 0.8mm
TP21
3.3V_SD
Testpoint 0.8mm
J7
M1.8VOUT
VCCA_SD
M3.3VOUT
Pin Header SMD 2.54 1Row 3pin
trenz electronic
Title: TEF1002 - PWR1
A4
Number: TEF1002 default
Rev. 02
Date: 2019-12-10
Copyright: Trenz Electronic GmbH
Page4 of 18
Filename: PWR1.SchDoc

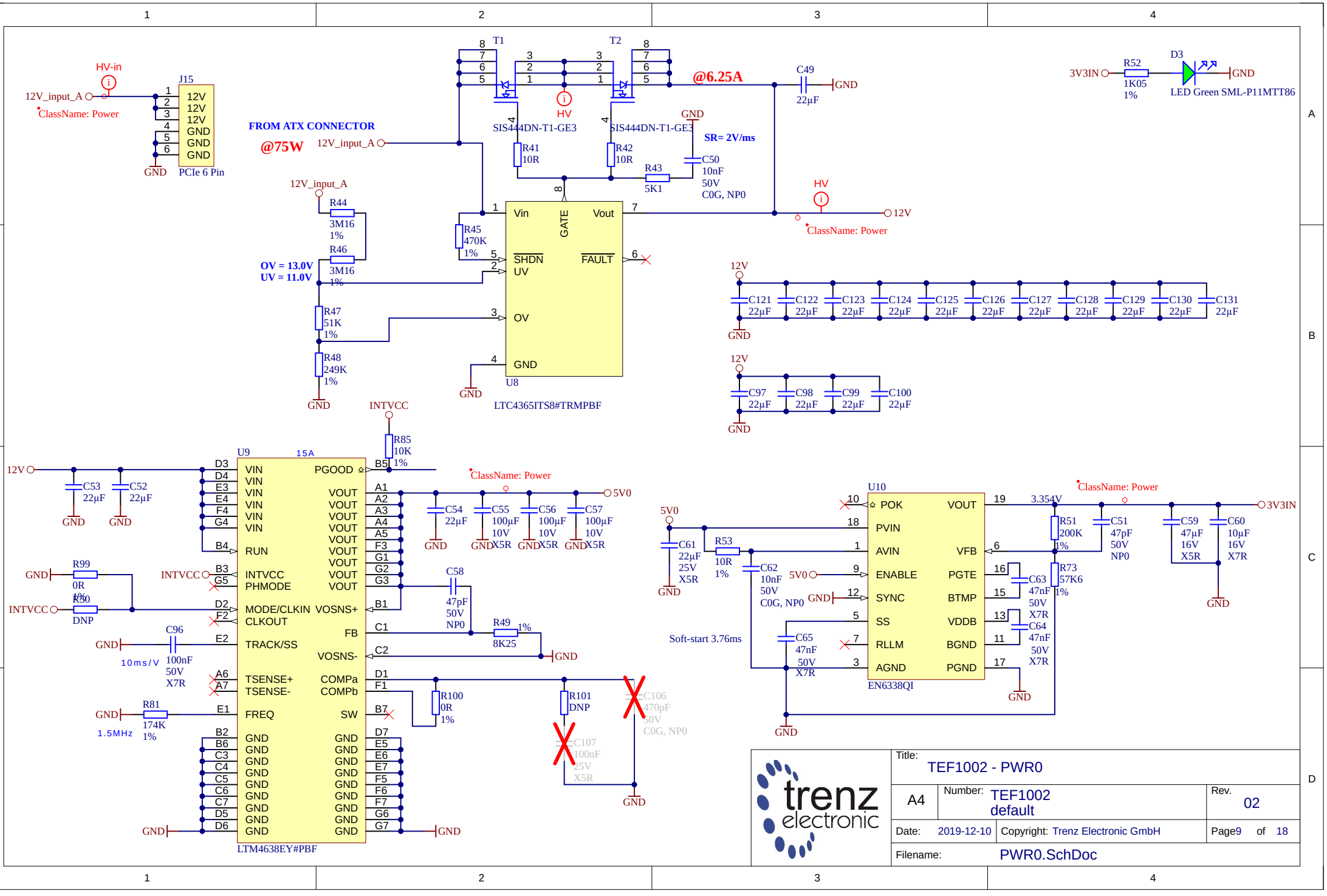


trenz electronic	Title: TEF1002 - PCIE CONNECTOR		
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page5 of 18
Filename: PCIE_CONN.SchDoc			



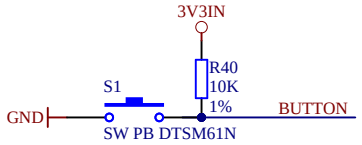
trenz electronic	Title: TEF1002 - FMC		
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page6 of 18
Filename: FMC.SchDoc			


U1A
ClassName: Power
3A
5V0
X5R
C2
22µF
25V
GND
PVIN
PVIN
PVIN
PVIN
AVIN
VOUT
VOUT
VOUT
VOUT
VOUT
VOUT
VOUT
VSENSE
EAIN
EAOUT
COMP
PGND
PGND
PGND
PGND
PAD
AGND
ENABLE
SS
ROCP
POK
VS0
VS1
VS2
FMC_VADJ
C3
C4
C5
22µF
25V
X5R
VID.. internal pulled up
VID0_FMC_VADJ
VID1_FMC_VADJ
VID2_FMC_VADJ
3V3IN
R12
10K
1%
PG_FMC_VADJ
R13
7K5
1%
C6
47nF
50V
X7R
T=3.2ms
EN_FMC_VADJ
R14
10K
1%
EN5335QI
U1B
NC
NC(SW)
EN5335QI
U2
GND
Single FMC Con. Cooled BB Snap
VS2 | VS1 | VS0 | Output Voltage
0 | 0 | 0 | 3.3V
0 | 0 | 1 | 2.5V
0 | 1 | 0 | 1.8V
0 | 1 | 1 | 1.5V
1 | 0 | 0 | 1.25V
1 | 0 | 1 | 1.2V
1 | 1 | 0 | 0.8V
Set default to 1.8V
R17
R18
10K
1%
VID2_FMC_VADJ
VID0_FMC_VADJ
ClassName: Power
R15
0R
1%
L1
MPZ1608S221A
C7
100nF
25V
X5R
Q1
VIN
VOUT
ON/OFF
R2
R1/C1
TPS27081ADDCR
FAN_FMC_EN
R75
10K
1%
R94
0R
1%
R16
10K
1%
C104
220pF
50V
X7R
C8
100nF
25V
X5R
J2
TO FAN 1 (FMC)
Wire to board, 2 pol. header
JX1
Wire to board, 2 pol. housing
JCT1
Crimp Terminal 4809, 22-30 AWG
JCT2
Crimp Terminal 4809, 22-30 AWG
FAN 1 (FMC)
M1
5V (Red)
GND (Black)
FAN 5VDC 45X5MM .7W 1.06CFM
Screw M3x6 C.Head
Nut M3
Screw M3x6 C.Head
Nut M3
trenz electronic
Title: TEF1002 - FMC_PWR
A4
Number: TEF1002 default
Rev. 02
Date: 2019-12-10
Copyright: Trenz Electronic GmbH
Page7 of 18
Filename: FMC_PWR.SchDoc

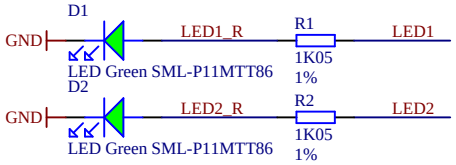

HV-in
12V_input_A
ClassName: Power
J15
12V
12V
12V
GND
GND
GND
PCIe 6 Pin
FROM ATX CONNECTOR
@75W
T1
T2
SIS444DN-T1-GE3
HV
@6.25A
C49
22µF
GND
SR= 2V/ms
R41
10R
R42
10R
R43
5K1
C50
10nF
50V
C0G, NP0
R44
3M16
1%
R46
3M16
1%
OV = 13.0V
UV = 11.0V
R47
51K
1%
R48
249K
1%
R45
470K
1%
Vin
Vout
GATE
SHDN
UV
OV
FAULT
GND
U8
LTC4365ITS8#TRMPBF
12V
ClassName: Power
C121
C122
C123
C124
C125
C126
C127
C128
C129
C130
C131
22µF
C97
C98
C99
C100
3V3IN
R52
1K05
1%
D3
LED Green SML-P11MTT86
INTVCC
R85
10K
1%
U9
15A
VIN
PGOOD
VOUT
RUN
INTVCC
PHMODE
MODE/CLKIN
CLKOUT
VOSNS+
TRACK/SS
FB
VOSNS-
TSENSE+
TSENSE-
COMPa
COMPb
FREQ
SW
GND
LTM4638EY#PBF
C53
C52
22µF
R99
0R
R50
DNP
C96
100nF
50V
X7R
10ms/V
R81
174K
1%
1.5MHz
C54
22µF
C55
100µF
10V
X5R
C56
100µF
10V
X5R
C57
100µF
10V
X5R
5V0
C58
47pF
50V
NP0
R49
8K25
1%
R100
0R
1%
R101
DNP
C106
470pF
50V
C0G, NP0
C107
100nF
25V
X5R
U10
POK
PVIN
AVIN
ENABLE
SYNC
SS
RLLM
AGND
VOUT
VFB
PGTE
BTMP
VDDB
BGND
PGND
EN6338QI
3.354V
C61
22µF
25V
X5R
R53
10R
1%
C62
10nF
50V
C0G, NP0
Soft-start 3.76ms
C65
47nF
50V
X7R
R51
200K
1%
C51
47pF
50V
NP0
C59
47nF
16V
X5R
C60
10µF
16V
X7R
R73
57K6
1%
C63
47nF
50V
X7R
C64
47nF
50V
X7R
trenz
electronic
Title:
TEF1002 - PWR0
A4
Number:
TEF1002
default
Rev.
02
Date:
2019-12-10
Copyright:
Trenz Electronic GmbH
Page9
of
18
Filename:
PWR0.SchDoc

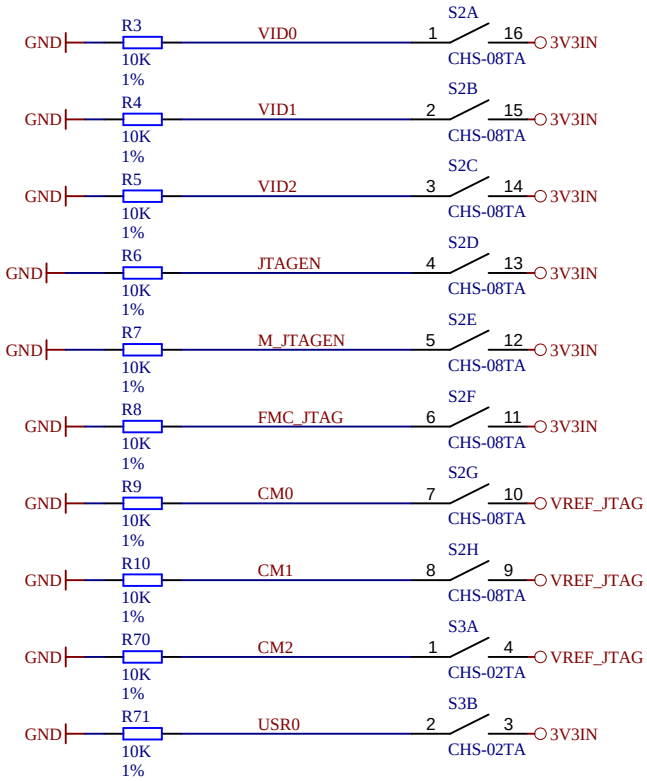
FPGA
FPGA.SchDoc

FPGA_MISC
FPGA_MISC.SchDoc



to CPLD e.g. for Control Module: nRST





to CPLD e.g. for Control Module: EN1

to CPLD e.g. for Control Module: NOSEQ

to CPLD e.g. for Control Module: BOOTMODE

VS2	VS1	VS0	Output Voltage
0	0	0	3.3V
0	0	1	2.5V
0	1	0	1.8V
0	1	1	1.5V
1	0	0	1.25V
1	0	1	1.2V
1	1	0	0.8V

JTAG access with standard CPLD Firmware

JTAGEN	M_JTAGEN	FMC_JTAG	Device	Port
ON	X	X	CPLD MAX 10	J5
OFF	ON	OFF	4x5 SoM CPLD	J10
OFF	OFF	OFF	4x5 SoM	J10
OFF	X	ON	FMC	J10

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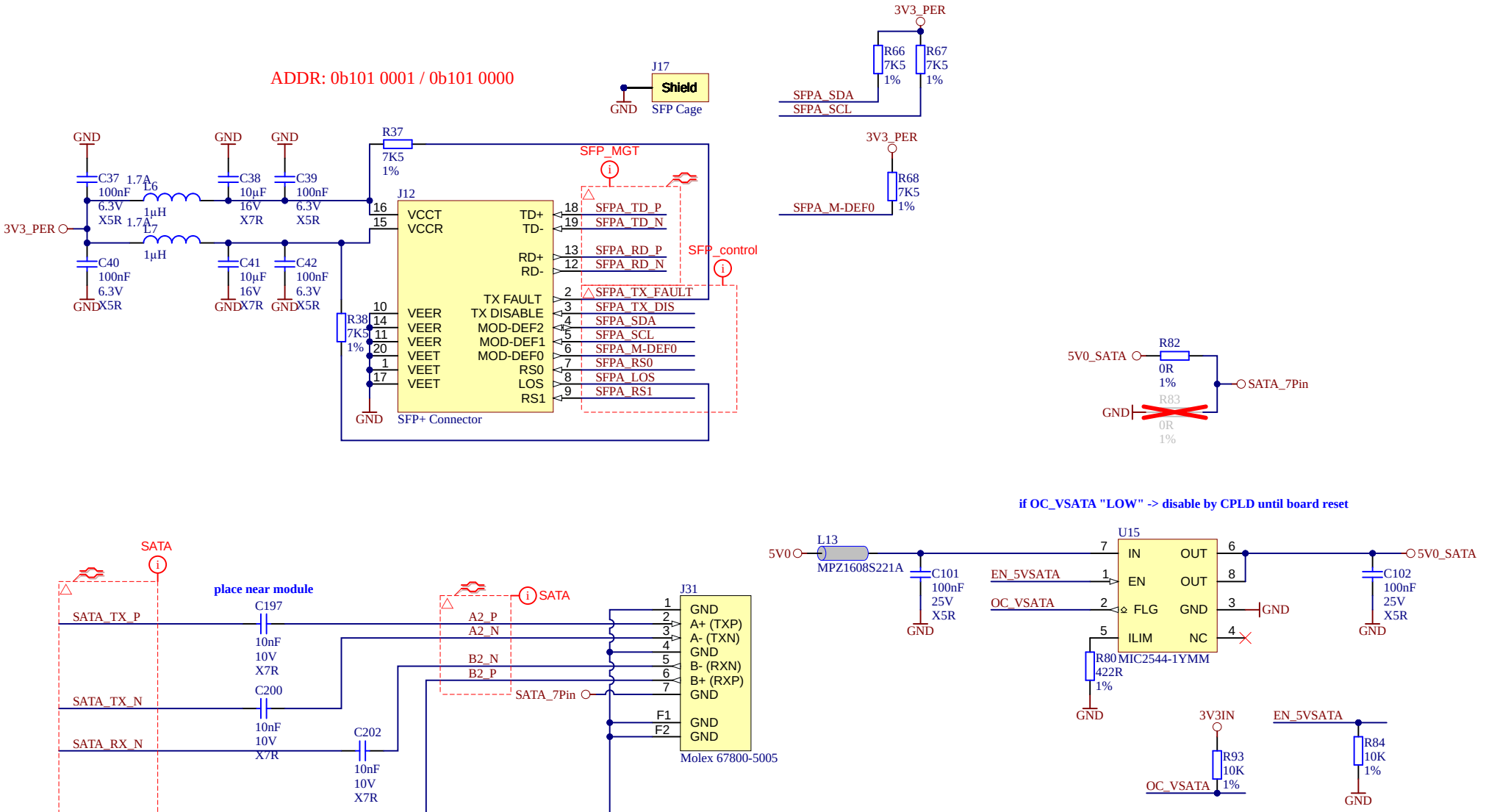
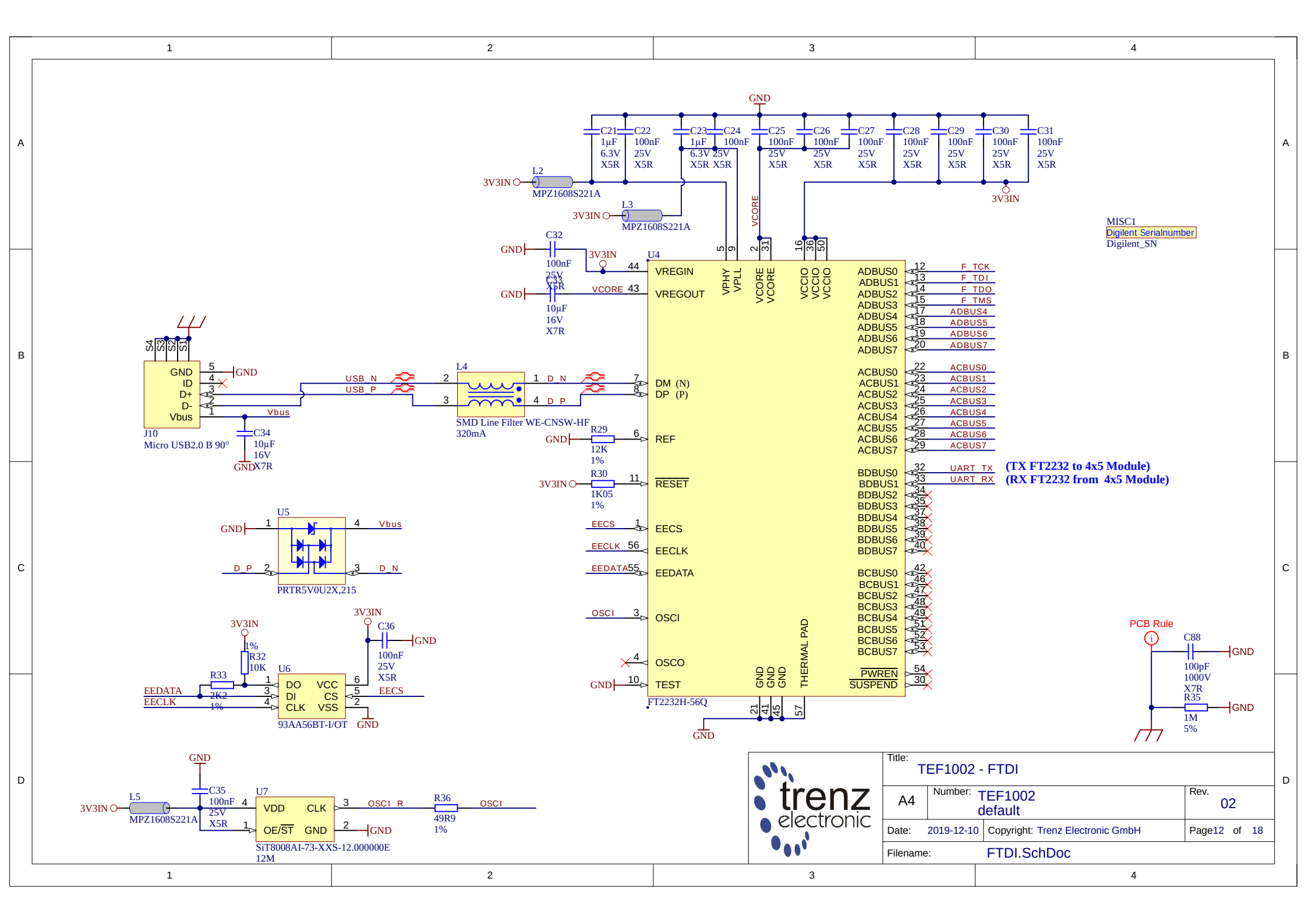
Title: TEF1002 - CPLD		
A4	Number: TEF1002 default	Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH	Page10 of 18
Filename: CPLD.SchDoc		



Title: TEF1002 - SFP,SATA		
A4	Number: TEF1002 default	Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH	Page11 of 18
Filename: SFP_SATA.SchDoc		


GND
C21 1µF 6.3V X5R
C22 100nF 25V X5R
C23 1µF 6.3V X5R
C24 100nF 25V X5R
C25 100nF 25V X5R
C26 100nF 25V X5R
C27 100nF 25V X5R
C28 100nF 25V X5R
C29 100nF 25V X5R
C30 100nF 25V X5R
C31 100nF 25V X5R
3V3IN
L2
MPZ1608S221A
L3
MPZ1608S221A
VCORE
C32 100nF 25V X5R
C33 10µF 16V X7R
U4
VREGIN
VREGOUT
VPHY
VPLL
VCORE
VCCIO
THERMAL PAD
DM (N)
DP (P)
REF
RESET
EECS
EECLK
EEDATA
OSCI
OSCO
TEST
ADBUS0
ADBUS1
ADBUS2
ADBUS3
ADBUS4
ADBUS5
ADBUS6
ADBUS7
ACBUS0
ACBUS1
ACBUS2
ACBUS3
ACBUS4
ACBUS5
ACBUS6
ACBUS7
BDBUS0
BDBUS1
BDBUS2
BDBUS3
BDBUS4
BDBUS5
BDBUS6
BDBUS7
BCBUS0
BCBUS1
BCBUS2
BCBUS3
BCBUS4
BCBUS5
BCBUS6
BCBUS7
PWREN
SUSPEND
F_TCK
F_TDI
F_TDO
F_TMS
UART_TX
UART_RX
FT2232H-56Q
MISC1
Digilent Serialnumber
Digilent_SN
(TX FT2232 to 4x5 Module)
(RX FT2232 from 4x5 Module)
J10
Micro USB2.0 B 90°
S4
S3
S2
S1
GND
ID
D+
D-
Vbus
USB_N
USB_P
L4
SMD Line Filter WE-CNSW-HF
320mA
D_N
D_P
C34 10µF 16V X7R
R29 12K 1%
R30 1K05 1%
U5
PRTR5V0U2X,215
R32 10K 1%
R33 2K2 1%
U6
DO
DI
CLK
CS
VSS
VCC
93AA56BT-I/OT
C36 100nF 25V X5R
EEDATA
EECLK
EECS
L5
MPZ1608S221A
C35 100nF 25V X5R
U7
VDD
OE/ST
CLK
GND
SiT8008AI-73-XXS-12.000000E
12M
OSCI_R
R36 49R9 1%
PCB Rule
C88 100pF 1000V X7R
R35 1M 5%
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Title: TEF1002 - FTDI
A4
Number: TEF1002 default
Rev. 02
Date: 2019-12-10
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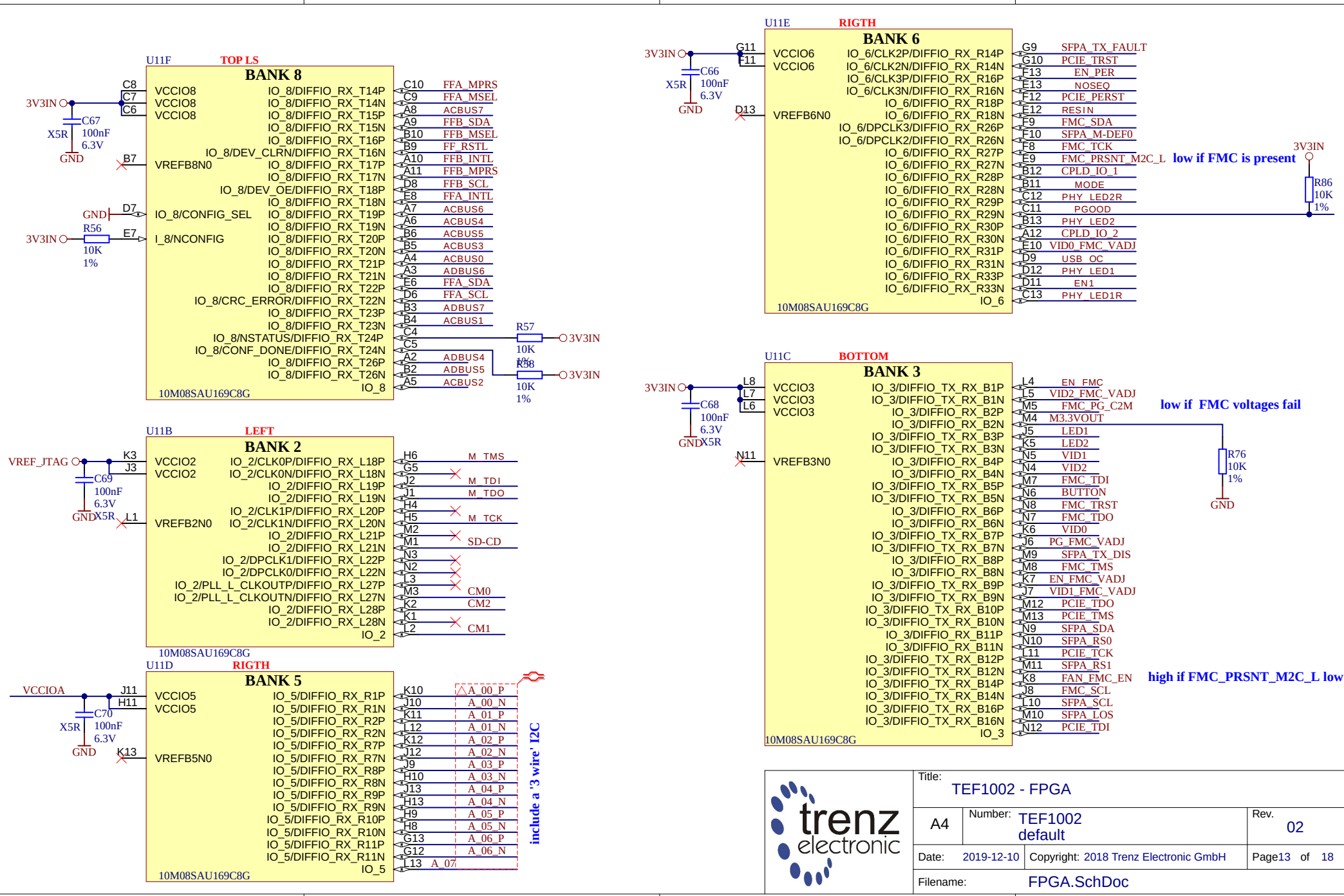
Filename: FTDI.SchDoc


U11F
TOP LS
BANK 8
VCCIO8
VCCIO8
VCCIO8
VREFB8N0
IO_8/CONFIG_SEL
I_8/NCONFIG
IO_8/DEV_CLRN/DIFFIO_RX_T16N
IO_8/DEV_OE/DIFFIO_RX_T18P
IO_8/CRC_ERROR/DIFFIO_RX_T22N
IO_8/NSTATUS/DIFFIO_RX_T24P
IO_8/CONF_DONE/DIFFIO_RX_T24N
IO_8
10M08SAU169C8G
FFA_MPRS
FFA_MSEL
ACBUS7
FFB_SDA
FFB_MSEL
FF_RSTL
FFB_INTL
FFB_MPRS
FFB_SCL
FFA_INTL
ACBUS6
ACBUS4
ACBUS5
ACBUS3
ACBUS0
ADBUS6
FFA_SDA
FFA_SCL
ADBUS7
ACBUS1
ADBUS4
ADBUS5
ACBUS2
3V3IN
C67
X5R
100nF
6.3V
GND
R56
10K
1%
R57
R58
U11B
LEFT
BANK 2
VCCIO2
VCCIO2
VREFB2N0
IO_2
10M08SAU169C8G
VREF_JTAG
C69
M_TMS
M_TDI
M_TDO
M_TCK
SD-CD
CM0
CM2
CM1
U11D
RIGTH
BANK 5
VCCIO5
VCCIO5
VREFB5N0
IO_5
10M08SAU169C8G
VCCIOA
C70
A_00_P
A_00_N
A_01_P
A_01_N
A_02_P
A_02_N
A_03_P
A_03_N
A_04_P
A_04_N
A_05_P
A_05_N
A_06_P
A_06_N
A_07
include a '3 wire' I2C
U11E
RIGTH
BANK 6
VCCIO6
VCCIO6
VREFB6N0
IO_6
10M08SAU169C8G
C66
D13
SFPA_TX_FAULT
PCIE_TRST
EN_PER
NOSEQ
PCIE_PERST
RESIN
FMC_SDA
SFPA_M-DEF0
FMC_TCK
FMC_PRSNT_M2C_L
low if FMC is present
CPLD_IO_1
MODE
PHY_LED2R
PGOOD
PHY_LED2
CPLD_IO_2
VID0_FMC_VADJ
USB_OC
PHY_LED1
EN1
PHY_LED1R
R86
U11C
BOTTOM
BANK 3
VCCIO3
VCCIO3
VCCIO3
VREFB3N0
IO_3
10M08SAU169C8G
C68
N11
EN_FMC
VID2_FMC_VADJ
FMC_PG_C2M
low if FMC voltages fail
M3.3VOUT
LED1
LED2
VID1
VID2
FMC_TDI
BUTTON
FMC_TRST
FMC_TDO
VID0
PG_FMC_VADJ
SFPA_TX_DIS
FMC_TMS
EN_FMC_VADJ
VID1_FMC_VADJ
PCIE_TDO
PCIE_TMS
SFPA_SDA
SFPA_RS0
PCIE_TCK
SFPA_RS1
FAN_FMC_EN
high if FMC_PRSNT_M2C_L low
FMC_SCL
SFPA_SCL
SFPA_LOS
PCIE_TDI
R76
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Title:
TEF1002 - FPGA
A4
Number:
TEF1002
default
Rev.
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Date:
2019-12-10
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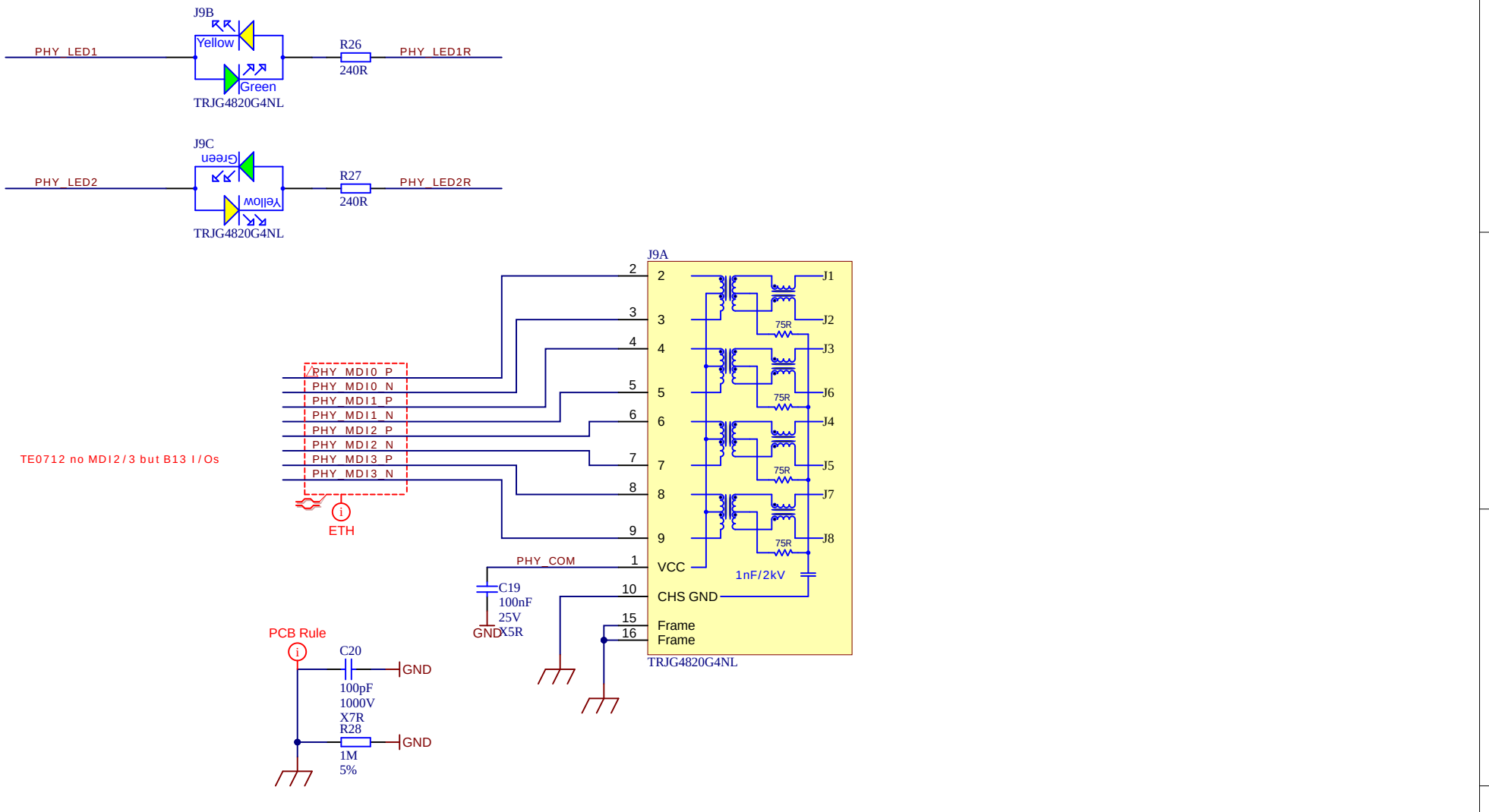
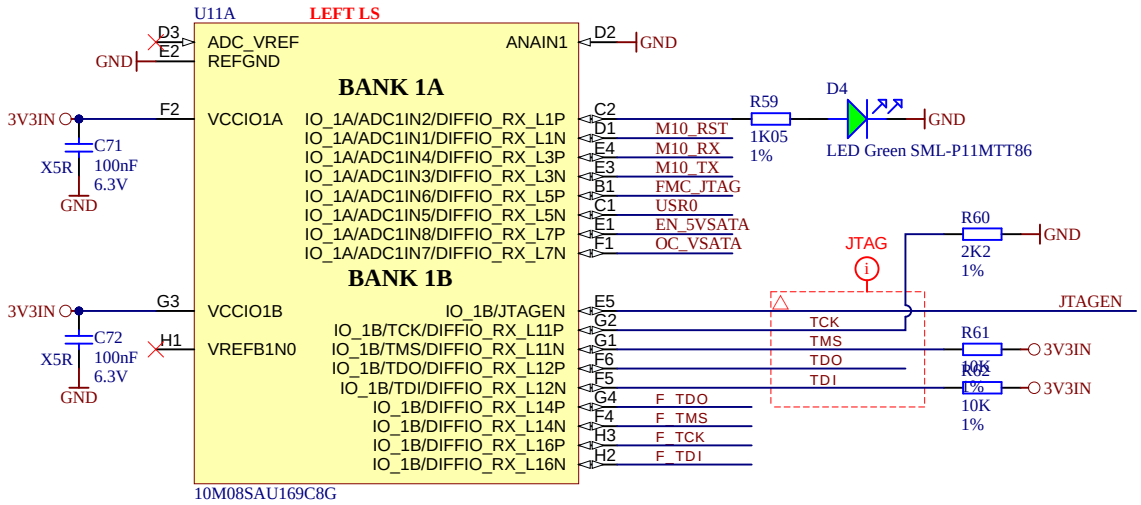
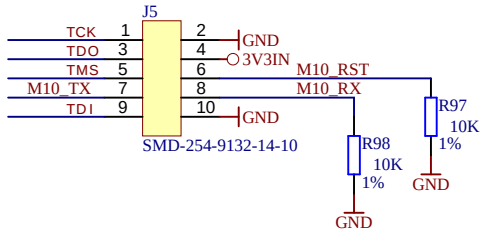
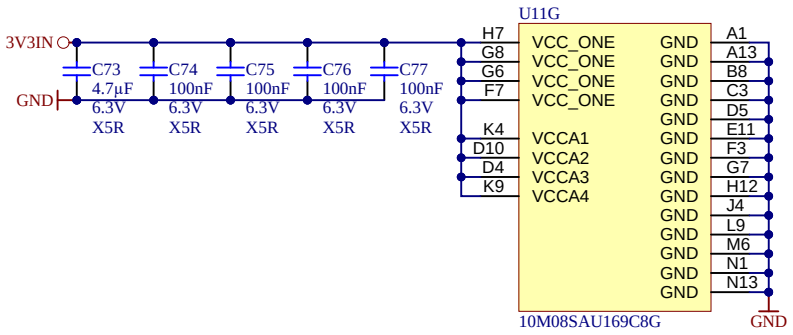
Filename:
FPGA.SchDoc



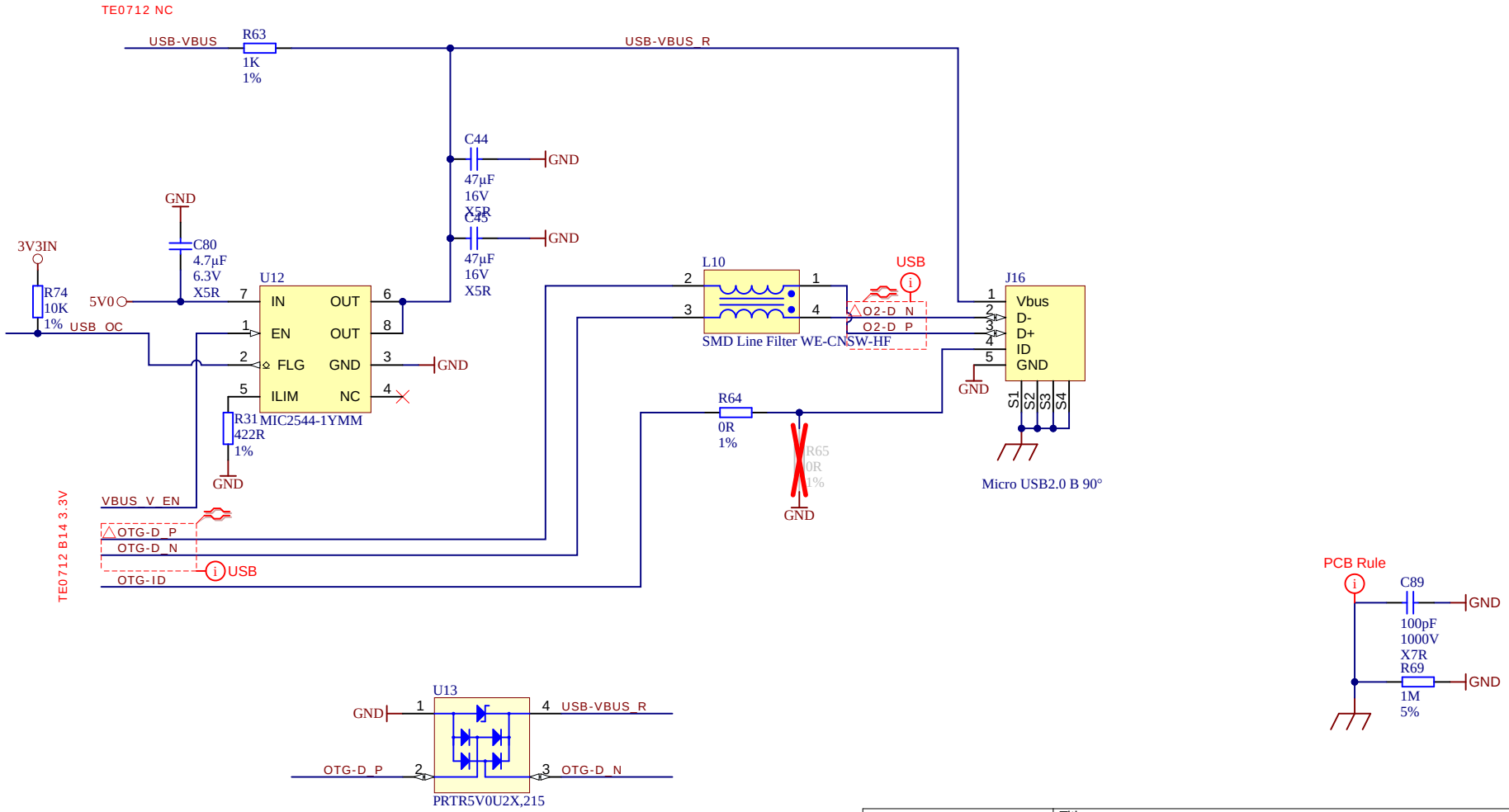
trenz electronic	Title: TEF1002 - Ethernet		
	A4	Number: TEF1002 default	Rev. 02
	Date: 2019-12-10	Copyright: Trenz Electronic GmbH	Page13 of 18
	Filename: ETHERNET.SchDoc		



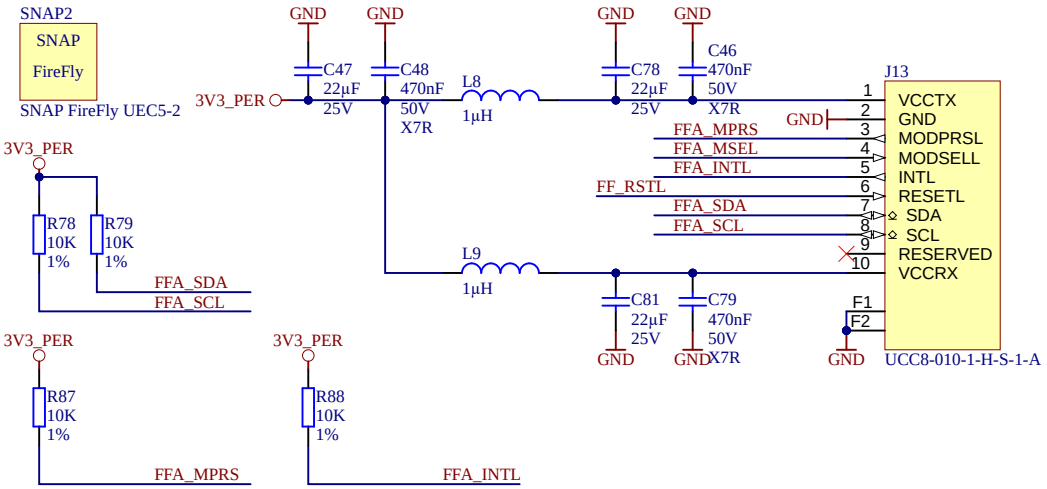


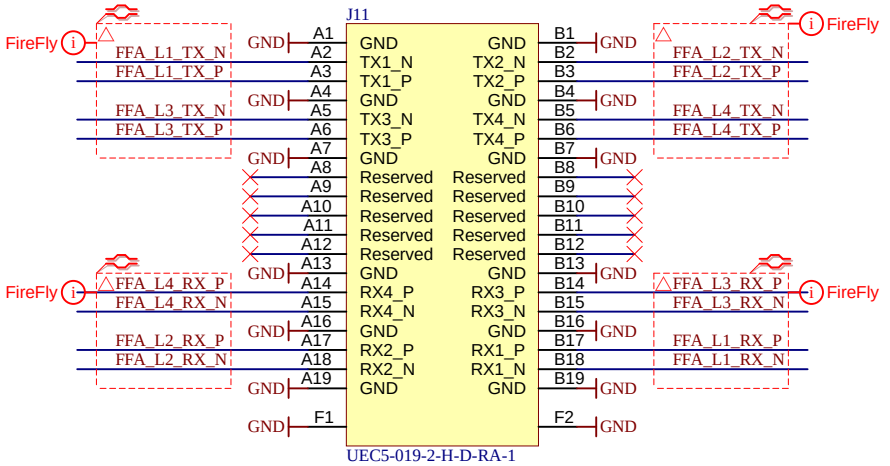


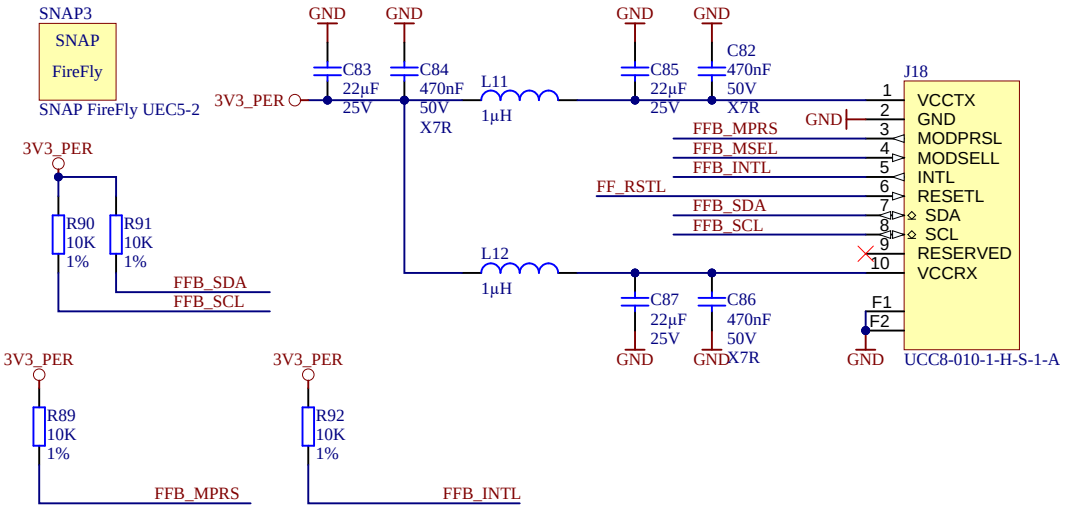
Title: TEF1002 - FPGA MISC			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: 2018 Trenz Electronic GmbH		Page14 of 18
Filename: FPGA_MISC.SchDoc			

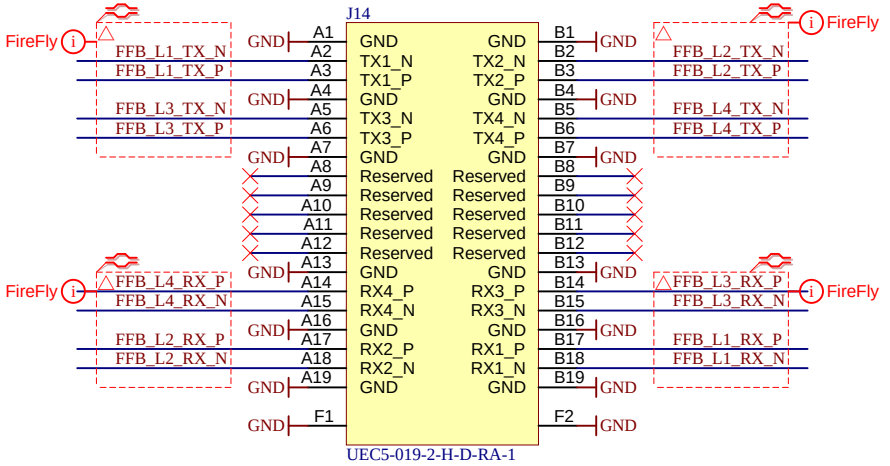


Title: TEF1002 - USB			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page15 of 18
Filename: USB.SchDoc			









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Title: TEF1002 - FireFly			
A4	Number: TEF1002 default		Rev. 02
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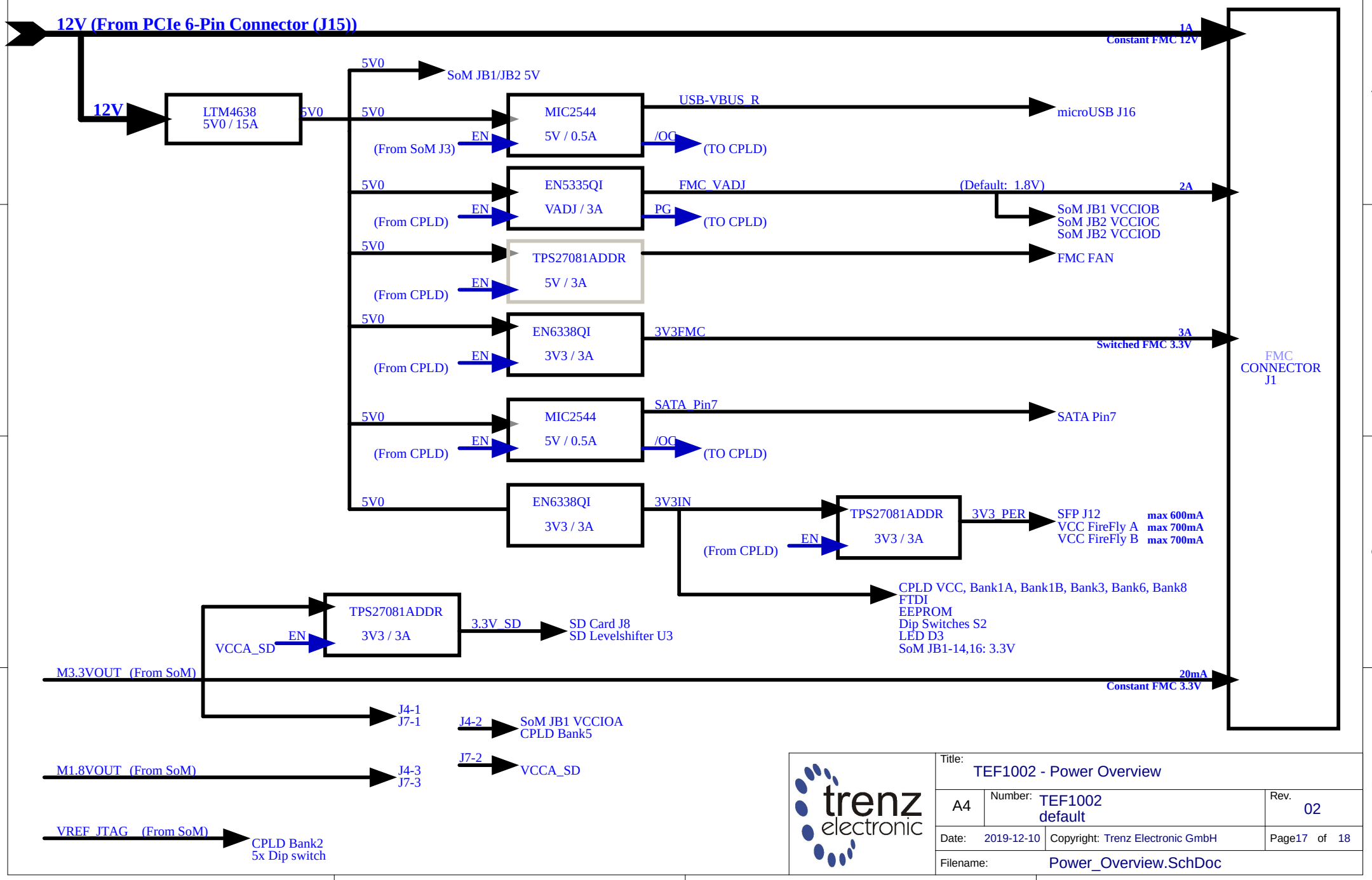
Filename: FireFly.SchDoc			



Title: TEF1002 - Power Overview			
A4	Number: TEF1002 default		Rev. 02
Date: 2019-12-10	Copyright: Trenz Electronic GmbH		Page17 of 18
Filename: Power_Overview.SchDoc			

REV01: Initial Revision

REV02:

Replace SD-Card socket by a push/pull version, Added card detect on CPLD. Added series resistors.
Replaced PJTAG header J19 by 2x3 pin header and removed 0Ohm series resistors.
Added pulldown on M3.3OUT R76 and FMC_FAN_EN R75
Replaced J6 with 3pin header (GND, PSBATT, GND)
Changed GTR lanes SATA<->PCIe (compability for TE0820)
Removed TP 22 23 24, and replaced J5 by header for TEI0004
J5 JTAG directly connected to CPLD. FTDI JTAG moved to other pins.
Inverted dips for JTAGEN and M_JTAG
Moved FMC and SFP
Moved FMC_JTAG and USR dip switches to other Bank
Changed USB power switch
Added SATA power switch with enable and overcurrent on CPLD for 7pin power configuration
Reworked 5V0 and 3V3IN power supply
Added optional R and C for slew rate adjustment of powerswitches Q1, Q3, Q4
(04.05.2022)
Set S/N track-it pad not fitted (EOL)

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Title: TEF1002 - Revision Changes		
A4	Number: TEF1002 default	Rev. 02
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Filename: Revision_Changes.SchDoc		