A New Gate Driver Integrated Circuit for IGBT Devices With Advanced Protections

Laurent Dulau, Serge Pontarollo, Anthony Boimond, Jean-François Garnier, Nicole Giraudo, and Olivier Terrasse

***Abstract*—The aim of this paper is to discuss new solutions in the design of insulated gate bipolar transistor (IGBT) gate drivers with advanced protections such as two-level turn-on to reduce peak current when turning on the device, two-level turn-off to limit over-voltage when the device is turned off, and an active Miller clamp function that acts against cross conduction phenomena. Afterwards, we describe a new circuit which includes a two-level turn-off driver and an active Miller clamp function. Tests and results for these advanced functions are discussed, with particular emphasis on the influence of an intermediate level in a two-level turn-off driver on overshoot across the IGBT.**

***Index Terms*—Active Miller clamp, bipolar CMOS DMOS (BCD), cross conduction, insulated gate bipolar transistor (IGBT), overshoot, peak current, two-level driver.**

I. Introduction

INSULATED gate bipolar transistor (IGBT) [1] devices play a large role in power applications due to their high current, voltage capability, and ease of driving. The majority of industrial applications commonly use a three-phase inverter with a 1200-V IGBT. Driving these devices in medium or large power applications requires separate, floating, high-, and low-side drivers with galvanic insulation. Control and protection functions are also required to ensure reliable operation [2]. The challenge in gate driver design is to find solutions to the dilemma between the requirement to minimize switching losses and the requirement to limit di/dt (IGBT collector current slope), dv/dt (IGBT collector voltage slope), peak reverse recovery current at turn-on, and voltage overshoot at turn-off [3]. This paper highlights the essential requirements of the gate driver circuits for safe switching of the IGBT.

We propose several new features available using bipolar CMOS DMOS (BCD) [4] technology. These features are: an output driver with a two-level turn-on, in order to reduce peak reverse recovery current; an output driver with two-level turn-off for limiting overshoot; and an active Miller clamp function that allows the use of simpler power supply systems, and in most cases, avoids having to use a negative gate drive to prevent occurring cross conduction [5]. Afterwards, we will describe a new integrated circuit that includes, in a single chip, a two-level turn-off output driver, an active Miller clamp function, a desaturation protection [6], [7] and the possibility to use a negative off-state control voltage. Then we will discuss tests and results for this integrated circuit.

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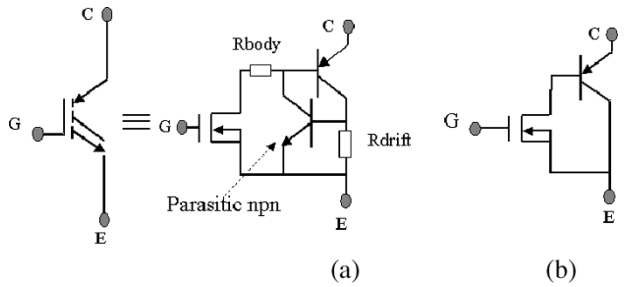

Fig. 1. IGBT equivalent circuit.

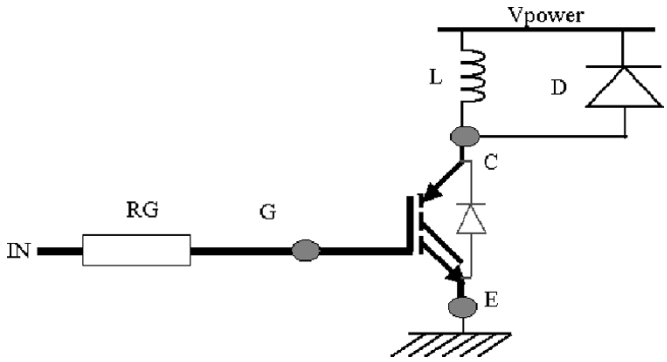

Fig. 2. Inductive load schematic for transient analysis.

II. IGBT Switching Analysis

A. Introduction

An IGBT combines the advantages of a bipolar transistor and a metal-oxide semiconductor field-effect transistor (MOSFET) [8]. As a first approximation, the IGBT can be modeled as a PNP transistor driven by an n-channel power MOSFET [Fig. 1(b)]. This model is very simple and does not take into account the negative effects on latch-up due to the parasitic NPN transistor [Fig. 1(a)]. But this approach is useful to explain the principal characteristics of the IGBT. Turn-on and turn-off can be analyzed in the simple way by using a typical schematic (Fig. 2) including a free-wheeling diode and a resistor on the gate. IGBT only requires power for turn-on and turn-off stages. A positive gate current ($I_{\rm G} > 0$) is necessary to charge at turn-on the IGBT input capacitance to create an electron channel. Once switched on, the IGBT needs no extra power ($I_{\rm G} = 0$) to keep this channel. In the same way at turn-off, a negative gate current ($I_{\rm G} < 0$) discharges the IGBT input capacitance for removing the electron channel.

B. Turn-On Analysis

The IGBT turn-on stage (a positive step voltage is applied on the input IN), shown in Fig. 3(a), is very similar to a power MOSFET turn-on stage.

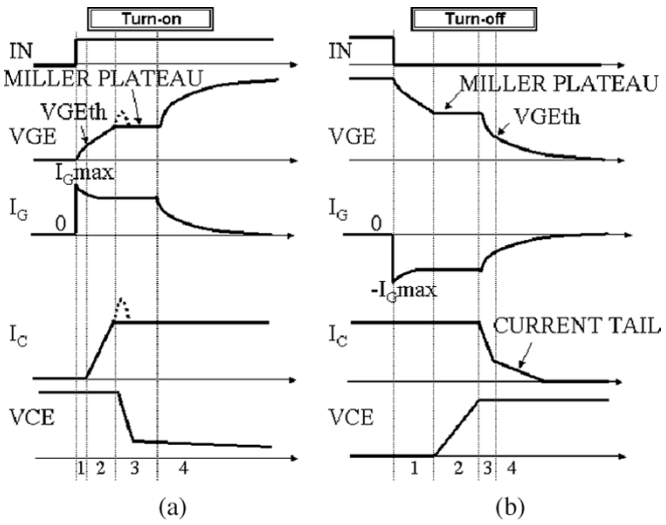

Fig. 3. IGBT turn-on and turn-off.

1) The first interval corresponds to the time delay required to bring the gate voltage (VGE) from zero to its VGEth threshold. Both the voltage across the switching device (VCE) and the current $(I_{\rm C})$ through it are unaffected during this delay time.
2) The second period starts when the gate voltage has reached the VGEth threshold and the collector current begins to increase.
3) During the third period, known as Miller plateau, the input capacitance of the IGBT appears to be infinite. The collector voltage begins to fall rapidly, while the IGBT is carrying maximum current. Most of the drive current from the driver is used to discharge the Miller capacitance CGC. If one considers the diode (D) as nonideal, then due to the reverse recovery, you will see a hump on the VGE curve, as well as in that of the $I_{\rm C}$ collector current [3].
4) After this period, the VGE continues to increase exponentially to its final value, which determines the $R_{\rm on}$ of the IGBT. At the same time, the VCE attains its lowest value.

C. Turn-Off Description

The IGBT turn-off stage (a negative step voltage is applied on the input IN), shown in Fig. 3(b), can be divided into four phases.

1) During the first phase, the gate voltage, with a constant $I_{\rm C}$ current, begins to decrease until it reaches the value when the Miller effect occurs.
2) In the second phase, due to the Miller effect, the gate voltage remains constant because of the modulation of the collector gate capacitance. The collector voltage is increased to its maximum value.
3) After, in the third phase, the collector current begins to fall quickly.
4) Finally, when the gate voltage is equal to the VGEth threshold, the input MOSFET switches off and the collector current continues to decrease with the tail current that is due to the recombination of minority carriers in the substrate. The tail current, which causes the major part of the switching losses [3], cannot be reduced by the driving circuit.

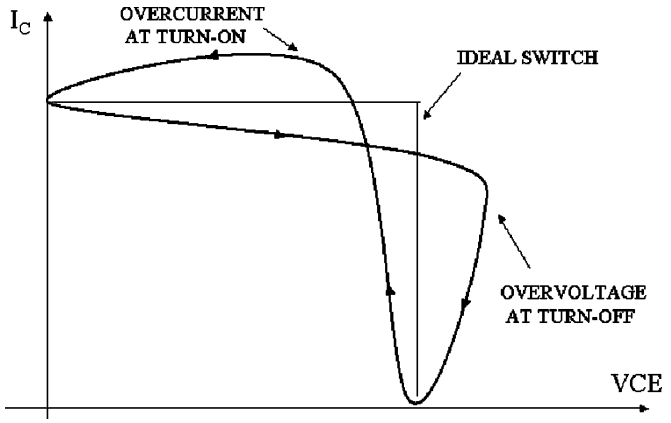

Fig. 4. IGBT operating area.

D. Real Operating Area

The operating point can go outside of the safe operating area (Fig. 4) [9], [10] under fast switching slope as dv/dt or di/dt [3] due to stray inductances and parasitic capacitors.

Our main goal in the next section is to propose new solutions to protect the IGBT during these abnormal operation conditions.

III. Advanced Protection and Driving Control for IGBT

A. Reduction of Over-Current at Turn-On

The gate resistor (RG) controls the IGBT collector current slope [8]. The choice of this resistor is based on a compromise between reduced power consumption (which requires a low value of RG) and a tolerable dv/dt or di/dt in order to limit the peak current due to the recovery diode and the electromagnetic interference (EMI) [11] generation requiring a high value of RG. The latching current depends upon the gate resistance value. The manufacturers guarantee a minimum gate resistance value to avoid the latching phenomenon. IGBT drivers are generally implemented using two resistors: one resistor is employed at turn-on and the other one for turn-off. Advanced methods are proposed to limit di/dt and dv/dt based on the feedback control of the IGBT collector current or the collector voltage slope [2], [9], [12]–[14]. However, it is not easy to achieve these complex methods, which require considerable silicon area.

In order to protect the IGBT from over-current, risk of latch-up and to limit the EMI, without incurring any increase in the values of gate resistance and the power consumption, the gate voltage must be increased in two separate stages [15]–[17]. By increasing the gate to an intermediate stage for a short time before the final turn-on, the IGBT collector current and its slope di/dt are limited. Hence, the peak current due to the diode reverse recovery is reduced. A two-level turn-on driver can be implemented as seen in Fig. 5 [18]. The low-side driver is an N-channel DMOS. In BCD, the high-voltage P-channel MOSFET takes up a lot of area due to the mobility, $\mu_{\rm p}$, which is superior to $\mu_{\rm n}$, and a minimum length that is much longer than for the N-channel DMOS. Because of these considerations, we

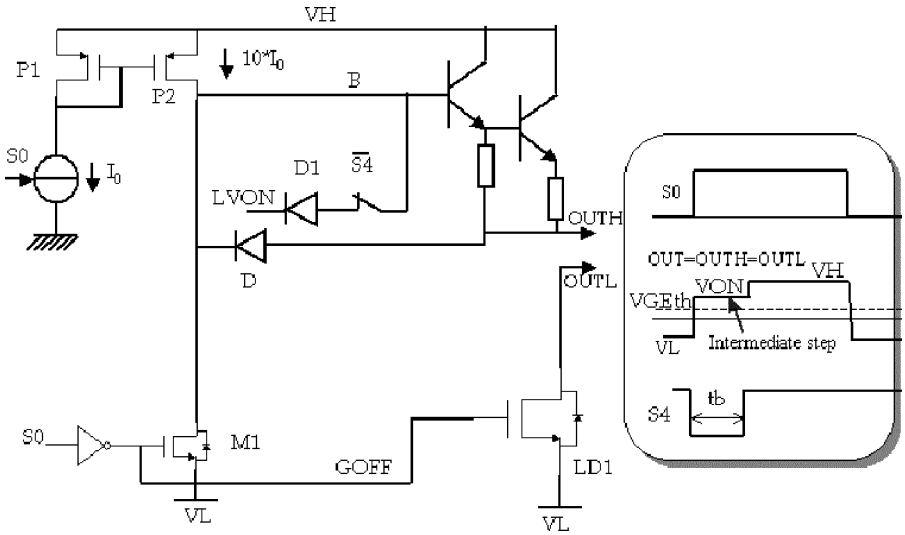

Fig. 5. Two-level turn-on driver [18].

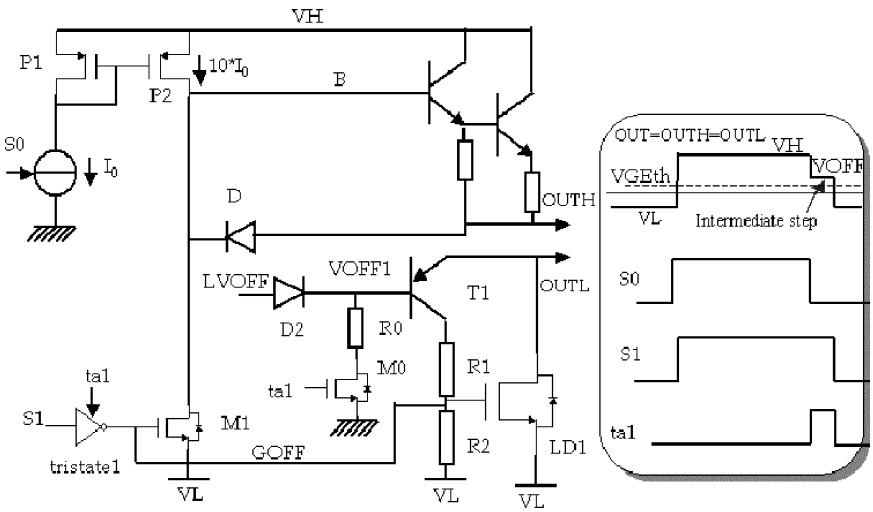

Fig. 6. Two-level turn-off driver [18].

chose to use a NPN Darlington architecture for the high-side driver, controlled by a current source. A voltage reference, VON, is applied to the LVON input in order to create an intermediate level during the turn-on stage. Before the turn-on stage, LD1 and M1 are on and OUTH $=$ OUTL $=$ VL. To begin the turn-on stage, we open M1 and LD1 and switch on S4. Furthermore, we put the current source I_0 on with S0.

The Darlington drives a big current. The output potential will increase as the output current charges the output capacitor. When the potential at point B reaches VON$+$VD1 (where VD1 is threshold of the diode D1), D1 becomes on. Then, the input current of the Darlington $(I_{\rm B})$, which is equal to $10\times I_0$, flows to the pin LVON via S4 and D1. The Darlington is no longer controlled by $I_{\rm B}$ and is not able to provide the output current. The potential of the output stays at a level near VON throughout the duration of the period Tb. After this period has elapsed, S4 is switched off and the Darlington is again controlled by $I_{\rm B}$. The output curve finishes its slope and the output potential finally reaches its maximum value equal to about VH-2 V.

To turn off the IGBT, we only have to turn off the current source I_0 and close switches LD1 and M1.

So with this schematic, users can adjust the intermediate level at the output by placing a potential (using a Zener diode, for example) on the LVON pin, with a value above all of the IGBT thresholds.

B. Reduction of Over-Voltage at Turn-Off

If there is a short-circuit or over-current in the load, a large voltage overshoot can occur across the IGBT at turn-off and can exceed the IGBT breakdown voltage [2]. We propose driving the IGBT by applying a signal on the gate with two different stages. By reducing the gate voltage to an intermediate level for a short time before the final turn-off, the IGBT collector current is limited and hence the potential overshoot is reduced [19].

A two-level turn-off driver can be implemented using a high-side NPN Darlington architecture and a low-side with an N-DMOS (Fig. 6) [18]. Before the turn-off stage, the DMOS LD1 and M1 switches are off, I_0 is on, and

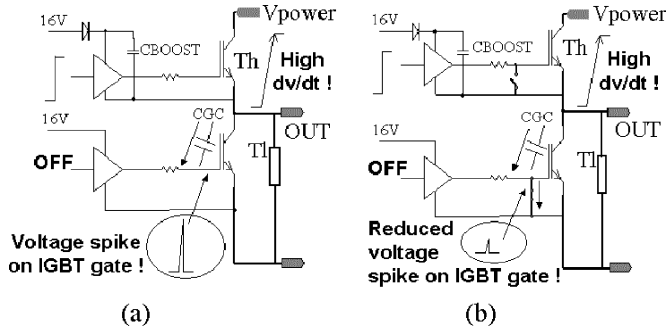

Fig. 7. Miller clamp principle.

OUTH = OUTL ≅ VH, $S0 = 1$, $S1 = 1$ and $ta1 = 0$. A voltage reference, VOFF, is applied on the LVOFF input to create an intermediate level at turn-off. We put the current source I_0 off with $S0 = 0$ in order to have no sourcing current. One puts the output of the tri-state switch in a high impedance state by setting the logic signal ta 1 equal to one and closing the DMOS M0 switch. The PNP transistor, T1, changes to on because a current flows from its base, via R0 and M0, to the ground. The collector current of T1 will put the DMOS M1 and LD1 in conduction due to the polarization of R2. At this point, the output, OUTH = OUTL, begins to fall. When the VOFF1 potential is equal to VOFF − VD2, the diode D2 becomes on and the PNP transistor, T1, is off, which cancels the collector current of T1. The DMOS switches M1 and LD1 become off and the output remains at an intermediate level near VOFF during the duration of the period Ta. After this period, the tri-state switch becomes on to control the gate of M1 and LD1 ($ta1 = 0$ and $S1 = 0$). Thus, the output falls to the VL potential.

If we want to turn-on the IGBT, we only have to open the DMOS LD1 and M1 switches and set the current source I_0 to on. This current source provides, via the Darlington, the current at the output that charges the output capacitor to a potential near VH—2 V ($S0 = 1$, $S1 = 1$, $ta1 = 0$).

With this schematic, users can adjust the intermediate level at the output by putting a potential (using a Zener diode, for example) on the LVOFF pin above all the IGBT thresholds.

C. Cross Conduction in Half Bridge

When the high-side IGBT Th in half bridge [Fig. 7(a)] turns on, OUT increases from almost 0 to V power with a high dv/dt. Following this, the current in the Miller capacitor, CGC, and the voltage on the gate of the low-side Tl, increase. This voltage can exceed the gate threshold level voltage of Tl and a large current can flow from Vpower to ground. This resulting voltage spike on the low-side IGBT [5]–[10] gate depends upon the level of dv/dt and gate off-state resistance. A negative off-state control voltage is generally used to prevent occurring cross conduction [20].

We propose an alternative solution to solve this problem: by using a dedicated clamp [Fig. 7(b)]. When Tl is off, a low-impedance path is established with this clamp between the IGBT gate and emitter to derive the Miller current and the voltage spike on the IGBT gate is greatly reduced. The active Miller clamp function is implemented using a comparator, a latch, and a laterally diffused metal oxide semiconductor (LDMOS) (see Fig. 8). This switch clamp goes on when the gate voltage becomes lower than 2 V relative to the GND level. Then the latch is set and the switch is pulled to ground until the next turn-on.

IV. New Driving Circuit

We propose a new family of IGBT gate drivers, which, at present, is comprised of three integrated circuits. All three ICs use 1-μm BCD3S process. The more complete circuit (Fig. 9) includes a desaturation protection, an active Miller clamp, and a two-level turn-off driver. It can be used with either a single positive power supply, or a dual positive/negative supply. Separated source (OUTH) and sink (OUTL) output pins allow the use of different gate resistors for turn-on and turn-off. The source stage is built with a bipolar NPN Darlington architecture, whereas the sink stage uses a LDMOS architecture. Peak output currents are 1.2-A sink, and 0.75-A source in worst case over the full temperature range (−20 °C to 125 °C). This circuit is especially adapted to 1200-V IGBT with current ratings of 25–80 A and the die area is only 5.55 mm^2.

An output driver including two-level for turn-on and turn-off has been validated as an intellectual property and tested with an output capacitance (Fig. 10). We do not propose integrated circuits including this driver, because the major request by IGBT applications manufacturers is to solve voltage overshoot failure at turn-off.

V. Experimental Results

A. Two-Level Turn-Off

In a first application, the circuit drives a pure capacitor and we obtain at the circuit output a signal with an intermediate level close to 11 V (Fig. 11).

Then, the two-level turn-off function is validated with IGBT using the schematics given in Fig. 12. The purpose of these measurements is to show the influence of VOFF on VCEmax [3]. This analysis was performed on two types of 1200-V IGBT (50 and 25 A). Under high current conditions, with a classical turn-off, a big overshoot appears for example, over 600 V [Fig. 13(a)] with $I_C = 150$ A and the turn-off switching losses $E_{OFF} = 15$ mJ on the second type of IGBT. By using a two-level turn-off, with the same current and an intermediate level VOFF equal to 11 V, the overshoot is only 240 V [Fig. 13(b)] with an increase of the turn-off switching losses ($E_{OFF} = 23$ mJ).

B. Active Miller Clamp and Cross Conduction

The tests were performed on a half-bridge configuration using two 1200-V 25-A IGBTs. Without an active Miller clamp, a big voltage spike appears on the IGBT gate in high dv/dt conditions [Fig. 14(a)]. The waveforms in Fig. 14(b) show the impact of the active Miller clamp on the voltage spike of the IGBT gate. The spike is decreased both in amplitude and duration with the active Miller clamp.

Therefore, we can conclude that the active Miller clamp function is suitable for reducing the risk of induced turn-on in high dv/dt conditions.

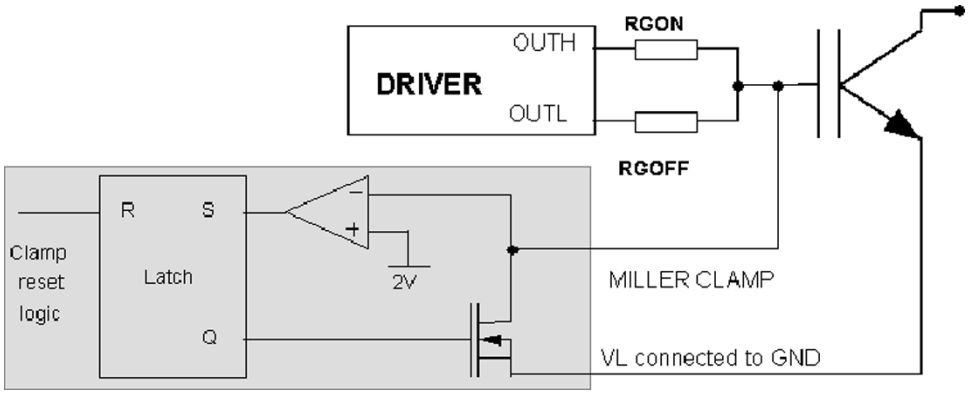

Fig. 8. Active Miller clamp function.

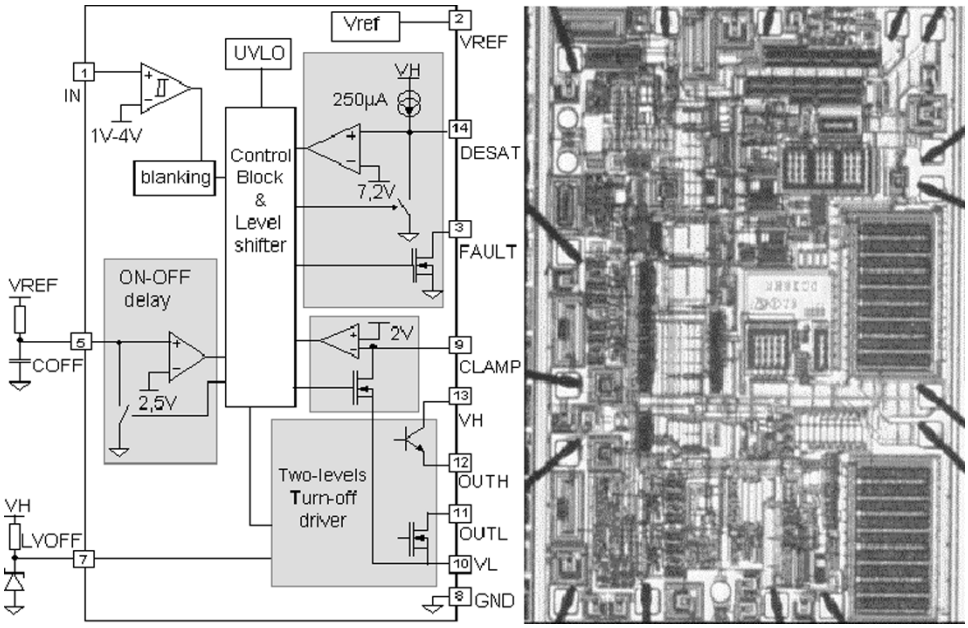

Fig. 9. IGBT driver block diagram and die.

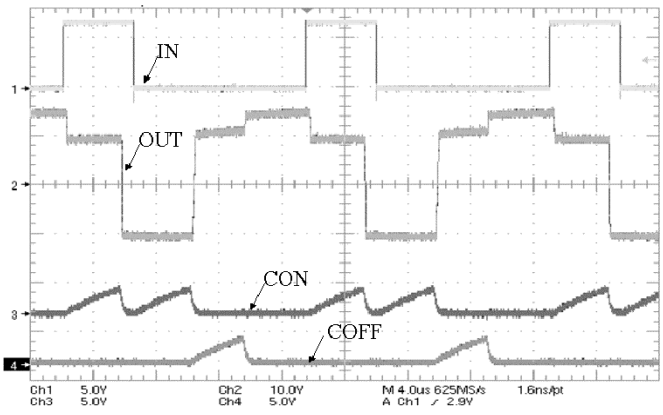

Fig. 10. Two-level turn-on and turn-off driver results with $C_{OUT} = 1$ nF, VON = 12 V and VOFF = 11 V.

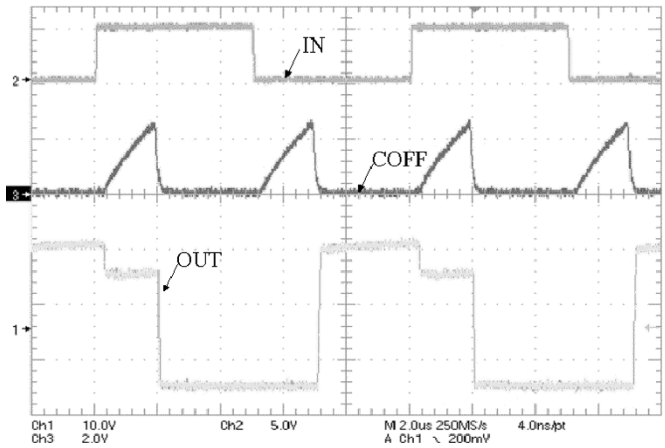

Fig. 11. Two-level turn-off driver results with $C_{OUT} = 1$ nF, VOFF = 11 V.

VI. Conclusion

A brief review of the IGBT operation has been presented. The main objective was to give a description of the IGBT turn-on or turn-off and to present a solution when the IGBT goes outside the safe operating area at both turn-on and turn-off. A new output driver using BCD technology was implemented to limit

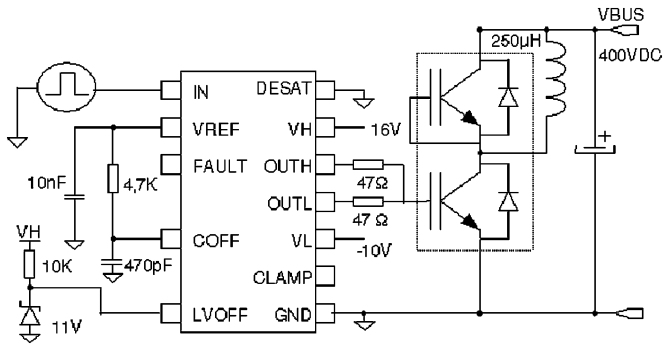

Fig. 12. Test bench for two-level turn-off driver.

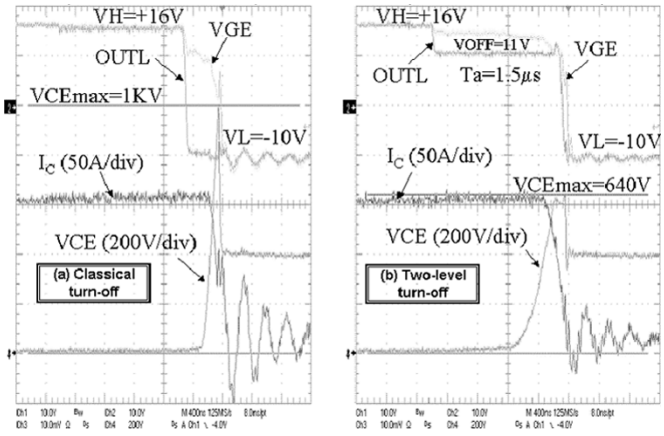

Fig. 13. Classical turn-off and two-level turn-off sequences with $\mathrm{VBUS} = 400$ V and $I_C = 150$ A.

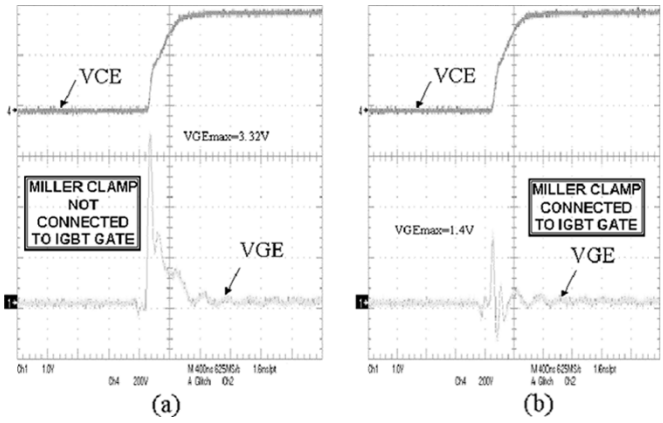

Fig. 14. VCE and VGE waveforms with and without the active Miller clamp function.

the peak reverse recovery current at turn-on and to limit overshoot at turn-off. An active Miller clamp function, to prevent cross conduction from occurring, was discussed in detail. A new driver circuit for IGBT in BCD3s process, containing a two-level turn-off driver, an active Miller clamp function and the well-known desaturation protection has been presented and achieved good results. These results have shown a large reduction of the overshoot at turn-off in high current conditions by using the two-level turn-off.

In conclusion, the advanced functions (active Miller clamp and two-level turn-off driver) and the well-known desaturation protection proposed inside this integrated circuit allow safe and reliable operation, with a minimum of external components, in applications such as motor control.

ACKNOWLEDGMENT

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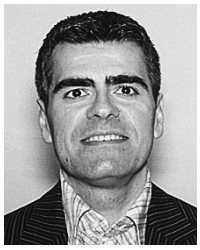

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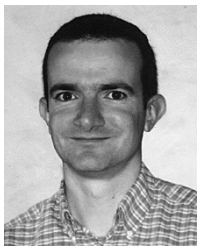
In 1988, he joined STMicroelectronics, Grenoble, France, as a designer of analog integrated circuits. He has worked in the field of power management, RF, and standard functions (operational amplifiers, comparators, voltage references). From 1999 to 2004, he was a Design Manager for the Power Management Ics Family. Since January 2005, he has been a Design Manager for standard integrated circuits. He has published two papers in conference proceedings and holds ten patents.



Anthony Boimond received the M.S. degree in electrical engineering from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France and from the Politecnico di Torino, Turin, Italy, in 1998.

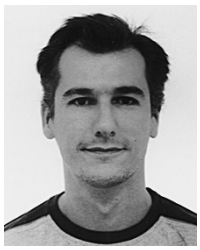
He joined the Discrete and Standard ICs Group (currently Micro Linear and Digital Group), STMicroelectronics, Grenoble, France, in 2000 as an Application Engineer for power management ICs.

Jean-François Garnier received the Ph.D. degree in electronics engineering from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France.

He has 15 years of experience in analog and power electronics. He joined the Discrete and Standard ICs Group (currently Micro Linear and Digital Group), STMicroelectronics, Grenoble, in 1999, and is currently in charge of defining new innovative products for power management applications.

Nicole Giraudo received the B.S. degree in biophysics from Ecole Technique Supérieure de Laboratoire (ETSL), Paris, France, in 1973 and the M.S. degree in solid state physics from the University Joseph Fourier, Grenoble, France, in 1981.

She joined Thomson Semiconducteurs (currently STMicroelectronics), Grenoble, in 1974 as a Device Engineer. Since 1995, she has been responsible for layout in the areas of power management devices, ADC converters, and high-speed operational amplifiers.



Olivier Terrasse received the B.S. degree in electrical engineering, the B.S. degree in robotics, and the M.S. degree in microelectronics from the Institut National Polytechnique de Grenoble (INPG), Grenoble, France, in 1989, 1991, and 1999, respectively.

He joined SGS-Thomson Microelectronics (currently STMicroelectronics), Grenoble, in 1992 as a Product Engineer. Since 1995, he has been responsible for test development and industrialization for power management devices.