

Hybrid ICs Drive High-Power IGBT Modules

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A pair of hybrid gate-driver ICs use optocoupling and isolated power supplies in compact, single inline packages to simplify the design of drive circuits for high-power IGBT modules.

Proper gate drive is critical to the performance and reliability of insulated gate bipolar transistor (IGBT) modules. The gate driver must produce high peak current for efficient switching and have stable driving voltages for good noise immunity and short-circuit durability. A completely isolated gate-drive circuit is most effective for meeting these requirements. A typical implementation of this type of gate drive is shown in Fig. 1. This circuit provides isolation of logic-level control signals using optocouplers and separate floating isolated power supplies for each gate driver. There

are a number of advantages to this topology, including:

- Stable on- and off-drive voltages that are independent of the power-device switching duty cycle.
- Capability of providing very high output currents for large IGBT modules.
- Power-circuit switching noise and high voltages are isolated from control circuits.
- Local power is available for protection circuits such as desaturation detection.

The main disadvantages of this type of driver are the cost, complexity and board space required. In addition, these circuits can be difficult to implement due to the severe requirements for noise immunity and high isolation voltage. To simplify the design and layout of isolated gate-drive electronics, Powerex has introduced the VLA500-01 and VLA502-01 hybrid integrated circuits to provide gate drive for high-power IGBT modules.

These gate drivers have been optimized for use with Powerex IGBT modules. However, the output characteristics are compatible with most MOS-gated power devices. A block diagram showing the main features of the VLA500-01 and VLA502-01 hybrid gate drivers is seen in Fig. 2. Both gate drivers convert logic level control signals into fully isolated +15-V/-8-V gate drive with up to 12 A of peak drive current. Isolated gate-drive power is produced by an integrated dc-dc converter, and control signals are isolated using high-speed optocouplers. In addition, short-circuit protection is provided by means of desaturation detection.

The two drivers are similar except that the VLA500-01 uses a standard open-collector type optocoupler with a maximum turn-off propagation delay of about 1.3 μ s. This makes it suitable for lower frequency industrial applications operating at up to about 15 kHz. The VLA500-01 is designed for use with Powerex NF-Series and A-Series IGBT modules. The VLA502-01 uses a high-speed buff-

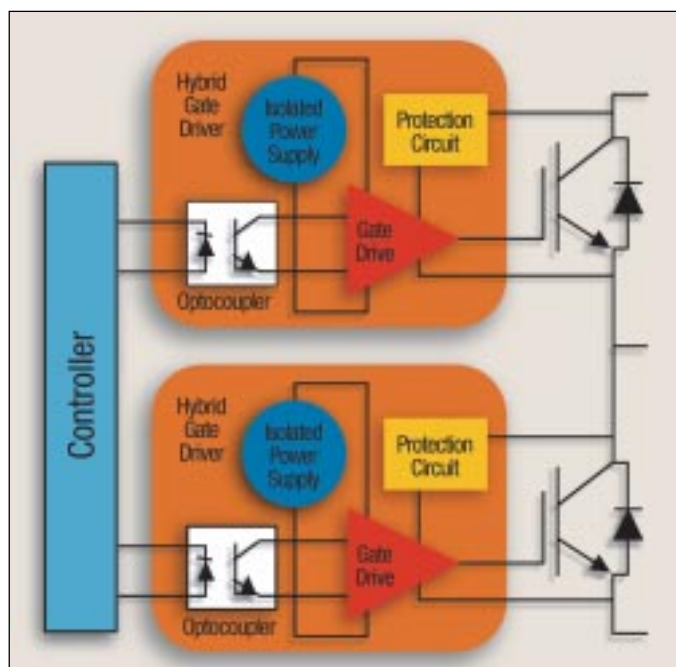


Fig. 1. A fully isolated gate driver combines optical isolation and high peak-current drive to an IGBT power module.

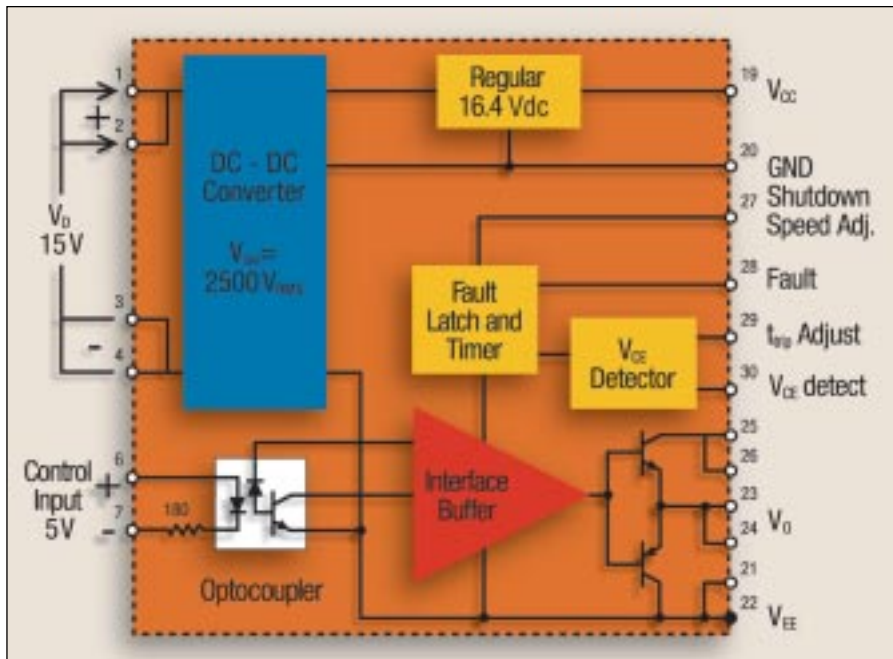


Fig. 2. The VLA500-01/VLA502-01 hybrid gate drivers include a fully isolated dc-dc converter power supply, optical isolation and up to 12 A of peak current to drive IGBT modules.

Comp.	Typical Value	Description
D1	0.5 A	V_{CE} detection diode—fast recovery, $V_{rrm} > V_{CES}$ of IGBT being used (Note 1)
DZ1	30 V, 0.5 W	Detect input pin surge voltage protection (Note 2)
DZ2, DZ3	18 V, 1.0 W	Gate-surge voltage protection
C1	150 μ F, 35 V	V_O supply decoupling—electrolytic, long life, low impedance, 105°C (Note 3)
C2, C3	100-1000 μ F, 35 V	DC-DC output filter—electrolytic, long life, low impedance, 105°C (Note 3,4)
C4	0.01 μ F	Fault feedback signal noise filter
C_s	0-1000 pF	Adjust soft shutdown—multilayer ceramic or film (see application note)
C_{TRIP}	0-200 pF	Adjust trip time—multilayer ceramic or film (see application note)
R1	4.7 k Ω , 0.25 W	Fault sink current limiting resistor
R2	3.3 k Ω , 0.25 W	Fault signal-noise suppression resistor
R3	1 k Ω , 0.25 W	Fault feedback signal-noise filter
R4	4.7 k Ω , 0.25 W	Fault feedback signal pull-up
OP1	NEC PS2501	Optocoupler for fault feedback signal isolation
B1	CMOS Buffer	74HC04 or similar—must actively pull high to maintain noise immunity

Notes:

1. The V_{CE} detection diode should have a blocking voltage rating equal to or greater than the V_{CES} of the IGBT being driven. Recovery time should be less than 200 ns to prevent application of high voltage to pin 30.
2. DZ1 is necessary to protect pin 30 of the driver from voltage surges during the recovery of D1.
3. Power supply input and output decoupling capacitors should be connected as close as possible to the pins of the gate driver.
4. DC-DC converter output decoupling capacitors must be sized to have appropriate ESR and ripple current capability for the IGBT being driven.

Table 1. Component types and values for a typical IGBT module driver design.



Fig. 3. Single inline packaging and upright mounting allows the VLA500-01/502-01 gate drivers to conserve printed circuit-board area and simplify layouts.

ered output-type optocoupler with a propagation delay of 0.4 μ s. This makes it suitable for use in higher frequency applications operating at more than 15 kHz. The VLA502-01 is designed for use with Powerex NFH-Series high-frequency optimized IGBT modules.

The hybrid gate drivers feature a compact, single inline package design, as shown in Fig. 3. The upright mounting design minimizes required printed-circuit board space to allow efficient flexible layout. Fig. 4 shows a complete application circuit schematic for the hybrid gate driver. Table 1 lists component types and values. The hybrid gate driver allows a complete isolated gate-drive circuit to be constructed with as few as 11 external components.

Short-circuit Protection

Most Powerex IGBT modules are designed to survive low-impedance short circuits for a minimum of 10 μ s. To take full advantage of this capability, it is desirable to include fast-acting protection as part of the gate-drive circuit. Implementing the protection as part of the gate-drive circuit helps to provide faster response by eliminating the propagation delays of the controller. The VLA500-01/VLA502-01 provide short-circuit protection by means of an on-state, collector-to-emitter voltage-sensing circuit. This type of protection is often called "desaturation detection."

Fig. 5 shows a block diagram of a typical desaturation detector. In this circuit, a high-voltage fast-recovery diode (D1) is connected to the IGBT's

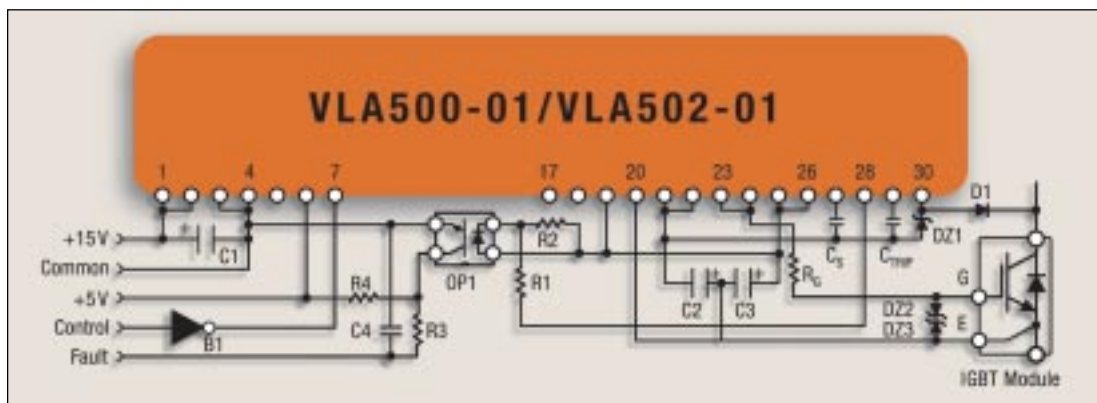


Fig. 4. A typical application design for the VLA500-01/502-01 gate drivers shows the interconnection of the devices to external components. The component values are listed in Table 1.

collector to monitor the collector-to-emitter voltage. When the IGBT is in the off state, V_{CE} is high and the diode is reverse biased. With the diode off, the (+) input of the comparator is pulled up to the positive gate-drive power supply (V_+). When the IGBT turns on, the comparator's (+) input is pulled down by the diode to the IGBT's $V_{CE(sat)}$. The (-) input of the comparator is supplied with a fixed voltage (V_{TRIP}). During a normal on-state condition, the comparator's (+) input will be less than V_{TRIP} and its output will be low. During a normal off-state condition, the comparator's (+) input will be larger than V_{TRIP} and its out-

put will be high. If the IGBT turns on into a short circuit, the high current will cause the IGBT's collector-emitter voltage to rise above V_{TRIP} even though the gate of the IGBT is being driven on. This abnormal presence of high V_{CE} when the IGBT is supposed to be on is called "desaturation."

Desaturation can be detected by a logical AND of the driver's input signal and the comparator's output. When the output of the AND goes high, a short circuit is indicated. The output of the AND can be used to command the IGBT to shut down in order to protect it from the short circuit. A delay (t_{TRIP}) must be provided after the comparator's output to allow for the normal turn-on time of the IGBT. The t_{TRIP} delay is set so that the IGBT's V_{CE} has enough time to fall below V_{TRIP} during normal turn-on switching. If t_{TRIP} is set too short, erroneous desaturation detection will occur. The maximum allowable t_{TRIP} delay is limited by the

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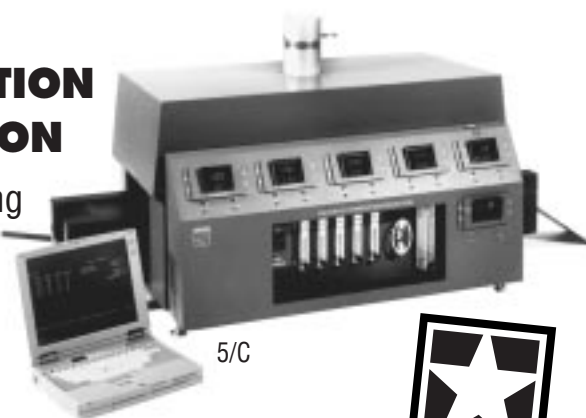


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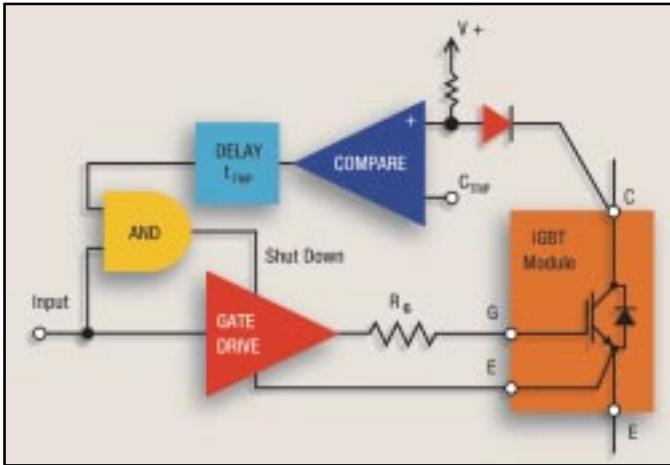


Fig. 5. A desaturation detector provides short-circuit protection for the gate drivers in case the external IGBT turns on into a short circuit.

IGBT's short-circuit withstanding capability.

The Powerex VLA500-01 and VLA502-01 incorporate short-circuit protection using desaturation detection as described previously. When desaturation is detected, the hybrid gate driver performs a soft shutdown of the IGBT and starts a timed (t_{timer}) 1.5-ms lockout. During the lockout, the driver produces a fault signal to notify the controller of the fault status. Normal operation of the driver will resume after the lockout time has expired and the control input signal returns to its off state.

The collector voltage of the IGBT is detected through the high-voltage blocking diode (D1) shown in Fig. 4. The blocking voltage of D1 should be equal to or greater than the V_{CES} rating of the IGBT being used. For applications using high-voltage IGBTs, it might be necessary to use series-connected diodes to achieve the desired blocking voltage. D1 must be an ultrafast recovery type to minimize the surge applied to the gate driver's detect input (pin 30). The Zener diode DZ1 provides additional protection of the gate driver's detect input from voltage surges during reverse recovery of the high-voltage blocking diode.

Trip Time and Soft Shutdown Speed

The VLA500-01 and VLA502-01 have a default short-circuit detection-time delay (t_{TRIP}) of approximately 3 μs . This will prevent erroneous detection of short-circuit conditions as long as the series gate resistance (R_g) is near the minimum recommended value for the module being used. The 3- μs delay is appropriate for most applications, so adjustment will not be necessary. However, in some low-frequency applications, it might be desirable to use a larger series gate-resistor to slow the switching of the IGBT, reduce noise and limit turn-off transient voltages.

When R_g is increased, the switching delay time of the IGBT also will increase. If the delay becomes long enough that the voltage on the detect pin (pin 30) is greater than V_{SC} at the end of the t_{TRIP} delay, the driver will erroneously indicate that a short circuit has occurred. To avoid

Eq. 1: RMS current for repetitive triangular pulses

$$i_{\text{RMS}} = i_p \sqrt{\frac{t_p \cdot f}{3}}$$

Where:

i_p = peak current

t_p = base width of pulse

f = frequency

Eq. 2: RMS current for turn-on gate pulses:

$$i_{G(\text{on})}(\text{RMS}) = i_{p(\text{on})} \sqrt{\frac{t_{p(\text{on})} \cdot f}{3}}$$

Where:

$i_{p(\text{on})}$ = peak turn-on current

$t_{p(\text{on})}$ = base width of on pulse

f = frequency

Eq. 3: RMS current for turn-off gate pulses

$$i_{G(\text{off})}(\text{RMS}) = i_{p(\text{off})} \sqrt{\frac{t_{p(\text{off})} \cdot f}{3}}$$

Where:

$i_{p(\text{off})}$ = peak turn-off current

$t_{p(\text{off})}$ = base width of off pulse

f = frequency

Eq. 4: Total RMS gate current

$$i_G(\text{RMS}) = \sqrt{i_{G(\text{on})}(\text{RMS})^2 + i_{G(\text{off})}(\text{RMS})^2}$$

Or assuming $i_{G(\text{off})} = i_{G(\text{on})}$
(on and off current pulses are symmetric)
the RMS gate current is:

$$i_G(\text{RMS}) = i_p \sqrt{\frac{2 \cdot t_p \cdot f}{3}}$$

Where:

i_p = peak gate current

t_p = base width of gate drive pulse

f = frequency

Table 2. Equations for calculating RMS ripple current in electrolytic capacitors.

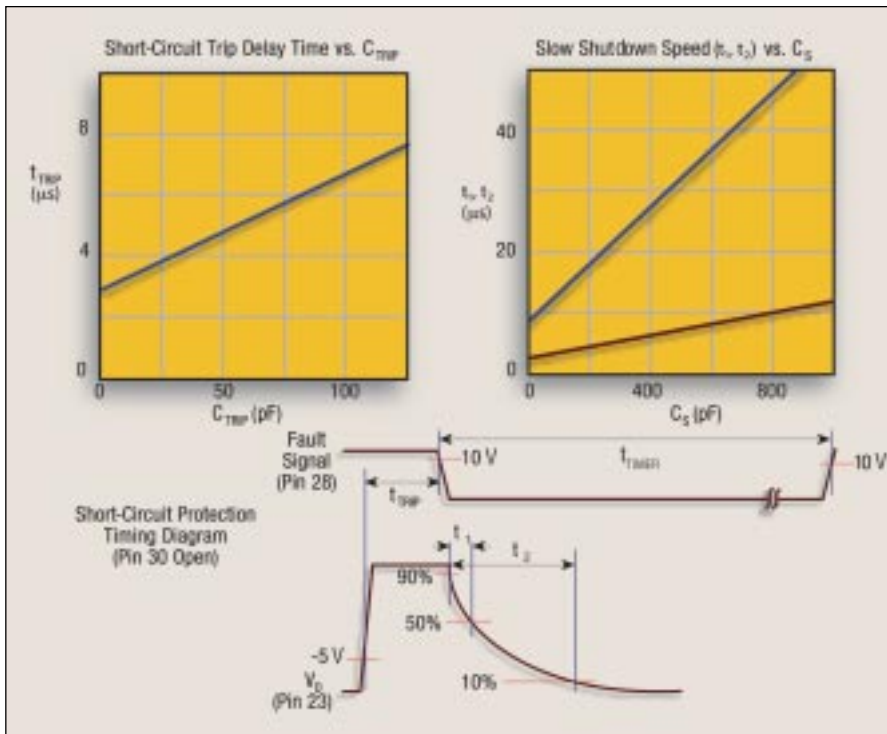


Fig. 6. The VLA500-01/502-01 drivers allow a trip-time delay to be adjusted by varying an external capacitor to prevent erroneous detection of short-circuit conditions.

this condition, the gate driver has provisions for extending the t_{TRIP} delay by connecting a capacitor (C_{TRIP}) between pin 29 and V_{EE} (pins 21 and 22). The effect of adding C_{TRIP} on trip time is shown in Fig. 6. If t_{TRIP} is extended, care must be taken not to exceed the short-circuit withstanding capability of the IGBT module. Normally, this will be satisfied for Powerex NF and A-Series IGBT modules as long as the total shutdown time does not exceed 10 μ s.

The gate driver provides a soft turn-off when a short circuit is detected to help limit the transient-voltage surge that occurs when large short-circuit currents are interrupted. The default shutdown speed will work for most applications, so adjustment is usually not necessary. In this case, C_S can be omitted. In some applications using large modules or parallel-connected devices, it might be helpful to make the shutdown even softer to minimize transient voltages. This can be accomplished by connecting a capacitor (C_S) between pin 27 and V_{EE} (pins 21 and 22). The speed of the shutdown as a function of C_S is shown in Fig. 6.

Powering the Driver

The gate driver requires a single 15-V control power supply (V_D) to power its internal circuits. The 15-V power supply is connected to the primary side of the hybrid gate driver's built-in dc-dc converter at pins 1, 2 and 3, 4. The control power supply must be decoupled with a capacitor ($C1$ in Fig. 4) connected as close as possible to the driver's pins. This decoupling capacitor is necessary to provide a stable, well-filtered voltage for the converter.

When selecting the input decoupling capacitor, it is important to ensure that it has a sufficiently high ripple current rating. The example circuit shown in Fig. 4 uses a 150- μ F low-impedance electrolytic for the input decoupling capacitor. This should be sufficient for most applications. It might be possible to use a smaller capacitor if the driver is lightly loaded and/or the main 15-V supply filter capacitor is located close to the driver. The current draw from the 15-V supply will vary from about 75 mA to almost 500 mA, depending on the size of IGBT being driven and the switching frequency. The gate-driver data sheet provides typical

curves that can be used to calculate the required supply current for a given application.

Isolated Power Supplies

The gate driver's dc-dc converter provides isolated gate-drive power consisting of +16.4 V (V_{CC}) at pin 19 and -9 V (V_{EE}) at pins 21 and 22. These supplies share a common at pin 20. Transformer coupling provides 2500-VRMS isolation between the 15-V control supply (V_D) and the gate-drive power. This feature allows the gate driver to provide completely floating gate drive that is suitable for high- or low-side switching.

The gate-drive power supplies must be decoupled using the low-impedance electrolytic capacitors C2 and C3 in Fig. 4. It is important that these capacitors have low enough impedance and sufficient ripple current capability to provide the required high-current gate-drive pulses.

Electrolytic capacitors have maximum allowable ripple current specifications due to internal heating effects. If the capacitor's ripple current specification is exceeded, the life of the capacitor can be significantly reduced. To estimate the ripple current requirements for the capacitors, it is necessary to measure or calculate RMS gate-drive current. When measuring RMS gate current, be certain the test instrument has a sufficiently high sampling rate to accurately resolve the relatively narrow gate current pulses. Most "true RMS" DMMs are not capable of making this measurement accurately.

The RMS gate current also can be estimated from the gate-drive waveform. Fig. 7 shows a typical gate current waveform. If we assume the turn-on and turn-off pulses are approximately triangular, we can estimate RMS gate current using the equations given in Table 2. Referring to Fig. 4, it can be seen that positive gate pulses are supplied by C3 while negative gate pulses are supplied by C2. In most applications, the peak gate current is much larger than the average current supplied by the dc-dc converter; thus,

it is reasonable to assume that the RMS ripple current in the decoupling capacitor is roughly equal to the RMS gate current.

The ripple current in the decoupling capacitors (C2, C3) can be estimated using equations 2 and 3 from Table 2. For example, in Fig. 7 we see that $i_p(\text{off}) = 12 \text{ A}$ and $t_p(\text{off}) = 1440 \text{ ns}$ from the triangle approximation of I_G . If the switching frequency $f = 20 \text{ kHz}$, then using equation 3 of Table 2, the RMS ripple current in C2 is approximately 1.11 A RMS.

Generally, it is a good idea to select a capacitor with a maximum ripple current rating larger than the calculated current. For this example, a low impedance 1000- μF electrolytic capacitor with a ripple current rating of 1.95 A would be an appropriate choice. If the application is operating at lower frequency or lower peak current (larger R_G), it is possible to reduce the size of the decoupling capacitors C2 and C3. However, keep in mind that larger capacitors with higher ripple current ratings will provide longer life and, therefore, are always desirable. The only penalties for using larger than necessary capacitors are their size and cost.

Selecting Gate Resistance

The V_{EE} and V_{CC} supplies are connected to the driver's output stage to produce gate drive at pins 23 and 24. The gate-drive current is adjusted by selecting the appropriate series gate resistance (R_G), and connecting it between pins 23, 24 and the gate of the IGBT (Fig. 4). R_G will normally be adjusted to provide suitable drive for the IGBT module being used. A smaller R_G will provide faster switching and lower losses while a larger R_G will provide reduced transient voltages and switching noise. Typically, larger modules will require a smaller R_G and smaller modules will use a larger R_G .


For most Powerex IGBT modules, the minimum recommended R_G can be found in the conditions for the switching time specifications on the module's data sheet. In most applications, the optimum R_G will be some-

where between the data sheet value and 10 times that value. Keep in mind that the minimum allowable R_G for the VLA500-01/VLA502-01 is 1 Ω . An R_G of less than 1 Ω may cause the peak output current to exceed the driver's 12-A limit.

When driving large IGBT modules at high frequency, the power dissipated in the series gate resistor R_G can be substantial. The power dissipation

can be estimated using equation 4 from Table 2. For example, at 20 kHz the waveform shown in Fig. 7 has a total RMS gate current of approximately 1.57 A RMS. If the series gate resistor is 1 Ω , then the power dissipation is: $P = i^2 R = 2.46 \text{ W}$. In this case, at least a 3-W resistor is required. The gate-drive circuit layout must be designed so that the additional heat produced by the gate resistor does not

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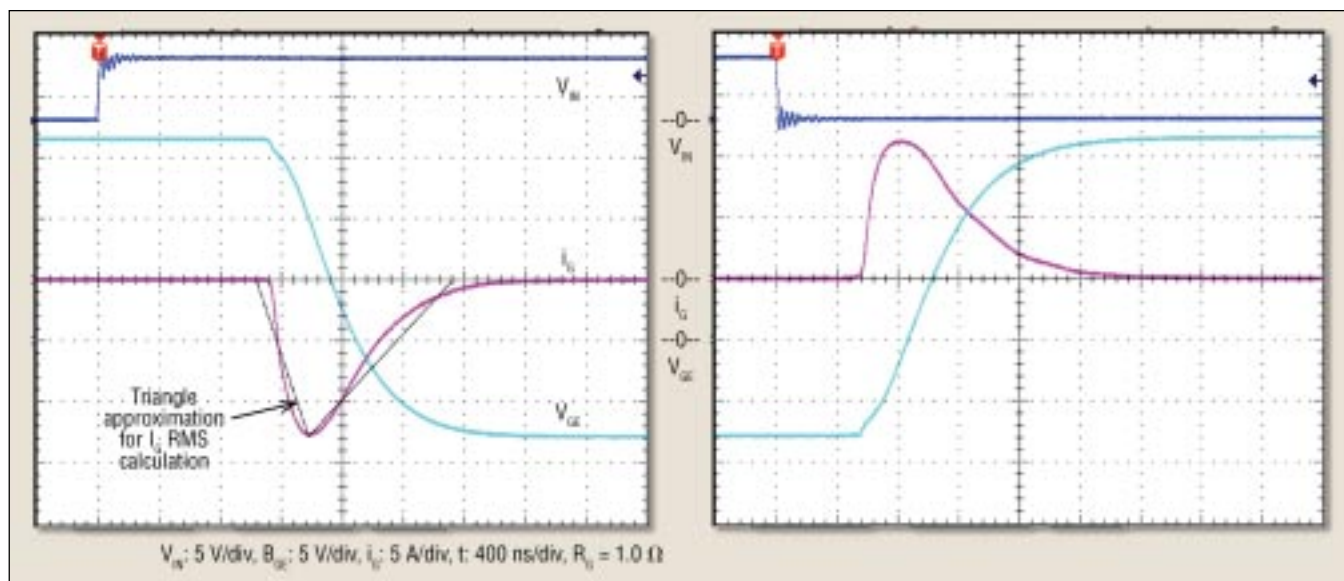


Fig. 7. Gate-drive current waveforms such as these are used to calculate the ripple current flowing into electrolytic capacitors.

overheat nearby components.

Protection against gate voltage surges is provided by back-to-back Zener diodes DZ2 and DZ3 (Fig. 4). These Zener diodes also help to con-

trol short-circuit currents by shunting Miller current away from the gate. These Zeners must be capable of supporting high-pulse currents. Therefore, devices with a minimum 1-W rating are recommended.

Input Circuit

The input circuit between pins 6 and 7 consists of the built-in high-speed optocoupler's LED in series with a resistor. In most applications, pin 6 will be tied directly to the 5-V logic power supply. An ON signal (gate output high) is generated by pulling pin 7 to ground using a CMOS buffer capable of sinking at least 16 mA (74HC04 or similar). In the off-state, the buffer should actively pull pin 7 high to maintain good noise immunity. Open collector drive that allows pin 7 to float will degrade common-mode noise immunity and, therefore, is not recommended.

Fault Signal

If the gate driver's short-circuit protection is activated, it will immediately shut down the gate drive and pull pin 28 low to indicate a fault. Current flows from Vcc (pin 19) through the LED in fault-isolation opto (OP1) to pin 28 (Fig. 4). The transistor in the fault-isolation opto

turns on and pulls the fault signal line low. During normal operation, the collector of OP1 is pulled high to the +5-V logic supply by the resistor R3. When a fault is detected, the hybrid gate driver disables the output and produces a fault signal for a minimum of 1 ms. Any signal on the fault line that is significantly shorter than 1 ms cannot be a legitimate fault, so it should be ignored. Therefore, for a robust noise-immune design, it is recommended that an RC filter with a time constant of approximately 10 μ s be added (R3, C4). This opto-isolated fault signal now can be used by the controller to detect the fault condition.

Additional detailed information on using the VLA500-01 gate driver can be found on the device data sheet. In addition, a BG2A gate-drive reference design is available for prototype evaluation. The BG2A is a complete two-channel gate-drive reference design-printed circuit board that uses the VLA500-01/VLA502-01 hybrid gate drivers.

Full documentation for the BG2A is available from the Powerex website (www.pwr.com). For additional general information on IGBT module gate-drive requirements, please refer to Powerex IGBT module application notes.

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