

ENT-AN1231 Application Note
VSC8541/VSC8531/VSC8540/VSC8530
Design and Layout Guide



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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.1

Revision 1.1 was published in September 2017. There were no changes to the technical content in revision 1.1 of this document.

1.2 Revision 1.0

Revision 1.0 was published in May 2017. It was the first publication of this document.

2 Overview

This document provides useful guidelines for the design and layout of printed circuit boards utilizing the VSC8541 and VSC8531 Single Port Gigabit Ethernet PHY and the VSC8540 and VSC8530 Single Port Fast Ethernet PHY. It is geared toward achieving first pass design success. Although the VSC8541 device number is used throughout the document, it is also applicable to the VSC8531, VSC8540, and VSC8530.

For more information about the devices, consult the VSC8541/VSC8531/VSC8540/VSC8530 datasheets.

IEEE 802.3, CSMA/CD Access Method and Physical Layer Specification

High Speed Digital Design, Author: Howard Johnson, PH.D., ISBN 0-13-395724-1

3 Design Considerations

The following sections describe the ground and power considerations to keep in mind when using the devices.

3.1 Ground Considerations

The following considerations are related to ground.

3.1.1 Exposed Ground Pad

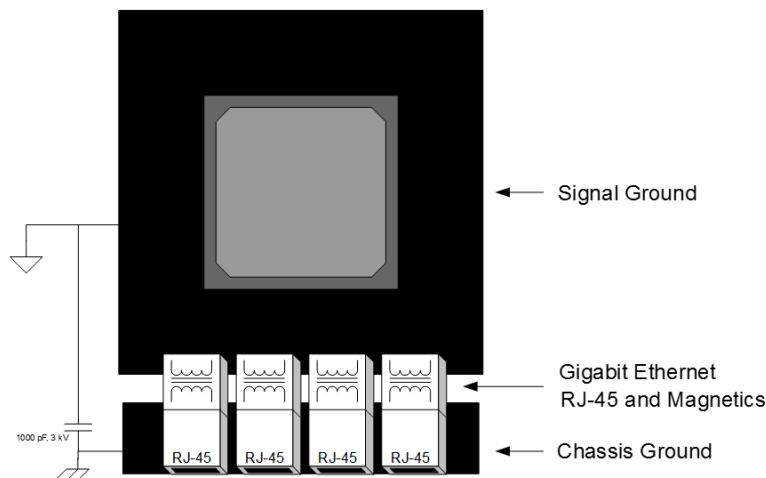
The VSC8541 package has an exposed pad at the bottom of the device. This exposed pad provides a path for electrical grounding and a heat transfer point to the PCB, and is sometimes referred to as the "thermal paddle" ([Thermal Considerations \(see page 9\)](#)). The pad provides a very low induction to the ground plane, which is ideal for high-speed applications. The exposed pad on the PCB is non-solder mask defined (NSMD). The exposed pad for VSC8541 on the PCB is 5.2 mm × 5.2 mm (same as the size on the package), while for VSC8531 it is 3.3 mm × 3.3 mm. The solder mask opening is 5.3 mm × 5.3 mm for VSC8541 and 3.4 mm × 3.4 mm for VSC8531, with solder mask-to-metal clearance of 50 µm. There should not be any solder mask on the exposed pad of the PCB in order to maximize thermal dissipation.

For detailed assembly guidelines, please see ENT-AN1203 VSC8540/VSC8541 Quad Flat No-Lead Package (QFN) Surface Mount Assembly Guidelines.

3.1.2 Ground Isolation

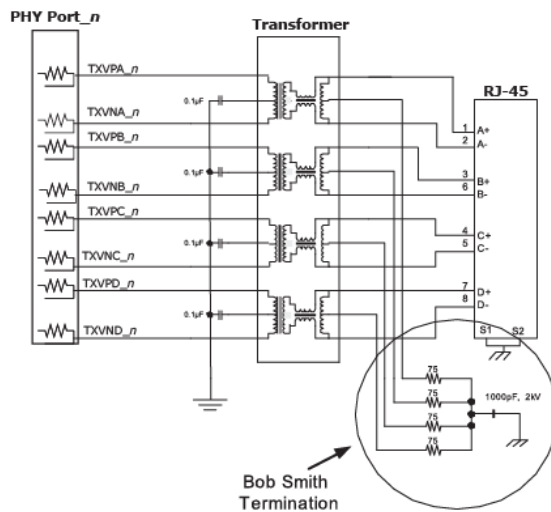
To isolate the board from electrostatic discharge (ESD) events and to prevent a common-mode noise ground path, a separate chassis ground region should be allocated. This separate chassis ground, shown in the following illustration, should be connected electrically to the external chassis and to the shield ground of the RJ-45 connectors.

Figure 1 • Ground Plane Layout



3.1.3 Bob Smith Termination

In addition, the Bob Smith termination impedance should be connected between the chassis ground and the cable-side center taps of the transformer module, as shown in the following illustration.

Figure 2 • Bob Smith Termination

3.2 Power Considerations

The following considerations relate to the power of the devices.

3.2.1 Power Supply Planes

The VSC8541 requires a minimum of two power rails, 2.5 V and 1.0 V. The filtered analog 1.0 V and 2.5 V supplies should not be shorted to any other digital supply at the package or PCB level. Refer to the datasheet for other power supply options. The following are the most important PCB design and layout considerations:

- Ensure that the return plane is adjacent to the power plane (that is to say, without a signal layer in-between).
- Ensure that a single plane is used for voltage reference with splits for individual voltage rails within that plane. Attempt to maximize the area of each power rail split on the power plane (based on corresponding via coordinates for each rail) in order to maximize coupling between each voltage rail and the return plane.
- Minimize resistive drop while efficiently conducting heat away from the device using 1 oz copper cladding.

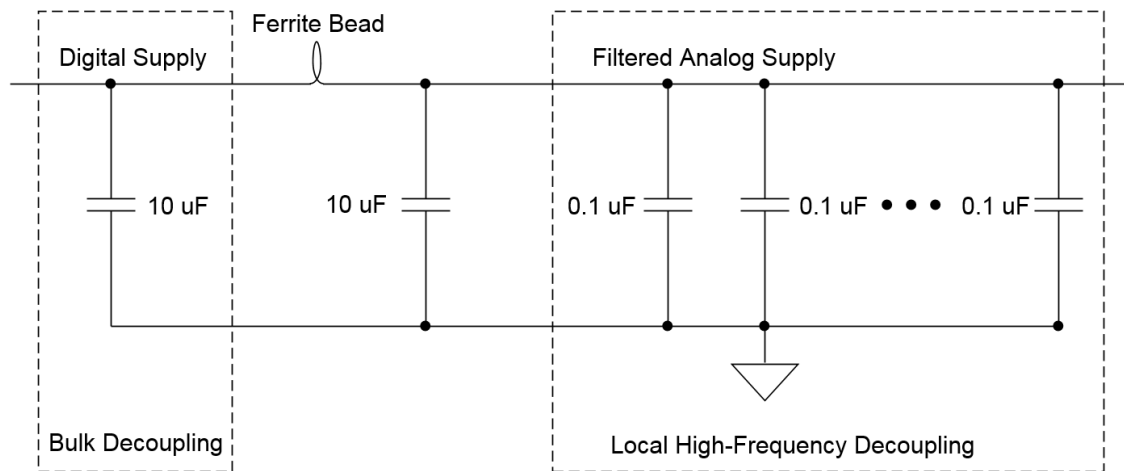
Each of these supplies requires the lowest resistive drop possible to the power pins of the device with properly placed local decoupling. For the analog supply filtering, a ferrite bead is required ([Analog Power Plane Filtering \(see page 4\)](#)). Given their low loss, it is recommended to use ferrite beads when possible over a series inductor filter, particularly for high-density/high-power devices.

3.2.2 Analog Power Plane Filtering

A ferrite bead should be used to isolate each analog supply from the rest of the board. This bead should be placed in series between the bulk decoupling capacitors and the local decoupling capacitors.

All PCB designs yield unique noise coupling behavior, so not all ferrite beads or decoupling capacitors may be needed for every design. It is recommended that system designers provide an option to replace the ferrite beads with zero-ohm resistors, once a thorough evaluation of system performance is completed.

The following illustration shows a schematic of the filtered supply.

Figure 3 • Filtered Supply

The beads should have the following characteristics:

- Current rating of at least 150% of the maximum current of the associated power supply
- Minimum DC resistance (DCR) of less than 100 milliohms (recommended)
- Impedance of 80 ohms to 100 ohms at 100 MHz

Recommended beads are:

- Panasonic EXCELSA39 or similar
- Steward HI1206N101R-00 or similar
- Murata BLM31PG121SN or other BLMxxPG parts

3.2.3 Local Decoupling

Bulk decoupling capacitors should be tantalum and can be placed at any convenient position on the board. Local decoupling capacitors should be X5R or X7R ceramic and placed as close to the VSC8541's power pins as possible for each and every power pin. Assuming the VSC8541 is on the top side of a PCB board, the best location for local decoupling capacitors is on the bottom/underside of the PCB board directly under the device.

3.3 Miscellaneous Design Considerations

The following sections describe additional considerations for design.

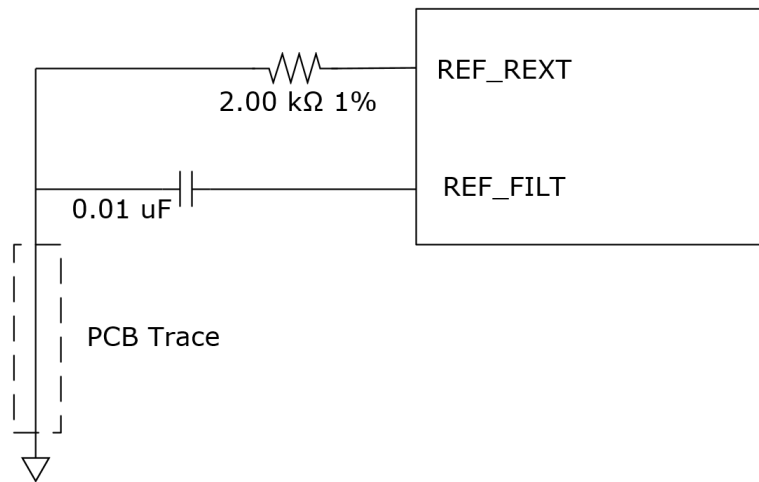
3.3.1 REF_FILT/REF_REXT Pins

For proper operation, the VSC8541 must generate an on-chip band gap reference voltage at the REF_FILT pin. For this, the following components are required for each VSC8541 in the system:

- 2.0 kΩ resistor, 1% tolerance, minimum 1/16 watt
- 0.01 μF capacitor, 20% tolerance, NPO, X7R or X5R ceramic materials are all acceptable

For best performance, special considerations for the ground connection of the voltage reference circuit are necessary to prevent bus drops that would cause inaccuracy of the reference voltage. The ground connections of the resistor and the capacitor should each connect to a shared PCB signal trace, rather than connect individually to a common ground plane. This PCB signal trace should then connect to a ground plane at a single point. In addition, the reference capacitor and resistor should be placed as close as possible to the VSC8541.

The following illustration shows a reference schematic for the voltage.

Figure 4 • Voltage Reference Schematic

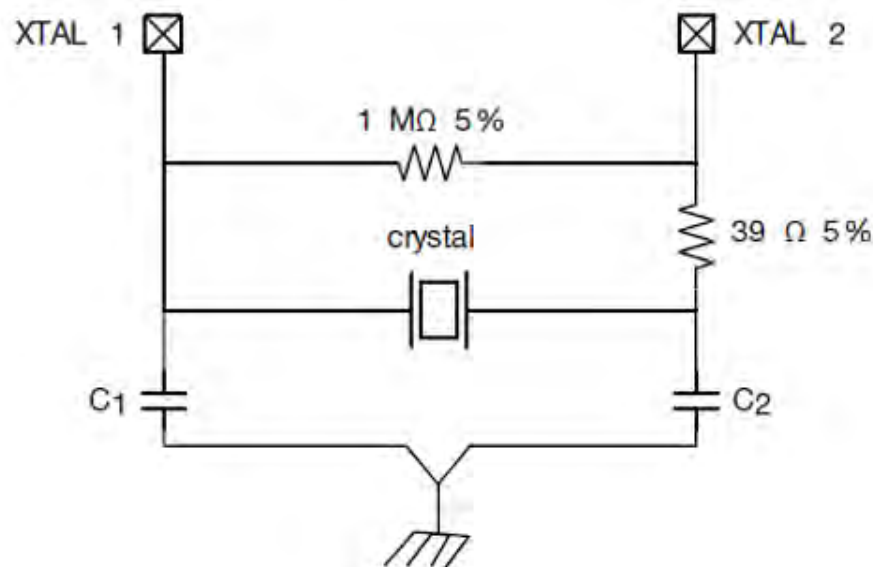
3.3.2 Clock Inputs

VSC8541 supports either crystal oscillator input mode or single-ended input reference clock mode. Two REFCLK_SEL pins are used to select among the various options. For more information, refer to the datasheet.

3.3.2.1 Crystal Oscillator Input Mode

When REFCLK_SEL[1:0] = 00, the on-chip oscillator will be enabled. The following illustration shows a reference tank circuit for a fundamental mode crystal.

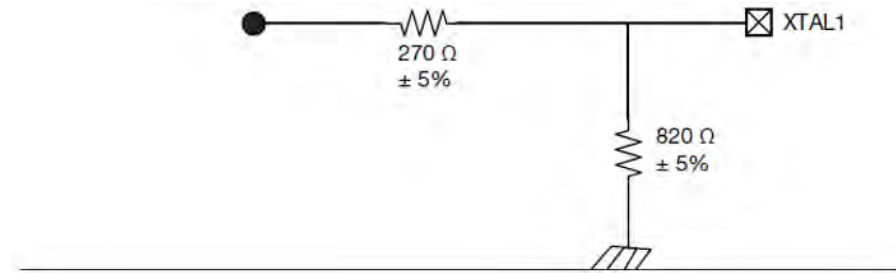
Note: For best performance, traces on the PCB should be of similar length and Kelvin-connected to ground.

Figure 5 • Tank Circuit

3.3.2.2 Input Reference Clock Mode

XTAL1 is referenced to Vdd25A (so in order to use the 3.3 V reference clock signal, voltage scaling is required).

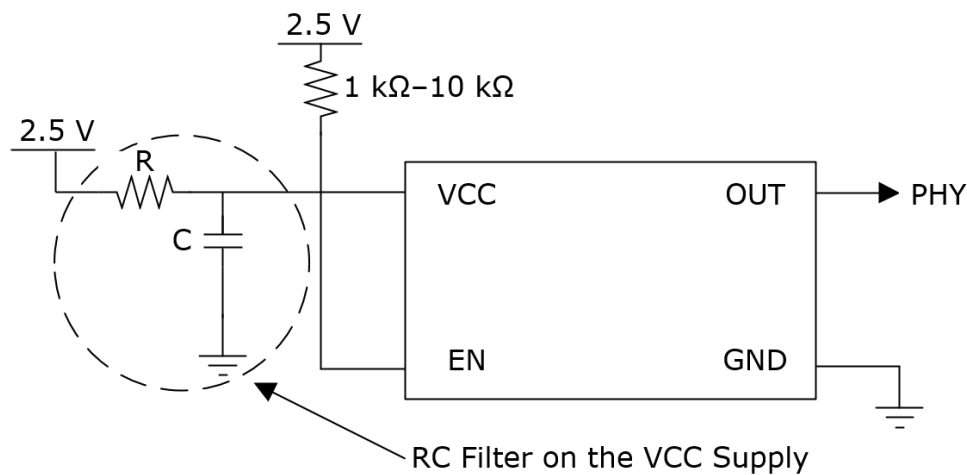
Figure 6 • External 3.3 V Reference Clock



3.3.2.3 Clock Power Supply Filtering

If using a 25 MHz or a 125 MHz 4-pin oscillator with a VCC pin, it is recommended an RC filter be implemented in order to avoid power supply switching noise coupling into the PHY. The filter should be set to filter out the frequency of the supply's switching regulation frequency. The OUT signal, as shown in the following illustration, should be tied to REFCLK.

Figure 7 • Clock Power Supply Filtering



Thus, for a supply with a switching frequency of 350 kHz, use an R value= 2.2 Ω and a C value= 11 μF.

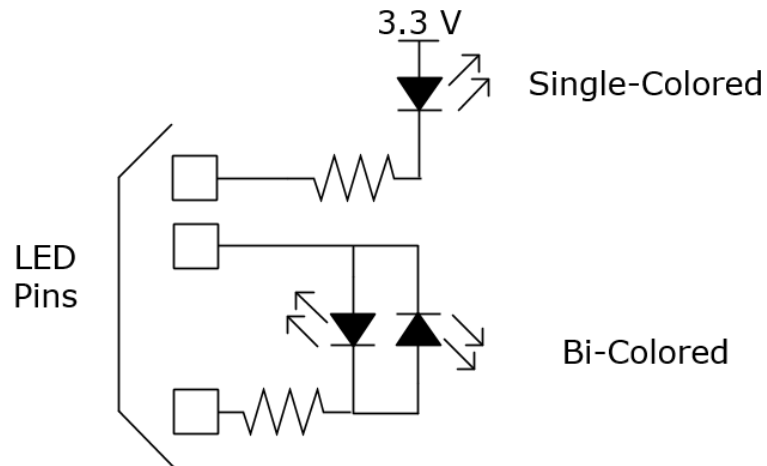
3.3.3 LEDs

The LED interface supports the following configuration: direct drive and basic serial LED mode. Each LED pin can be configured to display different status information that can be selected by setting the LED mode in register 29. In addition to the LED modes in register 29, there are LED modes that are enabled on the LED0 pin whenever the corresponding register 19E1, bits 15 to 12 are set to 1. For more information on LED settings, see the VSC8541 datasheet.

Each VSC8541 PHY port can support up to 2 single-colored LEDs. Each LED pin sinks current when an indication is present and de-asserts when inactive. By design, each LED pin can also drive current when not active. This is very useful in the case for bi-colored LEDs. Each LED pin in the VSC8541 can be designated to indicate any of the possible LED status signals, thereby further simplifying the overall design.

The following illustration shows LED configurations.

Figure 8 • LED Configurations

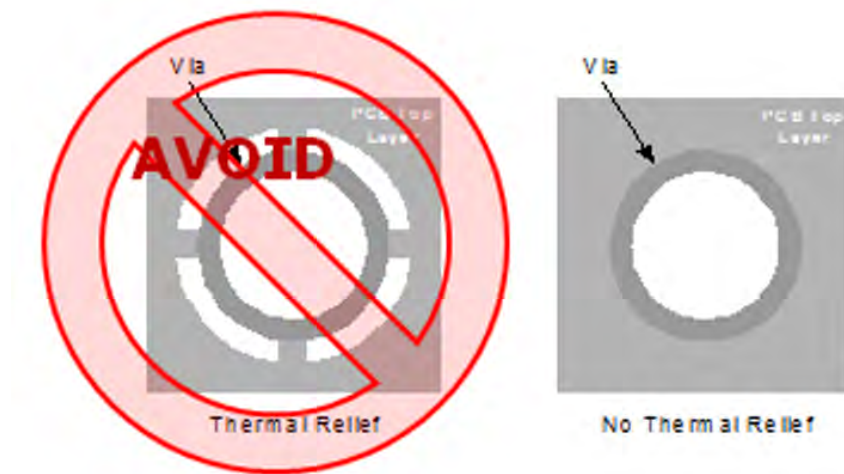


4 Thermal Considerations

For proper cooling and efficient thermal dissipation, maximize the number of via connections to the ground plane. Furthermore, additional ground planes will enhance thermal dissipation and signal integrity performance. For a QFN package, the die-attach (or thermal) paddle is exposed and directly conducts heat away from the die, so the thermal via should be drilled within the landing boundary (opposite the exposed paddle). The VSC8541 PCB reference design package includes an example of appropriate thermal connections for this device.

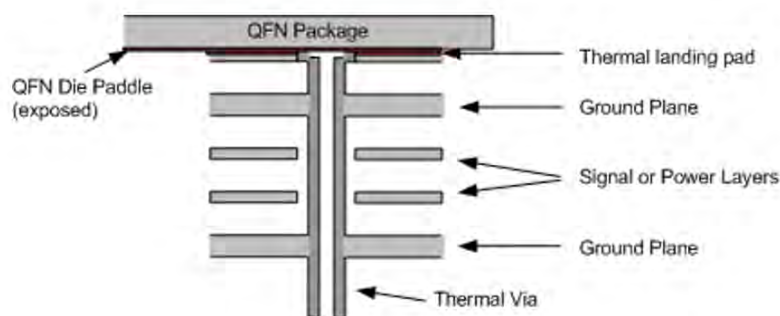
When connecting these thermal vias to ground planes, it is advisable to avoid thermal-relief connection traces. These, as shown in the left-hand side of the following illustration, are designed to prevent heat flow through the PCB. Instead, the thermal vias should have a solid connection to the traces and planes on each layer (as shown in the right-hand-side of [Thermal Ground Plane Connection](#) (see page 9)).

Figure 9 • Thermal Vias



In order to dissipate heat below the package, the PCB thermal via should connect to the solid ground planes within the board (minimum 1-oz cladding is recommended). The following illustration shows a simplistic profile of a thermal via within the PCB's thermal land area below the QFN paddle (package I/O pins and their corresponding pads are not shown). Also, steps should be taken to prevent solder wicking by the thermal vias. To avoid solder wicked by the thermal vias during the soldering process, it is recommended that the vias be fully copper-plated. If copper plating does not plug the vias, thermal vias can be tented with solder mask on the top layer. The solder mask should be larger than the diameter of the via.

Figure 10 • Thermal Ground Plane Connection



5 Copper Interface

The following sections describe the copper interface of the device.

5.1 Layout Considerations

The P0_DxP and P0_DxN pins interface to the external CAT5 cable and are organized in four differential pairs ($x = 0, 1, 2, 3$). When routing these pairs on a PCB, choose one of the following:

- Route each trace single-ended with a characteristic impedance of $50\ \Omega$ referenced to ground.
- Route each positive and negative trace on each port as differential pairs with $100\ \Omega$ characteristic differential impedance.

For any unused pairs, connect a $100\ \Omega$ termination resistor between P and N.

5.2 RJ-45 Connectors

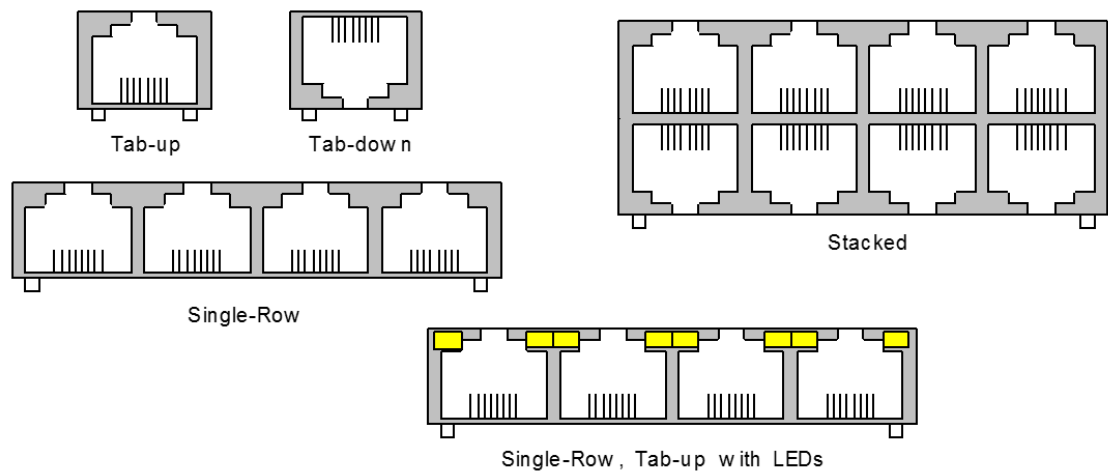
System designers have the following options for RJ-45 connectors.

- Two tab orientations: tab-up and tab-down.
- For multi-port connectors, two orientations: stacked and single-row.
- Single and bi-colored LEDs can be integrated into the connectors.
- Magnetics can be integrated into the connectors.

Most manufacturers can mix or match any combination of features. For example, LEDs can be added to any connector, or single-row, multi-port configurations can be tab-up or tab-down. The exception is the stacked connector, which contains both tab-up and tab-down orientations.

The following illustration shows example configurations of RJ-45 connectors.

Figure 11 • RJ-45 Example Configurations



An additional consideration is the pinout of tab-up versus tab-down connectors. Due to the orientation, the pinouts of these two are reversed. While the VSC8541 will work equally well using either orientation, signal routing will be simpler with the tab-down pinout. For the stacked variety, both orientations exist in one package, so both pinouts typically exist in one package. Some manufacturers have provided an option for “vertical” pin orientation, which allows for PCB routing ease.

6 MAC Interface

The VSC8541 supports MII, RMII, GMII, and RGMII MAC interfaces. This section's guidelines apply to all interfaces. With the high-speed nature of these interfaces, careful attention must be paid to the PCB layout in order to maintain adequate signal integrity. The MAC output pins are designed with fast rise and fall times to allow for 125-MHz operation. To adequately accommodate these signals on a PCB, it is recommended that the traces be designed as either microstrip or stripline transmission lines with a characteristic impedance of 50 ohms. It is also important that an unbroken plane exist below (and/or) above these signals.

The characteristic impedance of each MAC receive interface PCB trace must total 50 ohms. For the VSC8541 MAC receive interface, each pin has a **nominal output impedance of 11 ohms to 23 ohms (depending on the VDDMAC power rail)**; thus, an external 39-ohm to 27-ohm series resistor is required for each signal of the MAC receive interface.

For the VSC8541 MAC transmit interface, careful attention must be paid to the output impedance of the pins on the MAC or switch device. If that impedance is less than 50 ohms, additional series termination resistors are required. These resistors should be placed as close as possible to the MAC or switch device.

For MII, RMII, and GMII routing, each port should be independently matched in length to within **120 mils** (approximately 3 mm). It is not necessary to match the lengths of the TX traces to the RX traces. The TX traces can be of a different length in respect to the RX trace lengths.

6.1 RGMII Interface Clock Considerations

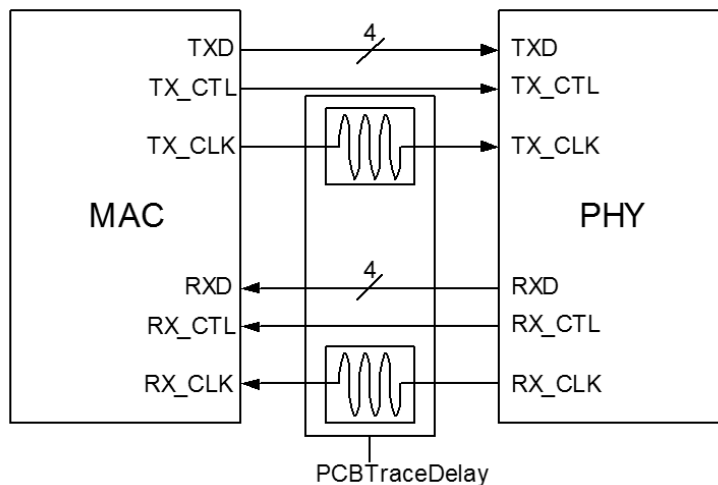
Proper operation of the RGMII bus requires careful control of the timing relationship between clock and data signals. The RGMII specification requires that the signal clock be delayed by a half bit time (2 ns) at the receiving end of the data path. This clock delay can be added externally (extended clock trace length), or by using internal delays built into the VSC8541.

6.1.1 External Delay Compensation

A delay of 1.5 ns to 2.0 ns can be added to the TX_CLK and RX_CLK signals by routing them through a long PCB "trombone" trace delay. The delay-line routing is shown in [Internal Delay Compensation in the PHY Only \(see page 12\)](#).

Note: For the VSC8541 device, the TX_CLK signal is named GTX_CLK.

Figure 12 • External Delay Compensation

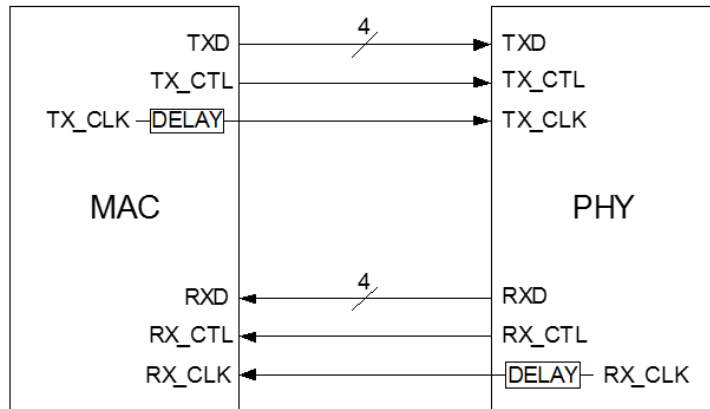


6.1.2 Internal Delay Compensation

An output clock skew can be integrated into the clock signal output of the transmitter. Specifically, this calls for the MAC to provide a clock skew on the TX_CLK, while the PHY must provide a clock skew on the RX_CLK. Devices supporting this type of configuration are defined as “RGMII-ID” in the RGMII standard.

The following illustration shows internal delay compensation in the MAC and PHY.

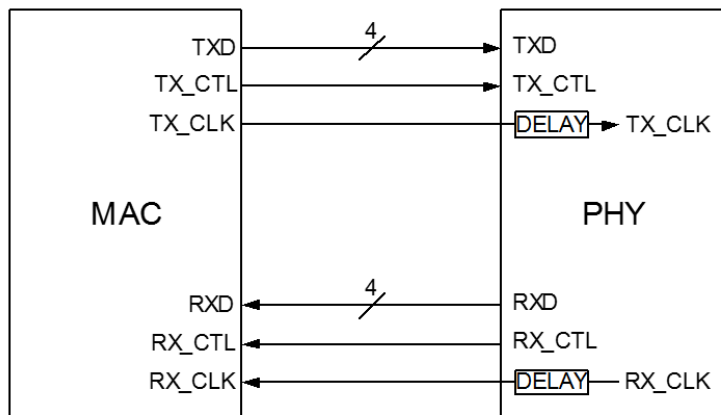
Figure 13 • Internal Delay Compensation in the MAC and PHY



However, the VSC8541 device can also support a clock skew integrated into the PHY for both RX_CLK and TX_CLK. This allows a MAC that does not support the RGMII-ID configuration to be connected to a PHY without the use of PCB trace delays.

The following illustration shows internal delay compensation in the PHY only.

Figure 14 • Internal Delay Compensation in the PHY Only



6.2 RMII Interface Clock Consideration

There are two basic modes of operation in RMII mode:

- Mode 1: System provides a 50-MHz clock that is used to clock the RMII interface and must be used as the chip reference clock.

- Mode 2: PHY operates from a 25-MHz or 125-MHz reference clock and sources the 50-MHz clock used for the RMIi interface.

Mode 1 and Mode 2 are shown in the following illustrations.

Figure 15 • Mode 1

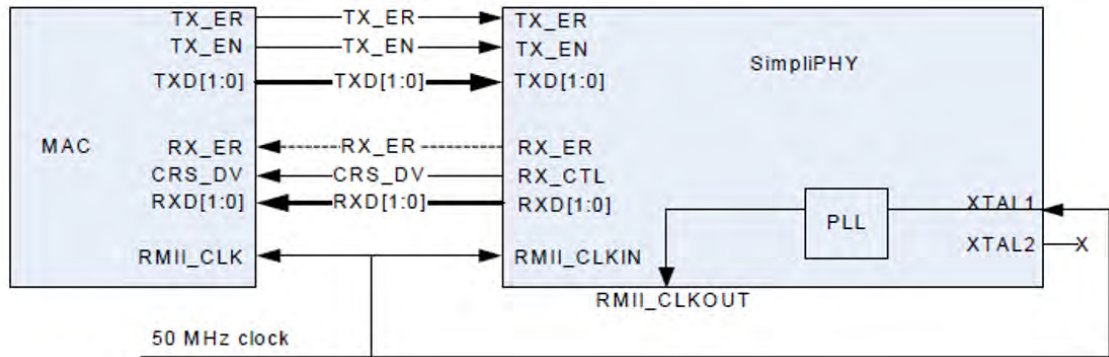
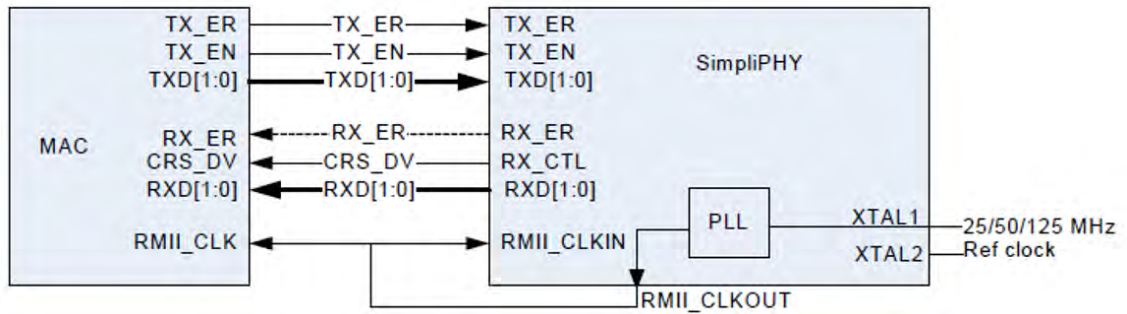


Figure 16 • Mode 2



7 Bringing Up the Device

The following section describes how to bring up the device.

7.1 Reset Sequence

Assuming that all input power supplies are stable, the JTAG reset can be de-asserted 100 nanoseconds after REFCLK is stable. Hardware (NRESET) reset should not be de-asserted until at least 100 nanoseconds after de-asserting JTAG reset.

Note: It is important that the values of the REFCLK_SEL pins and other HW strapping signals are latched on the rising edge of the NRESET pin, so the power supplies must be stable before the rising edge of NRESET. The NRESET should never be tied directly to logic high on the PCB; otherwise, the VSC8541 will behave unpredictably. If the design cannot control the NRESET pin, then a small delay circuit must be added to this signal to provide the necessary delay.

The following events occur sequentially when the VSC8541 is brought out of reset. This is triggered by a low-to-high transition of the NRESET pin. For unmanaged mode operation, the NRESET pin must have two rising edges (logical 0-1-0-1 transition sequence).

1. Values for the REFCLK_SEL and other HW strapping pins are latched asynchronously immediately out of reset.
2. Approximately 10 milliseconds after de-assert of NRESET, the analog reference voltages and current stabilize. This is seen on the REF_REXT and REF_FILT pins.
3. Once a stable analog reference is established, the internal PLL will require 110 microseconds to lock. The PLL provides the device its internal clocks.
4. With a locked PLL, the analog-to-digital converter (ADC) blocks require 4.9 milliseconds to calibrate.
5. Once the ADC is calibrated, the device is in normal operation and its MDC and MDIO pins are operational.

8 Schematic and Layout Review Checklist

The following checklist should be reviewed to ensure proper design connectivity and adherence to all considerations.

8.1 Generic Considerations

If a board design is based on a Microsemi reference design and Microsemi Software use is planned, please perform the following:

- Keep a log of changes made to the Microsemi design, such as port number and PHY addresses.
- Retain the reference board's use of GPIO (parallel as well as serial) whenever possible.

8.2 Pin Group Considerations

The following sections describe considerations for the pin groups of the device.

8.2.1 Reference Clock

Check	Signal Name(s)	Connectivity Comments
	XTAL1, XTAL2	Referenced to VDD25A. To use the 3.3 V reference clock signal, voltage scaling is required.
	REFCLK_SEL_[1:0]	Internal pull-up. Please review DS for detail.
	RCVRD_CLK	Only available in VSC8541 and VSC8540. Referenced to VDDIO. Please use proper back matching termination resistor.
	CLK_SQUELCH_IN	Internal pull-up. Place an optional resistor to GND for potential debug using the recovered clock.
	CLKOUT	Internal pull-down. Referenced to VDDIO. Please use proper back matching termination resistor.

8.2.2 Twisted Pair

Check	Signal Name(s)	Connectivity Comments
	P0_D[3:0]P, P0_D[3:0]N	<p>The naming convention used is such that [3:0] is the differential pair identification.</p> <p>Route as differential 100 Ω impedance or single-ended 50 Ω impedance reference to GND.</p> <p>Note: The correct RJ-45 connectivity to support 1GbE includes pairs (1,2; 3,6; 4,5; 7,8).</p> <p>Optional TVS components may be added, assuming junction capacitance <3 pF.</p> <p>Differential pair traces should be kept the same length.</p>
	Magnetics Guideline	<p>For more information on the following items, see the ENT-AN0098 Magnetic Guide application note:</p> <ul style="list-style-type: none"> • CMC on the line side • PHY-side center taps individually AC-coupled to GND • Individual Bob Smith termination per channel • Return loss of 18 dB for 1 MHz–40 MHz and 12–20log(f/80) dB over 40 MHz–100 MHz • Flatness of frequency response from 1 MHz–40 MHz (important) • Turn ratio tolerance $\pm 3\%$ or better • Insertion loss ~ 1 dB • CMNR 35 dB or better • Crosstalk 35 dB or better • 12 cores to provide better EMI

8.2.3 MAC Interface

Check	Signal Name	Connectivity Comments
	RXD[3:0]	Output. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping or PHY address. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	RX_CLK	Output clock for RGMII, GMII, and RMII. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	RX_DV /RX_CTL	Output. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping or PHY address. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	RXD[7:4]	Output. Only available in VSC8541 and VSC8540. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	RX_ER, COL, CRS	Output for GMII and MII i/f. Only available in VSC8541 and VSC8540. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	MII_TXCLK	Output clock for MII mode. Only available in VSC8541 and VSC8540. Please use the proper back matching termination resistor based on VDDMAC. These pins are also used as HW strapping. Internally pull-down, if external PU is required, placed as close as possible to the pin before the back match resistor.
	TXD[3:0]	Input.
	TXD[7:4]	Input, upper data bus for GMII. Only available in VSC8541 and VSC8540.
	GTX_CLK	Input clock for GMII, RGMII, and RMII. Identified as TX_CLK in VSC8531 and VSC8530.
	TX_EN /TX_CTL	Input control/enable for RGMII and GMII.
	TX_ER	Input. Only available in VSC8541 and VSC8540.

8.2.4 SMI Interface

Check	Signal Name	Connectivity Comments
	MDC	If not point-to-point, lay out as a daisy chain rather than branching which results in stubs. Confirm voltage swing compatibility with station master and other slaves on the bus.
	MDIO	If not point-to-point, lay out as a daisy chain rather than branching which results in stubs.
	MDINT	Open-drain output. A pull-up resistor to the proper supply is required.
	NRESET	Internal pull-down. Only de-assert NRESET after all power supplies and reference clocks are stable. Please refer to Reset Sequence (see page 14) for additional NRESET requirement in unmanaged applications.

8.2.5 Miscellaneous Pins

Check	Signal Name	Connectivity Comments
	THERMDA	Add a test pad and optional 0 Ω to GND if unused.
	THERMDC_VSS	Add a test pad if unused.

Check	Signal Name	Connectivity Comments
	REF_REXT REF_FILT	REF_REXT must use be 2.0 kΩ 1% resistor and REF_FILT must use a 0.01 uF capacitor. The two components must join at a single common point connected to the analog ground plane. For more information, see REF_FILT/REF_REXT Pins (see page 5) .
	COMA_MODE	Internal pull-up. If this signal will not be configured through software, it must be pulled-down to enable PHY operation. It is also used to synchronize LED operation among multiple chips.
	LED[0:1]	If unused, leave floating. LED pins shall have a low series resistance. Ensure each chosen pin can drive the correct LED indication.
	FASTLINK_FAIL	Only available in VSC8541 and VSC8540. Leave floating if unused.
	RESERVED*	Leave floating.

8.2.6 Power Pins

Check	Signal Name	Connectivity Comments
	VDD1A ¹	1.0 V analog supply, mostly associated with the SerDes.
	VDD1 ¹	1.0 V digital core supply.
	VDD25A ¹	2.5 V analog supply, mostly associated with the twisted pair interface.
	VDDMAC ¹	Supply for MAC interface signals: 1.5 V, 1.8 V, 2.5 V, or 3.3 V.
	VDDIO	2.5 V or 3.3 V for general I/O power. Ensure proper decoupling.
	VDDMDIO	1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V for SMI (MDC and MDIO) pins. Ensure proper decoupling.
	VSS (GND)	See Ground Considerations (see page 3) for proper decoupling and filtering details.

¹For more information about proper decoupling and filtering, see [Power Considerations \(see page 4\)](#).

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