iMX6 Rex Module

Variant: Prototype

27. 9. 2013
V1I1

RELEASED 27-SEP-2013

Page	Index	Page	Index	Page	Index	Page	Index
1	COVER PAGE	11	CPU - POWER	21	.....	31	.....
2	BLOCK DIAGRAM	12	CPU - UNUSED	22	.....	32	.....
3	CONNECTORS	13	ETHERNET PHY	23	.....	33	.....
4	CPU - DDR3, DDR3 MEM	14	SPI FLASH, LEDS	24	.....	34	.....
5	CPU - SATA, PCIe	15	PWR 3V3, 1V375, 3V0_ALWAYS	25	.....	35	.....
6	CPU - HDMI, LVDS	16	PWR 2V5, 1V5	26	.....	36	.....
7	CPU - USB, ETHERNET	17	MECH	27	.....	37	.....
8	CPU - SPI, I2C, SD, MMC	18	POWER SEQUENCING	28	.....	38	.....
9	CPU - UART, AUDIO	19	DOC REVISION HISTORY	29	.....	39	.....
10	CPU - JTAG, CONTROL	20	.....	30	.....	40	.....

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes .

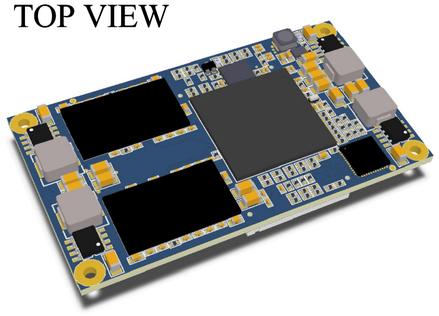
DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for debug notes.

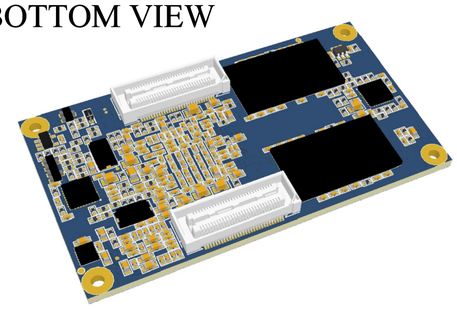
DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

TOP VIEW



BOTTOM VIEW



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Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[01] - COVER PAGE.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 1 of 20	

iMX6 Rex Module

(Block Diagram)

Input Voltage: 7~24V (DC)

POWERS

Page 15
PMIC 1

Page 15
PMIC 2

Page 16
PMIC 3

Page 4
DDR3 MEMORIES
(DDR3-1066 / Up to 4GB)
DDR3

Page 14
SPI FLASH
(Up to 32MB)
SPI3

USER LED
(ORANGE)

POWER LED
(GREEN)

Pages 4 - 12
CPU
(Freescale iMX6)

Page 13
ETHERNET PHY
(10/100/1000 Mbps)
RGMII
Ethernet PHY, LEDs

Page 3
BOARD CONNECTOR 1

1x HDMI
1x SD card (SD3)
1x SPI2
1x USB OTG
1x full UART1 (or 2x RX, TX, RTS, CTS UART1 and UART3)
1x I2C4
ON/OFF, RESET_IN, RESET_OUT

Page 3
BOARD CONNECTOR 2
(Optional)

Digital audio
1x LVDS0
1x MMC card (SD2)
1x SATA
1x PCIE
1x USB HOST
1x UART2
JTAG

http://www.iMX6Rex.com

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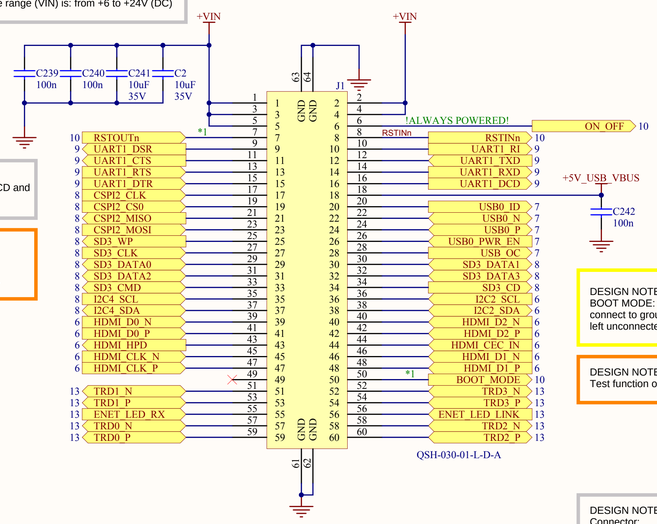
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[02] - BLOCK DIAGRAM.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 2 of 20	

CONNECTORS

DESIGN NOTE:
Input voltage range (VIN) is: from +6 to +24V (DC)

DESIGN NOTE:
UART1 signals DSR, DTR, DCD and RI can be used as UART3.

DESIGN NOTE:
*1 Be careful during debugging phase - this pin is connected to +3V0_ALWAYS.



DESIGN NOTE:
BOOT MODE: !ALWAYS POWERED!
connect to ground to boot from serial downloader, left unconnected to boot from e-fuses.

DESIGN NOTE:
Test function of BOOT MODE.

DESIGN NOTE:
Mating connector: QTH-030-02-L-D-A

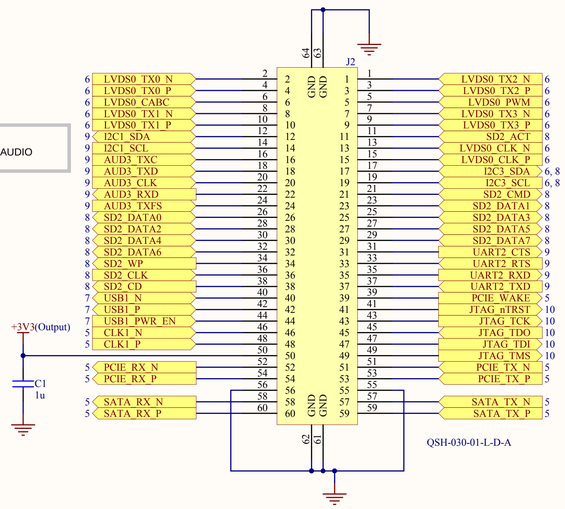
http://www.digikey.com/product-detail/en/QTH-030-02-L-D-A/SAM8186-ND/1106530

DESIGN NOTE:
Connector:
1.0A per contact, 7.8A ground plane

DESIGN NOTE:
3V3 output. Max. 1A (Can be used on Base board)

DESIGN NOTE:
If required, use Pin 49 on Connector 1 for Ethernet Tap Voltage.

DESIGN NOTE:
I2C1 is used with AUDIO



DESIGN NOTE:
I2C3 is used with LVDS

DESIGN NOTE:
In reference design I2C3 uses LVDS1. Software changes may be required.

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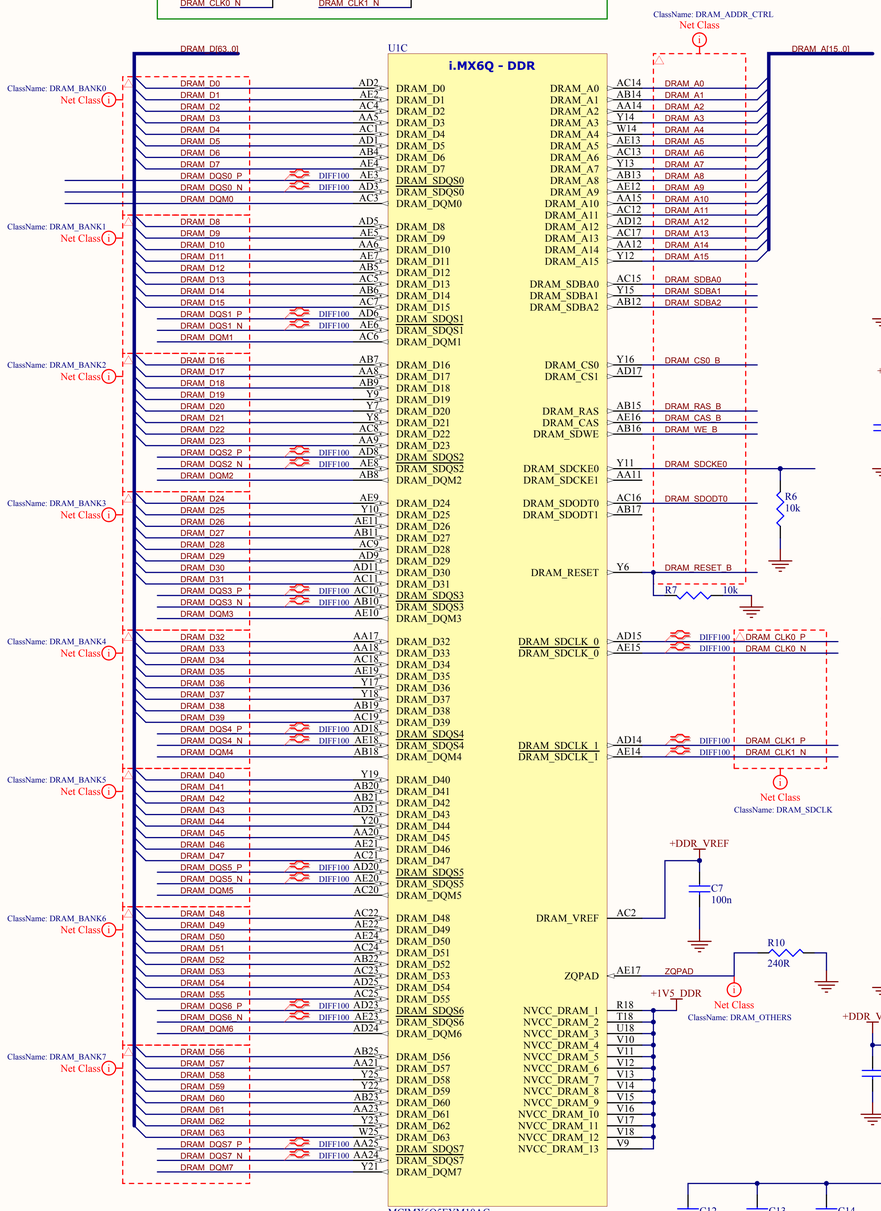
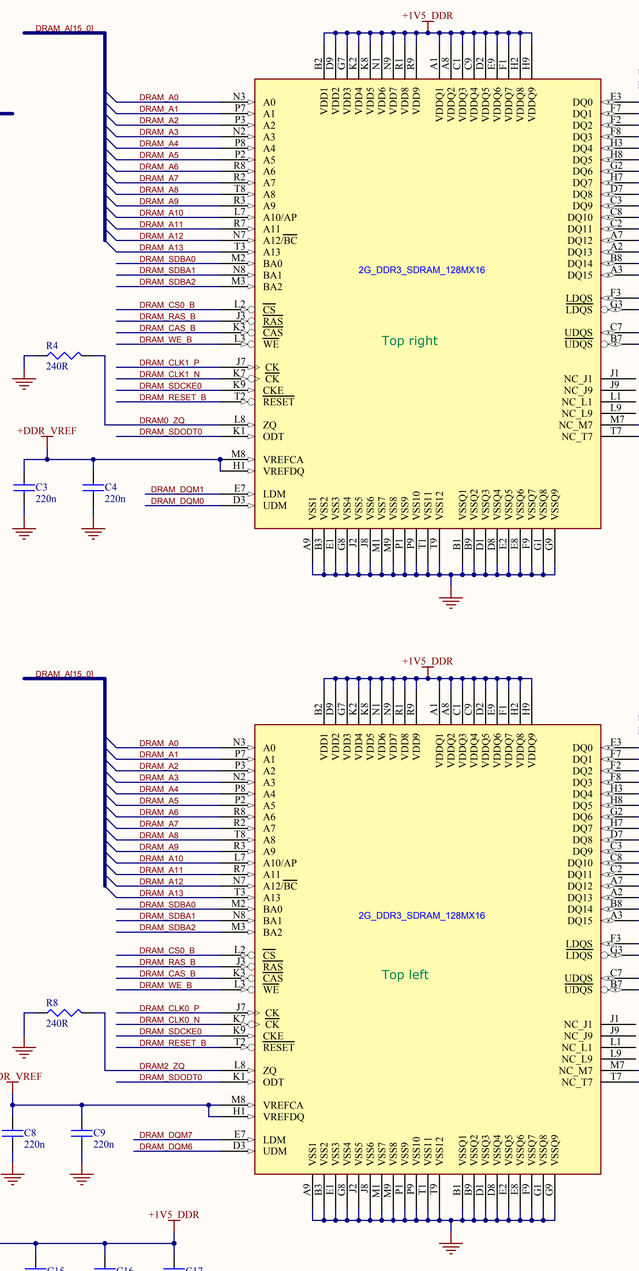
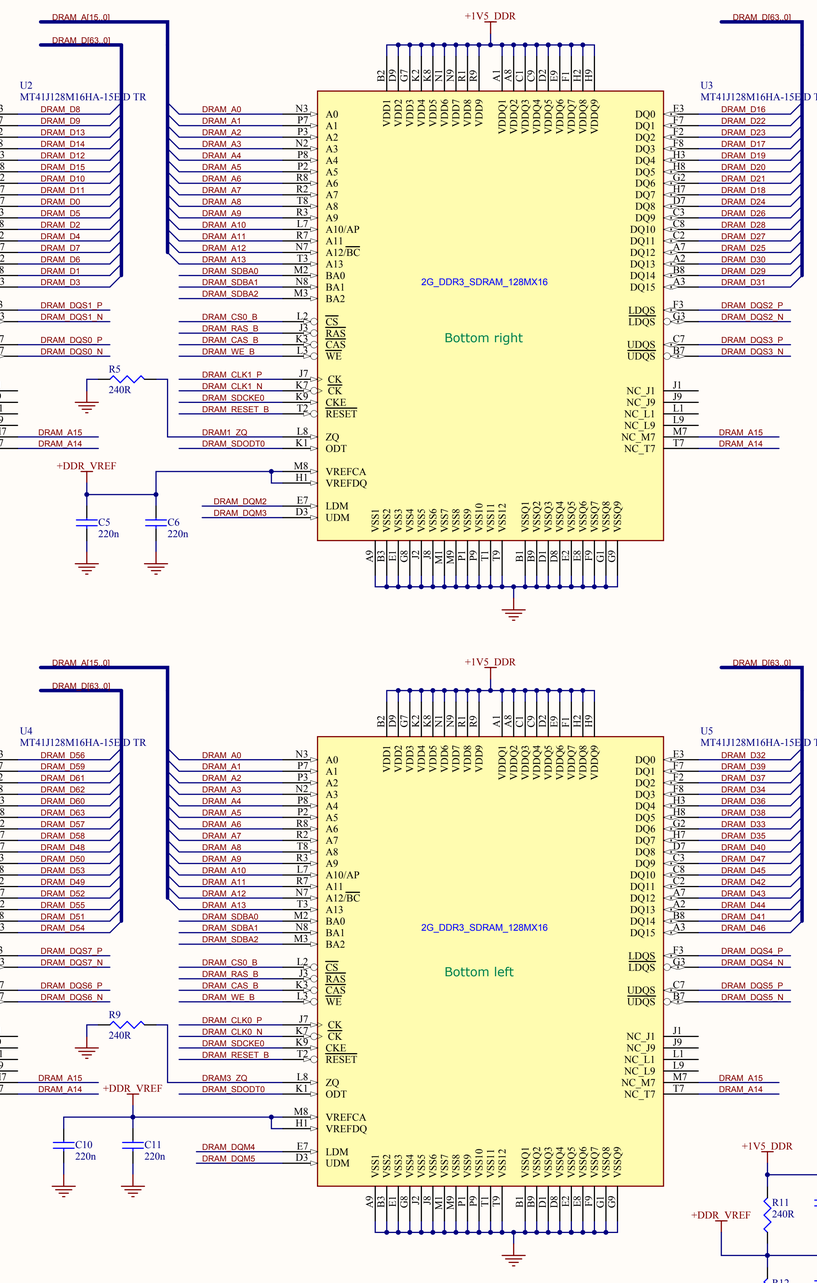
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[03] - CONNECTORS.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 3 of	20

CPU - DDR3, DDR3 MEM







DESIGN NOTE:
Pull down resistor RX3 is added to trace SDCKE0 in Rev B4 by soldering to an existing open via. Change will be made permanent in layout with the Rev C board.

DESIGN NOTE:
Using bit swapping for DATA bus to allow easy pcb routing.

DESIGN NOTE:
When using data bit swapping the low order bit of eachbyte must reside at bit 0 of the byte. The remaining 7 data bits can be swapped freely. This restriction is for write leveling calibration. Example D0 to D0 or D0 to D8, and D1-7 can be swapped.

DESIGN NOTE:
When swapping byte lanes on 16-bit memories, remember to move the DQMx, DQSx, and DQSx_B signals for that byte lane.

DESIGN NOTE:
Recommended resistor values R11 and R12 are 768 Ohm 1% (Hardware development guide).

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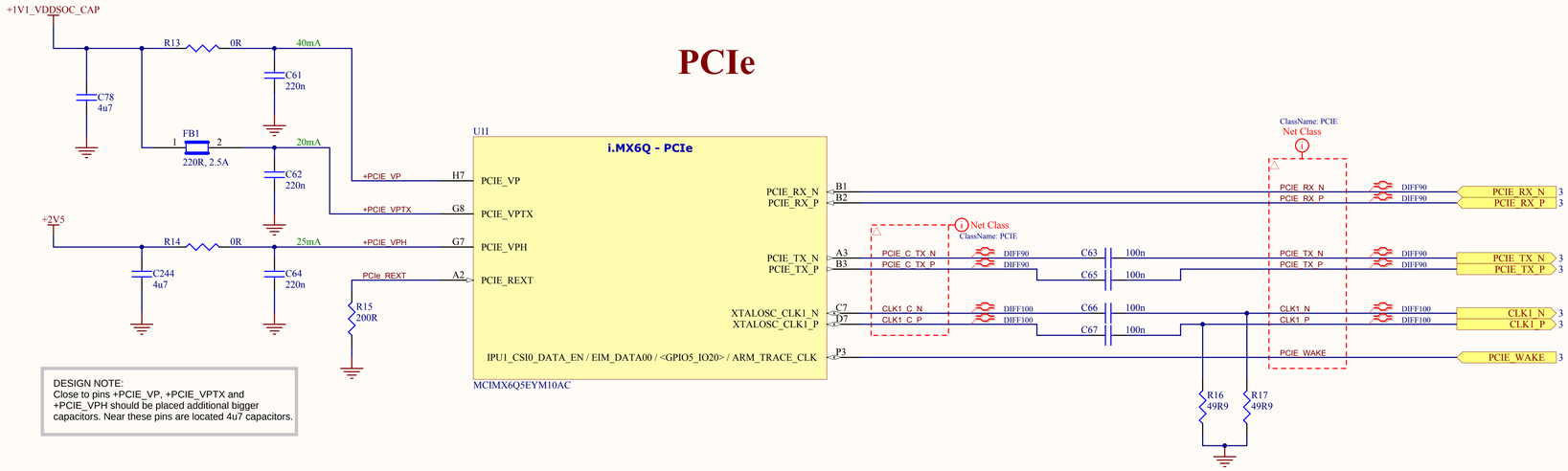
Title:	iMX6 Rex Module	Variant:	Prototype
Page Contents:	[04] - CPU - DDR3, DDR3 MEM.SchDoc		Checked by
Size:	DWG NO	Revision:	V1I1
Date:	27. 9. 2013	Sheet	4 of 20

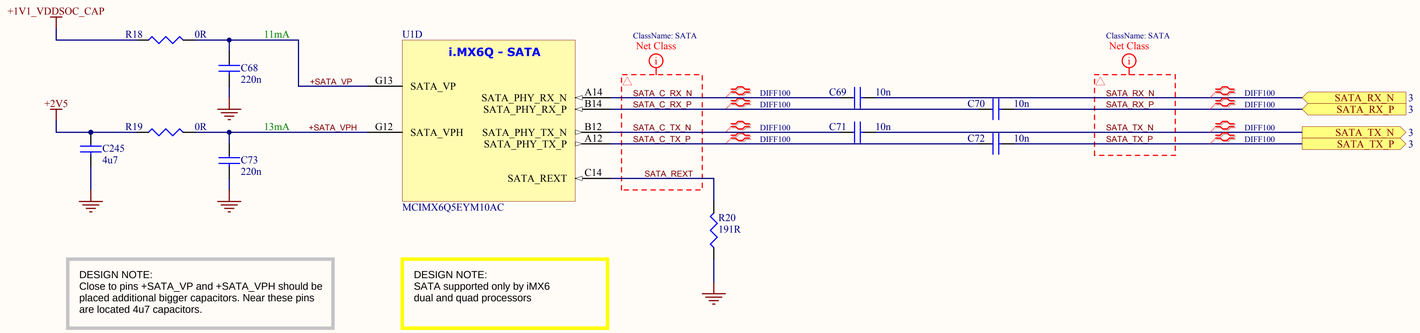
CPU - SATA, PCIe

PCIe



DESIGN NOTE:
Close to pins +PCIE_VP, +PCIE_VPTX and +PCIE_VPH should be placed additional bigger capacitors. Near these pins are located 4u7 capacitors.

SATA



DESIGN NOTE:
Close to pins +SATA_VP and +SATA_VPH should be placed additional bigger capacitors. Near these pins are located 4u7 capacitors.

DESIGN NOTE:
SATA supported only by iMX6 dual and quad processors

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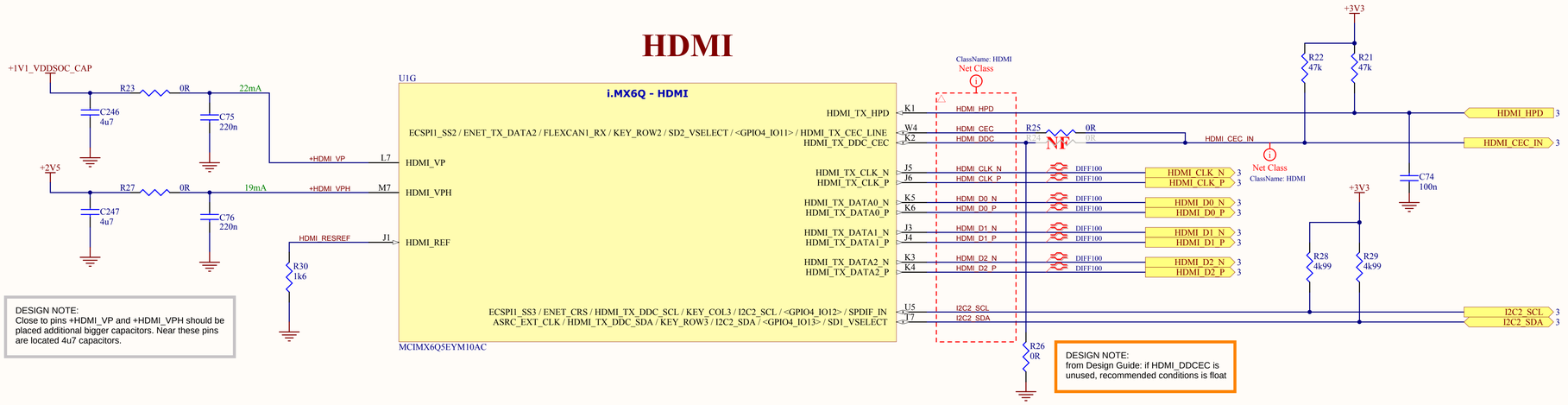
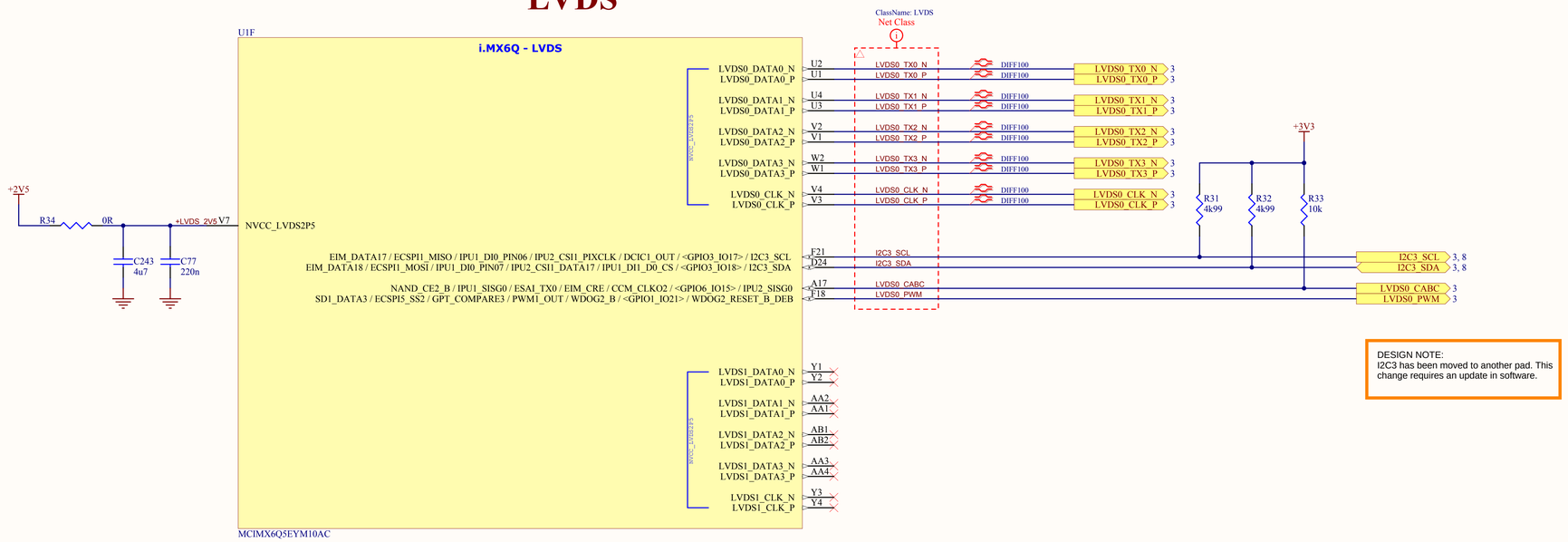
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[05] - CPU - PCIE, SATA.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 5 of 20	

CPU - HDMI, LVDS

HDMI



LVDS



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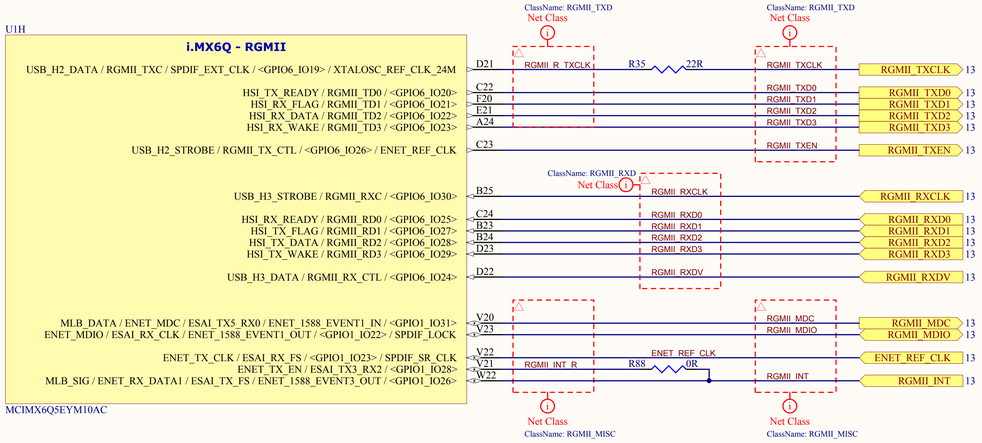
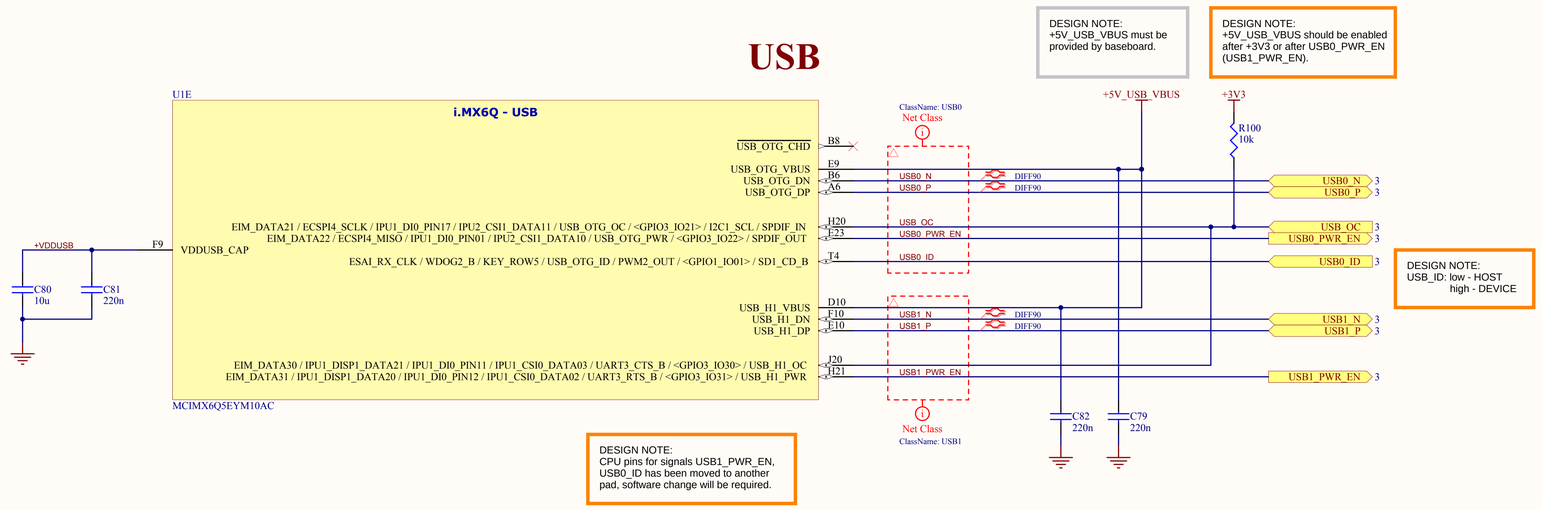
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[06] - CPU - HDMI, LVDS.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 6 of 20	

CPU - USB, ETHERNET

ETHERNET



USB



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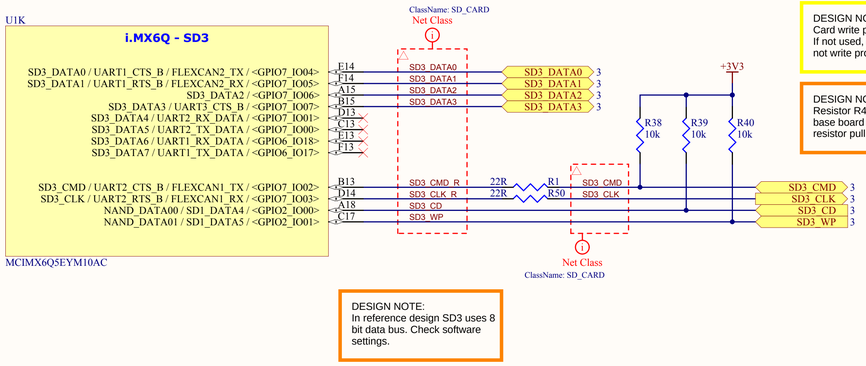
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[07] - CPU - USB, ETHERNET.SchDoc	Checked by	
Size:	DWG NO	Revision: V1I1	
Date:	27. 9. 2013	Sheet 7 of 20	

CPU - SPI, I2C, SD, MMC

SD-CARD



DESIGN NOTE:
Card detection pin:
If not used,tie to low to indicate there is a card attached.

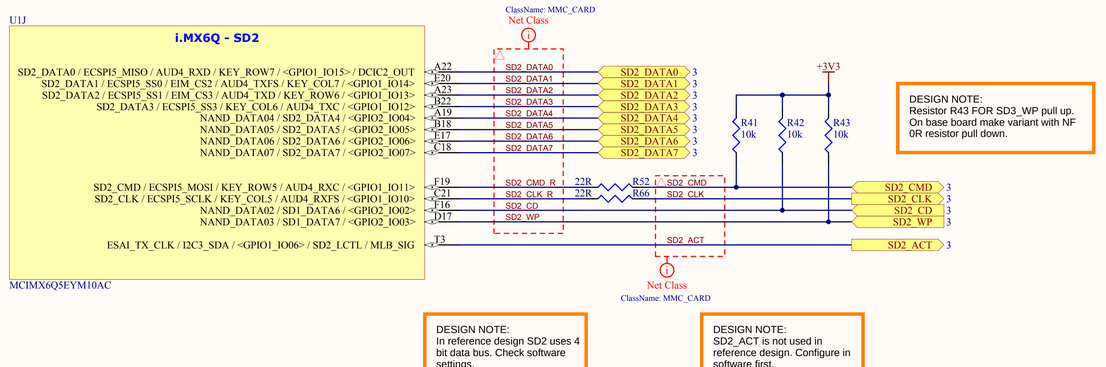
DESIGN NOTE:
Card write protect detect
If not used, tie to low to indicate it's not write protected.

DESIGN NOTE:
Resistor R40 for SD3_WP pull up. On base board make variant with NF 0R resistor pull down.

DESIGN NOTE:
In reference design SD3 uses 8 bit data bus. Check software settings.

DESIGN NOTE:
The maximum image size to load in SD/MMC boot is 32MB. (iMX6 reference manual)

MMC-CARD

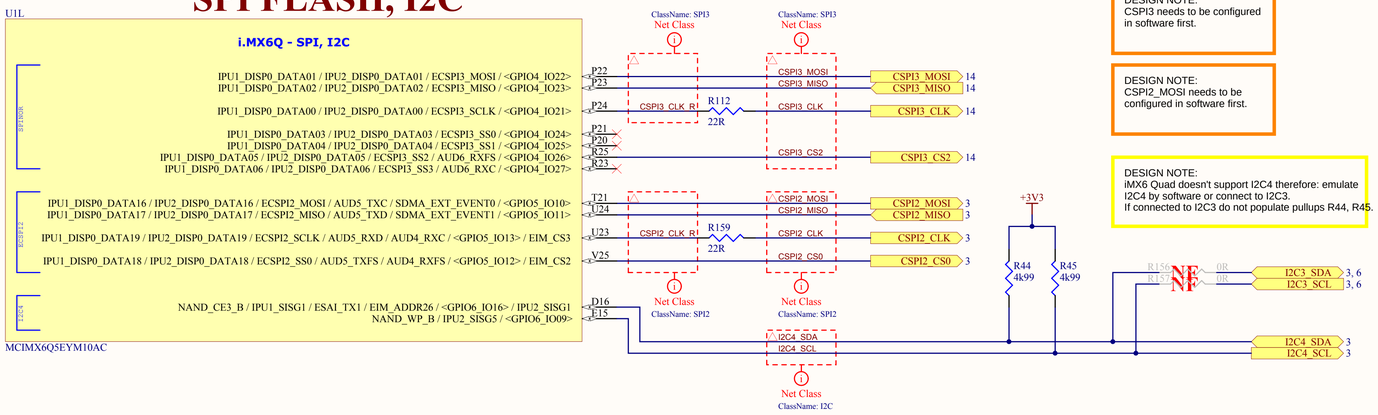


DESIGN NOTE:
Resistor R43 FOR SD3_WP pull up. On base board make variant with NF 0R resistor pull down.

DESIGN NOTE:
In reference design SD2 uses 4 bit data bus. Check software settings.

DESIGN NOTE:
SD2_ACT is not used in reference design. Configure in software first.

SPI FLASH, I2C



DESIGN NOTE:
CSPI3 needs to be configured in software first.

DESIGN NOTE:
CSPI2_MOSI needs to be configured in software first.

DESIGN NOTE:
iMX6 Quad doesn't support I2C4 therefore: emulate I2C4 by software or connect to I2C3.
If connected to I2C3 do not populate pullups R44, R45.

DESIGN NOTE:
I2C4 is not used in reference design. Configure in software first.

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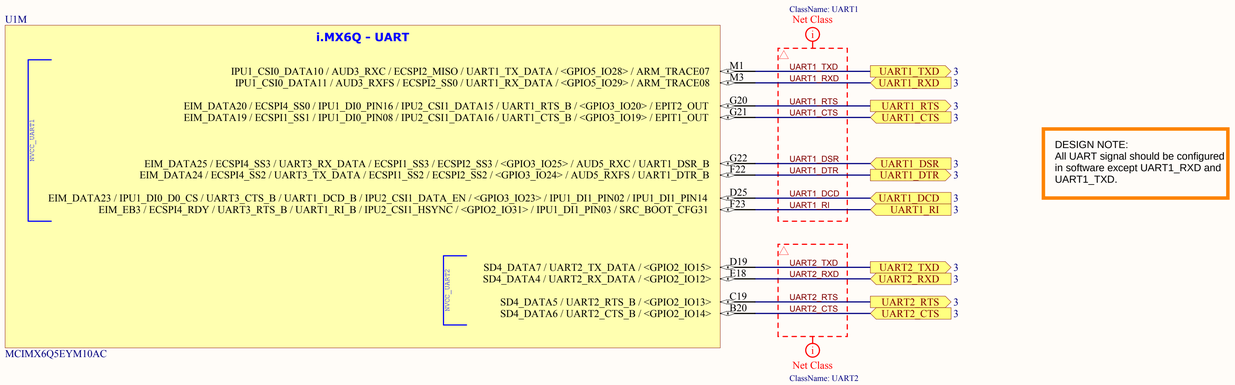
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[08] - CPU - SPI, I2C, SD, MMC.SchDoc	Checked by	
Size:	DWG NO	Revision:	V1I1
Date:	27. 9. 2013	Sheet 8 of	20

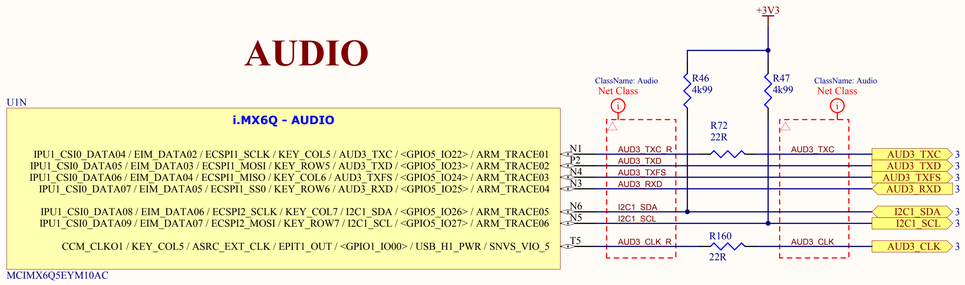
CPU - UART, AUDIO

UART



DESIGN NOTE:
All UART signal should be configured in software except UART1_RXD and UART1_TXD.

AUDIO



DESIGN NOTE:
In reference schematic I2C1 used by Audio has 1V8 level intefrace. IMX6 Rex Module has whole Audio intefrace on 3V3.

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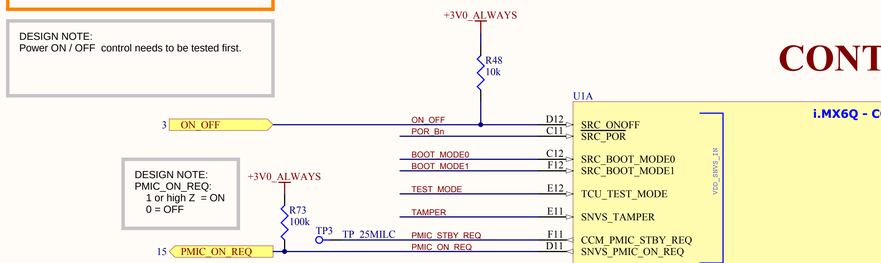
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[09] - CPU - UART, AUDIO.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 9 of 20	

CPU - JTAG, CONTROL

CONTROL

DESIGN NOTE:
from Design Guide: pullup not required
(ON / OFF).

DESIGN NOTE:
Power ON / OFF control needs to be tested first.

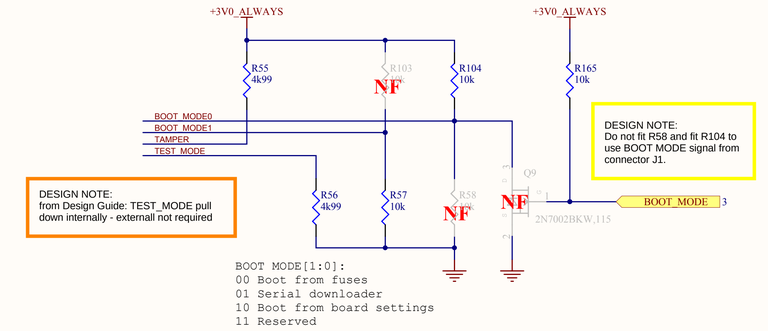


DESIGN NOTE:
Pins GPIO2_IO21 and 22 used to recognize version of the board. V1I1 - both pins pull down (00)

DESIGN NOTE:
USER_LED configure in software first.

DESIGN NOTE:
Resistor R37 from CPU_XTALO to GND is required to correct a known 24MHz slow starting issue present on some iMX6 part. Please refer to the i.MX 6 Processor Errata, issue # ERR005777 for more details.

DESIGN NOTE:
Per bulletin EB830, the i.MX6 processor may drive the 24 MHz crystal up to 250 uW. Freescale recommends following the guidelines contained in the bulletin.

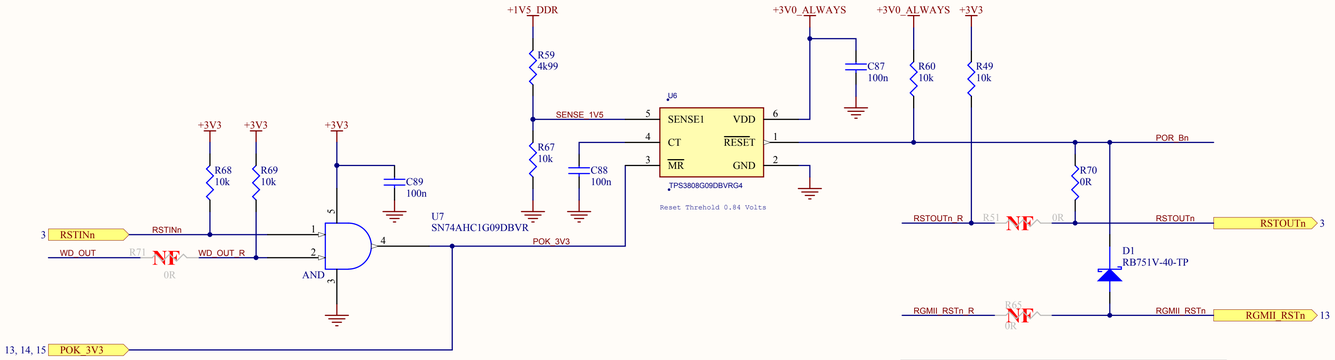


DESIGN NOTE:
from Design Guide: TEST_MODE pull down internally - externall not required

DESIGN NOTE:
Do not fit R58 and fit R104 to use BOOT MODE signal from connector J1.

DESIGN NOTE:
Default boot mode: 00 (eFuses).
Tamper will not be used. Test mode only for factory use.

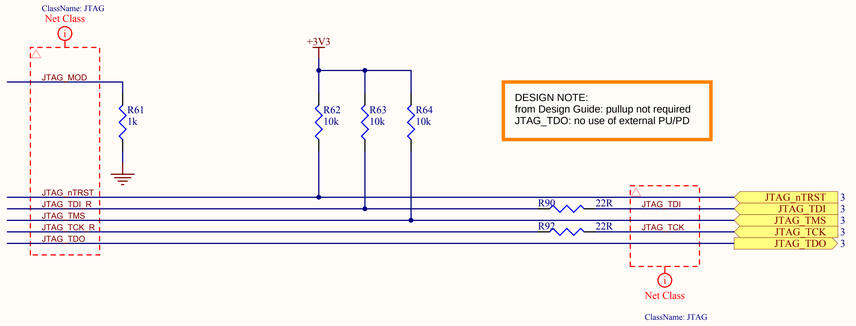
RESET



DESIGN NOTE:
The proper peripheral RESET (RSTOUTn) should be controlled by processor GPIO, but has to be supported by software first. Temporarily we use the POR to reset peripherals.

JTAG

DESIGN NOTE:
from Design Guide: JTAG_MOD use pulldown 1k or tie to GND



DESIGN NOTE:
from Design Guide: pullup not required
JTAG_TDO: no use of external PU/PD

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Title:	iMX6 Rex Module	Variant:	Prototype
Page Contents:	[10] - CPU - JTAG, CONTROL.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet	10 of 20

CPU - POWER

DESIGN NOTE:
Disable LDOs for VDDARM_IN, VDDARM23_IN and VDDSOC_IN.

DESIGN NOTE:
For testing purpuse only: Set +1V375 to +1.24V (when LDO VDDARM, VDDARM23 and VDDSOC are disabled) to lower power dissipation.

DESIGN NOTE:
The VDDARM_CAP and VDDARM23_CAP rails have been optimized for use with the i.MX 6 Quad and i.MX 6 DualLite processors. To achieve the lowest power mode (preventing internal leakage) when using the i.MX 6 Dual and the i.MX 6 SoloLite processors, VDDARM_CAP should be split from VDDARM23_CAP and the VDDARM23_CAP pins should be connected to ground. This can be done on a single board configured for use with all four processors by placing a Zero Ohm resistor between the VDDARM_CAP and VDDARM23_CAP rails (in place of the straight net connection). To use the board with different processors, populate the resistor when using Quad and DualLite processors and depopulate resistor when using Dual and SoloLite processors. When using Dual and SoloLite processors, depopulate the capacitors attached to VDDARM23_CAP pins and replace one of the capacitors with a zero Ohm resistor to short pins to ground. The configuration in this schematic will work with all four processors, but will not result in the most power optimized configuration for the i.MX 6 Dual and Solo processors.

LAYOUT NOTE:
It is critical that the bulk and decoupling capacitors placed on the VDDARM_CAP, VDDARM23_CAP, VDDSOC_CAP and VDDPU rails be placed directly underneath the processors. Development testing has shown that proper placement of the capacitors can reduce ripple on the voltage rails by as much as 50% compared to placing capacitors outside the physical boundaries of the processor. These will result in more stable processor operations.

MX6 power domains under-BGA decoupling (belongs to CPU pins on page 4)

+1V5_DDR
C157 220n, C158 220n, C159 220n, C160 220n, C161 220n, C162 220n
C167 220n, C168 220n, C169 220n, C170 220n, C171 220n, C172 22u, C173 22u

+1V375
2500mA (max 3920mA)
C90 220n, C91 220n, C92 220n, C93 220n, C94 220n, C95 220n, C96 22u
C107 220n, C108 220n, C109 220n, C110 220n, C111 22u
FB2 220R, 2.5A
1750mA (max 1890mA)
+1V375_VDDSOC_IN
C119 220n, C120 220n, C121 220n, C122 220n, C123 220n, C124 220n, C125 220n, C126 220n, C127 22u, C128 22u, C129 22u
+3V0_ALWAYS
100mA (max 125mA)
C136 220n, C137 22u
C142 220n

U1B
i.MX6Q - POWER

H14	VDDARM_IN_1	VDDARM_CAP_1 H13
J14	VDDARM_IN_2	VDDARM_CAP_2 J13
K14	VDDARM_IN_3	VDDARM_CAP_3 K13
L14	VDDARM_IN_4	VDDARM_CAP_4 L13
M14	VDDARM_IN_5	VDDARM_CAP_5 M13
N14	VDDARM_IN_6	VDDARM_CAP_6 N13
P14	VDDARM_IN_7	VDDARM_CAP_7 P13
R14	VDDARM_IN_8	VDDARM_CAP_8 R13
		VDDARM23_CAP_1 H11
K9	VDDARM23_IN_1	VDDARM23_CAP_2 J11
L9	VDDARM23_IN_2	VDDARM23_CAP_3 K11
M9	VDDARM23_IN_3	VDDARM23_CAP_4 L11
N9	VDDARM23_IN_4	VDDARM23_CAP_5 M11
P9	VDDARM23_IN_5	VDDARM23_CAP_6 N11
R9	VDDARM23_IN_6	VDDARM23_CAP_7 P11
T9	VDDARM23_IN_7	VDDARM23_CAP_8 R11
U9	VDDARM23_IN_8	
		VDDSOC_CAP_1 R10
H16	VDDSOC_IN_1	VDDSOC_CAP_2 T10
J16	VDDSOC_IN_2	VDDSOC_CAP_3 T13
K16	VDDSOC_IN_3	VDDSOC_CAP_4 T14
L16	VDDSOC_IN_4	VDDSOC_CAP_5 U10
M16	VDDSOC_IN_5	VDDSOC_CAP_6 U13
N16	VDDSOC_IN_6	VDDSOC_CAP_7 U14
P16	VDDSOC_IN_7	
R16	VDDSOC_IN_8	VDDPU_CAP_1 H17
T16	VDDSOC_IN_9	VDDPU_CAP_2 J17
U16	VDDSOC_IN_10	VDDPU_CAP_3 K17
		VDDPU_CAP_4 L17
H9	VDDHIGH_IN_1	VDDPU_CAP_5 M17
J9	VDDHIGH_IN_2	VDDPU_CAP_6 N17
		VDDPU_CAP_7 P17
		VDD_CACHE_CAP N12
		VDDHIGH_CAP_1 H10
G11	VDD_SNVS_IN	VDDHIGH_CAP_2 J10
		VDD_SNVS_CAP G9
A13	GND_1	NVCC_LCD P19
A25	GND_2	NVCC_CSI N7
A4	GND_3	NVCC_MIPI K7
A8	GND_4	NVCC_EIM0 K19
AA10	GND_5	NVCC_EIM1 L19
AA13	GND_6	NVCC_EIM2 M19
AA16	GND_7	NVCC_ENET R19
AA19	GND_8	NVCC_GPIO P7
AA22	GND_9	NVCC_PLL_OUT E8
AA7	GND_10	NVCC_RGMII G18
AB24	GND_11	NVCC_SD1 G16
AB3	GND_12	NVCC_SD2 G17
AD10	GND_13	NVCC_SD3 G14
AD13	GND_14	NVCC_NANDF G15
AD16	GND_15	NVCC_JTAG J7
AD19	GND_16	GPANAIO C8
AD22	GND_17	FA_ANA A5
AD4	GND_18	VDD_FA B5
AD7	GND_19	
AE1	GND_20	GND_80 T12
AE25	GND_21	GND_81 T15
B4	GND_22	GND_82 T17
C1	GND_23	GND_83 T19
C10	GND_24	GND_84 T8
C4	GND_25	GND_85 U11
C6	GND_26	GND_86 U12
D3	GND_27	GND_87 U15
D6	GND_28	GND_88 U17
D8	GND_29	GND_89 U8
E5	GND_30	GND_90 U19
E6	GND_31	GND_91 V8
E7	GND_32	GND_92 V19
F5	GND_33	GND_93 W3
F6	GND_34	GND_94 W7
F7	GND_35	GND_95 W8
F8	GND_36	GND_96 W9
G10	GND_37	GND_97 W10
G19	GND_38	GND_98 W11
G3	GND_39	GND_99 W12
H12	GND_40	GND_100 W13
H15	GND_41	GND_101 W15
H18	GND_42	GND_102 W16
H8	GND_43	GND_103 W17
J12	GND_44	GND_104 W18
J15	GND_45	GND_105 W19
J18	GND_46	GND_106 Y5
J2	GND_47	GND_107 Y24
J8	GND_48	
K10	GND_49	
K12	GND_50	
K15	GND_51	
K18	GND_52	
K8	GND_53	
L10	GND_54	
L12	GND_55	
L15	GND_56	
L18	GND_57	
L2	GND_58	
L5	GND_59	
L8	GND_60	
M10	GND_61	
M12	GND_62	
M15	GND_63	
M18	GND_64	
M8	GND_65	
N10	GND_66	
N15	GND_67	
N18	GND_68	
N8	GND_69	
P10	GND_70	
P12	GND_71	
P15	GND_72	
P18	GND_73	
P8	GND_74	
R12	GND_75	
R15	GND_76	
R17	GND_77	
R8	GND_78	
T11	GND_79	

MCIMX6Q5EYM10AC

+1V2_VDD_ARM_CAP
C97 220n, C98 220n, C99 220n, C100 220n, C101 22u
C102 220n, C103 220n, C104 220n, C105 220n, C106 22u
+1V1_VDDSOC_CAP
C112 220n, C113 220n, C114 220n, C115 220n, C116 220n, C117 220n, C118 22u
+VDDPU
C130 220n, C131 220n, C132 220n, C133 220n, C134 220n, C135 22u
{NVCC_CACHE_POWER}
C138 220n
+2V5_VDDHIGH_VPH
C139 10n, C140 220n, C141 22u
+VDD_SNVS_CAP
+3V3
C143 220n, C144 220n
+NVCC_CSI
+NVCC_MIPI
+3V3
C166 220n, C146 220n, C147 22u, C148 22u
+1V2_ETH
+1V375
NF R105 0R
NF R77 0R
+NVCC_ENET
+1V1_NVCC_PLL_OUT
+2V5
R80 0R
C150 220n, C151 22u
NF R79 0R
+3V3
C152 220n, C153 220n
+NVCC_RGMII
+3V3
C154 220n
+3V3
C163 220n
+3V3
C164 220n
+3V3
C165 220n
+3V3
C174 220n

DESIGN NOTE:
design guide: GPANAIO must be a no connect. VDD_FA and FA_ANA should be tied to GND.

DESIGN NOTE:
Measure +1V1_NVCC_PLL_OUT, if needed fit R77, R79.

DESIGN NOTE:
+1V1_NVCC_PLL_OUT: R77, R79, R105 for testing only.

DESIGN NOTE:
+NVCC_RGMII connected to 2V5 for RGMII 2V5 operation.

+3V3
+NVCC_CSI R76 0R
C145 220n
+2V5
+NVCC_MIPI R78 0R
C149 220n
+2V5
+NVCC_ENET R74 0R
C155 220n, C156 22u

DESIGN NOTE:
+NVCC_ENET connected to 2V5 to be able to easy connect cpu with ethernet phy (which is supplied from 2V5).

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Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[11] - CPU - POWER.SchDoc	Checked by	
Size:	DWG NO	Revision: V1I1	
Date:	27. 9. 2013	Sheet 11 of 20	

CPU - UNUSED PINS

U1O

i.MX6Q - UNUSED

A21	SD1_DATA0 / ECSPI5_MISO / GPT_CAPTURE1 / <GPIO1_IO16>	IPU1_DI0_PIN02 / IPU2_DI0_PIN02 / AUD6_TXD / <GPIO4_IO18>	N25
C20	SD1_DATA1 / ECSPI5_SS0 / PWM3_OUT / GPT_CAPTURE2 / <GPIO1_IO17>	IPU1_DI0_PIN03 / IPU2_DI0_PIN03 / AUD6_TXFS / <GPIO4_IO19>	N20
E19	SD1_DATA2 / ECSPI5_SS1 / GPT_COMPARE2 / PWM2_OUT / WDOG1_B / <GPIO1_IO19> / WDOG1_RESET_B_DEB	IPU1_DI0_PIN04 / IPU2_DI0_PIN04 / AUD6_RXD / SD1_WP / <GPIO4_IO20>	P25
		IPU1_DI0_PIN15 / IPU2_DI0_PIN15 / AUD6_TXC / <GPIO4_IO17>	N21
B21	SD1_CMD / ECSPI5_MOSI / PWM4_OUT / GPT_COMPARE1 / <GPIO1_IO18>	IPU1_DI0_DISP_CLK / IPU2_DI0_DISP_CLK / <GPIO4_IO16>	N19
D20	SD1_CLK / ECSPI5_SCLK / GPT_CLKIN / <GPIO1_IO20>		
		IPU1_CSI0_DATA12 / EIM_DATA08 / UART4_TX_DATA / <GPIO5_IO30> / ARM_TRACE09	M2
D18	SD4_DATA0 / NAND_DQS / <GPIO2_IO08>	IPU1_CSI0_DATA13 / EIM_DATA09 / UART4_RX_DATA / <GPIO5_IO31> / ARM_TRACE10	L1
B19	SD4_DATA1 / PWM3_OUT / <GPIO2_IO09>	IPU1_CSI0_DATA14 / EIM_DATA10 / UART5_TX_DATA / <GPIO6_IO00> / ARM_TRACE11	M4
F17	SD4_DATA2 / PWM4_OUT / <GPIO2_IO10>	IPU1_CSI0_DATA15 / EIM_DATA11 / UART5_RX_DATA / <GPIO6_IO01> / ARM_TRACE12	M5
A20	SD4_DATA3 / <GPIO2_IO11>	IPU1_CSI0_DATA16 / EIM_DATA12 / UART4_RTS_B / <GPIO6_IO02> / ARM_TRACE13	L4
		IPU1_CSI0_DATA17 / EIM_DATA13 / UART4_CTS_B / <GPIO6_IO03> / ARM_TRACE14	L3
B17	SD4_CMD / NAND_RE_B / UART3_TX_DATA / <GPIO7_IO09>	IPU1_CSI0_DATA18 / EIM_DATA14 / UART5_RTS_B / <GPIO6_IO04> / ARM_TRACE15	M6
E16	SD4_CLK / NAND_WE_B / UART3_RX_DATA / <GPIO7_IO10>	IPU1_CSI0_DATA19 / EIM_DATA15 / UART5_CTS_B / <GPIO6_IO05>	L6
		IPU1_CSI0_VSYNC / EIM_DATA01 / <GPIO5_IO21> / ARM_TRACE00	N2
D15	SD3_RESET / UART3_RTS_B / <GPIO7_IO08>	IPU1_CSI0_HSYNC / CCM_CLKO1 / <GPIO5_IO19> / ARM_TRACE_CTL	P4
		IPU1_CSI0_PIXCLK / <GPIO5_IO18> / ARM_EVENTO	P1
L20	<EIM_AD00> / IPU1_DISP1_DATA09 / IPU2_CSI1_DATA09 / GPIO3_IO00 / SRC_BOOT_CFG00		
J25	<EIM_AD01> / IPU1_DISP1_DATA08 / IPU2_CSI1_DATA08 / GPIO3_IO01 / SRC_BOOT_CFG01	ECSPI1_MOSI / ENET_TX_DATA3 / AUD5_TXD / KEY_ROW0 / UART4_RX_DATA / <GPIO4_IO07> / DCIC2_OUT	V6
L21	<EIM_AD02> / IPU1_DISP1_DATA07 / IPU2_CSI1_DATA07 / GPIO3_IO02 / SRC_BOOT_CFG02	ECSPI1_MISO / ENET_MDIO / AUD5_TXFS / KEY_COL1 / UART5_TX_DATA / <GPIO4_IO08> / SD1_VSELECT	J17
K24	<EIM_AD03> / IPU1_DISP1_DATA06 / IPU2_CSI1_DATA06 / GPIO3_IO03 / SRC_BOOT_CFG03		
L22	<EIM_AD04> / IPU1_DISP1_DATA05 / IPU2_CSI1_DATA05 / GPIO3_IO04 / SRC_BOOT_CFG04	ECSPI1_SCLK / ENET_RX_DATA3 / AUD5_TXC / KEY_COL0 / UART4_TX_DATA / <GPIO4_IO06> / DCIC1_OUT	W5
L23	<EIM_AD05> / IPU1_DISP1_DATA04 / IPU2_CSI1_DATA04 / GPIO3_IO05 / SRC_BOOT_CFG05		
K25	<EIM_AD06> / IPU1_DISP1_DATA03 / IPU2_CSI1_DATA03 / GPIO3_IO06 / SRC_BOOT_CFG06	ECSPI1_SS0 / ENET_COL / AUD5_RXD / KEY_ROW1 / UART5_RX_DATA / <GPIO4_IO09> / SD2_VSELECT	U6
L25	<EIM_AD07> / IPU1_DISP1_DATA02 / IPU2_CSI1_DATA02 / GPIO3_IO07 / SRC_BOOT_CFG07		
L24	<EIM_AD08> / IPU1_DISP1_DATA01 / IPU2_CSI1_DATA01 / GPIO3_IO08 / SRC_BOOT_CFG08	IPU1_DISP0_DATA07 / IPU2_DISP0_DATA07 / ECSPI3_RDY / <GPIO4_IO28>	R24
M21	<EIM_AD09> / IPU1_DISP1_DATA00 / IPU2_CSI1_DATA00 / GPIO3_IO09 / SRC_BOOT_CFG09		
M23	<EIM_AD10> / IPU1_DI1_PIN15 / IPU2_CSI1_DATA_EN / GPIO3_IO10 / SRC_BOOT_CFG10	IPU1_DISP0_DATA09 / IPU2_DISP0_DATA09 / PWM2_OUT / WDOG2_B / <GPIO4_IO30>	T25
M20	<EIM_AD11> / IPU1_DI1_PIN02 / IPU2_CSI1_HSYNC / GPIO3_IO11 / SRC_BOOT_CFG11	IPU1_DISP0_DATA10 / IPU2_DISP0_DATA10 / <GPIO4_IO31>	R21
M24	<EIM_AD12> / IPU1_DI1_PIN03 / IPU2_CSI1_VSYNC / GPIO3_IO12 / SRC_BOOT_CFG12	IPU1_DISP0_DATA11 / IPU2_DISP0_DATA11 / <GPIO5_IO05>	T23
M22	<EIM_AD13> / IPU1_DI1_D0_CS / GPIO3_IO13 / SRC_BOOT_CFG13	IPU1_DISP0_DATA12 / IPU2_DISP0_DATA12 / <GPIO5_IO06>	T24
N23	<EIM_AD14> / IPU1_DI1_D1_CS / GPIO3_IO14 / SRC_BOOT_CFG14	IPU1_DISP0_DATA13 / IPU2_DISP0_DATA13 / AUD5_RXFS / <GPIO5_IO07>	R20
N24	<EIM_AD15> / IPU1_DI1_PIN01 / IPU1_DI1_PIN04 / GPIO3_IO15 / SRC_BOOT_CFG15	IPU1_DISP0_DATA14 / IPU2_DISP0_DATA14 / AUD5_RXC / <GPIO5_IO08>	J25
		IPU1_DISP0_DATA15 / IPU2_DISP0_DATA15 / ECSPI1_SS1 / ECSPI2_SS1 / <GPIO5_IO09>	J22
J22	<EIM_ADDR18> / IPU1_DISP1_DATA13 / IPU2_CSI1_DATA13 / GPIO2_IO20 / SRC_BOOT_CFG18	IPU1_DISP0_DATA20 / IPU2_DISP0_DATA20 / ECSPI1_SCLK / AUD4_TXC / <GPIO5_IO14>	U22
G25	<EIM_ADDR19> / IPU1_DISP1_DATA14 / IPU2_CSI1_DATA14 / GPIO2_IO19 / SRC_BOOT_CFG19	IPU1_DISP0_DATA21 / IPU2_DISP0_DATA21 / ECSPI1_MOSI / AUD4_TXD / <GPIO5_IO15>	J20
H22	<EIM_ADDR20> / IPU1_DISP1_DATA15 / IPU2_CSI1_DATA15 / GPIO2_IO18 / SRC_BOOT_CFG20	IPU1_DISP0_DATA22 / IPU2_DISP0_DATA22 / ECSPI1_MISO / AUD4_TXFS / <GPIO5_IO16>	V24
H23	<EIM_ADDR21> / IPU1_DISP1_DATA16 / IPU2_CSI1_DATA16 / GPIO2_IO17 / SRC_BOOT_CFG21	IPU1_DISP0_DATA23 / IPU2_DISP0_DATA23 / ECSPI1_SS0 / AUD4_RXD / <GPIO5_IO17>	W24
F24	<EIM_ADDR22> / IPU1_DISP1_DATA17 / IPU2_CSI1_DATA17 / GPIO2_IO16 / SRC_BOOT_CFG22		
J23	<EIM_ADDR23> / IPU1_DISP1_DATA18 / IPU2_CSI1_DATA18 / IPU2_SISG3 / IPU1_SISG3 / GPIO6_IO06 / SRC_BOOT_CFG23		
F25	<EIM_ADDR24> / IPU1_DISP1_DATA19 / IPU2_CSI1_DATA19 / IPU2_SISG2 / IPU1_SISG2 / GPIO5_IO04 / SRC_BOOT_CFG24	NAND_CE0_B / <GPIO6_IO11>	F15
		NAND_CE1_B / SD4_VSELECT / SD3_VSELECT / <GPIO6_IO14>	C16
C25	EIM_DATA16 / ECSPI1_SCLK / IPU1_DI0_PIN05 / IPU2_CSI1_DATA18 / HDMI_TX_DDC_SDA / <GPIO3_IO16> / I2C2_SDA	NAND_ALE / SD4_RESET / <GPIO6_IO08>	A16
		NAND_CLE / IPU2_SISG4 / <GPIO6_IO07>	C15
E24	EIM_DATA26 / IPU1_DI1_PIN11 / IPU1_CSI0_DATA01 / IPU2_CSI1_DATA14 / UART2_TX_DATA / <GPIO3_IO26> / IPU1_SISG2 / IPU1_DISP1_DATA22	NAND_READY / IPU2_DI0_PIN01 / <GPIO6_IO10>	B16
E23	EIM_DATA27 / IPU1_DI1_PIN13 / IPU1_CSI0_DATA00 / IPU2_CSI1_DATA13 / UART2_RX_DATA / <GPIO3_IO27> / IPU1_SISG3 / IPU1_DISP1_DATA23		
G23	EIM_DATA28 / I2C1_SDA / ECSPI4_MOSI / IPU2_CSI1_DATA12 / UART2_CTS_B / <GPIO3_IO28> / IPU1_EXT_TRIG / IPU1_DI0_PIN13		
J19	EIM_DATA29 / IPU1_DI1_PIN15 / ECSPI4_SS0 / UART2_RTS_B / <GPIO3_IO29> / IPU2_CSI1_VSYNC / IPU1_DI0_PIN14	MLB_SIG_N	A9
		MLB_SIG_P	B9
N22	<EIM_BCLK> / IPU1_DI1_PIN16 / GPIO6_IO31	MLB_DATA_N	B10
K22	<EIM_LBA> / IPU1_DI1_PIN17 / ECSPI2_SS1 / GPIO2_IO27 / SRC_BOOT_CFG26	MLB_DATA_P	A10
J24	<EIM_OE> / IPU1_DI1_PIN07 / ECSPI2_MISO / GPIO2_IO25		
K20	<EIM_RW> / IPU1_DI1_PIN08 / ECSPI2_SS0 / GPIO2_IO26 / SRC_BOOT_CFG29	MLB_CLK_N	A11
M25	<EIM_WAIT> / EIM_DTACK_B / GPIO5_IO00 / SRC_BOOT_CFG25	MLB_CLK_P	B11
K21	<EIM_EB0> / IPU1_DISP1_DATA11 / IPU2_CSI1_DATA11 / CCM_PMIC_READY / GPIO2_IO28 / SRC_BOOT_CFG27	CSI_DATA0_N	E4
K23	<EIM_EB1> / IPU1_DISP1_DATA10 / IPU2_CSI1_DATA10 / GPIO2_IO29 / SRC_BOOT_CFG28	CSI_DATA0_P	E3
E22	EIM_EB2 / ECSPI1_SS0 / IPU2_CSI1_DATA19 / HDMI_TX_DDC_SCL / <GPIO2_IO30> / I2C2_SCL / SRC_BOOT_CFG30		
		CSI_DATA1_N	D1
		CSI_DATA1_P	D2
H24	<EIM_CS0> / IPU1_DI1_PIN05 / ECSPI2_SCLK / GPIO2_IO23		
J21	<EIM_CS1> / IPU1_DI1_PIN06 / ECSPI2_MOSI / GPIO2_IO24	CSI_DATA2_N	E1
		CSI_DATA2_P	E2
W20	MLB_CLK / ENET_TX_DATA1 / ESAI_TX2_RX3 / ENET_1588_EVENT0_IN / <GPIO1_IO29>		
		CSI_DATA3_N	F2
R1	ESAI_TX0 / ENET_1588_EVENT3_IN / CCM_PMIC_READY / SDMA_EXT_EVENT0 / SPDIF_OUT / <GPIO7_IO12>	CSI_DATA3_P	F1
P6	ESAI_TX1 / ENET_RX_CLK / SD3_VSELECT / SDMA_EXT_EVENT1 / ASRC_EXT_CLK / <GPIO7_IO13> / SNVS_VIO_5_CTL		
R4	ESAI_TX2_RX3 / KEY_ROW7 / CCM_CLKO1 / <GPIO1_IO05> / I2C3_SCL / ARM_EVENTI	CSI_CLK0_N	F4
R2	ESAI_TX3_RX2 / ENET_1588_EVENT2_IN / ENET_REF_CLK / SD1_LCTL / SPDIF_IN / <GPIO7_IO11> / I2C3_SDA / JTAG_DE_B	CSI_CLK0_P	F3
R3	ESAI_TX4_RX1 / ECSPI5_RDY / EPIT1_OUT / FLEXCAN1_TX / UART2_TX_DATA / <GPIO1_IO07> / SPDIF_LOCK / USB_OTG_HOST_MODE		
R5	ESAI_TX5_RX0 / XTALOSC_REF_CLK_32K / EPIT2_OUT / FLEXCAN1_RX / UART2_RX_DATA / <GPIO1_IO08> / SPDIF_SR_CLK / USB_OTG_PWR_CTL_WAKE	CSI_REXT	D4
R6	ESAI_TX_HF_CLK / KEY_COL7 / <GPIO1_IO04> / SD2_CD_B		
T7	ESAI_RX_FS / WDOG1_B / KEY_COL6 / CCM_REF_EN_B / PWM1_OUT / <GPIO1_IO09> / SD1_WP		
R7	ESAI_RX_HF_CLK / I2C3_SCL / XTALOSC_REF_CLK_24M / CCM_CLKO2 / <GPIO1_IO03> / USB_H1_OC / MLB_CLK	DSI_DATA0_N	G2
		DSI_DATA0_P	G1
W23	USB_OTG_ID / ENET_RX_ER / ESAI_RX_HF_CLK / SPDIF_IN / ENET_1588_EVENT2_OUT / <GPIO1_IO24>	DSI_DATA1_N	H2
P5	KEY_COL5 / ENET_1588_EVENT0_OUT / SPDIF_OUT / CCM_CLKO1 / ECSPI1_RDY / <GPIO4_IO05> / ENET_TX_ER	DSI_DATA1_P	H1
W6	ECSPI1_SS1 / ENET_RX_DATA2 / FLEXCAN1_TX / KEY_COL2 / ENET_MDC / <GPIO4_IO10> / USB_H1_PWR_CTL_WAKE		
U20	ENET_TX_DATA0 / ESAI_TX4_RX1 / <GPIO1_IO30>	DSI_CLK0_N	H3
W21	ENET_RX_DATA0 / ESAI_TX_HF_CLK / SPDIF_OUT / <GPIO1_IO27>	DSI_CLK0_P	H4
T6	FLEXCAN2_TX / IPU1_SISG4 / USB_OTG_OC / KEY_COL4 / UART5_RTS_B / <GPIO4_IO14>		
V5	FLEXCAN2_RX / IPU1_SISG5 / USB_OTG_PWR / KEY_ROW4 / UART5_CTS_B / <GPIO4_IO15>	DSI_REXT	G4

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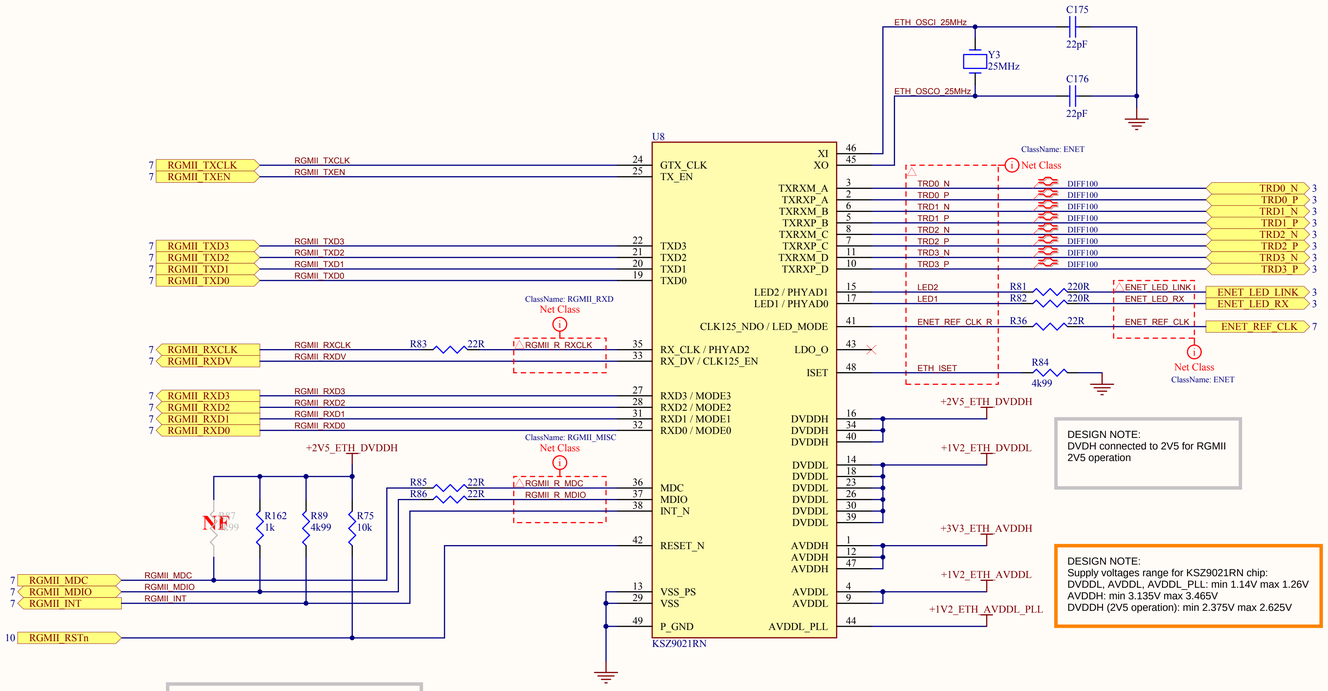
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[12] - CPU - UNUSED.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 12 of	20

ETHERNET PHY



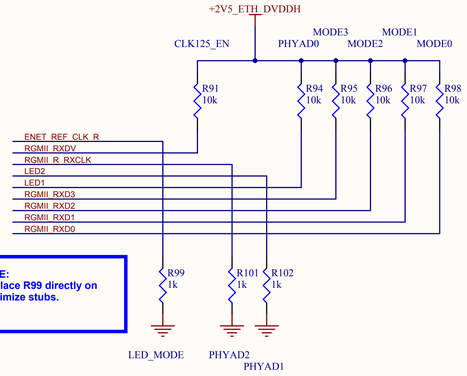
DESIGN NOTE:
DVDH connected to 2V5 for RGMII 2V5 operation

DESIGN NOTE:
Supply voltages range for KSZ9021RN chip:
DVDDL, AVDDL, AVDDL_PLL: min 1.14V max 1.26V
AVDDH: min 3.135V max 3.465V
DVDDH (2V5 operation): min 2.375V max 2.625V

DESIGN NOTE:
All RGMII signal from cpu are 2V5 level, therefore used pull up to 2V5.

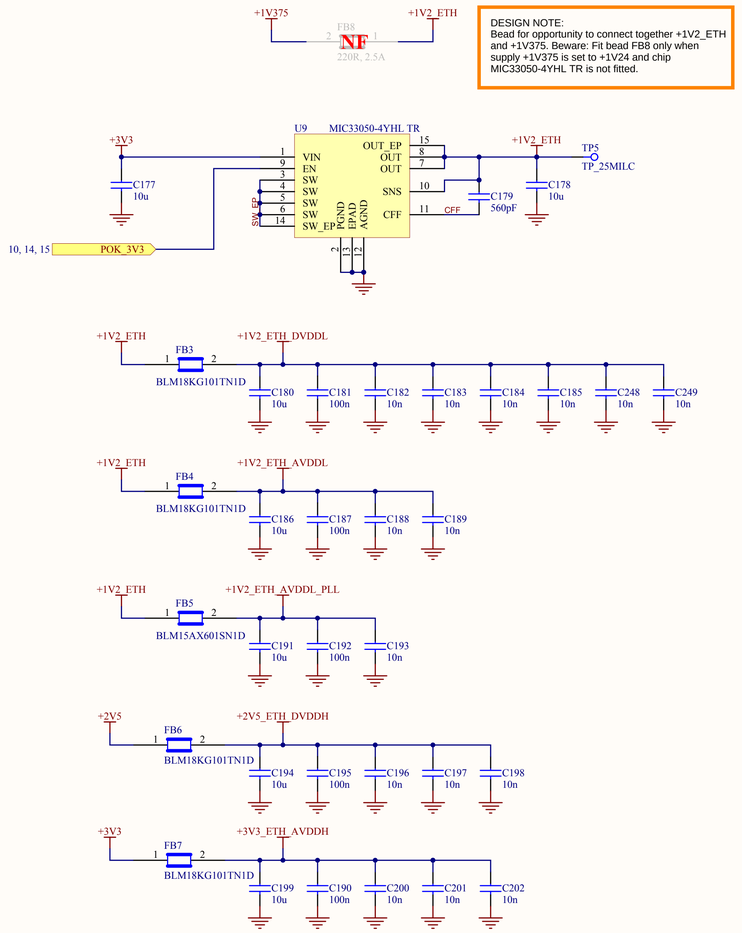
DESIGN NOTE:
Measure signals RGMII_MDC, RGMII_MDIO, RGMII_INT (if they are 2V5).

DESIGN NOTE:
Default Ethernet strapping options:
PHYAD2-0: PHY address 0x1
MODE3-0: RGMII mode (10/100/1000 half/full duplex)
CLK125_EM: ref. clock enable
LED_MODE: tri-color dual mode



LAYOUT NOTE:
Be sure you place R99 directly on the net to minimize stubs.

DESIGN NOTE:
Bead for opportunity to connect together +1V2_ETH and +1V375. Beware: Fit bead FB8 only when supply +1V375 is set to +1V24 and chip MIC33050-4YHL TR is not fitted.



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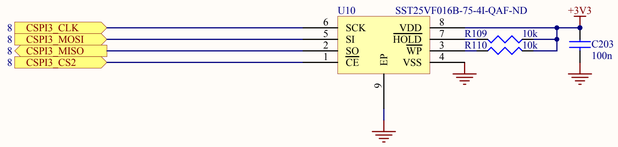
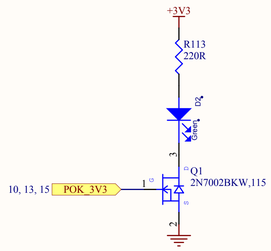
Title:	iMX6 Rex Module	Variant:	Prototype
Page Contents:	[13] - ETHERNET PHY.SchDoc		Checked by
Size:	DWG NO	Revision:	V1I1
Date:	27. 9. 2013	Sheet	13 of 20

SPI FLASH, LED

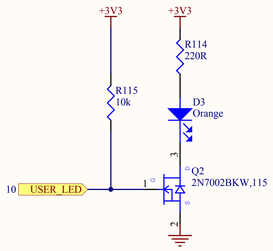
SPI NOR FLASH



POWER LED



USER DEFINED LED



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Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[14] - SPI FLASH, LEDS.SchDoc	Checked by	
Size:	DWG NO	Revision: V1I1	
Date:	27. 9. 2013	Sheet 14 of 20	

POWER +3.3V, +1.375V, +3.0_ALWAYS CON

DESIGN NOTE:
+3.3V / max 5A
(Required 2A)

DESIGN NOTE:
+1.375V / max 5.8A
(Required 4.25A)

DESIGN NOTE:
voltage created by voltage divider
connected to 3V3
REFIN2=3V3*10K/(10K+14K)=1.375V

DESIGN NOTE:
+3.0V / max 500mA
(Required 10mA)

DESIGN NOTE:
Voltage treeshold on FB pin Vref = 800mv

DESIGN NOTE:
resistor values for output voltage 3V0:
R138=R139*(Vout/Vref-1)=120k*(3.0/0.8-1)=330k
backward control:
Vout=Vref*(R138+R139)/R139=0.8*(330k+120k)/120k=3V

Note:
LDORFIN TIED TO GND = LDO 5V
LDORFIN TIED TO VCC = LDO 3.3V

POK
HIGH: POWER IS OK

TON
GND:400kHz/500kHz
NC:400kHz/300kHz
VCC:200kHz/300kHz

SET OUT1
VOTLAGE
TO 3.3V

SET OUT2
VOTLAGE
TO 1V375

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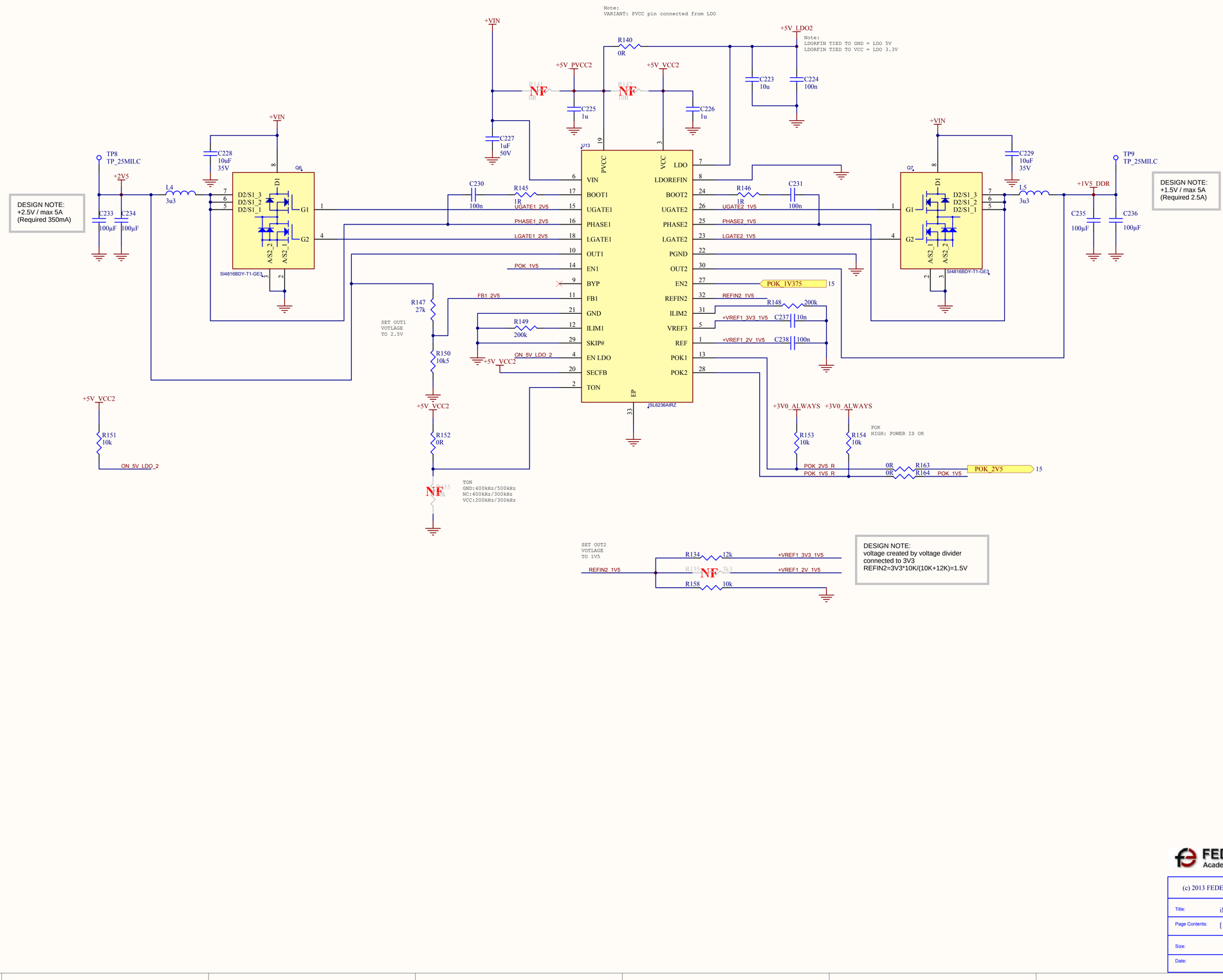
Title:	iMX6 Rex Module	Variant:	Prototype
Page Contents:	[15] - PWR 3V3, 1V375.SchDoc		Checked by
Size:	DWG NO	Revision:	V1I1
Date:	27. 9. 2013	Sheet	15 of 20

POWER +2.5V, +1.5V CON



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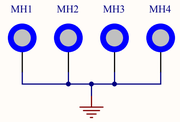
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[16] - PWR 2V5, 1V5.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 16 of 20	

MECHANICAL

TESTPOINT

MOUNTING HOLES



Mounting holes 5mm pad 2,2mm drill
BOARD MOUNTING HOLES - ONE IN EACH CORNER

FIDUCIALS

PCB

PCB1

iMX6 Rex V1I1 PCB

FIRMWARE

FIRMWARE_FOR_U10

iMX6_REX_uBOOT 1.0

LICENCE

ORIGINAL AUTHOR: FEDEVEL 2013
WEBSITE: http://www.iMX6Rex.com

****

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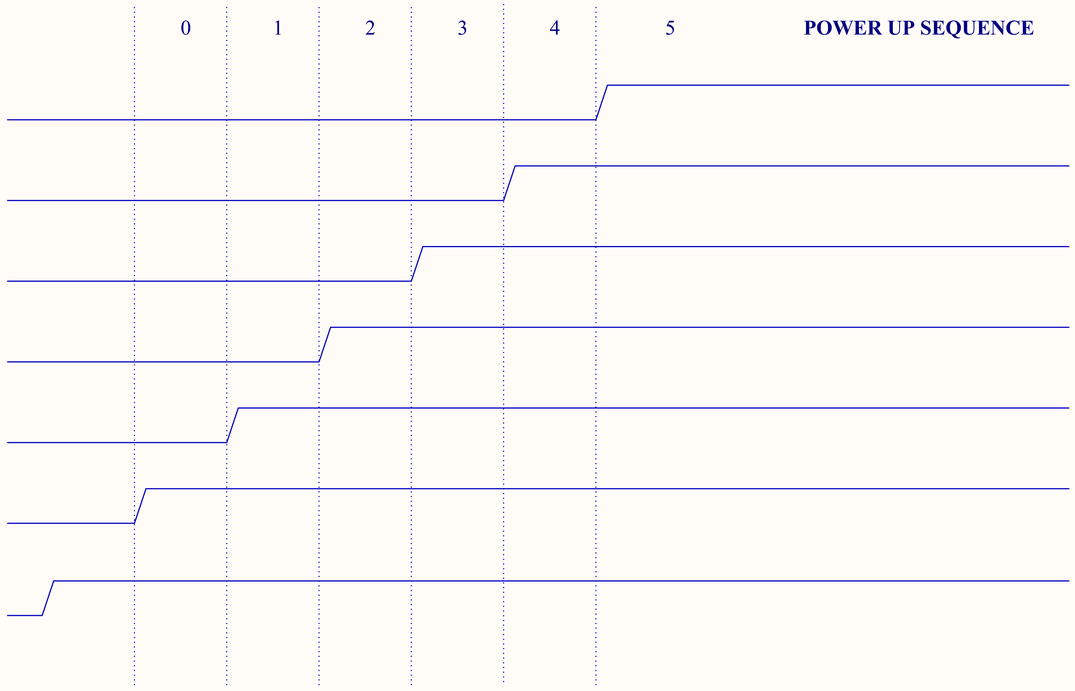
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[17] - MECH.SchDoc	Checked by	
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 17 of 20	

CPU - POWER SEQUENCING

OTHER POWERS	LEVEL	FROM	USED BY
+USB_VBUS	5V	connector	cpu
+DDR_VREF	0V75	+1V5_DDR	ref. for DDR memories, gen. with volt. divider
+1V2_VDD_ARM_CAP	1V2	iMX	cpu, core caps
+1V1_VDDSOC_CAP	1V1	iMX	core caps, cpu-sata, cpu-pcie, cpu-hdmi

CONTROLED BY	NAME	LEVEL	USED BY
POK_3V3	+1V2_ETH	1V2	ethernet phy
POK_2V5	+3V3	3V3	cpu, pull up
POK_1V5	+2V5	2V5	cpu, ethernet phy
POK_1V375	+1V5_DDR	1V5	cpu, memory
EN_1V375	+1V375	1V375	cpu, cpu core voltages
+VIN	+3V0_ALWAYS	3V0	cpu, supervisor, pull up
	+VIN	4.75V-25V	switching power supplies



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Title: iMX6 Rex Module	Variant: Prototype	
Page Contents: [18] - POWER SEQUENCING.SchDoc	Checked by	
Size:	DWG NO	Revision: V1I1
Date: 27. 9. 2013	Sheet 18 of 20	

DOC: REVISION HISTORY

01-AUG-2013 **Some HDMI and Ethernet signals swapped on J1**

19-AUG-2013 **Signals for SPI FLASH has been moved to CSPI3**

Added additional capacitors to +2V5 and +1V1_VDDSOC_CAP

21-AUG-2013 **Added resistor from CPU_XTALO to GND**

I2C3_SDA and I2C3_SCL has been moved to another CPU pins

22-AUG-2013 **Always powered voltage change level to 3V0 - supply voltage +3V0_ALWAYS**

Added bead to connect together +1V2_ETH and +1V375 (Only for testing purpose).

23-AUG-2013 **Added resistor to connect SLEEP pin of TPS62175DQCT to +3V0_ALWAYS.**

27-AUG-2013 **On connector J1 added BOOT_MODE signal to select boot source.**

CLOCKS (CPU & PCIE)

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Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	[19] - DOC REVISION HISTORY.SchDoc	Checked by	
Size:	DWG NO	Revision: V111	
Date:	27. 9. 2013	Sheet 19 of 20	

[01] - COVER PAGE.SchDoc
[01] - COVER PAGE.SchDoc

[02] - BLOCK DIAGRAM.SchDoc
[02] - BLOCK DIAGRAM.SchDoc

[03] - CONNECTORS.SchDoc
[03] - CONNECTORS.SchDoc

[04] - CPU - DDR3, DDR3 MEM.SchDoc
[04] - CPU - DDR3, DDR3 MEM.SchDoc

[05] - CPU - PCIE, SATA.SchDoc
[05] - CPU - PCIE, SATA.SchDoc

[06] - CPU - HDMI, LVDS.SchDoc
[06] - CPU - HDMI, LVDS.SchDoc

[07] - CPU - USB, ETHERNET.SchDoc
[07] - CPU - USB, ETHERNET.SchDoc

[08] - CPU - SPI, I2C, SD, MMC.SchDoc
[08] - CPU - SPI, I2C, SD, MMC.SchDoc

TEMPLATE NOTES

Set Project Parameters

1) Go to Project -> Project Options -> Parameters
2) Set Company, Project and VersionRevision

Mark Not Fitted Components as
NF

Net Class Example

Differential signal example

TITLE Examples (You can change the color to reflect your company color)

PAGE TITLE

Peripheral / Group of component title

Smaller Ttitle

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.

PRELIMINARY - Close to final schematic.

CHECKED - There should not be any mistakes. Tell the engineer if you find one.

RELEASED - A board with this schematic has been sent to production.

[09] - CPU - UART, AUDIO.SchDoc
[09] - CPU - UART, AUDIO.SchDoc

[10] - CPU - JTAG, CONTROL.SchDoc
[10] - CPU - JTAG, CONTROL.SchDoc

[11] - CPU - POWER.SchDoc
[11] - CPU - POWER.SchDoc

[12] - CPU - UNUSED.SchDoc
[12] - CPU - UNUSED.SchDoc

[13] - ETHERNET PHY.SchDoc
[13] - ETHERNET PHY.SchDoc

[14] - SPI FLASH, LEDS.SchDoc
[14] - SPI FLASH, LEDS.SchDoc

[15] - PWR 3V3, 1V375.SchDoc
[15] - PWR 3V3, 1V375.SchDoc

[16] - PWR 2V5, 1V5.SchDoc
[16] - PWR 2V5, 1V5.SchDoc

[17] - MECH.SchDoc
[17] - MECH.SchDoc

[18] - POWER SEQUENCING.SchDoc
[18] - POWER SEQUENCING.SchDoc

[19] - DOC REVISION HISTORY.SchDoc
[19] - DOC REVISION HISTORY.SchDoc

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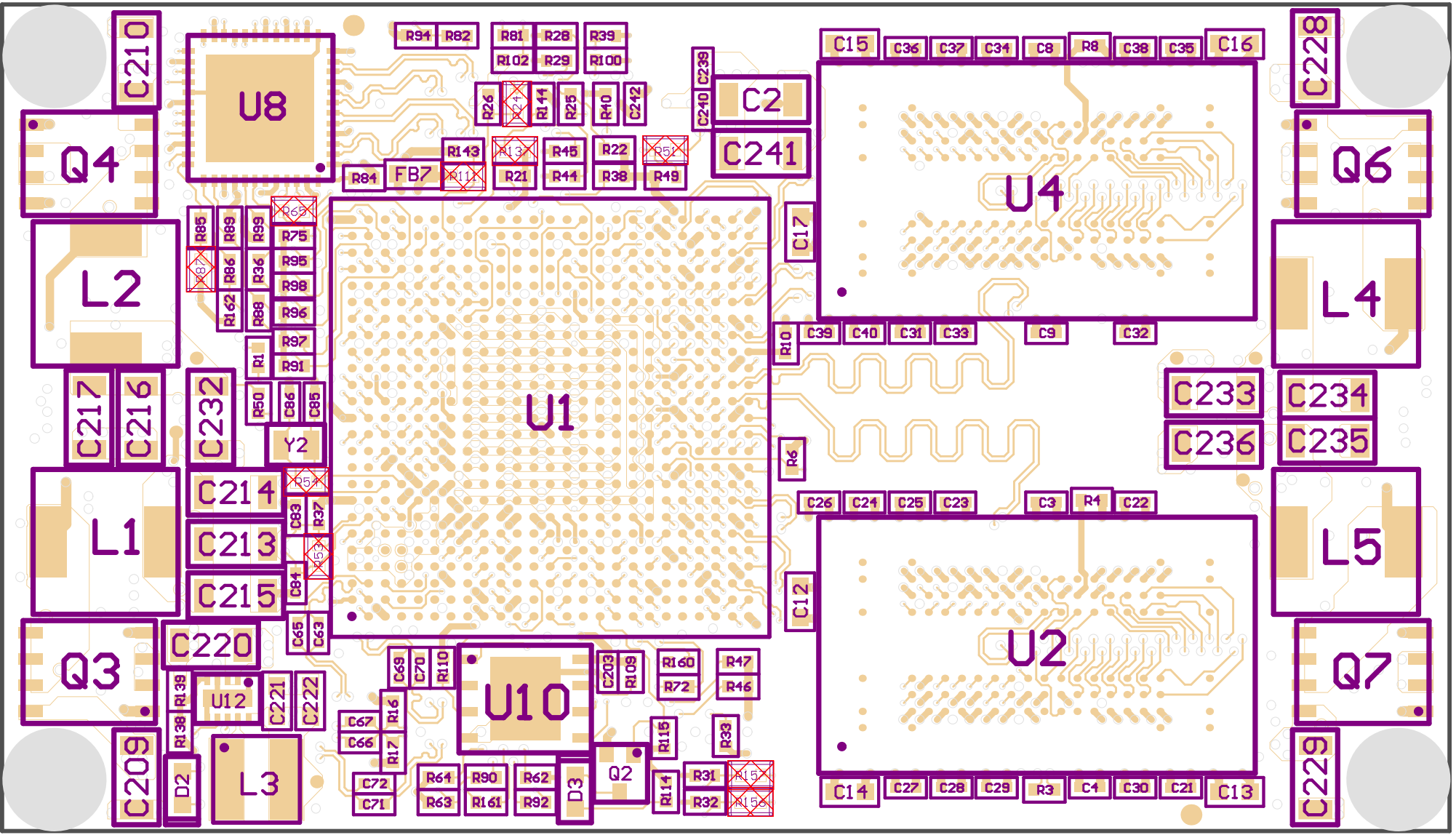
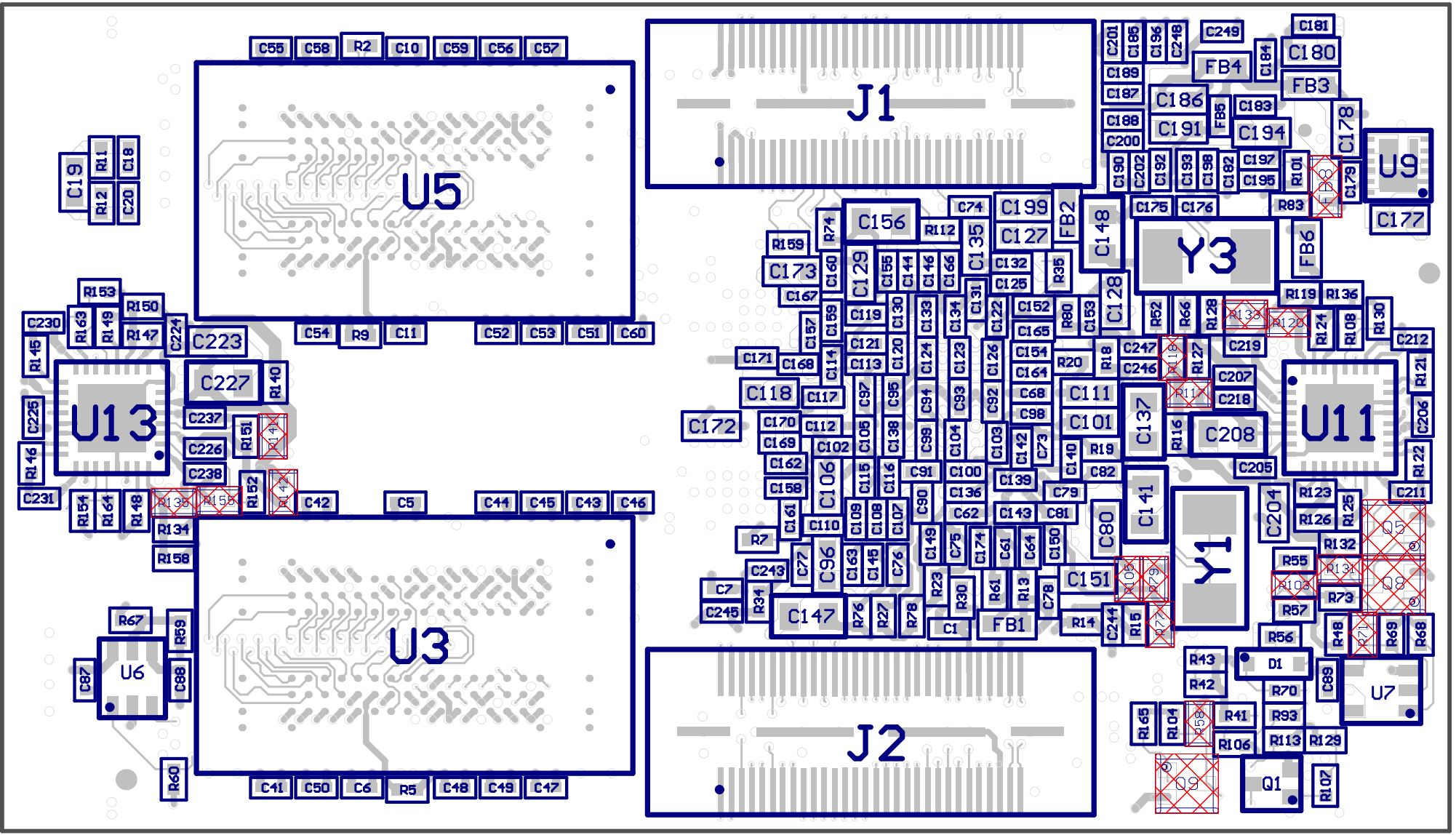
Title:	iMX6 Rex Module	Variant: Prototype	
Page Contents:	iMX6 Rex_V1I1 Project.SchDoc		Checked by
Size:	DWG NO		Revision: V1I1
Date:	27. 9. 2013	Sheet 20 of 20	

Assembly TOP of iMX6 Rex Module V1I1

Prototype



Assembly BOTTOM of iMX6 Rex Module V1I1

Prototype