Document identifier: IMX8MDQLQHDG
Rev. 4, 04/2021

i.MX 8MDQLQ Hardware Developer's Guide

Contents

Chapter 1
Overview

This document aims to help hardware engineers design and test the i.MX 8MDQLQ series processor. It gives examples on board layout, design checklists to ensure first-pass success, and solutions to avoid board bring-up problems.

Engineers should understand board layouts and board hardware terminology.

This guide is released with relevant device-specific hardware documentation such as datasheets, reference manuals, and application notes. All these documents are available on i.MX8M.

1.1 Device supported

This guide supports the i.MX 8MDQLQ (17 × 17 mm package).

1.2 Essential references

This guide is supplementary to the i.MX 8MDQLQ series chip reference manuals and data sheets. For reflow profile and thermal limits during soldering, see *General Soldering Temperature Process Guidelines* (document *AN3300*). These documents are available on i.MX8M.

1.3 Supplementary references

1.3.1 General information

The following documents introduce the Arm® processor architecture and computer architecture.

- For information about the Arm Cortex®-A35 processor, see Cortex-A35.
- For information about the Arm Cortex-A53 processor, see Cortex-A53
- For information about the Arm Cortex-A72 processor, see Cortex-A72
- For information about the Arm Cortex-M4F processor, see Cortex-M4
- *Computer Architecture: A Quantitative Approach (Fourth Edition)*, by John L. Hennessy and David A. Patterson
- *Computer Organization and Design: The Hardware/Software Interface (Second Edition)*, by David A. Patterson and John L. Hennessy

The following documentation introduces the high-speed board design:

- *Right the First Time- A Practical Handbook on High Speed PCB and System Design - Volumes I & II*, by Lee W. Ritchey (Speeding Edge) - ISBN 0-9741936- 0-72
- *Signal and Power Integrity Simplified (2nd Edition)*, by Eric Bogatin (Prentice Hall)- ISBN 0-13- 703502-0
- *High Speed Digital Design- A Handbook of Black Magic*, by Howard W. Johnson & Martin Graham (Prentice Hall) - ISBN 0-13-395724-1
- *High Speed Signal Propagation- Advanced Black Magic*, by Howard W. Johnson & Martin Graham - (Prentice Hall) - ISBN 0-13-084408-X
- *High Speed Digital System Design- A handbook of Interconnect Theory and Practice*, by Hall, Hall and McCall (Wiley Interscience 2000) - ISBN 0-36090-2
- *Signal Integrity Issues and Printed Circuit Design*, by Doug Brooks (Prentice Hall) ISBN 0-13- 141884-X
- *PCB Design for Real-World EMI Control*, by Bruce R. Archambeault (Kluwer Academic Publishers Group) - ISBN 1-4020-7130-2

- *Digital Design for Interference Specifications - A Practical Handbook for EMI Suppression*, by David L. Terrell & R. Kenneth Keenan (Newnes Publishing) - ISBN 0-7506-7282-X
- *Electromagnetic Compatibility Engineering*, by Henry Ott (1st Edition - John Wiley and Sons) - ISBN 0-471-85068-3
- *Introduction to Electromagnetic Compatibility*, by Clayton R. Paul (John Wiley and Sons) - ISBN 978-0-470-18930-6
- *Grounding & Shielding Techniques*, by Ralph Morrison (5th Edition - John Wiley & Sons) - ISBN 0- 471-24518-6
- *EMC for Product Engineers*, by Tim Williams (Newnes Publishing) - ISBN 0-7506- 2466-3

1.4 Related documentation

Additional literature will be published when new NXP products become available.

For the list of current documents, see i.MX8M.

1.5 Conventions

Table 1 lists the notational conventions used in this document.

Table 1. Conventions used in the document

Conventions	Description
`Courier`	Used to indicate commands, command parameters, code examples, and file and directory names.
Italics	Used to indicates command or function parameters.
Bold	Function names are written in bold.
cleared/set	When a bit takes the value zero, it means to be cleared; when it takes a value of one, it means to be set.
mnemonics	Instruction mnemonics are shown in lowercase bold. Book titles in text are set in italics.
sig_name	Internal signals are written in all lowercase.
nnnn nnnnh	Denotes hexadecimal number
0b	Denotes binary number
rA, rB	Instruction syntax used to identify a source GPR.
rD	Instruction syntax used to identify a destination GPR.
REG[FIELD]	Abbreviations for registers are shown in uppercase. Specific bits, fields, or ranges appear in brackets. For example, MSR[LE] refers to the little-endian mode enable bit in the machine state register.
x	An italicized *x* indicates an alphanumeric variable.
n, m	An italicized *n* indicates a numeric variable.

In this guide, notation for all logical, bit-wise, arithmetic, comparison, and assignment operations follow C Language conventions.

1.6 Acronyms and abbreviations

Table 2 defines the acronyms and abbreviations used in this document.

Table 2. Definitions and acronyms

Acronym	Definition
Arm™	Advanced RISC Machines processor architecture
BGA	Ball Grid Array package
BOM	Bill of Materials
BSDL	Boundary Scan Description Language
CAN	Flexible Controller Area Network peripheral
CCM	Clock Controller Module
CSI	MIPI Camera Serial Interface
DDR	Dual Data Rate DRAM
DDR3L	Low voltage DDR3 DRAM
DDR4	DDR4 DRAM
DDRC	DDR Controller
DFP	Downstream Facing Port (USB Type-C)
DRP	Dual Role Port (USB Type-C)
ECSPI	Enhanced Configurable SPI peripheral
EIM	External Interface Module
ENET	10/100/1000 Mbps Ethernet MAC peripheral
EPIT	Enhanced Periodic Interrupt Timer peripheral
ESR	Equivalent Series Resistance
GND	Ground
GPC	General Power Controller
GPIO	General Purpose Input/Output
HDCP	High-bandwidth Digital Content Protection
I2C	Inter-integrated Circuit interface
IBIS	Input output Buffer Information Specification
IOMUX	i.MX 8MDQLQ chip-level I/O multiplexing
JTAG	Joint Test Action Group

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Table 2. Definitions and acronyms (continued)

Acronym	Definition
KPP	Keypad Port Peripheral
LDB	LVDS Display Bridge
LDO	Low Drop-Out regulator
LPCG	Low Power Clock Gating
LPDDR4	Low Power DDR4 DRAM
LVDS	Low-Voltage Differential Signaling
MLB	Media Local Bus
ODT	On-Die Termination
OTP	One-Time Programmable
PCB	Printed Circuit Board
PCIe	PCI Express
PCISig	Peripheral Component Interconnect Special Interest Group
PDN	Power Distribution Network
PMIC	Power Management Integrated Circuit
POR	Power-On Reset
PTH	Plated Through Hole PCB (i.e. no microvias)
RGMII	Reduced Gigabit Media Independent Interface (Ethernet)
RMII	Reduced Media Independent Interface (Ethernet)
ROM	Read-Only Memory

Chapter 2
i.MX 8MDQLQ design checklist

This document provides a design checklist for the i.MX 8MDQLQ (17 × 17 mm package) processor. The design checklist tables recommend optimal design and provide explanations to help users understand better. All supplemental tables referred by the checklist appear in sections following the design checklist tables.

2.1 Design checklist table

Table 3. LPDDR4 recommendations (i.MX 8MDQLQ)

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. Connect the ZQ ball on the processor (ball AA13) to individual 240 Ω , 1 % resistors to GND.	This is a reference used during DRAM output buffer driver calibration.
✓	2. The ZQ0 and ZQ1 balls on LPDDR4 device should be connected through 240 Ω , 1 % resistors to the LPDDR4 VDDQ rail.	—
✓	3. Place a 10 kΩ , 5 % resistor to ground on the DRAM reset signal.	This will ensure adherence to the JEDEC specification until the control is configured and starts driving the DDR.
Connected	4. The VREF pin on the processor (ball AA14) can be left unconnected.	The VREF signal for LPDDR4 is generated internally by the processor.
✓	5. The processor balls AC12 and AE11 should be left unconnected. The `ODT_CA` balls on the LPDDR4 device should be connected directly or through a 10 kΩ to the LPDDR4 VDD2 rail.	LPDDR4 ODT on the i.MX 8MDQLQ is command-based, making processor `ODT_CA` output balls unnecessary.
✓	6. The architecture for each chip inside the DRAM package must be × 16.	The processor does not support byte mode specified in JESD209-4B.
✓	7. The processor ball MTEST (ball AB14), MTEST1 (ball AC13), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.
✓	8. It is strongly suggested to use LPDDR4 if lower power consumption is required since DLL-off mode is not supported.	The LPDDR4 can operate at low frequency without DLL-off mode.

~~Table 4. DDR4/DDR3L recommendations (i.MX 8MDQLQ)~~

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Connect the ZQ ball on the processor (ball AA13) to individual 240 Ω , 1 % resistors to GND.	This is a reference used during DRAM output buffer driver calibration.
	2. The ZQ ball on each DDR4/DDR3L device should be connected through individual 240 Ω , 1 %	—

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Table 4. DDR4/DDR3L recommendations (i.MX 8MDQLQ) (continued)

Check box	Recommendations	Explanation/Supplemental recommendations
	resistors to GND.	
	3. The processor ball MTEST (ball AB14), MTEST1 (ball AC13), should be left unconnected.	These are observability ports for manufacturing and are not used otherwise.
	4. DLL-off mode isn't supported, which means DDR4/ DDR3L can't run in low frequency such as 100 MTS.	The power consumption for low power mode in DDR4/DDR3L system will be higher compared with LPDDR4 system.

Table 5. I2C recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Verify the target I2C interface clock rates.	The I2C bus can only be operated as fast as the slowest peripheral on the bus. If faster operation is required, move the slow devices to another I2C port.
	2. Verify that there are no I2C address conflicts on any of the I2C buses utilized.	There are multiple I2C ports available on chip, so if a conflict exists, move one of the conflicting devices to a different I2C bus. If this isn't possible, use an I2C bus switch (NXP part number PCA9646).
	3. Do not place more than one set of pull-up resistors on the I2C lines.	This could result in excessive loading and potential incorrect operation. Choose the pull-up value commensurate with the bus speed being utilized.
	4. Ensure that the VCC rail powering the i.MX 8MDQLQ I2C interface balls matches the supply voltage used for the pull-up resistors and the slave I2C devices.	Prevent device damage or incorrect operation due to voltage mismatch.

Table 6. JTAG recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. Do not use external pullup or pulldown resistors on `JTAG_TDO`.	`JTAG_TDO` is configured with an on-chip keeper circuit and the floating condition is actively eliminated if an external pull resistor is not present.
✓	2. Follow the recommendations for external pull-up and pull-down resistors given in Table 14.	—
✓	3. For normal operation, TEST_MODE (ball V7) should be pulled down using a 100 KΩ resistor. To enter boundary-scan mode, this pin should be pulled up to `NVCC_JTAG` using a 4.7 KΩ resistor. Please see **COMPLIANCE_PATTERNS** in the chip BSDL file.	—

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Table 6. JTAG recommendations (continued)

Check box	Recommendations	Explanation/Supplemental recommendations
	4. To enter boundary-scan mode, `GPIO1_IO00`, `GPIO1_IO01`, `GPIO1_IO02` should be pulled down and `GPIO1_IO03`, `JTAG_nTRST` should be pulled up. Recommended pull resistor value is 4.7 KΩ. Please see **COMPLIANCE_PATTERNS** in the chip BSDL file.	—

Table 7. Reset and ON/OFF recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. The `POR_B` input must be asserted at power-up and remain asserted until the last power rail for devices required for system boot are at their working voltage. This functionality is controlled by the PMIC (PF4210) on EVK.	`POR_B` is driven by the PMIC. If a reset button is used, it should be connected to the enable pin of the PMIC and/or other power supply chips instead of directly connected to `POR_B` pin of the CPU. When `POR_B` is asserted (low) on the i.MX 8MDQLQ, the output `PMIC_ON_REQ` remains asserted (high).
✓	2. For portable applications, the **ON_OFF_BUTTON** input may be connected to an ON/OFF SPST push-button switch to ground. If the On-chip debouncing is provided, this input has an on-chip pullup. Otherwise, the **ON_OFF_BUTTON** should not be connected.	A brief connection to GND in OFF mode causes the internal power management state machine to change state to ON. In ON mode, a brief connection to GND generates an interrupt (intended to initiate a software-controllable power-down). The connection to GND for approximate 5 second or more causes a forced OFF.
Not used	3. If using `WDOG_B` (`GPIO1_IO02`) signal as a reset source, the signal should be AC coupled to reset input with a 1uF capacitor.	In boundary-scan mode `WDOG_B` (`GPIO1_IO02`) signal will be pulled down, which will keep the system in the reset state if DC is coupled to reset input.

Table 8. i.MX 8MDQLQ power/decoupling recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. Comply with the power-up sequence guidelines as described in the datasheet to guarantee reliable operations of the device.	Any deviation from these sequences may result in the following situations: • Excessive current during power-up phase • Prevention of the device from booting • Irreversible damage to the processor (worst case)
✓	2. Maximum ripple voltage requirements	Common requirement for ripple noise peak-to-peak value should be less than 5% of the supply voltage nominal value.
	3. Industrial part and commercial part have different `VDD_SOC` operation range	Please refer to IMX8MDQLQIEC and IMX8MDQLQCEC for details.

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Table 8. i.MX 8MDQLQ power/decoupling recommendations (continued)

Check box	Recommendations	Explanation/Supplemental recommendations
✓	4. Check PMIC switcher output currents and the switcher inductor current ratings against the maximum supply currents ratings per rail as specified in the datasheet.	When using an non-NXP PMIC, or scaling down a power rail, ensure the PMIC and inductor will meet the maximum current demands of the system. **NOTE** Currents will be higher at higher SoC temperatures than at room temperature.

✓ Table 9. Decoupling capacity recommendations (i.MX 8MDQLQ)

Checkbox	Supply	4.7 nF[1]	0.01 µF[2]	0.1 µF[3]	1 µF[4]	2.2 µF[5]	22 µF[6]	Notes
	`VDD_DRAM`	11	2	—	4	—	3	Location of these capacitors is critical for effective decoupling. See layout of EVK for the optimum location of these decoupling capacitors.
	`NVCC_DRAM`	—	—	—	~~18~~ 14	—	~~3~~ 4	—
	`VDD_ARM`	—	—	—	~~9~~ 8	—	3	—
	`VDD_GPU`	—	—	—	7	—	3	—
	`VDD_VPU`	—	—	—	~~4~~ 3	—	~~6~~ 3	—
	`VDD_SOC`	—	—	—	~~10~~ 14	—	~~3~~ 2	—
	`VDD_SNVS`	—	—	~~1~~	~~0~~ 1	—	—	—
	`NVCC_SNVS`	—	—	—	1	—	—	—
	`VDDA_0P9`	—	—	—	1	—	—	This rail should be sourced from the VDD_SOC rail through a 240 Ω ferrite bead.
	`VDDA_DRAM`, `VDDA_1P8_XXX`	—	—	6	—	—	1	—
	`NVCC_JTAG`, `NVCC_NAND`, `NVCC_SAI1`, `NVCC_SAI2`, `NVCC_SAI3`, `NVCC_SAI5`, `NVCC_GPIO1`, `NVCC_I2C`,	—	—	9	—	—	—	—

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Table 9. Decoupling capacity recommendations (i.MX 8MDQLQ) (continued)

Checkbox	Supply	4.7 nF[1]	0.01 µF[2]	0.1 µF[3]	1 µF[4]	2.2 µF[5]	22 µF[6]	Notes
	NVCC_UART, NVCC_ECSPI							
	NVCC_SD1	—	—	1	—	—	—	—
	NVCC_SD2	—	—	1	—	—	—	—
	NVCC_ENET	—	—	1	—	—	—	—
	USB1_VDD33, USB1_VPH, USB2_VDD33, USB2_VPH	—	—	2	—	1	—	—
	USB1_VPTX, USB1_VP, USB1_DVDD, USB2_VPTX, USB2_VP, USB2_DVDD	—	—	2	—	1	—	—
	PCIE_VPH	—	—	1	—	1	—	—
	PCIE_VPTX, PCIE_VP	—	—	2	—	1	—	—
	HDMI_AVDDIO	—	—	1	—	1	—	—
	HDMI_AVDDCLK, HDMI_AVDDCORE	—	—	2	—	1	—	—
	MIPI_VDDHA	—	—	1	—	1	—	—
	MIPI_VDDA, MIPI_VDDPLL	—	—	3	—	1	—	—
	MIPI_VDD	—	—	2	—	—	—	MIPI_VDD and MIPI_VDDA can share the same source. MIPI_VDD should be isolated with a 120 Ω ferrite bead.

1. The capacitor part number used on EVK is GRM033R61A472KA01D.
2. The capacitor part number used on EVK is GRM033R70J103KA01D.
3. The capacitor part number used on EVK is 0201X104K100CT.
4. The capacitor part number used on EVK is 02016D105MAT2A.
5. The capacitor part number used on EVK is C1005X5R1A225K.
6. The capacitor part number used on EVK is C1608X5R1A226M080AC.

Table 10. PCIe recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
	1. Use an appropriate PCIe reference clock generator.	The NXP EVK board design uses an IDT 9FGV0241 device. However, NXP does not recommend one supplier over another, and does not suggest that this is the only clock generator supplier. The device used should support all the specs (jitter, accuracy, etc.).
	2. The PCIe reference clock generator shall have an enable pin to connect to PCIe **CLKREQ#** signal and be able to output stable clock within 400 ns from the assertion of CLKREQ# signal.	This is to be compliant with the PCIe spec for entering into / exiting from L1 substate. For **9FGV0241** used on EVK board, this is achieved by connecting the **CLKREQ#** signal to `OE#` pin of the **9FGV0241**.
✓	3. The differential transmitters from the processor must be AC coupled. Use a 0.1 μF cap on both the `PCIE_TXP` and `PCIE_TXN` outputs.	PCIe specification compliance requires AC coupling at each transmitter. The receiver must be DC coupled.
✓	4. The `PCIEx_RESREF` ball (ball G25 and C25) should be connected to the ground through a 200 Ω, 1 % resistor.	—
✓	5. If supplying the PCIE_VPH power rail with 3.3 V, the PCIe PHY internal 1.8 V regulator must be enabled by setting `PCIE1/2_VREG_BYPASS=0` in `IOMUXC_GPR_GPR14` and `IOMUXC_GPR_GPR16` registers.	The PCIe PHY internal circuitry only works with 1.8 V. Supplying it with 3.3 V without enabling internal regulator will lead to overstress of the internal circuitry and significantly reduce its lifecycle.

Table 11. USB recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. Connect a 200 Ω , 1 % resistor to the ground on the `USBx_RESREF` ball (ball A11 and B11).	—
✓	2. Route all USB differential signals with 90 Ω differential impedance.	—
✓	3. ESD protection should be implemented at the connector pins. Choose a low capacitance device recommended for high-speed interfaces.	This will prevent potential damages to board components from ESD.

Table 12. HDMI recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
✓	1. Connect a 499 Ω , 1 % resistor to ground on the `HDMI_REXT` ball (ball P1).	—
✓	2. Route all HDMI differential pairs with 100 Ω differential impedance.	—

Table 13. Oscillator/Crystal recommendations

Check box	Recommendations	Explanation/Supplemental recommendations
√	1. Connect a 25 MHz crystal between XTALI_25M and XTALO_25 M (balls U24 and U25).	A 100 Ω typical ESR and 8 pF CL crystal rated for a maximum drive level of 200 μW is acceptable. Consult crystal vendor and do matching test for designing external compensation capacitors is preferred. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
√	2. Connect a 27 MHz crystal between XTALI_27M and XTALO_27M (balls V24 and V25).	A 100 Ω typical ESR and 8 pF CL crystal rated for a maximum drive level of 200 μW is acceptable. Consult crystal vendor and do matching test for designing external compensation capacitors is preferred. Use short traces between the crystal and the processor, with a ground plane under the crystal, load capacitors, and associated traces.
√	3. The i.MX 8MDQLQ 32.768 kHz needs to be driven with an external clock (oscillator) into the RTC input (ball V22).	The voltage level of this driving clock should not exceed the voltage of the NVCC_SNVS rail and the frequency should be less than 100 kHz. Do not exceed NVCC_SNVS, or the damage/malfunction may occur. The RTC signal should not be driven if the NVCC_SNVS supply is OFF. It can lead to damage or malfunction. For RTC VIL and VIH voltage levels, see the latest i.MX 8MDQLQ datasheet available at i.MX8M.

2.2 JTAG signal termination

Table 14 is a JTAG termination chart showing what terminations should be placed on PCB designs.

Table 14. Recommended JTAG board terminations

	JTAG signal	I/O type	External termination	Comments
√	JTAG_TCK	Input	10 kΩ pull-down	—
√	JTAG_TMS	Input	None	Internal pulled up to NVCC_JTAG, no external termination required.
√	JTAG_TDI	Input	None	Internal pulled up to NVCC_JTAG, no external termination required.
√	JTAG_TDO	3-state output	None	—
√	JTAG_TRSTB	Input	4.7 kΩ pull-up	In normal operation, this pin is internally pulled-up to NVCC_JTAG. But in boundary- scan mode, this pin is floating. An external pull-up resistor is required for boundary-scan mode.

Chapter 3
i.MX 8MDQLQ layout/routing recommendations

3.1 Introduction

This chapter introduces how to assist design engineers with the layout of an i.MX 8MDQLQ-based system.

3.2 Basic design recommendations

When using the Allegro design tool, the schematic symbol & PCB footprint created by NXP is recommended. When not using the Allegro tool, use the Allegro footprint export feature (supported by many tools). If the export is not possible, create the footprint per the package dimensions outlined in the product data sheet.

Native Allegro layout and gerber files are available on i.MX8M.

3.2.1 Placing decoupling capacitors

Place small decoupling and larger bulk capacitors on the bottom side of the PCB.

The 0201 or 0402 decoupling and 0603 or larger bulk capacitors should be mounted as close as possible to the power vias. The distance should be less than 50 mils. Additional bulk capacitors can be placed near the edge of the BGA via array. Placing the decoupling capacitors close to the power balls is critical to minimize inductance and ensure high-speed transient current required by the processor. See the i.MX 8MDQLQ EVK layouts for examples of the desired decoupling capacitor placement.

The following list introduces how to choose correct decoupling scheme:

- Place the largest capacitance in the smallest package that budget and manufacturing can support.
- For high speed bypassing, select the required capacitance with the smallest package (for example, 0.1 μF, 0.22 μF, 1.0 μF, or even 2.2 μF in a 0201 package size).
- Minimize trace length (inductance) to small caps.
- Series inductance cancels out capacitance.
- Tie caps to GND plane directly with a via.
- Place capacitors close to the power ball of the associated package from the schematic.
- A preferred BGA power decoupling design is available on the EVK board design available oni.MX8M. Customers should use the NXP design strategy for power and decoupling.

3.3 Stack-up recommendations

3.3.1 Stack-up recommendation (i.MX 8MDQLQ)

Due to the number of balls on the i.MX 8MDQLQ processor in the 17 mm × 17 mm package, a minimum 8-layer PCB stackup is recommended. Of the 8-layers on the PCB, a sufficient number of layers need to be dedicated to power on routing to meet the IR drop target of 1 % for the i.MX 8MDQLQ CPU power rails.

The constraints for the trace width will depend on such factors as the board stackup and associated dielectric and copper thickness, required impedance, and required current (for power traces). The stackup also determines the constraints for routing and spacing. Consider the following requirements when designing the stackup and selecting board material:

- Board stack-up is critical for high-speed signal quality.
- Preplanning impedance of critical traces is required.
- High-speed signals must have reference planes on adjacent layers to minimize cross-talk.

- PCB material: the material used on EVK is TU768.

3.4 DDR design recommendations

3.4.1 DDR connection information

The i.MX 8MDQLQ processor can be used with LPDDR4, DDR4 or DDR3L memory. Since these memory types have different I/O signals, there are 37 generically-named functional balls, depending on the type of memory used. See Table 15 for the connectivity of these generic balls for DDR3L, LPDDR4 and DDR4. The schematic symbol created by NXP already replaced these generic names with DDR function.

Table 15. DDR3L/LPDDR4/DDR4 connectivity

Ball name	Ball #	LPDD4 function	DDR4 function	DDR3L function
DRAM_AC00	AC16	√ CKE0_A	CKE0	CKE0
DRAM_AC01	AE17	√ CKE1_A	CKE1	CKE1
DRAM_AC02	AE18	√ CS0_A	CS0_n	CS0#
DRAM_AC03	AC18	√ CS1_A	C0	—
DRAM_AC04	AD14	√ CK_t_A	BG0	BA2
DRAM_AC05	AE14	√ CK_c_A	BG1	A14
DRAM_AC06	AE13	√ —	ACT_n	A15
DRAM_AC07	AB15	√ —	A9	A9
DRAM_AC08	AD17	√ CA0_A	A12	A12/BC#
DRAM_AC09	AE16	√ CA1_A	A11	A11
DRAM_AC10	AD20	√ CA2_A	A7	A7
DRAM_AC11	AE20	√ CA3_A	A8	A8
DRAM_AC12	AD19	√ CA4_A	A6	A6
DRAM_AC13	AE19	√ CA5_A	A5	A5
DRAM_AC14	AB16	√ —	A4	A4
DRAM_AC15	AC15	√ —	A3	A3
DRAM_AC16	AE15	√ —	CK_t_A	CK_A
DRAM_AC17	AD15	√ —	CK_c_A	CK#_A
DRAM_AC19	AB14	√ MTEST	MTEST	MTEST
DRAM_AC20	AD10	√ CKE0_B	CK_t_B	CK_B

Table continues on the next page...

Table 15. DDR3L/LPDDR4/DDR4 connectivity (continued)

Ball name	Ball #	LPDD4 function	DDR4 function	DDR3L function
DRAM_AC21	AE10	✓ CKE1_B	CK_c_B	CK#_B
DRAM_AC22	AD8	✓ CS1_B	—	—
DRAM_AC23	AC9	✓ CS0_B	—	—
DRAM_AC24	AD12	✓ CK_t_B	A2	A2
DRAM_AC25	AE12	✓ CK_c_B	A1	A1
DRAM_AC26	AB12	✓ —	BA1	BA1
DRAM_AC27	AA12	✓ —	PARITY	—
DRAM_AC28	AC7	✓ CA2_B	A13	A13
DRAM_AC29	AE7	✓ CA3_B	BA0	BA0
DRAM_AC30	AE6	✓ CA4_B	A10/AP	A10/AP
DRAM_AC31	AD6	✓ CA5_B	A0	A0
DRAM_AC32	AE8	✓ CA0_B	C2	—
DRAM_AC33	AE9	✓ CA1_B	CAS_n/A15	CAS#
DRAM_AC34	AC10	✓ —	WE_n A14	WE#
DRAM_AC35	AB10	✓ —	RAS_n/A16	RAS#
DRAM_AC36	AC12	✓ —	ODT0	ODT0
DRAM_AC37	AE11	✓ —	ODT1	ODT1
DRAM_AC38	AC11	✓ —	CS1_n	CS1#

3.4.2 LPDDR4-3200 design recommendations

The following list details some generic guidelines that should be adhered to when implementing an i.MX 8MDQLQ design using LPDDR4.

1. It is expected that the layout engineer and design team already has experience and training with DDR designs at speeds of 1.6 GHz/3200 MT/s.
2. Refer to solid GND plane only for all the high-speed signal traces. If referring to both GND and NVCC_DRAM (VDDQ) plane, make sure the dielectric thickness between trace and NVCC_DRAM plane is larger than that between trace and GND plane. Do not refer to other power planes.
3. The impedance of DQ and DMI signal traces should be controlled to 42 Ω instead of 50 Ω to maximize the timing margin at 3200 MT/s.
4. The DQ/DMI/DQS signals must be routed in inner layers as stripline or embedded microstrip and follow 3W rule(center to center) to minimize trace crosstalk.

5. At a speed of 3200 MT/s, signal vias can be a significant source of crosstalk. If not properly designed, it can introduce crosstalk larger than that from the trace. To minimize via crosstalk, make sure the total number of vias to be two or less on each point-to-point single-ended/differential trace. Place at least one ground stitching via within 40 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 1.

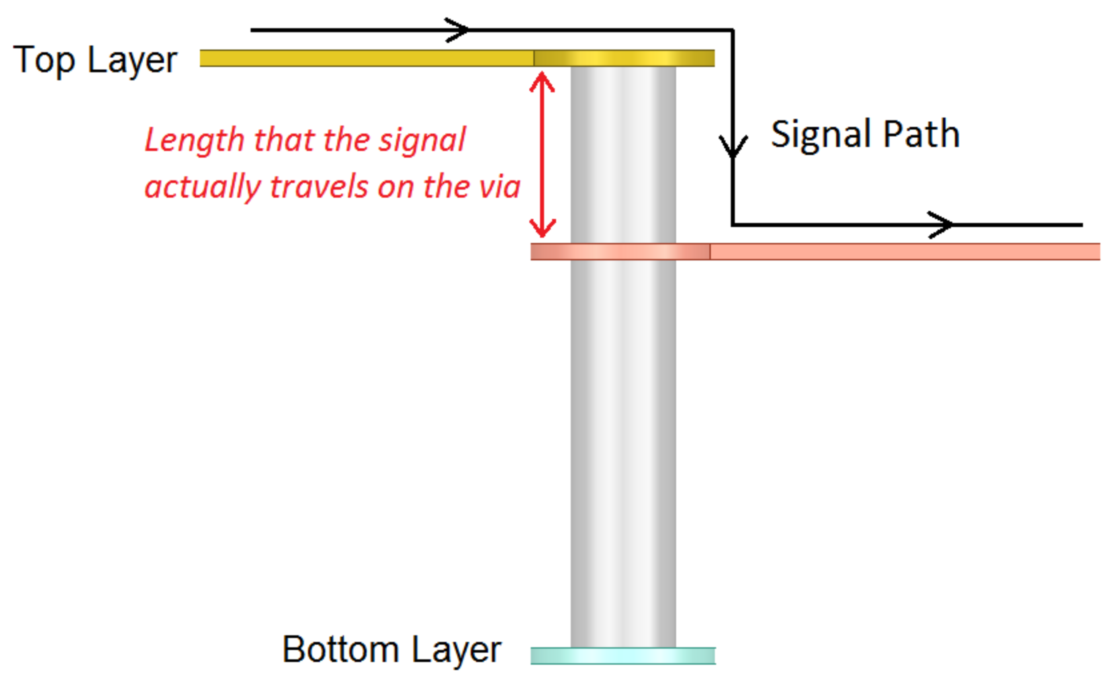

Figure 1. Length that the signal actually travels on the Via

6. Route the CLK signal on top layer with no via transition and keep over than 5 W spacing from other signals.
7. DQS and DMI with the same slice should have the same number of vias/layer changes.
8. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delay. Incorporate the package pin delay into the CAD tool's constraint manager.
9. Include the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling the **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.
10. Byte swapping within each 16-bit channel is OK. Bit swapping within each slice/byte lane is OK.
11. Bit swapping of Command/Address (CA[5:0]) signals is **NOT** allowed.
12. For an i.MX 8MDQLQ design, DRAM_AC14 and DRAM_AC34 on the processor must be left unconnected if using LPDDR4. The ODT_CA balls on the LPDDR4 devices should be connected directly or through a resistor to the VDD2 supply.
13. In general, the 200-ball LPDDR4 package should be placed 100 mils from the i.MX 8MDQLQ.
14. Enable the DBI (data bus inversion) feature. It can help reduce both power consumption and power noise.

3.4.2.1 i.MX 8MDQLQ LPDDR4-3200 routing recommendations

LPDDR4-3200 needs to be routed with signal fly times matched shown in Table 16. The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling the **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.

An example of the delay match calculation has been shown for the i.MX 8MDQLQ EVK board design in Table 17 and Table 18. This analysis was done for the LPDDR4-3200 implementation using the i.MX 8MDQLQ.

NXP recommends that users simulate their LPDDR4 implementation before fabricating PCBs.

Table 16. i.MX 8MDQLQ LPDDR4-3200 routing recommendations

LPDDR4-3200				
LPDDR4 signal (each 16-bit channel)	Group	PCB + package prop delay		
		Min.	Max.	Considerations
CK_t/CK_c	Clock	Short as possible	175 ps	Match the true/ complement signals within 1 ps.
CA[5:0]	Address/Command/Control	CK_t - 25 ps	CK_t + 25 ps	—
CS[1:0]				
CKE[1:0]				
DQS0_t/DQS0_c	Byte 0 - DQS	CK_t - 85 ps	CK_t + 85 ps	Match the true/ complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -10 ps	DQS0_t +10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	CK_t - 85 ps	CK_t + 85 ps	
DM1	Byte 1 - Data	DQS1_t -10 ps	DQS1_t +10 ps	
DQ[15:8]				

Table 17. LPDDR4 delay matching example (CA/CTL signals)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
DRAM_CK_T_A	106.6	42.7	Routed on top layer, no via
	149.3		Total Net Delay
DRAM_CK_C_A	107.1	41.5	Routed on top layer, no via
	148.6		Total Net Delay
DRAM_CA0_A	105.0	49.8	Vias are L1-> L8->L1
	154.8		Total Net Delay
DRAM_CA1_A	85.1	73.5	Vias are L1-> L8->L1
	158.6		Total Net Delay
DRAM_CA2_A	106.6	51.2	Vias are L1-> L8->L1

Table continues on the next page...

Table 17. LPDDR4 delay matching example (CA/CTL signals) (continued)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
	157.8		Total Net Delay
DRAM_CA3_A	106.2	52.6	Vias are L1-> L8->L1
	158.8		Total Net Delay
DRAM_CA4_A	111.8	58.6	Vias are L1-> L8->L1
	170.4		Total Net Delay
DRAM_CA5_A	105.7	56.2	Vias are L1-> L8->L1
	161.9		Total Net Delay
DRAM_nCS0_A	106.6	51.0	Vias are L1-> L8->L1
	157.6		Total Net Delay
DRAM_nCS1_A	108.1	47.8	Vias are L1-> L8->L1
	155.9		Total Net Delay
DRAM_CKE0_A	121.1	36.5	Vias are L1-> L8->L1
	157.6		Total Net Delay
DRAM_CKE1_A	106.1	47.4	Vias are L1-> L8->L1
	153.5		Total Net Delay

1. Obtained directly from the Allegro PCB file.
2. obtained from Table 24

Table 18. LPDDR4 length matching example (byte lane 1 signals)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
DRAM_SDQS1_T_A	180.1	45.2	Vias are L1-> L4->L1
	225.3		Total Net Delay
DRAM_SDQS1_C_A	179.5	45.3	Vias are L1-> L4->L1
	224.8		Total Net Delay
DRAM_DMI1_A	180.2	43.4	Vias are L1-> L4->L1
	223.6		Total Net Delay
DRAM_DATA8_A	179.1	44.2	Vias are L1-> L4->L1

Table continues on the next page...

Table 18. LPDDR4 length matching example (byte lane 1 signals) (continued)

Net name	PCB delay (ps)	Pkg delay (ps)	Comments
	223.3		Total Net Delay
DRAM_DATA9_A	182.7	46.5	Vias are L1-> L4->L1
	229.2		Total Net Delay
DRAM_DATA10_A	175.5	53.8	Vias are L1-> L4->L1
	229.3		Total Net Delay
DRAM_DATA11_A	185.9	43.5	Vias are L1-> L4->L1
	229.4		Total Net Delay
DRAM_DATA12_A	179.1	44.9	Vias are L1-> L4->L1
	224.0		Total Net Delay
DRAM_DATA13_A	182.0	45.0	Vias are L1-> L4->L1
	227.0		Total Net Delay
DRAM_DATA14_A	188.0	35.3	Vias are L1-> L4->L1
	223.3		Total Net Delay
DRAM_DATA15_A	184.3	40.4	Vias are L1-> L4->L1
	224.7		Total Net Delay

3.4.2.2 LPDDR4-3200 routing example (i.MX 8MDQLQ)

Figure 2 to Figure 5 show the placement and routing of the LPDDR4 signals on the i.MX 8MDQLQ EVK board. The CLK signals are routed on top layer with no via to achieve the best signal quality. Data byte lane 1 signals are routed on layer 4 to make the length that the signal actually travels on the via as short as possible, as limited number of GND vias can be placed near these signal vias. Data byte lane 0 signals are routed on layer 6. CA/CTL signals are routed on layer 8 as their data rate is only half of the data signals, and CA/CTL has more tolerance for crosstalk.

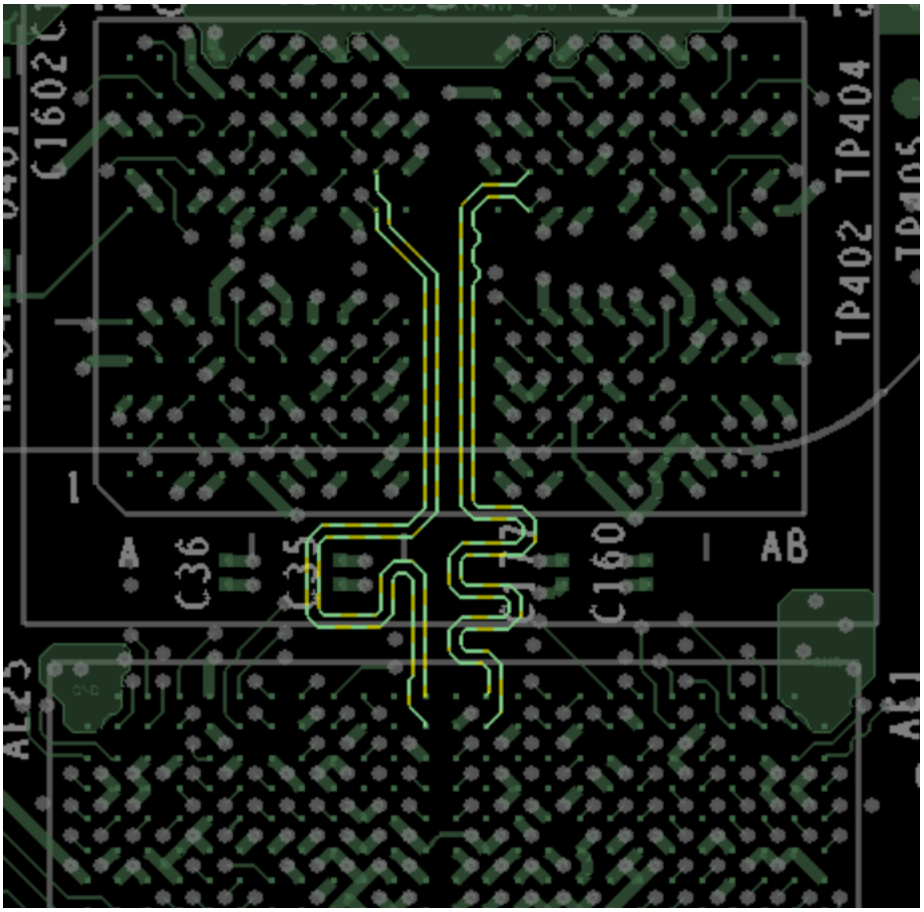

Figure 2. i.MX 8MDQLQ EVK board LPDDR4 routing (top layer)

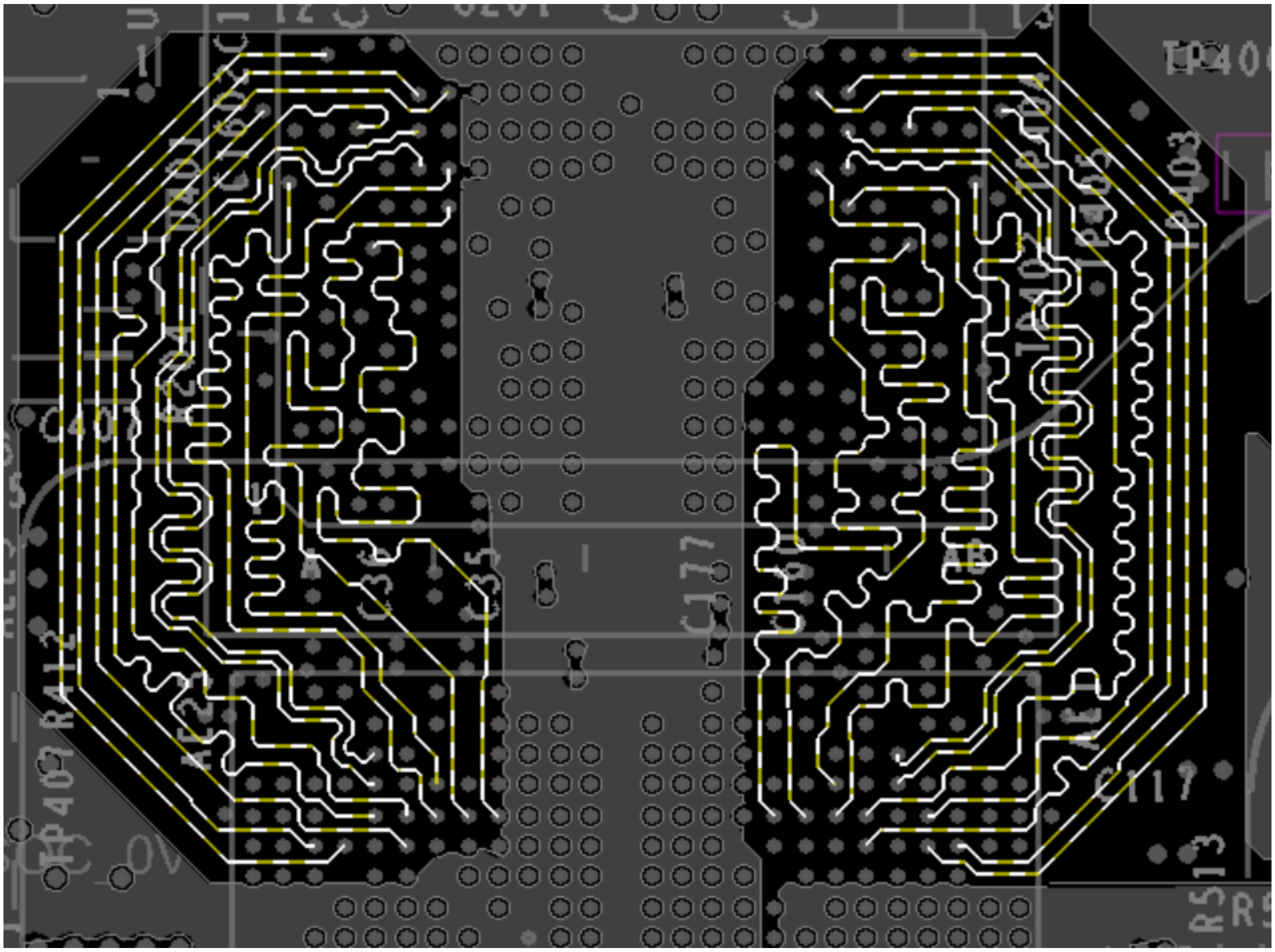

Figure 3. i.MX 8MDQLQ EVK board LPDDR4 routing (Layer 4)

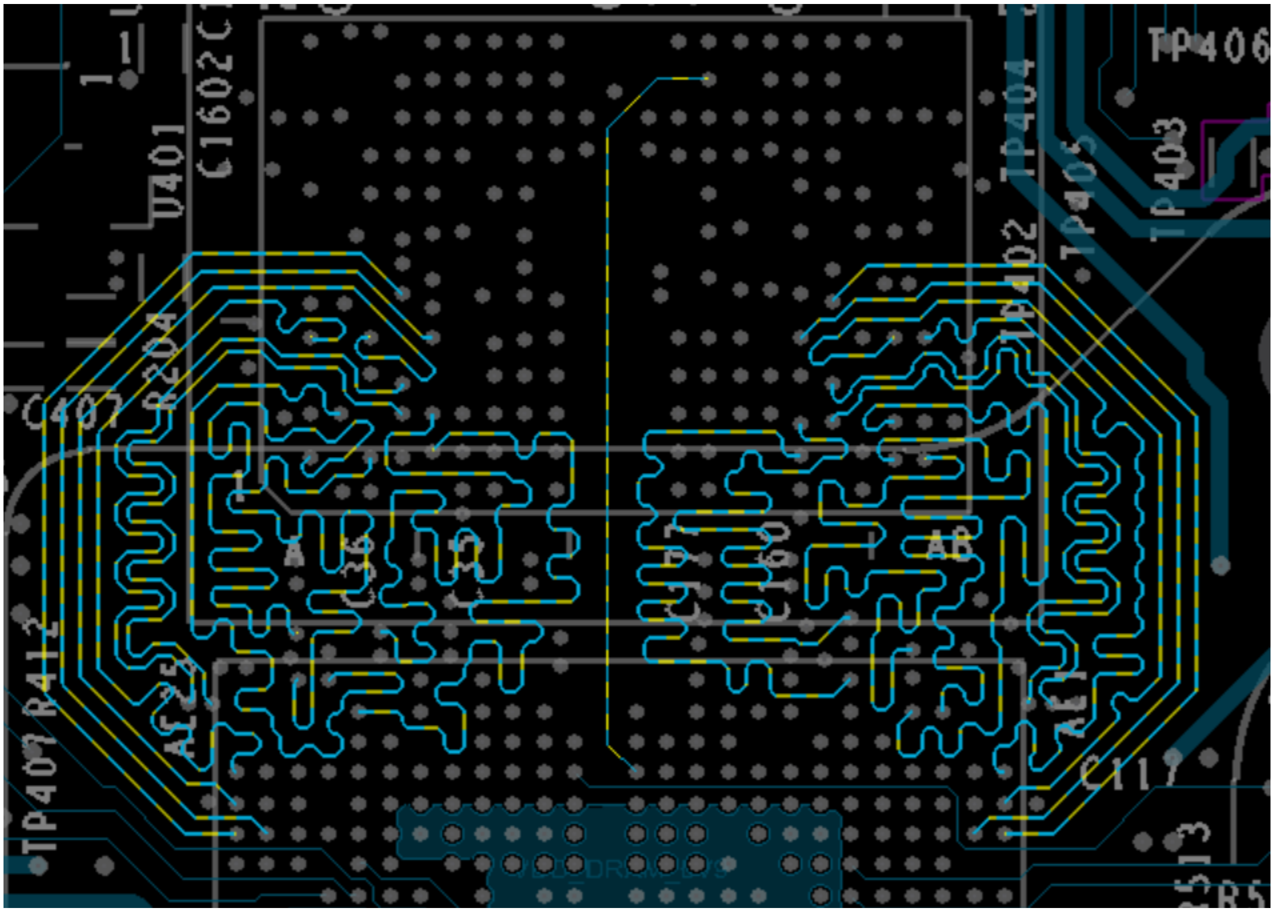

Figure 4. i.MX 8MDQLQ EVK board LPDDR4 routing (Layer 6)

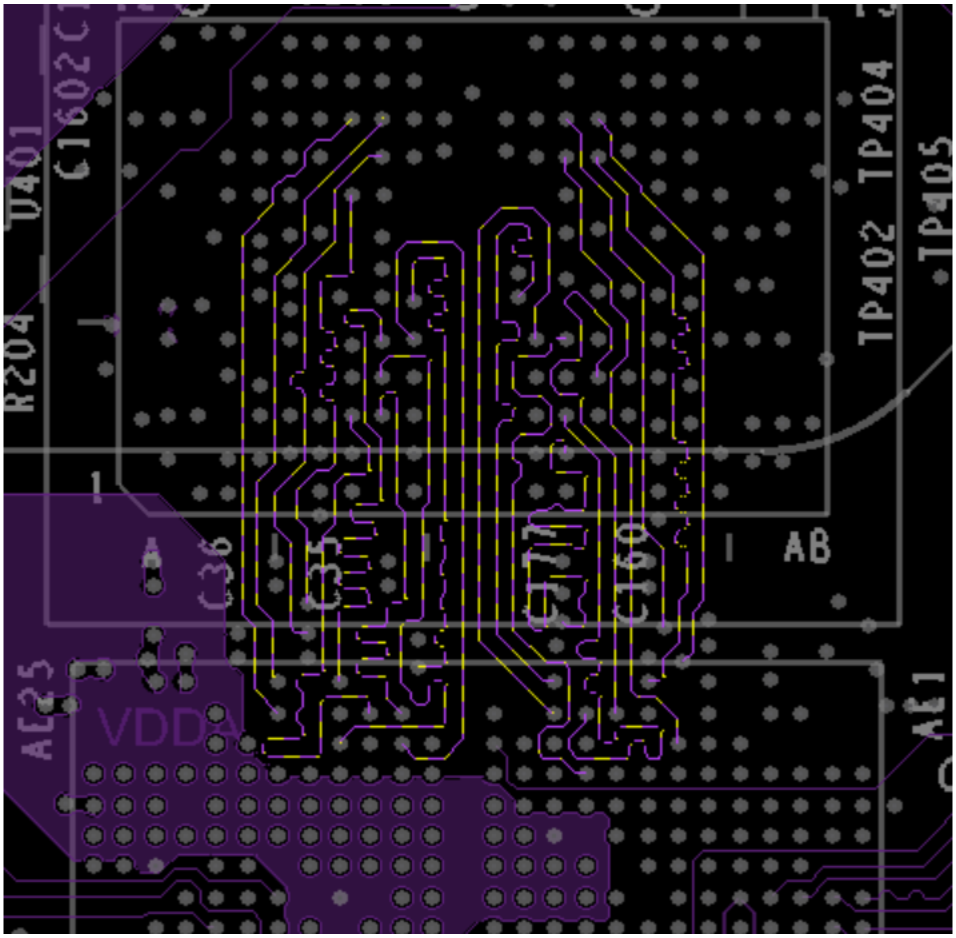

Figure 5. i.MX 8MDQLQ EVK board LPDDR4 routing (Layer 8)

3.4.2.3 LPDDR4-3200 SI simulation guide

The simulation architecture includes the DDR controller (i.e. the i.MX 8MDQLQ processor), the PCB and the LPDDR4 device. The IBIS model for the i.MX 8MDQLQ processor is available from NXP. The LPDDR4 device IBIS model must be obtained from the memory vendor.

This section introduces how to check SI performance of the layout for an LPDDR4-3200 design using the i.MX 8MDQLQ.

1. Perform S-parameter extraction:
    - It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
    - Set the extraction bandwidth to 20 GHz.
    - Port reference impedance: 50 Ω for signal ports, and 0.1 Ω for power ports.
    - Coupled mode: Set the rise time to 20 ps and coupling coefficient to 1 %.
2. Perform time domain simulation:
    - Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
    - Ideal power.
    - Probe at the die.
    - Simulation at slow corner (worst case).
    - Eye waveform triggered by aligning with the timing reference (DQS/CLK).

3.4.2.4 Eye width requirements

The simulated worst eye width should meet following requirements:

- DQ Write: Eye width @VREF ±70 mV should be over 221 ps.
- CA/CTL: Eye width @VREF ±77.5 mV should be over 380 ps.

Figure 6 shows an example of simulated eye width of DQ write.

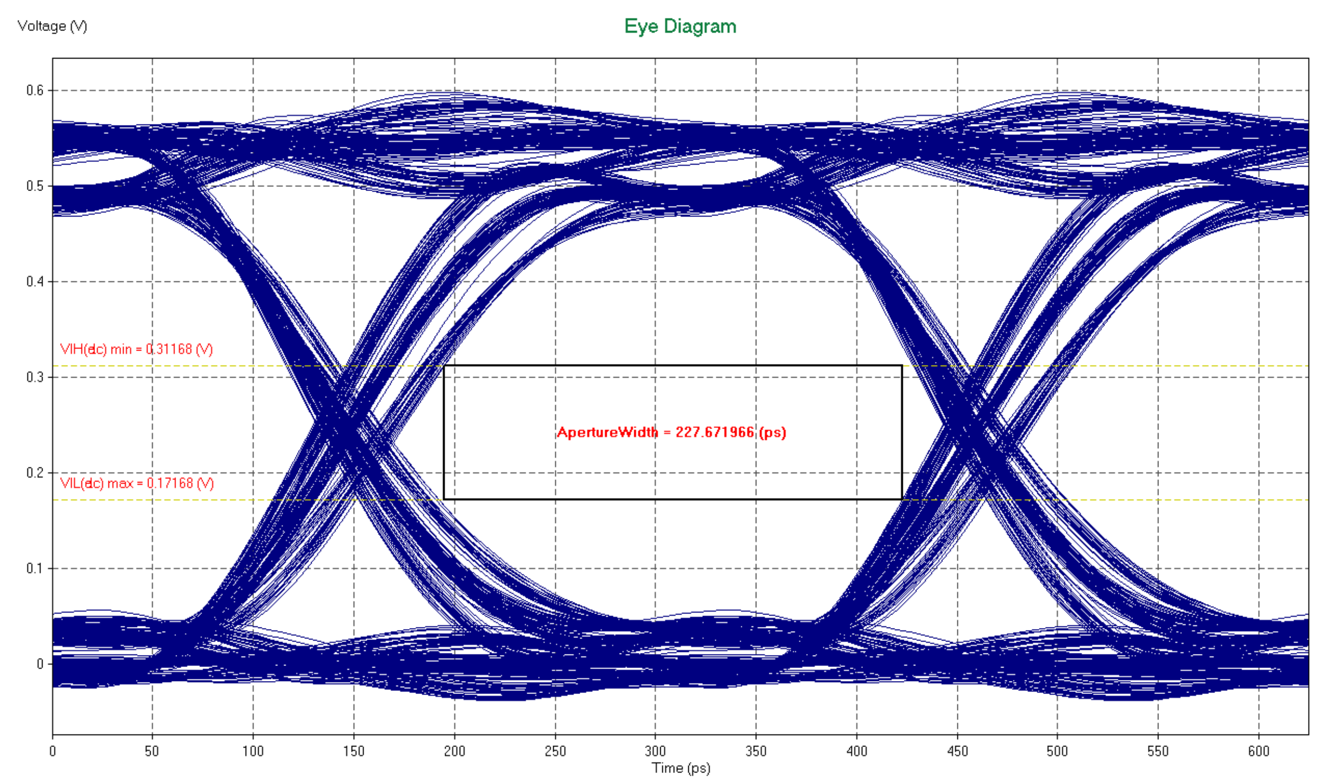

Figure 6. Example of simulated eye width

~~3.4.3 i.MX 8MDQLQ DDR4-2400/DDR3L-1600 design recommendations~~

The following lists details some generic guidelines that should be adhered to when implementing an i.MX 8MDQLQ design using DDR4/DDR3L.

1. Use a T PCB routing topology for a 2-rank system. Mount a rank of SDRAM on both top and bottom of the board, mirroring in a clamshell design for highest performance.

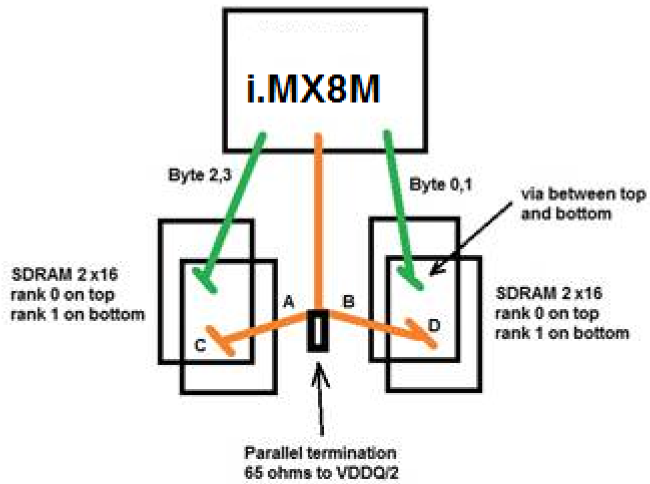

Figure 7. PCB routing topology for a 2-rank system

2. As illustrated in Figure 7, for data bytes, route straight from SOC to the SDRAM devices and via up and down with minimal stubs. For address/command signals, it is a T structure with branch to the SDRAM devices and via up and down with minimal stubs. And add a parallel termination (about 65 Ω to VDDQ/2 or VTT) at the branch point of the T.
3. The branch and stubs to the SDRAM pins must be the same length on both sides of the branch point (A+C=B+D); otherwise, the signal will show significant distortion. Also try to minimize length of branch as it is un-terminated at the SDRAM devices.
4. The impedance of DQ& DMI & the trunk of address/command signal traces should be controlled to 40 Ω instead of 50 Ω to maximize the timing margin.
5. All data signals within a byte lane should have the same number of vias/layer changes.
6. All the high-speed signal traces must be referred to solid GND or NVCC_DRAM (VDDQ) plane. Do not refer to other power planes.
7. For DQ nets, bit swapping within each slice/byte lane is OK.
8. For Address nets, use address mirroring to minimize top to bottom stubs. i.MX 8MDQLQ supports address mirroring but the wiring from i.MX 8MDQLQ to the two DRAM ranks must conform to Table 19 and Table 20, for DDR4 and DDR3L respectively.

Table 19. Wiring definition for DDR4 address mirroring

DDR4-2400		
i.MX 8MDQLQ pin	DRAM pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8

Table continues on the next page...

Table 19. Wiring definition for DDR4 address mirroring (continued)

DDR4-2400		
i.MX 8MDQLQ pin	DRAM pin	
	Rank 0	Rank 1
A8	A8	A7
A11	A11	A13
A13	A13	A11
BA0	BA0	BA1
BA1	BA1	BA0

Table 20. Wiring definition for DDR3L address mirroring

DDR4-2400		
i.MX 8MDQLQ pin	DRAM pin	
	Rank 0	Rank 1
A3	A3	A4
A4	A4	A3
A5	A5	A6
A6	A6	A5
A7	A7	A8
A8	A8	A7
BA0	BA0	BA1
BA1	BA1	BA0

9. The DQ/DMI/DQS signal must follow 3 W rule (center to center) to minimize trace crosstalk.
10. Place at least one ground stitching via within 40 mils of signal via when switching reference planes to provide continuous return path and reduce crosstalk. If it is not possible to place enough ground stitching vias due to space limitation, try to make the length that the signal actually travels on the via as short as possible, as illustrated in Figure 8.

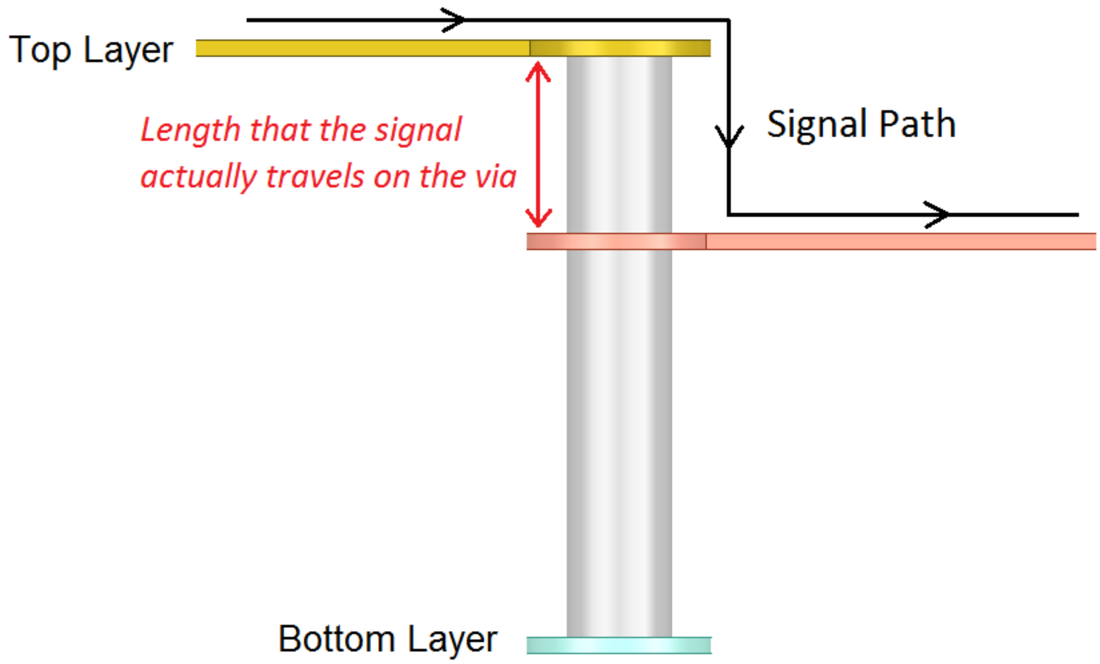

Figure 8. Length that the signal actually travels on the Via

11. Use time delay instead of length when performing the delay matching. The delay matching includes the PCB trace delay and the IC package delays. Incorporate the package pin delay into the CAD tool's constraint manager.
12. Consider the delay of vias when performing delay matching. This can be realized in Allegro tool by enabling **Z Axis Delay** in **Setup** -> **Constraints** -> **Modes**.

3.4.3.1 i.MX 8MDQLQ DDR4-2400/DDR3L-1600 routing recommendations

DDR4-2400/DDR3L-1600 needs to be routed with signal fly times matched as shown in Table 21.

The delay of the via transitions needs to be included in the overall calculation. This can be realized in Allegro tool by enabling **Z Axis Delay** in **Setup** -> **Constraints**-> **Modes**.

An example of the delay match calculation has been shown for the i.MX 8MDQLQ validation board design in Table 22 and Table 23. This analysis was done for the DDR4-2400 implementation using the i.MX 8MDQLQ.

NXP recommends that users simulate their DDR implementation before fabricating PCBs.

Table 21. i.MX 8MDQLQ DDR4-2400/DDR3L-1600 routing recommendations

DDR4-2400/DDR3L-1600				
DDR4/DDR3L signal	Group	PCB + package prop delay		Considerations
		Min.	Max.	
CK_t/CK_c	Clock	Short as possible	400ps	Match the true/ complement signals within 1 ps.
A[13:0]	Address/Command/Control	CK_t - 25 ps	CK_t + 25 ps	—

Table continues on the next page...

Table 21. i.MX 8MDQLQ DDR4-2400/DDR3L-1600 routing recommendations (continued)

DDR4-2400/DDR3L-1600				
DDR4/DDR3L signal	Group	PCB + package prop delay		Considerations
		Min.	Max.	
CS[1:0]/RAS/WE/CAS BA[1:0]/BG0				
CKE[1:0]/ODT[1:0]				
DQS0_t/DQS0_c	Byte 0 - DQS	Short as possible	CK_t + 1.0 * tCK	Match the true/ complement signals of DQS within 1 ps.
DM0	Byte 0 - Data	DQS0_t -10 ps	DQS0_t +10 ps	
DQ[7:0]				
DQS1_t/DQS1_c	Byte 1 - DQS	Short as possible	CK_t + 1.0 * tCK	
DM1	Byte 1 - Data	DQS1_t -10 ps	DQS1_t +10 ps	
DQ[15:8]				
DQS2_t/DQS2_c	Byte 2 - DQS	Short as possible	CK_t + 1.0 * tCK	
DM2	Byte 2 - Data	DQS2_t -10 ps	DQS2_t +10 ps	
DQ[23:16]				
DQS3_t/DQS3_c	Byte 3 - DQS	Short as possible	CK_t + 1.0 * tCK	
DM3	Byte 3 - Data	DQS3_t -10 ps	DQS3_t +10 ps	
DQ[31:24]				

Table 22. DDR4 delay matching example (CA/CTL/CMD/CK signals)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
ACT_N U1.AE13: U4.L3	268.3	46.4	Vias are L1-> L8->L6->L8
	314.7		Total Net Delay
A0 U1.AD6: U4.P3	271.8	63.7	Vias are L1-> L4->L6->L8
	335.5		Total Net Delay
A1 U1.AE12: U4.P7	275.1	44.0	Vias are L1-> L8->L3->L8
	319.1		Total Net Delay
A2 U1.AD12: U4.R3	276.6	40.9	Vias are L1-> L4->L6->L8

Table continues on the next page...

Table 22. DDR4 delay matching example (CA/CTL/CMD/CK signals) (continued)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
	317.5		Total Net Delay
A3 U1.AC15: U4.N3	267.5	47.9	Vias are L1-> L4->L6->L8
	315.4		Total Net Delay
A4 U1.AB16: U4.N7	280.0	45.2	Vias are L1-> L8->L6->L8
	325.2		Total Net Delay
A5 U1.AE19: U4.P2	266.0	56.2	Vias are L1-> L4->L6->L8
	322.2		Total Net Delay
A6 U1.AD19: U4.P8	272.1	58.6	Vias are L1-> L8->L3->L8
	330.7		Total Net Delay
A7 U1.AD20: U4.R2	268.9	51.2	Vias are L1-> L4->L6->L8
	320.1		Total Net Delay
A8 U1.AE20: U4.R8	266.4	52.6	Vias are L1-> L8->L3->L8
	319.0		Total Net Delay
A9 U1.AB15: U4.R7	295.2	40.0	Vias are L1-> L4->L3->L8
	335.2		Total Net Delay
A10 U1.AE6: U4.M3	259.7	58.1	Vias are L1-> L4->L6->L8
	317.8		Total Net Delay
A11 U1.AE16: U4.T8	257.4	73.5	Vias are L1-> L8->L3->L8
	330.9		Total Net Delay
A12 U1.AD17: U4.M7	262.3	49.8	Vias are L1-> L8->L3->L8
	312.1		Total Net Delay
A13 U1.AC7: U4.T2	303.4	51.1	Vias are L1-> L4->L6->L8
	354.5		Total Net Delay
BA0 U1.AE7: U4.N8	263.1	49.2	Vias are L1-> L4->L3->L8
	312.3		Total Net Delay

Table continues on the next page...

Table 22. DDR4 delay matching example (CA/CTL/CMD/CK signals) (continued)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
BA1 U1.AB12: U4.N2	273.3	39.6	Vias are L1-> L4->L6->L8
	312.9		Total Net Delay
BG0 U1.AD14: U4.M2	271.9	42.7	Vias are L1-> L4->L3->L8
	314.6		Total Net Delay
CAS_N U1.AE9: U4.M8	298.5	50.2	Vias are L1-> L4->L3->L8
	348.7		Total Net Delay
CKE0 U1.AC16: U2.K2	278.0	36.5	Vias are L1-> L8->L3->L1
	314.5		Total Net Delay
CKE1 U1.AE17: U4.K2	263.9	47.4	Vias are L1-> L8->L6->L8
	311.3		Total Net Delay
CLK0_C U1.AD15: U2.K8	292.5	43.0	Vias are L1-> L6->L1
	335.5		Total Net Delay
CLK0_T U1.AE15: U2.K7	292.5	43.7	Vias are L1-> L6->L1
	336.2		Total Net Delay
CLK1_C U1.AE10: U4.K8	289.9	44.5	Vias are L1-> L3->L8
	334.4		Total Net Delay
CLK1_T U1.AD10: U4.K7	290.4	44.0	Vias are L1-> L3->L8
	334.4		Total Net Delay
CS0_N U1.AE18: U2.L7	265.2	51.0	Vias are L1-> L8->L6->L1
	316.2		Total Net Delay
CS1_N U1.AC11: U4.L7	270.6	48.2	Vias are L1-> L4->L3->L8
	318.8		Total Net Delay
ODT0 U1.AC12: U2.K3	277.2	38.2	Vias are L1-> L8->L3->L1
	315.4		Total Net Delay
ODT1 U1.AE11: U4.K3	267.0	43.8	Vias are L1-> L8->L6->L8
	310.8		Total Net Delay

Table continues on the next page...

Table 22. DDR4 delay matching example (CA/CTL/CMD/CK signals) (continued)

Net name	PCB delay (ps)[1]	Pkg delay (ps)[2]	Comments
PAR U1.AA12 U4.T3	297.4	33.3	Vias are L1-> L4->L6->L8
	330.7		Total Net Delay
RAS_N U1.AB10: U4.L8	273.8	43.1	Vias are L1-> L4->L6->L8
	316.9		Total Net Delay
WE_N U1.AC10: U4.L2	271.7	49.2	Vias are L1-> L8->L3->L8
	320.9		Total Net Delay

1. Directly from the Allegro PCB file.
2. Obtained from Table 24.

Table 23. DDR4 delay matching example (byte lane 0 signals)

Net Name	PCB Delay (ps)	Pkg Delay (ps)	Comments
DM0 U1.AD23: U4.E7	173.9	67.8	Vias are L1-> L6->L8
	241.7		Total Net Delay
DQS0_C U1.AC25: U4.F3	173.8	70.5	Vias are L1-> L6->L8
	244.3		Total Net Delay
DQS0_T U1.AC24: U4.G3	173.6	71.4	Vias are L1-> L6->L8
	245.0		Total Net Delay
DQ0 U1.AE23: U4.G2	186.1	65.9	Vias are L1-> L6->L8
	252.0		Total Net Delay
DQ1 U1.AD24: U4.H3	178.8	74.2	Vias are L1-> L6->L8
	253.0		Total Net Delay
DQ2 U1.AE22: U4.H7	180.7	56.3	Vias are L1-> L6->L8
	237.0		Total Net Delay
DQ3 U1.AD22: U4.F7	173.0	62.1	Vias are L1-> L6->L8
	235.1		Total Net Delay
DQ4 U1.AA24: U4.J7	173.4	74.3	Vias are L1-> L6->L8
	247.7		Total Net Delay

Table continues on the next page...

Table 23. DDR4 delay matching example (byte lane 0 signals) (continued)

DQ5 U1.Y25: U4.H8	181.6	72.8	Vias are L1-> L6->L8
	254.3		Total Net Delay
DQ6 U1.AA25: U4.H2	176.2	65.7	Vias are L1-> L6->L8
	241.9		Total Net Delay
DQ7 U1.AB25: U4.J3	174.1	65.4	Vias are L1-> L6->L8
	239.5		Total Net Delay

3.4.3.2 DDR4-2400 routing example (i.MX 8MDQLQ)

Figure 9 to Figure 13 show the placement and routing of the DDR4 signals on the i.MX 8MDQLQ validation board.

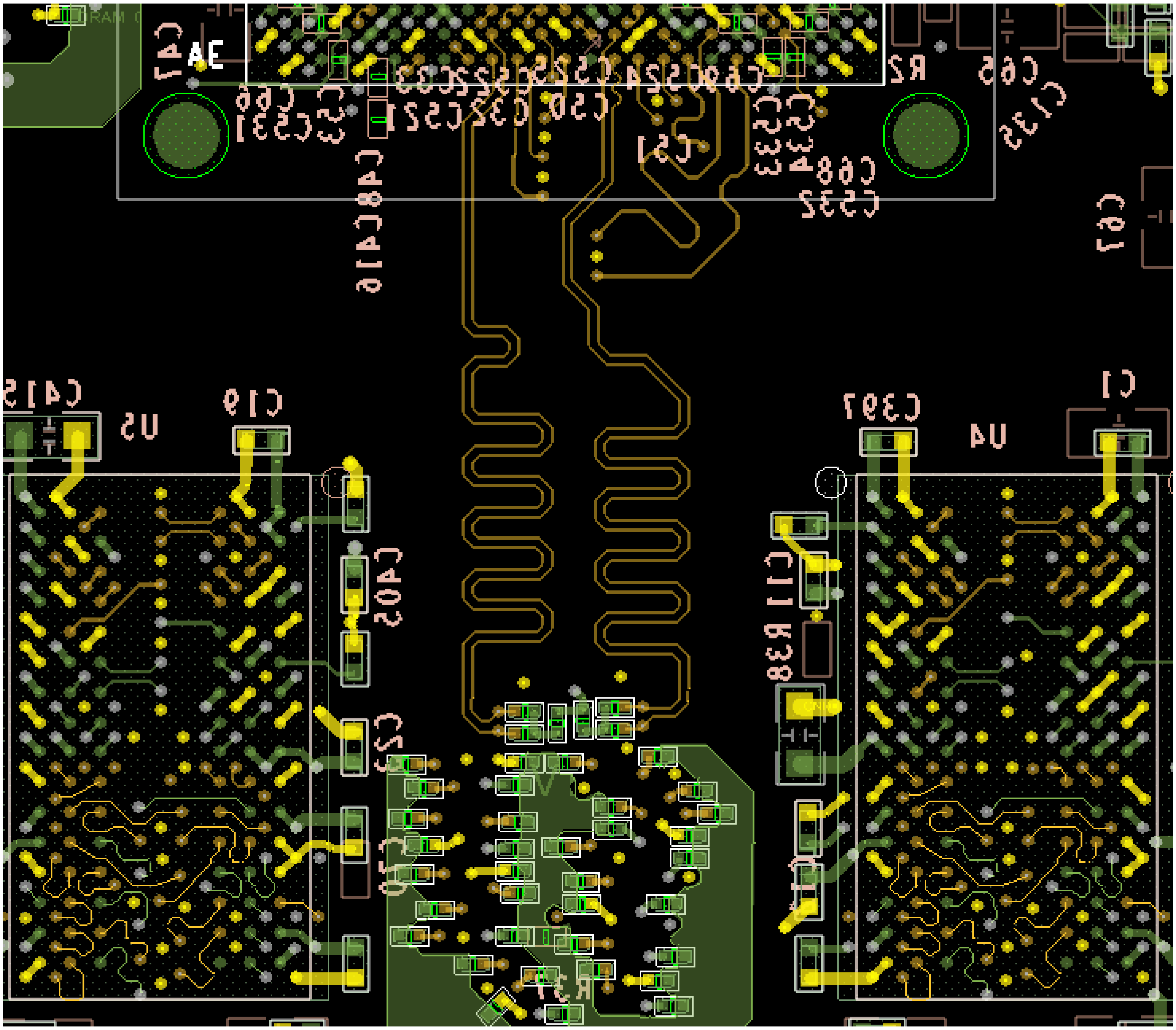

Figure 9. i.MX 8MDQLQ validation board DDR4 routing (top layer)

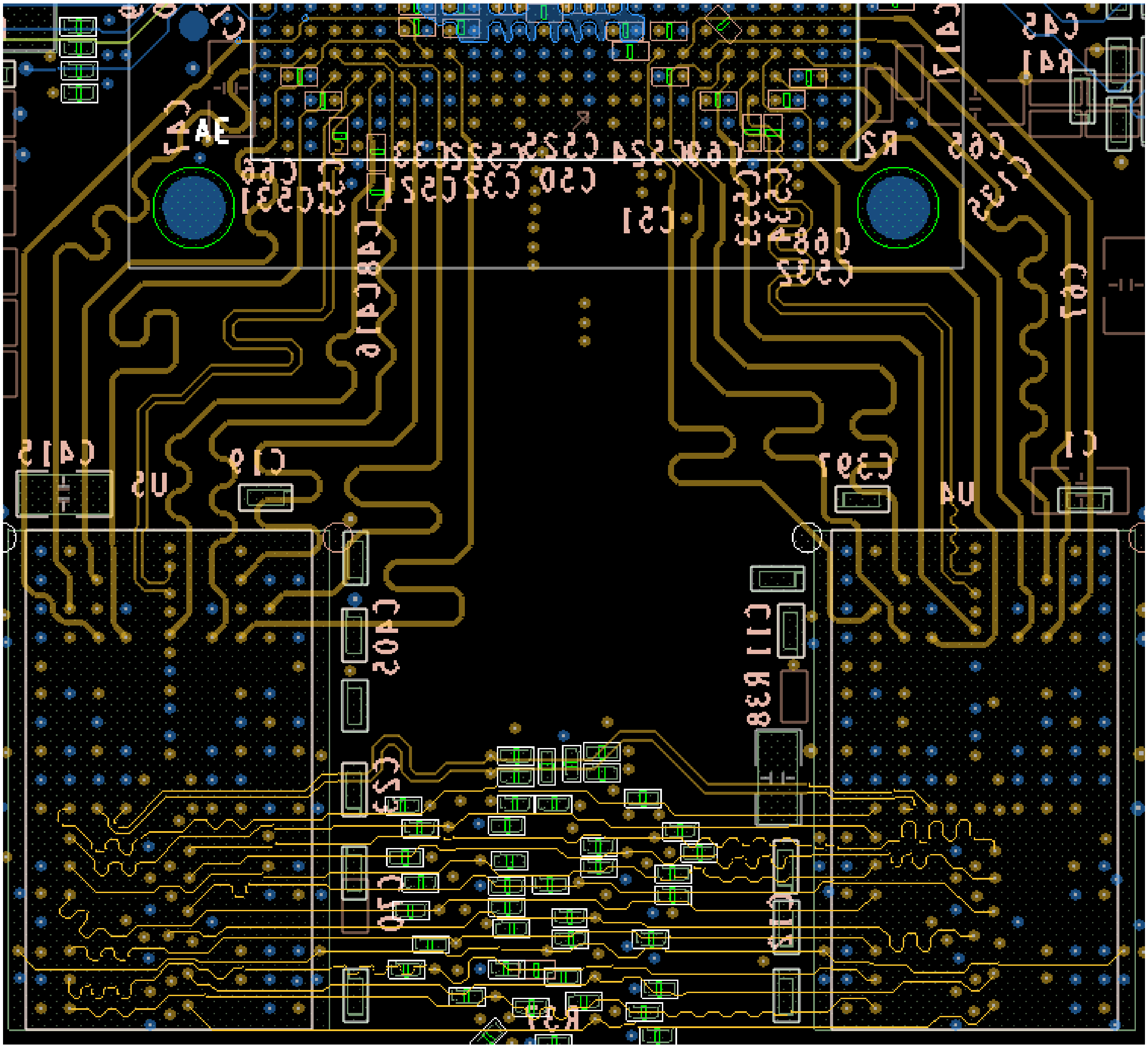

Figure 10. i.MX 8MDQLQ validation board DDR4 routing (Layer 3)

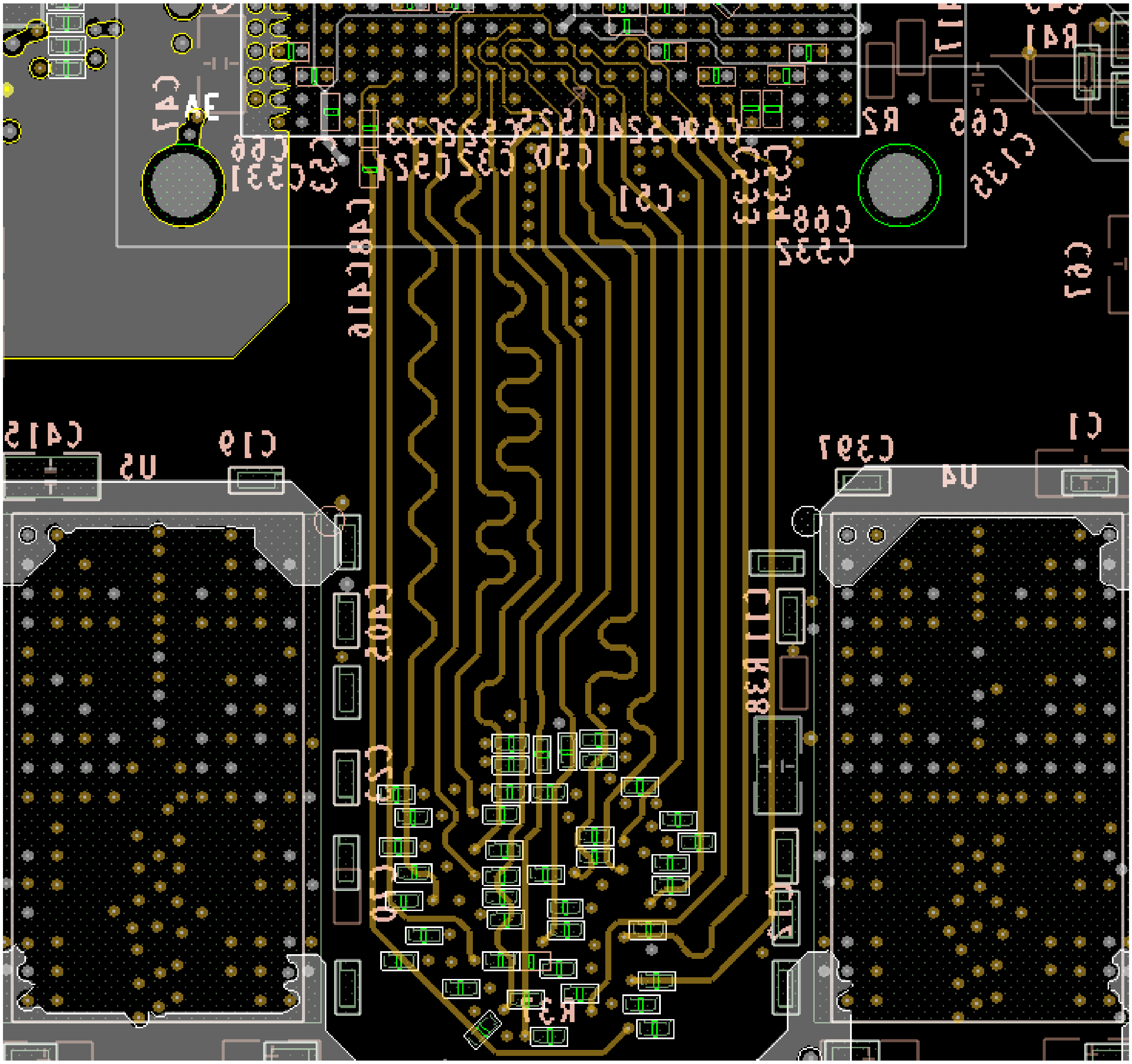

Figure 11. i.MX 8MDQLQ validation board DDR4 routing (Layer 4)

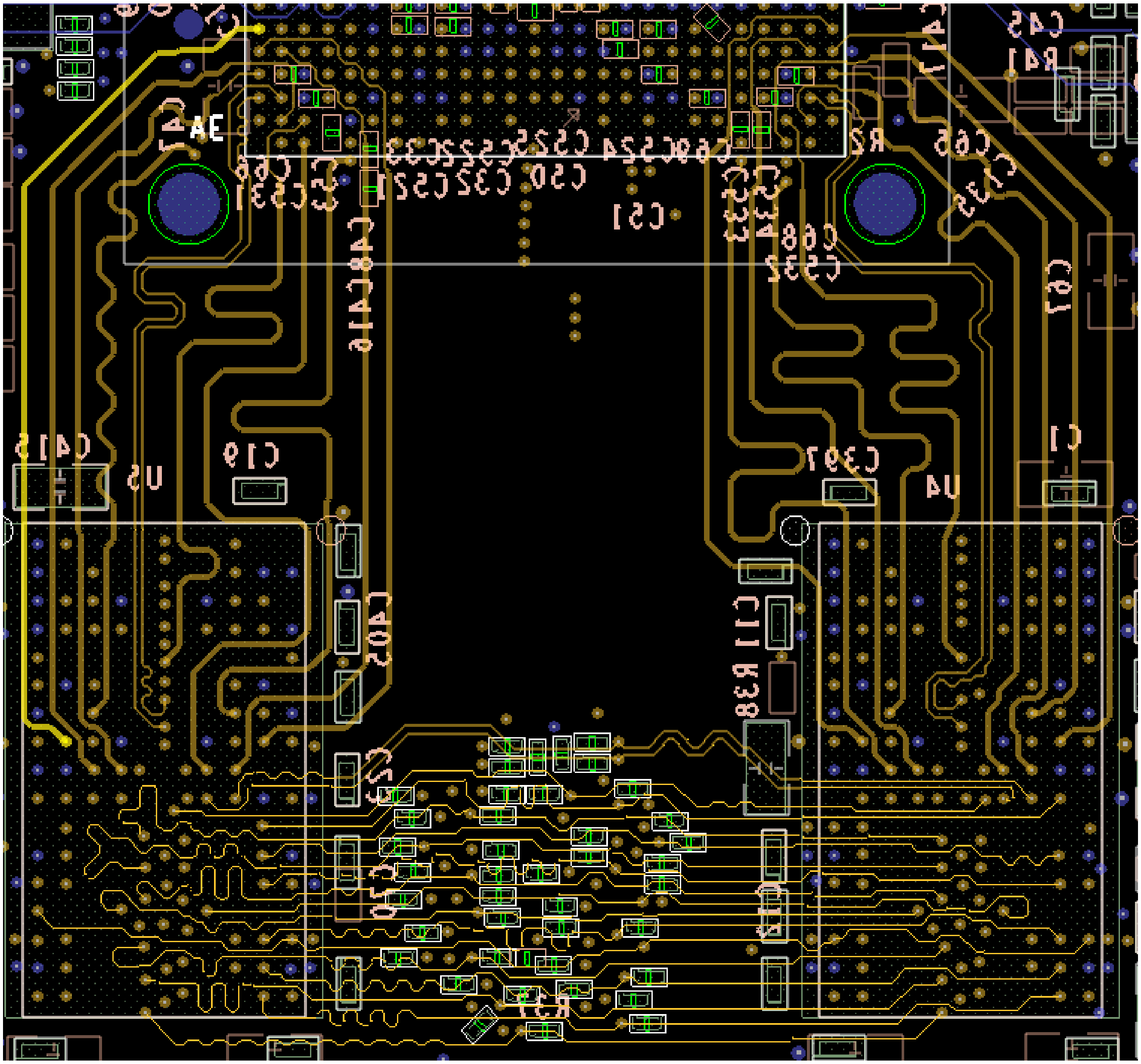

Figure 12. i.MX 8MDQLQ validation board DDR4 routing (Layer 6)

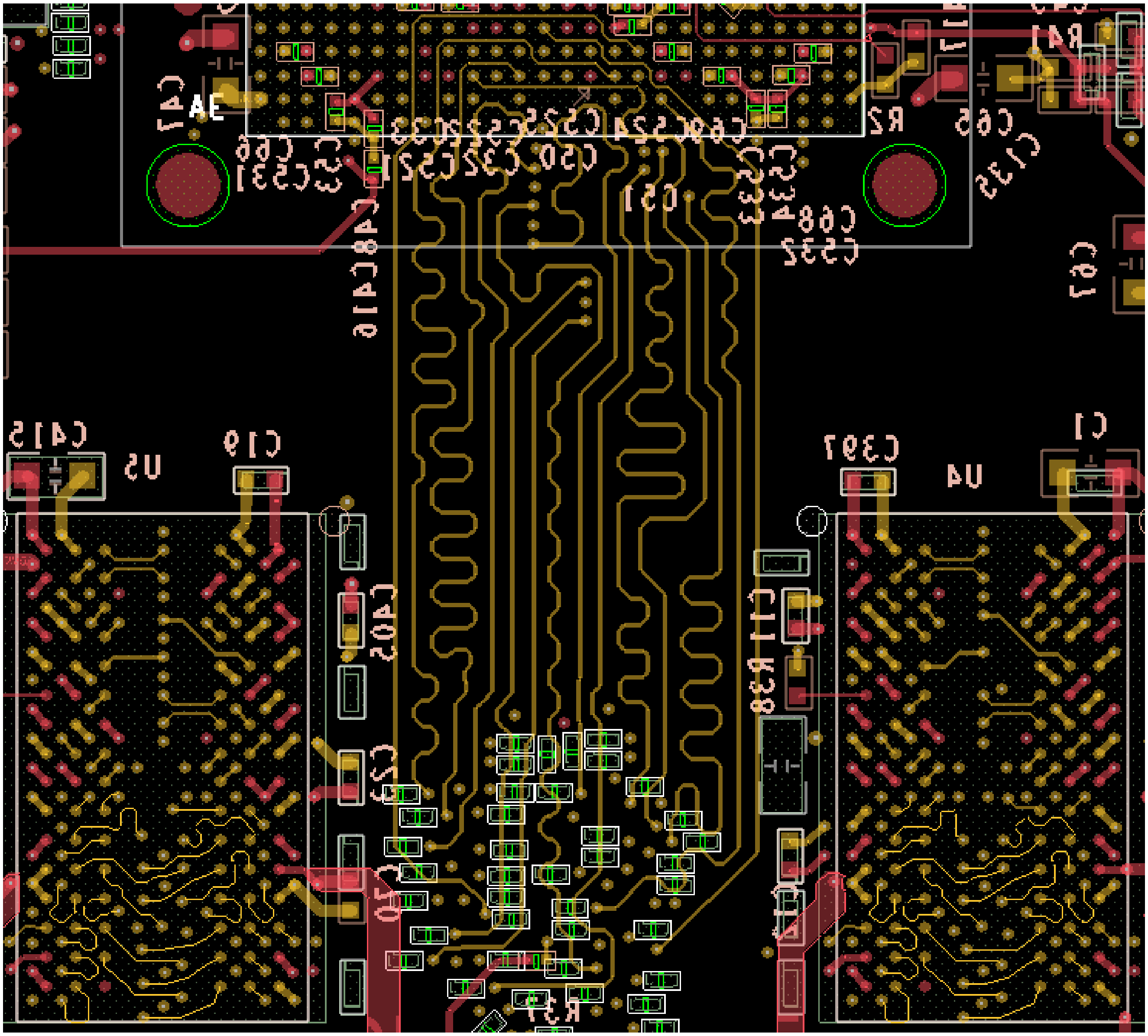

Figure 13. i.MX 8MDQLQ validation board DDR4 routing (Layer 8)

3.4.3.3 DDR3L-1600 routing example (i.MX 8MDQLQ)

Figure 14 to Figure 18 show the placement and routing of the DDR3L signals on the i.MX 8MDQLQ validation board.

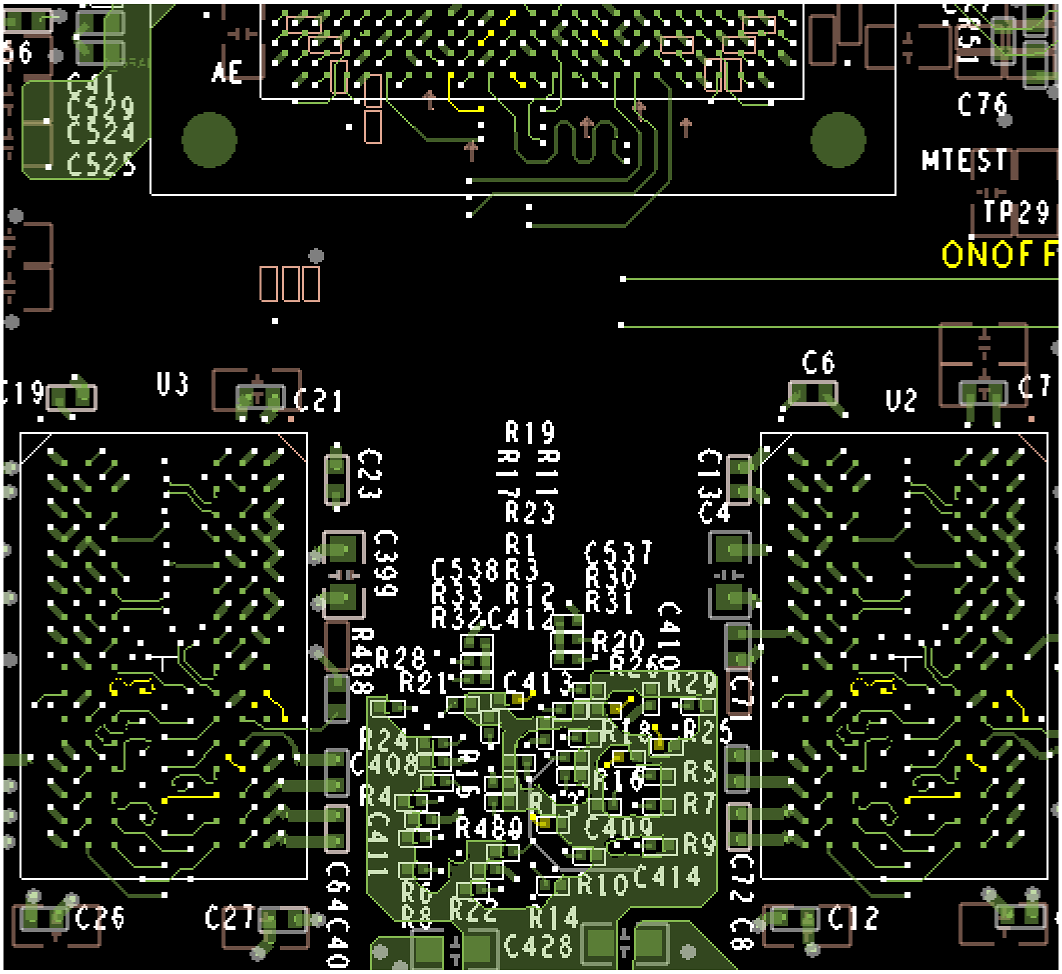

Figure 14. i.MX 8MDQLQ validation board DDR3L routing (top layer)

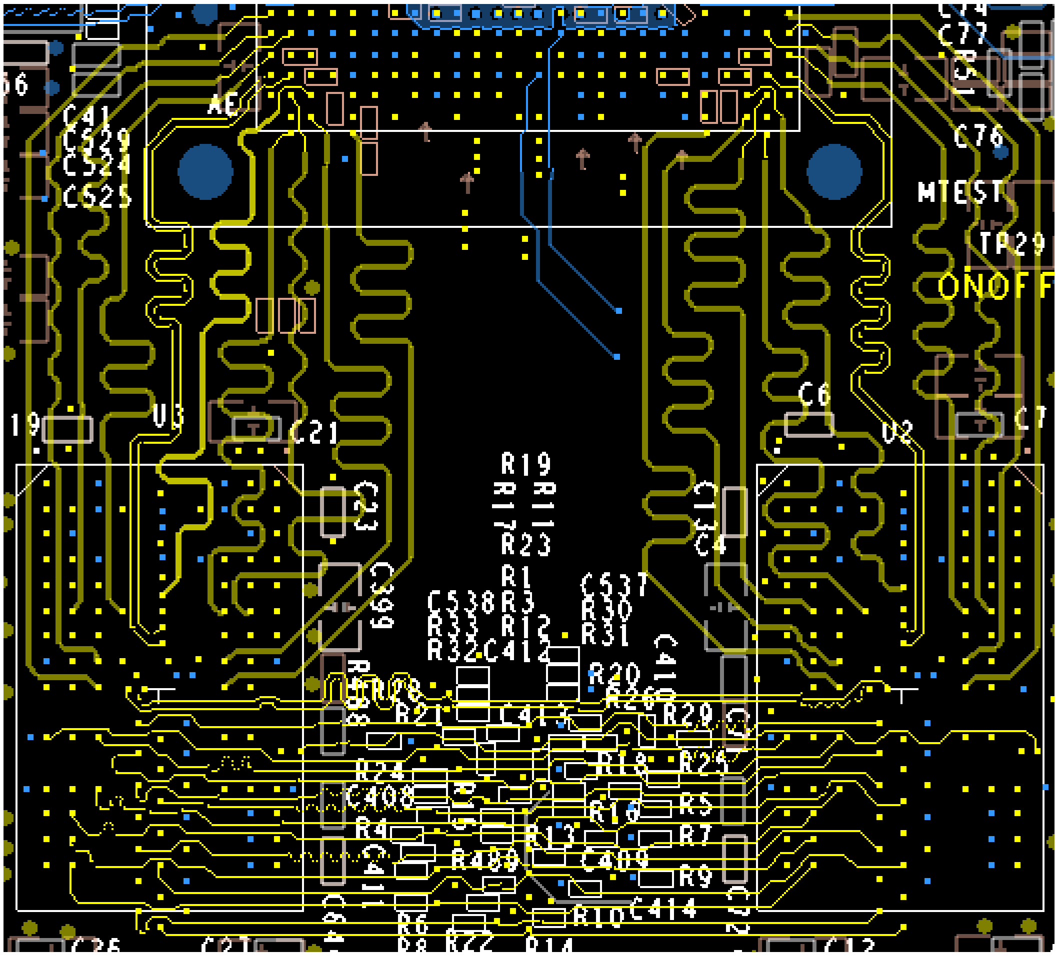

Figure 15. i.MX 8MDQLQ validation board DDR3L routing (Layer 3)

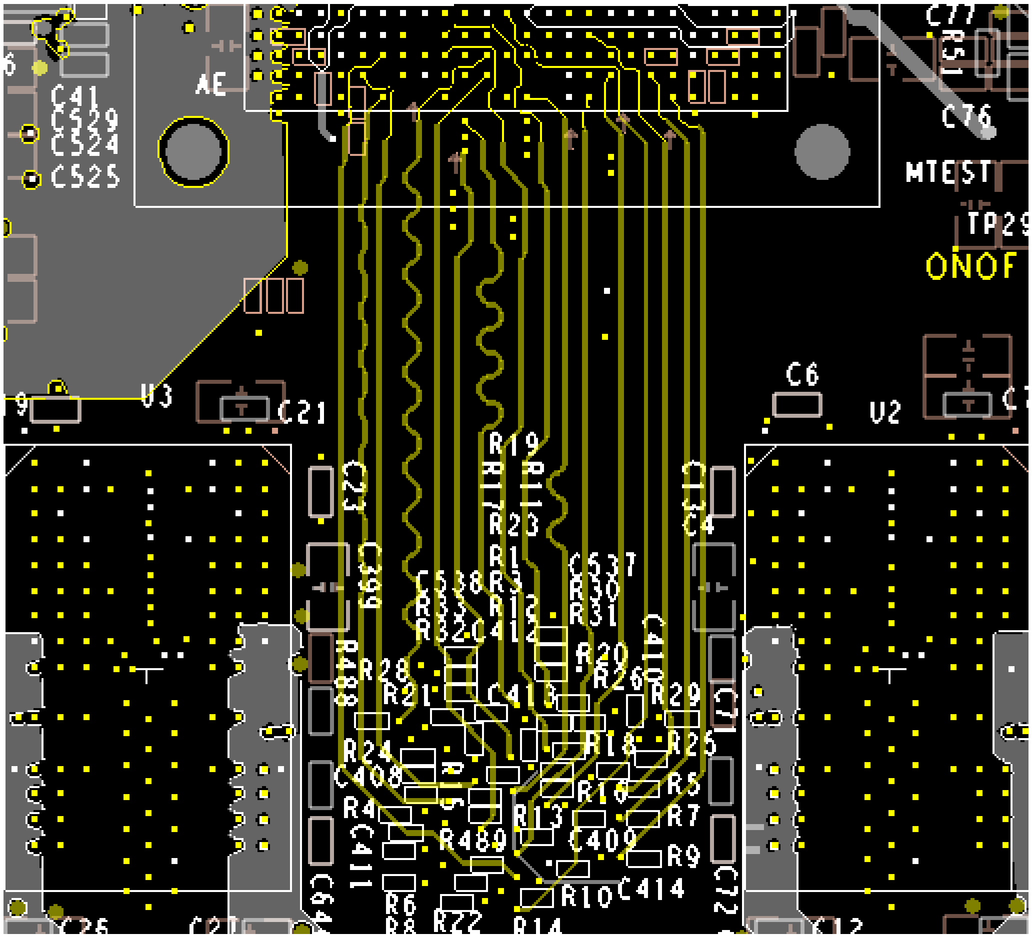

Figure 16. i.MX 8MDQLQ validation board DDR3L routing (Layer 4)

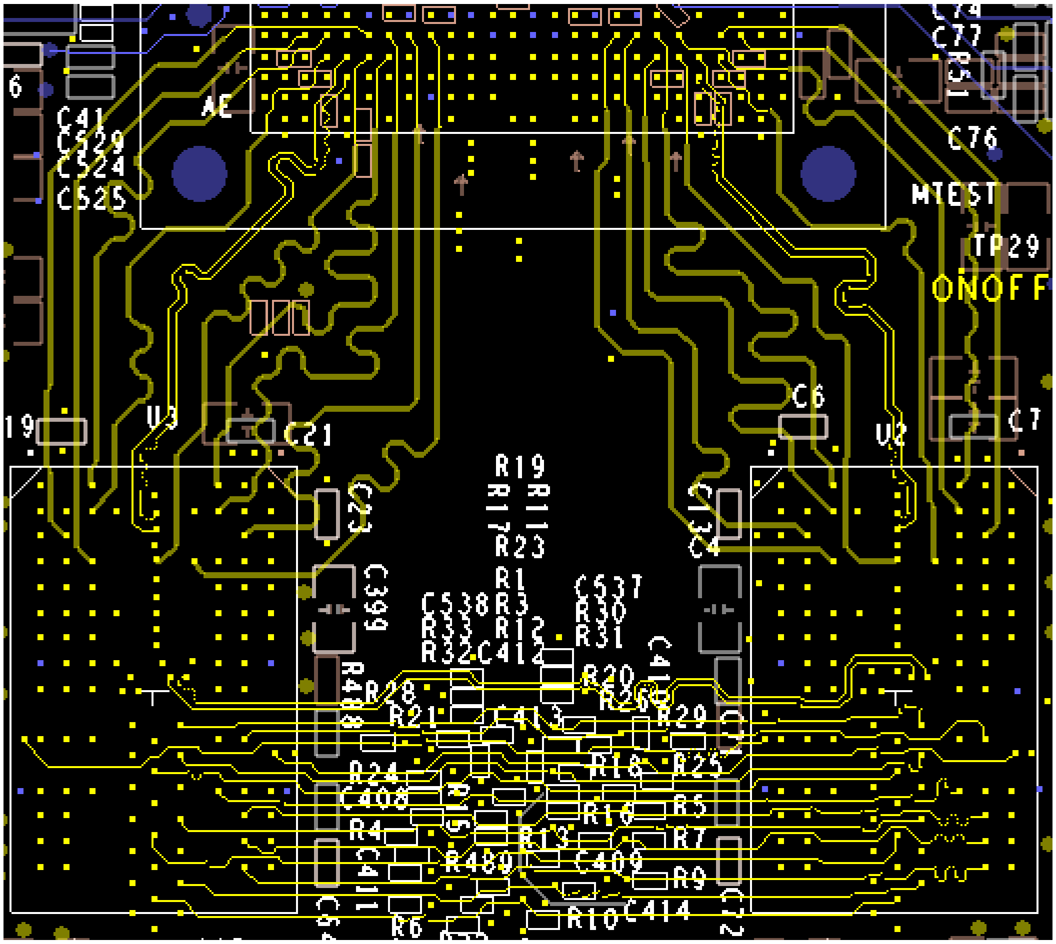

Figure 17. i.MX 8MDQLQ validation board DDR3L routing (Layer 6)

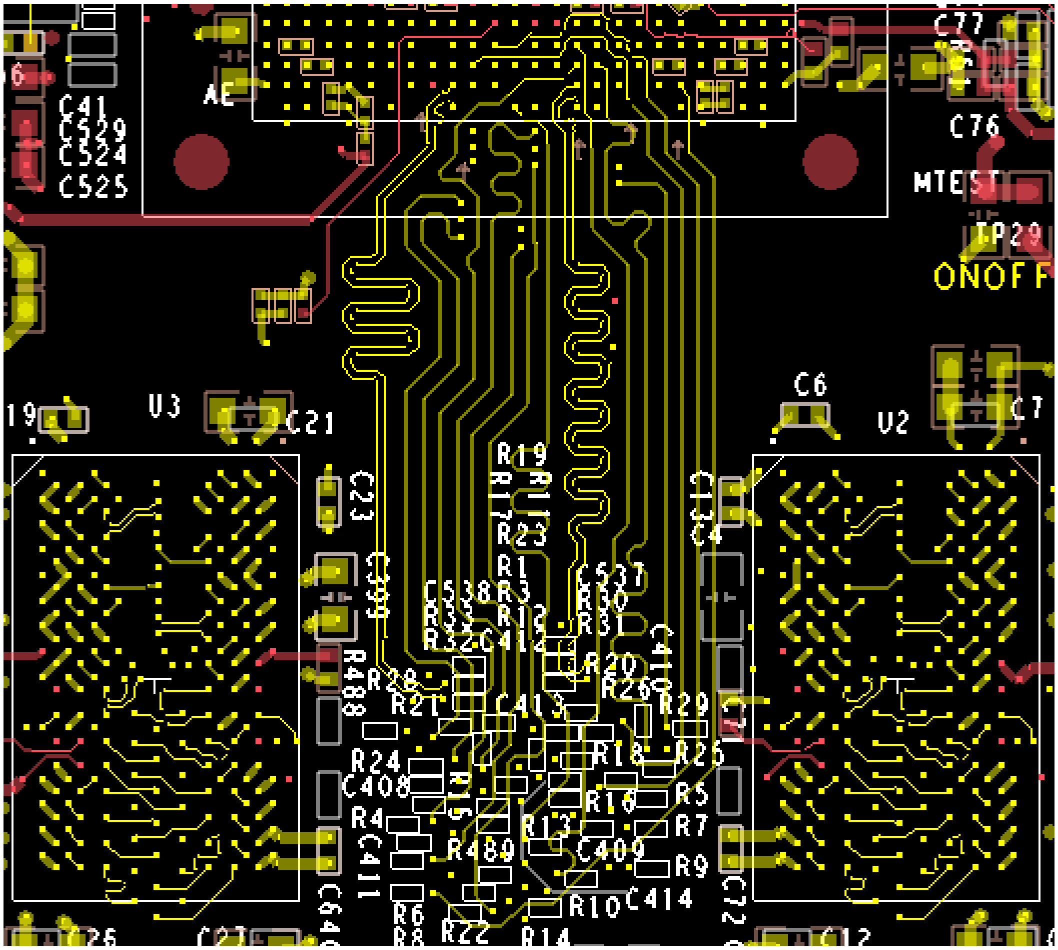

Figure 18. i.MX 8MDQLQ validation board DDR3L routing (Layer 8)

3.4.3.4 DDR4-2400/DDR3L-1600 SI simulation guide

The simulation architecture includes the DDR controller (i.e. the i.MX 8MDQLQ processor), the PCB and the DDR4/DDR3L device. The IBIS model for the i.MX 8MDQLQ processor is available from NXP. The DDR4/DDR3L device IBIS model must be obtained from the memory vendor.

This section introduces how to check SI performance of the layout for a DDR4-2400 /DDR3L-1600 design using the i.MX 8MDQLQ.

1. Perform S-parameter extraction:
    - It requires a 2.5D full-wave extraction tool, such as PowerSI from Cadence.
    - Set the extraction bandwidth to 20 GHz.
    - Port reference impedance: Set 50 Ω for signal ports and 0.1 Ω for power ports.
    - Coupled mode: Set rise time to 20 ps and coupling coefficient to 1 %.
2. Perform time domain simulation:
    - Stimulus pattern: 500-bit random code and different pattern for each signal within the same byte.
    - Ideal power.
    - Probe at the die.
    - Simulation at slow corner (worst case).

- Eye waveform triggered by aligning with the timing reference (DQS/CLK).

3.4.3.5 Eye width requirements

The simulated worst eye width should meet following requirement:

- For DDR4-2400
  — DQ Write: Eye width at threshold should be over 290 ps.
  — Add/Cmd: Eye width at threshold should be over 460 ps.
- For DDR3L-1600
  — DQ Write: Eye width at threshold should be over 380 ps.
  — Add/Cmd: Eye width at threshold should be over 660 ps.

Figure 19 shows an example of simulated eye width of DDR4-2400 DQ write.

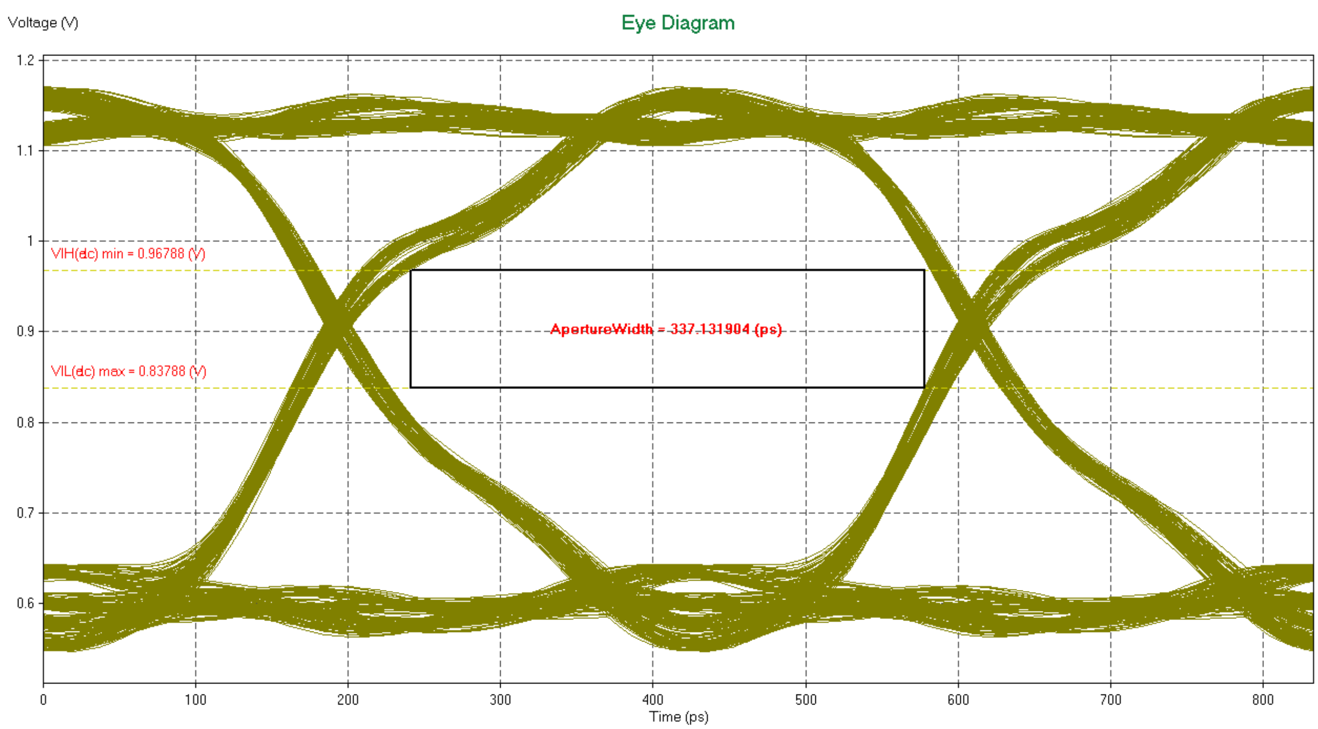

Figure 19. Example of simulated eye width

3.4.4 i.MX 8MDQLQ DDR package delay

When performing the required delay matching for LPDDR4/DDR4 routing, the bond wires within the i.MX 8MDQLQ QM package need to be accounted for and included in the match calculation. Table 24 lists the lengths from each die I/O to the package ball, as well as the propagation/fly time from the die I/O to the package ball.

Table 24. i.MX 8MDQLQ DDR package trace lengths/delays

Ball name	Length (microns)	Delay (ps)	Ball name	Length (microns)	Delay (ps)
DRAM_AC00	5474.2	36.5	DRAM_DM2	10212.9	68.1

Table continues on the next page...

Table 24. i.MX 8MDQLQ DDR package trace lengths/delays (continued)

Ball name	Length (microns)	Delay (ps)	Ball name	Length (microns)	Delay (ps)
DRAM_AC01	7103.5	47.4	DRAM_DM3	6728.3	44.9
DRAM_AC02	7654.0	51.0	DRAM_DQS0_N	10568.8	70.46
DRAM_AC03	7176.6	47.8	DRAM_DQS0_P	10711.6	71.41
DRAM_AC04	6407.3	42.7	DRAM_DQS1_N	6793.6	45.29
DRAM_AC05	6219.0	41.5	DRAM_DQS1_P	6776.4	45.18
DRAM_AC06	6954.1	46.4	DRAM_DQS2_N	10316.5	68.78
DRAM_AC07	6007.4	40.0	DRAM_DQS2_P	10746.9	71.65
DRAM_AC08	7465.4	49.8	DRAM_DQS3_N	7734.3	51.56
DRAM_AC09	11031.9	73.5	DRAM_DQS3_P	7545.1	50.30
DRAM_AC10	7685.0	51.2	DRAM_DQ00	9879.7	65.9
DRAM_AC11	7893.6	52.6	DRAM_DQ01	11130.7	74.2
DRAM_AC12	8785.9	58.6	DRAM_DQ02	8439.7	56.3
DRAM_AC13	8424.5	56.2	DRAM_DQ03	9321.9	62.1
DRAM_AC14	6785.9	45.2	DRAM_DQ04	11139.5	74.3
DRAM_AC15	7189.7	47.9	DRAM_DQ05	10920.2	72.8
DRAM_AC16	6559.5	43.7	DRAM_DQ06	9849.4	65.7
DRAM_AC17	6452.7	43.0	DRAM_DQ07	9805.5	65.4
DRAM_AC19	5633.1	37.6	DRAM_DQ08	6626.6	44.2
DRAM_AC20	6609.6	44.1	DRAM_DQ09	6975.4	46.5
DRAM_AC21	6681.6	44.5	DRAM_DQ10	8074.3	53.8
DRAM_AC22	8329.9	55.5	DRAM_DQ11	6518.8	43.5
DRAM_AC23	8004.5	53.4	DRAM_DQ12	6734.6	44.9
DRAM_AC24	6129.2	40.9	DRAM_DQ13	6746.1	45.0
DRAM_AC25	6594.4	44.0	DRAM_DQ14	5300.8	35.3
DRAM_AC26	5941.5	39.6	DRAM_DQ15	6053.7	40.4
DRAM_AC27	4994.3	33.3	DRAM_DQ16	9074.1	60.5

Table continues on the next page...

Table 24. i.MX 8MDQLQ DDR package trace lengths/delays (continued)

Ball name	Length (microns)	Delay (ps)	Ball name	Length (microns)	Delay (ps)
DRAM_AC28	7671.3	51.1	DRAM_DQ17	10708.2	71.4
DRAM_AC29	7386.5	49.2	DRAM_DQ18	10055.7	67.0
DRAM_AC30	8720.1	58.1	DRAM_DQ19	9854.4	65.7
DRAM_AC31	9555.6	63.7	DRAM_DQ20	11381.6	75.9
DRAM_AC32	7136.8	47.6	DRAM_DQ21	10925.5	72.8
DRAM_AC33	7525.5	50.2	DRAM_DQ22	10193.4	68.0
DRAM_AC34	7377.9	49.2	DRAM_DQ23	9977.5	66.5
DRAM_AC35	6469.0	43.1	DRAM_DQ24	7588.0	50.6
DRAM_AC36	5730.8	38.2	DRAM_DQ25	7241.9	48.3
DRAM_AC37	6570.7	43.8	DRAM_DQ26	8836.6	58.9
DRAM_AC38	7224.1	48.2	DRAM_DQ27	5774.4	38.5
DRAM_ALERT_N	6065.6	40.4	DRAM_DQ28	5579.5	37.2
DRAM_RESET_N	4480.6	29.9	DRAM_DQ29	6855.0	45.7
DRAM_DM0	10176.3	67.8	DRAM_DQ30	4834.7	32.2
DRAM_DM1	6512.0	43.4	DRAM_DQ31	4239.0	28.3

3.4.5 High-speed routing recommendations

The following lists the routing traces for high speed signals. The propagation delay and the impedance control should match to ensure the correct communication with the devices.

- High-speed signals (DDR, PCIe, RGMII, MIPI, etc.) must not cross gaps in the reference plane.
- Avoid creating slots, voids and splits in reference planes. Review via placements to ensure that they don’t inadvertently create splits/voids (i.e. space vias out to eliminate this possibility).
- Ensure that ground stitching vias are present within 50 mils from signal layer transition vias on high speed signals when transitioning between different reference ground planes.
- A solid GND plane must be directly under crystals, associated to components and traces.
- Clocks or strobes that are on the same layer need at least 2.5x height from reference plane spacing from adjacent traces to reduce crosstalk.
- All synchronous interfaces should have appropriate bus length matching and relative clock length control.

For SD module interfaces:

- Match data and CMD trace lengths (allowable delta depends on the access rate being used).
- CLK should be longer than the longest signal in the Data/CMD group (+5 mils).

3.4.6 Reset architecture/routing

A debounced reset button may be logical connected to EN pin of PMIC and other discrete power supply chips for development purposes. This allows all voltages to be put to their initial default power-on state when depressing the reset button. See Figure 20 for a diagram example of the reset functionality.

Pressing the reset button causes the supervisor IC at U704 to assert its RESETn output. This will power down the `VDD_SOC_0V9` and make `PMIC_ON` pulled low by PG signal of U705. Since `PMIC_ON` serves as the enable signal of PMIC and other discrete power supply chips, all the power supplies except for the SNVS domain will be OFF. The RESETn will keep asserted for 240 ms after the button is released, thus providing enough time for the power supplies to be completely powered down. During this time, the `POR_B` driven by the PMIC will also keep asserted (low). After RESETn is released, the power supplies will start to ramp up in defined sequence. When all the power supplies have reached their operating voltages, `POR_B` will be de-asserted, and the CPU may begin booting from reset.

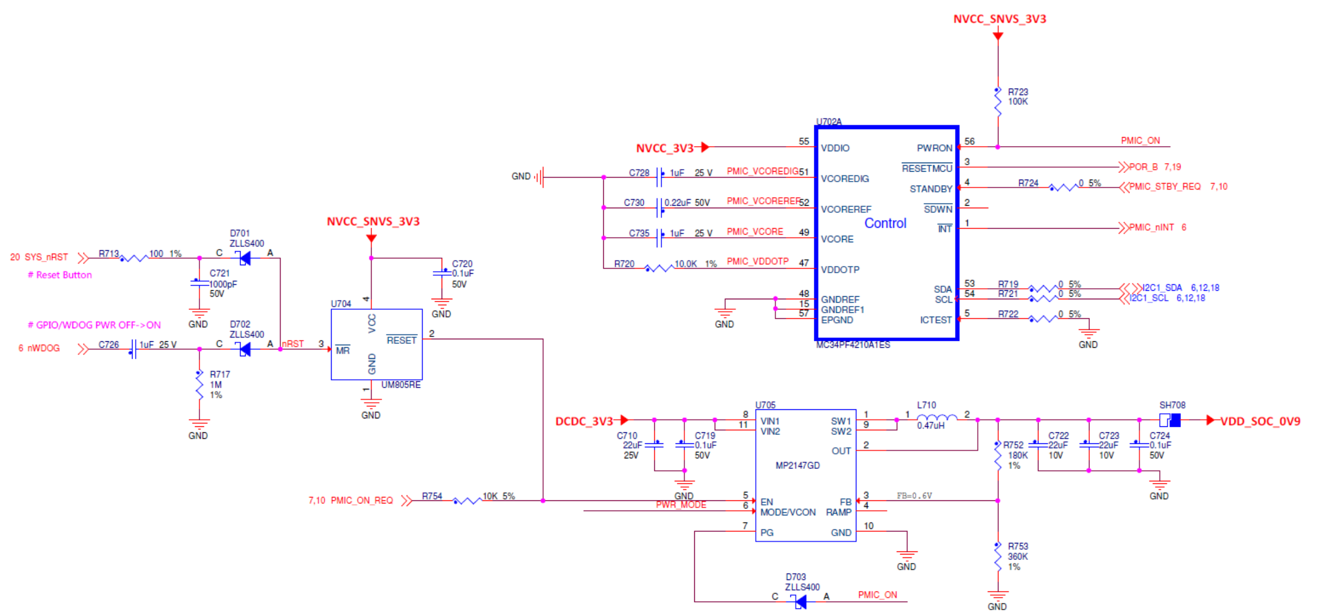

Figure 20. i.MX 8MDQLQ reset routing

3.5 Trace impedance recommendations

Table 25 is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/ trace widths.

Table 25. Trace impedance recommendations

Signal group	Impedance	PCB manufacturer tolerance (+/-)
LPDDR4 DQ, DMI signals	42 Ω single-ended	10%
All single-ended signals, unless specified	50 Ω single-ended	10%
DDR DQS/CLK, PCIe TX/RX data pairs	85 Ω Differential	10%
USB differential signals	90 Ω differential	10%
Differential signals, including Ethernet, PCIe clocks, HDMI, MIPI (CSI and DSI)	100 Ω Differential	10%

Figure 21 shows the dimensions of a stripline and microstrip pair. Figure 22 shows the differential pair routing.

- The space between two adjacent differential pairs should be greater than or equal to twice the space between the two individual conductors.
- The skew between HDMI pairs should be within the minimum recommendation (±100 mil).

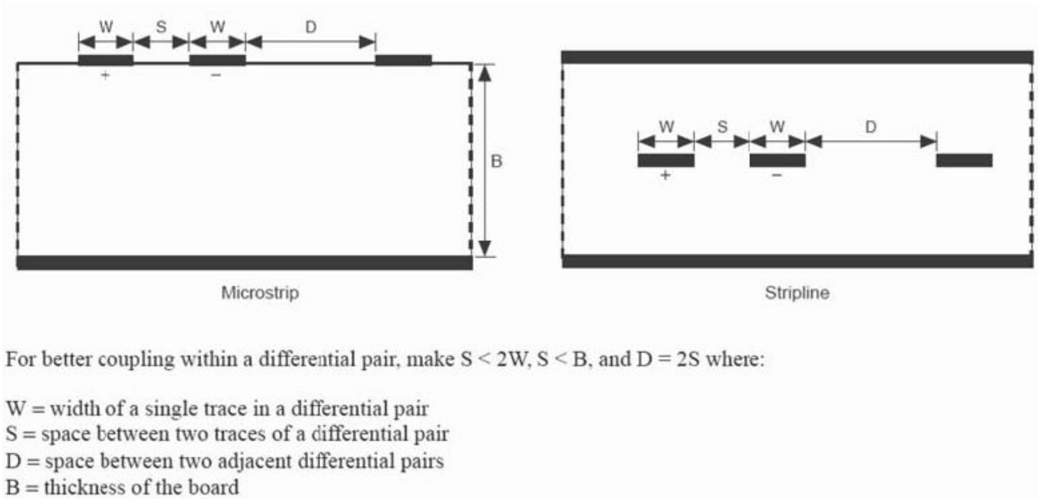

Figure 21. Microstrip and stripline differential pair dimensions

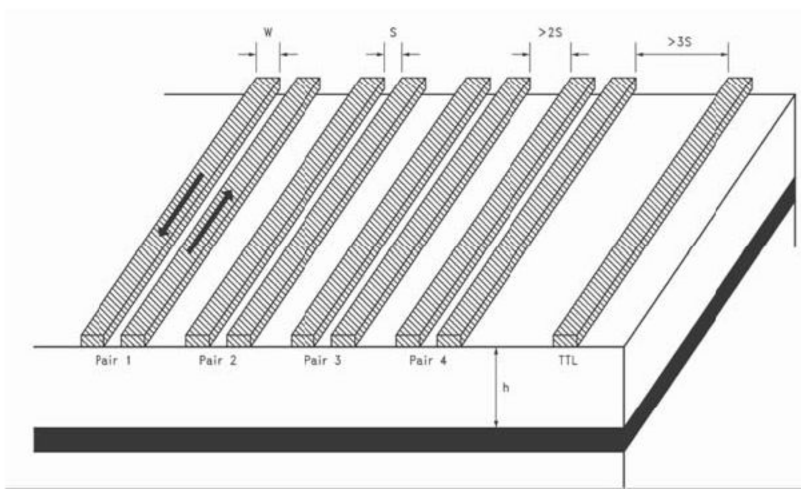

Figure 22. Differential pair routing

3.6 Power connectivity/routing

Delivering clean, reliable power to the i.MX 8MDQLQ internal power rails is critical to a successful board design. The PCB PDN should be designed to accommodate the maximum output current from each SMPS into the i.MX 8MDQLQ supply balls. Table 26 lists the design goals for each high-current i.MX 8MDQLQ power rail.

Table 26. i.MX 8MDQLQ maximum current design levels

Supply input	i.MX 8MDQLQ Max current
VDD_ARM	4 A

Table continues on the next page...

Table 26. i.MX 8MDQLQ maximum current design levels (continued)

Supply input	i.MX 8MDQLQ Max current
VDD_SOC	3.6 A
VDD_GPU	2 A
VDD_VPU	1 A
VDD_DRAM	2.5 A
NVCC_DRAM	1 A

3.6.1 i.MX 8MDQLQ power distribution block diagram

There are companion PMICs that provide a low-cost and efficient solution for powering the i.MX 8MDQLQ processor.

Figure 23 shows a block diagram of the power tree of the NXP i.MX 8MDQLQ EVK board. It uses a single PF4210 PMIC with several discrete buck converters to power ON rails of the processor.

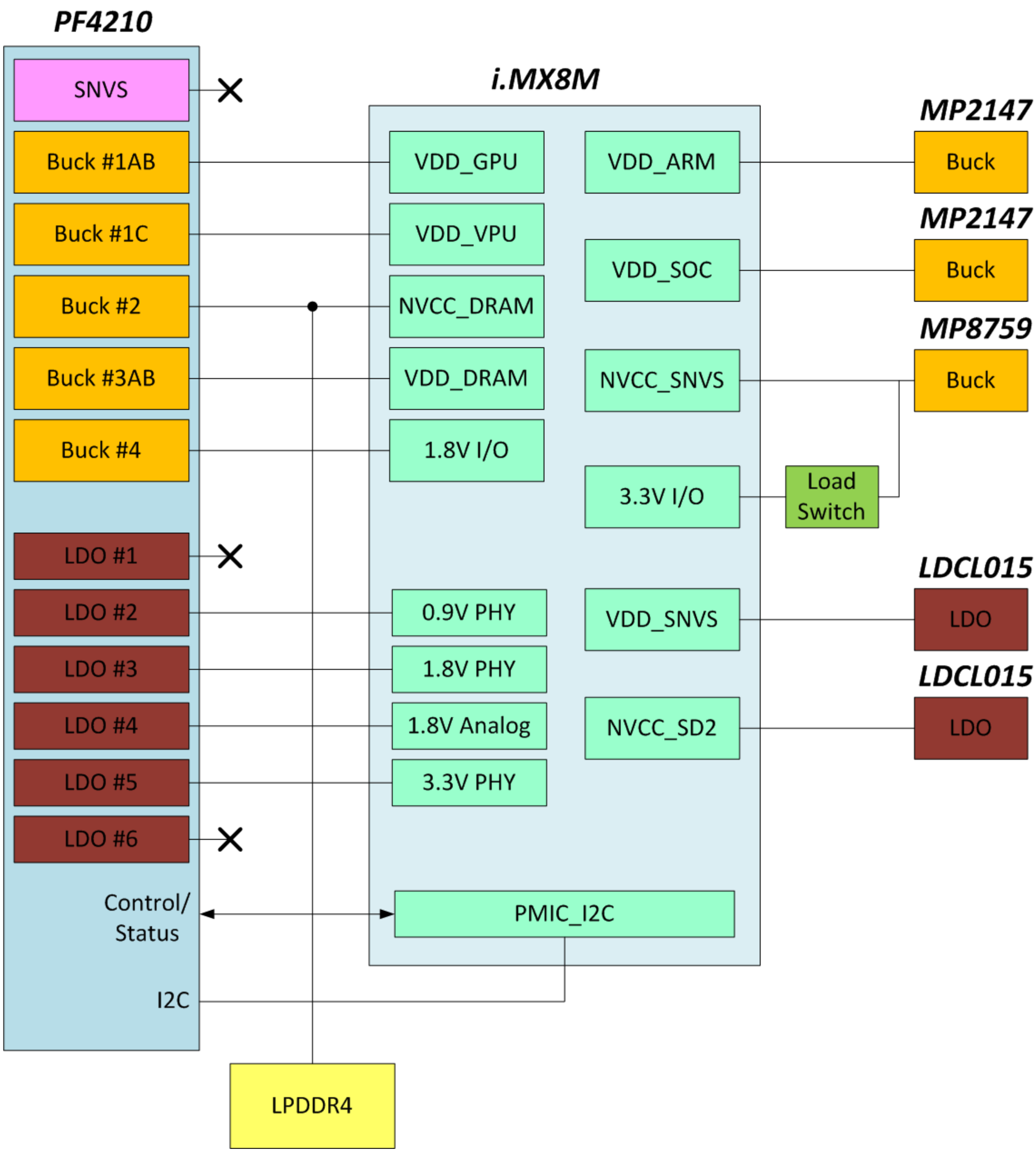

Figure 23. i.MX 8MDQLQ development platform power distribution block diagram

3.6.2 Power routing/distribution requirements

The designing for a good Power Delivery Network (PDN) is complicated. It includes:

1. Choose a good PCB stackup (adequate Cu thicknesses, and layer assignments/utilization).

2. Optimize the placement and routing of the PDN. This includes good placement of the decoupling capacitors and connecting them to the power ground planes with as short and wide a trace as possible (as the increased inductance of a longer etch will degrade the effectivity of the capacitor). Use the number/placement of capacitors on the NXP development platforms.
3. Optimize DC IR drop. This involves using very wide traces/plane fills to route high-current power nets and ensure an adequate number of vias on power net layer transitions. Neck down of fill areas should be minimized and current density minimized. The maximum DC IR drop on a board should be 2 % (preferably 1 %) of the voltage rail (i.e. on a 1.1V rail, the maximum voltage drop should be less than 0.022 V, preferably less than 0.011 V). See Table 27 for the DC IR drop requirement.

Table 27. i.MX 8MDQLQ DC IR drop requirements

Supply input	Nominal voltage (V)	Max current (mA)	IR drop target	Corresponding power path resistance requirement
VDD_ARM	0.9	4000	< 2 %	< 4.5 mΩ
VDD_SOC	0.9	3600	< 2 %	< 5 mΩ
VDD_GPU	0.9	2000	< 2 %	< 9 mΩ
VDD_VPU	0.9	1000	< 2 %	< 18 mΩ
VDD_DRAM	0.9	2500	< 2 %	< 7.2 mΩ
NVCC_DRAM	1.1	1000	< 2 %	< 22 mΩ

4. AC impedance check – the target impedance at different frequencies should be below specified values. See Table 28 for the impedance targets vs. frequency for specified power rail for the i.MX 8MDQLQ PCB design.

Table 28. i.MX 8MDQLQ PDN impedance requirements

Supply input	< 20 MHz (mΩ)	20 - 100 MHz (mΩ)
VDD_ARM	13.5	63
VDD_SOC	12	50
VDD_GPU	20	90
VDD_VPU	40	150
VDD_DRAM	15	50
NVCC_DRAM	7	30

3.7 USB connectivity

The i.MX 8MDQLQ provides two complete USB3.0 interfaces and the following configurations (or any subset) are supported:

- Dedicated host or device using Type-A connector or Type-B connector.
- Dual role using Type-C connector.

To implement a USB Type-C interface (UFP, DFP, or DRP), external hardware must be added to manage the two configuration channel IOs (CC1 and CC2) as well as monitor the plug orientation and switch the single USB3 SS interface.

See the NXP development platform schematic for an example USB Type-C implementation.

3.7.1 USB routing recommendations

Use the following recommendations when routing USB signals:

- Route the DP/DM and SS_TX/SS_RX differential pairs first.
- Route DP/DM and SS_TX/SS_RX signals on the top or bottom layer of the board if possible:
  - Keep DP/DM and SS_TX/SS_RX traces as short as possible.
  - Route DP/DM and SS_TX/SS_RX signals with a minimum number of corners. Use 45ºo turns instead of 90º turns.
  - Minimize the number of vias on DP/DM and SS_TX/SS_RX signals. Do not create stubs or branches.
- The trace width and spacing of the DP/DM and SS_TX/SS_RX signals should meet the differential impedance requirement of 90 Ω.
- Route traces over continuous planes (power and ground).
  - They should not pass over any power/GND plane slots or anti-etch.
- When placing connectors, make sure the ground plane clearouts around each through hole pin have ground continuity between all pins.
- Maintain symmetric routing for each differential pair. Keep the delay skew between P and N less than 1 ps.
- Do not route DP/DM and SS_TX/SS_RX traces under oscillators or parallel to clock traces and/or data buses.
- Minimize the lengths of high speed signals that run parallel to the DP/DM and SS_TX/SS_RX pairs.
- Provide ground return vias within 50 mils distance from signal layer-transition vias when transitioning between different reference ground planes.

✓ 3.8 HDMI port connectivity (i.MX 8MDQLQ)

The i.MX 8MDQLQ provides an HDMI transmitter capable of supporting an HDMI2.0 compatible output.

shows the HDMI connectivity. For the HDMI output, 604 Ω resistors on the positive and negative sides of each high-speed output pair are grounded through a FET. The gate to this FET should be tied to the 1.8 V power for the HDMI transmit circuitry (HDMI_AVDDIO, ball P2). This will disconnect the resistors automatically when the HDMI transmit circuitry is powered down. Although a single FET is adequate to achieve the functionality, a dedicated FET for each signal can provide better isolation between signals and minimize crosstalk.

When configured as HDMI output, the two pins named `HDMI_REFCLK_P` and `HDMI_REFCLK_N` are not clock output to the connector. They are input pins to provide 27 MHz reference clock to the HDMI PHY to improve jitter performance. The reference clock is generated by an external oscillator supporting HCSL compatible output. Table 29 lists the specifications of the reference clock.

Table 29. HDMI external reference clock specification

Normative electrical parameter	Specification			Unit	Conditions
	Min.	Typ.	Max.		
External clock frequency	—	27	1	MHz	—
Input duty	45	—	55	%	—
Differential peak-to-peak amplitude at pin	0.5	—	2.2	V	—
Rise/Fall time (10–90 %)	—	—	200	ps	—

Table continues on the next page...

Table 29. HDMI external reference clock specification (continued)

Normative electrical parameter	Specification			Unit	Conditions
	Min.	Typ.	Max.		
Input random jitter	—	—	-140	dBC/Hz	Noise floor density from 10 KHz to 10 MHz.
	—	—	2.963	ps	For a 27 MHz reference, integrated jitter from 10 KHz to 10 MHz.
Input determines tic jitter	—	—	—	ps	Over a band of 10 KHz to 10 MHz.

The true HDMI clock output pins are HDMI_TX_P_LN_3 and HDMI_TX_M_LN_3. They are connected to the HDMI connector, as shown in Figure 24.

Figure 24 does not show optional circuitry (i.e. common mode chokes).

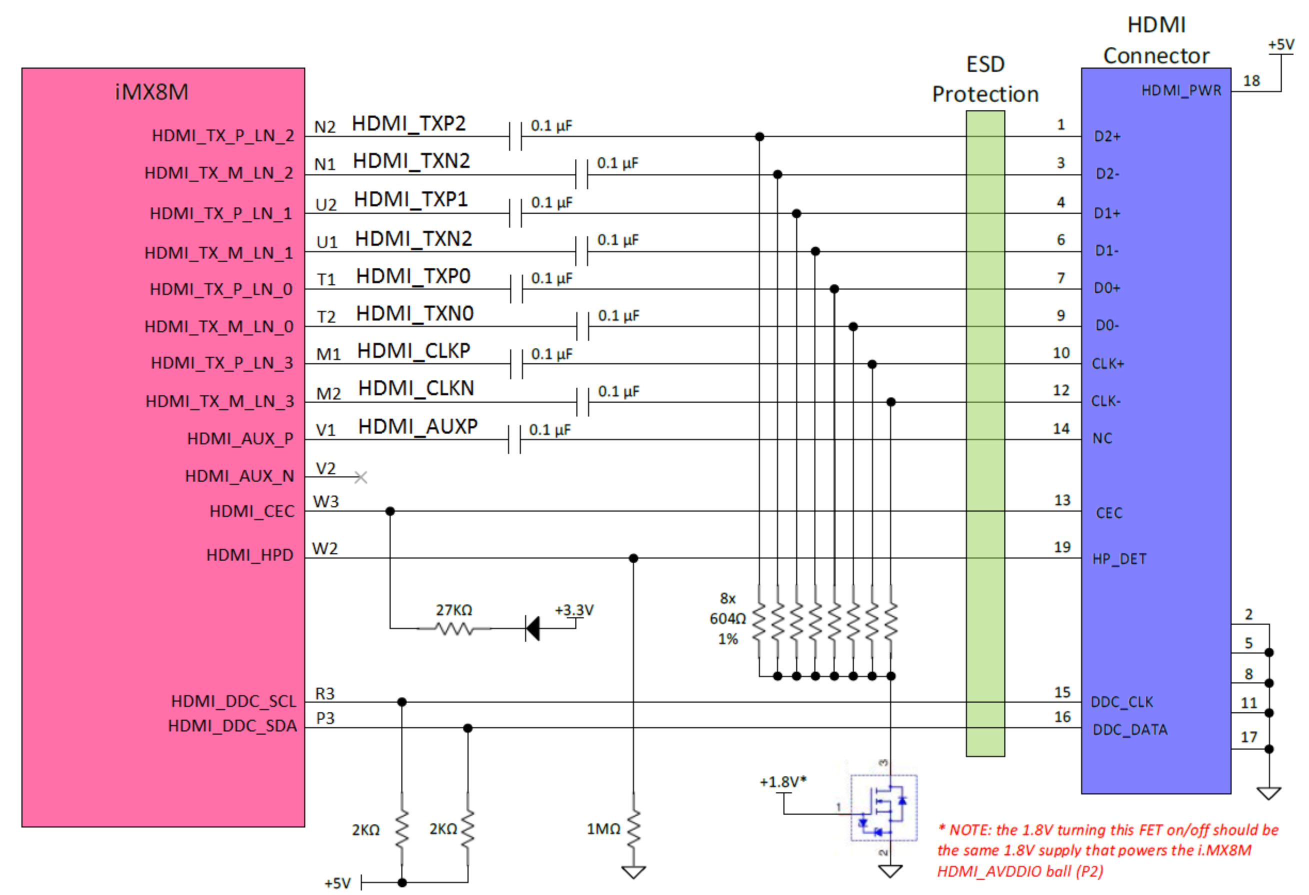

Figure 24. HDMI output connectivity

When planning the HDMI interface, place the 604 Ω pull-down resistors directly on the signal trace, as shown in Figure 25.

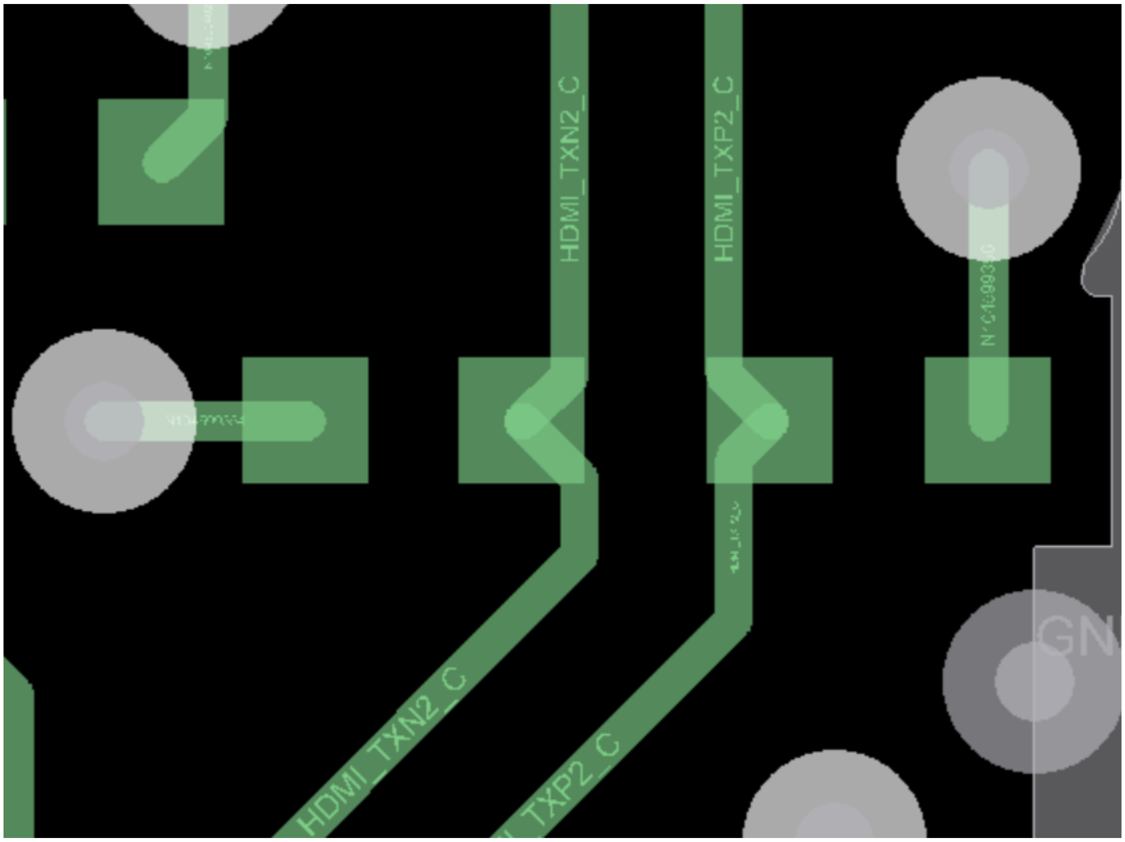

Figure 25. HDMI interface pull-down resistor placement

3.9 PCIE connectivity

The i.MX 8MDQLQ has two PCIE interfaces. Each has a pair of pins with the name of `PCIEx_REF_PAD_CLK_P/N`. The pins are used to feed 100 MHz reference clock to the PHY from external clock source. They are input-only pins and have no capability to output clock. Do not connect them to PCIE connector or PCIE device.

A PCIE clock generator chip (i.e. 9FGV0241) is used to feed high quality clock to both the PHY and connecter/device. If a PCIE clock generator is not available, use the internal clock of the chip as the clock source of the PHY. The internal clock can be output from `CLK2_P/N` (ball T22 and U22) to provide clock to the connector/device. The internal clock exhibits larger jitter than that from PCIE clock generator.

To support PCIE L1.1 and L1.2 PM substate, a bidirectional open-drain clock request (`CLKREQ#`) signal is required for entry to and exit from these two states. This can be realized by connecting a GPIO, configured as open-drain, directly to `CLKREQ#` signal of the PCIE peripheral and the clock generator. Figure 26 shows the connection diagram and Figure 27 shows the reference schematic.

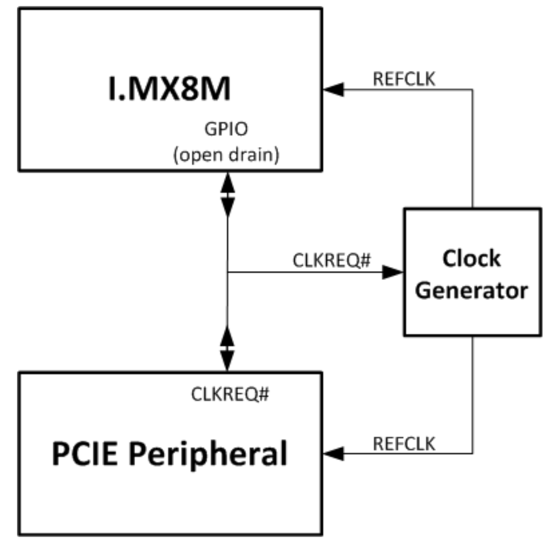

Figure 26. Connection diagram

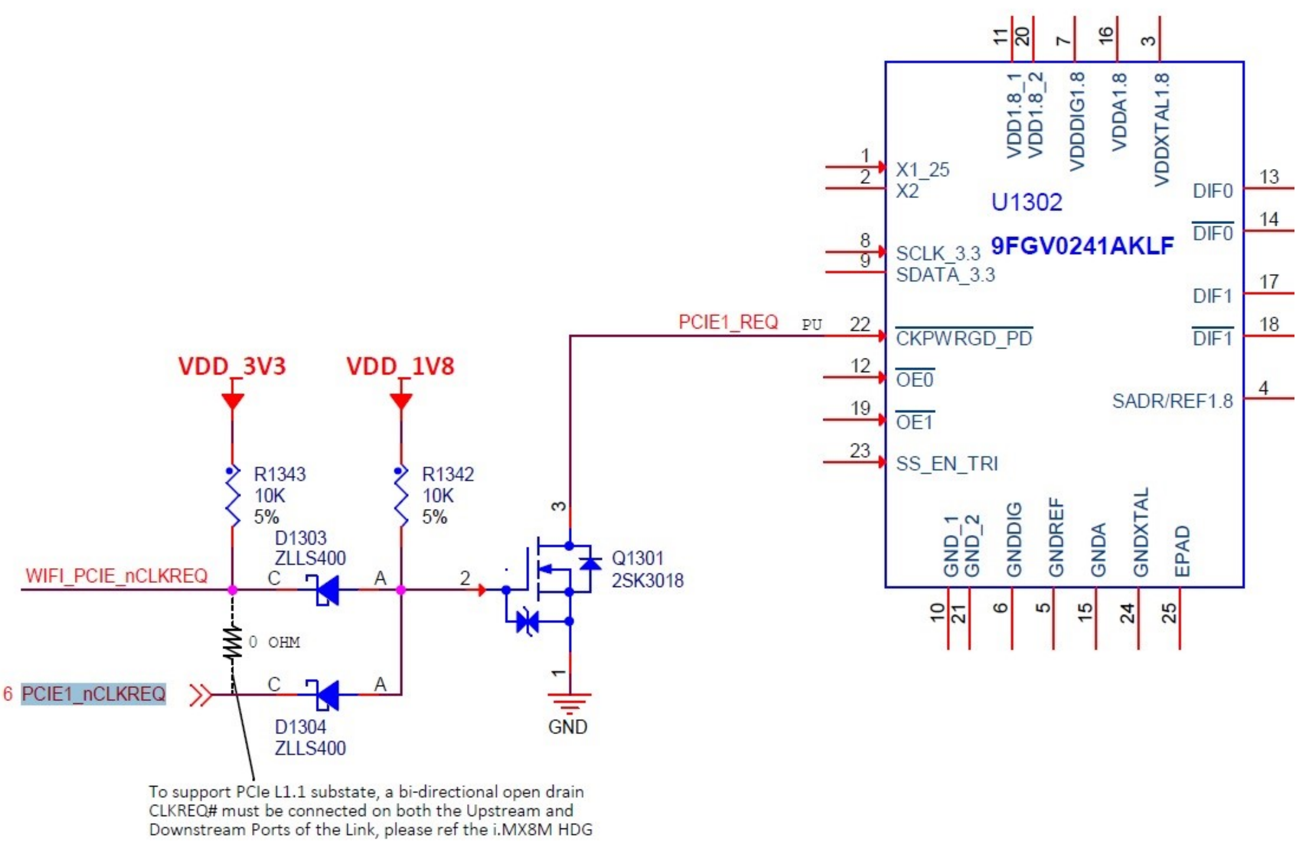

Figure 27. Reference schematic

3.10 Unused input/output terminations

3.10.1 i.MX 8MDQLQ unused input/output guidance

For the i.MX 8MDQLQ, the I/Os and power rails of an unused function can be terminated to reduce overall board power. lists connectivity examples for unused power supply rails and lists connectivity examples for unused signal contacts/interfaces.

Table 30. i.MX 8MDQLQ unused power rail strapping recommendations

Function	Ball name	Recommendation if unused
MIPI-CSI & MIPI-DSI	MIPI_VDDHA, MIPI_VDDA, MIPI_VDD, MIPI_VDDPLL	Tie to the ground
PCIe	PCIE_VPH, PCIE_VPTX, PCIE_VP	Leave unconnected[1]
USB1	USB1_VDD33, USB1_VPH, USB1_VPTX, USB1_VP, USB1_DVDD	Leave unconnected
USB2	USB2_VDD33, USB2_VPH, USB2_VPTX, USB2_VP, USB2_DVDD	Leave unconnected
HDMI	HDMI_AVDDIO, HDMI_AVDDCLK, HDMI_AVDDCORE	Tie to the ground
VPU	VDD_VPU	Leave unconnected
GPU	VDD_GPU	Leave unconnected
Digital I/O supplies	NVCC_NAND, NVCC_SAI1, NVCC_SAI2, NVCC_SAI3, NVCC_SAI5, NVCC_GPIO1, NVCC_I2C, NVCC_UART, NVCC_ECSPI, NVCC_SD1, NVCC_SD2, NVDD_ENET	These digital I/O supplies can be left unconnected when the associated I/O balls are not in use. NOTE: Driving/connecting associated I/O balls is prohibited when the power supply is OFF.

1. These balls supply all the PCIe interfaces (PCIe1, PCIe2) and must be connected/powered if any PCIe port is used.

Table 31. i.MX 8MDQLQ unused signal strapping recommendations

Function	Ball name	Recommendation if unused
MIPI-CSI	MIPI_CSIx_CLK_P/N, MIPI_CSIx_Dx_P/N	Tie to the ground
MIPI-DSI	MIPI_DSI_CLK_P/N, MIPI_DSI_Dx_P/N	Leave unconnected
	MIPI_DSI_REXT	Tie to the ground
PCIe1	PCIE1_TXN_P/N, PCIE1_REF_PAD_CLK_P/N, PCIE1_RESREF	Leave unconnected
PCIe2	PCIE2_TXN_P/N, PCIE2_REF_PAD_CLK_P/N, PCIE2_RESREF	Leave unconnected
USB1	USB1_VBUS, USB1_DN/DP, USB1_ID, USB1_TX_P/N, USB1_RX_P/N, USB1_RESREF	Leave unconnected

Table continues on the next page...

Table 31. i.MX 8MDQLQ unused signal strapping recommendations (continued)

Function	Ball name	Recommendation if unused
USB2	USB2_VBUS, USB2_DN/DP, USB2_ID, USB2_TX_P/N, USB2_RX_P/N, USB2_RESREF	Leave unconnected
HDMI	HDMI_DDC_SCL, HDMI_DDC_SDA, HDMI_HPD, HDMI_CEC, HDMI_REFCLK_P/N, HDMI_TX_P/M_LN_x, HDMI_AUX_P/N	Leave unconnected
	HDMI_REXT	Tie to the ground

Chapter 4
Avoiding board bring-up problems

4.1 Introduction

This chapter introduces how to avoid mistakes when bringing up a board for the first time. The recommendations below consist of basic techniques for detecting board issues and preventing/locating the three issues encountered: power, clocks, and reset.

4.2 Avoiding power pitfalls - Current

Excessive current can damage the board. Use a current-limiting laboratory supply set to the expected main current draw (at most). Monitor the main supply current with an ammeter when powering up the board for the first time. You can use the supply's internal ammeter if there is. By monitoring the main supply current and controlling the current limit, any excessive current can be detected before permanent damage occurs.

Before the board test, you can ohm out the board power rails to the ground to verify that there are no short circuits. Then, you can power on the board and there will not be any damage to the board and/or components.

4.3 Avoiding power pitfall - Voltage

To avoid incorrect voltage rails, create a basic table called a voltage report prior to board bring up/testing. The table helps to validate that all the supplies are reaching the expected levels.

To create a voltage report, list the following:

- Board voltage sources
- Default power-up values for the board voltage sources
- Best location on the board to measure the voltage level of each supply

Determine the best measurement location for each power supply to avoid a large voltage drop (IR drop) on the board. The drop causes inaccurate voltage values. The following guidelines help produce the best voltage measurements:

- Measure closest to the load (in the case of the i.MX 8MDQLQ processor).
- Make two measurements: the first after initial board power-up and the second while running a heavy use-case that stresses the i.MX 8MDQLQ processor.

Ensure that the i.MX 8MDQLQ power supply meets the DC electrical specifications as listed in the chip-specific data sheet. See Table 32 for a sample voltage report table.

NOTE

This report table is for the i.MX 8MDQLQ EVK board. Sample voltage reports for customer PCBs will be different from this, depending on the Processor and Power Management IC (PMIC) used and the assignment of the PMIC power resources.

Table 32. Sample voltage report table

Source	Net name	Expected (V)	Measured (V)	Measure point	Comments
DC jack input	VSYS	12	—	C703.1	Main 12 V supply for board
MP8759	NVCC_SNVS_3V3	3.3	—	U801.3	—

Table continues on the next page...

Table 32. Sample voltage report table (continued)

Source	Net name	Expected (V)	Measured (V)	Measure point	Comments
LDCL015	VDD_SNVS_0V9	0.9	—	U703.5	—
MP2147	VDD_SOC_0V9	0.9	—	SH708	—
MP2147	VDD_ARM_0V9	0.9	—	SH709	—
PF4210_SW1AB	VDD_GPU_0V9	0.9	—	SH701	—
PF4210_SW1C	VDD_VPU_0V9	0.9	—	SH702	—
PF4210_SW3AB	VDD_DRAM_0V9	0.9	—	SH704	—
PF4210_LDO4	VDDA_1V8	1.8	—	C754.1	—
IRLML6401	NVCC_3V3	3.3	—	C915.1	—
PF4210_SW4	NVCC_1V8	1.8	—	SH706	—
PF4210_SW2	NVCC_DRAM_1V1	1.1	—	SH703	—
LDCL015	NVCC_SD2	1.8/3.3	—	U1601.5	Can be either under SW control
PF4210_LDO3	VDD_PHY_1V8	1.8	—	C751.1	—
PF4210_LDO2	VDD_PHY_0V9	0.9	—	C749.1	—
PF4210_LDO5	VDD_PHY_3V3	3.3	—	C757.1	—

4.4 Checking for clock pitfalls

Problems with the external clocks are another board bring-up issue. Ensure that all the clock sources are running as expected.

The `XTALI_25M`/`XTALO_25M`, `XTALI_27M`/`XTALO_27M` and the RTC clocks are the main clock sources for 25 MHz, 27 MHz and 32.768 kHz reference clocks. Although not required, the use of low jitter external oscillators to feed `CLK1_P`/`N` can be an advantage if low jitter or special frequency clock sources are required by modules driven by `CLK1_P`/`N` or `CLK2_P`/`N`. See the CCM chapter in the i.MX 8MDQLQ chip reference manual for details.

When checking crystal frequencies, use an active probe to avoid excessive loading. A passive probe inhibits the 25 MHz and 27 MHz oscillators from starting up. Use the following guidelines:

- RTC clock is running at 32.768 kHz.
- `XTALI_25M`/`XTALO_25M` is running at 25 MHz (used for the PLL reference).
- `XTALI_27M`/`XTALO_27M` is running at 27 MHz (used for the PLL reference).

4.5 Avoiding reset pitfalls

Follow these guidelines to ensure that you are booting correctly.

- During initial power-on while asserting the POR_B reset signal, ensure that 25 MHz and 27 MHz clock is active before releasing `POR_B`.
- Follow the recommended power-up sequence specified in the i.MX 8MDQLQ data sheet.

- Ensure the POR_B signal remains asserted (low) until all voltage rails associated with bootup are ON.

The `SAI_TXD[0:7]`, `SAI_RXD[0:7]`, `BOOT_MODE[0:1]` balls and internal fuses control boot. For a more detailed description about the boot modes, see the **System boot** chapter in the chip reference manual.

4.6 Sample board bring-up checklist

The checklist incorporates the recommendations described in the previous sections. Blank cells should be filled in during the bring-up.

Table 33. Board bring-up checklist

Checklist item	Details	Owner	Findings &Status
Note: The following items must be completed serially.			
1. Perform a visual inspection.	Check major components to make sure nothing has been misplaced or rotated before powering ON.		
2. Verify all i.MX 8MDQLQ voltage rails.	Confirm that the voltages match the data sheet's requirements. Be sure to check voltages as close to the i.MX 8MDQLQ as possible (like on a bypass capacitor). This reveals any IR drops on the board that could cause issues later. Ideally, all the i.MX 8MDQLQ voltage rails should be checked, but see guidance below for important rails to check for the i.MX 8MDQLQ.		
	`VDD_SNVS`, `NVC_SNVS`, `VDD_SOC`, `VDD_ARM`, `VDD_DRAM`, `NVCC_DRAM` are particularly important voltages, and must fall within the parameters provided in the i.MX 8MDQLQ data sheet.		
3. Verify power-up sequence.	Verify that power on reset, `POR_B`, is deserted (high) after all power rails have come up and are stable. See the i.MX 8MDQLQ data sheet for details about power-up sequencing.		
4. Measure/probe input clocks (32.768 kHz, 25 MHz, others).	Without proper clocks, the i.MX 8MDQLQ will not function correctly.		
5. Check JTAG connectivity.	This is one of the most fundamental and basic access points to the i.MX 8MDQLQ to allow the debug and execution of low level code, and probe/access processor memory.		
Note: The following items may be worked on in parallel with other bring-up tasks.			
Access internal RAM	Verify basic operation of the i.MX 8MDQLQ in system. The on-chip internal RAM starts at address 0x0090 0000 and is 128 Kbytes in density. Perform a basic test by performing a write-read-verify operation to the internal RAM. No software initialization is required to access internal RAM.		
Verify CLKO outputs (measure and verify default clock frequencies for desired clock output options) if the	This ensures that the corresponding clock is working and that the PLLs are working. This step requires chip initialization, for example, via the JTAG debugger, to properly set up the		

Table continues on the next page...

Table 33. Board bring-up checklist (continued)

Checklist item	Details	Owner	Findings &Status
board design supports the probing of clock output balls.	IOMUX to output clocks to I/O balls and to set up the clock control module to output the desired clock. See the chip reference manual for more details.		
Measure boot mode frequencies. Set the boot configure switch for each boot mode and measure the following (depending on system availability): • NAND (probe CE to verify boot, measure RE frequency) • SPI-NOR (probe slave select and measure clock frequency) • MMC/SD (measure clock frequency)	This verifies the connectivity of signals between the i.MX 8MDQLQ and boot device and that the boot mode signals are properly set. See the “System Boot” chapter in the chip reference manual for details for boot mode configurations.		
Run basic DDR initialization and test memory	1. Assuming the use of a JTAG debugger, run the DDR initialization and open a debugger memory window pointing to the DDR memory map starting address. 2. Try writing a few words and verify if they can be read correctly. 3. If not, recheck the DDR initialization sequence and whether the DDR has been correctly soldered onto the board. Users should recheck the schematic to ensure that the DDR memory has been connected to the i.MX 8MDQLQ correctly.		

Chapter 5
Using BSDL for board-level test

5.1 BSDL overview

Boundary Scan Description Language (BSDL) is used for board-level test after components have been assembled. The interface for this test uses the JTAG pins. The definition is contained within IEEE Std 1149.1.

5.2 How BSDL functions

A BSDL file defines the internal scan chain, which is the serial linkage of the IO cells, within a particular device. The scan chain looks like a large shift register, which provides a means to read the logic level applied to a pin or a logic state output on that pin. Using JTAG commands, a test tool uses the BSDL file to control the scan chain so that device-board connectivity can be tested.

For example, when using an external ROM test interface, the test tool perform the following operations:

1. Output a specific set of addresses and controls to pins connected to the ROM.
2. Perform a read command and scan out the values of the ROM data pins.
3. Compare the values read with the known golden values.

Based on this procedure, the tool can determine whether the interface between the two parts is connected properly and does not contain shorts or opens.

5.3 Downloading BSDL files

The BSDL file for each i.MX processor is stored on the NXP website upon product release. Contact your local sales office or fields applications engineer to check the availability of information prior to product releases.

5.4 Pin coverage of BSDL

Each pin is defined as a port within the BSDL file. You can open the file with a text editor (such as, Wordpad) to review how each pin functions. The BSDL file defines these functions as below:

```
-- PORT DESCRIPTION TERMS
-- in = input only
-- out = three-state output (0, Z, 1)
-- buffer = two-state output (0, 1)
-- inout = bidirectional
-- linkage = OTHER (vdd, vss, analog)
```

The appearance of linkage in a pin's file implies that the pin cannot be used with boundary scan. They are usually power pins or analog pins that cannot be defined with a digital logic state.

5.5 Boundary scan operation

The boundary scan operation is controlled by:

- `BOOT_MODE0`, `BOOT_MODE1`, and `JTAG_MOD` pins
- On-chip Fuse bits

The **`JTAG_MOD`** pin state decides to select JTAG to the core logic or boundary scan.

- For the definitions of the JTAG interface operations, see the System JTAG Controller (SJC) chapter in the chip reference manual.

- For an explanation of the operation of the e-Fuse bit definitions in Table 34, see **JTAG Security Modes** in the chip reference manual.
- For the fusemap tables, see the **Fusemap** chapter in the chip reference manual.

Table 34. System considerations for BSDL

Pin name	Logic state	Description
JTAG_MOD	1	IEEE 1149.1 JTAG compliant mode
BOOT_MODE[1:0]	[0:0] [0:1] [1:0]	Boot From Fuses Serial Downloader Internal Boot (Development)
POR_B	1	Power On Reset for the device
e-Fuse bits		
JTAG_SMODE[1:0]	[0:0] [0:1]	JTAG enable mode Secure JTAG mode
SJC_DISABLE	0	Secure JTAG Controller is enabled.

NOTE

When use the BSDL file to force i.MX8M enter into boundary scan mode on our MCIMX8M-EVK.

1. COMPLIANCE_PATTERNS of IMX8M: entity is "(BOOT_MODE0, BOOT_MODE1, GPIO1_IO00, GPIO1_IO01, GPIO1_IO02, " &"GPIO1_IO03, TEST_MODE)(0000011)"; BOOT_MODE0, BOOT_MODE1, GPIO1_IO00, GPIO1_IO01 and GPIO1_IO02 should be low, GPIO1_IO03, TEST_MODE should be high.
2. JTAG_nTRST should be 4.7 KΩ pull up to NVCC_JTAG.

5.6 I/O pin power considerations

The boundary scan operation uses each of the available device pins to drive or read values within a given system. Therefore, the power supply pin for each specific module must be powered for the IO buffers to operate. This is straightforward for the digital pins within the system.

NOTE

BSDL was only tested at 1.8 V.

Chapter 6
Revision history

Table 35. Revision history

Revision number	Date	Substantive changes
0	01/2018	Initial release
1	08/2018	1. Updated Table 8, Table 10, and Table 13. 2. Added Figure 26 and Figure 27.
2	06/2019	1. Updated Table 22, Table 23, and Table 27. 2. Updated Table 6 to add information related to the boundary-scan mode. 3. Added Using BSDL for board-level test.
3	11/2020	1. Added checklist of DLL-off mode in Table 3 and Table 4. 2. Added checklist of PMIC and inductor power rating in Table 8.
4	04/2021	1. Added checklist of PCIe clock control and internal regulator in Table 10. 2. Changed the VREF connection recommendation in Table 3.

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Date of release: 04/2021
Document identifier: IMX8MDQLQHDG