National University of Computer and Emerging Sciences, Lahore Campus

Course:	**Digital Logic Design Lab**	**Course Code:**	**EL-227**
Program:	**BS(Computer Science)**	**Semester:**	**Spring 2020**
Duration:	**4 Hours 30 Mins**	**Total Marks:**	**90**
Paper Date:	**21-July-2020**	**Weight**	**50**
Section:	**All Sections**	**Page(s):**	**9**
Exam:	**Final**		

Instruction/Notes:

1. You may solve this on an A4 size paper or assignment sheets or any presentable paper.
2. You may take pictures of the handwritten solution and convert them into a single PDF file. Consider using CamScanner or similar app and transfer the file to your PC via Airdroid app or by uploading it to the Google Drive or USB connection.
3. The images of the solution must be clear, any ambiguous/unclear answer will be considered wrong.
4. You have to submit a single zip file of the solution on the Google Classroom. The zip file must be renamed with your roll number. The format for naming is 19L-XXXX.zip. The zip file will comprise of solution in the form of single PDF and CCT files.
5. If you are facing any problem in uploading your work on Google Classroom then you can submit your work via email to respective lab instructor.
6. Please don't submit BAK file as this is a back-up file for LogicWorks.
7. Multiple submissions of the same solution are unacceptable and you may lose marks for it. So, make sure everything is in order before you submit your file.
8. The final exam is closed book and notes. You are **unallowed** to take help from anyone. Use of any other unfair mean is strictly prohibited. On suspicion, you may be invited for an oral examination.
9. Late submissions are not allowed. So, make sure you have a back-up ready in case of power failure.
10. There is no ambiguity in the exam, so do not waste your valuable time in asking questions.
11. To avoid compatibility issues, download Logicworks from the Google Drive: https://drive.google.com/file/d/1iP9OdTSCfjoKR7olGxepFcRdLvl_aCRh/view?usp=sharing

Question No. 1

Design a "disk spinning" animation circuit for a CD player. The input to the circuit will be a 3-bit binary number A_1, A_2, A_3 provided by 3-bit up counter. The circuit for 3-bit counter has already been provided in CCT file on Google Classroom, so there is no need to design the up counter yourself.

The animation will appear on the top four lights of the LED display of Figure, i.e., on X_1, X_2, X_7, and X_6, going clockwise as shown in Figure 1.

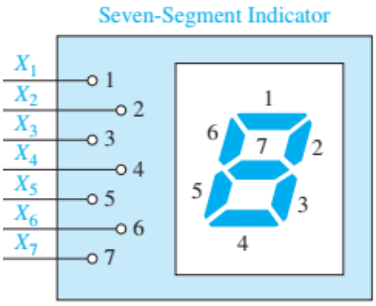

Figure 1 Seven Segment Indicator

The animation should consist of a blank spot on a disk spinning around once, beginning with X_1. Then, the entire disk should blink on and off twice. The pattern is shown in figure 2.

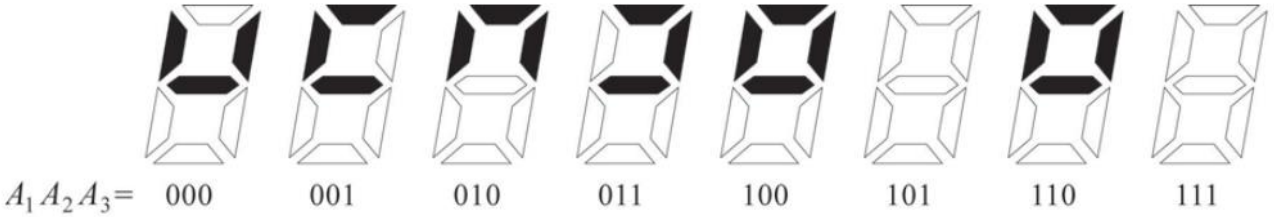

Figure 2 Disk Spinning Pattern

You have to design a circuit that **must** use two 2x1 multiplexers, and two 4x1 multiplexers in the design. You may also use logic gate(s) in the design.

(a) Draw the truth table for the circuit below. The truth table must cover all the possible cases. Stick to the notations use in the question. [8 Marks]

(b) Drive the input equations for the multiplexers. [12 Marks]

(c) Implement the same circuit on LogicWorks. The output of the circuit must be shown through **7-Seg Disp** component in the LogicWorks. There is no restriction on the selection of 2x1 mux and 4x1 mux variants available in the LogicWorks. You have to connect the up-counter circuit already provided to you with your designed circuit. [20 Marks]

Question No. 2

Consider a sequential circuit which have one input I and two outputs Z1 and Z2. All input and outputs are 1-bit binary only. The circuit detects a sequence 100 or 011. There is no possibility that both the sequences i.e. 100 and 011 occurs at the same time.

1. If the sequence 100 occurs then Z1 = 1 and Z2 = 0.
2. If the sequence 011 occurs then Z1 = 0 and Z2 = 1.
3. If neither of the sequence appears then Z1 =0 and Z2 = 0.
4. There is no case where Z1= Z2 =1.

Test Cases:

Case 1:

I	1	0	1	0	1	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Z1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
Z2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Case 2:

I	1	0	1	0	1	1	0	0	0	1	0	1	0	0	1	1	1	1	1	0	0	0	1	0	1	0	1	0	1	1	0	1	0	1	0
Z1	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Z2	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Case 3:

I	0	1	1	0	1	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Z1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Z2	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Case 4:

I	1	0	0	1	0	1	0	1	0	1	0	1	0	0	0	1	0	1	1	0	1	0	1	0	1	0	0	0	0	0	0	0	0	0
Z1	0	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
Z2	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(a) Draw State Diagram for the circuit [10 Marks]

(b) Draw the State Table considering D-Flip Flop(s). The table must include columns for present state(s), input(s), next state(s), and outputs(s). [10 marks]

(c) Drive the input equation(s) of the D-Flip Flop(s) and output equation(s) using K-maps.
[10 marks]

(d) Implement the same circuit on LogicWorks.

i. Use binary switch instead of clock generator for the clock input.
ii. The present state and output of the circuit must be shown through binary probe or LEDs.
iii. Set and Reset switches should be provided or at least reset switch must be available.
iv. All the switches must be located next to each other on the LogicWorks sheet.
v. All outputs shown through binary probe or LEDs must be located next to each other.

You will lose marks, if you don't adhere to the guidelines. [20 Marks]