Final Paper

DLD

Abdul Rehman

CS-D

19L-1135

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Q.1

(a)

4×1 mux =

$I_0 = 1$
$I_1 = \overline{C \oplus D}$
$I_2 = C$
$I_3 = D$

A	B	2×4 Input =
0	0	I_0
0	1	I_1

I in D-latch as control is on "1" value will be updated by at "C" it will remain unchanged.

Let output of 4×1 mux be Y_1
Let output of 2×4 decoder be D_0, D_1, D_2, D_3.

(b)

A	B	C	D	$C \oplus D$	Y_1	Y_1'	D_0	D_1	D_2
0	0	0	0	1	$I_0=1$	0	0	1	0
0	0	0	1	0	$I_0=1$	0	0	1	0
0	0	1	0	0	$I_0=1$	0	0	1	0
0	0	1	1	1	$I_0=1$	0	0	1	0
0	1	0	0	1	$I_1=1$	0	0	1	0

D_3	$D = D_0 + D_1$	Control $= \overline{D_2 \cdot D_3}$	$F(A, B, C, D)$
0	1	1	1
0	1	1	1
0	1	1	1
0	1	1	1
0	1	1	1

D-latch =

C	D	Next State of Q
0	X	No change
1	0	Q = 0, Reset State
1	1	Q = 1, Set State

Q-2

(a)

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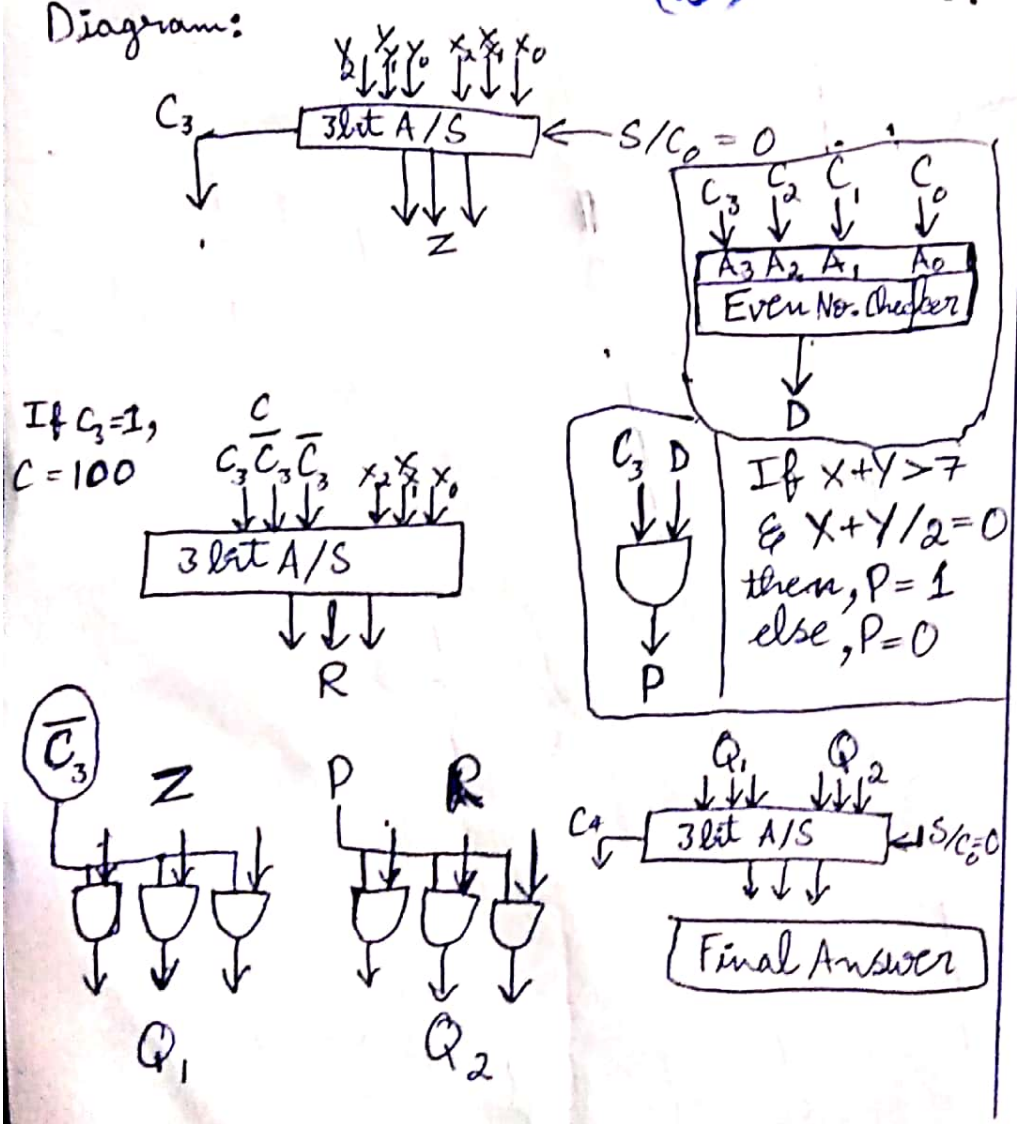
X			Y			X+Y>=7	X+Y<12	X-4	X+Y
X_2	X_1	X_0	Y_2	Y_1	Y_0			R	Z
0	0	0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	0	0	1
0	0	0	0	1	0	0	1	0	1
0	0	0	0	1	1	0	0	0	1
0	0	0	1	0	0	0	1	0	1
0	0	0	1	0	1	0	0	0	1
0	0	0	1	1	0	0	1	0	1
0	0	0	1	1	1	0	0	0	1
0	0	1	0	0	0	0	1	0	1
0	0	1	0	0	1	0	0	0	1
0	0	1	0	1	0	0	1	0	1
0	0	1	0	1	1	0	0	0	1
0	0	1	1	0	0	0	1	0	1
0	0	1	1	0	1	0	0	0	1
0	0	1	1	1	0	0	1	0	1
0	0	1	1	1	1	0	0	0	1
0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	1	0	0	0	1
0	1	0	0	1	0	0	1	0	1
0	1	0	0	1	1	0	0	0	1
0	1	0	1	0	0	0	1	0	1
0	1	0	1	0	1	0	0	0	1
0	1	0	1	1	0	0	1	0	1
0	1	0	1	1	1	0	0	0	1
0	1	1	0	0	0	0	1	0	1
0	1	1	0	0	1	0	0	0	1
0	1	1	0	1	0	0	1	0	1
0	1	1	0	1	1	0	0	0	1
0	1	1	1	0	0	0	1	0	1
0	1	1	1	0	1	0	0	0	1
0	1	1	1	1	0	0	1	0	1
0	1	1	1	1	1	0	0	0	1
1	0	0	0	0	0	0	1	0	1
1	0	0	0	0	1	0	0	0	1
1	0	0	0	1	0	0	1	0	1
1	0	0	0	1	1	0	0	0	1
1	0	0	1	0	0	0	1	0	1
1	0	0	1	0	1	0	0	0	1
1	0	0	1	1	0	0	1	0	1
1	0	0	1	1	1	0	0	0	1
1	0	1	0	0	0	0	1	0	1
1	0	1	0	0	1	0	0	0	1
1	0	1	0	1	0	0	1	0	1
1	0	1	0	1	1	0	0	0	1
1	0	1	1	0	0	0	1	0	1
1	0	1	1	0	1	0	0	0	1
1	0	1	1	1	0	0	1	0	1
1	0	1	1	1	1	0	0	0	1
1	1	0	0	0	0	0	1	0	1
1	1	0	0	0	1	0	0	0	1
1	1	0	0	1	0	0	1	0	1
1	1	0	0	1	1	0	0	0	1
1	1	0	1	0	0	0	1	0	1
1	1	0	1	0	1	0	0	0	1
1	1	0	1	1	0	0	1	0	1
1	1	0	1	1	1	0	0	0	1
1	1	1	0	0	0	0	1	0	1
1	1	1	0	0	1	0	0	0	1
1	1	1	0	1	0	0	1	0	1
1	1	1	0	1	1	0	0	0	1
1	1	1	1	0	0	0	1	0	1
1	1	1	1	0	1	0	0	0	1
1	1	1	1	1	0	0	1	0	1
1	1	1	1	1	1	0	0	0	1

X			Y			X+Y>7	X-4		X+Y
X_2	X_1	X_0	Y_2	Y_1	Y_0			R	Z
0	1	1	0	0	0	0	0	0	1
0	1	1	0	0	1	0	1	0	1
0	1	1	0	1	0	0	0	0	1
0	1	1	0	1	1	0	1	0	1
0	1	1	1	0	0	0	0	0	1
0	1	1	1	0	1	0	1	0	1
0	1	1	1	1	0	1	0	0	1
0	1	1	1	1	1	1	1	0	1
1	0	0	0	0	0	0	0	1	0
1	0	0	0	0	1	0	1	1	0
1	0	0	0	1	0	0	0	1	0
1	0	0	0	1	1	0	1	1	0
1	0	0	1	0	0	0	0	1	0
1	0	0	1	0	1	0	1	1	0
1	0	0	1	1	0	1	0	1	0
1	0	0	1	1	1	1	1	1	0
1	0	1	0	0	0	0	0	1	1
1	0	1	0	0	1	0	1	1	1
1	0	1	0	1	0	0	0	1	1
1	0	1	0	1	1	0	1	1	1
1	0	1	1	0	0	0	0	1	1
1	0	1	1	0	1	0	1	1	1
1	0	1	1	1	0	1	0	1	1
1	0	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	2	0
1	1	0	0	0	1	0	1	2	0
1	1	0	0	1	0	0	0	2	0
1	1	0	0	1	1	0	1	2	0
1	1	0	1	0	0	0	0	2	0
1	1	0	1	0	1	0	1	2	0
1	1	0	1	1	0	1	0	2	0
1	1	0	1	1	1	1	1	2	0
1	1	1	0	0	0	0	0	3	1
1	1	1	0	0	1	0	1	3	1
1	1	1	0	1	0	0	0	3	1
1	1	1	0	1	1	0	1	3	1
1	1	1	1	0	0	0	0	3	1
1	1	1	1	0	1	0	1	3	1
1	1	1	1	1	0	1	0	3	1
1	1	1	1	1	1	1	1	3	1

X			Y			X+Y>7	X+Y/2=0	X-Y (R)	X+Y (Z)
X_2	X_1	X_0	Y_2	Y_1	Y_0			R	Z
1	1	1	0	0	0	0	0	0	1
1	1	1	0	0	1	1	1	1	0
1	1	1	0	1	0	1	0	0	1
1	1	1	0	1	1	1	1	1	0
1	1	1	1	0	0	1	0	0	1
1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	0	1	0	0	1
1	1	1	1	1	1	1	1	1	0

(b)

Diagram:



Rough:

Q-3

(a)

Flour (Kg)		Milk (Ltr)	Sugar (Kg)	Sweet	Sugar Free
F_1	F_0	M	S	SW	SF
0	0	X	X	0	0
0	1	0	X	X	X
0	1	1	0	0	0
0	1	1	1	1	0
1	0	0	X	X	X
1	0	1	0	0	1
1	0	1	1	1	0
1	1	X	X	0	0

(b) For SW, Kmap

F_1F_0 \ MS	$\bar{M}\bar{S}$ 00	$\bar{M}S$ 01	MS 11	$M\bar{S}$ 10
$\bar{F}_1\bar{F}_0$ 00	0 (0)	0 (1)	0 (3)	0 (2)
$\bar{F}_1F_0$ 01	X (4)	X (5)	1 (7)	0 (6)
F_1F_0 11	0 (12)	0 (13)	0 (15)	0 (14)
$F_1\bar{F}_0$ 10	X (8)	X (9)	1 (11)	0 (10)

$$SW = \bar{F}_1F_0S + F_1\bar{F}_0S$$

$$SW = (\bar{F}_1F_0 + F_1\bar{F}_0)S$$

$$SW = (F_1 \oplus F_0)S$$

For SF, Kmap

F_1F_0 \ MS	$\bar{M}\bar{S}$ 00	$\bar{M}S$ 01	MS 11	$M\bar{S}$ 10
$\bar{F}_1\bar{F}_0$ 00	0	0	0	0
$\bar{F}_1F_0$ 01	X	X	0	0
F_1F_0 11	0	0	0	0
$F_1\bar{F}_0$ 10	X	X	0	1

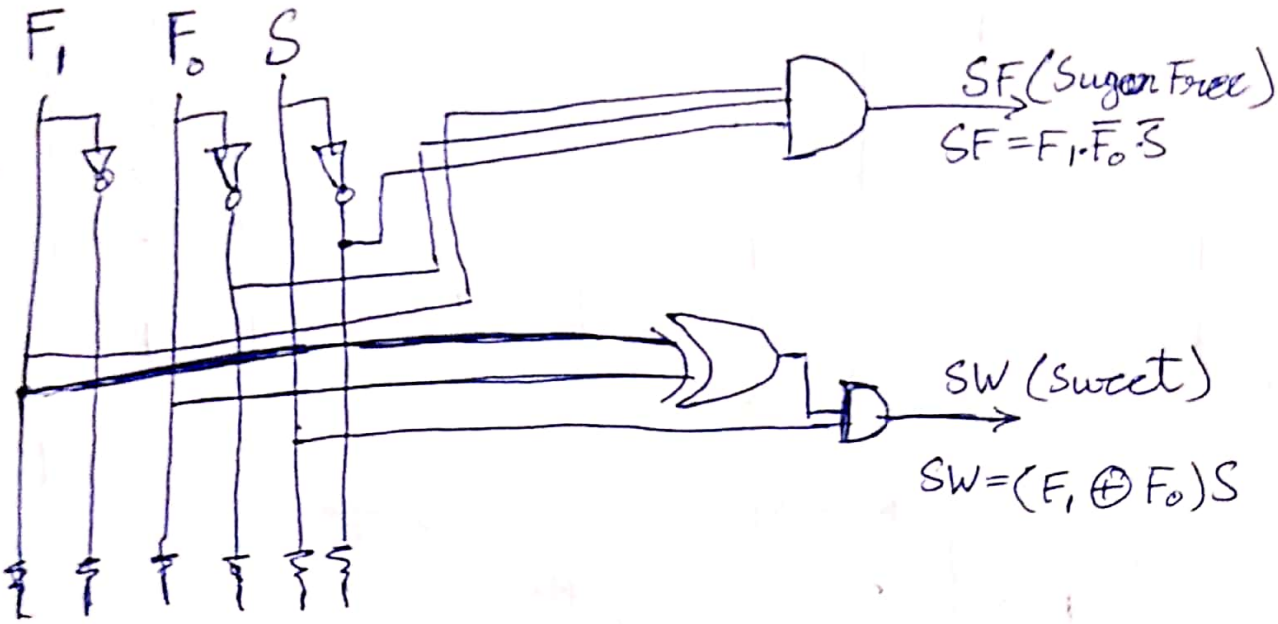
$$SF = F_1\bar{F}_0\bar{S}$$

(C) Circuit Diagram :

$SF = F_1 \bar{F}_0 \bar{S}$

~~$SW = (F_0 \oplus \bar{F}_1$~~

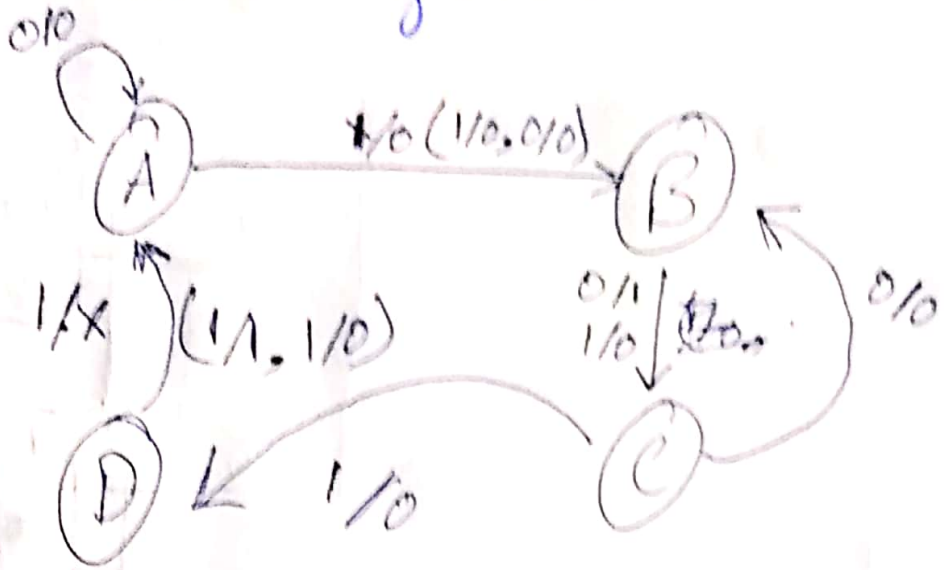
$SW = (F_1 \oplus F_0)S$



(6)

Q-4

(a) State Diagram:



(b)

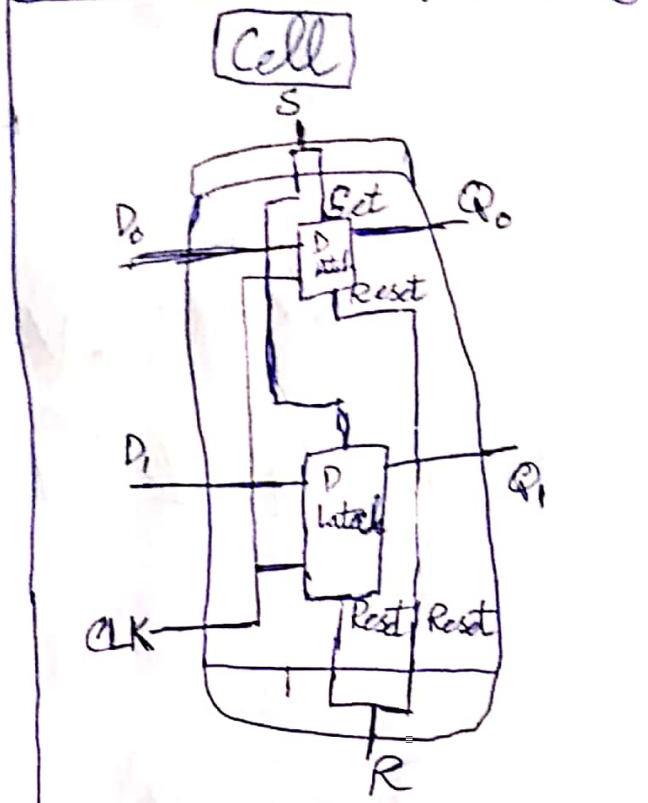
Input

$A_{(x)}$	$B_{(x)}$	$C_{(x)}$	X	$A_{(x+1)}$	$B_{(x+1)}$	$C_{(x+1)}$	Y	Z	W
0	0	0	0	0	0	1	0	0	0
0	0	0	1	0	1	0	0	0	0
0	0	1	0	0	0	0	0	1	1
0	0	1	1	0	1	1	0	0	0
0	1	0	0	0	1	1	0	0	0
0	1	0	1	1	0	0	0	0	0
0	1	1	0	0	1	0	0	0	0
0	1	1	1	1	0	1	0	0	0
1	0	0	0	1	0	1	0	0	0
1	0	0	1	1	1	0	0	0	0
1	0	1	0	1	0	0	0	1	1
1	0	1	1	1	1	1	0	0	0
1	1	0	0	1	1	1	0	0	0
1	1	0	1	0	0	0	0	0	0
1	1	1	0	1	1	0	0	0	0
1	1	1	1	0	0	1	1	0	1

(7)

Q-5

Each Cell of Array

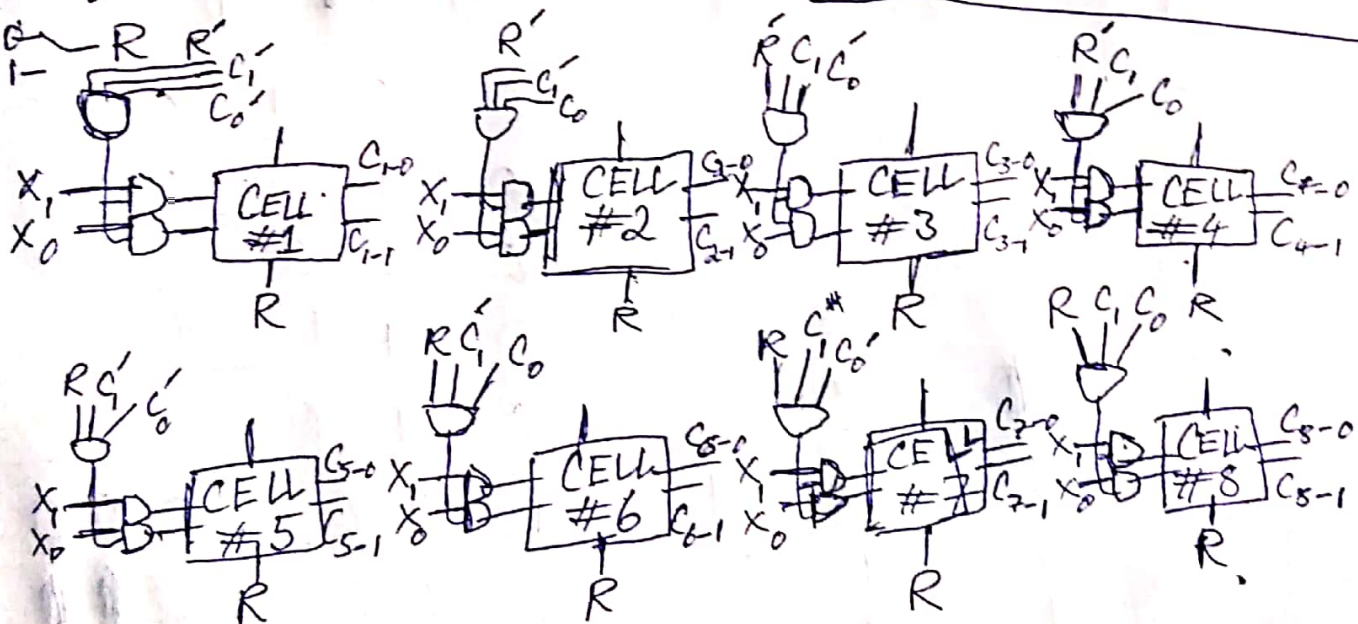


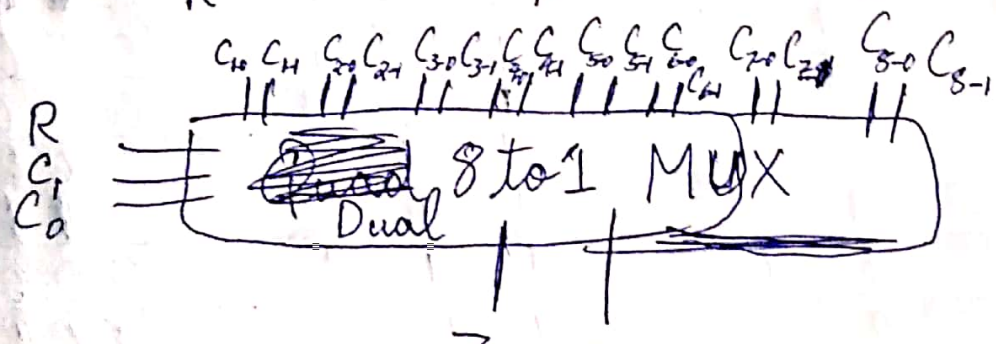
X_1 0 1
X_0 0 1

0 1 R (Reset All)
Reset switch

0 1 C_1
0 C_0
1

R 0 1 R R' C_1' C_0'





Z_0 Z_1