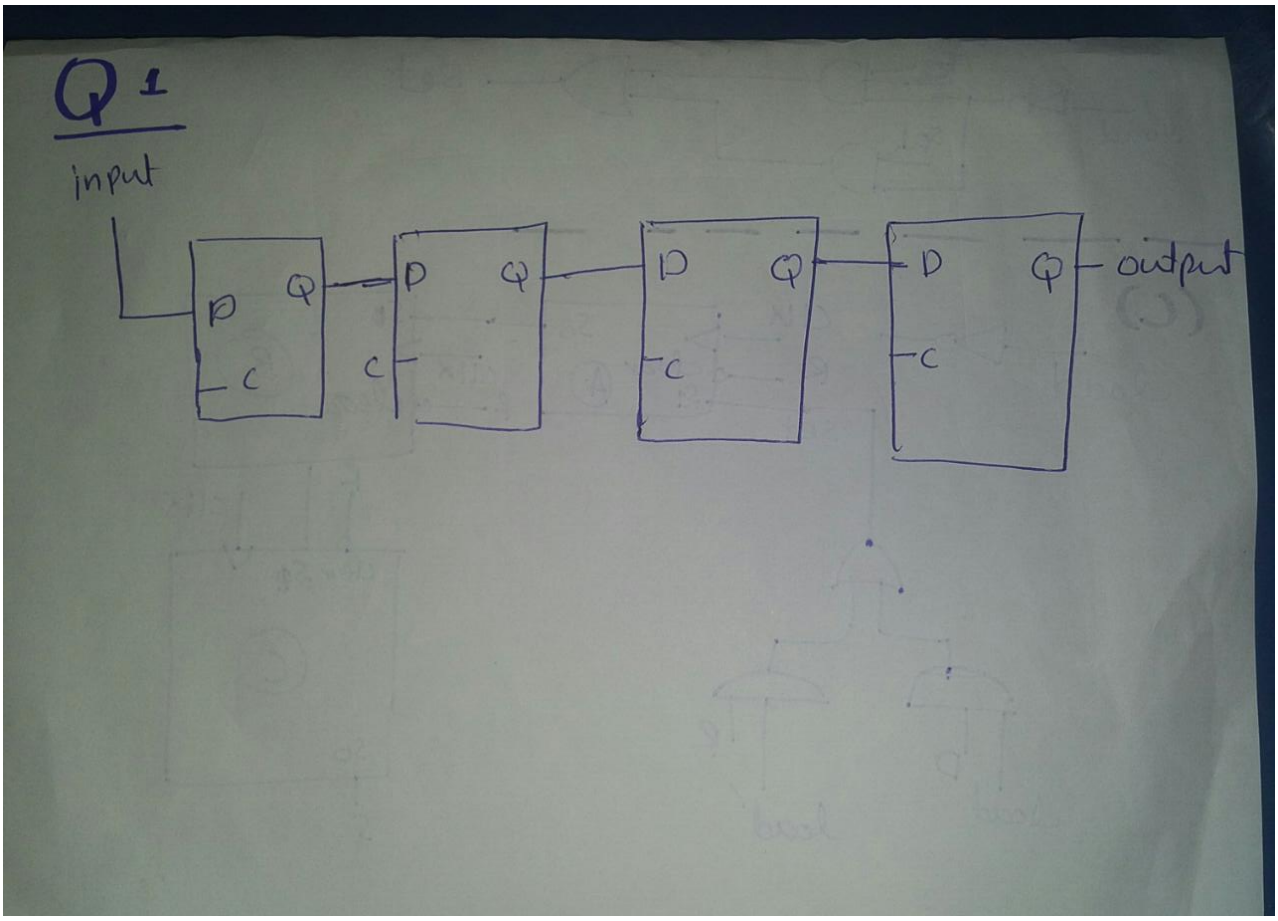
DLD Assignment 6

Roll NO: 19L -1196 2E1

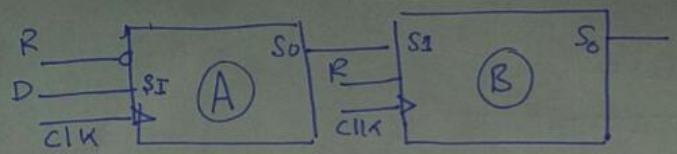
To: Farah Munir

Section: BSCS-19 Batch

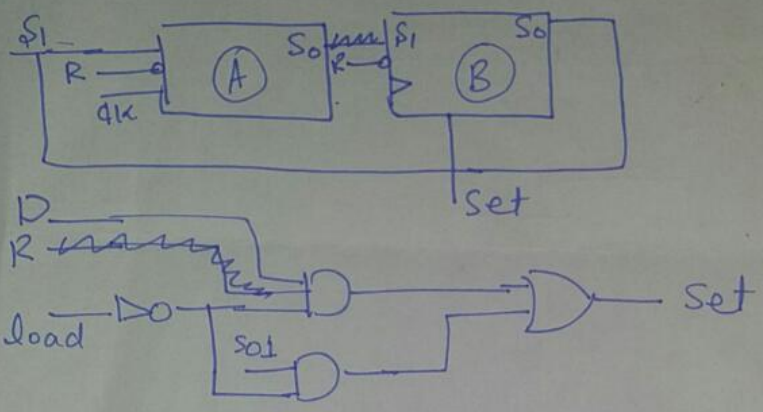


Q2 using 4-Bit SISO Registers

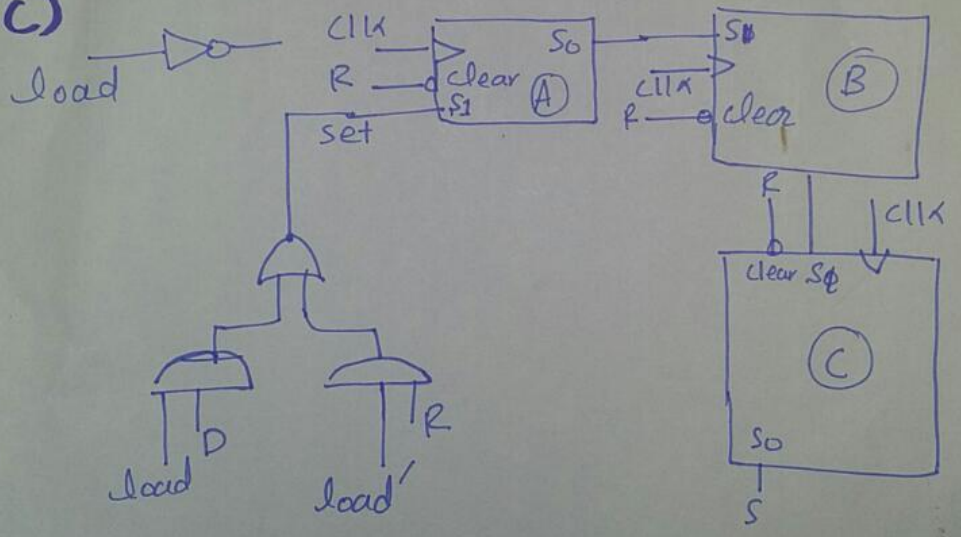
(a) B = A and A = A



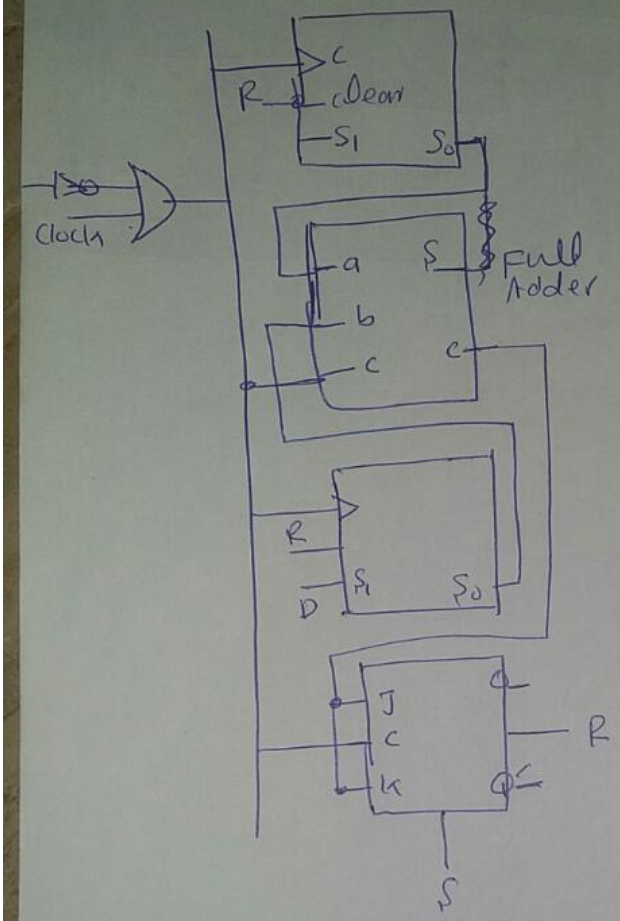
b) B = A and A = B



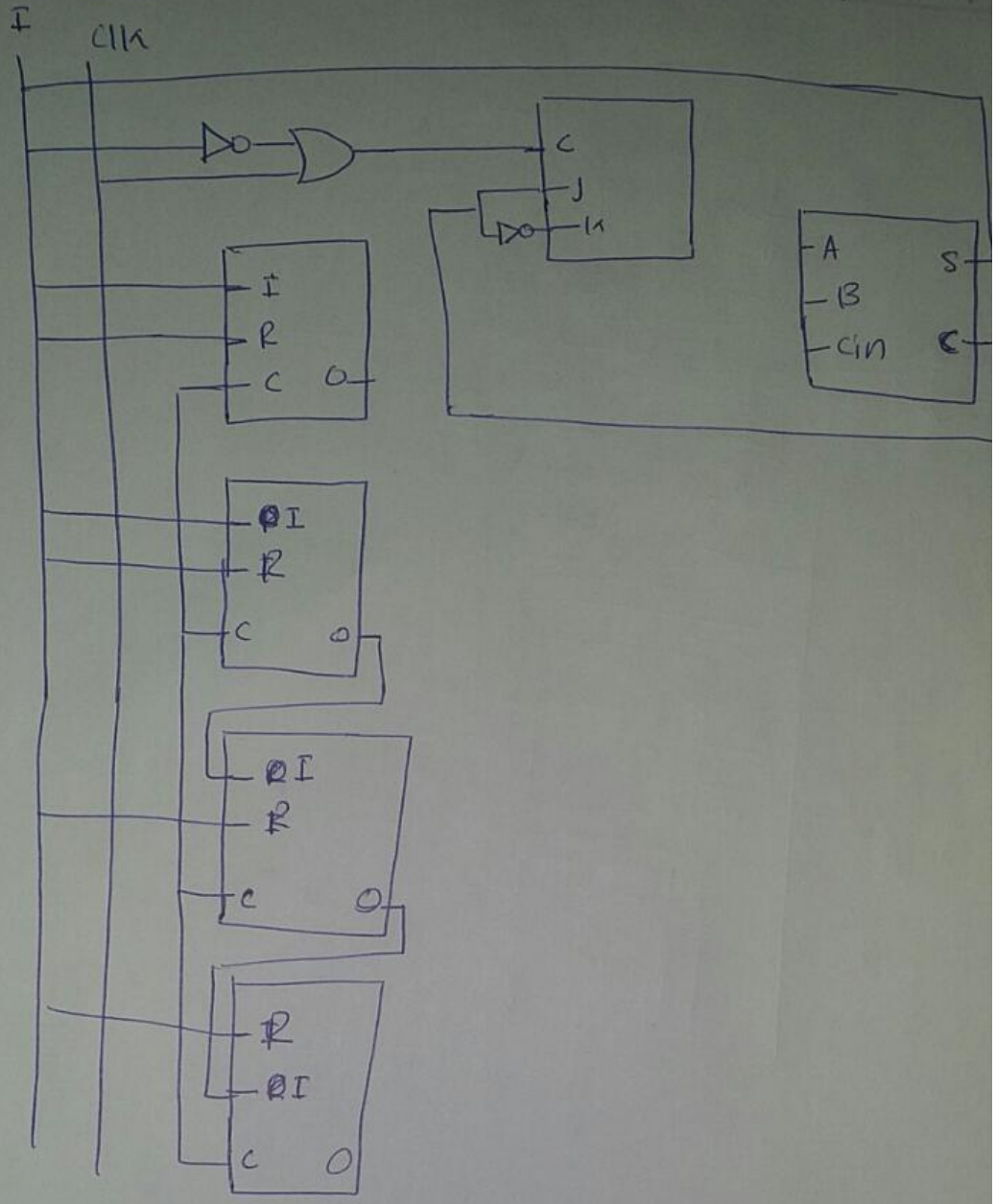
(C)



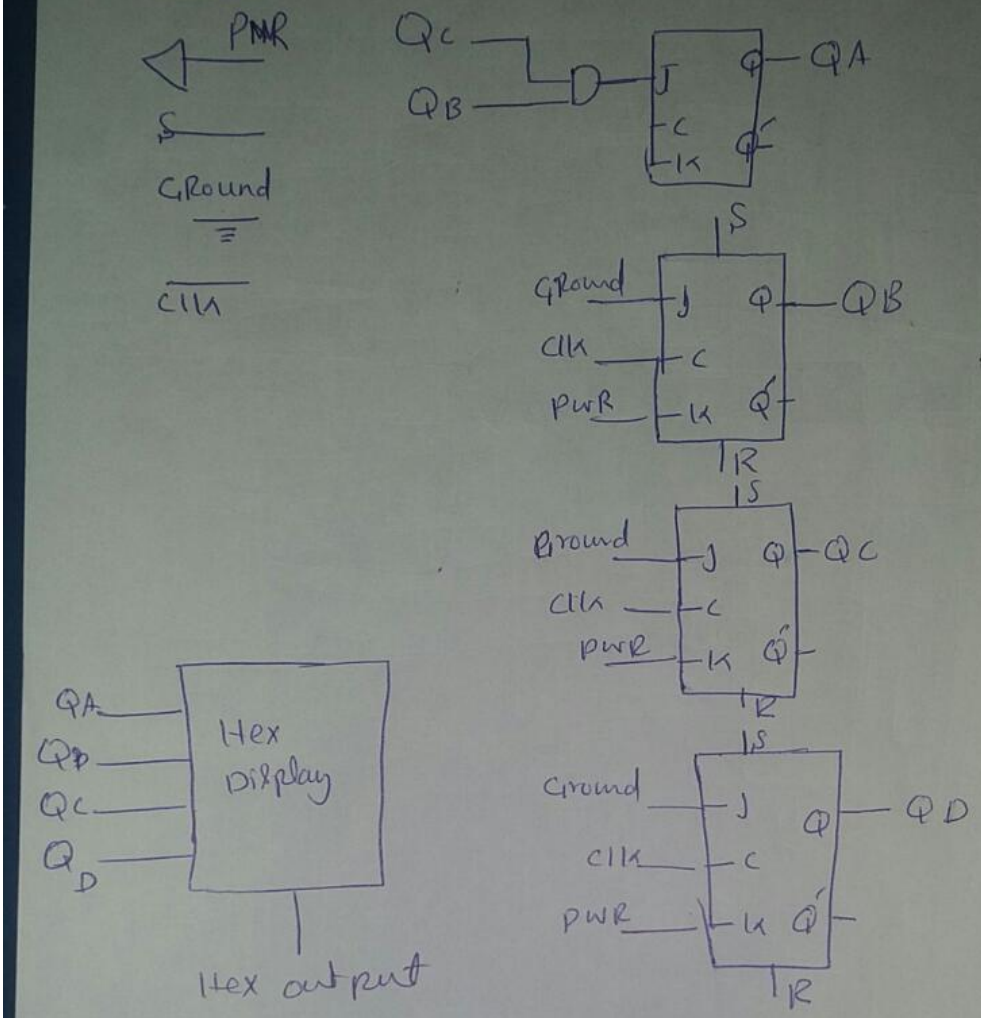
Q 3 4-Bit Serial Adder using JK-flip flop



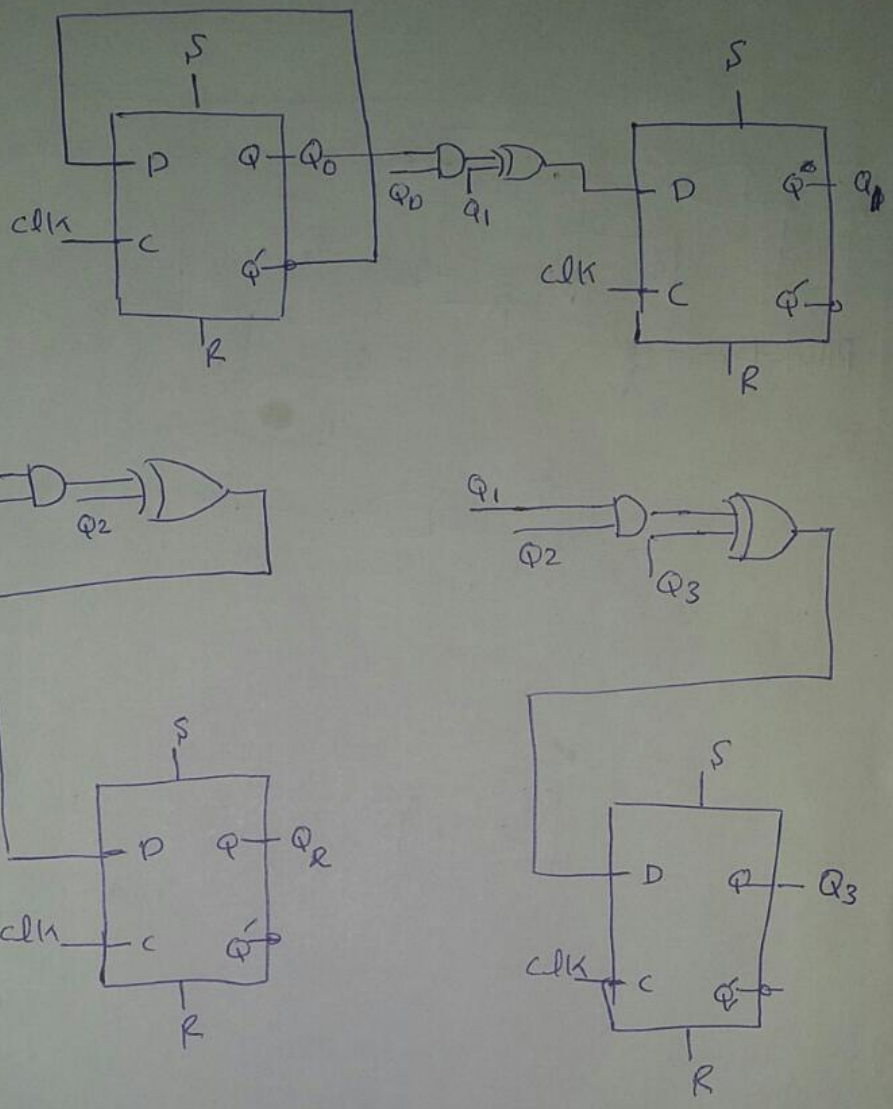
Q 4 Serial addition circuit



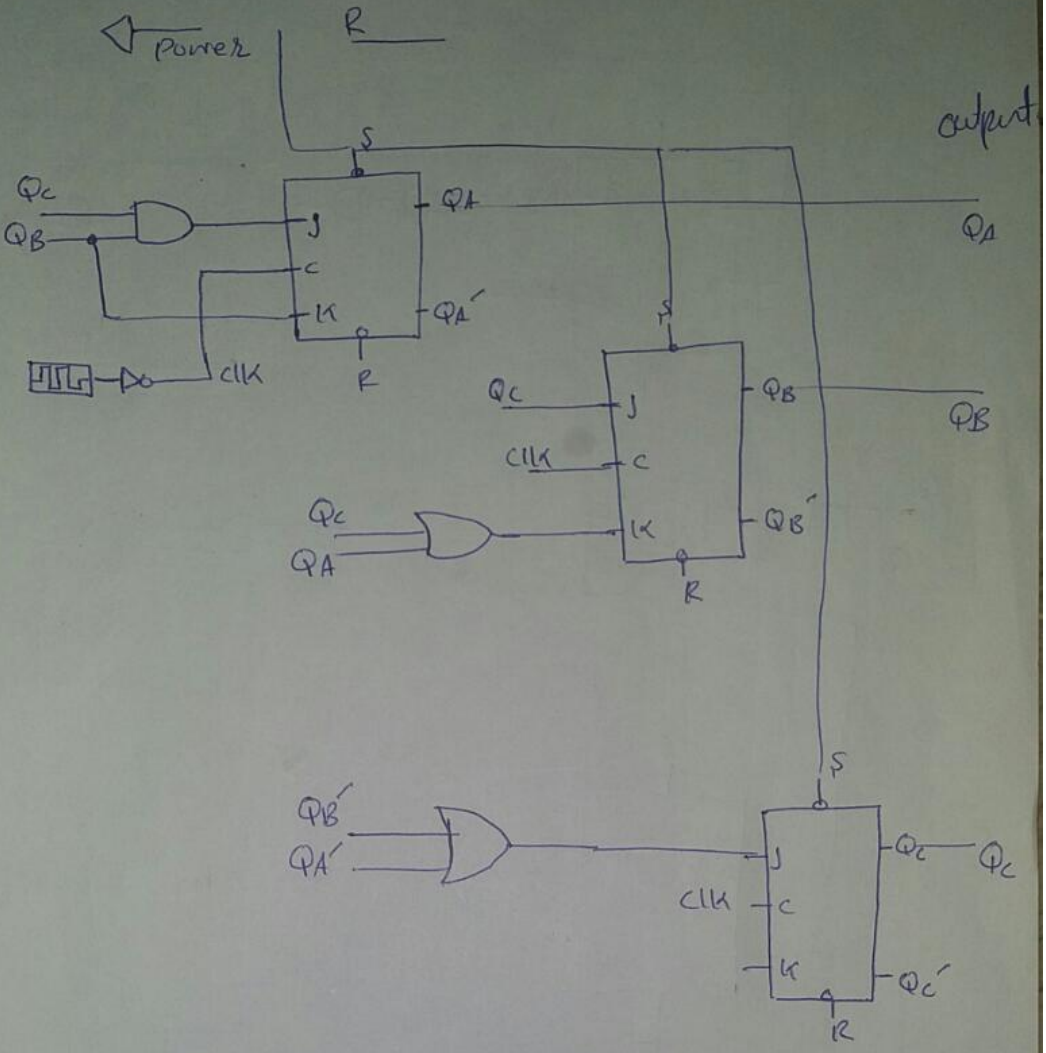
Q5


PWR
S
GRound
CLK
Qc
QB
D
J
C
CLK
Q
Q'
QA
S
GRound
J
C
CLK
PWR
Q
Q'
QB
R
S
GRound
J
C
CLK
PWR
Q
Q'
QC
R
S
Ground
J
C
CLK
PWR
Q
Q'
QD
R
QA
QB
Qc
QD
Hex
Display
Hex output

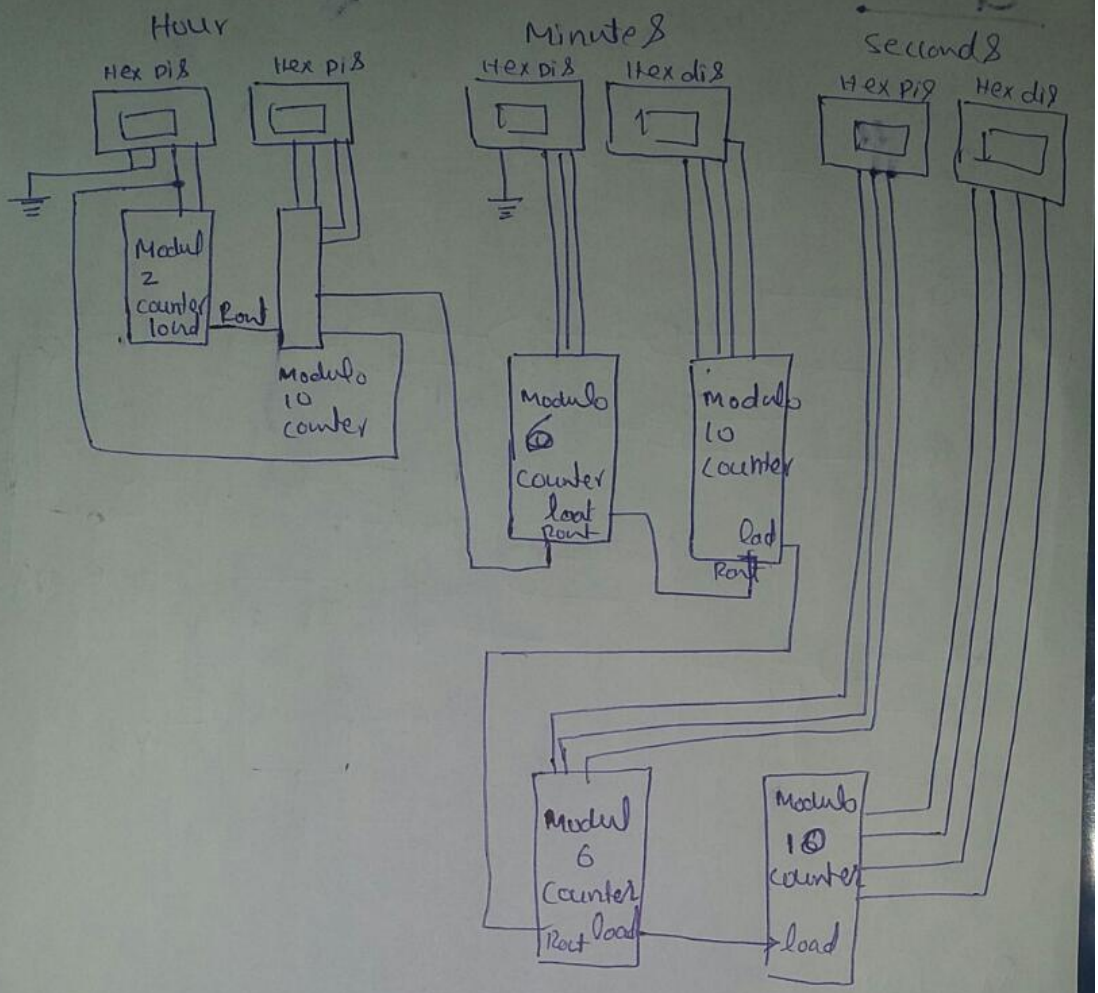
Q6 BCD Synchronous counter



Q7 Modulo 7 Counter

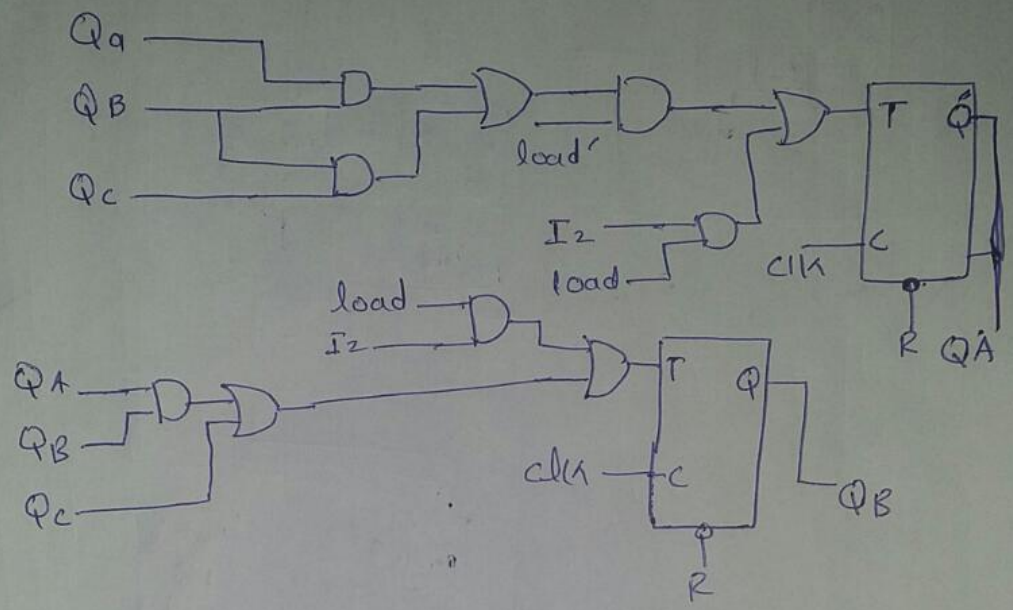


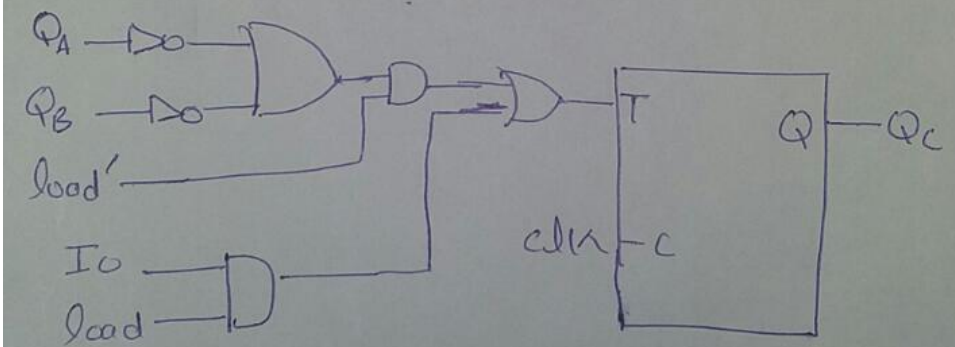
Q8 custom digital watch

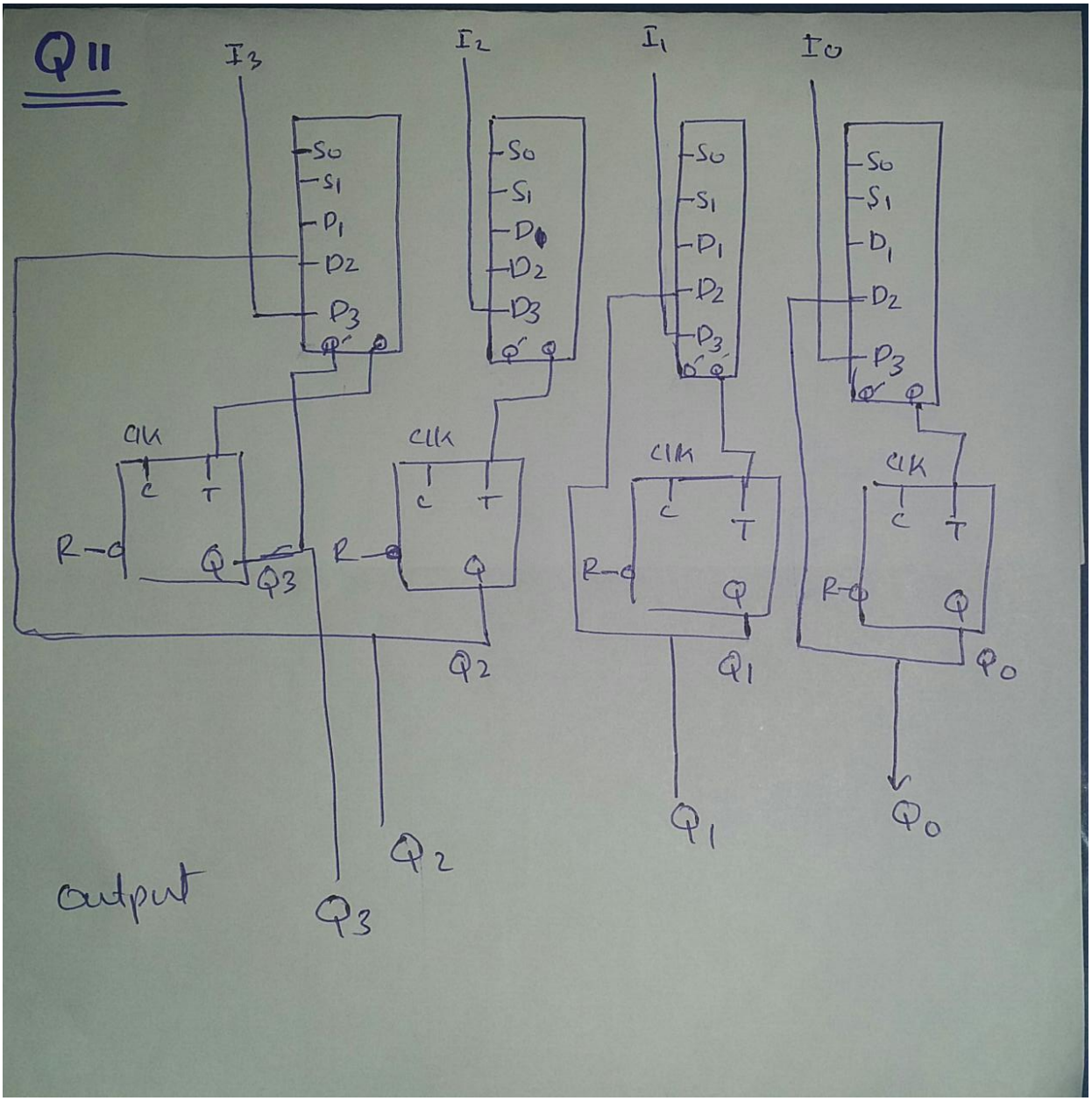


Q 10 Circuit counter with parallel load.

load ——▷○—— load′






Q11
I3
I2
I1
I0
S0
S1
D1
D2
D3
CLK
C
T
R
Q
Q3
Q2
Q1
Q0
output