6 Power control (PWR)

6.1 Introduction

The Power control section (PWR) provides an overview of the supply architecture for the different power domains and of the supply configuration controller.

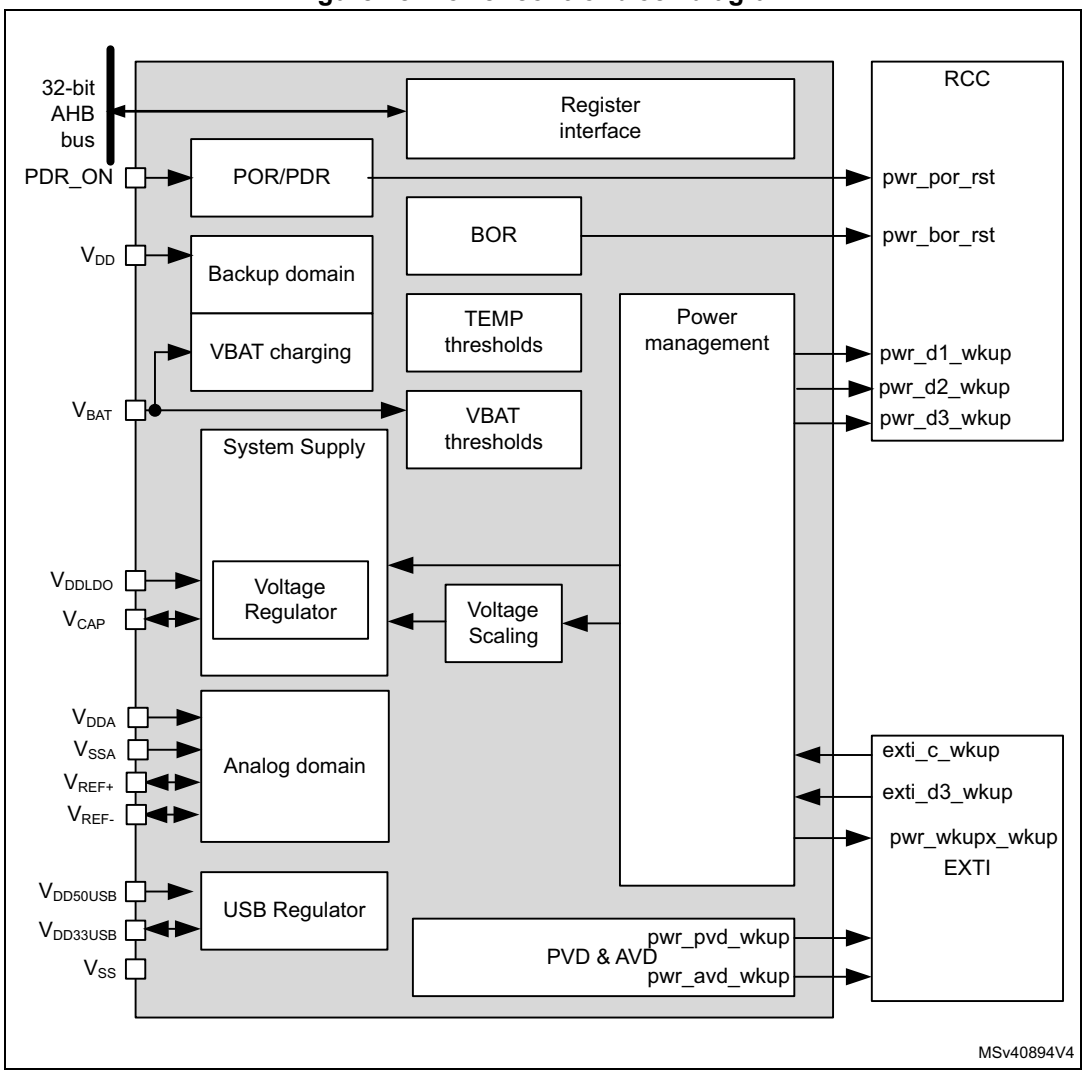
It also describes the features of the power supply supervisors and explains how the V_{CORE} supply domain is configured depending on the operating modes, the selected performance (clock frequency) and the voltage scaling.

6.2 PWR main features

- Power supplies and supply domains
  - Core domains (V_{CORE})
  - V_{DD} domain
  - Backup domain (V_{SW}, V_{BKP})
  - Analog domain (V_{DDA})
- System supply voltage regulation
  - Voltage regulator (LDO)
- Peripheral supply regulation
  - USB regulator
- Power supply supervision
  - POR/PDR monitor
  - BOR monitor
  - PVD monitor
  - AVD monitor
  - V_{BAT} thresholds
  - Temperature thresholds
- Power management
  - V_{BAT} battery charging
  - Operating modes
  - Voltage scaling control
  - Low-power modes

6.3 PWR block diagram

Figure 18. Power control block diagram



6.3.1 PWR pins and internal signals

Table 32 lists the PWR inputs and output signals connected to package pins or balls, while *Table 33* shows the internal PWR signals.

Table 32. PWR input/output signals connected to package pins or balls

Pin name	Signal type	Description
VDD	Supply input	Main I/O and V_{DD} domain supply input
VDDA	Supply input	External analog power supply for analog peripherals
VREF+,VREF-	Supply Input/ Outputs	External reference voltage for ADCs and DAC
VBAT	Supply input	Backup battery supply input
VDDLDO	Supply input	Voltage regulator supply input
VCAP	Supply Input/ Output	Digital core domain supply
VDD50USB	Supply input	USB regulator supply input
VDD33USB	Supply Input/ Output	USB regulator supply output
VSS	Supply input	Main ground
AHB	Digital inputs/ outputs	AHB register interface
PDR_ON	Digital input	Power Down Reset enable

Table 33. PWR internal input/output signals

Signal name	Signal type	Description
pwr_pvd_wkup	Digital output	Programmable voltage detector output
pwr_avd_wkup	Digital output	Analog voltage detector output
pwr_wkupx_wkup	Digital output	CPU wakeup signals (x=1 to 6)

Table 33. PWR internal input/output signals (continued)

Signal name	Signal type	Description
pwr_por_rst	Digital output	Power-on reset
pwr_bor_rst	Digital output	Brownout reset
exti_c_wkup	Digital input	CPU wakeup request
exti_d3_wkup	Digital input	D3 domain wakeup request
pwr_d1_wkup	Digital output	D1 domain bus matrix clock wakeup request
pwr_d2_wkup	Digital output	D2 domain bus matrix clock wakeup request
pwr_d3_wkup	Digital output	D3 domain bus matrix clock wakeup request

6.4 Power supplies

The device requires V_{DD} power supply as well as independent supplies for V_{DDLDO}, V_{DDA}, V_{DDUSB}, and V_{CAP}. It also provides regulated supplies for specific functions (voltage regulator, USB regulator).

- V_{DD} external power supply for I/Os and system analog blocks such as reset, power management and oscillators
- V_{BAT} optional external power supply for backup domain when V_{DD} is not present (V_{BAT} mode)

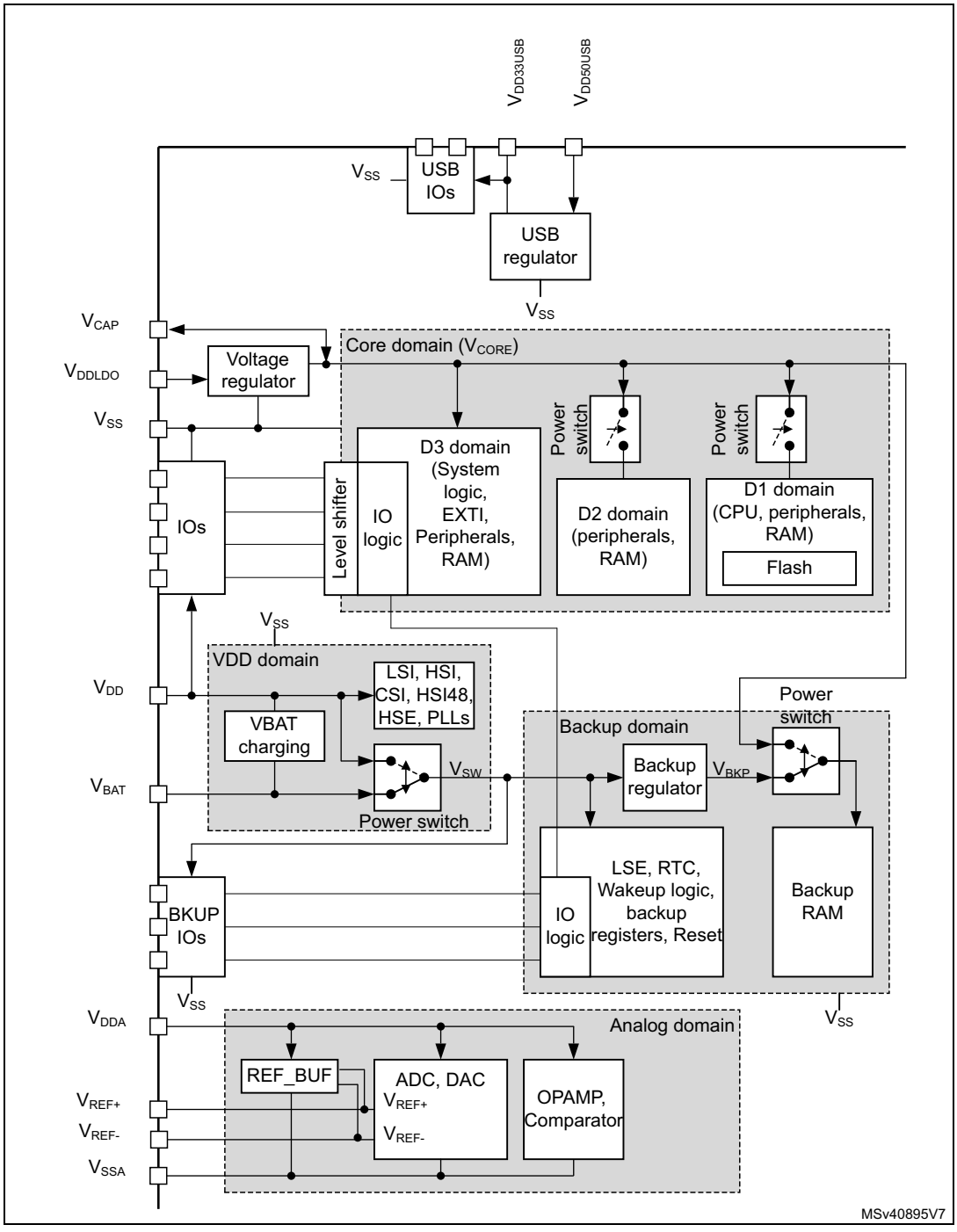
  This power supply shall be connected to V_{DD} when no battery is used.
- V_{DDLDO} external power supply for voltage regulator
- V_{CAP} digital core domain supply

  This power supply is independent from all the other power supplies:
  - When the voltage regulator is enabled, V_{CORE} is delivered by the internal voltage regulator.
  - When the voltage regulator is disabled, V_{CORE} is delivered by an external power supply through V_{CAP} pin.
- V_{DDA} external analog power supply for ADCs, DACs, OPAMPs, comparators and voltage reference buffers

  This power supply is independent from all the other power supplies.
- V_{REF+} external reference voltage for ADC and DAC.
  - When the voltage reference buffer is enabled, V_{REF+} and V_{REF-} are delivered by the internal voltage reference buffer.
  - When the voltage reference buffer is disabled, V_{REF+} is delivered by an independent external reference supply.
- V_{SSA} separate analog and reference voltage ground.
- $V_{DD50USB}$ external power supply for USB regulator.
- $V_{DD33USB}$ USB regulator supply output for USB interface.
  - When the USB regulator is enabled, $V_{DD33USB}$ is delivered by the internal USB regulator.
  - When he USB regulator is disabled, $V_{DD33USB}$ is delivered by an independent external supply input.
- V_{SS} common ground for all supplies and analog regulator.

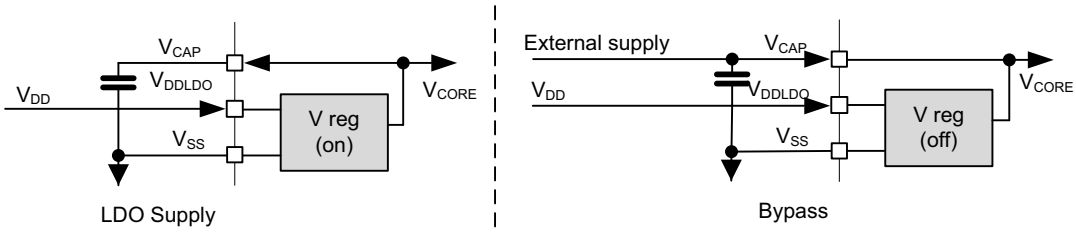
Note: Depending on the operating power supply range, some peripherals might be used with limited features and performance. For more details, refer to section "General operating conditions" of the device datasheets.

Figure 19. Power supply overview



By configuring the voltage regulator the supply configurations shown in *Figure 20* are supported for the V_{CORE} core domain and an external supply.

Figure 20. System supply configurations



The different supply configurations are controlled through the LDOEN and BYPASS bits in *PWR control register 3 (PWR_CR3)* register according to *Table 34*.

Table 34. Supply configuration control

Supply configuration	LDOEN	BYPASS	Description
Default configuration	1	0	– V_{CORE} Power Domains are supplied from the LDO according to VOS.
LDO supply	1	0	– V_{CORE} Power Domains are supplied from the LDO according to VOS. – LDO power mode (Main, LP, Off) will follow system low-power modes.
LDO Bypass	0	1	– V_{CORE} supplied from external source – LDO bypassed, voltage monitoring still active.
Illegal	0	0	– Illegal combination, the default configuration is kept. (write data will be ignored).
	1	1	

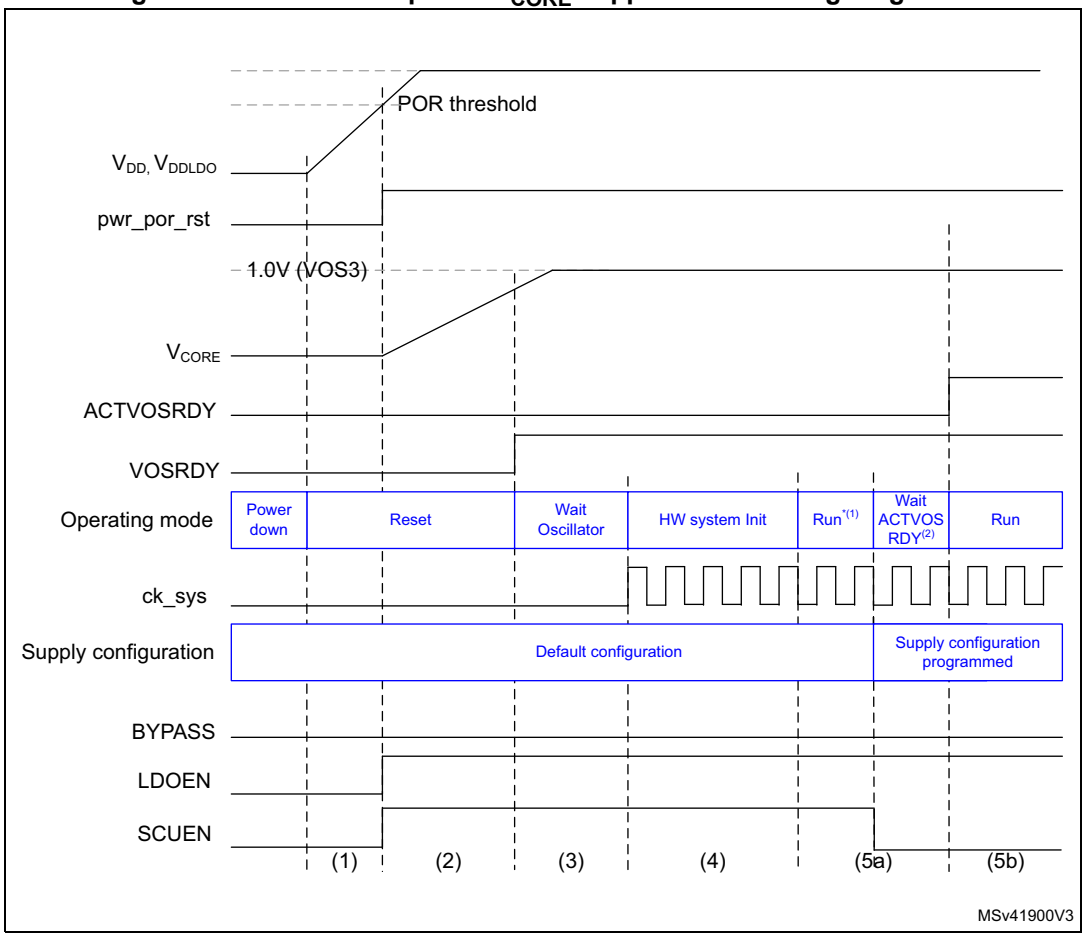
6.4.1 System supply startup

The system startup sequence from power-on in different supply configurations is the following (see *Figure 21* for LDO supply):

1. When the system is powered on, the POR monitors V_{DD} supply. Once V_{DD} is above the POR threshold level, the voltage regulator is enabled in the default supply configuration:
   – The Voltage converter output level is set at 1.0 V in accordance with the VOS3 level configured in *PWR D3 domain control register (PWR_D3CR)*.
2. The system is kept in reset mode as long as V_{CORE} is not correct.
3. Once V_{CORE} is correct, the system is taken out of reset and the HSI oscillator is enabled.
4. Once the oscillator is stable, the system is initialized: Flash memory and option bytes are loaded and the CPU starts in limited run mode (Run*).
5. The software shall then initialize the system including supply configuration programming in *PWR control register 3 (PWR_CR3)*. Once the supply configuration has been configured, the ACTVOSRDY bit in *PWR control status register 1 (PWR_CSR1)* shall be checked to guarantee valid voltage levels:
   a) As long as ACTVOSRDY indicates that voltage levels are invalid, the system is in Run* mode, write accesses to the RAMs are not permitted and VOS shall not be changed.
   b) Once ACTVOSRDY indicates that voltage levels are valid, the system is in normal Run mode, write accesses to RAMs are allowed and VOS can be changed.

The software has to program the supply configuration in *PWR control register 3 (PWR_CR3)*.

Figure 21. Device startup with V_{CORE} supplied from voltage regulator



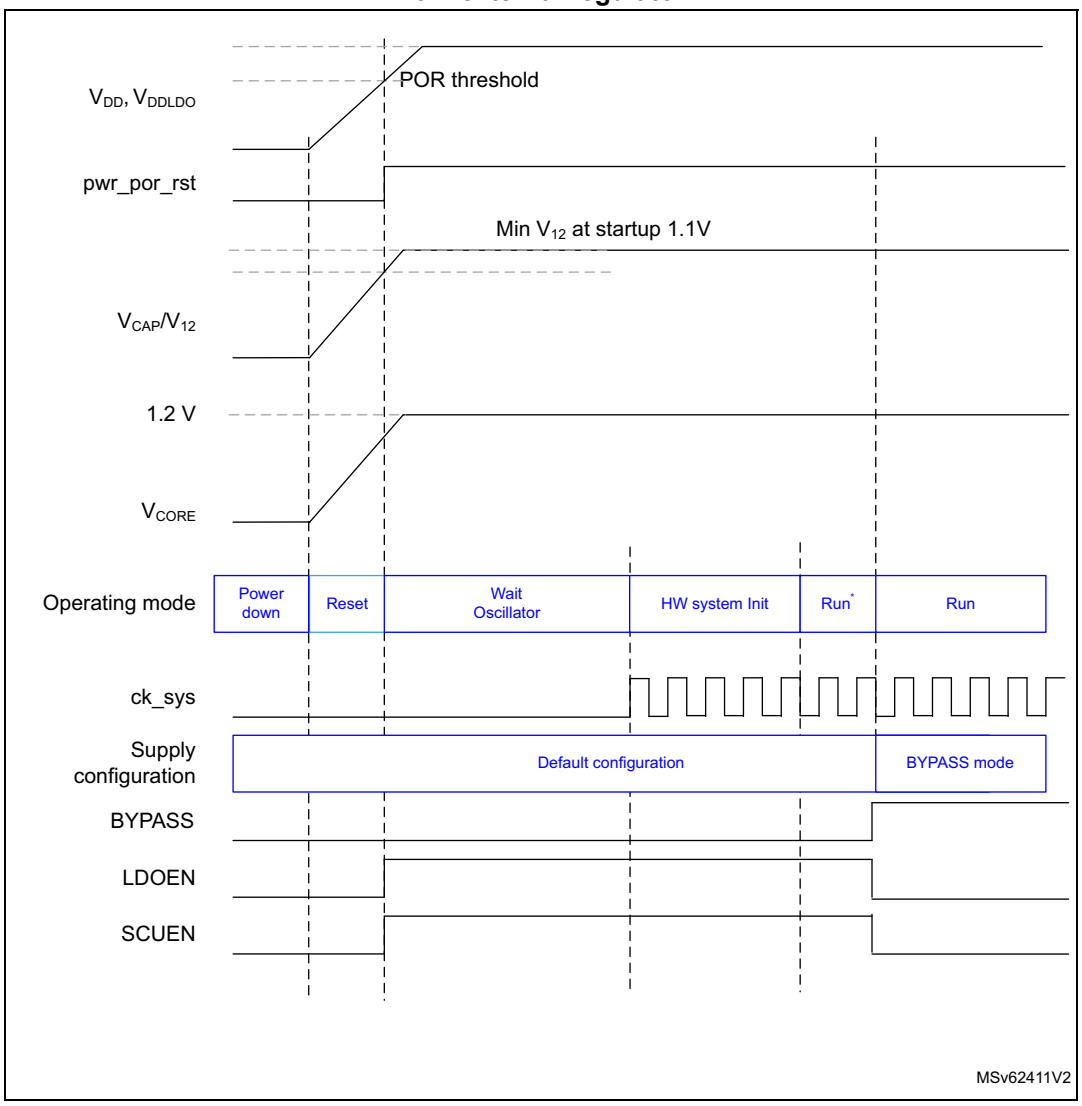
1. In Run* mode, write operations to RAM are not allowed.
2. Write operations to RAM are allowed and VOS can be changed only when ACTVOSRDY is valid.

When exiting from Standby mode, the supply configuration is known by the system since the *PWR control register 3 (PWR_CR3)* register content is retained. However the software shall still wait for the ACTVOSRDY bit to be set in *PWR control status register 1 (PWR_CSR1)* to indicate V_{CORE} voltage levels are valid, before performing write accesses to RAM or changing VOS.

For packages where VDDLDO is internally connected to VDD, when V_{CORE} is supplied in Bypass mode (LDO OFF), the V_{CORE} voltage must first settle at a default level higher than 1.1 V. Due to the LDO default state after power-up (enabled by default), the external V_{CORE} voltage must remain higher than 1.1 V until the LDO is disabled by software.

When the LDO is disabled, the external V_{CORE} voltage can be adjusted according to the user application needs (refer to section *General operating conditions* of the datasheet for details on V_{CORE} level versus the maximum operating frequency).

Figure 22. Device startup with V_{CORE} supplied in Bypass mode from external regulator



Note: Before accessing the RAM, it is strongly recommended to switch to the correct VOS setting depending on the external voltage level as soon as possible.

6.4.2 Core domain

The V_{CORE} core domain supply can be provided by the voltage regulator or by an external supply (V_{CAP}). V_{CORE} supplies all the digital circuitries except for the backup domain and the Standby circuitry. The V_{CORE} domain is split into 3 sections:

- D1 domain containing the CPU (Cortex®-M7), Flash memory and peripherals.
- D2 domain containing peripherals.
- D3 domain containing the system control, I/O logic and low-power peripherals.

When a system reset occurs, the voltage regulator is enabled and supplies V_{CORE}. This allows the system to start up in any supply configurations (see *Figure 20*).

After a system reset, the software shall configure the used supply configuration in *PWR control register 3 (PWR_CR3)* register before changing VOS in *PWR D3 domain control register (PWR_D3CR)* or the RCC ck_sys frequency. The different system supply configurations are controlled as shown in *Table 34*.

Voltage regulator

The embedded voltage regulator (LDO) requires external capacitors to be connected to V_{CAP} pins.

The voltage regulator provides three different operating modes: Main (MR), Low-power (LP) or Off. These modes will be used depending on the system operating modes (Run, Stop and Standby).

- Run mode

  The LDO regulator is in Main mode and provides full power to the V_{CORE} domain (core, memories and digital peripherals). The regulator output voltage can be scaled by software to different voltage levels (VOS0[a], VOS1, VOS2, and VOS3) that are configured through VOS bits in *PWR D3 domain control register (PWR_D3CR)*. The VOS voltage scaling allows optimizing the power consumption when the system is clocked below the maximum frequency. By default VOS3 is selected after system reset. VOS can be changed on-the-fly to adapt to the required system performance.

- Stop mode

  The voltage regulator supplies the V_{CORE} domain to retain the content of registers and internal memories.

  The regulator can be kept in Main mode to allow fast exit from Stop mode, or can be set in LP mode to obtain a lower V_{CORE} supply level and extend the exit-from-Stop latency. The regulator mode is selected through the SVOS and LPDS bits in *PWR control register 1 (PWR_CR1)*. Main mode and LP mode are allowed if SVOS3 voltage scaling is selected, while only LP mode is possible for SVOS4 and SVOS5 scaling. Due to a lower voltage level for SVOS4 and SVOS5 scaling, the Stop mode consumption can be further reduced.

- Standby mode

  The voltage regulator is OFF and the V_{CORE} domains are powered down. The content of the registers and memories is lost except for the Standby circuitry and the backup domain.

Note: For more details, refer to the voltage regulator section in the datasheets.

6.4.3 PWR external supply

When V_{CORE} is supplied from an external source, different operating modes can be used depending on the system operating modes (Run, Stop or Standby):

- In Run mode

  The external source supplies full power to the V_{CORE} domain (core, memories and digital peripherals). The external source output voltage is scalable through different voltage levels (VOS0, VOS1, VOS2 and VOS3). The externally applied voltage level shall be reflected in the VOS bits of PWR_D3CR register. The RAMs shall only be

a. VOS0 corresponds to V_{CORE} boost allowing to reach the system maximum frequency (refer to *Section : VOS0 activation/deactivation sequence*)

accessed for write operations when the external applied voltage level matches VOS settings.

- In Stop mode

  The external source supplies V_{CORE} domain to retain the content of registers and internal memories. The regulator can select a lower V_{CORE} supply level to reduce the consumption in Stop mode.

- In Standby mode

  The external source shall be switched OFF and the V_{CORE} domains powered down. The content of registers and memories is lost except for the Standby circuitry and the backup domain. The external source shall be switched ON when exiting Standby mode.

6.4.4 Backup domain

To retain the content of the backup domain (RTC, backup registers and backup RAM) when V_{DD} is turned off, V_{BAT} pin can be connected to an optional standby voltage which is supplied from a battery or from an another source.

The switching to V_{BAT} is controlled by the power-down reset embedded in the Reset block that monitors the V_{DD} supply.

Warning: **During $t_{RSTTEMPO}$ (temporization at V_{DD} startup) or after a PDR is detected, the power switch between V_{BAT} and V_{DD} remains connected to V_{BAT}.**
During the a startup phase, if V_{DD} is established in less than $t_{RSTTEMPO}$ (see the datasheet for the value of $t_{RSTTEMPO}$) and $V_{DD} > V_{BAT} + 0.6$ V, a current may be injected into V_{BAT} through an internal diode connected between V_{DD} and the power switch (V_{BAT}).
If the power supply/battery connected to the V_{BAT} pin cannot support this current injection, it is strongly recommended to connect an external low-drop diode between this power supply and the V_{BAT} pin.

When the V_{DD} supply is present, the backup domain is supplied from V_{DD}. This allows saving V_{BAT} power supply battery life time.

If no external battery is used in the application, it is recommended to connect V_{BAT} externally to V_{DD} through a 100 nF external ceramic capacitor.

When the V_{DD} supply is present and higher than the PDR threshold, the backup domain is supplied by V_{DD} and the following functions are available:

- PC14 and PC15 can be used either as GPIO or as LSE pins.
- PC13 can be used either as GPIO or as RTC_AF1 or RTC_TAMP1 pin assuming they have been configured by the RTC.
- PI8/RTC_TAMP2 and PC1/RTC_TAMP3 when they are configured by the RTC as tamper pins.

Note: Since the switch only sinks a limited amount of current, the use of PC13 to PC15 and PI8 GPIOs is restricted: only one I/O can be used as an output at a time, at a speed limited to 2 MHz with a maximum load of 30 pF. These I/Os must not be used as current sources (e.g. to drive an LED).

In V_{BAT} mode, when the V_{DD} supply is absent and a supply is present on V_{BAT}, the backup domain is supplied by V_{BAT} and the following functions are available:

- PC14 and PC15 can be used as LSE pins only.
- PC13 can be used as RTC_AF1 or RTC_TAMP1 pin assuming they have been configured by the RTC.
- PI8/RTC_TAMP2 and PC1/RTC_TAMP3 when they are configured by the RTC as tamper pins.

Accessing the backup domain

After reset, the backup domain (RTC registers and RTC backup registers) is protected against possible unwanted write accesses. To enable access to the backup domain, set the DBP bit in the *PWR control register 1 (PWR_CR1)*.

For more detail on RTC and backup RAM access, refer to *Section 8: Reset and Clock Control (RCC)*.

Backup RAM

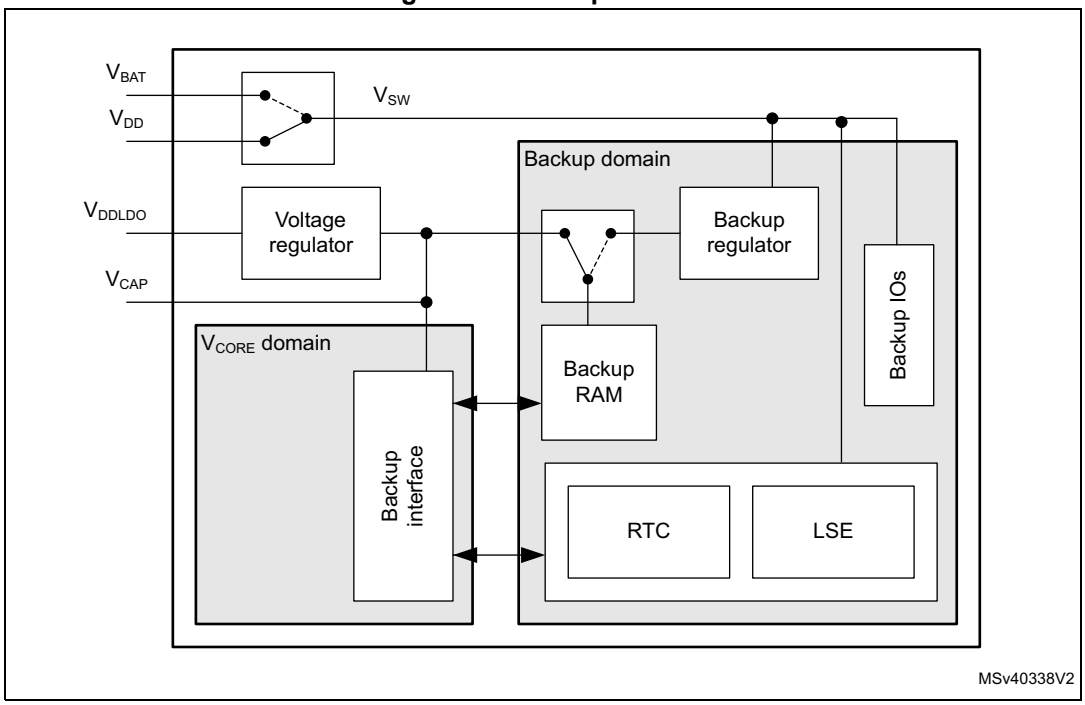
The backup domain includes 4 Kbytes of backup RAM accessible in 32-bit, 16-bit or 8-bit data mode. The backup RAM is supplied from the Backup regulator in the backup domain. When the Backup regulator is enabled through BREN bit in *PWR control register 2 (PWR_CR2)*, the backup RAM content is retained even in Standby and/or V_{BAT} mode (it can be considered as an internal EEPROM if V_{BAT} is always present.)

The Backup regulator can be ON or OFF depending whether the application needs the backup RAM function in Standby or V_{BAT} modes.

The backup RAM is not mass erased by an tamper event, instead it is read protected to prevent confidential data, such as cryptographic private key, from being accessed. To re-gain access to the backup RAM after a tamper event, the memory area needs to be first erased. The backup RAM can be erased:

- through the Flash interface when a protection level change from level 1 to level 0 is requested (refer to the description of Read protection (RDP) in the Flash programming manual).
- After a tamper event, by performing a dummy write with zero as data to the backup RAM.

Figure 23. Backup domain



6.4.5 V_{BAT} battery charging

When V_{DD} is present, the external battery connected to V_{BAT} can be charged through an internal resistance.

V_{BAT} charging can be performed either through a 5 kΩ resistor or through a 1.5 kΩ resistor, depending on the VBRS bit value in *PWR control register 3 (PWR_CR3)*.

The battery charging is enabled by setting the VBE bit in *PWR control register 3 (PWR_CR3)*. It is automatically disabled in V_{BAT} mode.

6.4.6 Analog supply

Separate V_{DDA} analog supply

The analog supply domain is powered by dedicated V_{DDA} and V_{SSA} pads that allow the supply to be filtered and shielded from noise on the PCB, thus improving ADC and DAC conversion accuracy:

- The analog supply voltage input is available on a separate V_{DDA} pin.
- An isolated supply ground connection is provided on V_{SSA} pin.

Analog reference voltage V_{REF+}/V_{REF-}

To achieve better accuracy low-voltage signals, the ADC and DAC also have a separate reference voltage, available on V_{REF+} pin. The user can connect a separate external reference voltage on V_{REF+}.

The V_{REF+} controls the highest voltage, represented by the full scale value, the lower voltage reference (V_{REF-}) being connected to V_{SSA}.

When enabled by ENVR bit in the VREFBUF control and status register (see *Section 27: Voltage reference buffer (VREFBUF)*), V_{REF+} is provided from the internal voltage reference buffer. The internal voltage reference buffer can also deliver a reference voltage to external components through V_{REF+}/V_{REF-} pins.

When the internal voltage reference buffer is disabled by ENVR, V_{REF+} s delivered by an independent external reference supply voltage.

6.4.7 USB regulator

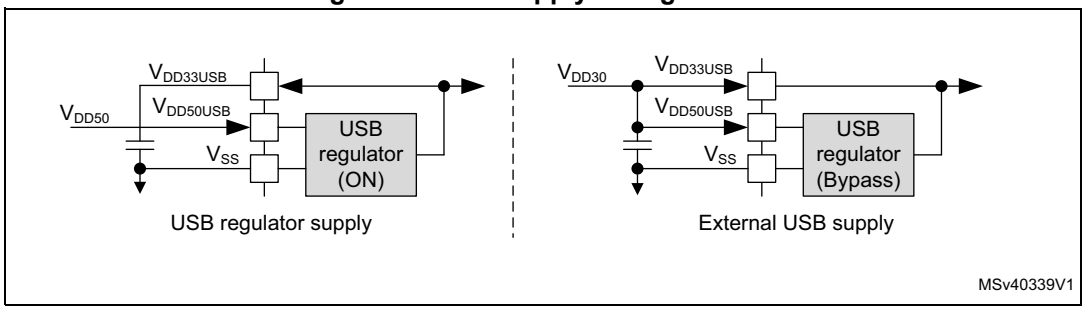
The USB transceivers are supplied from a dedicated $V_{DD33USB}$ supply that can be provided either by the integrated USB regulator, or by an external USB supply.

When enabled by USBREGEN bit in *PWR control register 3 (PWR_CR3)*, the $V_{DD33USB}$ is provided from the USB regulator. Before using $V_{DD33USB}$, check that it is available by monitoring USB33RDY bit in *PWR control register 3 (PWR_CR3)*. The $V_{DD33USB}$ supply level detector shall be enabled through USB33DEN bit in PWR_CR3 register.

When the USB regulator is disabled through USBREGEN bit, $V_{DD33USB}$ can be provided from an external supply. In this case $V_{DD33USB}$ and $V_{DD50USB}$ shall be connected together. The $V_{DD33USB}$ supply level detector must be enabled through USB33DEN bit in PWR_CR3 register before using the USB transceivers.

For more information on the USB regulator (see *Section 57: **USB on-the-go high-speed (OTG_HS)***).

Figure 24. USB supply configurations



6.5 Power supply supervision

Power supply level monitoring is available on the following supplies:

- V_{DD} via POR/PDR (see *Section 6.5.1*), BOR (see *Section 6.5.2*) and PVD monitor (see *Section 6.5.3*)
- V_{DDA} via AVD monitor (see *Section 6.5.4*)
- V_{BAT} via VBAT threshold (see *Section 6.5.5*)
- V_{SW} via rst_vsw, which keeps V_{SW} domain in Reset mode as long as the level is not OK.
- V_{BKP} via a BRRDY bit in *PWR control register 2 (PWR_CR2)*.
- $V_{DD33USB}$ via USBRDY bit in *PWR control register 3 (PWR_CR3)*.

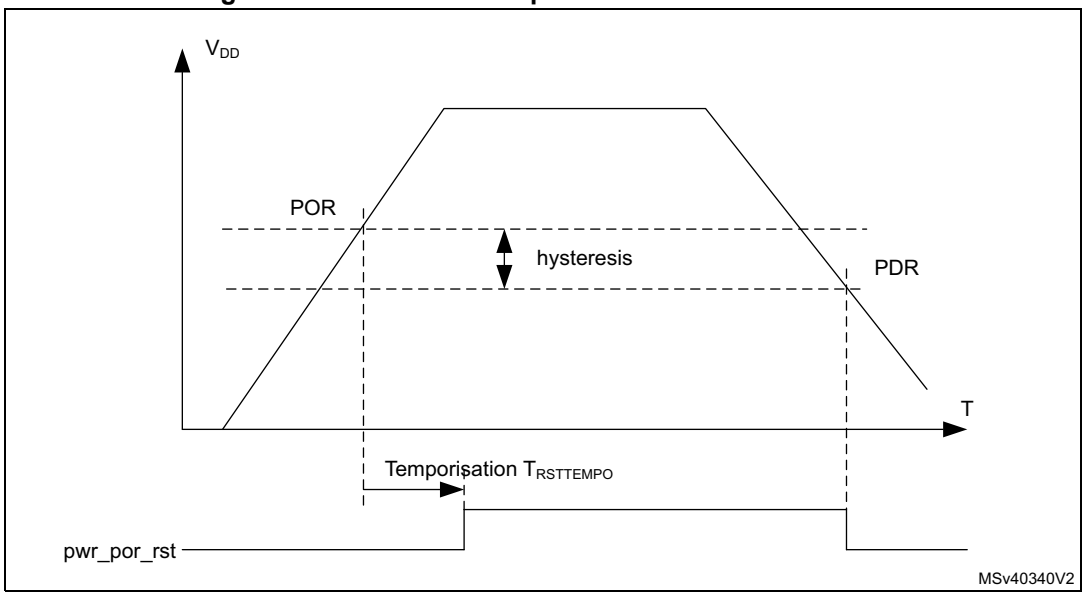
6.5.1 Power-on reset (POR)/power-down reset (PDR)

The system has an integrated POR/PDR circuitry that ensures proper startup operation.

The system remains in Reset mode when V_{DD} is below a specified V_{POR} threshold, without the need for an external reset circuit. Once the V_{DD} supply level is above the V_{POR} threshold, the system is taken out of reset (see *Figure 25*). For more details concerning the power-on/power-down reset threshold, refer to the electrical characteristics section of the datasheets.

The PDR can be enabled/disabled by the device PDR_ON input pin.

Figure 25. Power-on reset/power-down reset waveform



1. For thresholds and hysteresis values, please refer to the datasheets.

6.5.2 Brownout reset (BOR)

During power-on, the Brownout reset (BOR) keeps the system under reset until the V_{DD} supply voltage reaches the specified V_{BOR} threshold.

The V_{BOR} threshold is configured through system option bytes. By default, BOR is OFF. The following programmable V_{BOR} thresholds can be selected:

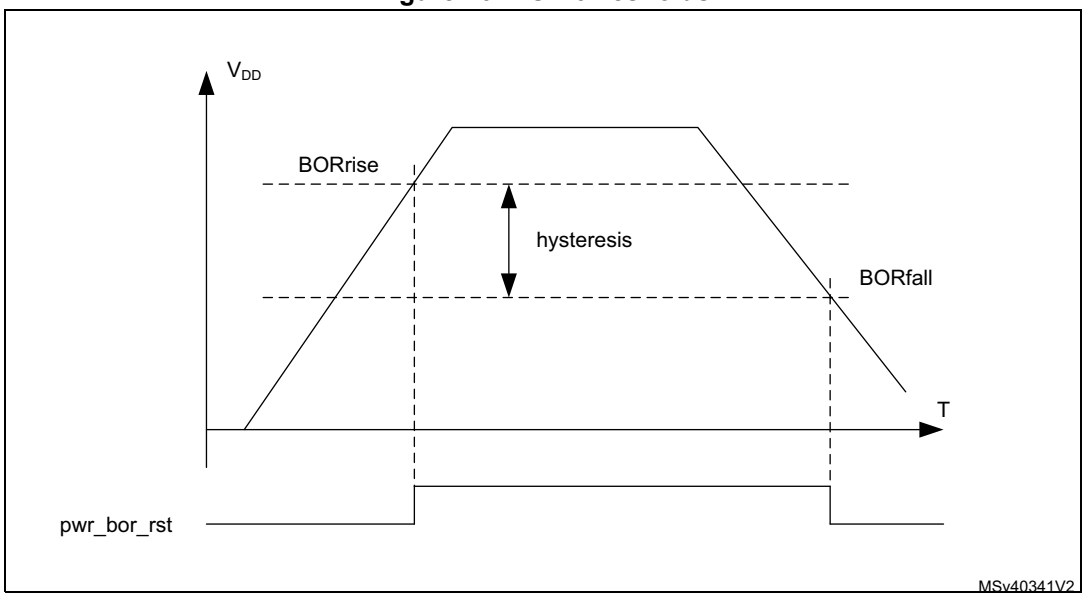
- BOR OFF (V_{BOR0})
- BOR Level 1 (V_{BOR1})
- BOR Level 2 (V_{BOR2})
- BOR Level 3 (V_{BOR3})

For more details on the brown-out reset thresholds, refer to the section “Electrical characteristics” of the product datasheets.

A system reset is generated when the BOR is enabled and V_{DD} supply voltage drops below the selected V_{BOR} threshold.

BOR can be disabled by programming the system option bytes. To disable the BOR function, V_{DD} must have been higher than V_{BOR0} to start the system option byte programming sequence. The power-down is then monitored by the PDR (see *Section 6.5.1*).

Figure 26. BOR thresholds



1. For thresholds and hysteresis values, please refer to the datasheets.

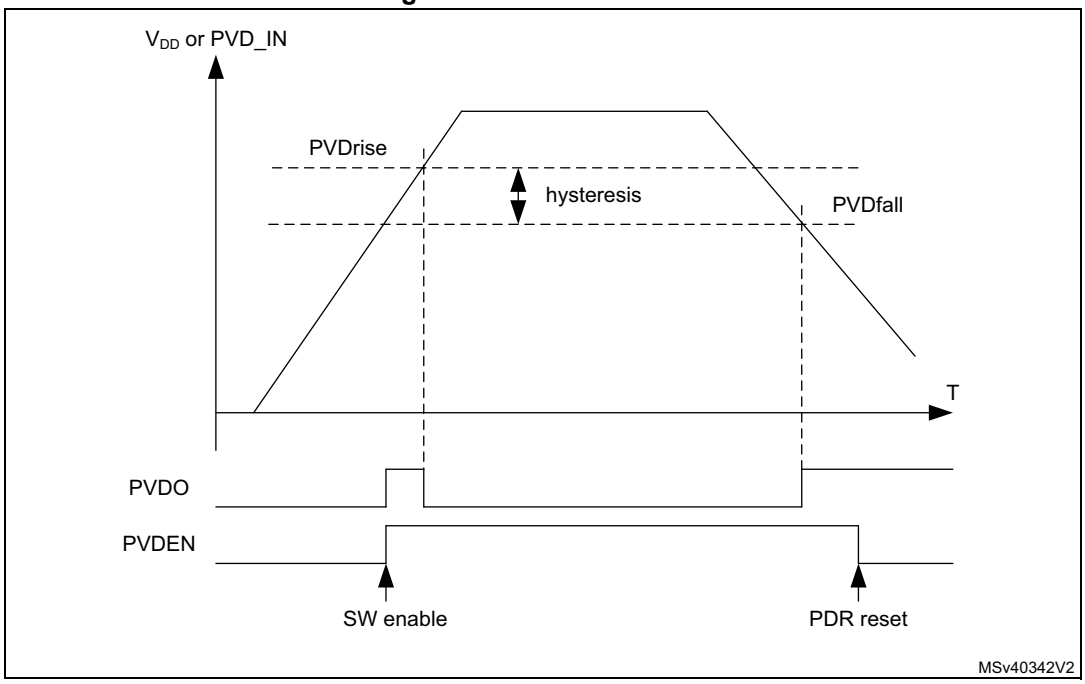
6.5.3 Programmable voltage detector (PVD)

The PVD can be used to monitor the V_{DD} power supply by comparing it to a threshold selected by the PLS[2:0] bits in the *PWR control register 1 (PWR_CR1)*. The PVD can also be used to monitor a voltage level on the PVD_IN pin. In this case PVD_IN voltage is compared to the internal V_{REFINT} level.

The PVD is enabled by setting the PVDE bit in *PWR control register 1 (PWR_CR1)*.

A PVDO flag is available in the *PWR control status register 1 (PWR_CSR1)* to indicate if V_{DD} or PVD_IN voltage is higher or lower than the PVD threshold. This event is internally connected to the EXTI and can generate an interrupt, assuming it has been enabled through the EXTI registers. The pwr_pvd_wkup output interrupt can be generated when V_{DD} or PVD_IN voltage drops below the PVD threshold and/or when V_{DD} or PVD_IN voltage rises above the PVD threshold depending on EXTI rising/falling edge configuration. As an example the service routine could perform emergency shutdown tasks.

Figure 27. PVD thresholds



1. For thresholds and hysteresis values, please refer to the datasheets.

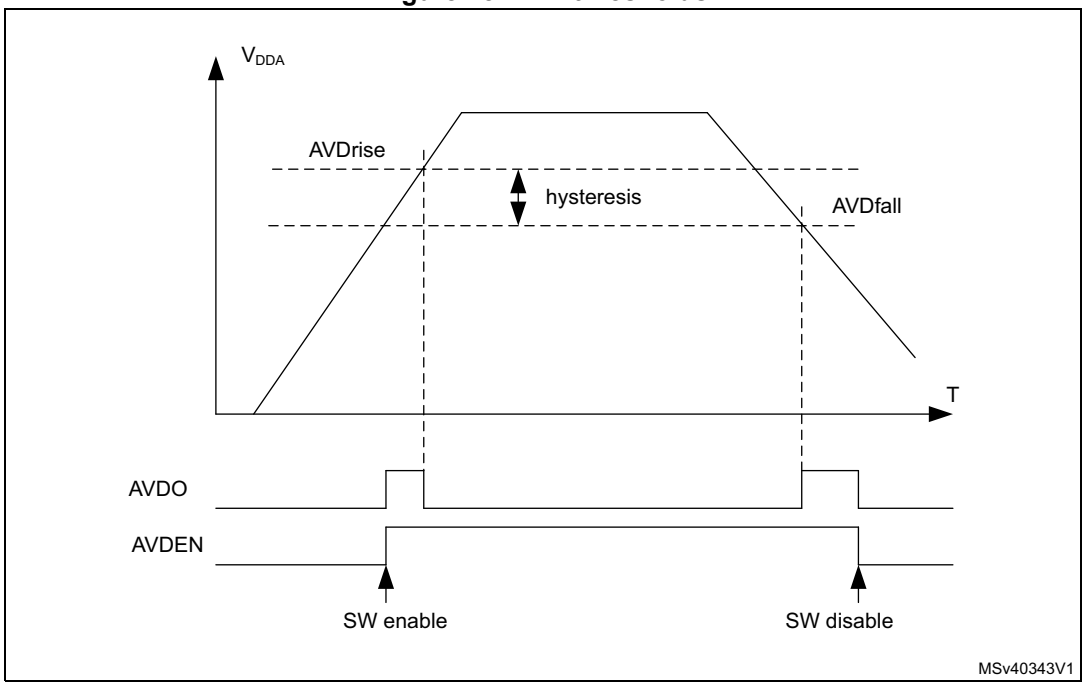
6.5.4 Analog voltage detector (AVD)

The AVD can be used to monitor the V_{DDA} supply by comparing it to a threshold selected by the ALS[1:0] bits in the *PWR control register 1 (PWR_CR1)*.

The AVD is enabled by setting the AVDEN bit in *PWR control register 1 (PWR_CR1)*.

An AVDO flag is available in the *PWR control status register 1 (PWR_CSR1)* to indicate whether V_{DDA} is higher or lower than the AVD threshold. This event is internally connected to the EXTI and can generate an interrupt if enabled through the EXTI registers. The pwr_avd_wkup interrupt can be generated when V_{DDA} drops below the AVD threshold and/or when V_{DDA} rises above the AVD threshold depending on EXTI rising/falling edge configuration. As an example the service routine could indicate when the V_{DDA} supply drops below a minimum level.

Figure 28. AVD thresholds



1. For thresholds and hysteresis values, please refer to the datasheets.

6.5.5 Battery voltage thresholds

The battery voltage supply monitors the backup domain V_{SW} level. Vsw is monitored by comparing it with two threshold levels: $V_{BAThigh}$ and V_{BATlow}. VBATH and VBATL flags in the *PWR control register 2 (PWR_CR2)*, indicate if V_{SW} is higher or lower than the threshold.

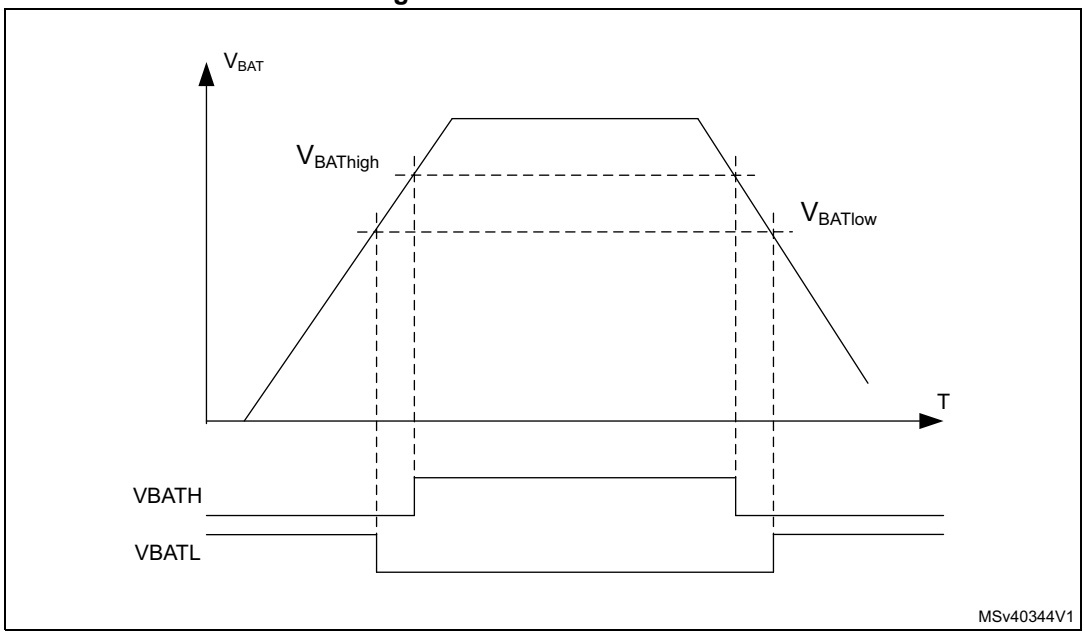
The V_{BAT} supply monitoring can be enabled/disabled via MONEN bit in *PWR control register 2 (PWR_CR2)*. When it is enabled, the battery voltage thresholds increase power consumption. As an example the V_{SW} levels monitoring could be used to trigger a tamper event for an over or under voltage of the RTC power supply domain (available in VBAT mode).

VBATH and VBATL are connected to RTC tamper signals (see *Section 46: Real-time clock (RTC)*).

Note: Battery voltage monitoring is only available when the backup regulator is enabled (BREN bit set in PWR control register 2 (PWR_CR2)).

When the device does not operate in VBAT mode, the battery voltage monitoring checks V_{DD} level. When V_{DD} is available, V_{SW} is connected to V_{DD} through the internal power switch (see Section 6.4.4: Backup domain).

Figure 29. VBAT thresholds



1. For thresholds and hysteresis values, please refer to the datasheets.

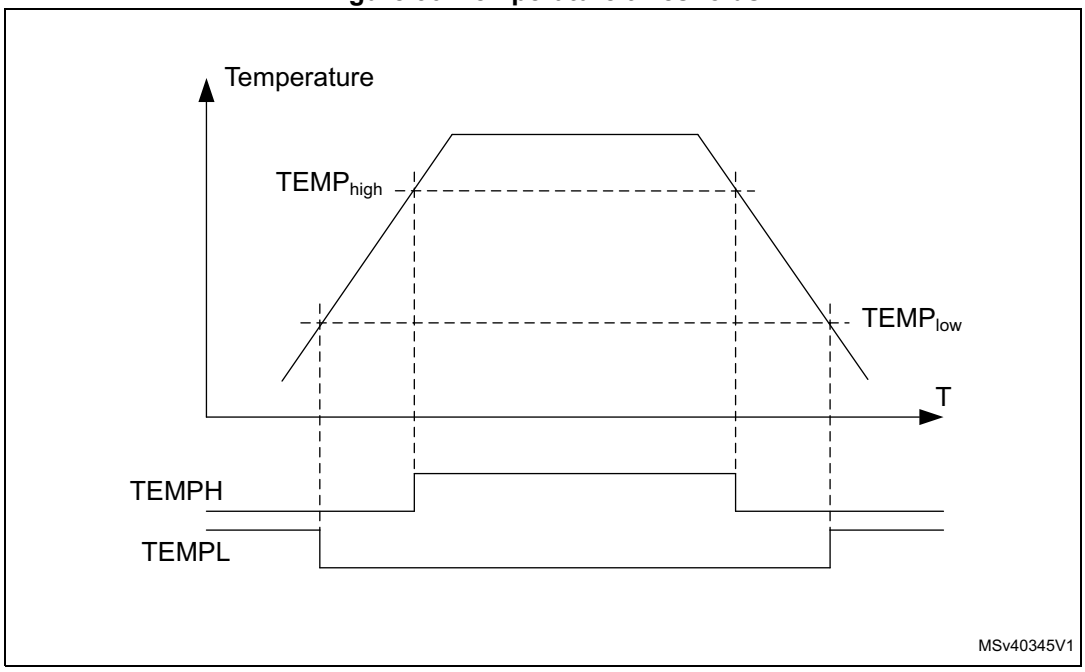
6.5.6 Temperature thresholds

The junction temperature can be monitored by comparing it with two threshold levels, $TEMP_{high}$ and $TEMP_{low}$. TEMPH and TEMPL flags, in the *PWR control register 2 (PWR_CR2)*, indicate whether the device temperature is higher or lower than the threshold. The temperature monitoring can be enabled/disabled via MONEN bit in *PWR control register 2 (PWR_CR2)*. When enabled, the temperature thresholds increase power consumption. .

The temperature thresholds are available only when the backup regulator is enabled (BREN bit set in the PWR_CR2 register).

TEMPH and TEMPL wakeup interrupts are available on the RTC tamper signals (see *Section 46: Real-time clock (RTC)*).

Figure 30. Temperature thresholds



1. For thresholds and hysteresis values, please refer to the datasheets.

6.6 Power management

The power management block controls the V_{CORE} supply in accordance with the system operation modes (see *Section 6.6.1*).

The V_{CORE} domain is split into the following power domains.

- D1 domain containing some peripherals and the Cortex®-M7 Core (CPU).
- D2 domain containing a large part of the peripherals.
- D3 domain containing some peripherals and the system control.

The D1, D2 and system D3 power domains can operate in one of the following operating modes:

- DRun/Run/Run* (power ON, clock ON)
- DStop/Stop (power ON, clock OFF)
- DStandby/Standby (Power OFF, clock OFF).

The operating modes for D1 domain and D2 domain are independent. However system D3 domain power modes depend on D1 and D2 domain modes:

- For system D3 domain to operate in Stop mode, both D1 and D2 domains must be in DStop or DStandby mode.
- For system D3 domain to operate in Standby mode, both D1 and D2 domains must be in DStandby too.

D1, D2 and system D3 domains are supplied from a single regulator at a common V_{CORE} level. The V_{CORE} supply level follows the system operating mode (Run, Stop, Standby). The D1 domain and/or D2 domain supply can be powered down individually when the domains are in DStandby mode.

The following voltage scaling features allow controlling the power with respect to the required system performance (see *Section 6.6.2: Voltage scaling*):

- To obtain a given system performance, the corresponding voltage scaling shall be set in accordance with the system clock frequency. To do this, configure the VOS bits to the Run mode voltage scaling.
- To obtain the best trade-off between power consumption and exit-from-Stop mode latency, configure the SVOS bits to Stop mode voltage scaling.

6.6.1 Operating modes

Several system operating modes are available to tune the system according to the performance required, i.e. when the CPU does not need to execute code and is waiting for an external event. It is up to the user to select the operating mode that gives the best compromise between low power consumption, short startup time and available wakeup sources.

The operating modes allow controlling the clock distribution to the different system blocks and powering them. The system operating mode is driven by the CPU subsystem, D2 domain and system D3 autonomous wakeup. The CPU subsystem can include multiple domains depending on its peripheral allocation (see *Section 8.5.11: Peripheral clock gating control*).

The following operating modes are available for the different system blocks (see *Table 35*):

- CPU subsystem modes:
  - **CRun**

    CPU and CPU subsystem peripheral(s) allocated via RCC PERxEN bits are clocked.
  - **CSleep**:

    The CPU clocks is stalled and the CPU subsystem allocated peripheral(s) clock operate according to RCC PERxLPEN.
  - **CStop**:

    CPU and CPU subsystem peripheral(s) clocks are stalled.
- D1 domain mode:
  - DRun

    The domain bus matrix is clocked. The CPU subsystem operates in CRun or CSleep mode.
  - DStop

    The domain bus matrix clock is stalled.

    The CPU subsystem operates in CStop mode and the PDDS_D1[(a)] bit selects DStop mode.
  - DStandby

    The domain is powered down.

    The CPU subsystem operates in CStop mode and the PDDS_D1 bit selects DStandby mode.
- D2 domain mode:
  - DRun

    The domain bus matrix is clocked.

    The CPU subsystem has an allocated peripheral in the D2 domain and the CPU subsystem operates in CRun or CSleep mode.

a. The PDDS_Dn bits belong to *PWR CPU control register (PWR_CPUCR)*.

  - DStop

    The domain bus matrix clock is stalled.

    The CPU subsystem has no peripherals allocated in the D2 domain and PDDS_D2(*a*) bit selects DStop mode,

    or

    the CPU subsystem has an allocated peripheral in D2 domain, the CPU subsystem operates in CStop mode and PDDS_D2 bit selects DStop mode.
  - DStandby

    The domain is powered down.

    The CPU subsystem has no peripherals allocated in the D2 domain and PDDS_D2 bit selects DStandby mode,

    or

    the CPU subsystem has an allocated peripheral in the D2 domain, the CPU subsystem operates in CStop mode and PDDS_D2 bit selects DStandby mode.

- System /D3 domain modes
  - **Run/Run***

    The system clock and D3 domain bus matrix clock are running:
    - The CPU subsystem is in CRun or CSleep mode
    or
    - A wakeup signal is active. (i.e. System D3 autonomous mode)

    The Run* mode is entered after a POR reset and a wakeup from Standby. In Run* mode, the performance is limited and the system supply configuration shall be programmed in *PWR control register 3 (PWR_CR3)*. The system enters Run mode only when the ACTVOSRDY bit in *PWR control status register 1 (PWR_CSR1)* is set to 1.
  - **Stop**

    The system clock and D3 domain bus matrix clock is stalled:
    - The CPU subsystem is in CStop mode.
    and
    - all wakeup signals are inactive.
    and
    - At least one PDDS_Dn(a) bit for any domain select Stop mode.
  - **Standby**

    The system is powered down:
    - The CPU subsystem is in CStop mode
    and
    - all wakeup signals are inactive.
    and
    - All PDDS_Dn(a) bits for all domains select Standby mode.

In Run mode, power consumption can be reduced by one of the following means:

- Lowering the system performance by slowing down the system clocks and reducing the V_{CORE} supply level through VOS voltage scaling bits.
- Gating the clocks to the APBx and AHBx peripherals when they are not used, through PERxEN bits.

Table 35. Low-power mode summary

System	Domain	CPU	Entry	Wakeup	Sys-oscillator	System clk	Domain bus matrix clk	Peripheral clk	CPU clk	Voltage regulator	Domain supply
Run	DRun(1)	CRun	-	-	ON	ON	ON	ON	ON	ON	ON
		CSleep	WFI or return from ISR or WFE	Any interrupt or event				ON/OFF(2)	OFF		
	DStop(3)	CStop	SLEEPDEEP bit + WFI or return from ISR or WFE	Any EXTI interrupt or event			OFF	ON/OFF(4)			OFF
	DStandby(3)										
Stop(5)	DStop(3)		SLEEPDEEP bit + WFI or return from ISR or WFE or Wakeup source cleared(6)		ON/OFF(7)	OFF		OFF			ON
	DStandby(3)										OFF
Standby(8)	DStandby(3)		All PDDS_Dn bit + SLEEPDEEP bit + WFI or return from ISR or WFE or Wakeup source cleared(6)	WKUP pins rising or falling edge, RTC alarm (Alarm A or Alarm B), RTC Wakeup event, RTC tamper events, RTC time stamp event, external reset in NRST pin, IWDG reset	OFF					OFF	

1. The CPU subsystem has an allocated peripheral in the D2 domain and operates in CRun or CSleep mode.
2. The CPU subsystem peripherals that have a PERxLPEN bit will operate accordingly.
3. If the CPU subsystem has an allocated peripheral in the D2 domain, it must operate in CStop mode.
4. The CPU subsystem peripherals that have a PERxAMEN bit will operate accordingly.
5. All domains need to be in DStop Or DStandby.
6. When the CPU is in CStop and D3 domain in autonomous mode, the last EXTI Wakeup source is cleared.
7. When the system oscillator HSI or CSI is used, the state is controlled by HSIKERON and CSIKERON, otherwise the system oscillator is OFF.
8. All domains are in DStandby mode.

6.6.2 Voltage scaling

The D1, D2, and D3 domains are supplied from a single voltage regulator supporting voltage scaling with the following features:

- Run mode voltage scaling
  - VOS0: Scale 0 (V_{CORE} boost)
  - VOS1: Scale 1
  - VOS2: Scale 2
  - VOS3: Scale 3
- Stop mode voltage scaling
  - SVOS3: Scale 3
  - LP-SVOS4: Scale 4
  - LP-SVOS5: Scale 5

For more details on voltage scaling values, refer to the product datasheets.

After reset, the system starts on the lowest Run mode voltage scaling (VOS3). The voltage scaling can then be changed on-the-fly by software by programming VOS bits in *PWR D3 domain control register (PWR_D3CR)* according to the required system performance. When exiting from Stop mode or Standby mode, the Run mode voltage scaling is reset to the default VOS3 value.

Before entering Stop mode, the software can preselect the SVOS level in *PWR control register 1 (PWR_CR1)*. The Stop mode voltage scaling for SVOS4 and SVOS5 also sets the voltage regulator in Low-power (LP) mode to further reduce power consumption. When preselecting SVOS3, the use of the voltage regulator low-power mode (LP) can be selected by LPDS register bit.

VOS0 activation/deactivation sequence

The system maximum frequency can be reached by boosting the voltage scaling level to VOS0. This is done through the ODEN bit in the SYSCFG_PWRCR register.

The sequence to activate the VOS0 is the following:

1. Ensure that the system voltage scaling is set to VOS1 by checking the VOS bits in PWR D3 domain control register (*PWR D3 domain control register (PWR_D3CR)*)
2. Enable the SYSCFG clock in the RCC by setting the SYSCFGEN bit in the RCC_APB4ENR register.
3. Enable the ODEN bit in the SYSCFG_PWRCR register.
4. Wait for VOSRDY to be set.

Once the V_{CORE} supply has reached the required level, the system frequency can be increased. *Figure 31* shows the recommended sequence for switching V_{CORE} from VOS1 to VOS0 sequence.

The sequence to deactivate the VOS0 is the following:

1. Ensure that the system frequency was decreased.
2. Ensure that the SYSCFG clock is enabled in the RCC by setting the SYSCFGEN bit set in the RCC_APB4ENR register.
3. Reset the ODEN bit in the SYSCFG_PWRCR register to disable VOS0.

Once VOS0 is disabled, the voltage scaling can be reduced further by configuring VOS bits in PWR D3 domain control register (PWR_D3CR) according to the required system performance.

Note: VOS0 can be enabled only when VOS1 is programmed in PWR D3 domain control register (PWR_D3CR) VOS bits. VOS0 deactivation must be managed by software before the system enters low-power mode.

Figure 31. Switching V_{CORE} from VOS1 to VOS0

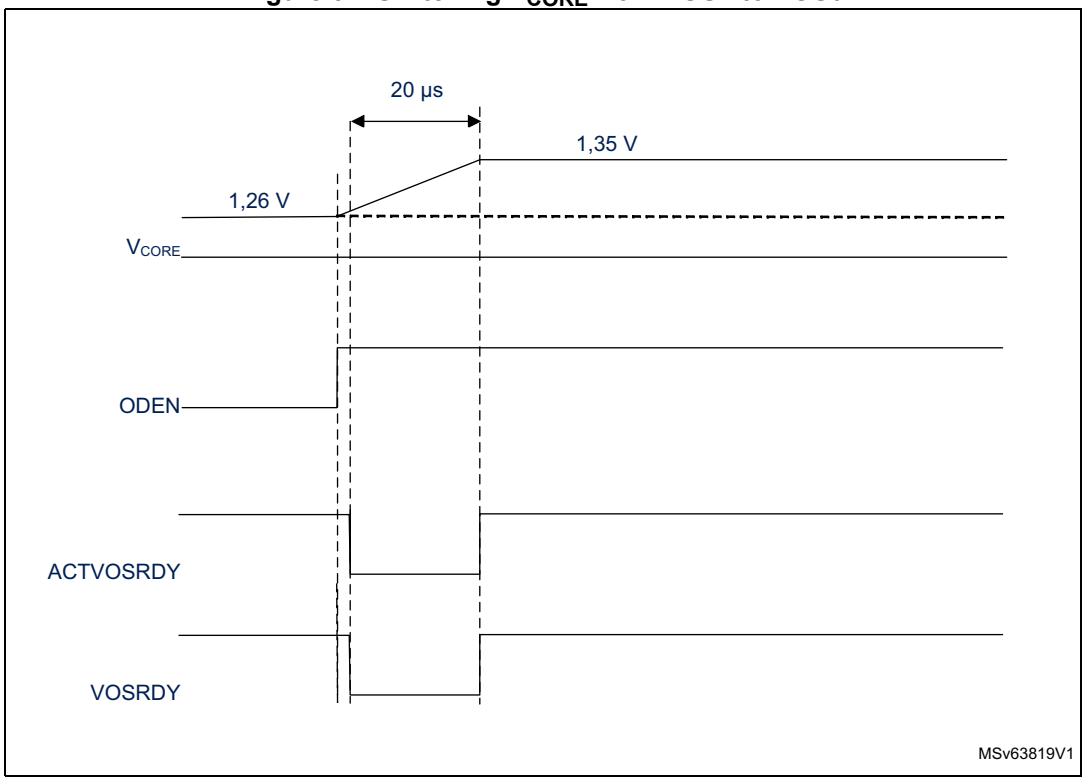
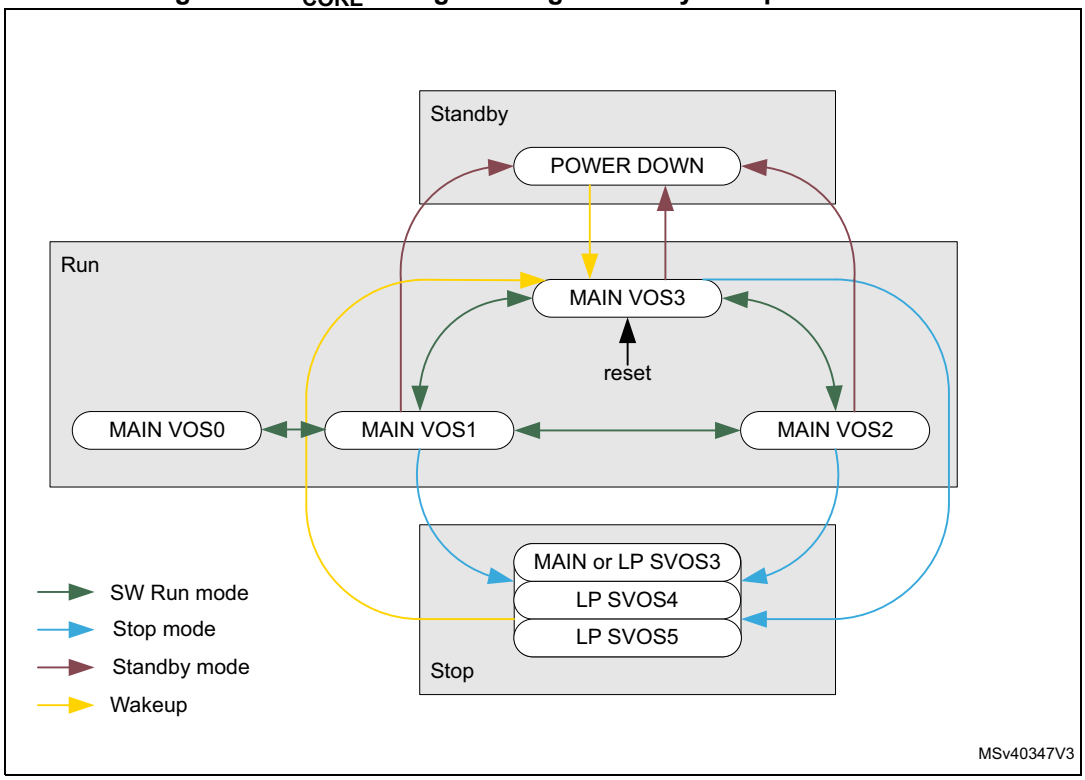


Figure 32. V_{CORE} voltage scaling versus system power modes



6.6.3 Power control modes

The power control block handles the V_{CORE} supply for system Run, Stop and Standby modes.

The system operating mode depends on the CPU subsystem modes (CRun, CSleep, CStop), on the domain modes (DRun, DStop, DStandby), and on the system D3 autonomous wakeup:

- In Run mode, V_{CORE} is defined by the VOS voltage scaling.
  The CPU subsystem is in CRun or CSleep or an EXTI wakeup is active.
- In Stop mode, V_{CORE} is defined by the SVOS voltage scaling.
  The CPU subsystem is in CStop mode and all EXTI wakeups are inactive. The D1 domain and D2 domain are either in DStop or DStandby mode.
- In Standby mode, V_{CORE} supply is switched off.
  The CPU subsystem is in CStop mode and all EXTI wakeups are inactive. The D1 domain and D2 domain are both in DStandby mode.

The domain operating mode can depend on the CPU subsystem when peripherals are allocated in the corresponding domain. The domain mode selection between DStop and DStandby is configured via domain dedicated PDDS_Dn bits in *PWR CPU control register (PWR_CPUCR)*. The CPU can choose to keep a domain in DStop, or allow a domain to enter DStandby mode.

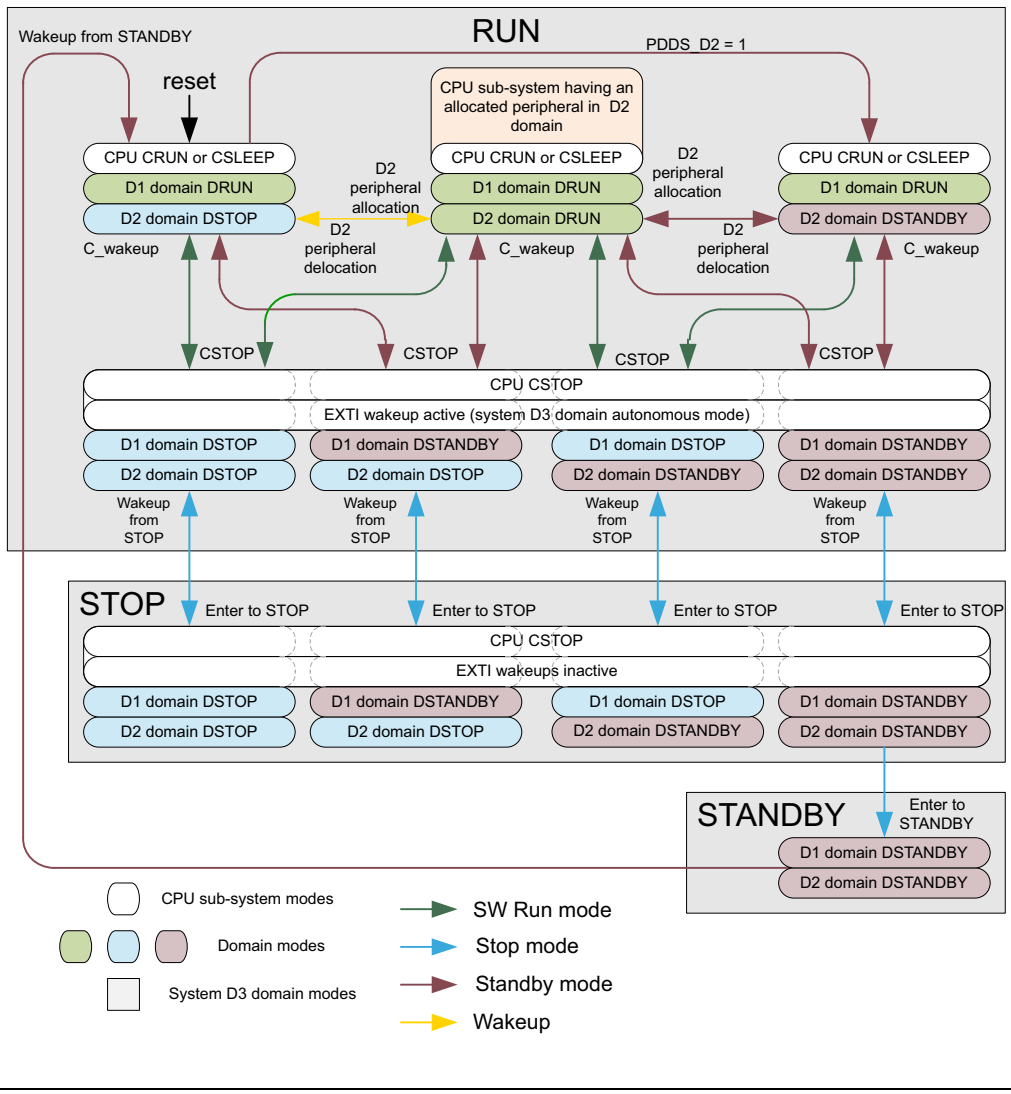
If a domain is in DStandby mode, the corresponding power is switched off.

All the domains can be configured for the system mode (Stop or Standby) through PDDS_Dn bits in *PWR CPU control register (PWR_CPUCR)*. The system enters Standby only when all PDDS_Dn bits for all domains have allowed it.

Table 36. PDDS_Dn low-power mode control

PWR_CPUCR			D1 mode	D2 mode	D3 mode
PDDS_D1	PDDS_D2	PDDS_D3			
0	x	x	DStop	any	Run or Stop
1			DStandby	any	any
x	0		any	DStop	Run or Stop
	1		any	DStandby	any
at least one = 0			DStop or DStandby	DStop or DStandby	Stop
1	1	1	DStandby	DStandby	Standby

Figure 33. Power control modes detailed state diagram



After a system reset, the CPU is in CRun mode.

Power control state transitions are initiated by the following events:

- CPU going to CStop mode (state transitions in Run mode are marked in green and red)
  - Green transitions: CPU wakes up as from CSleep.
  - Red transitions: CPU wakes up with domain reset. The SBF_Dn is set.
- Allocating or de-locating a peripheral in a domain (state transitions in Run mode are marked in orange and red)
  - Orange transitions: the domain wakes up from DStop
  - Red transitions: the domain wakes up from DStandby. The SBF_Dn is set.
- The system enters or exits from Stop mode (state transitions marked in blue)
  - Blue transitions the system wakes up from Stop mode. The STOPF is set.
- The system enters or exits from Standby mode (state transitions in Stop and Standby mode are marked in red).
  - When exiting from Standby mode, the SBF is set.

When a domain exits from DStandby, the domain peripherals are reset, while the domain SBF_Dn bit is set (state transitions causing a domain reset are marked in red).

Table 37 shows the flags that indicate from which mode the domain/system exits. The CPU features a set of flags which can be read from *PWR CPU control register (PWR_CPUCR)*.

Table 37. Low-power exit mode flags

System mode	D1 domain mode	D2 domain mode	SBF_D1	SBF_D2	SBF	STOPF	Comment
Run	DRun or DStop	DRun or DStop	0	0	0	0	D1, D2 and system contents retained
Run	DStandby	DStop	1	0	0	0	D1 contents lost, D2 and system contents retained
Run	DRun or DStop	DStandby	0	1	0	0	D2 contents lost, D1 and system contents retained
Run	DStandby	DStandby	1	1	0	0	D1 and D2 contents lost, system contents retained
Stop	DStop	DStop	0	0	0	1	D1, D2 and system contents retained, clock system reset.
Stop	DStandby	DStop	1	0	0	1	D1 contents lost, D2 and system contents retained, clock system reset
Stop	DStop	DStandby	0	1	0	1	D2 contents lost, D1 and system contents retained, clock system reset
Stop	DStandby	DStandby	1	1	0	1	D1 and D2 contents lost, system contents retained, clock system reset
Standby	DStandby	DStandby	0(1)	0(1)	1	0	D1, D2 and system contents lost

1. When returning from Standby, the SBF_D1 and SBF_D2 reflect the reset value.

6.6.4 Power management examples

- *Figure 34* shows V_{CORE} voltage scaling behavior in Run mode.
- *Figure 35* shows V_{CORE} voltage scaling behavior in Stop mode.
- *Figure 36* shows V_{CORE} voltage regulator and voltage scaling behavior in Standby mode.
- *Figure 37* shows V_{CORE} voltage scaling behavior in Run mode with D1 and D2 domains are in DStandby mode

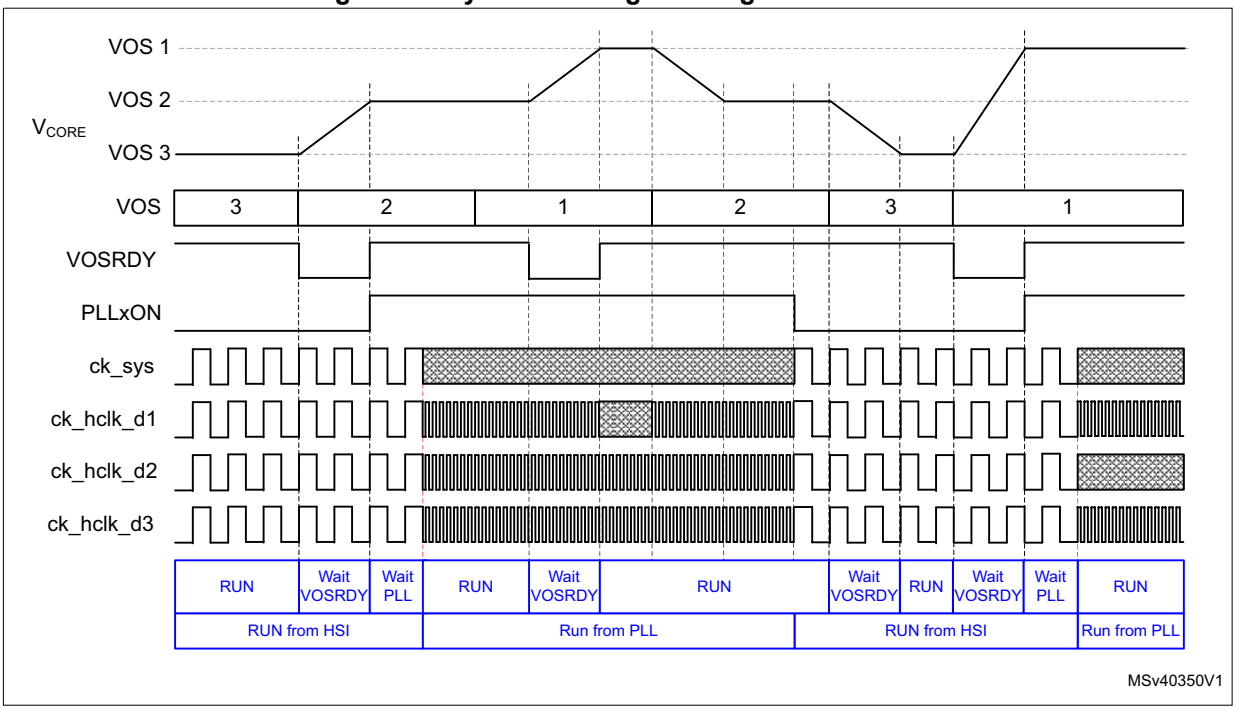
Example of V_{CORE} voltage scaling behavior in Run mode

Figure 34 illustrates the following system operation sequence example:

1. After reset, the system starts from HSI with VOS3.
2. The system performance is first increased to a medium-speed clock from the PLL with voltage scaling VOS2. To do this:
   a) Program the voltage scaling to VOS2.
   b) Once the V_{CORE} supply has reached the required level indicated by VOSRDY, increase the clock frequency by enabling the PLL.
   c) Once the PLL is locked, switch the system clock.
3. The system performance is then increased to high-speed clock from the PLL with voltage scaling VOS1. To do this:
   a) Program the voltage scaling to VOS1.
   b) Once the V_{CORE} supply has reached the required level indicated by VOSRDY, increase the clock frequency.
4. The system performance is then reduced to a medium-speed clock with voltage scaling VOS2. To do this:
   a) First decrease the system frequency.
   b) Then decrease the voltage scaling to VOS2.
5. The next step is to reduce the system performance to HSI clock with voltage scaling VOS3. To do this:
   a) Switch the clock to HSI.
   b) Disable the PLL.
   c) Decrease the voltage scaling to VOS3.
6. The system performance can then be increased to high-speed clock from the PLL. To do this:
   a) Program the voltage scaling to VOS1.
   b) Once the V_{CORE} supply has reached the required level indicated by VOSRDY, increase the clock frequency by enabling the PLL.
   c) Once the PLL is locked, switch the system clock.

When the system performance (clock frequency) is changed, VOS shall be set accordingly. otherwise the system might be unreliable.

Figure 34. Dynamic voltage scaling in Run mode



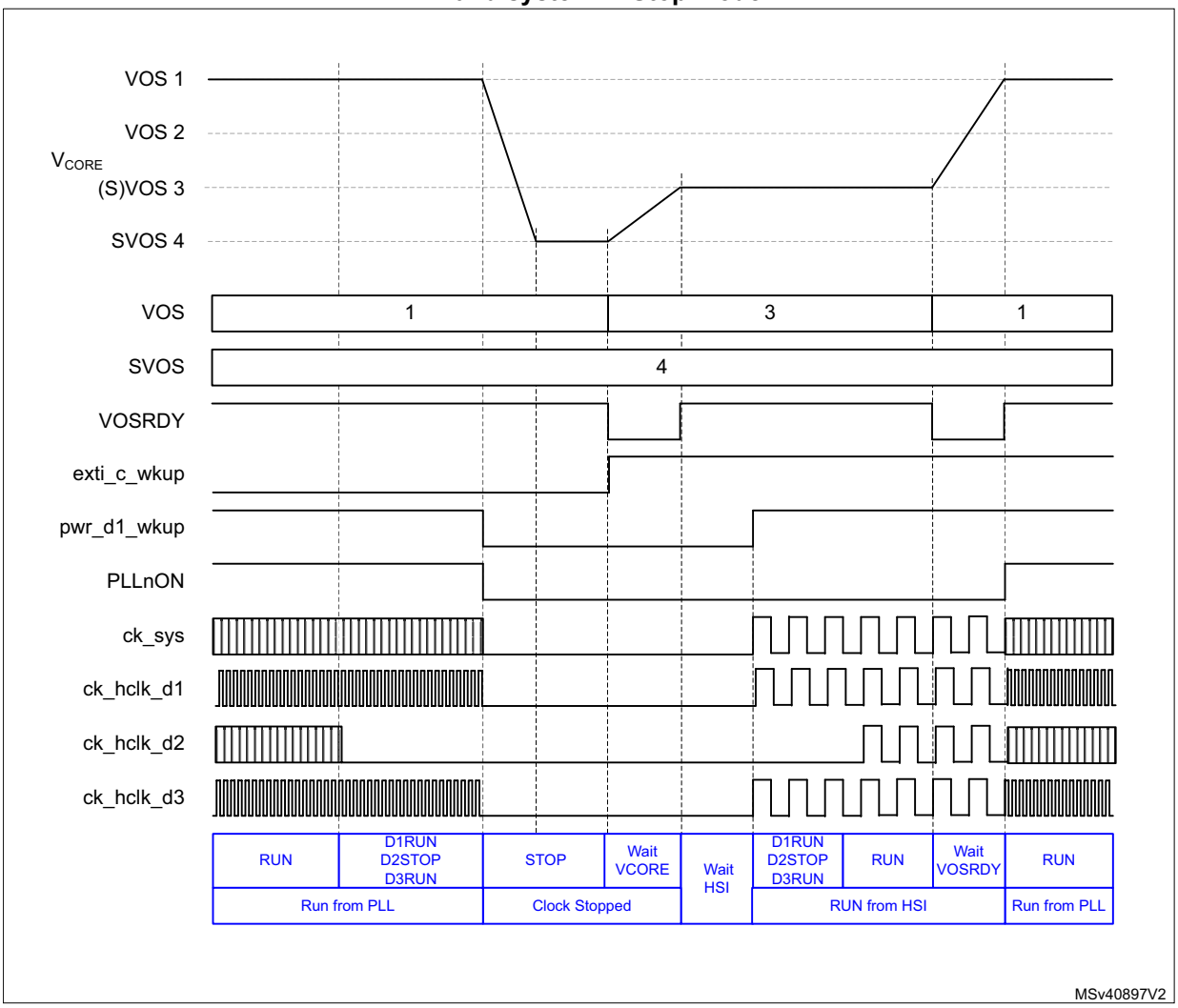
1. The status of the register bits at each step is shown in blue.

Example of V_{CORE} voltage scaling behavior in Stop mode

Figure 35 illustrates the following system operation sequence example:

1. The system is running from the PLL in high-performance mode (VOS1 voltage scaling).
2. The CPU subsystem deallocates all the peripheral in the D2 domain that will first enter DStop mode. D2 system clock is stopped. The system still provides the high-performance system clock, hence the voltage scaling shall stay at VOS1 level.
3. In a second step, the CPU subsystem enters CStop mode, D1 domain enters DStop mode and the system enters Stop mode. The system clock is stopped and the hardware lowers the voltage scaling to the software preselected SVOS4 level.
4. The CPU subsystem is then woken up. The system exits from Stop mode, the D1 domain exits from DStop mode and the CPU subsystem exits from CStop mode. The hardware then sets the voltage scaling to VOS3 level and waits for the requested supply level to be reached before enabling the HSI clock. Once the HSI clock is stable, the system clock and the D1 system clock are enabled.
5. The CPU subsystem allocates a peripheral in the D2 domain. The D2 system clock is enabled.
6. The system performance is then increased. To do this:
   a) The software first sets the voltage scaling to VOS1.
   b) Once the V_{CORE} supply has reached the required level indicated by VOSRDY, the clock frequency can be increased by enabling the PLL.
   c) Once the PLL is locked, the system clock can be switched.

Figure 35. Dynamic voltage scaling behavior with D1, D2 and system in Stop mode



1. The status of the register bits at each step is shown in blue.

Example of V_{CORE} voltage regulator and voltage scaling behavior in Standby mode

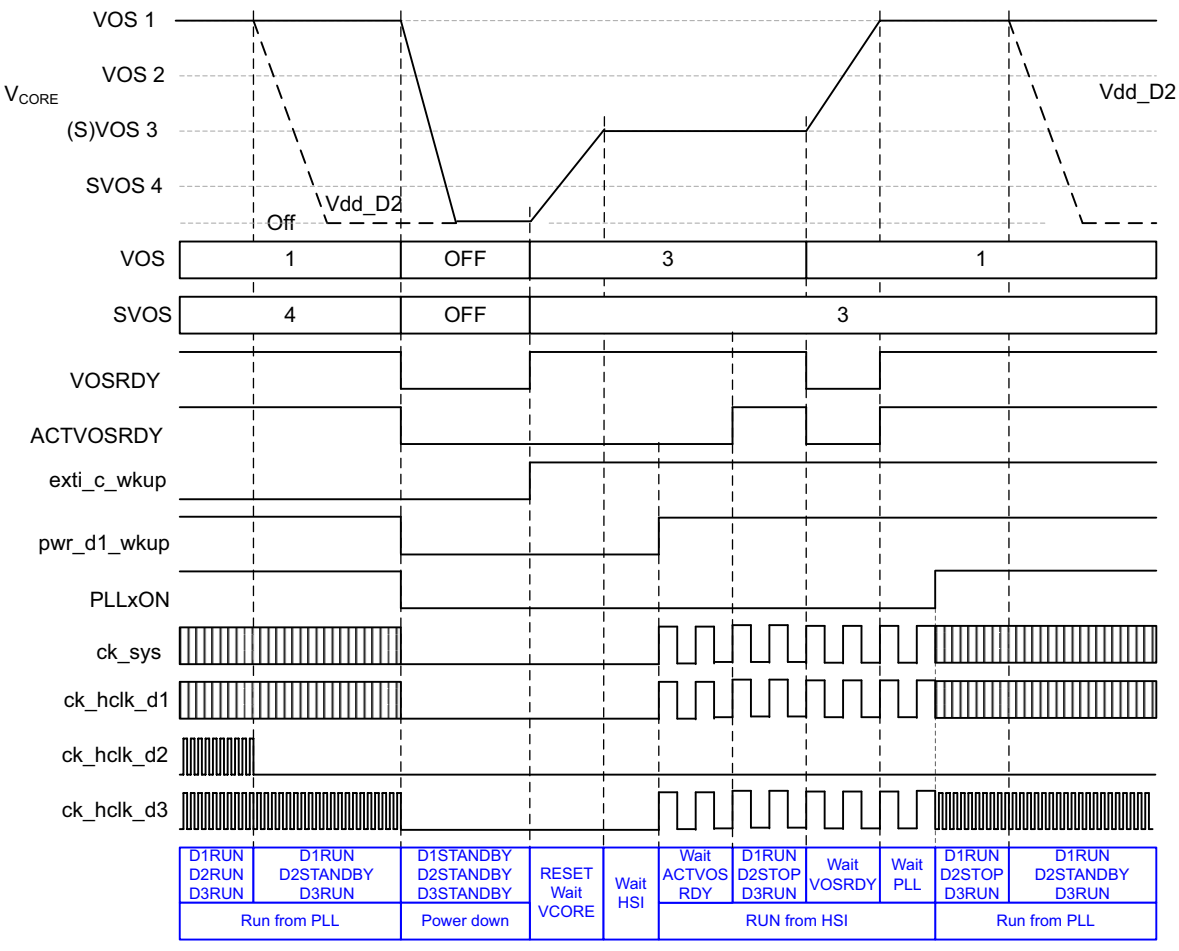
Figure 36 illustrates the following system operation sequence example:

1. The system is running from the PLL in high-performance mode (VOS1 voltage scaling).
2. The CPU subsystem deallocates all the peripherals in the D2 domain that will first enter DStandby mode.The D2 domain bus matrix clock is stopped and the power is switched off. The system performance is unchanged hence the voltage scaling does not change.
3. The CPU subsystem then enters to CStop mode, D1 domain enters DStandby mode and the system enters Standby mode. The system clock is stopped and the voltage regulator switched off.
4. The system is then woken up by a wakeup source. The system exits from Standby mode. The hardware sets the voltage scaling to the default VOS3 level and waits for the requested supply level to be reached before enabling the default HSI oscillator. Once the HSI clock is stable, the system clock and D1 subsystem clock are enabled.

Since there are no allocated peripherals in the D2 domain, this domain remains in DStop mode. The software shall then check the ACTVOSRDY is valid before changing the system performance.

5. In a next step, increase the system performance. To do this:
   a) The software first increases the voltage scaling to VOS1 level
   b) Before enabling the PLL, it waits for the requested supply level to be reached by monitoring VOSRDY bit.
   c) Once the PLL is locked, the system clock can be switched.
6. The CPU subsystem puts the D2 domain in DStandby mode.

Figure 36. Dynamic Voltage Scaling D1, D2, system Standby mode



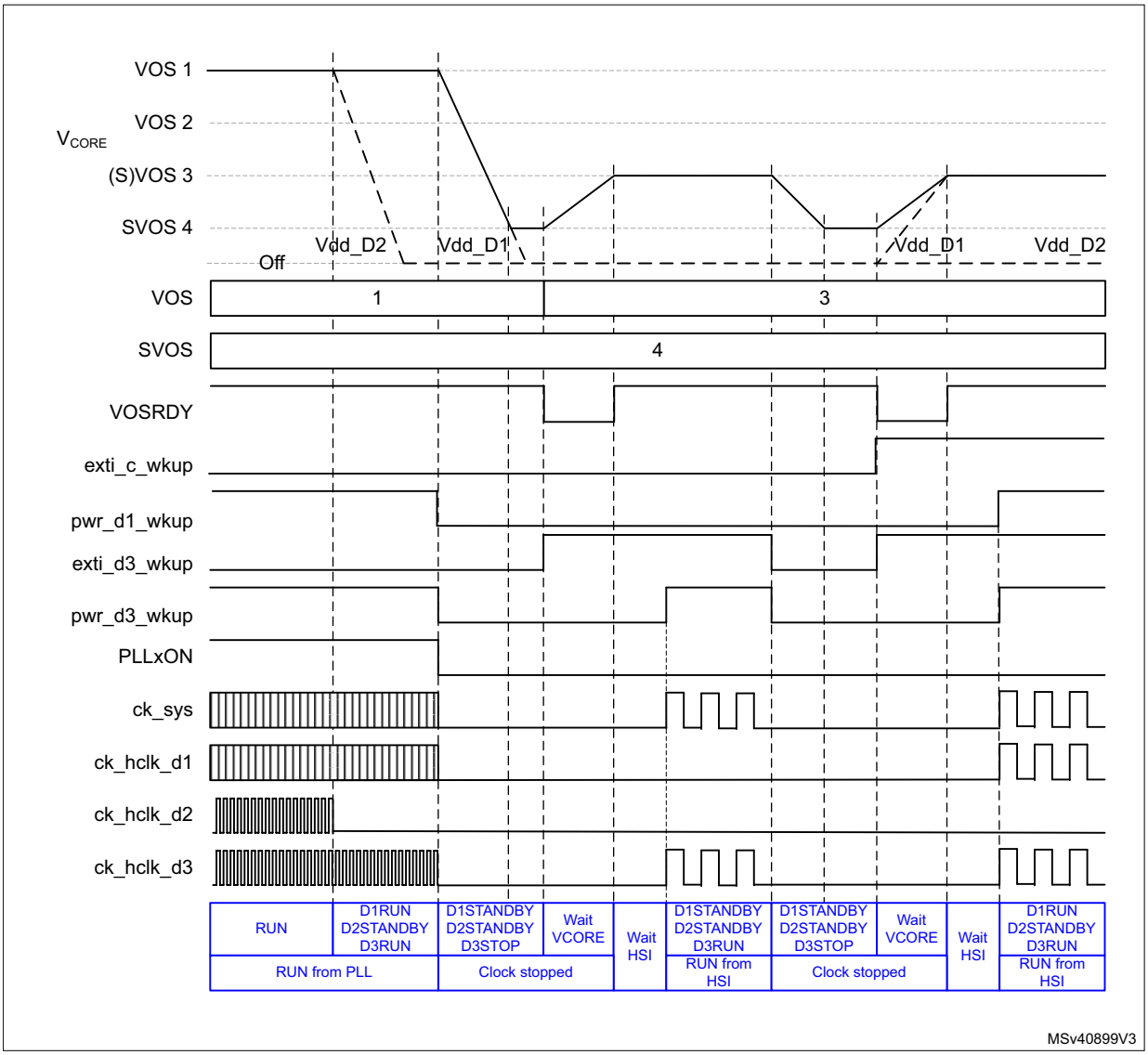
1. The status of the register bits at each step is shown in blue.

Example of V_{CORE} voltage scaling behavior in Run mode with D1 and D2 domains in DStandby mode

Figure 37 illustrates the following system operation sequence example:

1. The system is running from the PLL with system in high performance mode (VOS1 voltage scaling).
2. The CPU subsystem deallocates all the peripherals in the D2 domain that will first enter DStandby mode. The D2 domain bus matrix clock is stopped and its power switched off. The system performance is unchanged hence the voltage scaling does not change.
3. The CPU subsystem then enters CStop mode and the D1 domain enters DStandby mode. The D1 domain bus matrix clock is stopped and its power switched off. At the same time the system enters Stop mode. The system clock is stopped and the hardware lowers the voltage scaling to the software preselected SVOS4 level.
4. The system is then woken up by a D3 autonomous mode wakeup event. The system exits from Stop mode. The hardware sets the voltage scaling to the default VOS3 level and waits for the requested supply level to be reached before enabling the HSI clock. Once the HSI clock is stable, the system clock is enabled. The system is running in D3 autonomous mode.
5. The D3 autonomous mode wakeup source is then cleared, causing the system to enter Stop mode. The system clock is stopped and the voltage scaling is lowered to the software preselected SVOS4 level.
6. The CPU subsystem is then woken up. The system exits from Stop mode, the D1 domain exits from DStandby mode and the CPU subsystem exits from CStop mode. The hardware sets the voltage scaling to the default VOS3 level and waits for the requested supply level to be reached before enabling the default HSI oscillator. Once the HSI clock is stable, the system clock and the D1 subsystem clock are enabled. The D2 domain remains in DStandby mode.

Figure 37. Dynamic voltage scaling behavior with D1 and D2 in DStandby mode and D3 in autonomous mode



1. The status of the register bits at each step is shown in blue.

6.7 Low-power modes

Several low-power modes are available to save power when the CPU does not need to execute code (i.e. when waiting for an external event). It is up to the user application to select the mode that gives the best compromise between low power consumption, short startup time and available wakeup sources:

- Slowing down system clocks (see *Section 8.5.6: System clock (sys_ck)*)
- Controlling individual peripheral clocks (see *Section 8.5.11: Peripheral clock gating control*)
- Low-power modes
  - CSleep (CPU clock stopped)
  - CStop (CPU subsystem clock stopped)
  - DStop (Domain bus matrix clock stopped)
  - Stop (System clock stopped)
  - DStandby (Domain powered down)
  - Standby (System powered down)

6.7.1 Slowing down system clocks

In Run mode, the speed of the system clock ck_sys can be reduced. For more details refer to *Section 8.5.6: System clock (sys_ck)*.

6.7.2 Controlling peripheral clocks

In Run mode, the HCLKx and PCLKx for individual peripherals can be stopped by configuring at any time PERxEN bit in RCC_C1_xxxxENR or RCC_DnxxxxENR to reduce power consumption.

To reduce power consumption in CSleep mode, the individual peripheral clocks can be disabled by configuring PERxLPEN bit in RCC_C1_xxxxLPENR or RCC_DnxxxxLPENR. For the peripherals still receiving a clock in CSleep mode, their clock can be slowed down before entering CSleep mode.

6.7.3 Entering low-power modes

CPU subsystem CSleep and CStop low-power modes are entered by the MCU when executing the WFI (Wait For Interrupt) or WFE (Wait for Event) instructions, or when the SLEEPONEXIT bit in the Cortex®-M System Control register is set on Return from ISR.

A domain can enter DStop or DStandby low-power mode when the CPU subsystem has an allocated peripheral in the domain and enters CStop mode, or when all D2 domain peripherals are deallocated.

The system can enter Stop or Standby low-power mode when all EXTI wakeup sources are cleared and the other domains are in DStop or DStandby mode.

6.7.4 Exiting from low-power modes

The CPU subsystem exits from CSleep mode through any interrupt or event depending on how the low-power mode was entered:

- If the WFI instruction or Return from ISR was used to enter to low-power mode, any peripheral interrupt acknowledged by the NVIC can wake up the system.
- If the WFE instruction is used to enter to low-power mode, the CPU exits from low-power mode as soon as an event occurs. The wakeup event can be generated either by:
  - An NVIC IRQ interrupt.

    When SEVONPEND = 0 in the Cortex®-M7 System Control register, the interrupt must be enabled in the peripheral control register and in the NVIC.

    When the MCU resumes from WFE, the peripheral interrupt pending bit and the NVIC peripheral IRQ channel pending bit in the NVIC interrupt clear pending register have to be cleared. Only NVIC interrupts with sufficient priority will wakeup and interrupt the MCU.

    When SEVONPEND = 1 in the Cortex®-M7 System Control register, the interrupt must be enabled in the peripheral control register and optionally in the NVIC. When the MCU resumes from WFE, the peripheral interrupt pending bit and, when enabled, the NVIC peripheral IRQ channel pending bit (in the NVIC interrupt clear pending register) have to be cleared.

    All NVIC interrupts will wakeup the MCU, even the disabled ones.

    Only enabled NVIC interrupts with sufficient priority will wakeup and interrupt the MCU.
  - An event

    An EXTI line must be configured in event mode. When the CPU resumes from WFE, it is not necessary to clear the EXTI peripheral interrupt pending bit or the NVIC IRQ channel pending bit as the pending bits corresponding to the event line is not set. It might be necessary to clear the interrupt flag in the peripheral.

The CPU subsystem exits from CStop, DStop and Stop modes by enabling an EXTI interrupt or event depending on how the low-power mode was entered (see above).

The system can wakeup from Stop mode by enabling an EXTI wakeup, without waking up a CPU subsystem. In this case the system will operate in D3 autonomous mode.

The CPU subsystem exits from DStandby mode by enabling an EXTI interrupt or event, regardless on how DStandby mode was entered. Program execution restarts from CPU local reset (such as a reset vector fetched from System configuration block (SYSCFG).

The D2 domain can exit from DStop or DStandby mode when the CPU allocates a first peripheral in the domain.

The CPU subsystem exits from Standby mode by enabling an external reset (NRST pin), an IWDG reset, a rising edge on one of the enabled WKUPx pins or a RTC event. Program execution restarts in the same way as after a system reset (such as boot pin sampling, option bytes loading or reset vector fetched).

6.7.5 CSleep mode

The CSleep mode applies only to the CPU subsystem. In CSleep mode, the CPU clock is stopped. The CPU subsystem peripheral clocks operate according to the values of PERxLPEN bits in RCC_C1_xxxxENR or RCC_DnxxxxENR.

Entering CSleep mode

The CSleep mode is entered according to *Section 6.7.3: Entering low-power modes*, when the SLEEPDEEP bit in the Cortex®-M System Control register is cleared.

Refer to *Table 38* for details on how to enter to CSleep mode.

Exiting from CSleep mode

The CSleep mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 38* for more details on how to exit from CSleep mode.

Table 38. CSleep mode

CSleep mode	Description
Mode entry	WFI (Wait for Interrupt) or WFE (Wait for Event) while: – SLEEPDEEP = 0 (Refer to the Cortex®-M System Control register.) – CPU NVIC interrupts and events cleared.
	On return from ISR while: – SLEEPDEEP = 0 and – SLEEPONEXIT = 1 (refer to the Cortex®-M System Control register.) – CPU NVIC interrupts and events cleared.
Mode exit	If WFI or return from ISR was used for entry: – Any Interrupt enabled in NVIC: Refer to *Table 145: NVIC* If WFE was used for entry and SEVONPEND = 0: – Any event: Refer to *Section 20.5.3: EXTI CPU wakeup procedure* If WFE was used for entry and SEVONPEND = 1: – Any Interrupt even when disabled in NVIC: refer to *Table 145: NVIC* or any event: refer to *Section 20.5.3: EXTI CPU wakeup procedure*
Wakeup latency	None

6.7.6 CStop mode

The CStop mode applies only to the CPU subsystem. In CStop mode, the CPU clock is stopped. Most CPU subsystem peripheral clocks are stopped too and only the CPU subsystem peripherals having a PERxAMEN bit operate accordingly.

In CStop mode, the CPU subsystem peripherals that have a kernel clock request can still request their kernel clock. For the peripheral that have a PERxAMEN bit, this bit shall be set to be able to request the kernel clock.

Entering CStop mode

The CStop mode is entered according to *Section 6.7.3: Entering low-power modes*, when the SLEEPDEEP bit in the Cortex®-M System Control register is set.

Refer to *Table 39* for details on how to enter to CStop mode.

Exiting from CStop mode

The CStop mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 39* for more details on how to exit from CStop mode.

Table 39. CStop mode

CStop mode	Description
Mode entry	WFI (Wait for Interrupt) or WFE (Wait for Event) while: – SLEEPDEEP = 1 (Refer to the Cortex®-M System Control register.) – CPU NVIC interrupts and events cleared. – All CPU EXTI Wakeup sources are cleared.
	On return from ISR while: – SLEEPDEEP = 1 and – SLEEPONEXIT = 1 (Refer to the Cortex®-M System Control register.) – CPU NVIC interrupts and events cleared. – All CPU EXTI Wakeup sources are cleared.
Mode exit	If WFI or return from ISR was used for entry: – EXTI Interrupt enabled in NVIC: Refer to *Table 145: NVIC*, for peripheral which are not stopped or powered down. If WFE was used for entry and SEVONPEND = 0: – EXTI event: Refer to *Section 20.5.3: EXTI CPU wakeup procedure*, for peripheral which are not stopped or powered down. If WFE was used for entry and SEVONPEND = 1: – EXTI Interrupt even when disabled in NVIC: refer to *Table 145: NVIC* or EXTI event: refer to *Section 20.5.3: EXTI CPU wakeup procedure*, for peripheral which are not stopped or powered down.
Wakeup latency	EXTI and RCC wakeup synchronization (see *Section 8.4.7: Power-on and wakeup sequences*)

6.7.7 DStop mode

D1 domain and/or D2 domain enters DStop mode only when the CPU subsystem is in CStop mode and has allocated peripheral in the domain (see *Table 40*). In DStop mode the domain bus matrix clock is stopped.

The Flash memory can enter low-power Stop mode when it is enabled through FLPS in PWR_CR1 register. This allows a trade-off between domain DStop restart time and low power consumption.

Table 40. DStop mode overview

Peripheral allocation	CPU	D1 domain	D2 domain	Comment
No peripheral allocated in D2 domain	CRun or CSleep	DRun	DStop	
	CStop	DStop	DStop	
Peripheral allocated in D2 domain	CRun or CSleep	DRun	DRun	CPU subsystem, keep D2 domain active.
	CStop	DStop	DStop	

In DStop mode domain peripherals using the LSI or LSE clock and peripherals having a kernel clock request are still able to operate.

Entering DStop mode

The DStop mode is entered according to *Section 6.7.3: Entering low-power modes*, when at least one PDDS_Dn bit in *PWR CPU control register (PWR_CPUCR)* for the domain select Stop.

Refer to *Table 41* for details on how to enter DStop mode.

If Flash memory programming is ongoing, the DStop mode entry is delayed until the memory access is finished.

If an access to the domain bus matrix is ongoing, the DStop mode entry is delayed until the domain bus matrix access is complete.

Exiting from DStop mode

The DStop mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 41* for more details on how to exit from DStop mode.

When exiting from DStop mode, the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling depend on the system mode.

- When the system did not enter Stop mode, the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling values are the same as when entering DStop mode.
- When the system has entered Stop mode, the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling are reset.

Table 41. DStop mode

DStop mode	Description
Mode entry	– The domain CPU subsystem enters CStop. – The CPU subsystem has an allocated peripheral in the D2 domain and enters CStop. – The CPU subsystem deallocated its last peripheral in the D2 domain. – The PDDS_Dn bit for the domain selects Stop mode.
Mode exit	– The domain CPU subsystem exits from CStop mode (see *Table 39*) – The CPU subsystem has an allocated peripheral in the D2 domain and exits from CStop mode (see *Table 39*) – The CPU subsystem allocates a first peripheral in the D2 domain.
Wakeup latency	EXTI and RCC wakeup synchronization (see *Section 8.4.7: Power-on and wakeup sequences*).

6.7.8 Stop mode

The system D3 domain enters Stop mode only when the CPU subsystem is in CStop mode, the EXTI wakeup sources are inactive and at least one PDDS_Dn bit in *PWR CPU control register (PWR_CPUCR)* for any domain request Stop. In Stop mode, the system clock including a PLL and the D3 domain bus matrix clocks are stopped. When HSI or CSI is selected, the system oscillator operates according to the HSIKERON and CSIKERON bits in RCC_CR register. Other system oscillator sources are stopped.

In system D3 domain Stop mode, D1 domain and D2 domain are either in DStop and/or DStandby mode.

In Stop mode, the domain peripherals that use the LSI or LSE clock, and the peripherals that have a kernel clock request to select HSI or CSI as source, are still able to operate.

In system Stop mode, the following features can be selected to remain active by programming individual control bits:

- Independent watchdog (IWDG)

  The IWDG is started by writing to its Key register or by hardware option. Once started it cannot be stopped except by a Reset (see *Section 45.3* in *Section 45: Independent watchdog (IWDG)*.
- Real-time clock (RTC)

  This is configured via the RTCEN bit in the *RCC backup domain control register (RCC_BDCR)*.
- Internal RC oscillator (LSI RC)

  This is configured via the LSION bit in the *RCC clock control and status register (RCC_CSR)*.
- External 32.768 kHz oscillator (LSE OSC)

  This is configured via the LSEON bit in the *RCC backup domain control register (RCC_BDCR)*.

- Peripherals capable of running on the LSI or LSE clock.
- Peripherals having a kernel clock request.
- Internal RC oscillators (HSI and CSI)

  This is configured via the HSIKERON and CSIKERON bits in the *RCC clock control and status register (RCC_CSR)*.
- The ADC or DAC can also consume power during Stop mode, unless they are disabled before entering this mode. To disable them, the ADON bit in the ADC_CR2 register and the ENx bit in the DAC_CR register must both be written to 0.

The selected SVOS4 and SVOS5 levels add an additional startup delay when exiting from system Stop mode (see *Table 42*).

Table 42. Stop mode operation

SVOS	LPDS	Stop mode Voltage regulator operation	Wake-up Latency
SVOS3	0	**Main**	No additional wakeup time.
	1	**LP**	Voltage Regulator wakeup time from LP mode.
SVOS4 or SVOS5	x	**LP**	Voltage Regulator wakeup time from LP mode + voltage level wakeup time for SVOS4 or SVOS5 level to VOS3 level

Entering Stop mode

The Stop mode is entered according to *Section 6.7.3: Entering low-power modes*, when at least one PDDS_Dn bit n *PWR CPU control register (PWR_CPUCR)* for any domain request Stop.

Refer to *Table 43* for details on how to enter Stop mode.

If Flash memory programming is ongoing, the Stop mode entry is delayed until the memory access is finished.

If an access to a bus matrix (AXI, AHB or APB) is ongoing, the Stop mode entry is delayed until the bus matrix access is finished.

To allow peripherals having a kernel clock request to operate in Stop mode, the system must use SVOS3 level.

Note: Use a DSB instruction to ensure that outstanding memory transactions complete before entering stop mode.

Before entering Stop mode, the software must ensure that VOS0 s not active.

Exiting from Stop mode

The Stop mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 43* for more details on how to exit from Stop mode.

When exiting from Stop mode, the system clock, D3 domain bus matrix clocks and voltage scaling are reset.

STOPF status flag in *PWR CPU control register (PWR_CPUCR)* indicates that the system has exited from Stop mode (see *Table 37*).

Table 43. Stop mode

Stop mode	Description
Mode entry	– When the CPU is in CStop mode and there is no active EXTI Wakeup source and Run_D3 = 0. – At least one PDDS_Dn bit for any domain select Stop.
Mode exit	– On a EXTI Wakeup.
Wakeup latency	System oscillator startup (when disabled). + EXTI and RCC wakeup synchronization. + Voltage Scaling refer to *Table 42* (see *Section 6.6.2: Voltage scaling*)

I/O states in Stop mode

I/O pin configuration remain unchanged in Stop mode.

6.7.9 DStandby mode

Like DStop mode, DStandby mode is based on the CPU subsystem CStop mode. However the domain V_{CORE} supply is powered off. A domain enters DStandby mode only when the CPU subsystem is in CStop mode if peripherals are allocated in the domain

A domain enters DStandby mode only when the CPU subsystem is in CStop mode if peripherals are allocated in the domain and the PDDS_Dn bit in *PWR CPU control register (PWR_CPUCR)* for the domain is configured accordingly. In DStandby mode, the domain is powered down and the domain RAM and register contents are lost.

Entering DStandby mode

The DStandby mode is entered according to *Section 6.7.3: Entering low-power modes*, when the PDDS_Dn bit in *PWR CPU control register (PWR_CPUCR)* for the Dn domain selects Standby mode.

Refer to *Table 44* for details on how to enter DStandby mode.

If Flash memory programming is ongoing, the DStandby mode entry is delayed until the memory access is finished.

If an access to the domain bus matrix is ongoing, the DStandby mode entry is delayed until the domain bus matrix access is finished.

Note: When the CPU sets the PDDS_D2 bit to select Standby mode, the D2 domain enters DStandby mode (the CPU has no allocated peripherals in the D2 domain).

Exiting from DStandby mode

The DStandby mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 44* for more details on how to exit from DStandby mode.

Note: When the D2 domain is in DStandby mode and the CPU sets the domain PDDS_D2 bit to select Stop mode, the D2 domain remains in DStandby mode. The D2 domain will only exit DStandby when the CPU allocates a peripheral in the D2 domain.

When exiting from DStandby mode, the domain CPU and peripherals are reset. However the state of the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling depends on the system mode:

- When the system did not enter Stop mode, the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling are the same as when entering DStandby mode.
- When the system has entered Stop or Standby mode, the CPU subsystem clocks, domain(s) bus matrix clocks and voltage scaling are reset.

When the D2 domain exits from DStandby mode due to the CPU subsystem (i.e when allocating a first peripheral or when peripherals are allocated in the D2 domain and the CPU subsystem exits from CStop mode), the CPU shall verify that the domain has exited from DStandby mode. To ensure correct operation, it is recommended to follow the sequence below:

1. First check that the domain bus matrix clock is available. The domain bus matrix clock state can be checked in RCC_CR register:
   – When RCC DnCKRDY = 0, the domain bus matrix clock is stalled.
   – If RCC DnCKRDY = 1, the domain bus matrix clock is enabled.
2. Then wait for the domain has exited from DStandby mode. To do this, check the SBF_Dn flag in *PWR CPU control register (PWR_CPUCR)*. The domain is powered and can be accessed only when SBF_Dn is cleared. Below an example of code:

```
Loop
write PWR SBF_Dn = 0 ; try to clear bit.
read PWR SBF_Dn
While 1 ==> loop
```

Table 44. DStandby mode

DStandby mode	Description
Mode entry	– The domain CPU subsystem enters CStop. – The CPU subsystem has an allocated peripheral in D2 domain and enters CStop. – The CPU subsystem deallocated its last peripheral in the D2 domain. – The PDDS_Dn bits for the domain select Standby mode. – All WKUPF bits in Power Control/Status register (PWR_WKUPFR) are cleared.
Mode exit	– The CPU subsystem exits from CStop mode (see *Table 39*) – The CPU subsystem has an allocated peripheral in the D2 domain and exits from CStop mode (see *Table 39*) – The CPU subsystem allocates a first peripheral in the D2 domain.
Wakeup latency	EXTI and RCC wakeup synchronization. + Domain power up and reset. (see *Section 8.4.7: Power-on and wakeup sequences*)

6.7.10 Standby mode

The Standby mode allows achieving the lowest power consumption. Like Stop mode, it is based on CPU subsystem CStop mode. However the V_{CORE} supply regulator is powered off.

The system D3 domain enters Standby mode only when the D1 and D2 domain are in DStandby. When the system D3 domain enters Standby mode, the voltage regulator is disabled. The complete V_{CORE} domain is consequently powered off. The PLLs, HSI oscillator, CSI oscillator, HSI48 and the HSE oscillator are also switched off. SRAM and register contents are lost except for backup domain registers (RTC registers, RTC backup register and backup RAM), and Standby circuitry (see *Section 6.4.4: Backup domain*).

In system Standby mode, the following features can be selected by programming individual control bits:

- Independent watchdog (IWDG)

  The IWDG is started by programming its Key register or by hardware option. Once started, it cannot be stopped except by a reset (see *Section 45.3* in *Section 45: Independent watchdog (IWDG)*.
- Real-time clock (RTC)

  This is configured via the RTCEN bit in the backup domain control register (RCC_BDCR).
- Internal RC oscillator (LSI RC)

  This is configured by the LSION bit in the Control/status register (RCC_CSR).
- External 32.768 kHz oscillator (LSE OSC)

  This is configured by the LSEON bit in the backup domain control register (RCC_BDCR).

Entering Standby mode

The Standby mode is entered according to *Section 6.7.3: Entering low-power modes*, when all PDDS_Dn bits in *PWR CPU control register (PWR_CPUCR)* for all domains request Standby.

Refer to *Table 46* for more details on how to enter to Standby mode.

Note: Before entering Standby mode, the software must ensure that VOS0 is not active.

Exiting from Standby mode

The Standby mode is exited according to *Section 6.7.4: Exiting from low-power modes*.

Refer to *Table 46* for more details on how to exit from Standby mode.

The system exits from Standby mode when an external Reset (NRST pin), an IWDG Reset, a WKUP pin event, a RTC alarm, a tamper event, or a time stamp event is detected. All registers are reset after waking up from Standby except for power control and status registers (*PWR control register 2 (PWR_CR2)*, *PWR control register 3 (PWR_CR3)*), SBF bit in *PWR CPU control register (PWR_CPUCR)*, *PWR wakeup flag register (PWR_WKUPFR)*, and *PWR wakeup enable and polarity register (PWR_WKUPEPR)*.

After waking up from Standby mode, the program execution restarts in the same way as after a system reset (boot option sampling, boot vector reset fetched, etc.). The SBF status flags in *PWR CPU control register (PWR_CPUCR)* registers indicate from which mode the system has exited (see *Table 45*).

Table 45. Standby and Stop flags

SBF_D2	SBF_D1	SBF	STOPF	Description
0	1	0	0	D1 domain exits from DStandby while system stayed in Run
0	1	0	1	D1 domain exits from DStandby, while system has been in or exits from Stop
1	0	0	0	D2 domain exits from DStandby while system stayed in Run
1	0	0	1	D2 domain exits from DStandby while system has been in or exits from Stop
1	1	0	0	D1 and D2 domain exit from DStandby while the system remains in Run mode
1	1	0	1	D1 and D2 domain exit from DStandby while the system is in Stop mode or is exiting this mode.
0	0	0	1	System has been in or exits from Stop
0(1)	0(1)	1	0	System exits from Standby

1. When exiting from Standby the SBF_D1 and SBF_D2 reflect the reset value

Table 46. Standby mode

Standby mode	Description
Mode entry	– The CPU subsystem is in CStop mode, and there is no active EXTI Wakeup source and RUN_D3 = 0. – All PDDS_Dn bits for all domains select Standby. – All WKUPF bits in Power Control/Status register (PWR_WKUPFR) are cleared.
Mode exit	– WKUP pins rising or falling edge, RTC alarm (Alarm A and Alarm B), RTC wakeup, tamper event, time stamp event, external reset in NRST pin, IWDG reset.
Wakeup latency	System reset phase (see *Section 8.4.2: System reset*)

I/O states in Standby mode

In Standby mode, all I/O pins are high impedance without pull, except for:

- Reset pad (still available)
- RTC_AF1 pin if configured for tamper, time stamp, RTC Alarm out, or RTC clock calibration out
- WKUP pins (if enabled). The WKUP pin pull configuration can be defined through WKUPPUPD register bits in *PWR wakeup enable and polarity register (PWR_WKUPEPR)*.

6.7.11 Monitoring low-power modes

The devices feature state monitoring pins to monitor the CPU and Domain state transition to low-power mode (refer to *Table 47* for the list of pins and their description). The GPIO pin corresponding to each monitoring signal has to be programmed in alternate function mode.

This feature is not available in Standby mode since these I/O pins are switched to high impedance. It is available only on devices revision V.

Table 47. Low-power modes monitoring pin overview

Power state monitoring pins	Description
CSLEEP	Sleeping CPU state
CDSLEEP	Deepsleep CPU state
DxPWREN	Domain (Dx, x= 1 or 2) power enabled

The values of the monitoring pins reflect the state of the CPU and domains. Refer to *Table 48*. for the GPIO state depending on CPU and domain state.

Table 48. GPIO state according to CPU and domain state

Domain DxPWREN	CPU		CPU power state	Domainx power state
	CSLEEP	CDSLEEP		
1	0	0	CPU in Run mode	DRun mode
1	1	0	CPU in Sleep mode	
1	0	1	CPU in Run mode	
1	1	1	CPU in Deepsleep mode	DStop mode
0	-	-	-(1)	DStandby mode

1. The full domain is in power off state and the CPU is powered off.

6.8 PWR register description

The PWR registers can be accessed in word, half-word and byte format, unless otherwise specified.

6.8.1 PWR control register 1 (PWR_CR1)

Address offset: 0x000

Reset value: 0xF000 C000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ALS		AVDEN
													rw	rw	rw

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SVOS		Res.	Res.	Res.	Res.	FLPS	DBP	PLS			PVDE	Res.	Res.	Res.	LPDS
rw	rw					rw	rw	rw	rw	rw	rw				rw

Bits 31:19 Reserved, must be kept at reset value.

Bits 18:17 **ALS:** Analog voltage detector level selection
These bits select the voltage threshold detected by the AVD.
00: 1.7 V
01: 2.1 V
10: 2.5 V
11: 2.8 V

Bit 16 **AVDEN:** Peripheral voltage monitor on V_{DDA} enable
0: Peripheral voltage monitor on V_{DDA} disabled.
1: Peripheral voltage monitor on V_{DDA} enabled

Bits 15:14 **SVOS:** System Stop mode voltage scaling selection
These bits control the V_{CORE} voltage level in system Stop mode, to obtain the best trade-off between power consumption and performance.
00: Reserved
01: SVOS5 Scale 5
10: SVOS4 Scale 4
11: SVOS3 Scale 3 (default)

Bits 13:10 Reserved, must be kept at reset value.

Bit 9 **FLPS:** Flash low-power mode in DStop mode
This bit allows to obtain the best trade-off between low-power consumption and restart time when exiting from DStop mode.
When it is set, the Flash memory enters low-power mode when D1 domain is in DStop mode.
0: Flash memory remains in normal mode when D1 domain enters DStop (quick restart time).
1: Flash memory enters low-power mode when D1 domain enters DStop mode (low-power consumption).

Bit 8 **DBP:** Disable backup domain write protection

In reset state, the RCC_BDCR register, the RTC registers (including the backup registers), BREN and MONEN bits in PWR_CR2 register, are protected against parasitic write access. This bit must be set to enable write access to these registers.

0: Access to RTC, RTC Backup registers and backup SRAM disabled

1: Access to RTC, RTC Backup registers and backup SRAM enabled

Bits 7:5 **PLS:** Programmable voltage detector level selection

These bits select the voltage threshold detected by the PVD.

000: 1.95 V

001: 2.1 V

010: 2.25 V

011: 2.4 V

100: 2.55 V

101: 2.7 V

110: 2.85 V

111: External voltage level on PVD_IN pin, compared to internal V_{REFINT} level.

Note: Refer to Section "Electrical characteristics" of the product datasheet for more details.

Bit 4 **PVDE:** Programmable voltage detector enable

0: Programmable voltage detector disabled.

1: Programmable voltage detector enabled

Bits 3:1 Reserved, must be kept at reset value.

Bit 0 **LPDS:** Low-power Deepsleep with SVOS3 (SVOS4 and SVOS5 always use low-power, regardless of the setting of this bit)

0: Voltage regulator in Main mode (MR) when SVOS3 is selected for Stop mode

1: Voltage regulator in Low-power mode (LPR) when SVOS3 is selected for Stop mode

6.8.2 PWR control status register 1 (PWR_CSR1)

Address offset: 0x004

Reset value: 0x0000 4000.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	AVDO
															r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ACTVOS		ACTVOSRDY	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	PVDO	Res.	Res.	Res.	Res.
r		r									r				

Bits 31:17 Reserved, must be kept at reset value.

Bit 16 **AVDO**: Analog voltage detector output on V_{DDA}

This bit is set and cleared by hardware. It is valid only if AVD on V_{DDA} is enabled by the AVDEN bit.

0: V_{DDA} is equal or higher than the AVD threshold selected with the ALS[2:0] bits.

1: V_{DDA} is lower than the AVD threshold selected with the ALS[2:0] bits

Note: Since the AVD is disabled in Standby mode, this bit is equal to 0 after Standby or reset until the AVDEN bit is set.

Bits 15:14 **ACTVOS**: VOS currently applied for V_{CORE} voltage scaling selection.

These bits reflect the last VOS value applied to the voltage regulator.

Bit 13 **ACTVOSRDY:** Voltage levels ready bit for currently used VOS

This bit is forced by hardware to 1 when the Bypass mode is selected in PWR control register 3 (PWR_CR3).

0: Voltage level invalid, above or below current VOS selected level.

1: Voltage level valid, at current VOS selected level.

Bits 12:5 Reserved, must be kept at reset value.

Bit 4 **PVDO**: Programmable voltage detect output

This bit is set and cleared by hardware. It is valid only if the PVD has been enabled by the PVDE bit.

0: V_{DD} or PVD_IN voltage is equal or higher than the PVD threshold selected through the PLS[2:0] bits.

1: V_{DD} or PVD_IN voltage is lower than the PVD threshold selected through the PLS[2:0] bits.

Note: since the PVD is disabled in Standby mode, this bit is equal to 0 after Standby or reset until the PVDE bit is set.

Bits 3:0 Reserved, must be kept at reset value.

6.8.3 PWR control register 2 (PWR_CR2)

Address offset: 0x008

Reset value: 0x0000 0000

This register is not reset by wakeup from Standby mode, RESET signal and V_{DD} POR. It is only reset by V_{SW} POR and VSWRST reset.

This register shall not be accessed when VSWRST bit in RCC_BDCR register resets the V_{SW} domain.

After reset, PWR_CR2 register is write-protected. Prior to modifying its content, the DBP bit in PWR_CR1 register must be set to disable the write protection.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TEMPH	TEMPL	VBATH	VBATL	Res.	Res.	Res.	BRRDY
								r	r	r	r				r
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	MONEN	Res.	Res.	Res.	BREN
											rw				rw

Bits 31:24 Reserved, must be kept at reset value.

Bit 23 **TEMPH**: Temperature level monitoring versus high threshold
0: Temperature below high threshold level.
1: Temperature equal or above high threshold level.

Bit 22 **TEMPL**: Temperature level monitoring versus low threshold
0: Temperature above low threshold level.
1: Temperature equal or below low threshold level.

Bit 21 **VBATH**: V_{BAT} level monitoring versus high threshold
0: V_{BAT} level below high threshold level.
1: V_{BAT} level equal or above high threshold level.

Bit 20 **VBATL**: V_{BAT} level monitoring versus low threshold
0: V_{BAT} level above low threshold level.
1: V_{BAT} level equal or below low threshold level.

Bits 19:17 Reserved, must be kept at reset value.

Bit 16 **BRRDY**: Backup regulator ready
This bit is set by hardware to indicate that the Backup regulator is ready.
0: Backup regulator not ready.
1: Backup regulator ready.

Bits 15:5 Reserved, must be kept at reset value.

Bit 4 **MONEN:** V_{BAT} and temperature monitoring enable
When set, the V_{BAT} supply and temperature monitoring is enabled.
0: V_{BAT} and temperature monitoring disabled.
1: V_{BAT} and temperature monitoring enabled.
Note: V_{BAT} and temperature monitoring are only available when the backup regulator is enabled (BREN bit set to 1).

Bits 3:1 Reserved, must be kept at reset value.

Bit 0 **BREN:** Backup regulator enable
When set, the Backup regulator (used to maintain the backup RAM content in Standby and V_{BAT} modes) is enabled.
If BREN is reset, the backup regulator is switched off. The backup RAM can still be used in Run and Stop modes. However, its content will be lost in Standby and V_{BAT} modes.
If BREN is set, the application must wait till the Backup Regulator Ready flag (BRRDY) is set to indicate that the data written into the SRAM will be maintained in Standby and V_{BAT} modes.
0: Backup regulator disabled.
1: Backup regulator enabled.

6.8.4 PWR control register 3 (PWR_CR3)

Address offset: 0x00C

Reset value: 0x0000 0006 (rev Y)

Reset value: 0x0000 0046 (rev V)

This register is reset only by POR. It is not reset by wakeup from Standby mode and by the RESET pad.

The lower byte of this register is written once after POR and shall be written before changing VOS level or ck_sys clock frequency. No limitation applies to the upper bytes.

Programming data corresponding to an invalid combination of LDOEN and BYPASS bits (see *Table 34*) will be ignored: data will not be written, the written-once mechanism will lock the register and any further write access will be ignored. The default supply configuration will be kept and the ACTVOSRDY bit in *PWR control status register 1 (PWR_CSR1)* will go on indicating invalid voltage levels. The system shall be power cycled before writing a new value.

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	USB33RDY	USBREGEN	USB33DEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
					r	rw	rw								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	VBRS	VBE	Res.	Res.	Res.	Res.	Res.	SCUEN	LDOEN	BYPASS
						rw	rw						rw	rw	rw

Bits 31:27 Reserved, must be kept at reset value.

Bit 26 **USB33RDY**: USB supply ready.
0: USB33 supply not ready.
1: USB33 supply ready.

Bit 25 **USBREGEN**: USB regulator enable.
0: USB regulator disabled.
1: USB regulator enabled.

Bit 24 **USB33DEN**: $V_{DD33USB}$ voltage level detector enable.
0: $V_{DD33USB}$ voltage level detector disabled.
1: $V_{DD33USB}$ voltage level detector enabled.

Bits 23:10 Reserved, must be kept at reset value.

Bit 9 **VBRS**: V_{BAT} charging resistor selection
0: Charge V_{BAT} through a 5 kΩ resistor.
1: Charge V_{BAT} through a 1.5 kΩ resistor.

Bit 8 **VBE**: V_{BAT} charging enable
0: V_{BAT} battery charging disabled.
1: V_{BAT} battery charging enabled.

Bits 7:3 Reserved, must be kept at reset value.

Bit 2 **SCUEN**: Supply configuration update enable
0: Supply configuration update locked.
1: Single write enabled to Supply configuration (LDOEN and BYPASS)

Bit 1 **LDOEN**: Low drop-out regulator enable
0: Low drop-out regulator disabled.
1: Low drop-out regulator enabled (default)

Bit 0 **BYPASS**: Power management unit bypass
0: Power management unit normal operation.
1: Power management unit bypassed, voltage monitoring still active.

6.8.5 PWR CPU control register (PWR_CPUCR)

This register allows controlling CPU power.

Address offset: 0x010

Reset value: 0x0000 0000

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	RUN_D3	Res.	CSSF	SBF_D2	SBF_D1	SBF	SOPFF	Res.	Res.	PDDS_D3	PDDS_D2	PDDS_D1
				rw		rw	r	r	r	r			rw	rw	rw

Bits 31:12 Reserved, must be kept at reset value.

Bit 11 **RUN_D3:** Keep system D3 domain in Run mode regardless of the CPU subsystem modes
0: D3 domain follows CPU subsystem modes.
1: D3 domain remains in Run mode regardless of CPU subsystem modes.

Bit 10 Reserved, must be kept at reset value.

Bit 9 **CSSF:** Clear Standby and Stop flags (always read as 0)
This bit is cleared to 0 by hardware.
0: No effect.
1: STOPF, SBF, SBF_D1, and SBF_D2 flags are cleared.

Bit 8 **SBF_D2:** D2 domain DStandby flag
This bit is set by hardware and cleared by any system reset or by setting the CSSF bit. Once set, this bit can be cleared only when the D2 domain is no longer in DStandby mode.
0: D2 domain has not been in DStandby mode
1: D2 domain has been in DStandby mode.

Bit 7 **SBF_D1:** D1 domain DStandby flag
This bit is set by hardware and cleared by any system reset or by setting the CSSF bit. Once set, this bit can be cleared only when the D1 domain is no longer in DStandby mode.
0: D1 domain has not been in DStandby mode
1: D1 domain has been in DStandby mode.

Bit 6 **SBF:** System Standby flag
This bit is set by hardware and cleared only by a POR (Power-on Reset) or by setting the CSSF bit
0: System has not been in Standby mode
1: System has been in Standby mode

Bit 5 **STOPF:** STOP flag
This bit is set by hardware and cleared only by any reset or by setting the CSSF bit.
0: System has not been in Stop mode
1: System has been in Stop mode

Bits 4:3 Reserved, must be kept at reset value.

Bit 2 **PDDS_D3:** System D3 domain Power Down Deepsleep.
This bit allows defining the Deepsleep mode for System D3 domain.
0: Keep Stop mode when D3 domain enters Deepsleep.
1: Allow Standby mode when D3 domain enters Deepsleep.

Bit 1 **PDDS_D2:** D2 domain Power Down Deepsleep.
This bit allows defining the Deepsleep mode for D2 domain.
0: Keep DStop mode when D2 domain enters Deepsleep.
1: Allow DStandby mode when D2 domain enters Deepsleep.

Bit 0 **PDDS_D1:** D1 domain Power Down Deepsleep selection.
This bit allows defining the Deepsleep mode for D1 domain.
0: Keep DStop mode when D1 domain enters Deepsleep.
1: Allow DStandby mode when D1 domain enters Deepsleep.

6.8.6 PWR D3 domain control register (PWR_D3CR)

This register allows controlling D3 domain power.

Address offset: 0x018

Reset value: 0x0000 4000 (Following reset VOSRDY will be read 1 by software).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
VOS		VOSRDY	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
rw		r													

Bits 31:16 Reserved, must be kept at reset value.

Bits 15:14 **VOS:** Voltage scaling selection according to performance
These bits control the V_{CORE} voltage level and allow to obtains the best trade-off between power consumption and performance:
– When increasing the performance, the voltage scaling shall be changed before increasing the system frequency.
– When decreasing performance, the system frequency shall first be decreased before changing the voltage scaling.
00: Reserved (Scale 3 selected).
01: Scale 3 (default)
10: Scale 2
11: Scale 1

Bit 13 **VOSRDY:** VOS Ready bit for V_{CORE} voltage scaling output selection.
This bit is forced by hardware to 1 when the Bypass mode is selected in PWR control register 3 (PWR_CR3).
0: Not ready, voltage level below VOS selected level.
1: Ready, voltage level at or above VOS selected level.

Bits 12:0 Reserved, must be kept at reset value.

6.8.7 PWR wakeup clear register (PWR_WKUPCR)

Address offset: 0x020

Reset value: 0x0000 0000 (reset only by system reset, not reset by wakeup from Standby mode)

5 wait states are required when writing this register (when clearing a WKUPF bit in PWR_WKUPFR, the AHB write access will complete after the WKUPF has been cleared).

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	WKUPC6	WKUPC5	WKUPC4	WKUPC3	WKUPC2	WKUPC1
										rc_w1	rc_w1	rc_w1	rc_w1	rc_w1	rc_w1

Bits 31:6 Reserved, always read as 0.

Bits 5:0 **WKUPCn:Clear Wakeup pin flag for WKUPn.**

These bits are always read as 0.
0: No effect
1: Writing 1 clears the WKUPFn Wakeup pin flag (bit is cleared to 0 by hardware)

6.8.8 PWR wakeup flag register (PWR_WKUPFR)

Address offset: 0x024

Reset value: 0x0000 0000 (reset only by system reset, not reset by wakeup from Standby mode)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	WKUPF6	WKUPF5	WKUPF4	WKUPF3	WKUPF2	WKUPF1
										r	r	r	r	r	r

Bits 31:6 Reserved, must be kept at reset value.

Bits 5:0 **WKUPn:** Wakeup pin WKUPn flag.

This bit is set by hardware and cleared only by a Reset pin or by setting the WKUPCn bit in the *PWR wakeup clear register (PWR_WKUPCR)*.
0: No wakeup event occurred
1: A wakeup event was received from WKUPn pin

6.8.9 PWR wakeup enable and polarity register (PWR_WKUPEPR)

Address offset: 0x028

Reset value: 0x0000 0000 (reset only by system reset, not reset by wakeup from Standby mode)

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Res.	Res.	Res.	Res.	WKUPPUPD6		WKUPPUPD5		WKUPPUPD4		WKUPPUPD3		WKUPPUPD2		WKUPPUPD1	
				rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw	rw
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Res.	Res.	WKUPP6	WKUPP5	WKUPP4	WKUPP3	WKUPP2	WKUPP1	Res.	Res.	WKUPEN6	WKUPEN5	WKUPEN4	WKUPEN3	WKUPEN2	WKUPEN1
		rw	rw	rw	rw	rw	rw			rw	rw	rw	rw	rw	rw

Bits 31:28 Reserved, must be kept at reset value.

Bits 27:16 **WKUPPUPD[truncate(n/2)-7)**: Wakeup pin pull configuration for WKUP(truncate(n/2)-7)

These bits define the I/O pad pull configuration used when WKUPEN(truncate(n/2)-7) = 1. The associated GPIO port pull configuration shall be set to the same value or to ‘00’.

The Wakeup pin pull configuration is kept in Standby mode.

00: No pull-up

01: Pull-up

10: Pull-down

11: Reserved

Bits 15:14 Reserved, must be kept at reset value.

Bits 13:8 **WKUPPn-7**: Wakeup pin polarity bit for WKUPn-7

These bits define the polarity used for event detection on WKUPn-7 external wakeup pin.

0: Detection on high level (rising edge)

1: Detection on low level (falling edge)

Bits 7:6 Reserved, must be kept at reset value.

Bits 5:0 **WKUPENn+1**: Enable Wakeup Pin WKUPn

Each bit is set and cleared by software.

0: An event on WKUPn pin does not wakeup the system from Standby mode.

1: A rising or falling edge on WKUPn+1 pin wakes-up the system from Standby mode.

Note: An additional wakeup event is detected if WKUPn pin is enabled (by setting the WKUPENn bit) when WKUPn pin level is already high when WKUPPn selects rising edge, or low when WKUPPn selects falling edge.

6.8.10 PWR register map

Table 49. Power control register map and reset values

Offset	Register name	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x000	**PWR_CR1**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	ALS		AVDEN	SVOS		Res.	Res.	Res.	Res.	FLPS	DBP	PLS			PVDE	Res.	Res.	Res.	LPDS
	Reset value														0	0	0	1	1					0	0	0	0	0	0				0
0x004	**PWR_CSR1**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	AVDO	ACTVOS		ACTVOSRDY	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	PVDO	Res.	Res.	Res.	Res.
	Reset value																0	0	1	0									0				
0x008	**PWR_CR2**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	TEMPH	TEMPL	VBATH	VBATL	Res.	Res.	Res.	BRRDY	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	MONEN	Res.	Res.	Res.	BREN
	Reset value									0	0	0	0				0												0				0
0x00C	**PWR_CR3**	Res.	Res.	Res.	Res.	Res.	USB33RDY	USBREGEN	USB33DEN	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	VBRS	VBE	Res.	Res.	Res.	Res.	Res.	SCUEN	LDOEN	BYPASS
	Reset value						0	0	0															0	0						1	1	0
0x010	**PWR_CPUCR**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	RUN_D3	Res.	CSSF	SBF_D2	SBF_D1	SBF	STOPF	Res.	Res.	PDDS_D3	PDDS_D2	PDDS_D1
	Reset value																					0		0	0	0	0	0			0	0	0
0x014	**Reserved**	Reserved																															
	Reset value																																
0x018	**PWR_D3CR**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	VOS		VOSRDY	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.
	Reset value																	0	1	0													
0x020	**PWR_WKUPCR**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	WKUPC6	WKUPC5	WKUPC4	WKUPC3	WKUPC2	WKUPC1
	Reset value																											0	0	0	0	0	0
0x024	**PWR_WKUPFR**	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	Res.	WKUPF6	WKUPF5	WKUPF4	WKUPF3	WKUPF2	WKUPF1
	Reset value																											0	0	0	0	0	0
0x028	**PWR_WKUPEPR**	Res.	Res.	Res.	Res.	WKUPPUPD6		WKUPPUPD5		WKUPPUPD4		WKUPPUPD3		WKUPPUPD2		WKUPPUPD1		Res.	Res.	WKUPP6	WKUPP5	WKUPP4	WKUPP3	WKUPP2	WKUPP1	Res.	Res.	WKUPEN6	WKUPEN5	WKUPEN4	WKUPEN3	WKUPEN2	WKUPEN1
	Reset value					0	0	0	0	0	0	0	0	0	0	0	0			0	0	0	0	0	0			0	0	0	0	0	0
0x030	Reserved																																

Refer to *Section 2.3 on page 129* for the register boundary addresses.