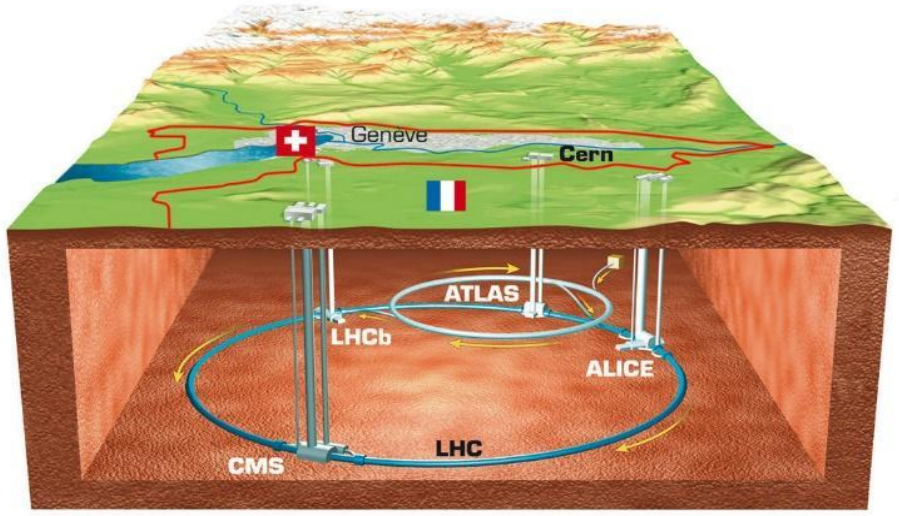
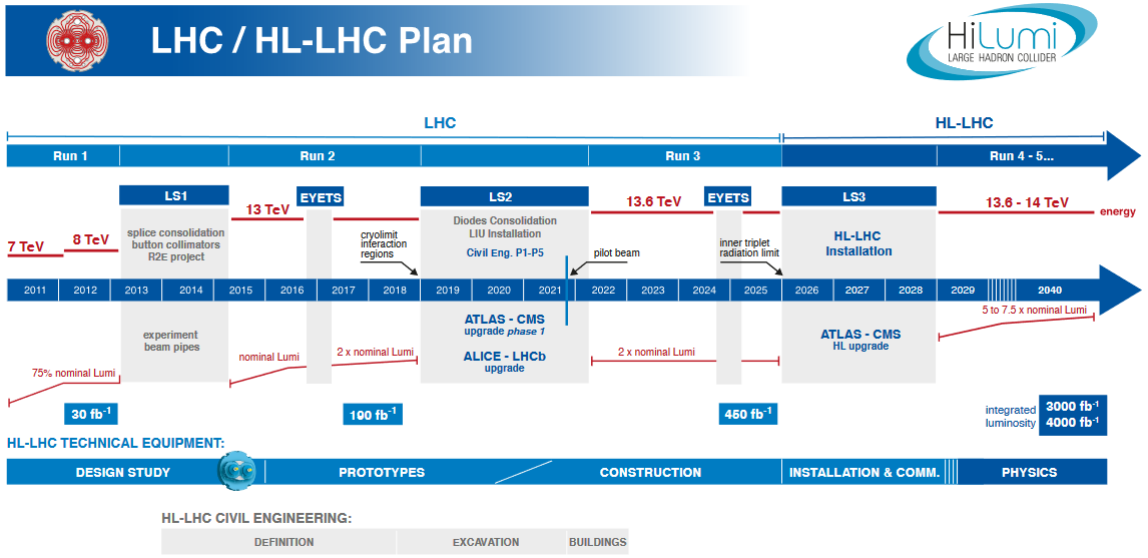
Rapid Synchronization Recovery from Single Event Effects in the Large Hadron Collider

Anatoliy Martynyuk – 8th of June, 2022

The Large Hadron Collider

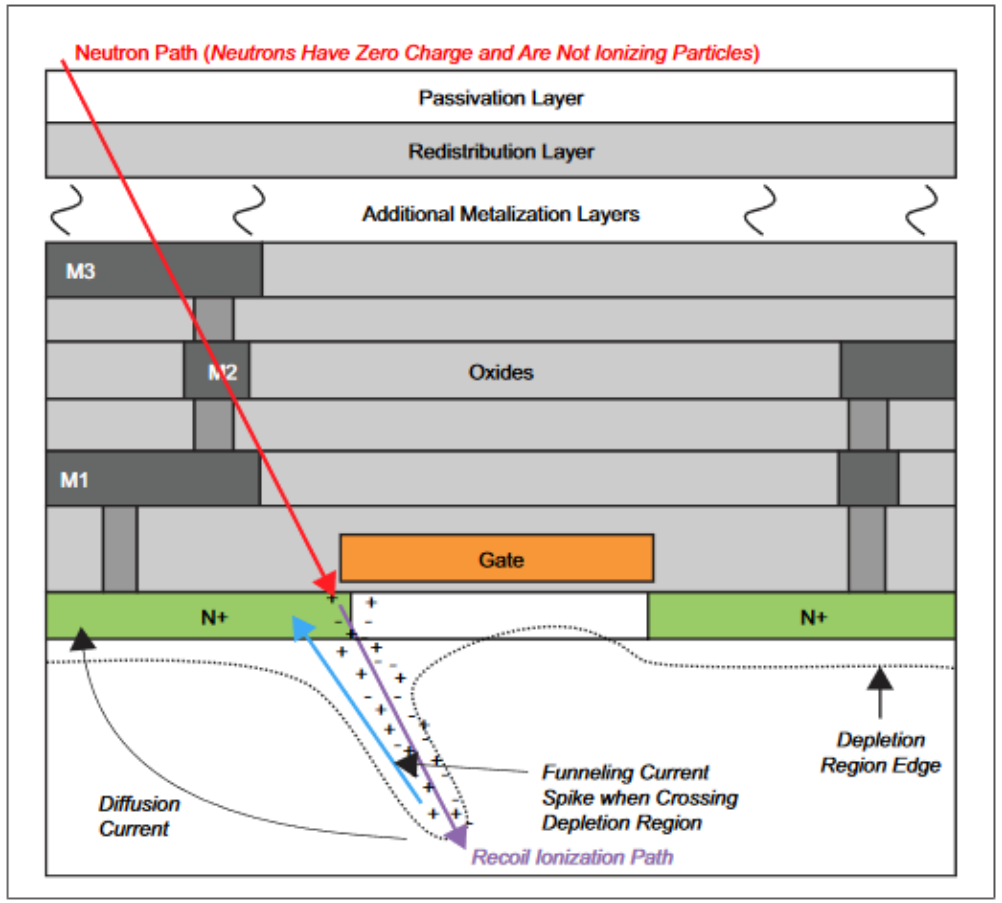
- The largest particle accelerator in the world
- Operation involves speeding subatomic particles up to near light speed, colliding them and recording the output results of the collision
- Anticipating a significant upgrade in luminosity through 2029





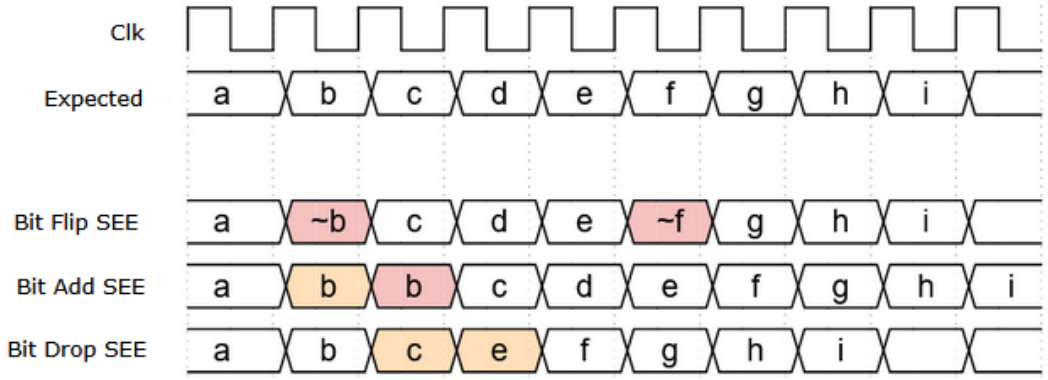
Single Event Effects: Physics

- SEEs are a consequence of subatomic particles creating charged paths resulting in current/voltage spikes
- Single Event Upset (SEU): Event occurred in memory and flipped a bit
- Single Event Transient (SET): Event occurred on a wire and triggered a glitch



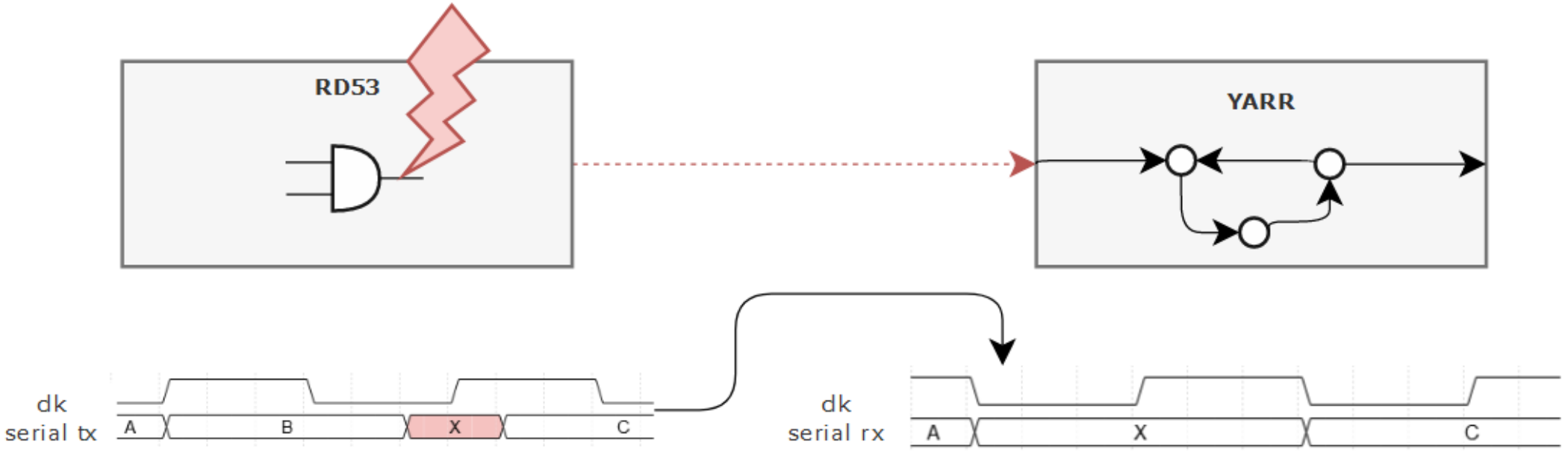
Single Event Effects: Digital Abstraction

- We can ignore how or where an SEE occurs and deal with the result of its occurrence: bit flips, bit duplication/adds and bit deletion/drops
- Bit flips are a result of memory upsets, and glitches being sampled
- Adds and drops are a result of glitches and frequency drift in the clock or in clock generating logic



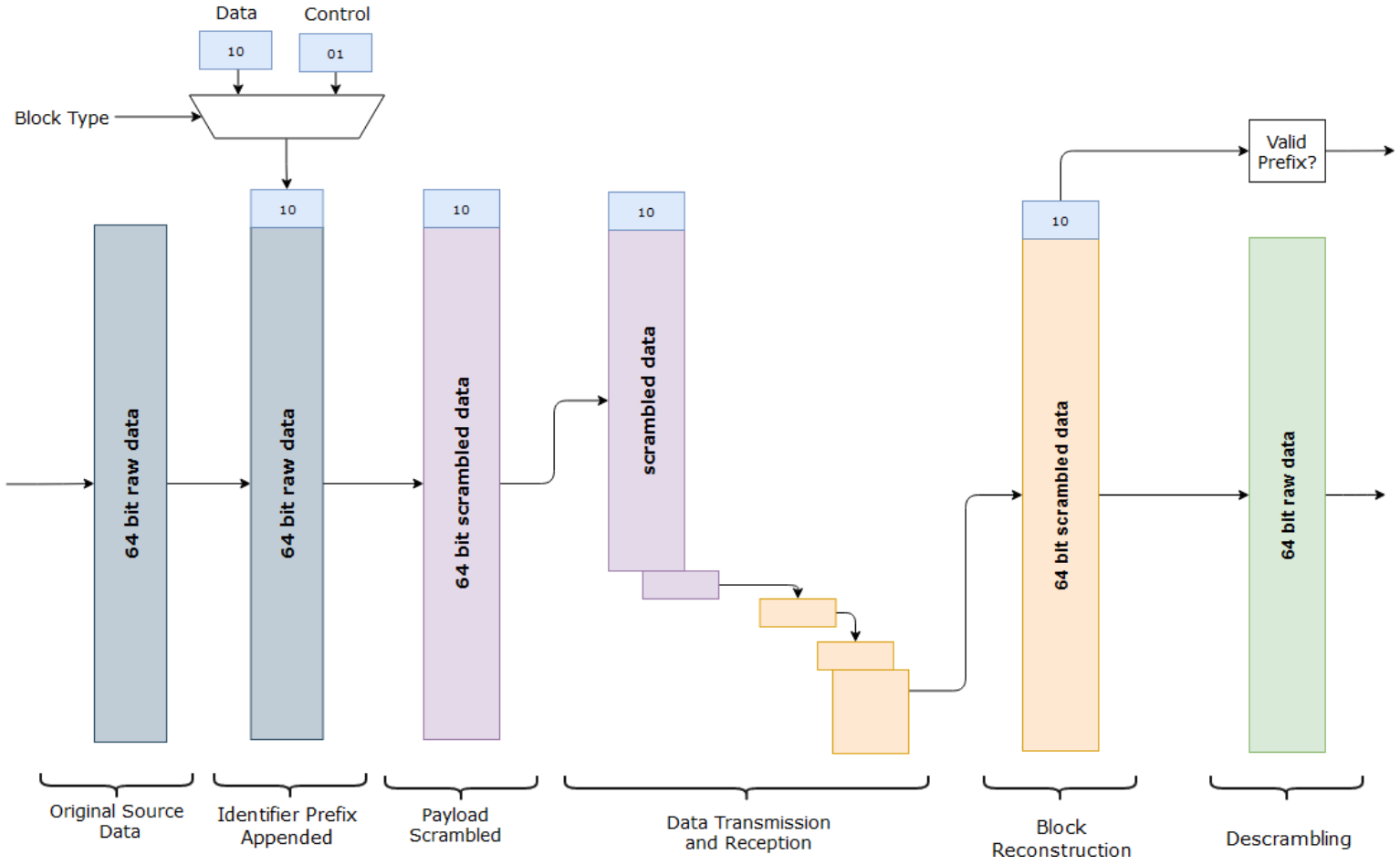
Single Event Effects: At the LHC

- RD53 Pixel Readout Chip is at the collision site and experiences high radiation
- YARR DAQ is far from radiation site and experiences effectively no radiation
- However, YARR has to deal with SEE effects passed to it by the RD53



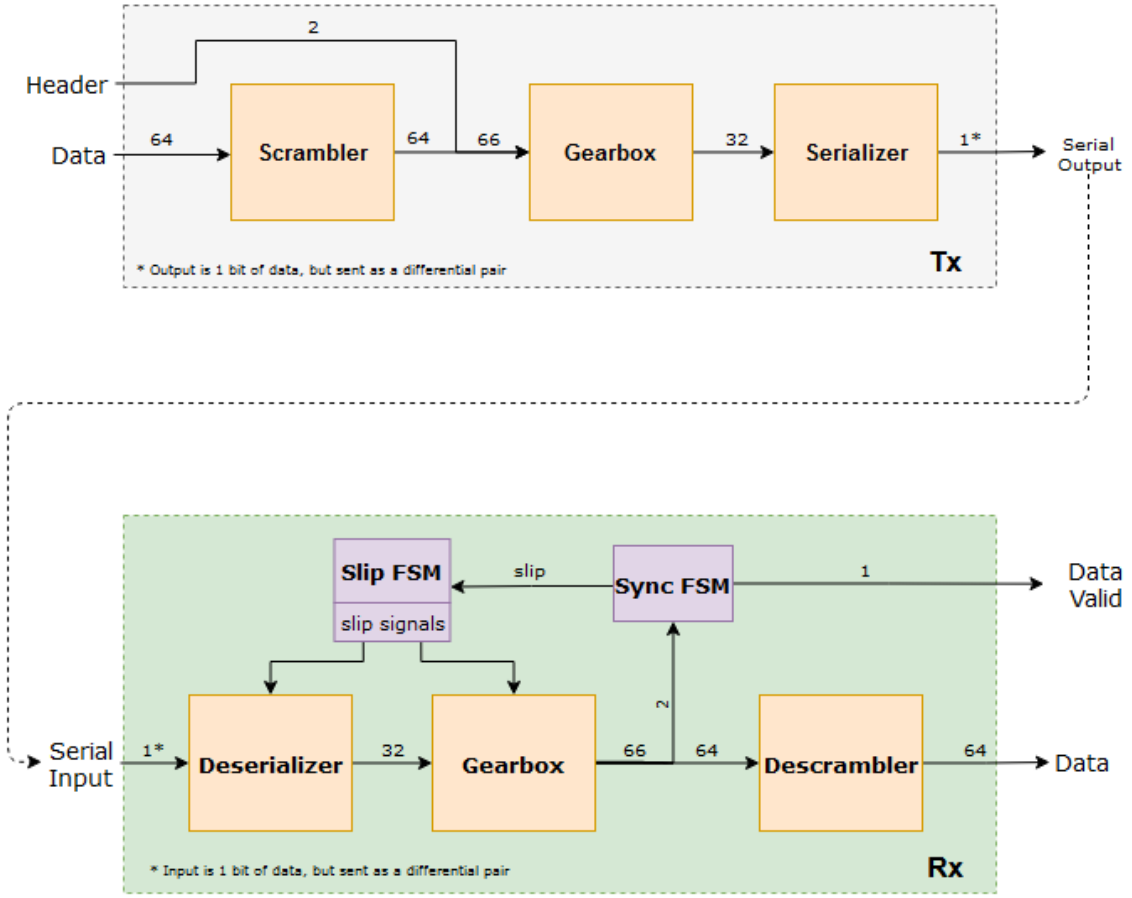
64b/66b Encoding

- Communication is done over a single differential pair
- Each block contains 64 payload bits and 2 alignment/header bits
- Protocol features:
  - Stream alignment
  - Guaranteed transition
  - Statistical DC Balancing



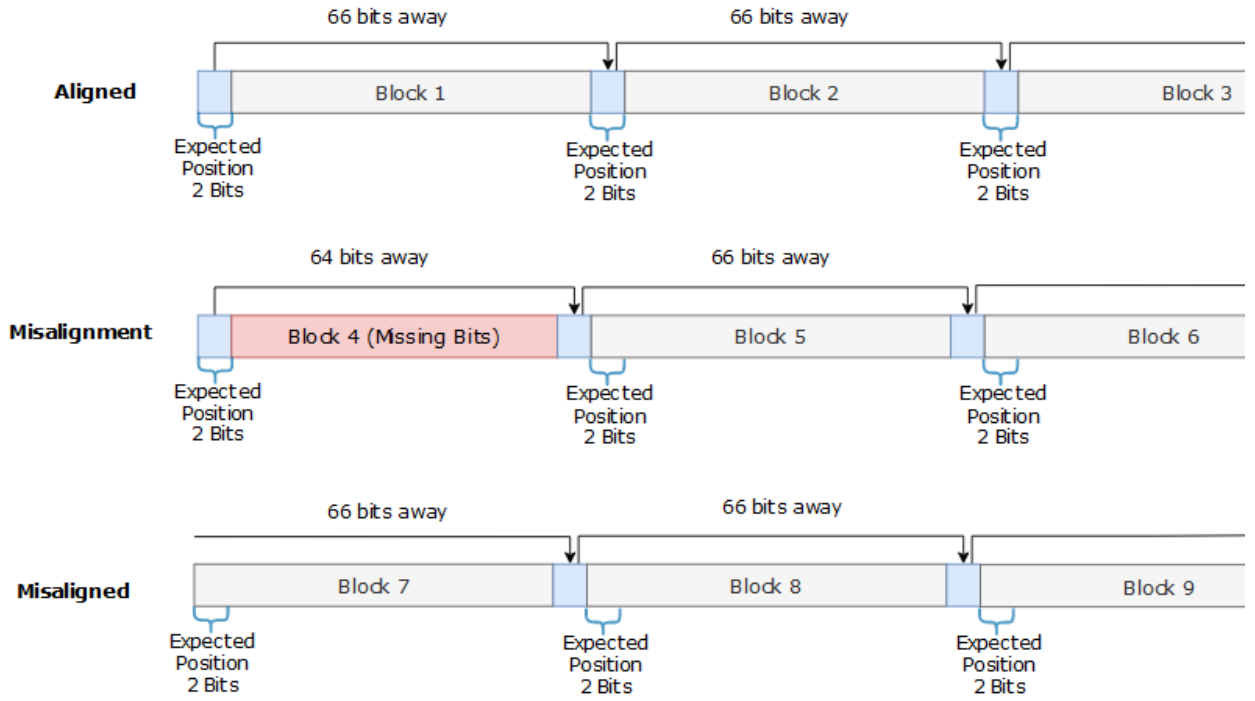
Communication Tx/Rx

- Communication hardware is responsible for the implementation of the 64b/66b protocol
- Each block in the Tx has a reverse counterpart in the Rx
- The scrambler is responsible for the data formatting features
- Gearbox transforms each 66-bit input into two 32-bit outputs



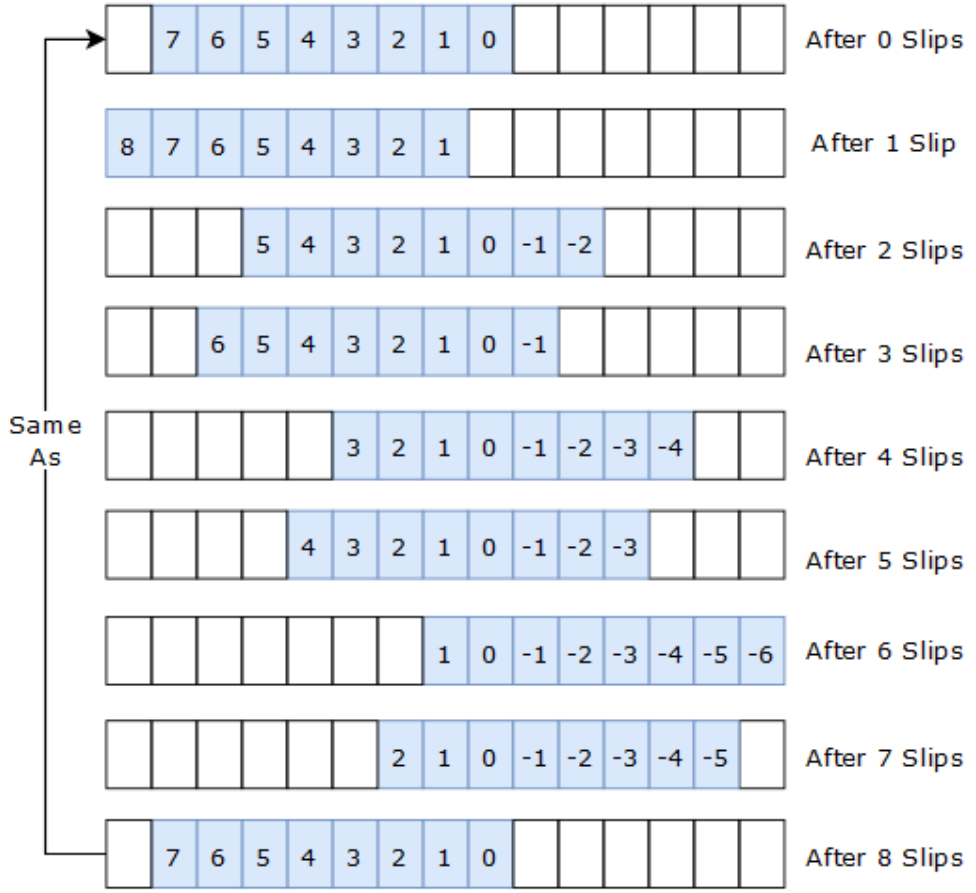
Stream Alignment

- Alignment based around stream periodicity
- YARR expects a 01 or 10 every 66 bits received and monitors the position where the bits are expected
- Once misaligned, the stream needs to be shifted to move header bits back into expected position



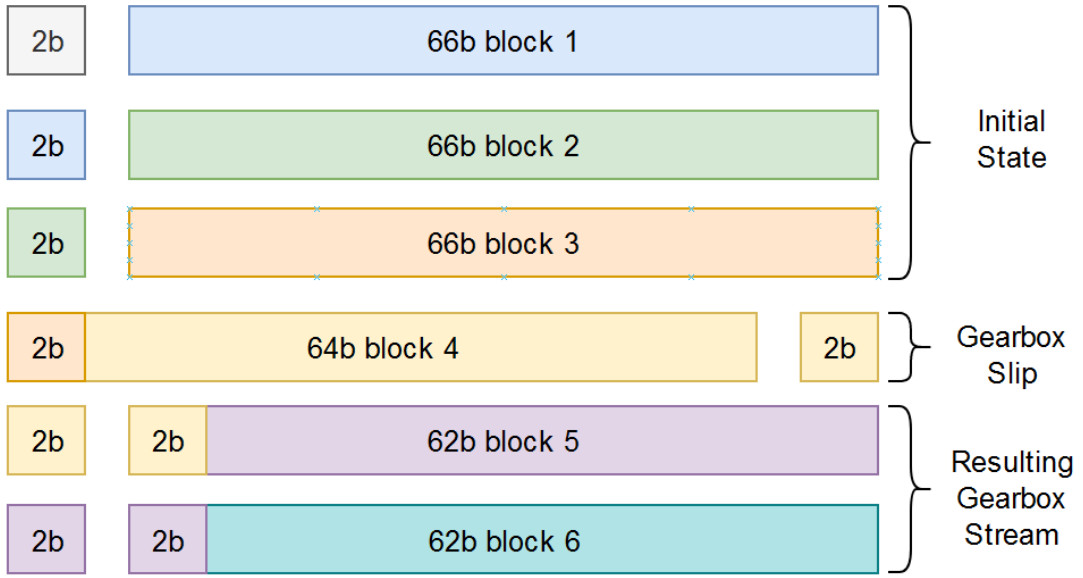
Original Scheme: Serializer Bitslip

- Serializer operates in DDR mode to keep up with 1.28 Gbps data rate
- DDR serializer utilizes bit slip module to drop and add bits
- Abstractly view as a 15-bit buffer with a selection window that snaps back after 8 “slips”



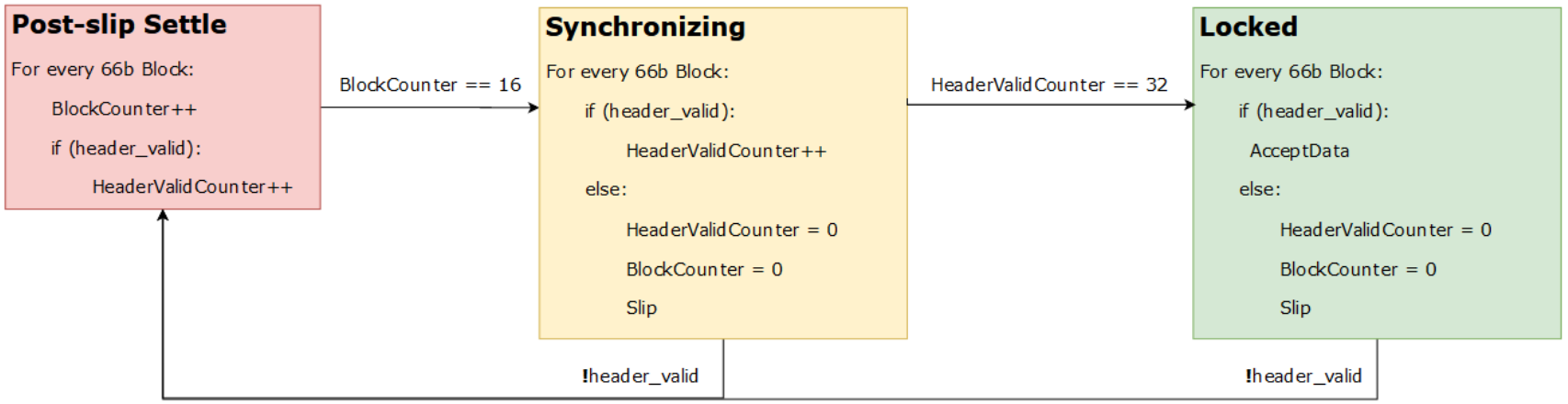
Original Scheme: Gearbox Slip

- Rx Gearbox performs 64-bit to 66-bit transformation utilizing an internal buffer
- The buffer allows the gearbox to maintain a 66-bit block as well as the bottom two bits of the previous block
- The gearbox can opt to use the two bits of the previous block, effectively shifting the data stream by 2 bits



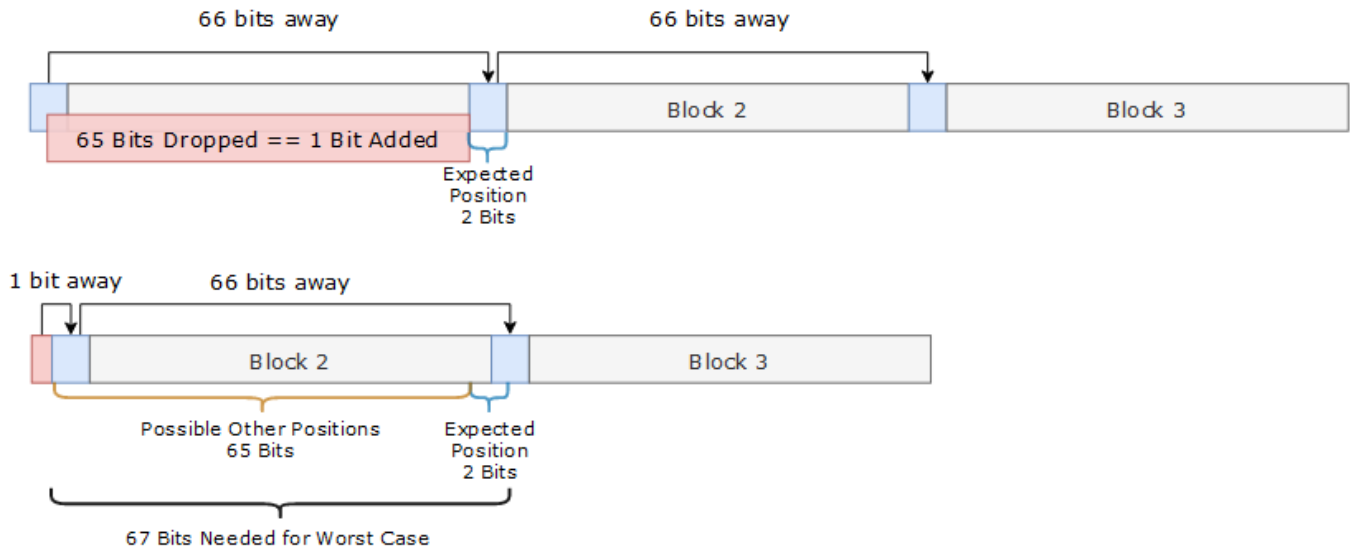
Original Scheme: Control FSM

- Synchronizing state counts a minimum of 16 consecutive valid words before the system locks on
- Any single invalid header desynchronizes and moves the FSM to the Settle state unless the FSM is already there
- Slip activates either the gearbox or serializer slip
- There are 8 serializer slips for every gearbox slip



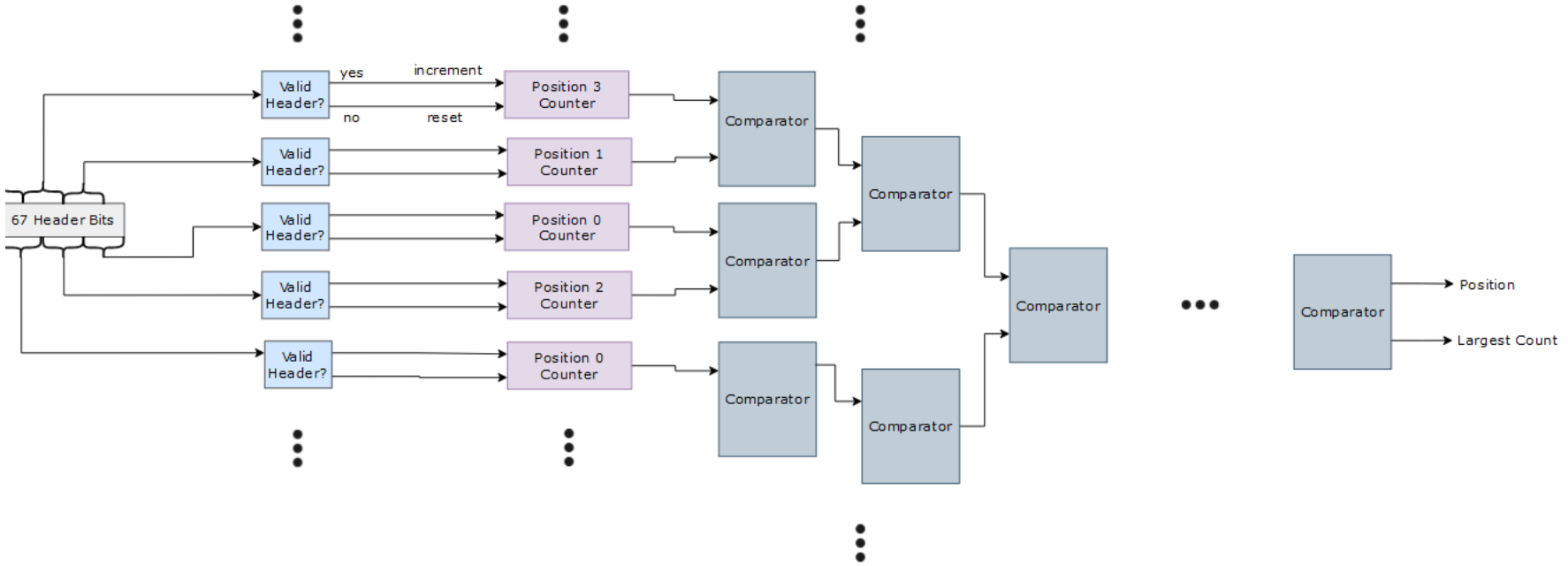
Fully Parallel (FP) Alignment

- Goal is to utilize parallelism to monitor multiple possible positions simultaneously
- By monitoring every possible position, the slip mechanisms become redundant



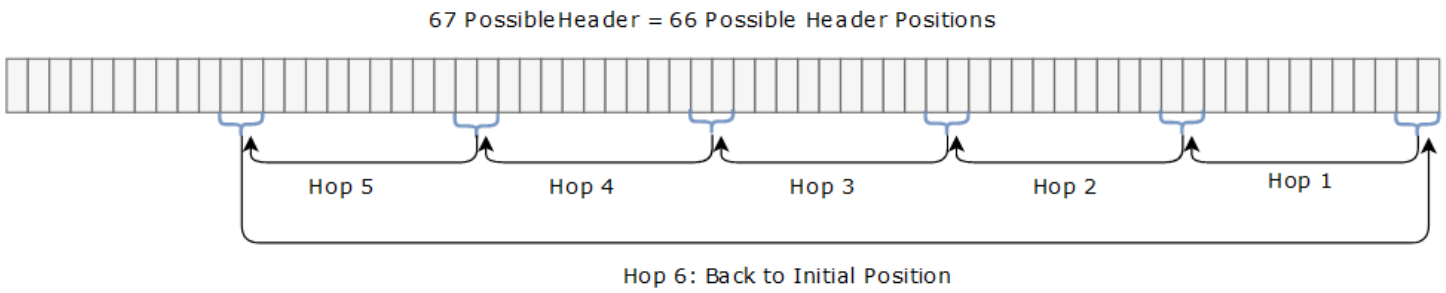
Fully Parallel (FP) Alignment

- However, evaluating every possible position is costly:
  - Combinatorial logic requires pipelining to meet timing constraints
  - Combinatorial logic and pipelining overhead demand significant FPGA resources



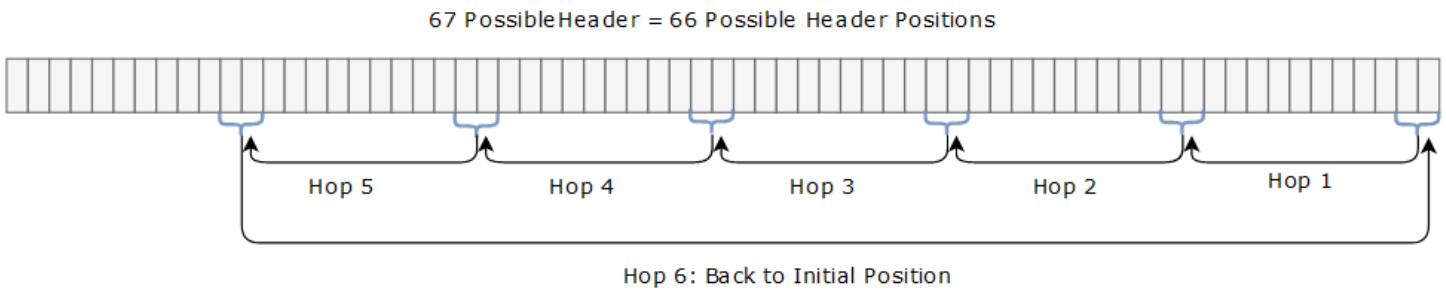
Header Seeker (HS*n*) Alignment

- HS*n* utilizes less parallelism to reduce resources and pipelining costs but aims to retain the benefits of FP
- By assigning multiple positions to an individual seeker/monitor, a small group of seekers can monitor the full 66 position range
- Seekers hop between their assigned positions whenever the position being monitored has invalid header/alignment bits.



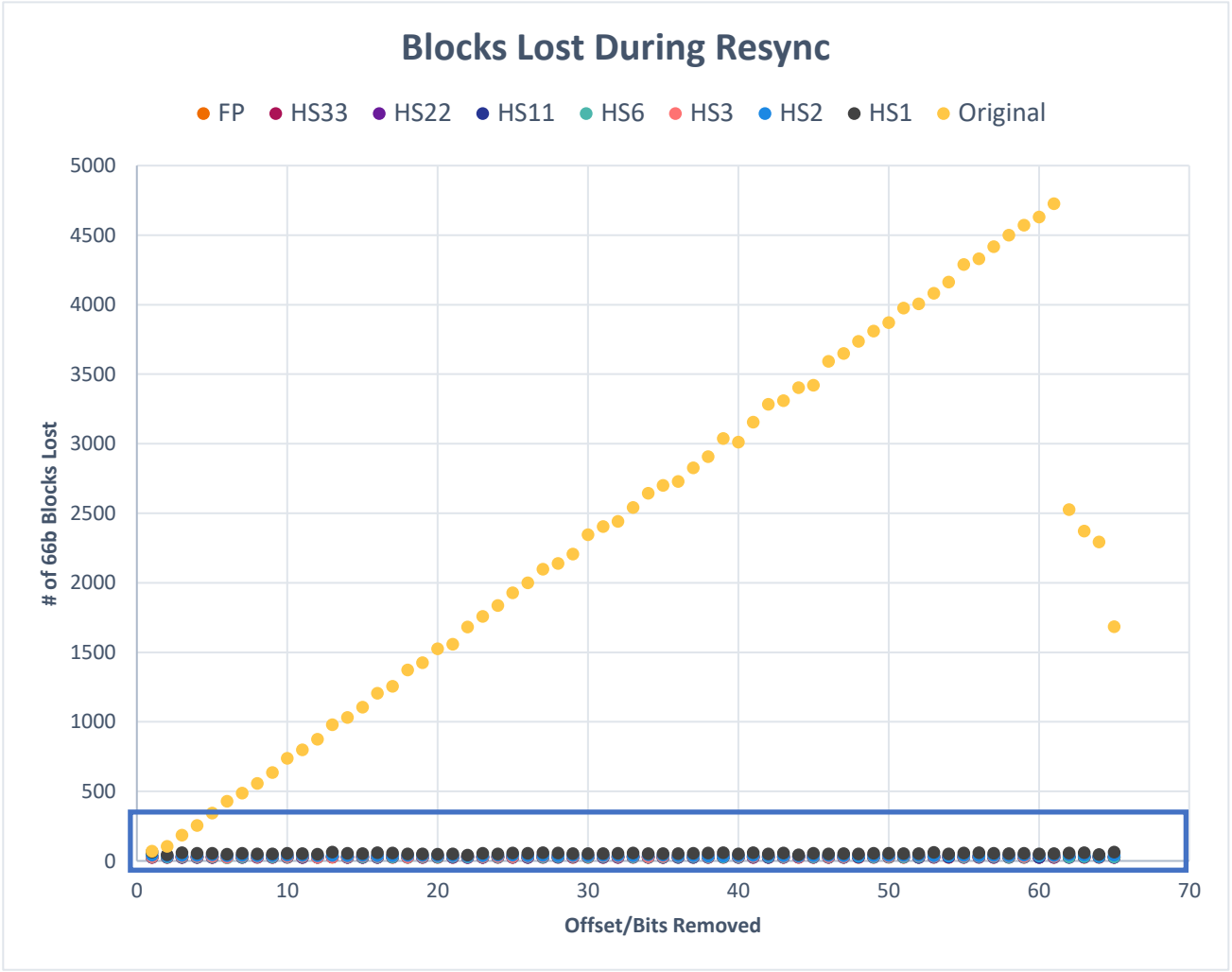
Header Seeker (HS*n*) Variants

- With 66 positions, variations with 33, 22, 11, 6, 3, 2 and 1 seeker are possible
- Seekers can do up to 8 hops per 66-bit block
- Even when one seeker is locked onto the correct header, the remaining seekers continue to rotate through their assigned positions



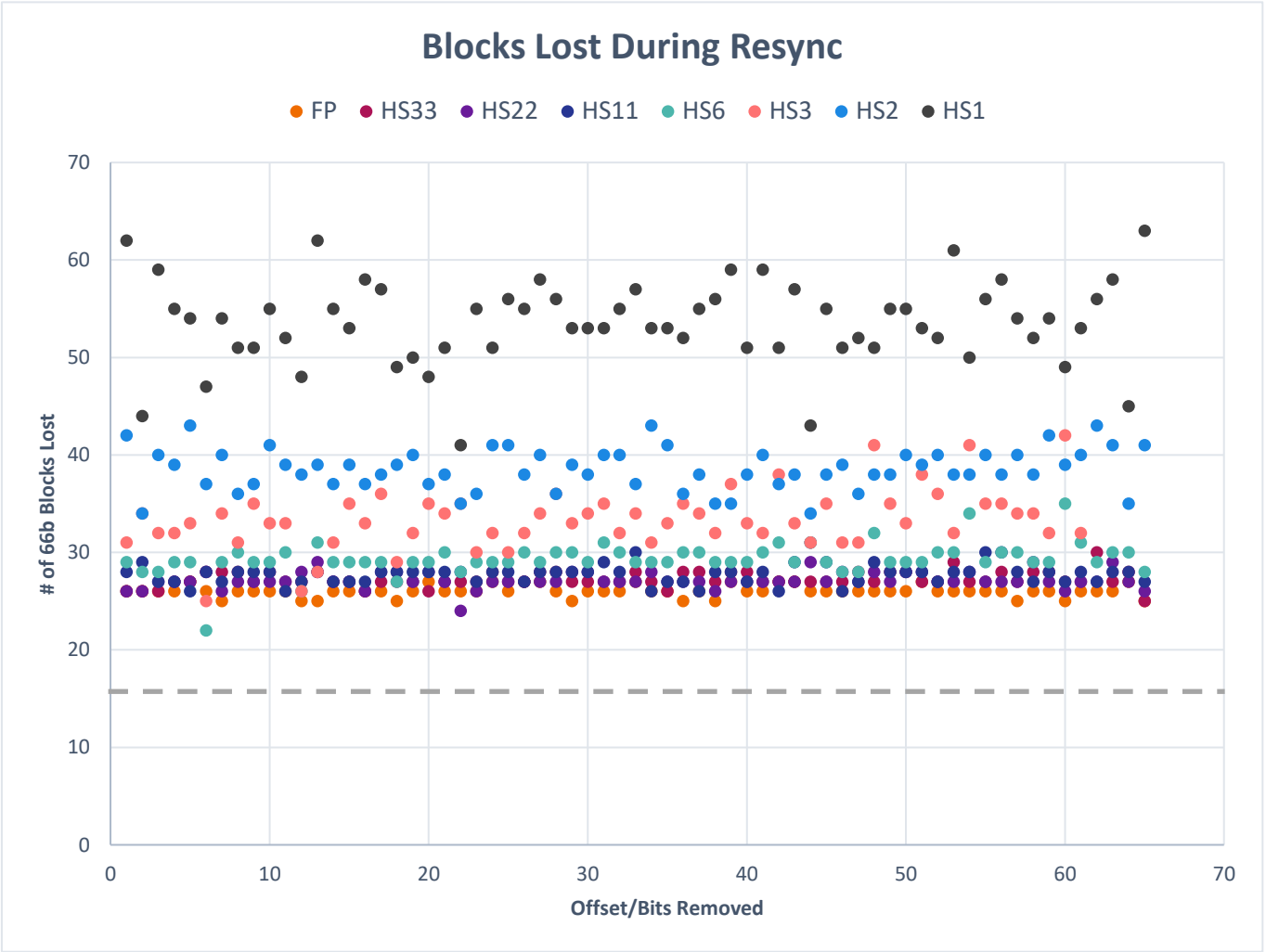
Performance Comparison

- Simulated shifting stream bits by *n,* with *n* swept from 1 to 65.
- Variants have too good of performance to be clearly visible, see next slide.
- Last 4 “Original” system data points are the result of the Serializer’s slip pattern.



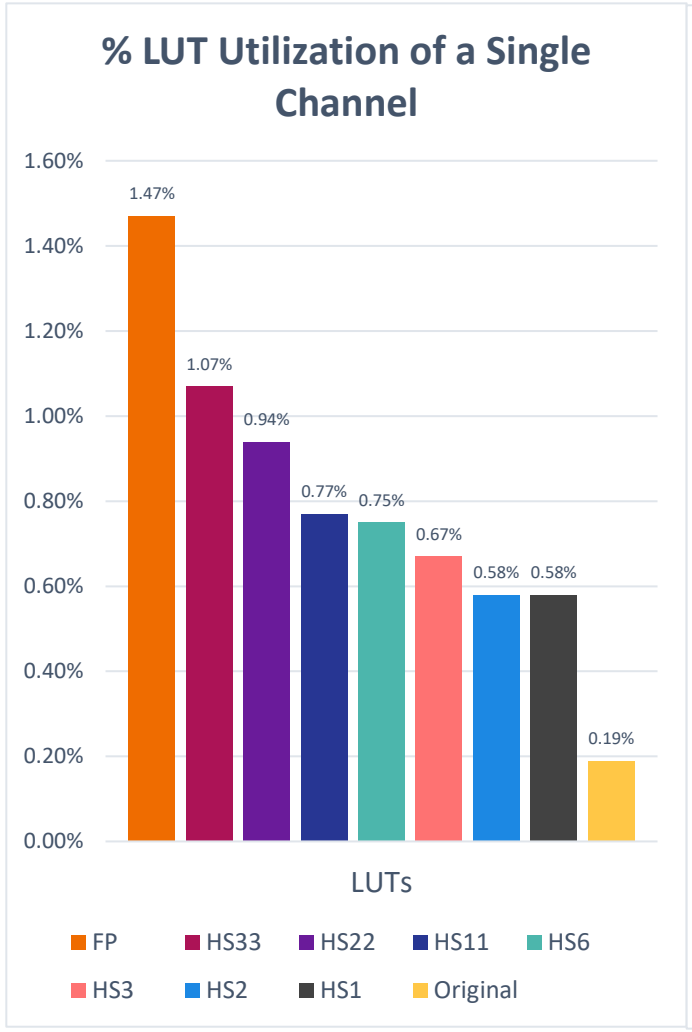
Performance Comparison

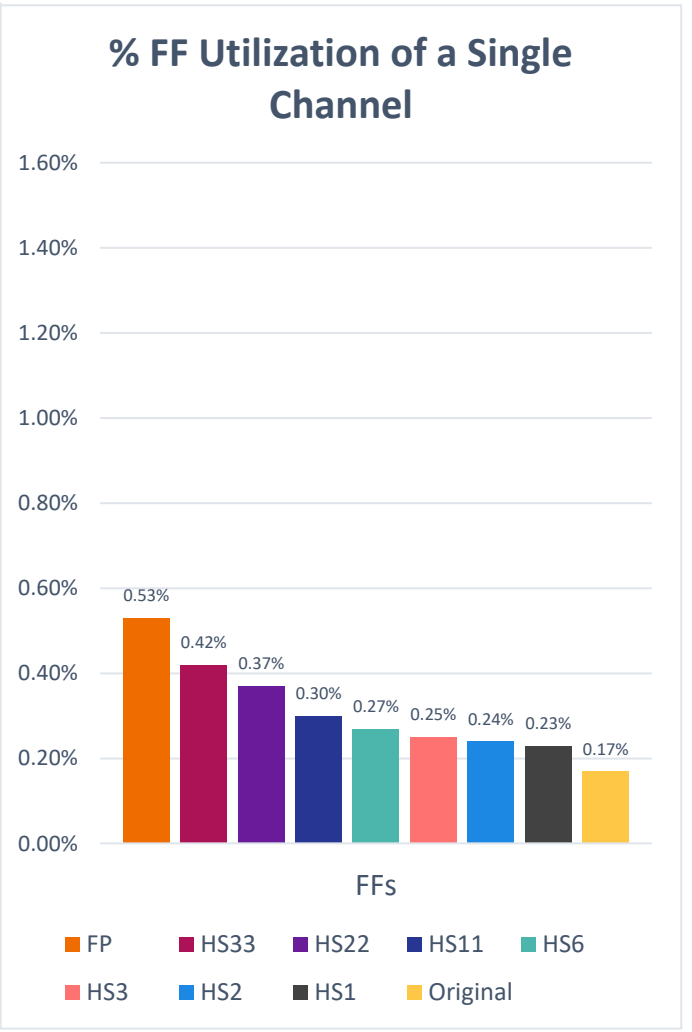
- 16 of the blocks lost because of the minimum number of consecutive valid blocks requirement to achieve synchronization
- Additional lost blocks are how long it takes for the aligner to detect desync and determine correct alignment



Resource Utilization Comparison

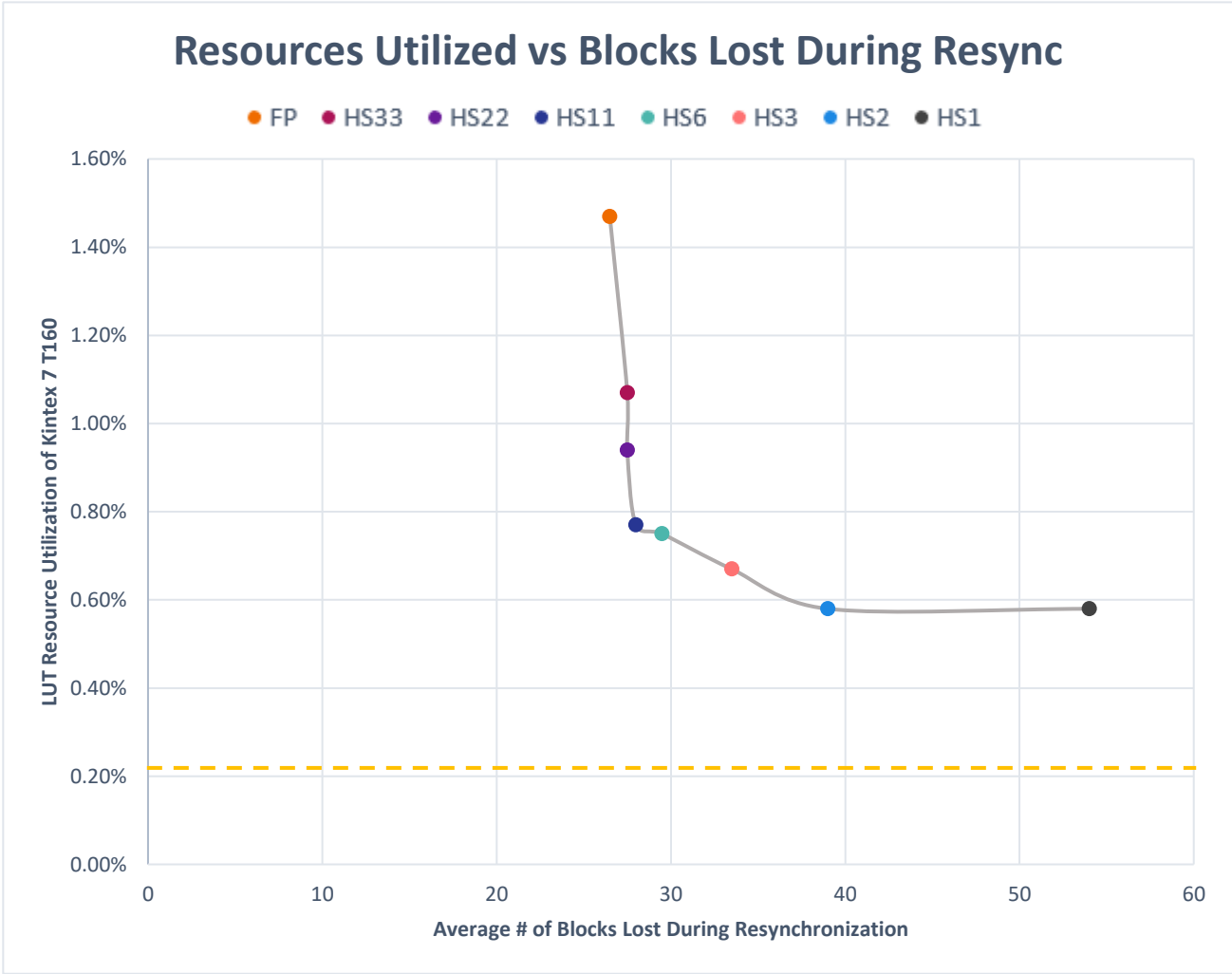
- Targeted a Kintex 7 T160 Xilinix FPGA, using Vivado Mapping tools
- Original system leveraged existing logic for alignment
- Developed variants added significant additional logic





FP and HS*n* Variant Tradeoffs

- Summary of LUT resource utilization vs average of blocks lost during resynchronization
- Logic outside of the aligner utilize 0.22% of FPGA resources



Future Work

- The number of consecutive valid headers required for synchronization can be mathematically optimized with sufficient data. The performance enhancement would be significant compared to the negligible cost in resources associated.

- The system can be improved, or a variant can be developed, which address bit flips. The aligners in this project are built to recover quickly from adds or drops but not flips.

Questions?

Extra Slides

Original Scheme: Gearbox Bitslip