ANATOLIY
MARTYNYUK

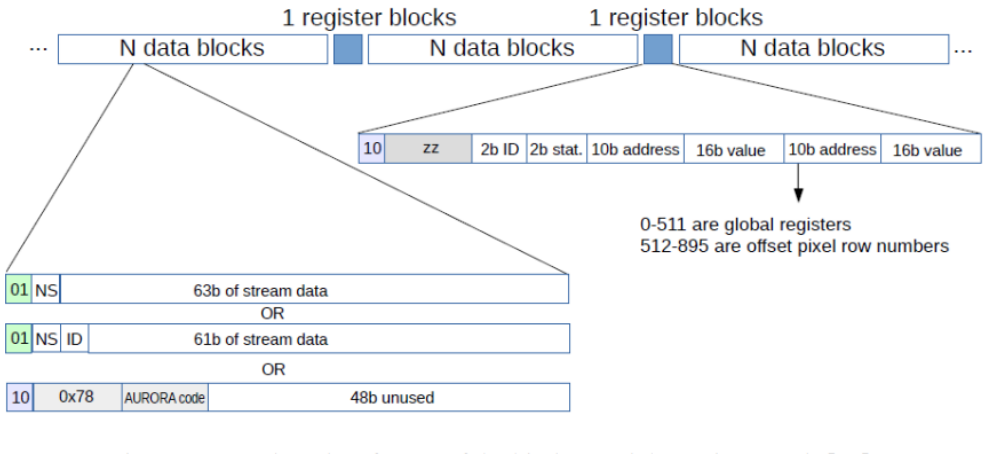
Custom “SEE tolerant” Aurora Gearbox

Overview

- The YARR rx from the RD53B receives serial data across multiple lanes with a 2 bit “delimiter” to identify individual data blocks.
- SEEs can corrupt the data on the output of the RD53B so that bits are dropped, added or flipped within the data stream, resulting in a loss of synchronization between the RD53B and YARR.
- THE YARR rx has a sync loss detection and recovery scheme… however, it suffers from inefficiencies which result in an unnecessary number of lost data and can be improved.
- The new recovery scheme aims to remove redundancy and complexity as well add parallelism to improve sync recovery performance.
- The new recovery scheme can provide moderate improvements at no cost in resources, upwards to drastic improvements with an investment in device resources.

Context : Communication

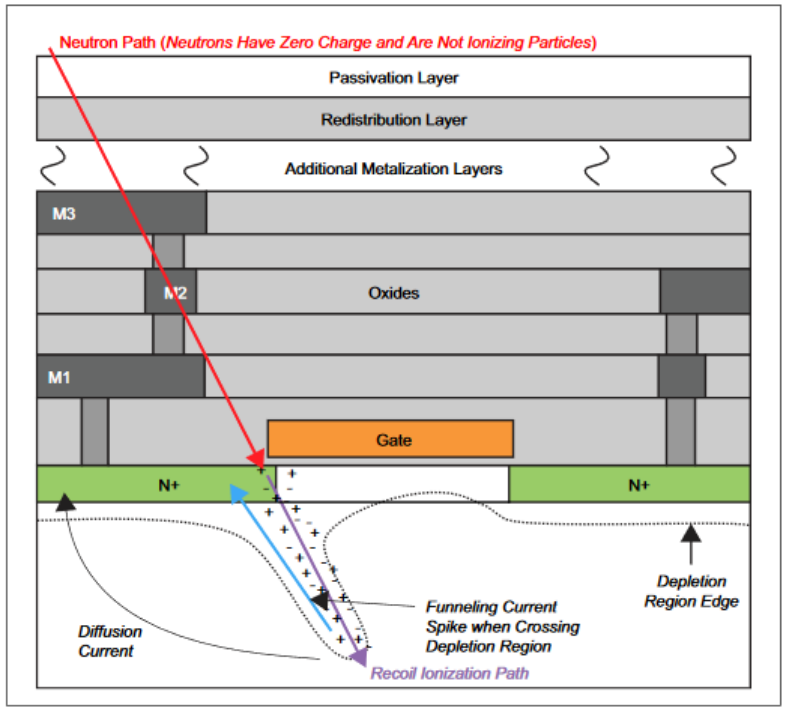
- The RD53B and YARR DAQ communicate via the 64b/66b Aurora encoding. Four Channels transmit data simultaneously.
- Aurora encoding packs together 64 “scrambled” bits of scrambled data with 2 header bits, which can be either a “01” or a “10”.
  - The scrambled aims to improve the DC balancing of transferred bits.
  - The two header bits are notably unscrambled.
- The YARR examines 2 of every 66 bits of the stream.
  - If a 01 or 10 appear consistently for a set number of data blocks, the stream is considered in sync.
  - Otherwise, the YARR will choose two new bits to observe.



Context : Single Event Effects (SEEs)

SEEs are radiation phenomena observed in electronic devices which result in functional errors either temporarily or sometimes irreversibly. Two of the relevant temporary SEEs are SEUs and SETs:

- SEUs (Single Event Upsets) :
  - Occur when charged particles create an ionization path within a memory cell. The resulting current/voltage spike may flip the cells value.
  - Flipped memory cells can have consequences ranging from mild, as in a pipeline register bit flipping, to moderate, as in a control or FSM state register flipping, to drastic, in the case where FPGA configuration memory may be altered.
- SETs (Single Event Transients):
  - Occur when charged particles cause a current/voltage spike in a combinatorial path.
  - May result in incorrect data being latched if the path was in the datapath.
  - May have more drastic consequences if a clock path or reset were to experience the glitch.



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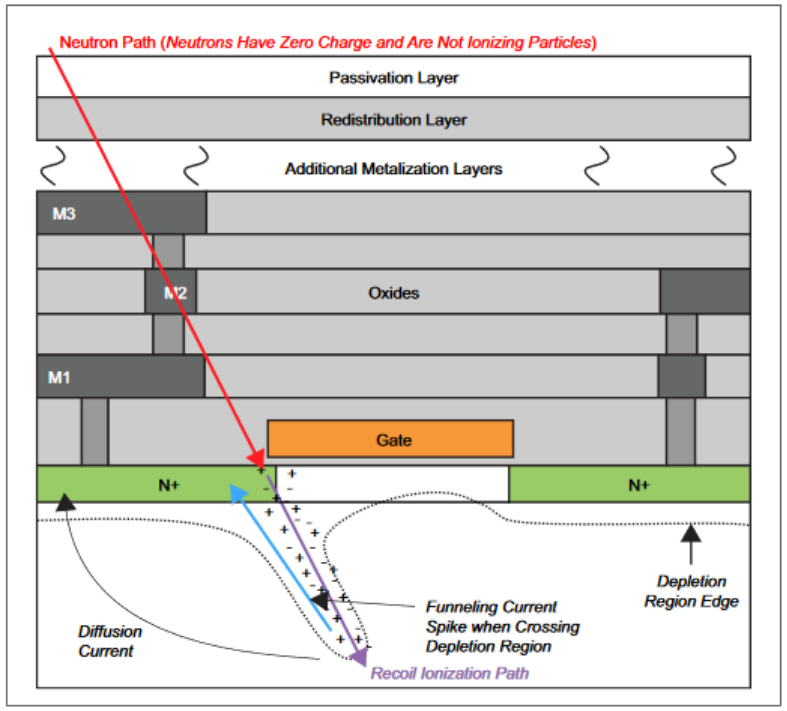


SEEs Consequences to the YARR

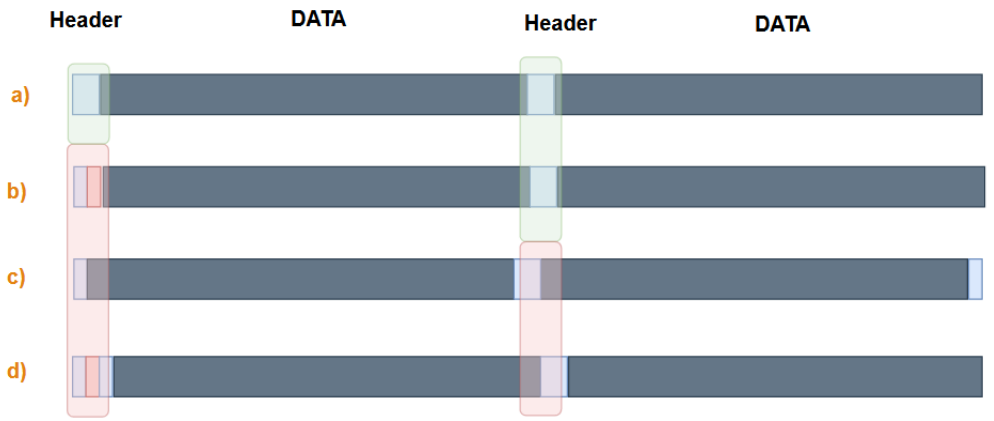
We can ignore the physics surrounding SEEs and represent them in digital logic as bit flips, bit drops, and bit adds:

a) The YARR watches for two header bits and once its seen enough consecutively, it is considered in sync.

b) A bit flip may cause the header to become invalid, which may start a resync process unless there is some flip tolerance, or it happened at a data bit.

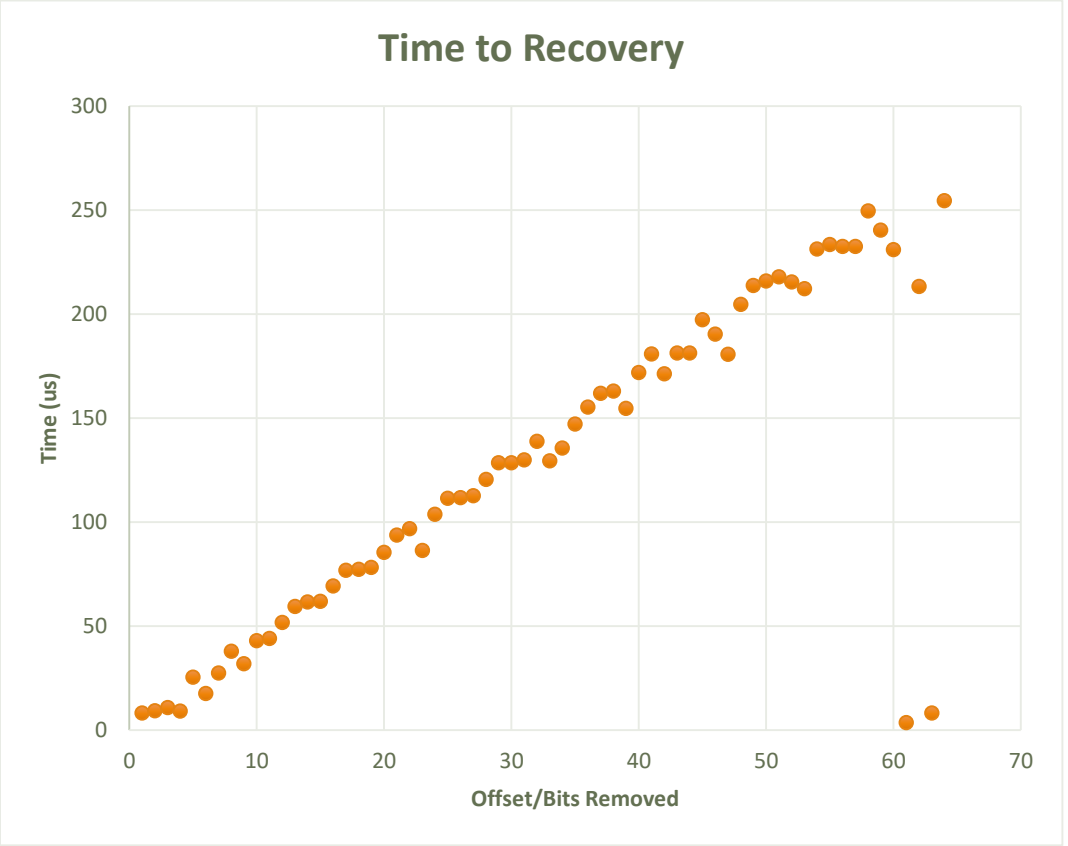
c) A bit drop, always resulting in a resync process.

d) A bit add, always resulting in a resync process.



Original Resync Scheme

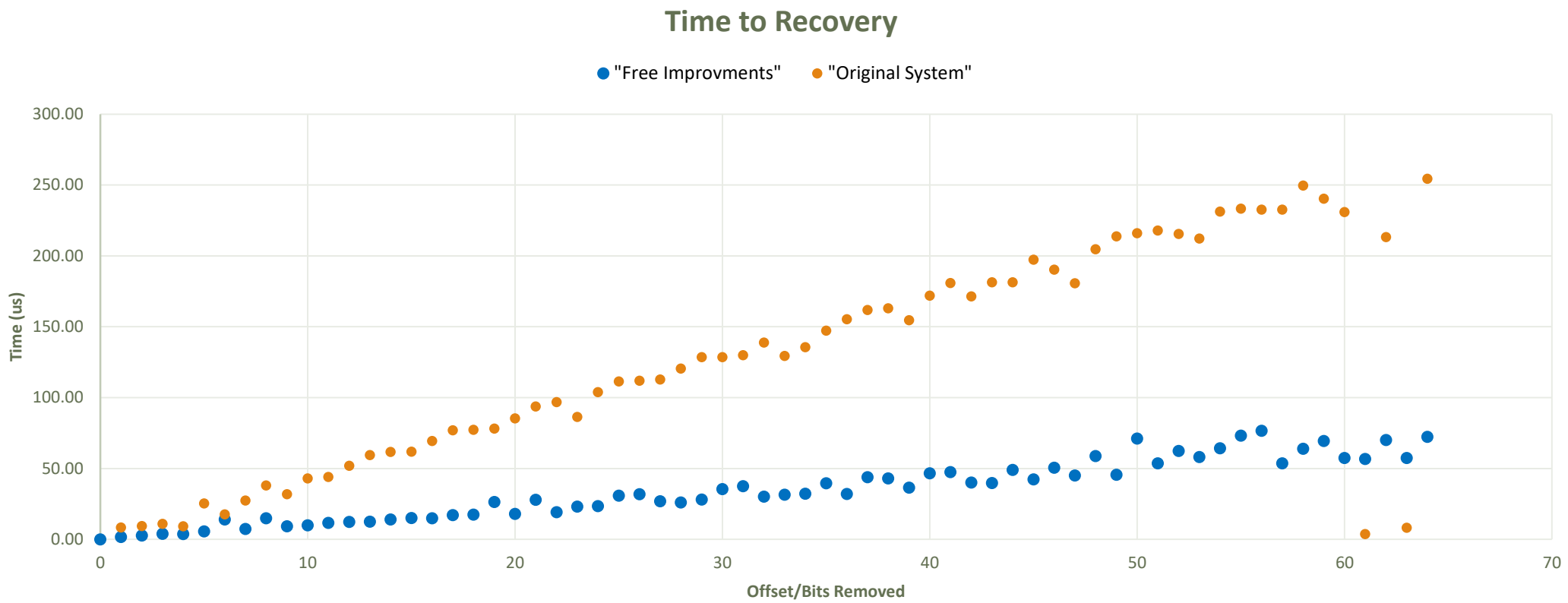
TODO: Describe and discuss primary issues with original resync scheme



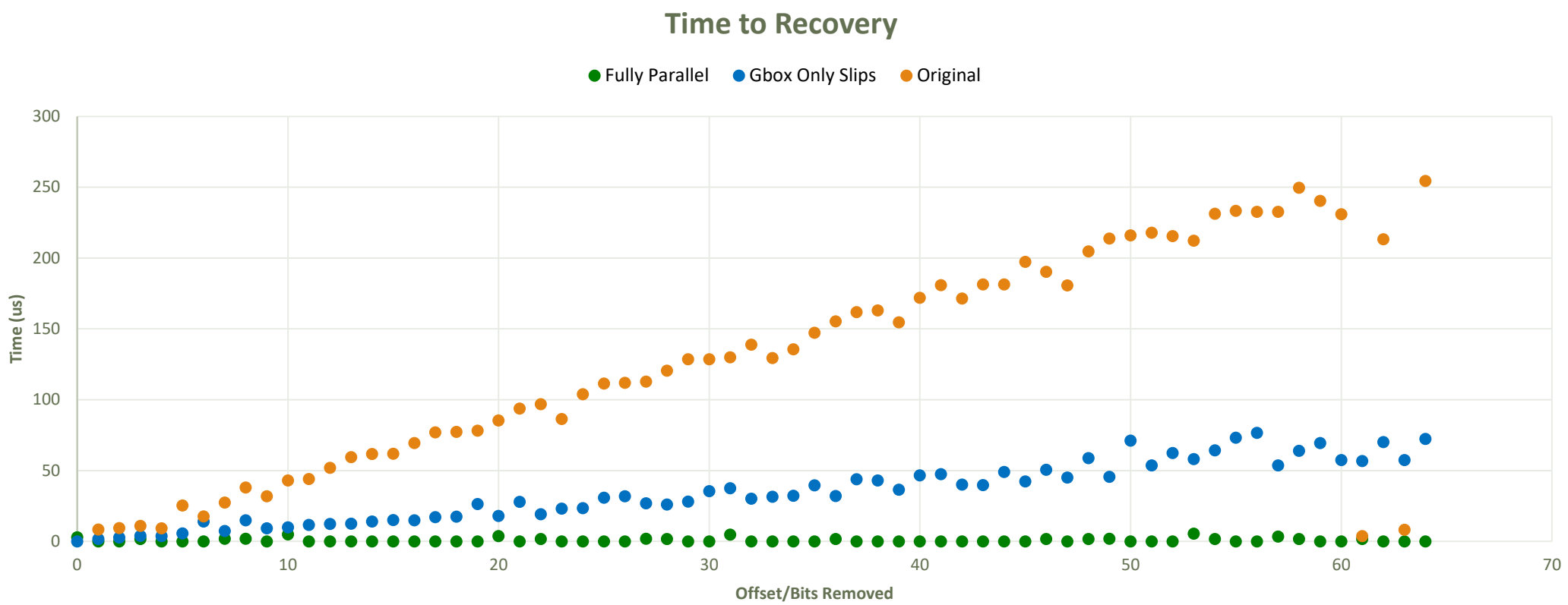
New and Improved Resync Scheme

TODO: Discuss changes and additions outside of improvements to the issues mentioned in the previous slide.

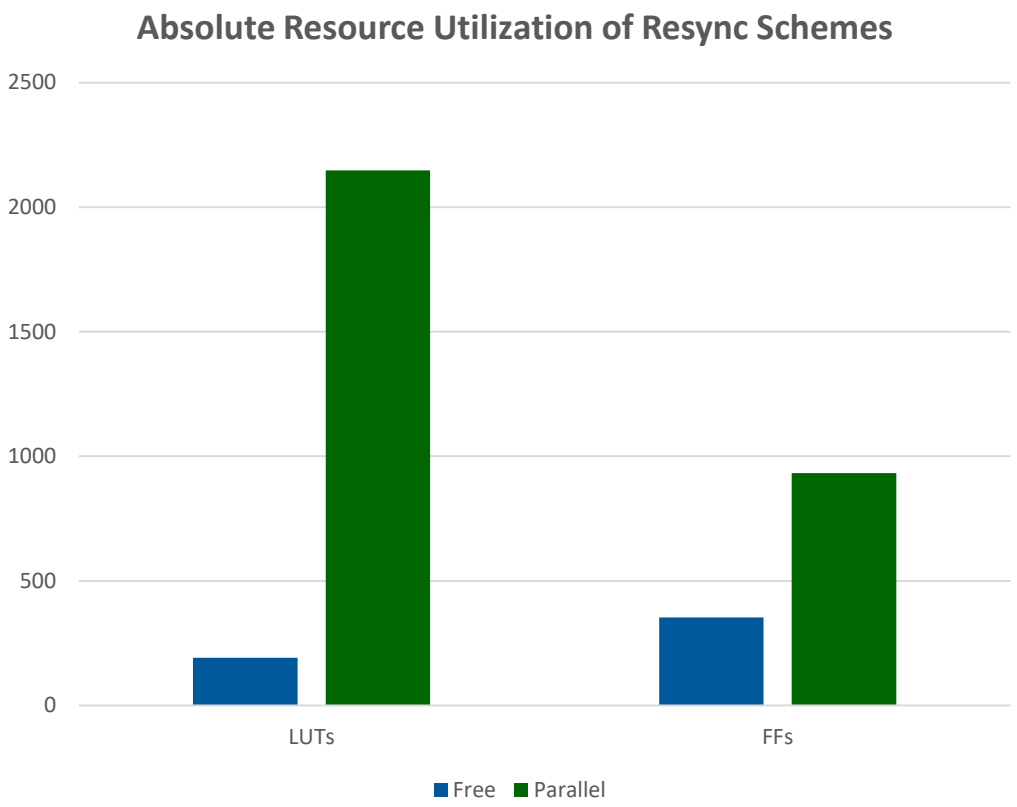
Performance with Resource Free Improvements

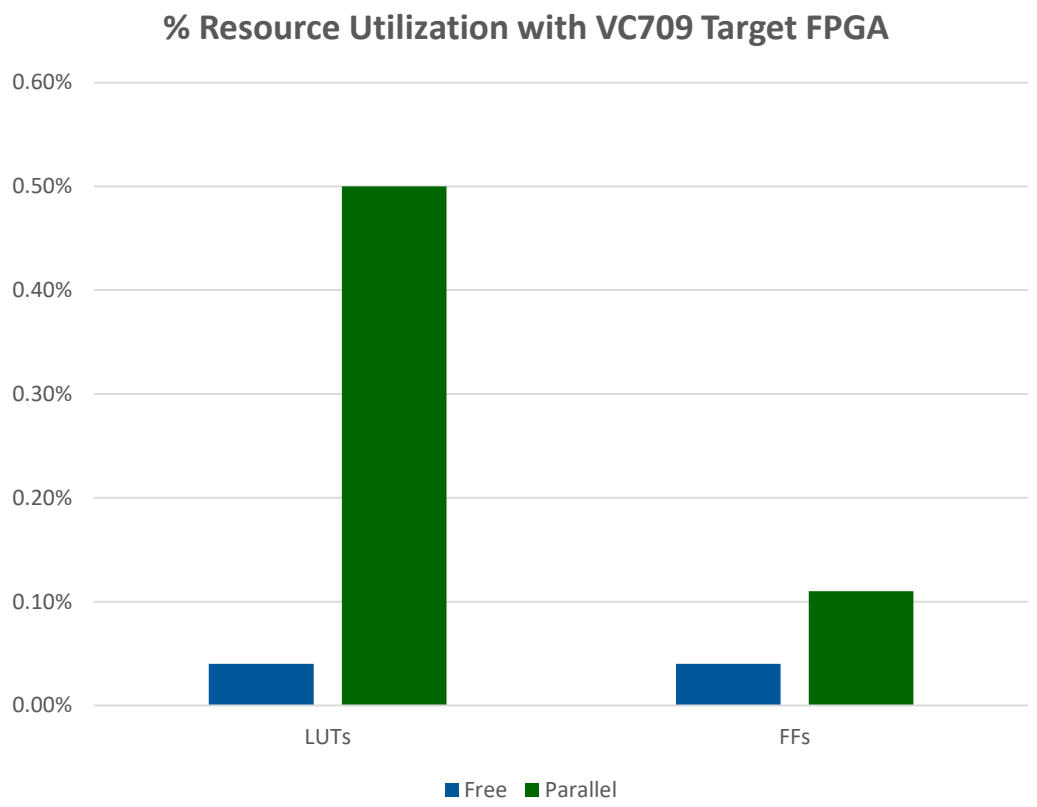


Performance With Fully Parallel Search



Current Resource Utilization Comparisons





Further Development

- Resolve Outstanding Issues:
  - Although simulations demonstrate the new sync schemes working functionally, newly introduced timing issues must be resolved which may introduce additional resource to those already accounted for.
- Parameterizable Partially Parallel Search:
  - A tradeoff can be made between the amount of parallel search occurring to maximize common case recovery while minimizing the additional resource required to support the search.
- Error Tolerance Algorithms:
  - At a relatively cheap cost in resources, various error tolerance schemes can strike a balance to avoid pointless and costly searches as a result of a bit flip, while remaining vigilant to bit adds and bit drops.
  - The resources used to track tolerance and evaluate whether sync is achieved can be merged with the parallel header checking to reduce resources.