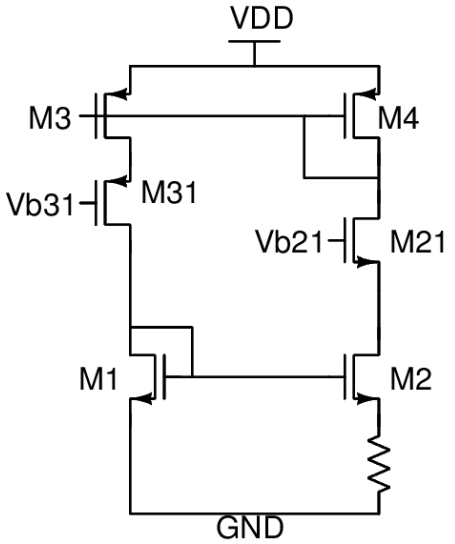
CMOS DESIGN CHALLENGE

16 JAN 2015

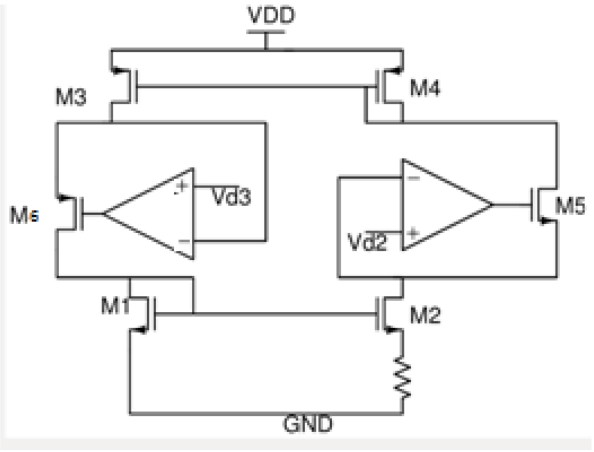
Q1.1) Modification of beta multiplier circuit

We want to modify beta multiplier circuit to make it independent of finite output resistances of transistors.

- Due to finite resistances (r_0) of each MOSFET, current value in transistor changes as per V_{DS} value.
- Stabilizing V_{DS} by making $r_0$infinite is solution for short channel devices.
- Cascode configuration is generally used to improve equivalent resistance of MOSFET and reduce its dependence of current on V_{DS}.
- Modified circuit is as shown below:



- Value of Vb31 is chosen such that drain voltage Of M3 matches with drain voltage of M4 in saturation for given current values. Similarly, Vb21 is chosen such that drain voltage of M2 matches with drain voltage of M1.
- This circuit has improved output resistances of M3 and M2. To improve the circuit further, op-amp can be incorporated as shown below:



- Here, op amp are used to derive gate drive of additional MOSFETs M6, M5. Explanation is as follows. Vd3 and Vd2 are expected voltages to draw desired current by M3 and M2.

Q1.2) Qualitative explanation

Explanation for M3 drain voltage stabilization:

- If M3 draws more current than M4 due to finite output resistance difference, its drain voltage will be below than the voltage required for drawing desired current. Now, op-amp has reduced value of voltage at negative terminal. Hence, M6 gate voltage increases. As gate voltage of M6 increases, its current starts reducing forcing reduction of current in M3. Hence, current value in M3 is stabilized.
- Similarly, if M3 draws less current than M4, its drain voltage will increase and op-amp will have reduced voltage difference between its positive and negative terminals. This will reduce gate voltage of M6. Hence M6 draws more current forcing increase of current in M3.
  Above explanation holds in case of M5 and Vd2.

Q2) Operational amplifier design:

This is two stage op-amp with miller compensation.

Desired specifications:

1. Gain ≥ 50 dB
2. 3-db Bandwidth ≥ 2 kHz
3. Unity gain bandwidth ≥ 3 MHz
4. Power ≤ 10 mW
5. C_L = 1 to 1.5 pF

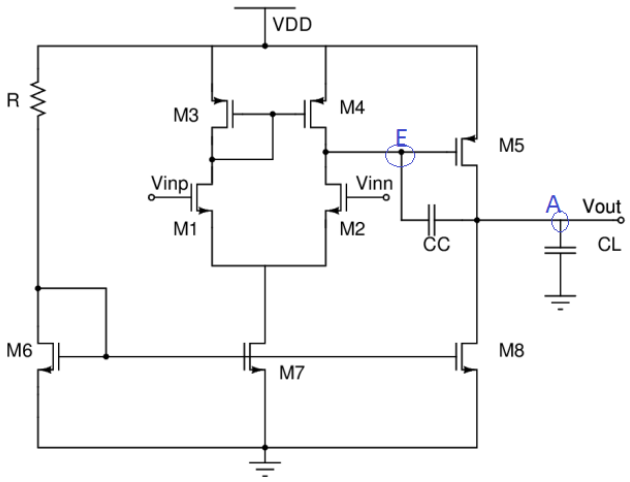
Formulae for given specifications:

1) In band gain of the two stage op-amp is multiplication of individual stage gain.

$$A_V = g_{m_2} * \left(r_{o_2} || r_{o_4}\right) * g_{m_5}(r_{o_5} || r_{o_8})$$

2) 3dB bandwidth and unity gain bandwidth:

Due to miller compensation, dominant pole will be present t node "E" as indicated in figure below. 2nd dominant pole will be present at output node "A".
It is assumed that 2nd pole is far away from unity gain frequency and additional zero introduced by the compensation is also far away. (This has to be made sure by selecting appropriate value of C_c andg_{m_5}). Transistor internal capacitances are ignored while calculation.



Dominant pole at point E:

Equivalent resistor at this node is parallel combination of output resisistances of M_2 and M_4.

Equivalent capacitance at this node is contributed by miller capacitance c_c maximally. Exact expression is $[(1 + g_{m_5}(r_{o_5}||r_{o_8})) * C_c + (r_{o_5}||r_{o_8}) * (C_c + C_L)]$.

Hence value of pole is given by -

$$P_E = \frac{1}{(r_{o_2}||r_{o_4}) * [(1 + g_{m_5}(r_{o_5}||r_{o_8})) * C_c + (r_{o_5}||r_{o_8}) * (C_c + C_L)]}$$

Pole at output node is given by –

$$P_A = \frac{g_{m_5}}{C_L}$$

Zero introduced by the miller compensation is –

$$W_z = \frac{g_{m_5}}{C_c}$$

3) Power constraint:

Total power consumed by the circuit is product of sum of currents drawn by tail transistors and supply voltage. Assume -

$$I_{M_6} = I_{M_7} = I_{M_8}$$

For power less than 10mW, current drawn in total should not exceed 2mA. Assume current drawn by each transistor is **500uA**. Hence, power constraint is satisfied.

Derivation of device parameters based on above equations:

- As we are assuming first dominant pole is given by node E and pole at node A and zero are outside pass band and far enough. Hence, we can consider 20dB/decade slope for gain after first pole till unity gain frequency.
- Currents of each transistor and hence output resistance is as per table below (using value of λ as per given data):

Transistor	Current	Output resistance($r_0 = \frac{1}{\lambda I_D}$)
M1	250uA	200K
M2	250uA	200K
M3	250uA	320K
M4	250uA	320K
M5	500uA	160K
M8	500uA	100K

$$P_A = \frac{g_{m_5}}{C_L} \gg 4MHz * 2 * \pi$$

With $C_L = 1pf$, $g_{m_5} \gg 2.52 * 10^{-5}$.

Choose, $\boldsymbol{g_{m_5} = 4 * 10^{-3}}$.

Similarly for

$W_z = \frac{g_{m_5}}{C_c}$ $greater\ than\ 4MHz * 2 * \pi$ and choosing C_c=1pf, above choice of g_{m_5} will suffice.

Now, turn our attention to 3dB edge.

Putting values of resistances and g_{m_5}, C_c and C_L:

$P_E =$ 32872.62 rad/s

Hence dominant pole is present at **5.232KHz.** It satisfies 2KHz criteria.

For 50dB gain → 10^(2.5) = 316.23.

Using gain equation - $\boldsymbol{g_{m_2} > 1.044 * 10^{-5}}$.

Choose $\boldsymbol{g_{m_2} = 2 * 10^{-4}}$

- Recalculating specifications as per choice of values –

Gain	81.67dB
3dB bandwidth	5.232KHz
Pole at node A	636.62MHz
Zero frequency	636.62MHz

By 20dB/decade attenuation from 5.232KHz, unity gain frequency will be **63.406MHz** will be unity gain frequency.
As all criteria are satisfied, we now calculate values of W with L=1um for all transistors.
Assumption: For 1um length devices, long channel approximation can be used.

$$g_m = \text{sqrt}(\frac{2\mu C_{ox} W}{L} I_D)$$

M1, M2:
Using $g_m, I_D, \mu_n C_{ox}$ values:
(W/L) = 0.67
Choose, **L = 2um and W = 1.34um**

M5:
Using $g_m, I_D, \mu_p C_{ox}$ values:
(W/L) = 400
Choose, **L = 1um and W = 400um. Use 10 fingers of 40um in design to implement this transistor.**

M6, M7, M8:
M6 acts as current source and M7, M8 mirrors current. We assume same (W/L) for these transistors. Hence, 500uA carries by each of them.
I_D = 500uA

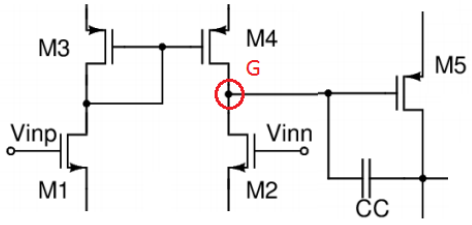
$$I = \mu_n C_{ox} \frac{W}{2L} (V_{GS} - V_{th})^2 = \frac{(V_{DD} - V_{GS})}{R}$$

Putting values of $V_{DD} = 5V$ and assuming $V_{GS} = 1.9V. (greater\ than\ V_{th})$.

$$R = 6.2K$$

(W/L) = 6.887
Choose **L = 1um and W = 6.887um.**

M3, M4:



For M5 to be in saturation,

$$V_G - V_{DD} < -0.9V$$

We assume $V_G = 3.1V$ in quiescent condition.

$V_{Drain} < V_{Gate} + 0.9$ for PMOS transistor in saturation. For M4, $V_{Drain} = 3.1V$.

Hence, $\mathrm{V_{Gate}} > 2.2V$ *in quiescent condition*. Assuming, $\mathrm{V_{Gate}} = 2.5\mathrm{V}$ and using current equation for PMOS –

(W/L) = 4.883

Choose L=1um and W=4.883um