## Device under test

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# Testing Digital Circuits using Embedded Systems

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## **Project Description**

Testing and verification of digital circuits using embedded systems.

- Combinational
  - Brute force.
  - Stuck at fault: s-a-0, s-a-1.
- Sequential
  - Scan Chain.
  - Checking experiment.
  - State-table based test generation.

#### Motivation

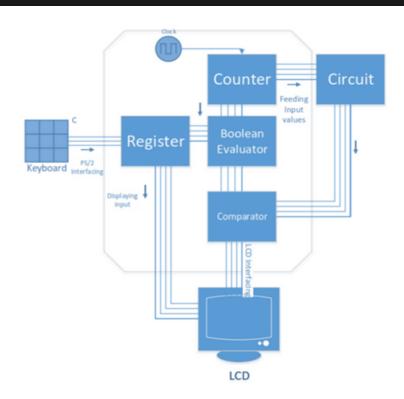
- To increase focus on circuit design than testing IC's.
- Efficient testing of design.
- Reduce the task of documentation.
- Aging of semi-conductors leads to less reliability on datasheet.

## Components



Beaglebone Black Keyboard and Mouse HDMI display

# Block diagram



## Overview

Input from user

Pattern generation

Verification

### **Combinational circuits**

- Accept no. of inputs/outputs from the user and formulas corresponding to different outputs.
- Generate all possible input patterns (Different types of counting).
- Compare expected and observed output.
- Display output.

## Circuit description

- No. of inputs: 8
- No. of outputs: 4
- Output 1: a+b
- Output 4: g+h
- ...
- Pin configuration

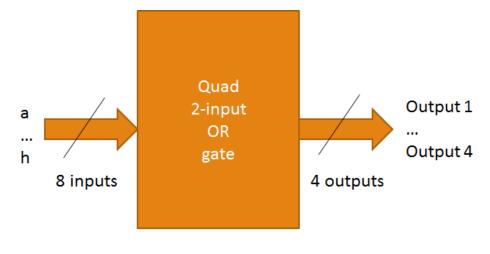


Fig 1. 7432

## Graphical User Interface

#### Refer to demonstration

## Sequential circuits

- Accept description of Mealy machine.
- Verification of each state and all its possible transition using graph theory.
- Generate result.

## Circuit description

 Description for the graph shown in figure 1 is as follows:

0:'ab', 1:'bc', 2:'ca', 3:' cd', 4:'db', 5:'da'

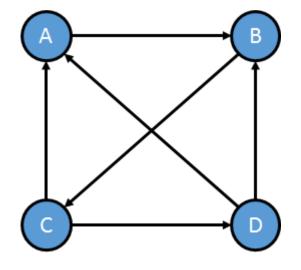


Fig 2. State Transition Graph

## Graphical User Interface

#### Refer to demonstration

### Future work

- Product design.
- Validating formulation of sequential circuit testing algorithm based on combination of random path traversal and shortest path algorithm.
- Optimized algorithm for directed graphs.
- Developing indigenous Data Acquisition hardware for measuring transient behaviour.
- Creating online Javascript based software.
- Implementation on FPGA.

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