



gradeup

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Computer Organization and Architecture

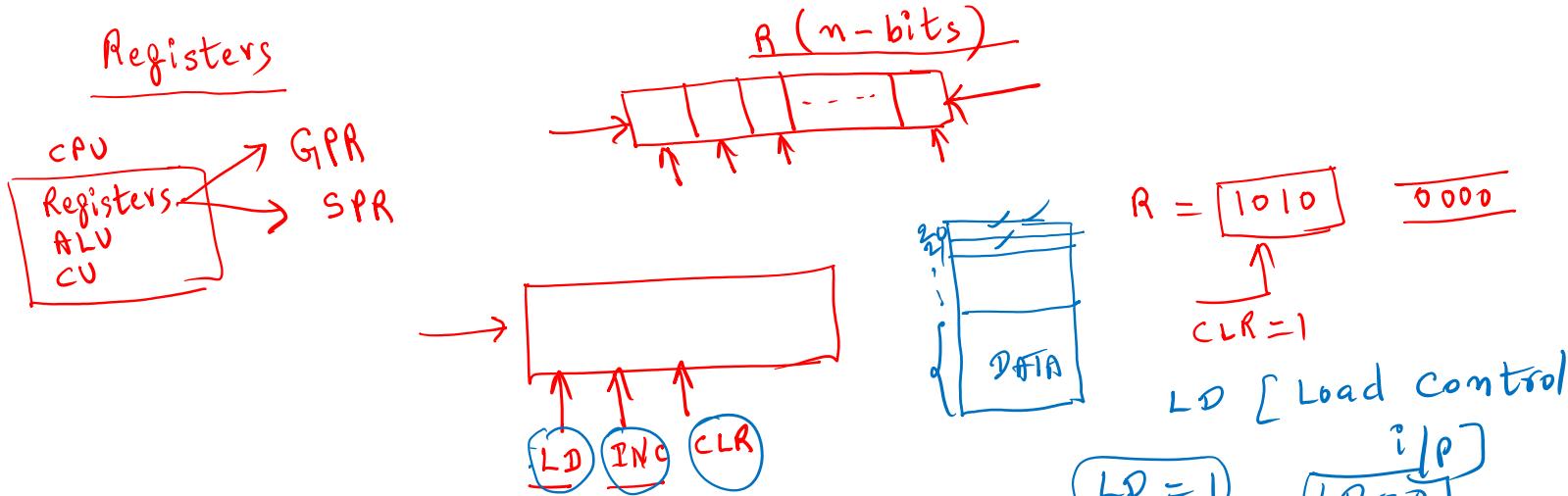
Registers and Memory Unit

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



Registers and Memory Unit



Special Purpose Registers

✓ PC = Program Counter
 ✓ MAR = Mem. Address Register
 ✓ IR = Instruction Register
 ✓ DR (MBR) = Data Register

\underline{SP} = Stack Pointer
 \underline{INPR} = Input Register
 \underline{OUTR} = Output Register
 \underline{AC} = Accumulator Register
 \underline{TR} = Temporary Register.
 \underline{PSW} = Processor Status Word

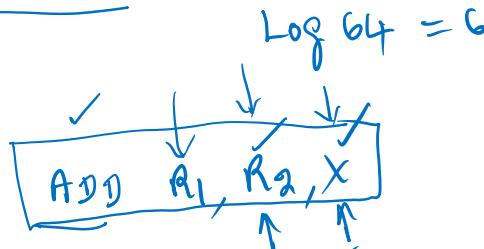
Registers and Memory Unit

General Purpose Registers [GPR]

$\log_{16} 2^4 = 4$ bits

16 Registers [R₀ to R₁₅]

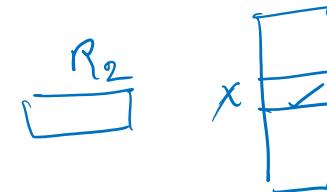
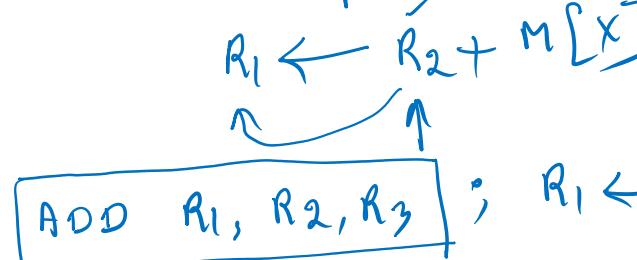
$$\left\{ \begin{array}{l} R_0 = 0000 \\ R_1 = 0001 \\ \vdots \\ R_{15} = 1111 \end{array} \right.$$



64 GPR

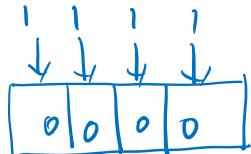
[R₀ → R₆₃]

$$\begin{aligned} R_0 &= 000000 \\ R_1 &= 000001 \\ &\vdots \\ R_{63} &= 111111 \end{aligned}$$



Registers and Memory Unit

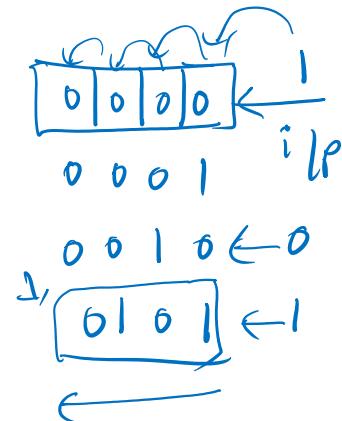
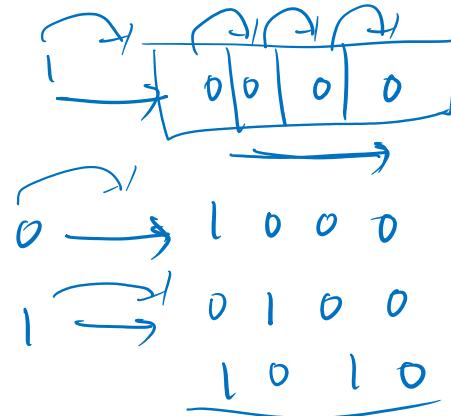
Parallel Load



R
1111
0000

1111

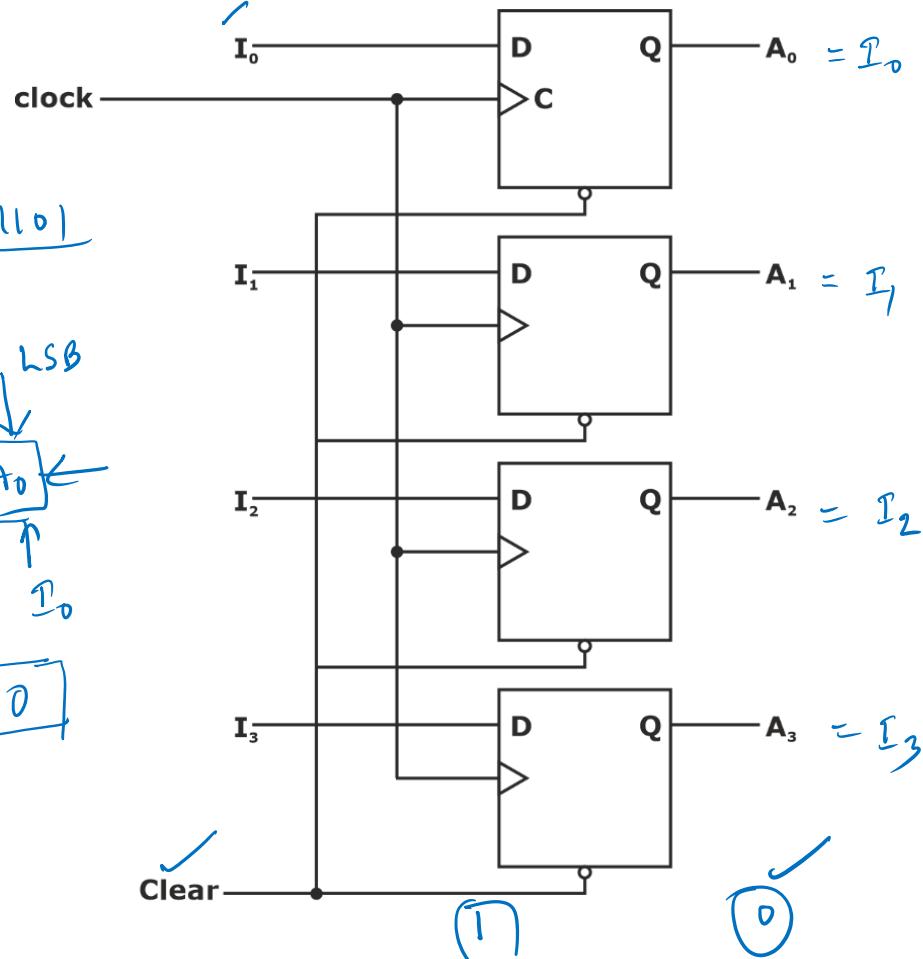
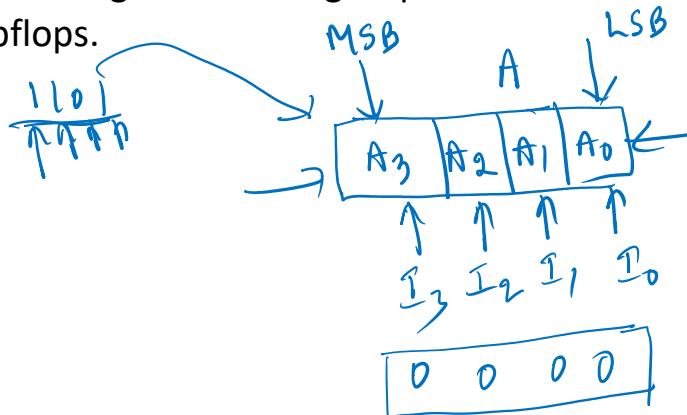
Serial Load



Registers and Memory Unit

Registers

A register is a group of flip flops with each flip flop capable of storing one bit of information. An n-bit register is the group of n-flip flops.



Registers and Memory Unit

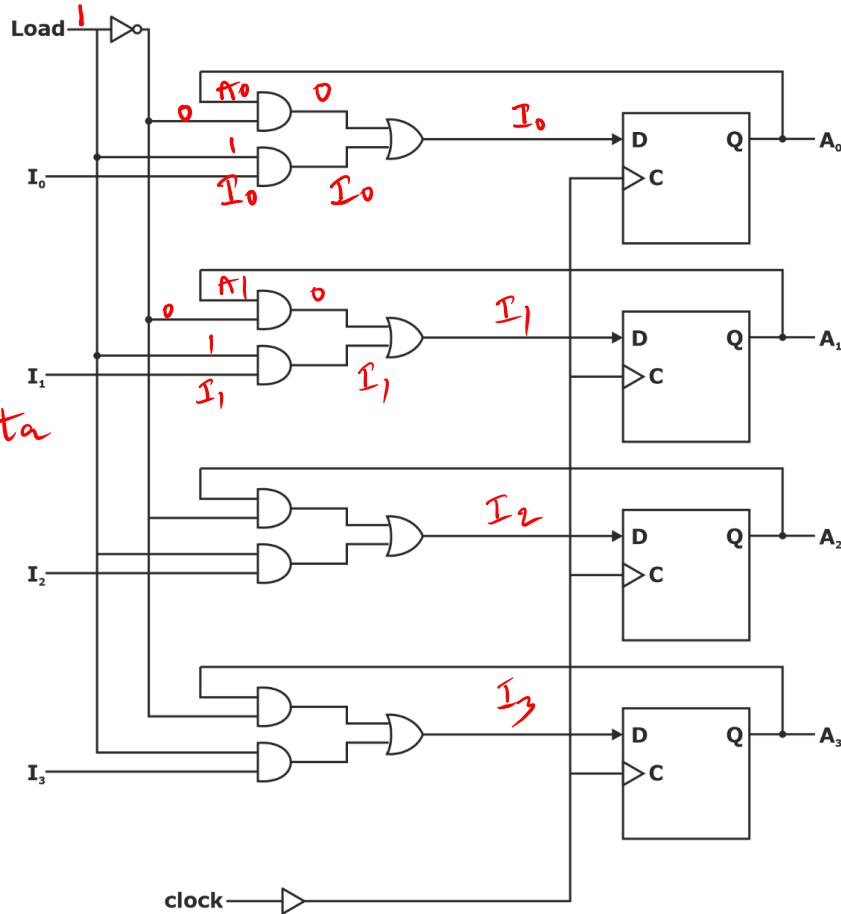
Register with Parallel load

Load Control i/p

Load = 0 [No - change]

Load = 1 [New Data can be loaded] ✓

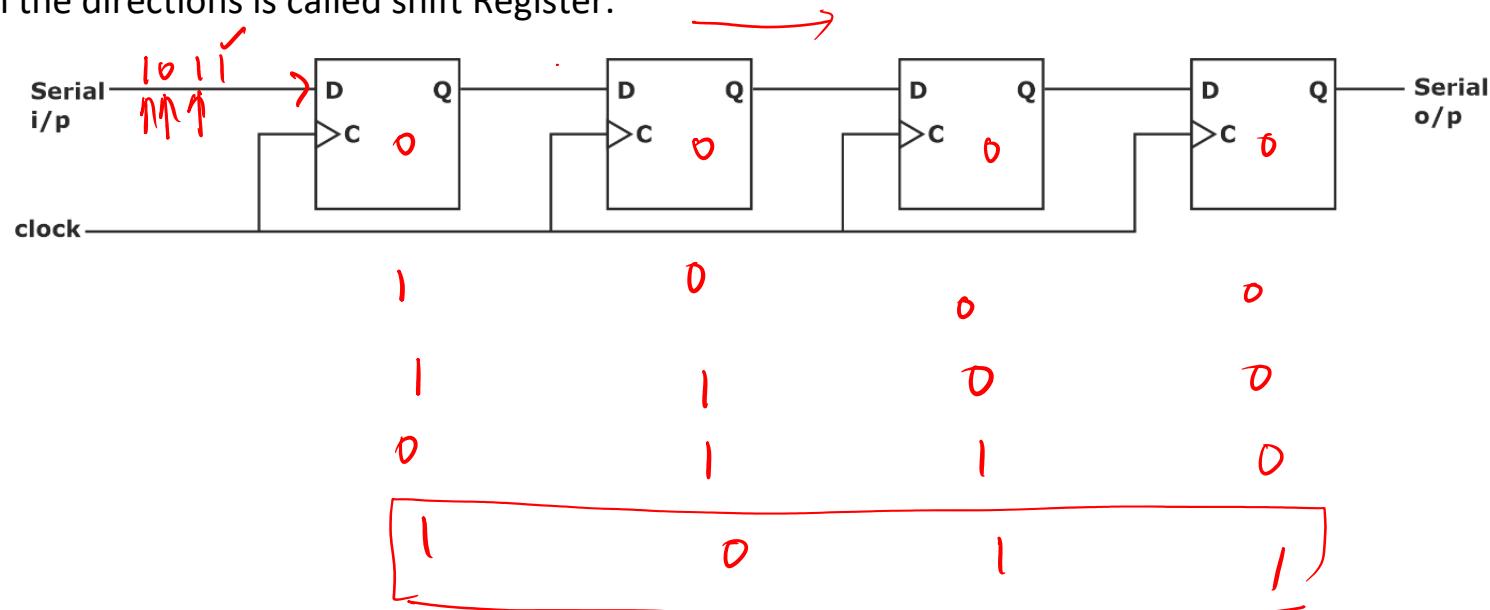
→ Parallelly, the data is Loaded.



Registers and Memory unit

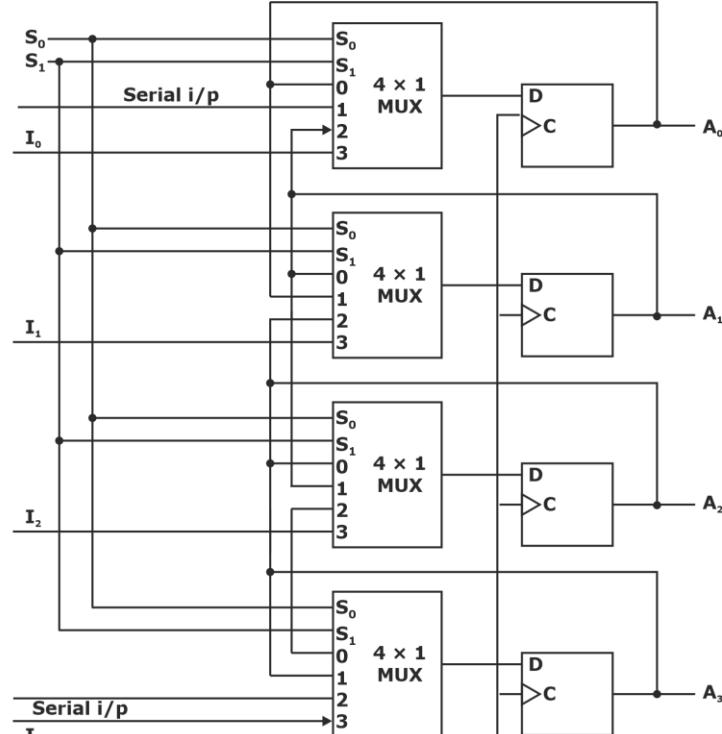
Shift Registers

A Register Capable of shifting its binary information in one or both the directions is called shift Register.



Registers and memory unit

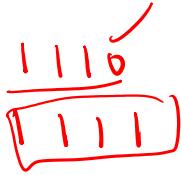
Bi-Directional Shift Register with Parallel load



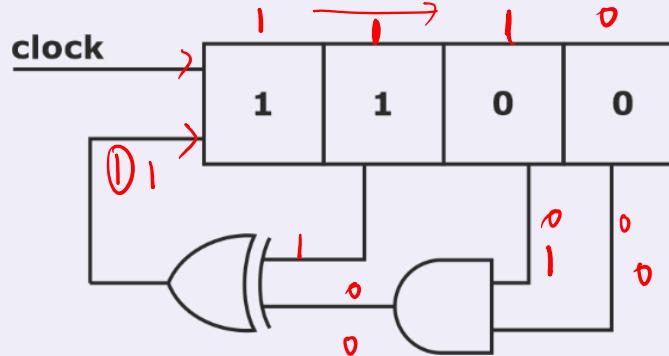
S ₁	S ₀	Reg opn	clock
0	0	No change	
0	1	Shift Right (down)	
1	0	left (up)	
1	1	parallel load	

Registers and Memory Unit

1st



1. Consider the following shift register

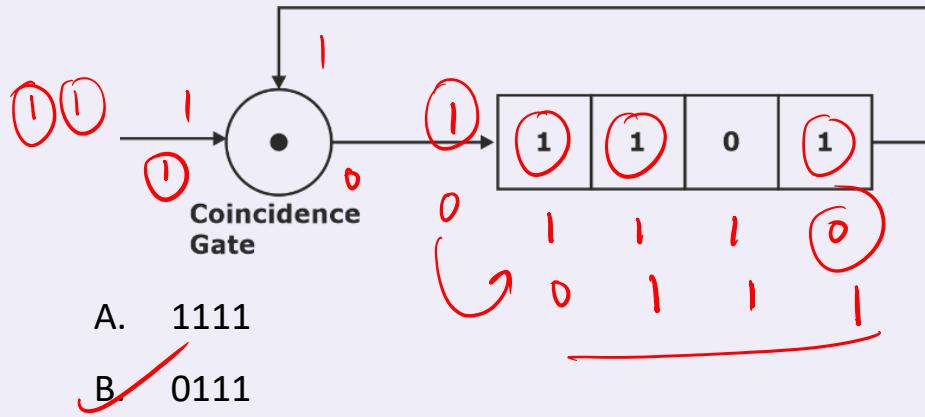


If initially register content is 1100, then after two clock pulse what will be the register content ?

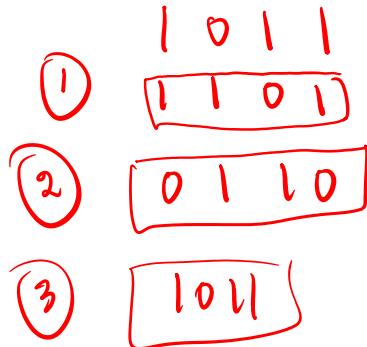
- A. 1100
- B. 1110
- C. 1111
- D. 0111

Registers and Memory Unit

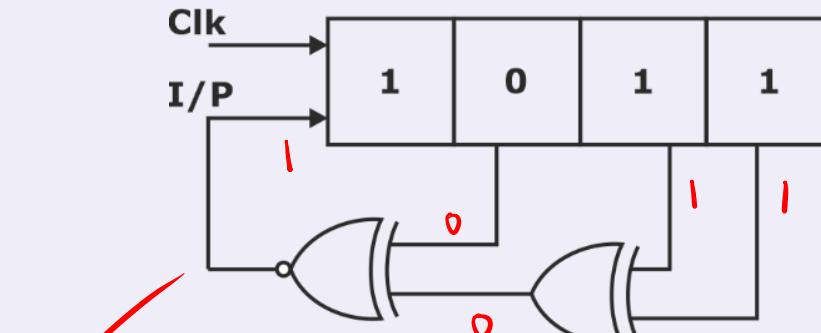
2. What is the final value stored in the linear feedback shift register, if the input is 11 ?



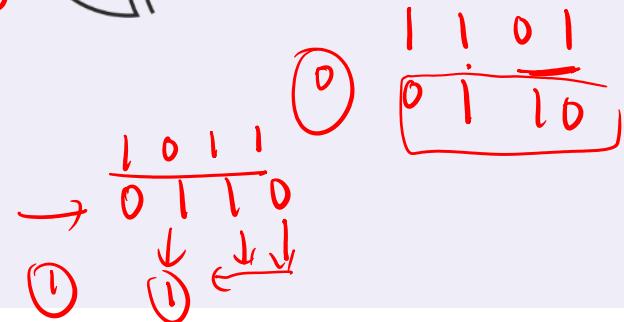
Registers and Memory Unit



3. The shift register in the following figure is initially loaded with 1011. With each clock pulse the pattern in the register shifts one place right. What will the register contain after 3 clock pulses ?

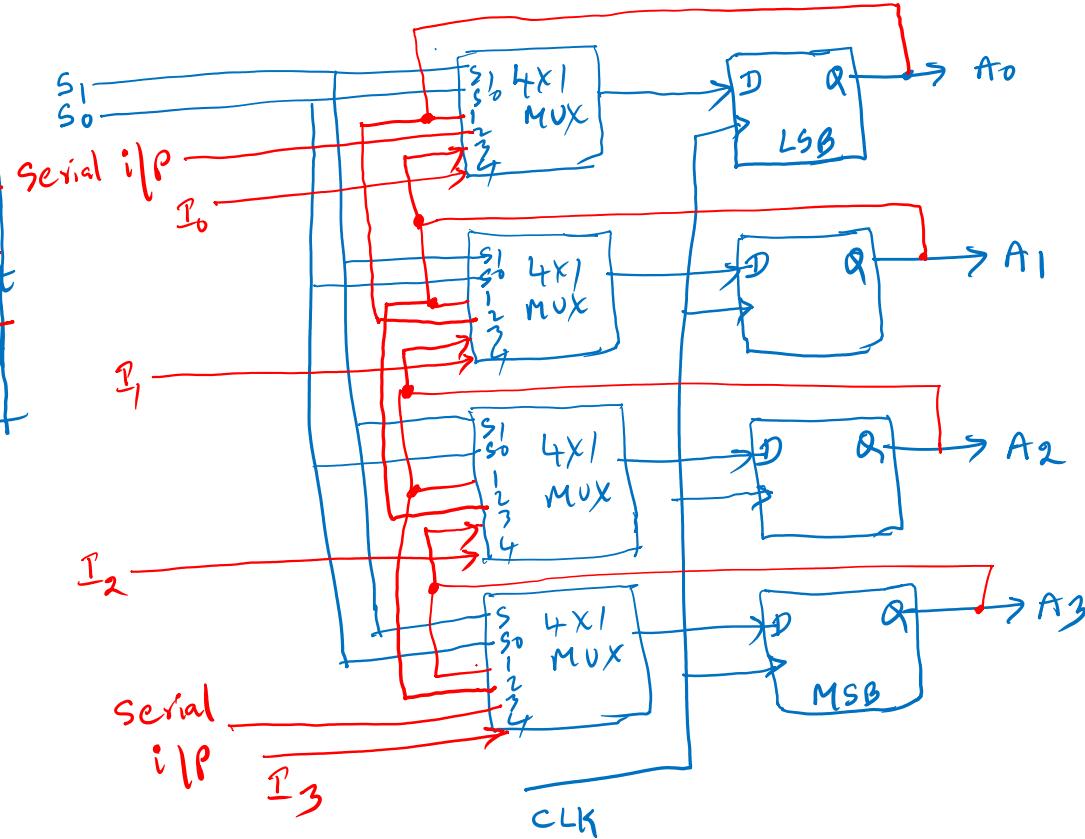
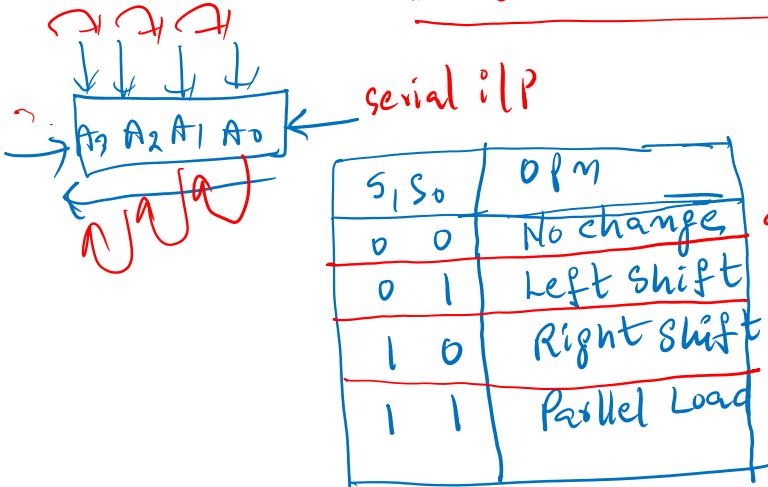


- A. 1011
B. 1100
C. 1111
D. 1110



Registers and Memory Unit

Bi-Directional Shift Register with Parallel Load



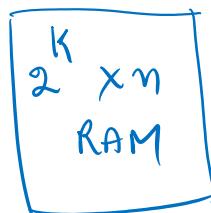
Registers and Memory Unit

Primary Memory

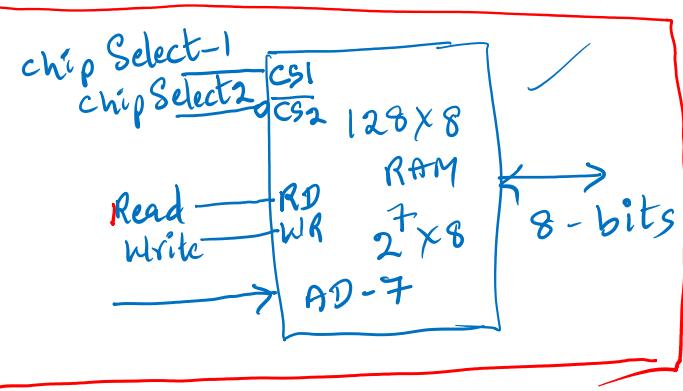
RAM [Random Access Memory] Volatile
ROM [Read only Memory] Non-Volatile

BIOS

RAM Chips



ROM chip

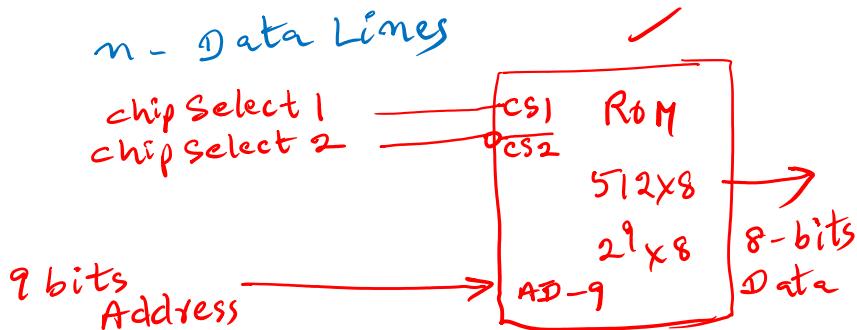


2^K words of n bits each

K - Address Lines

n - Data Lines

chip Select 1
chip Select 2



Registers and Memory Unit

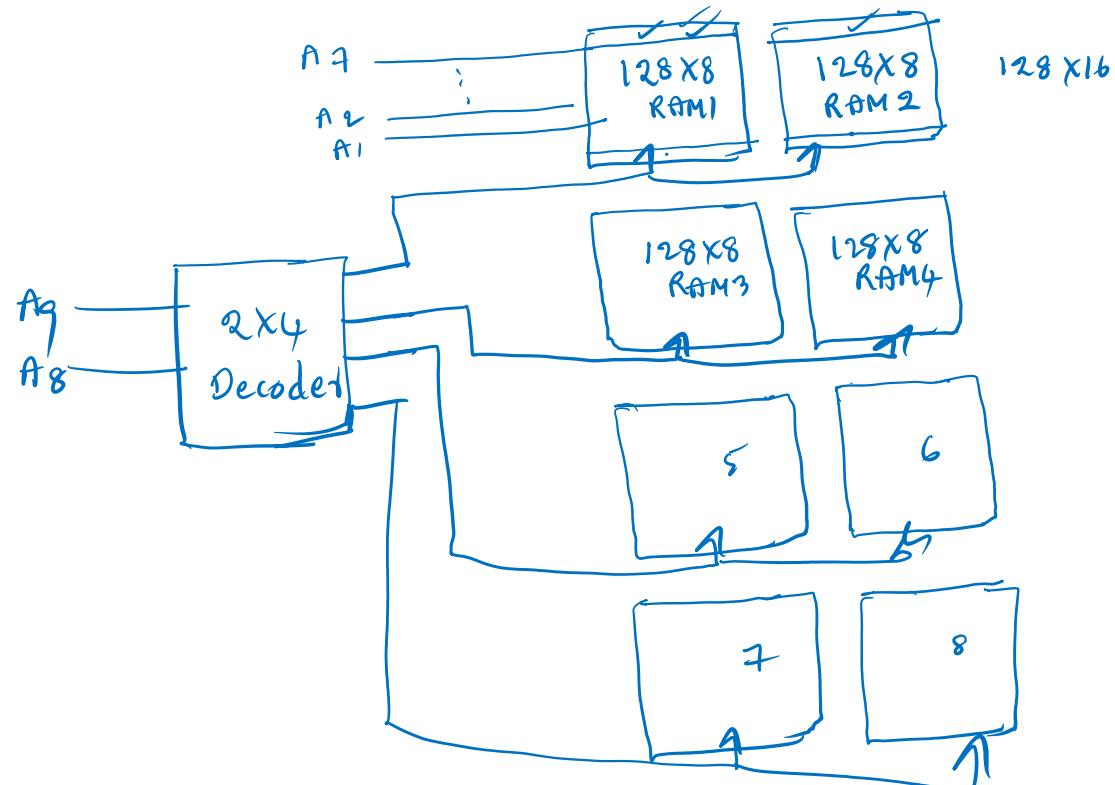
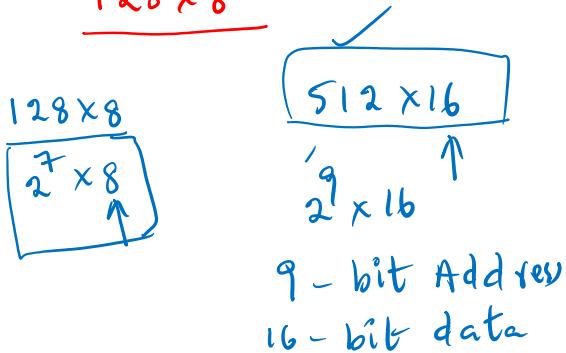
Function Table

$\overline{CS1}$	$\overline{CS2}$	RD	WR	Memory Function	Status of Data Bus
1	0	X	X	Inhibit	High Impedance
0	1	X	X	Inhibit	High Impedance
1	0	0	0	Inhibit	High Impedance
1	0	1	X	Mem. Read	Op's data from Mem
1	0	0	1	Mem. Write	Op's data to Mem
1	1	X	X	Inhibit	High Impedance

Registers and Memory Unit

Design of "512 x 16" RAM by using small RAM chips of size

128 x 8

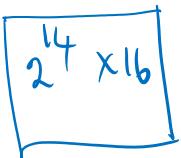


Registers and Memory Unit

$$16 \times 2 = 32$$

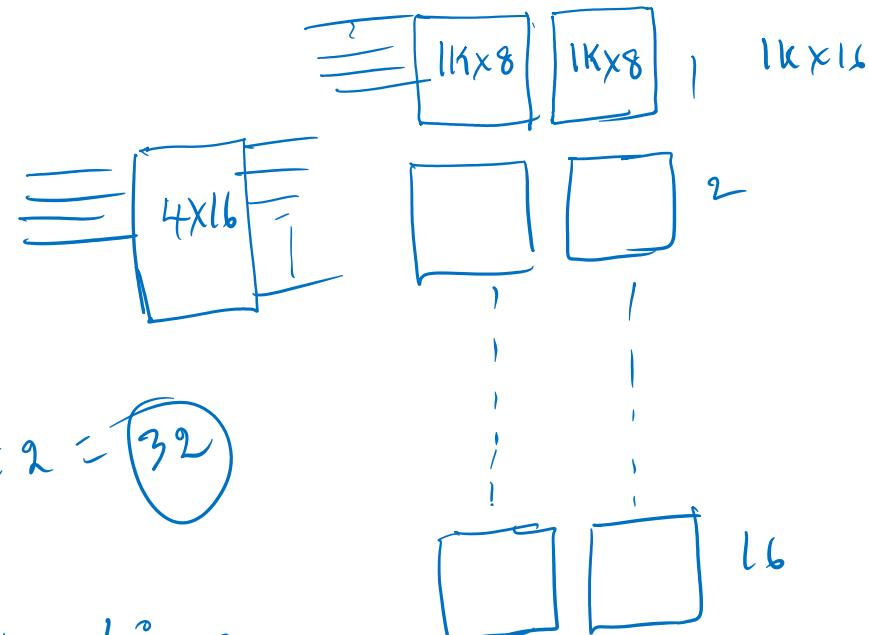
→ How Many RAM Chips are required to Provide a Memory Capacity of "16K X 16" by using RAM chips of size "1K X 8" ?

$$16K \times 16$$



$$2^{10} \times 8$$

16-bit Address



$$16 \times 2 = 32$$

(5)

2x4 Line
Decoders are Needed.