

Prep Smart. Score Better.

Computer Organization and Architecture

Problem solving of previous NET papers

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- M.Tech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD





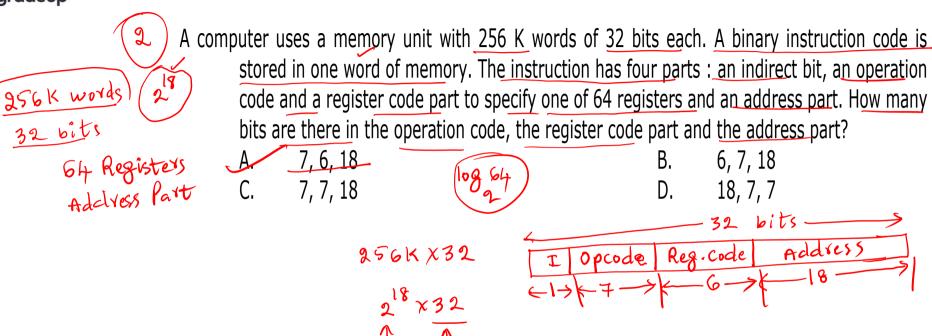
The Boolean expression $\overline{A}.B+A.\overline{B}+A.B$ is equivalent to

- A. A.B
- C. A.B

B.
$$A+B$$

$$\overline{A}B + A\overline{B} + AB$$
 $\overline{A}B + A (\overline{B} + B)$
 $\overline{A}B + A .$
 $(\overline{A} + A) (B + A)$
 $(\overline{A} + A) (B + A)$
 $(A + B)$





$$I=0$$
 (Direct)

I = I (Indived



(3

Consider the following x86 – assembly language instructions:

MOV AL, 153

Ollo ollo

NEG (AL)

The contents of the destination register AL (in 8-bit binary notation), the status of Carry Flag (CF) and Sign Flag (SF) after the execution of above instructions, are

AL = 0110 0110; CF = 0; SF = 0

B. $AL = 0110 \ 0111$; CF = 0; SF = 1

C. $AL = 0110 \ 0110$; CF = 1; SF = 1

1001 loo)

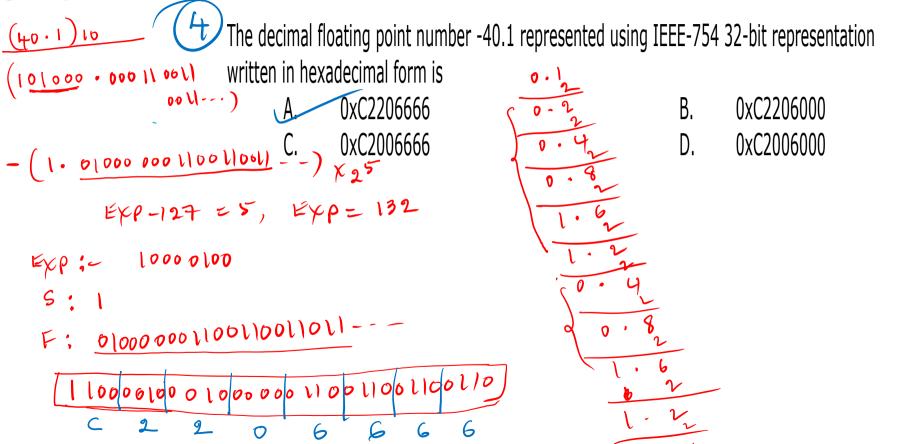
0110 011

D. $AL = 0110 \ 0111$; CF = 1; SF = 0

gradeup

Problem solving of previous NET papers

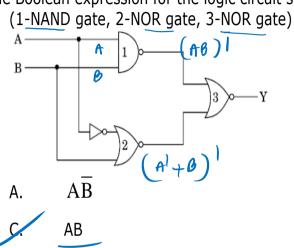
and







Find the Boolean expression for the logic circuit shown below:



$$(AB) + (A+B)$$

$$(AB) + (A+B)$$

$$ABA + ABB = 0 + AB$$

$$B. \overline{AB}$$

$$D. \overline{AB}$$



2 Sectors

n-bits

Consider a disk pack with 32 surfaces, 64 tracks and 512 sectors per pack. 256 bytes of data are stored in a bit serial manner in a sector. The number of bits required to specify a particular sector in the disk is

A. 18

V. 10

3. 1

. 2

Sol: - 32 x 64 x 512 x 256 Bytes

$$2^{5} \times 2^{6} \times 2^{9} \times 2^{8} = 2^{8}$$

25 x 96 x 29 sectors = 20 Sectors



21.4° 21.0° 21.0° 21.0° 20.5° 20.3° 26.5° 20.3°

Consider a system with 2 level cache. Access times of Level 1 cache, Level 2 cache and main memory are 0.5 ns, 5 ns and 100 ns respectively. The hit rates of Level 1 and Level 2 caches are 0.7 and 0.8, respectively. What is the average access time of the system ignoring the search time within the cache?

A. 35.20 ns C. 20.75 ns

D. 24.35 ns

$$Avg = 0.7 \times [0.5] + 0.3 \times [0.8 \times [5+0.5] + 0.2] \times [100+5] \times [100$$





A non-pipelined system takes 30ns to process a task. The same task can be processed in a foursegment pipeline with a clock cycle of 10ns. Determine the speed up of the pipeline for 100

10 10 10 10 tasks.

T₁ S₁ S₂ S₃ S₄ A. 3

T₂ S₁ S₂ S₃ S₄ C. 3.91

T₃ S₁ S₁ S₁ D. 2.91

Speed Up = Time taken for Non-pipeline

Time-taken for pipeline

MP = 30 × 100 = 3000 nos

4×10 +99×10

1030 ns



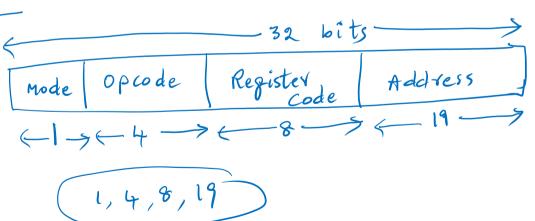
512 K words 2¹⁹ words 256 Register A computer uses a memory unit of 512 K words of 32 bits each. A binary instruction code is stored in one word of the memory. The instruction has four parts: an addressing mode field to specify one of the two-addressing mode (direct and indirect), an operation code, a register code part to specify one of the 256 registers and an address part. How many bits are there in addressing mode part, opcode part, register code part and the address part?

A. 1,3,9,19

B. 1,4,9,18

C. 1,4,8,19

D. 1,3,8,20





7 bits



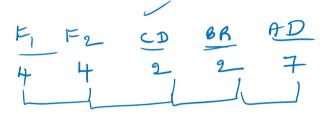
A micro instruction format has microoperation field which is divided into 2 subfields F1 and F2, each having 15 distinct microoperations, condition field CD for four status bits, branch field BR having four options used in conjunction with address field AD. The address space is of 128 memory words. The size of micro instruction is:

A. 19

B. 18

C. 17

D. 20







Given following equation:

$$(142)_b + (112)_{b-2} = (75)_8$$
, find base b.

$$\boxed{7\times8+5\times8^0}$$

$$(142)_{b} + (112)_{b-2} = (75)_{8}$$

$$b^{2} + 4b + 2 + (b-2)^{2} + (b-2) + 2 = 61$$

$$b^{2} + 4b + 2 + b^{2} + 4b + 4b + b^{2} + 6 = 61$$

$$2b^{2} + b + 6 = 61$$





The following program is stored in the memory unit of the basic computer. Give the content of accumulator register in hexadecimal after the execution of the program.



	Location	Instruction	
	010	CLA	AC=0
	011	ADD 016	AC = 0 + C1 A5 -
	012	BUN 014	
	013	HLT	
77	014	AND 017	-> 8184 (AC)
X6	015	BUN 013	
	016	C1A5	
9	017	93C6	•

- A. A1B4
- B. 81B4
- C. A184

D. 8184



Consider the equation $(146)_b + (313)_{b-2} = (246)_8$. Which of the following is the value of b?

A. 8
C. 10

$$1 \times b^{2} + 4b + 6 + 3(b-2)^{2} + (b-2) + 3$$

 $b^{2} + 4b + 6 + 3(b^{2} + 4 - 4b) + b-2 + 3 = 166$
 $b^{2} + 4b + 6 + 3b^{2} + 12 - 12b + 6 - 2 + 3' = 166$
 $4b^{2} - 7b + 19 = 166$

$$2\times8^{2}+4\times8+6$$

$$128+32+6$$

$$(166)_{10}$$

(246)₈





How many address lines and data lines are required to provide a memory capacity of 16K × 16?

- B. 16, 16
- D. 4, 16

16K X16

K - Address

2 × n

14 - Address 16 - data





In computers, subtraction is generally carried out by

- A. 9's complement
- 10's complement

1's complement 2's complement

2's Complement

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WX + WY + X

 $(\omega+1)x+\omega y$

the following Declary equations:

Consider the following Boolean equations:

$$\checkmark$$
 i. $wx + w(x + y) + x(x + y) = x + wy$

wtw (xy)

i is true

$$wx + w(x+y) + x(x+y) = x + wy$$

$$wx + wx + wy + x + xy \qquad w\overline{x}yy + \overline{w}\overline{x}y$$

$$wx + wy + x[1+y] \qquad w\overline{x}y + \overline{w}\overline{x}y$$