



Computer Organization and Architecture

CPU Organization Part-1

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



CPU Organization Part-1

more GPR's
Efficient

- { (1) single AC organization [one]
- (2) General Register's orgn. [three (or) Two Addresses]
- (3) Stack-organization. [zero]

General Purpose Registers

$$R_0 \rightarrow 000\ 000$$

$$R_1 \rightarrow 000\ 001$$

$$R_2 \rightarrow 000\ 010$$

$$R_3 \quad |$$

$$| \quad |$$

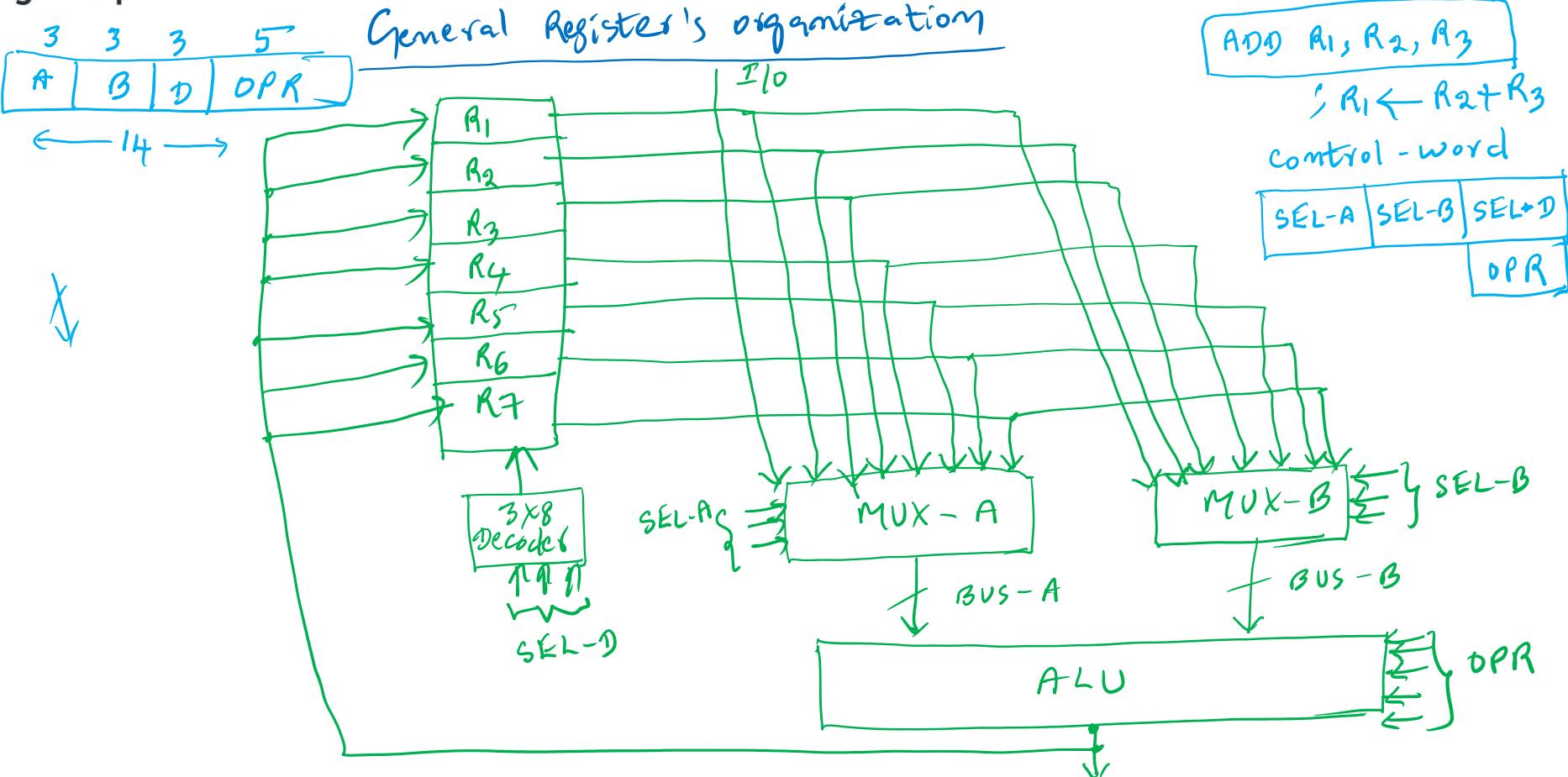
$$R_{63} \rightarrow 111\ 111$$

$$\begin{array}{c} \text{ADD} \\ \diagdown \quad \diagdown \\ R_1, R_2, R_3 \\ \diagup \quad \diagup \\ \text{---} \end{array} ; R_1 \leftarrow R_2 + R_3$$

$$\text{ADD } R_1, X$$

$$; R_1 \leftarrow R_1 + M[X]$$

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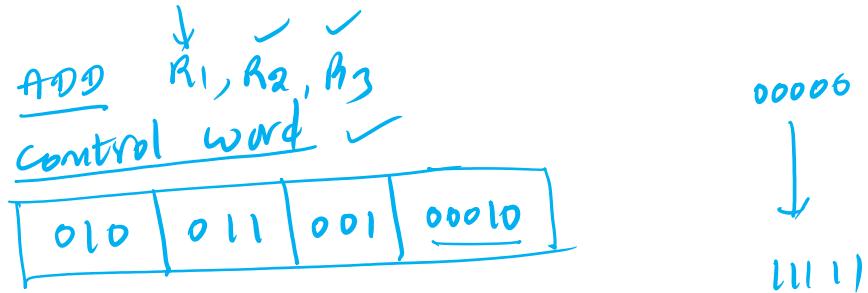
CPU Organization Part-1

$$R_1 = 001$$

$$R_2 = 010$$

⋮

$$R_7 = 111$$



Example 2

SUB R₁, R₂ ; R₁ ← R₁ + R₂ ✓

SEL-A	SEL-B	SEL-D	OPR
001	010	001	00011

CPU Organization Part-1

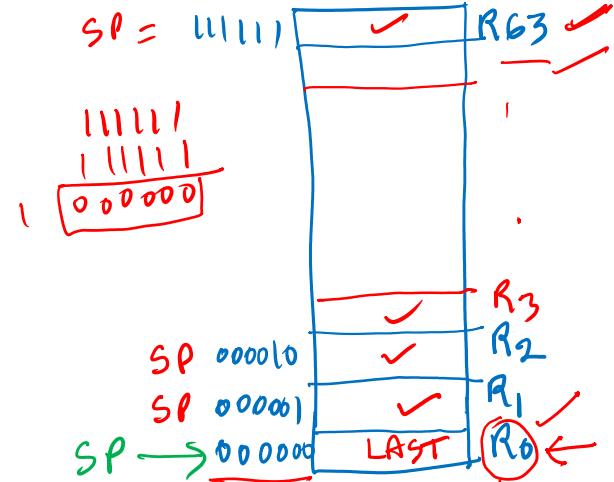
000 000 3
111111
111111

- (1) Register Stack
- (2) Memory Stack

$\log_2^{64} = 6$ bits
LIFO

Stack - Organization

Register's Stack



SP (Points to the Tos)

EMPTY ← 1 (stack is empty)
FULL ← 0 (stack is not full)
(0-1)

Push

SP ← SP + 1

M[SP] ← DR

If (SP=0) the stack is full.
FULL ← 1

Pop

DR ← M[SP]

SP ← SP - 1

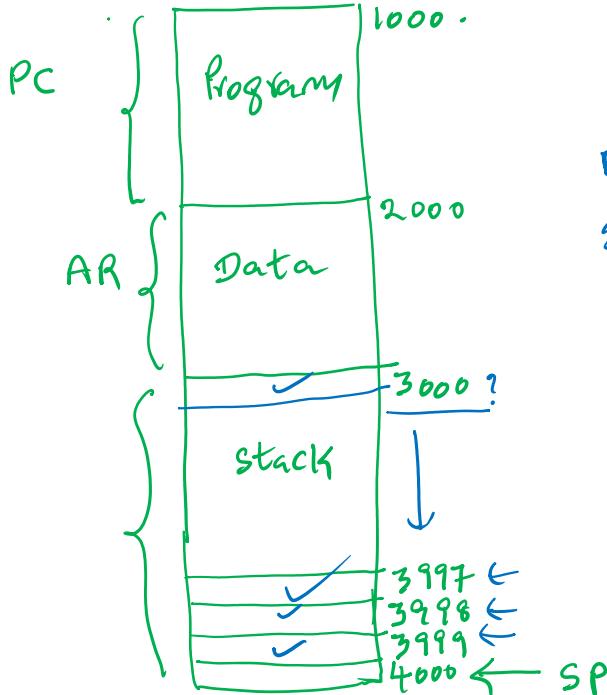
If (SP=0) the stack is empty
EMPTY ← 1

CPU Organization Part-1

SP



Memory Stack .



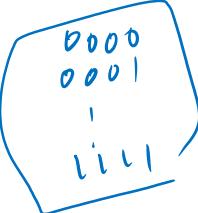
Push

$SP \leftarrow SP - 1$ }
 $M[SP] \leftarrow DR$
 If ($SP = 3000$) then stack overflow.

Pop

$DR \leftarrow M[SP]$ }
 $SP \leftarrow SP + 1$
 If ($SP = 4000$) then stack is empty.

CPU Organization Part-1

!  mode
 $\log_2 16 = 4$
 $\log_2 8 = 3$
 1 = 0 (Direct)
 2 = 1 (Indirect)

1. A digital computer has two address instructions which has register and memory addresses. If there are 32 registers and one Megabyte of memory ,and it is able to perform 16 operations and has 8 different addressing modes. Then the size of binary instruction code in bits is ?

- A. 24 bits
- B. 20 bits
- C. 32 bits
- D. 64 bits

$$\frac{1 \text{ MByte}}{2^{20}}$$

$$\boxed{32 \text{ Registers}} = 2^5 \text{ Registers}$$

$$1 \text{ Megabyte} = \underline{2^{20}}$$

16 operations

$$\frac{20}{\begin{smallmatrix} 5 \\ 4 \\ 3 \\ 32 \end{smallmatrix}}$$

Mode	Operation Code	Reg.Opnd	Mem.Opnd
← 3 →	4	5 →	→ 20

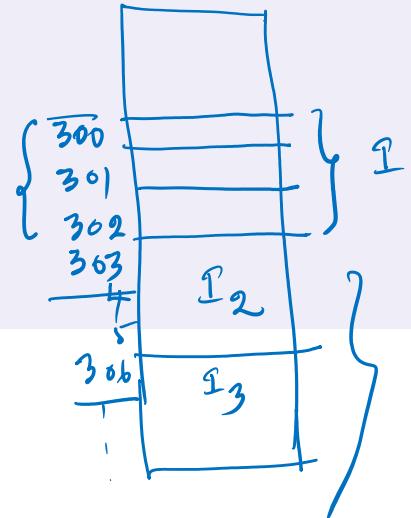


CPU Organization Part-1

24-bits (3 Bytes)

2. A CPU has 24 bit instructions . A program stored at address 300 in decimal. Which of the following is the legal program counter?

- A. 400
- B. 500
- C. 600
- D. 700



CPU Organization Part-1

Two - Address

One - Address

16 - bits

(16-12)
12

3 . A computer has 16-bit instructions and 6-bit addresses. If there are 12 two address instructions, then how many one address instructions can be formulated ?

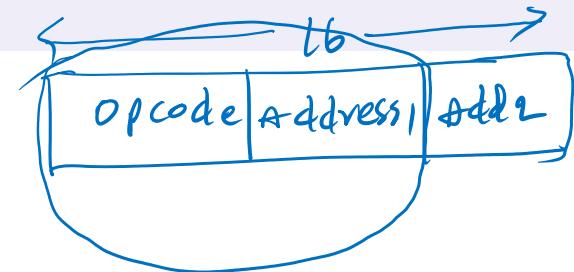
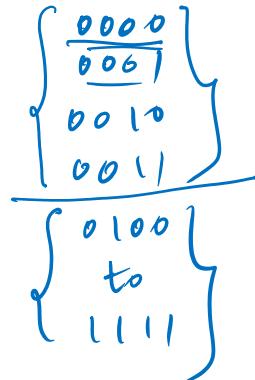
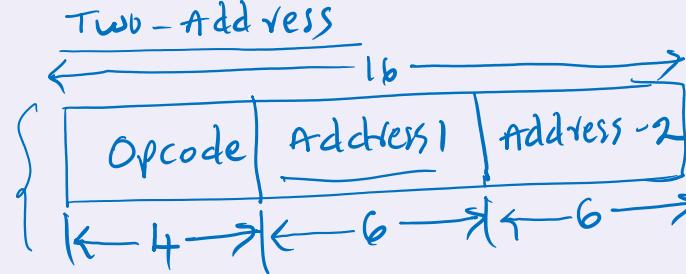
- A. 256
- B. 128
- C. 4
- D. 64

$\left\{ \begin{array}{l} 0000 \\ 0001 \\ 0010 \\ \downarrow \\ 1111 \end{array} \right.$

$$4 \times 2^6$$

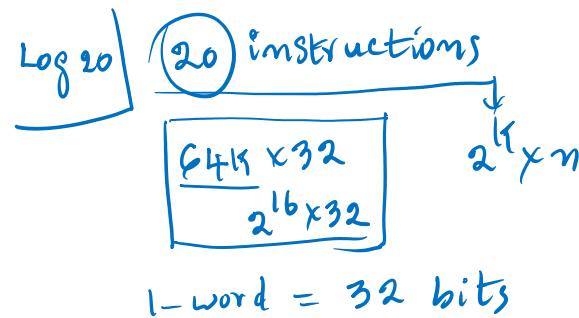
$$4 \times 2^6$$

256



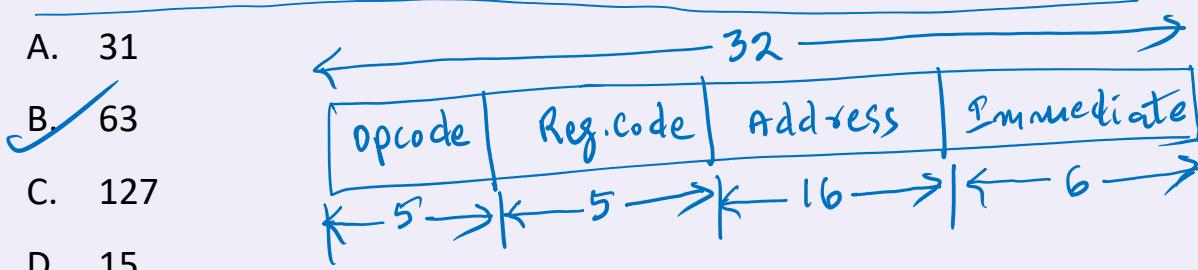
Opcode .

CPU Organization Part-1



4. Consider a computer system with an instruction set of 20 and memory size of 64 Kx 32, each instruction is of one word in size. Instruction has four parts, An opcode , A Register code part specify one out of 32 registers, An address part and an immediate operand. What is the maximum value of the immediate operand if it is an unsigned integer?

- A. 31
- B. 63
- C. 127
- D. 15



$$\log_2 \frac{32}{2} = 5$$

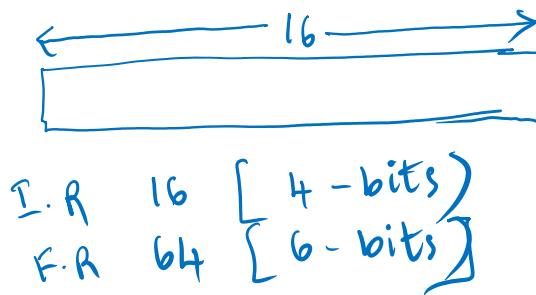
$$32 - (5 + 5 + 16) = 6$$

$$32 - 26 = \underline{6 \text{ bits}}$$

(000000)
(111111)

111111 $(2^6 - 1)$
 $64 - 1 = 63$

CPU Organization Part-1



5. A processor has 16 integer registers (R_0, R_1, \dots, R_{15}) and 64 floating point registers (F_0, F_1, \dots, F_{63}). It uses a 2-byte instruction format. There are four categories of instructions: Type-1, Type-2, Type-3, and Type-4. Type-1 category consists of four instructions, each with 3 integer register operands (3Rs). Type-2 category consists of eight instructions, each with 2 floating point register operands (2Fs). Type-3 category consists of fourteen instructions, each with one integer register operand and one floating point register operand (1R + 1F). Type-4 category consists of N instructions, each with a floating point register operand (1F).

The maximum value of N is _____.

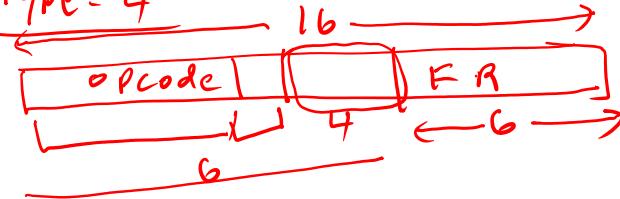
$$\begin{aligned} \text{Type1} &\rightarrow 3\text{IR} \quad (4) \\ \text{Type2} &\rightarrow 2\text{FR} \quad (8) \\ \text{Type3} &\rightarrow 1\text{IR} + 1\text{FR} \quad (14) \\ \text{Type4} &\rightarrow 1\text{FR} \quad (N) \end{aligned}$$

CPU Organization Part-1

$$2^4 = 16$$

$$16 - 4 = 12 \text{ Left over.}$$

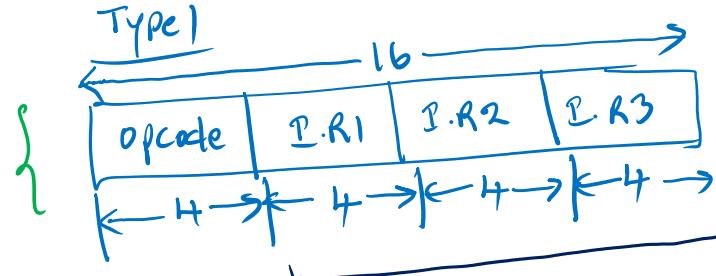
Type-4



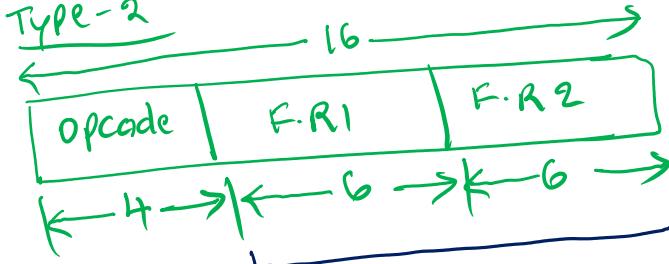
$$2 \times 2^4 = 32$$

$$N = 32$$

Type-4
instructions

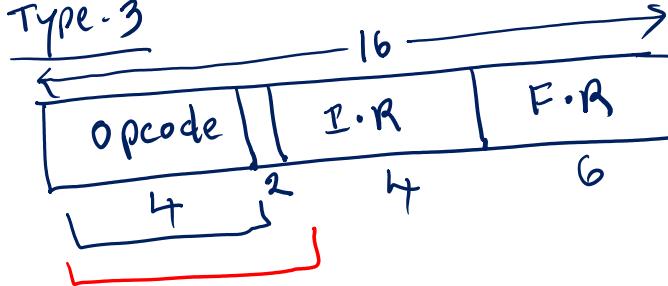


Type-2



$$12 - 8 = 4 \text{ Left over}$$

Type-3



$$4 \times 2^2 = 16$$

16 opcodes

$$16 - 14 = 2 \text{ Left over.}$$

CPU Organization Part-1

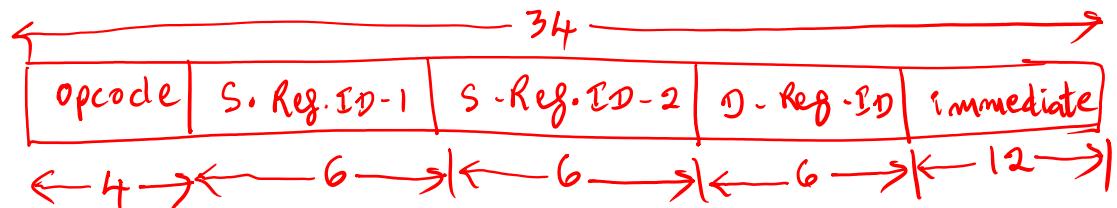
64 Registers

$$\log_2 64 = 6$$

$$100 \times 5 = 500$$

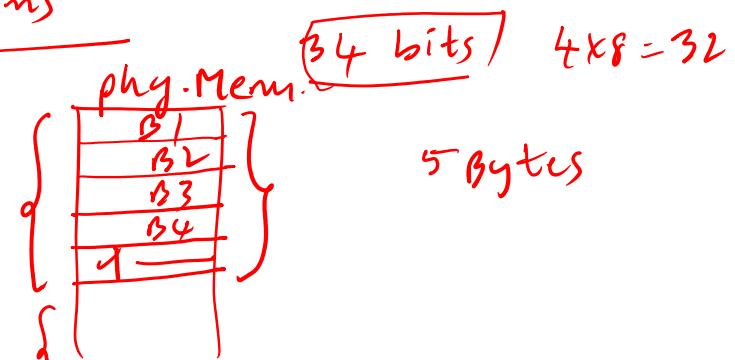
12
Log 12

6. Consider a processor with 64 registers and an instruction SET- of size twelve. Each instruction has five distinct fields, namely, opcode, two source register identifiers, one destination register identifier, and a twelve-bit immediate value. Each instruction must be stored in memory in a byte-aligned fashion. If a program has 100 instructions, the amount of memory (in bytes) consumed by the program text is?



100-instructions

500



CPU Organization Part-1

7. For computer based on three-address instruction formats, each address field can be used to specify which of the following :

- {
 S1: A memory operand ✓
 S2: A processor register ✓
 S3: An implied accumulator register ✗
 } one address
- A. Either S1 or S2 opcode add addr addr
- B. Either S2 or S3
- C. Only S2 and S3
- D. All of S1, S2 and S3

CPU Organization Part-1

Clock frequency = Hz

$$\text{cycle} = \frac{1}{\text{frequency}}$$

8. Consider two processors P1 and P2 executing the same instruction set . Assume that under identical conditions , for the same input a program running on P2 takes 25% less time but incurs 20% more CPI (Clock cycles per instruction) as compared to the program running on P1. If the clock frequency of P1 is 1 GHz then the clock frequency of P2 is ?

✓
1 GHz

$$= \frac{1}{10^9} \text{ sec} = 1 \text{ n.s}$$

P₁

$$\underline{1 \text{ cycle time} = 1 \text{ n.s}}$$

P₂ = ?

P₂ 25%. Less time

P₂ 20%. More CPI

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$$\frac{3.75 \times 10^{-1}}{600}$$

P_2

1.6 GHz

Sol :- Let us Assume that P_1 takes 5 cycles.

$$\text{Time taken} = \underline{5 \text{ n.s}}$$

$$P_2 \text{ takes } 5 + 0.2(5) = \underline{6 \text{ cycles}}$$

$$P_2 \text{ takes } 5 - 0.25(5) = \underline{3.75 \text{ n.s}}$$

$$6 \text{ cycles} = 3.75 \text{ n.s}$$

$$6 \times \frac{1}{x \text{ GHz}} = 3.75$$

$$x = 6 / 3.75 = 1.6$$