



# Computer Organization and Architecture

Memory  
Management  
hardware

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- M.Tech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD

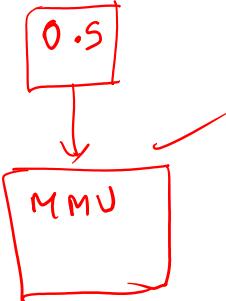


# Memory Management hardware

Logical Address

→ Address generated by CPU

LAS :- the set of all logical addresses,



physical address

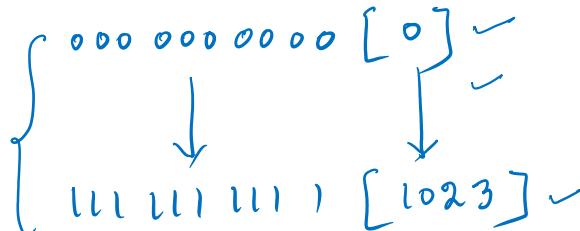
→ Actual Address of physical memory.

PAS :- the set of all physical addresses

Process - P [ 1 KByte ]

$2^{10}$  Bytes

10-bit Address



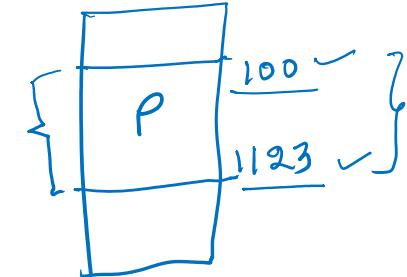
phy. Mem : 1 M Bytes

$2^{20}$  Byte

$[0, 1 \dots 2^{-1}]$

MMU

100
20
120

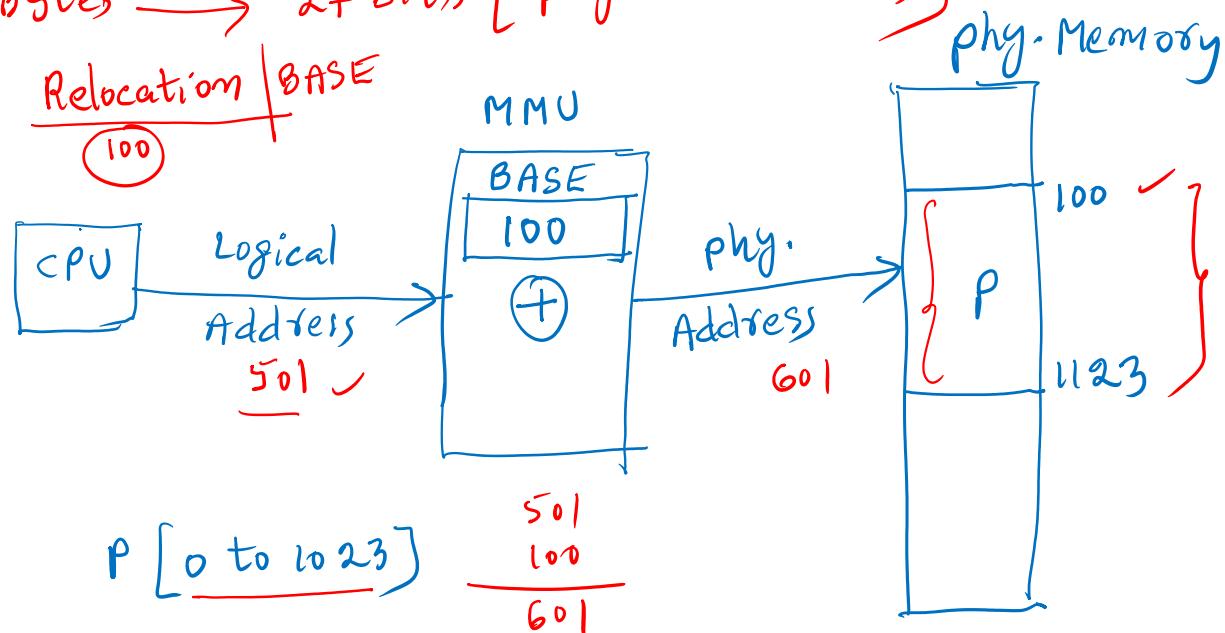


# Memory Management hardware

Example :- If the size of Process is 64 KBytes and phy. Memory size 128 MBytes.

$$64K = 2^6 \cdot 2^{10} = 2^{16} \text{ Bytes} \rightarrow 16 \text{ bits [Logical Address]}$$

$$128MB = 2^7 \cdot 2^{20} = 2^{27} \text{ Bytes} \rightarrow 27 \text{ bits [Physical Address]}$$



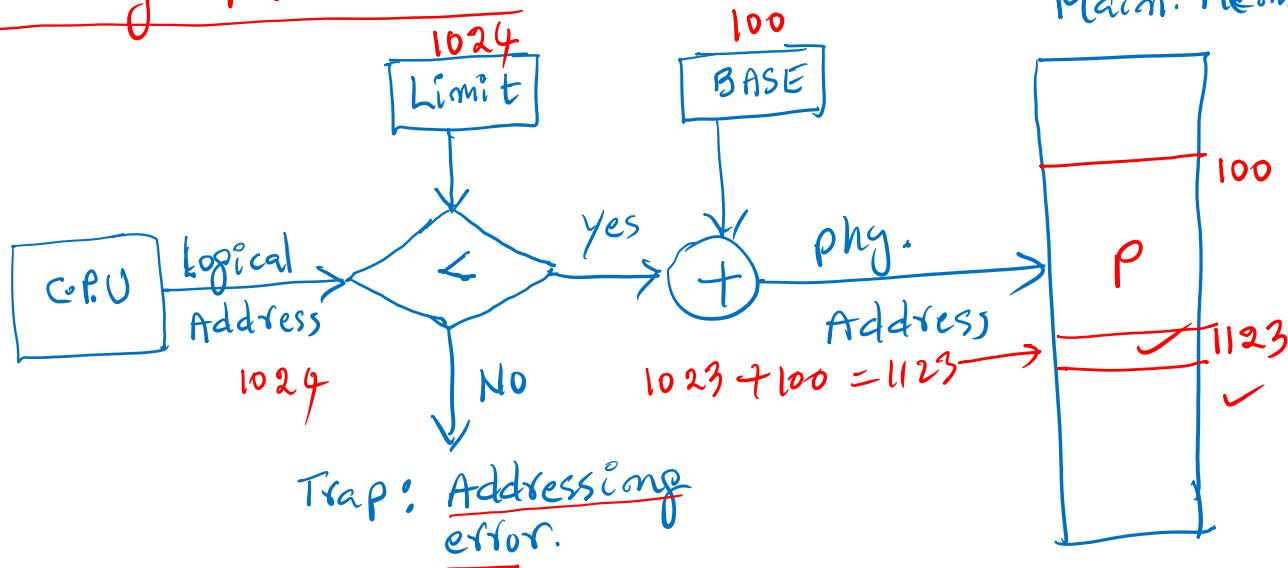
# Memory Management hardware

1 KB

$$P = 1024 \text{ Bytes}$$

(0 to 1023)

## Memory - Protection



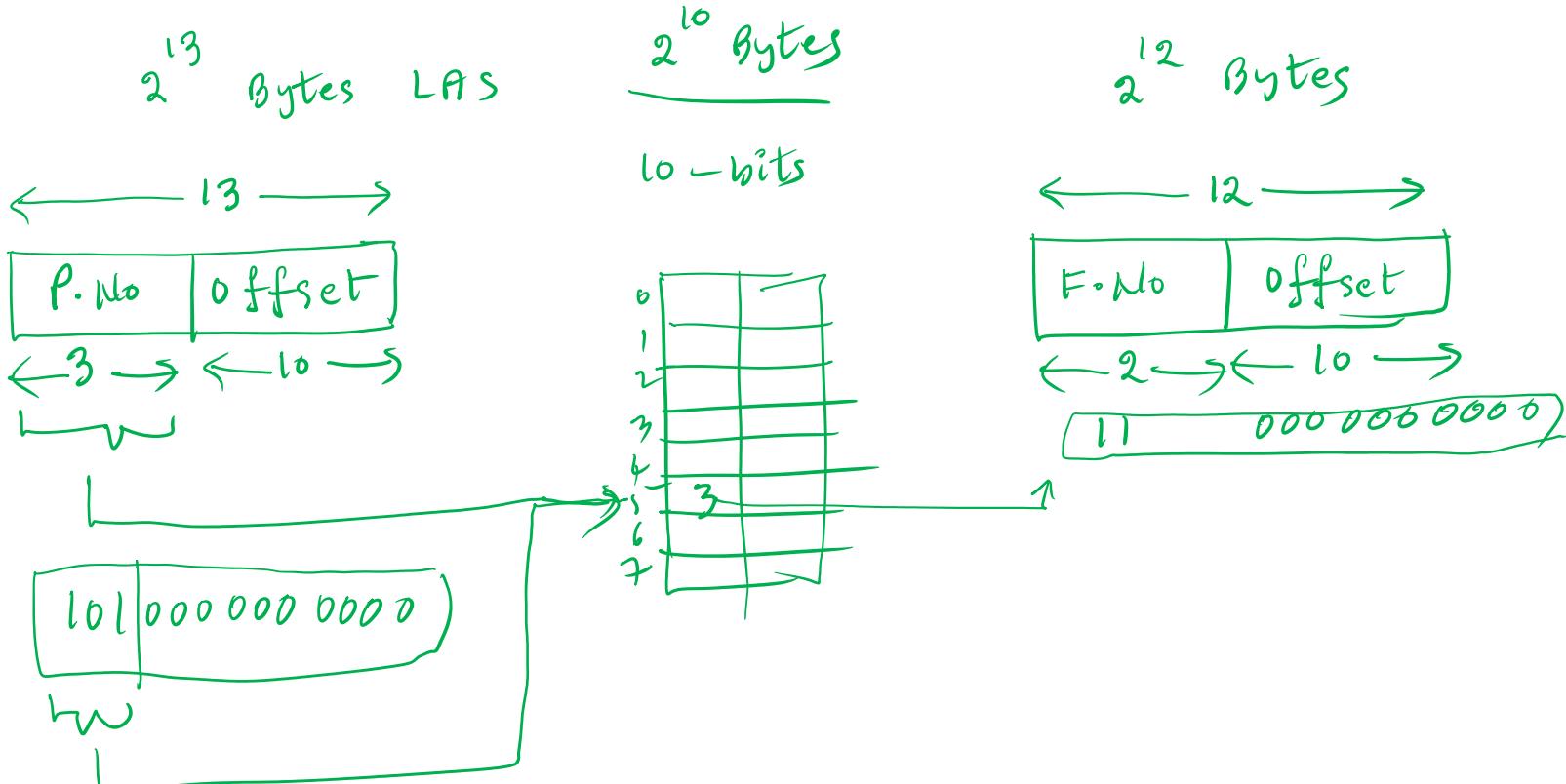
Main. Memory

$$1024 < 1024 \times$$

1023

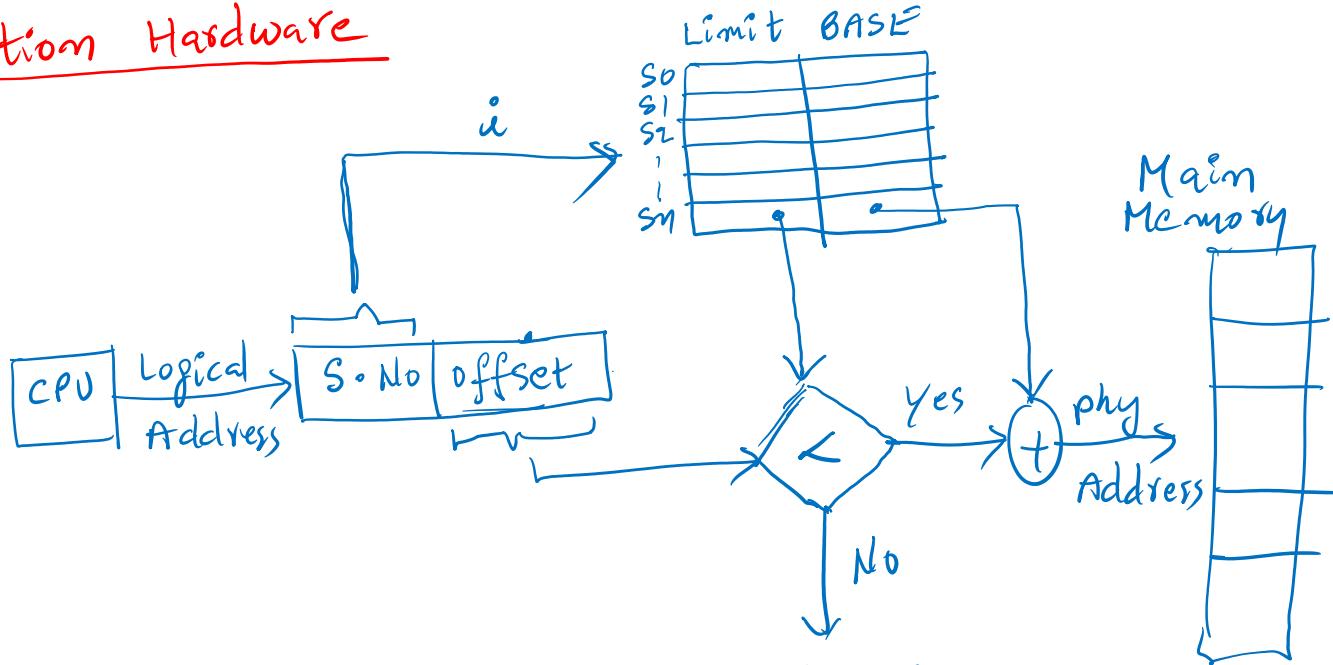
Limit :- The range of Logical Addresses  
[The length of the Process]

# Memory Management hardware



# Memory Management hardware

## Segmentation Hardware

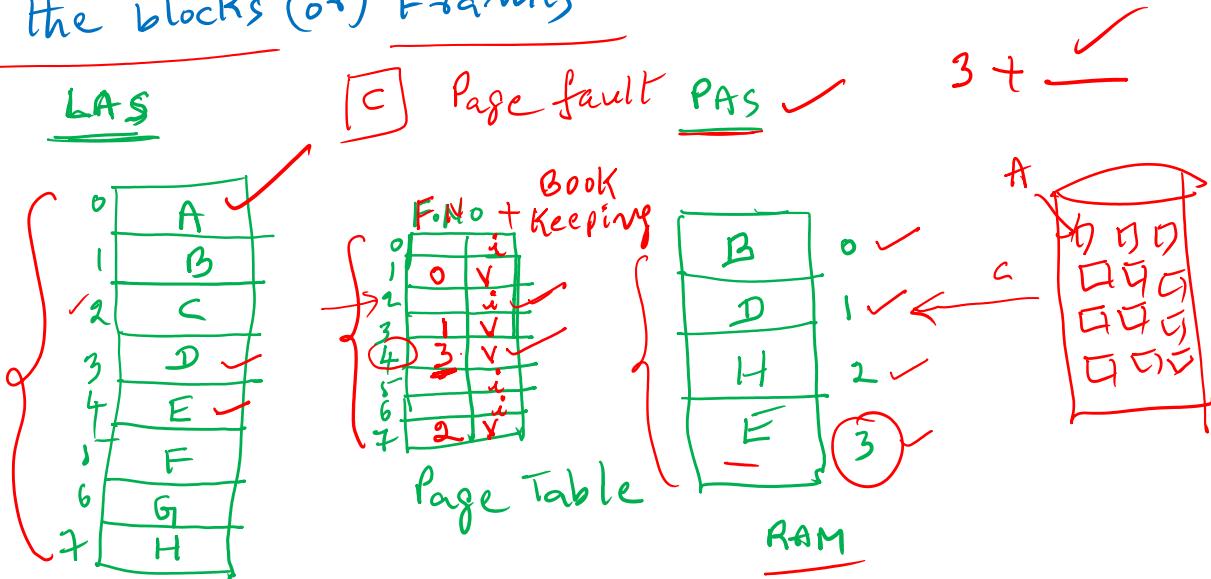


Trap : Addressing error.

# Memory Management hardware

## Paging

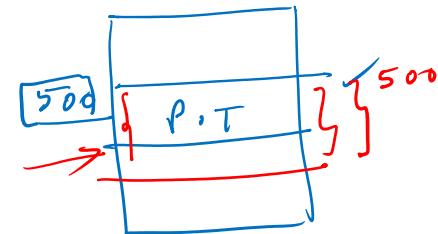
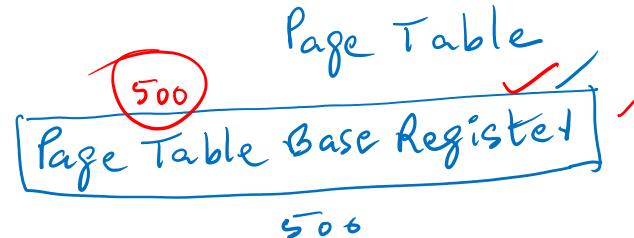
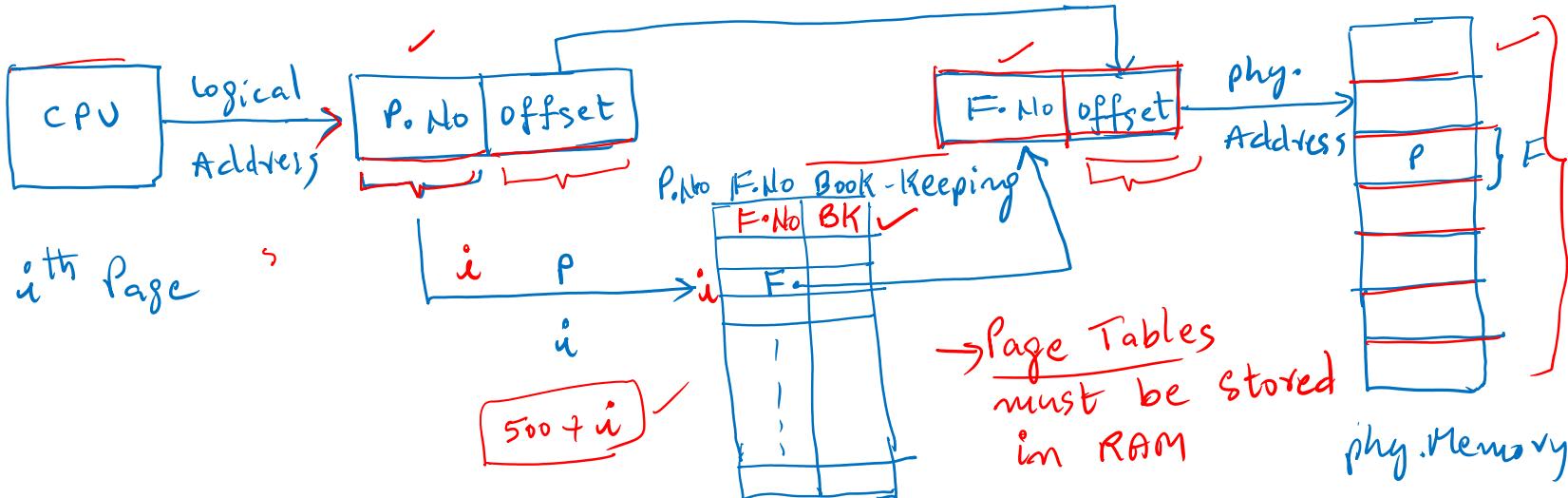
- It is the process of dividing the logical address space of a process into equal sized partitions called the pages.
- phy. Address Space is divided into equal sized partitions called the blocks (of) Frames



# Memory Management hardware

## Paging Hardware.

Y  
i  
Count  
Time



# Memory Management hardware

8KB bytes

13  
2-Bytes

P

13 bits  $\rightarrow$  12 bits

A diagram of a 64-bit pointer. It consists of two 32-bit fields: 'base' and 'offset'. The 'base' field contains the value 101. The 'offset' field contains the value 0000000000.

L5

## Example

$$P = \boxed{8\text{ KBytes}}$$

13 - bits

Page Size = 1KB

$$= \frac{2^{10}}{2} \text{ bytes}$$

Memory = 4 Kbytes

2<sup>12</sup> Bytes

The diagram illustrates the Addressing Structure (LAS) and Page Size.

**Addressing Structure (LAS):**

- A Logical Address (LA) is divided into two fields: P. No. and offset.
- The width of the LA is  $m$ .
- The width of the P. No. field is  $n$ .
- The width of the offset field is  $m-n$ .
- The total width of the LA is  $m$ .

**Page Size:**

- A page is represented as a box with fields P. No. and offset.
- The width of the page is  $l_3$ .
- The width of the P. No. field is  $l_0$ .
- The width of the offset field is  $l_1$ .
- The total width of the page is  $l_3$ .

**Mapping:**

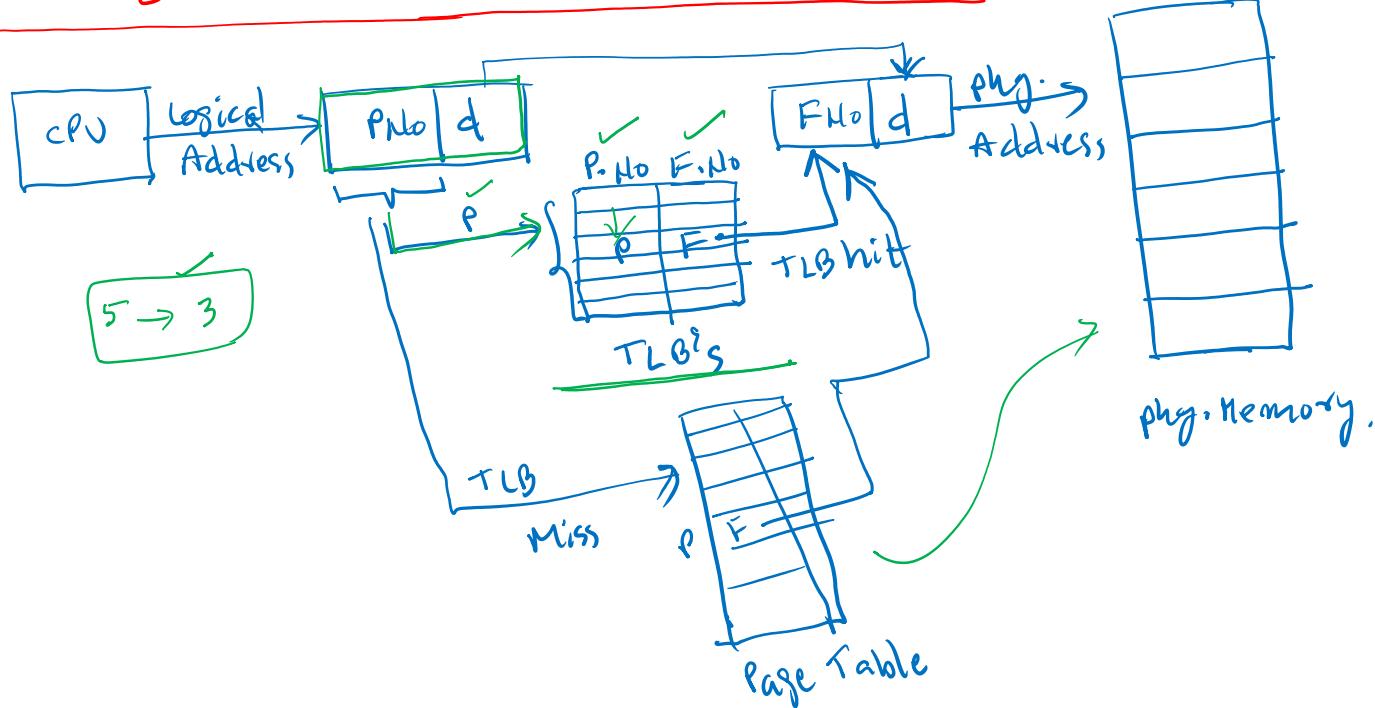
- The P. No. field of the LA is compared with the P. No. field of the page.
- If they match, the offset field of the LA is used as the offset field of the page.
- If they don't match, the LA is mapped to a frame number (F No.) and an offset.
- The F No. is compared with the P. No. of the page.
- If they match, the offset field of the LA is used as the offset field of the page.
- If they don't match, the LA is mapped to a frame number (F No.) and an offset.
- The F No. is mapped to a frame (F N.B.Y) and the offset is mapped to a page (P.S).
- The page is then mapped to memory locations 00, 01, 10, 11.

# Memory Management hardware

Note :- If normal memory access takes K-n.s, then paged memory access takes  $2K$  nanoseconds.

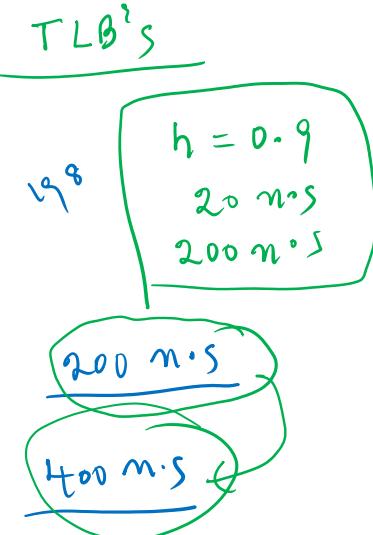
200 n.s  
400 n.s

## TLB [Translation Look-Aside Buffers]



# Memory Management hardware

- \* Assume that a single level paging uses TLB's to reduce effective access time. If TLB access takes 20 n.s, and main memory access takes 200 n.s. If TLB hit ratio is 90%, then what is the effective memory access time?



Assume that no page faults

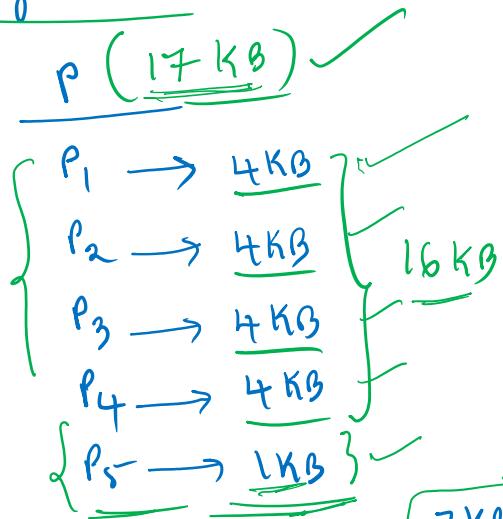
$$\begin{aligned}
 \text{So} ;-\text{ EMT} &= \frac{h}{\uparrow} \left[ \underset{\downarrow}{\text{TLB Access}} + \underset{\downarrow}{\text{Main Mem. Access}} \right] \\
 &\quad + (1-h) \left[ \underset{\uparrow}{\text{TLB Access}} + \underset{\downarrow}{2 \times \text{Main Mem. Access}} \right] \\
 \text{EMT} &= \frac{0.9 \times [20 + 200]}{\uparrow \downarrow} + \frac{0.1 \times [20 + \frac{200}{\uparrow} + \frac{200}{\downarrow}]}{\uparrow \downarrow} \\
 &= \frac{0.9 \times 220}{\uparrow} + 0.1 \times 420 \\
 &= \frac{9 \times 22 + 42}{198 + 42} = \boxed{240 \text{ n.s}}
 \end{aligned}$$

# Memory Management hardware

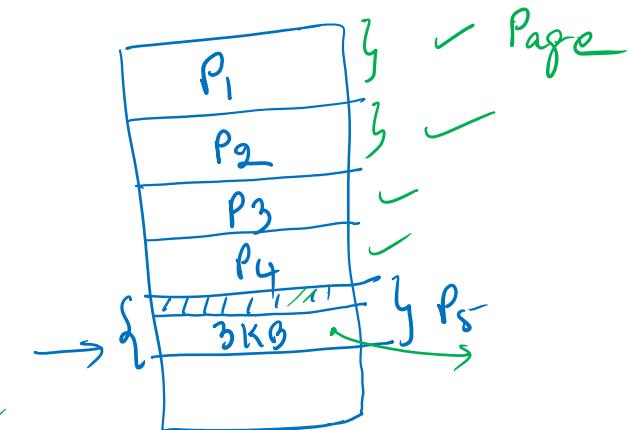
## Internal Fragmentation

Unused memory within a partition is called internal fragmentation.

Process - 17 KB  
Page Size = 4 KB



Paging is suffering from internal fragmentation

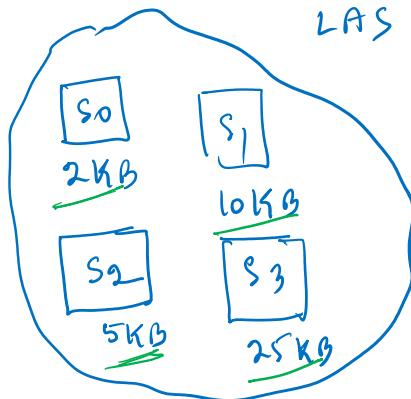


3 KB of internal fragmentation.

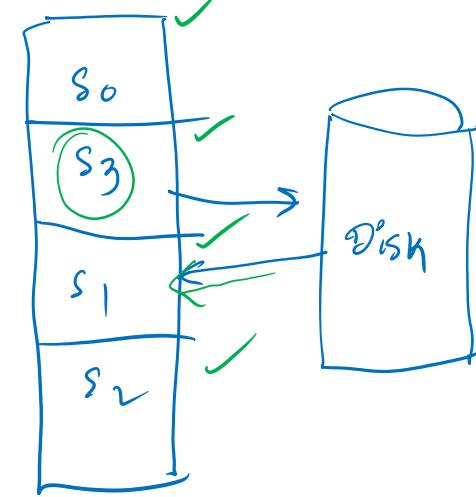
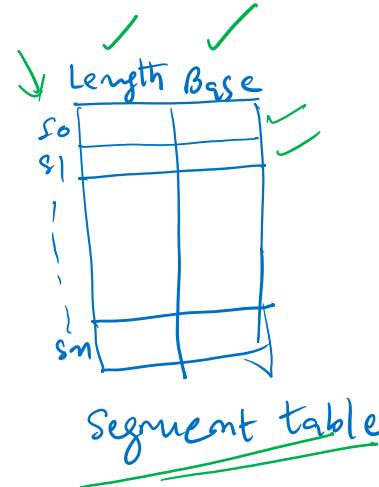
# Memory Management hardware

size of segment  
phy. Mem. Address  
(smallest)

## Segmentation



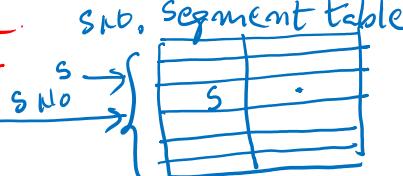
Non-Contiguous Allocation



→ It Divides the LAS into Variable sized partitions

# Memory Management hardware

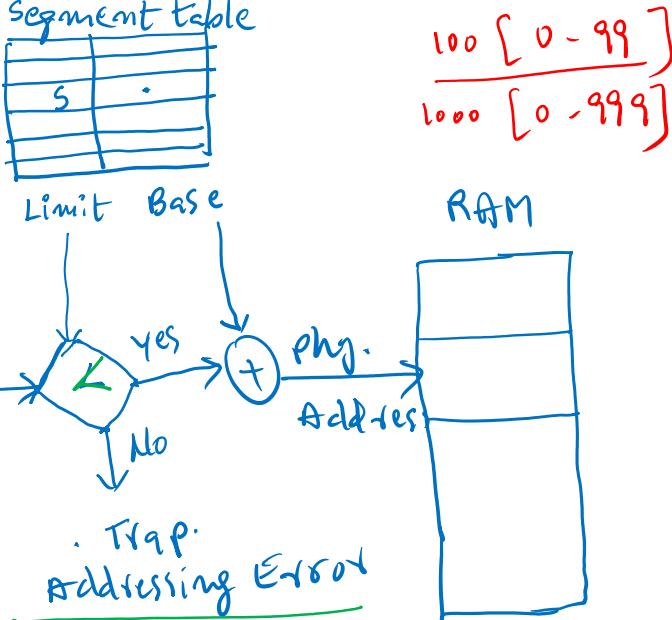
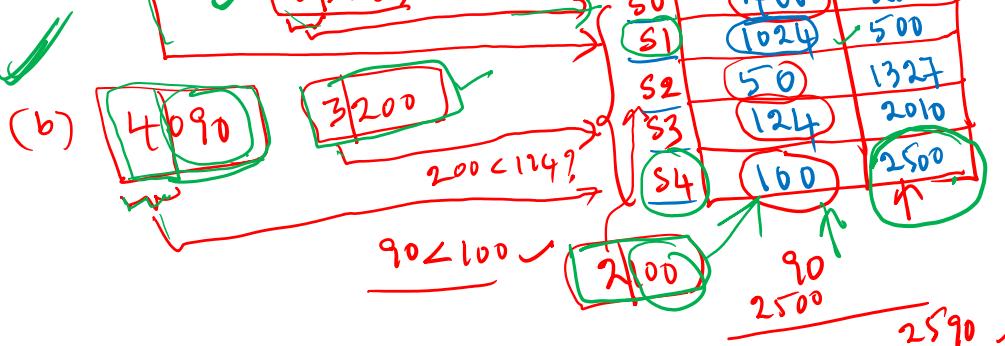
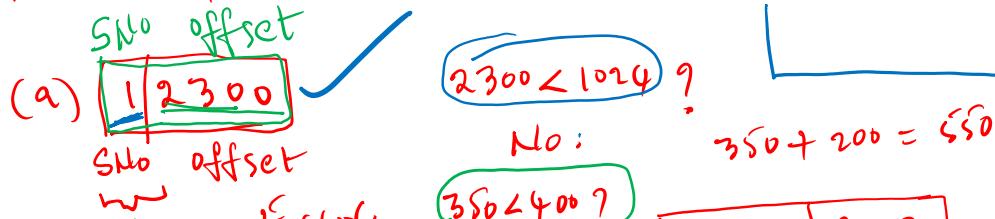
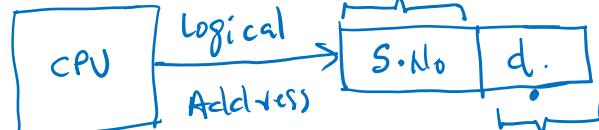
## Segmentation Hardware



(5)

(10)

0, 1, 2, ..., 9



→ what are the phys. addresses for the following logical addresses?

- (a)     
- (b)     Error.
- (c)    Error.

# Memory Management hardware

H/w

→ ① A Paging system uses TLB's whose access is 10 n.s.  
Memory access takes 150 n.s. If Effective memory  
access time is 200 n.s, then what should be  
the hit ratio of TLB ? [ Assume Single Level  
Paging is used ]

②

Assume that Process size is 100 KBytes and  
Page size is 8KBytes, what will be the  
internal fragmentation ?

# Memory Management hardware

Sol. ① TLB Access = 10 n.s

Main Memory Access = 150 n.s

E.M.T = 200 n.s      TLB hit ratio = ?

$$\begin{array}{c} \text{us} \\ \text{ns} \end{array} \begin{array}{c} 110 \\ 10 \\ \hline 50 \end{array} \begin{array}{c} (0.73) \\ \text{ns} \\ \text{us} \end{array}$$

$$200 = x[10 + 150] + (1-x)[10 + 150 + 150]$$

$$200 = 160x + 310 - 310x$$

$$110 = 150x$$

$$x = \frac{110}{150} = \frac{11}{15} .$$

0.73

73 %

# Memory Management hardware

Sd. Q.No. 2

4 kB of Internal  
Fragmentation.

Process Size = 100 kB.

Page Size = 8 kBytes.

Internal fragmentation = ?

$$12 \times 8 = 96 \text{ kBytes}$$

$$12 \text{ Pages} \rightarrow 12 \times 8 \text{ kB} = \underline{96 \text{ kB}}$$

$$13^{\text{th}} \text{ Page} = 4 \underline{\text{kB}}$$

