



Computer Organization and Architecture

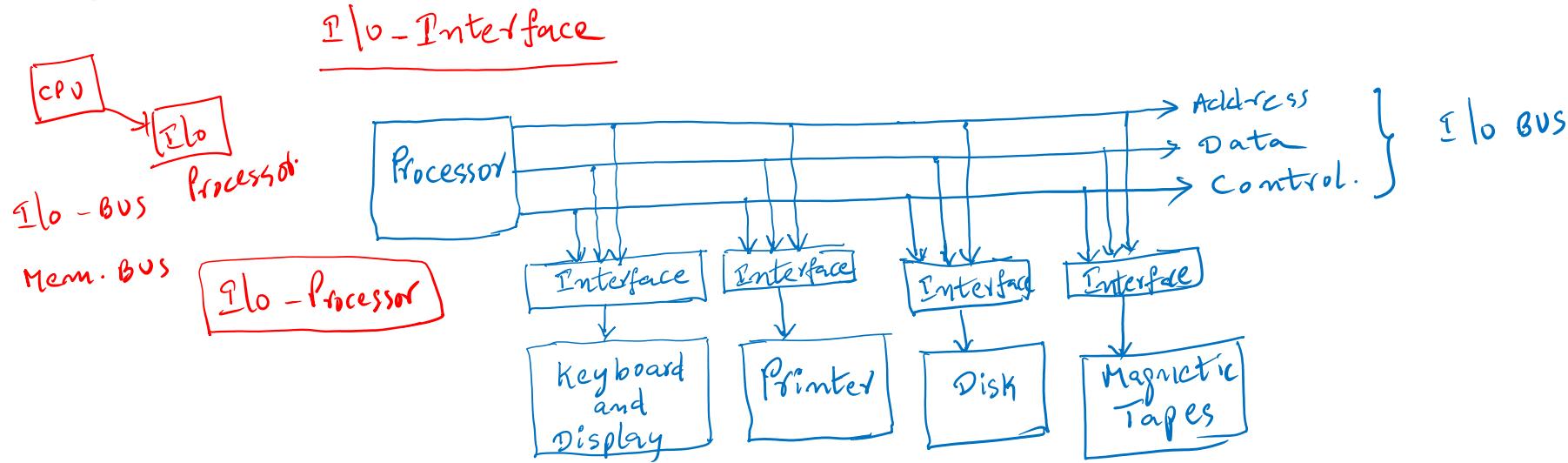
I/O organization part-1

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



I/O organization part-1



I/O Versus Memory BUS

- {
- (1) use separate BUS for memory and I/O
- (2) use one bus for both memory and I/O but we can have separate control lines
- (3) use common bus for both Mem and I/O with common control lines.

I/O organization part-1

Isolated I/O and Memory mapped I/O

CPU - Address Space

$$8086 - 2^{20}$$

I/O (Isolated)

Memory Mapped I/O.

Read : —

Write : —

Interface Unit

{ Buffers
 Registers
 Control Registers
 Status Registers
 Chip.

Isolated I/O

Mem. Read

Mem. write

I/O - Read

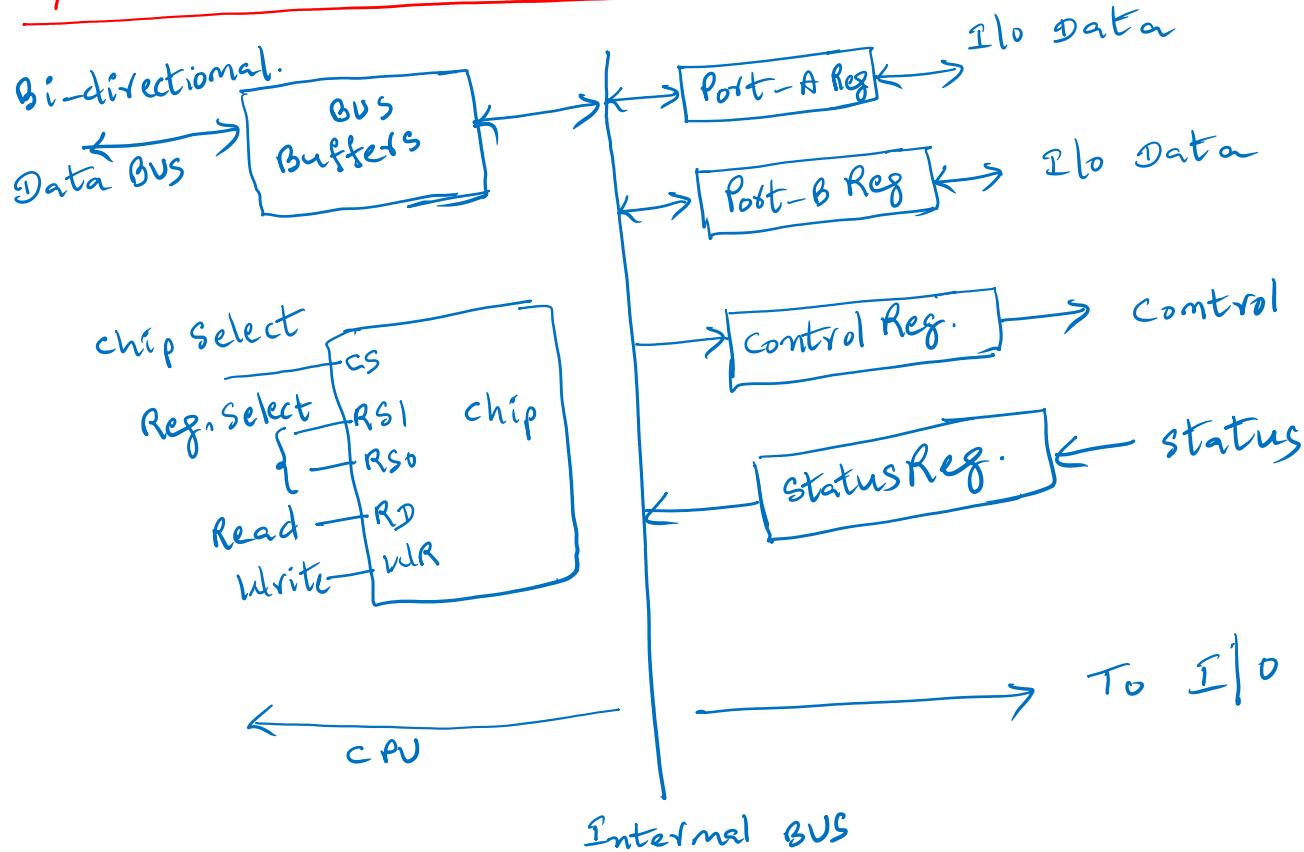
I/O - write

Function Table

CS	RS1	RS0	Register Selected
0	X	X	High Impedance
1	0	0	Port-A
1	0	1	Port-B
1	1	0	Control Register
1	1	1	Status Register

I/O organization part-1

Typical I/O - Interface Unit



I/O organization part-1

ISR

Initialize the address register - 1

500

Initialize the count to 500 - 1

LOOP: Load a byte from device - 2 ✓

Store in memory at address given by address register 2

Increment the address register 1 -

Decrement the count 1 -

If count != 0 go to LOOP 1 -

Interrupt I/O

$$2 + 500 [2 + 2 + 1 + 1 + 1]$$

$$2 + 500 \times 7 = 3502 \text{ cycles}$$

DMA - I/O

$$\frac{20}{\uparrow} + \frac{500 \times 2 \text{ cycles}}{\uparrow} = 1020 \text{ cycles}$$

$$\text{Speed Up} = \frac{3502}{1020} = 3.4$$

1. On a non-pipelined sequential processor, a program segment, which is a part of the interrupt service routine, is given to transfer 500 bytes from an I/O device to memory.

Assume that each statement in this program is equivalent to a machine instruction which takes one clock cycle to execute if it is a non-load/store instruction. The load-store instructions take two clock cycles to execute.

The designer of the system also has an alternate approach of using the DMA controller to implement the same transfer. The DMA controller requires 20 clock cycles for initialization and other overheads. Each DMA transfer cycle takes two clock cycles to transfer one byte of data from the device to the memory.

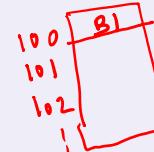
What is the approximate speedup when the DMA controller based design is used in place of the interrupt driven program based input-output?

A. 3.4

B. 4.4

C. 5.1

D. 6.7



I/O organization part-1

Data Count Register

$$2^{16} = \underline{64 \text{ Kbytes}}$$



2. The size of the data count register of a DMA controller is 16 bits. The processor needs to transfer a file of 29, 154 kilobytes from disk to main memory. The memory is byte addressable. The minimum number of times the DMA controller needs to get the control of the system bus from the processor to transfer the file from the disk to main memory is ?

456

$$\text{File-Size} = \underline{29154 \text{ Kbytes}}$$

No. of Requests to be made

$$= \frac{\text{FileSize}}{\text{Max.Transfer in single request}}$$

$$= \frac{29154 \text{ KB}}{64 \text{ KB}} \\ = 455.58$$

456 times

I/O organization part-1

$$1 \text{ rev} = \frac{60 \text{ sec}}{15000 \text{ rev}} = 4 \text{ m.sec}$$

Aus (6.11)

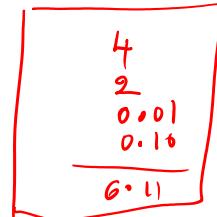
$$\text{Avg. Rot. Latency} = \frac{\text{Time for 1 rot}}{2} = \frac{4}{2} = 2 \text{ m.sec}$$

$$1 \text{ sec} = 50 \times 10^6 \text{ Bytes}$$

$$1 \text{ Byte} = \frac{1}{50 \times 10^6} \text{ sec}$$

$$= \frac{1}{50000} \text{ m.sec}$$

$$\text{For 512 Bytes} = 512 \times \frac{1}{50000} \text{ m.sec} = 0.010$$



3. Consider a typical disk that rotates at 15000 rotations per minute (RPM) and has a transfer rate of 50×10^6 bytes/sec. If the average seek time of the disk is twice the average rotational delay and the controller's transfer time is 10 times the disk transfer time, the average time (in milliseconds) to read or write a 512-byte sector of the disk is ?

$$\text{Avg. Seek} = 2 \times 2 = 4$$

Disk Access time

$$= \underline{\text{Avg. Seek time}} + \underline{\text{Avg. Rot Delay}} + \underline{\text{Avg. Disk Transfer time}}$$

+ controller's overhead

$$= 6 + 2 +$$

Controller's transfer

$$= 10 \times 0.010$$

$$= 0.10$$

I/O organization part-1

10 MBytes/sec.

600 MHz.

$$1 \text{ cycle} = \frac{1}{600 \times 10^6} \text{ sec}$$

DMA initiation

$$= \frac{10}{6} \text{ n.s}$$

$$1200 \times \frac{10}{6} = 2000 \text{ n.s}$$

4. A Hard Disk with a transfer rate of 10 Mbytes per second is constantly transferring data to memory using DMA. The processor runs at 600 MHz, and takes 300 and 900 clock cycles to initiate and complete DMA transfer respectively. If the size of the transfer is 20 Kbytes, what is the percentage of processor time consumed for the transfer operation?

- A. 5.0%
- B. 1.0%
- C. 0.5%
- D. 0.1%

$$300 + 900 = 1200 \text{ cycles}$$

$$T_t = \frac{L}{B} = \frac{20 \times 1000}{10 \times 10^6} \text{ sec}$$

$$\begin{aligned} 1K &= 10^3 \\ 1M &= 10^6 \end{aligned}$$

$$\begin{aligned} 1K &= 2^{10} \\ 1M &= 2^{20} \end{aligned}$$

$$= \frac{2}{1000} \text{ sec}$$

$$= \frac{2}{1000} \times 10^9 = 2000000 \text{ n.s}$$

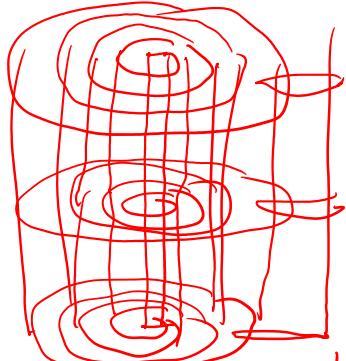
$$\text{Total time} = 2002000 \text{ n.s}$$

$$\frac{2000}{2002000} \times 100$$

$$= 0.09$$

$$0.1$$

I/O organization part-1

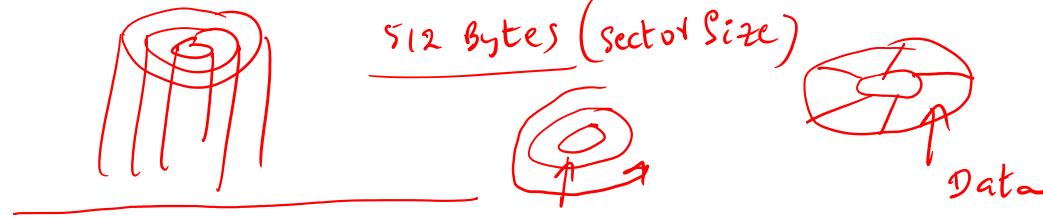


R/W Headset

5. A Disk has 24 recording surfaces and has a total of 14000 cylinders. There is an average of 400 sectors per track. Each sector contains 512 bytes of data. What is the data transfer rate in bytes per second at a rotational speed of 7200 RPM?

7200-RPM

14000 cylinders \rightarrow 14000 tracks on one surface



$$60 \text{ sec} = 7200 \text{ rev}$$

$$\begin{aligned} 1 \text{ rev} &= \frac{60}{7200} \text{ sec} \\ &= \frac{1}{120} \text{ sec} \end{aligned}$$

In $\left(\frac{1}{120} \text{ sec}\right) = \frac{400 \text{ sectors}}{= 400 \times 512 \text{ Bytes}}$

$$\begin{aligned} 1 \text{ sec} &= 120 \times 400 \times 512 \text{ Bytes} \\ &= \frac{120 \times 200 \times 2 \times 512 \text{ B}}{24000 \text{ KB}} \end{aligned}$$

I/O organization part-1

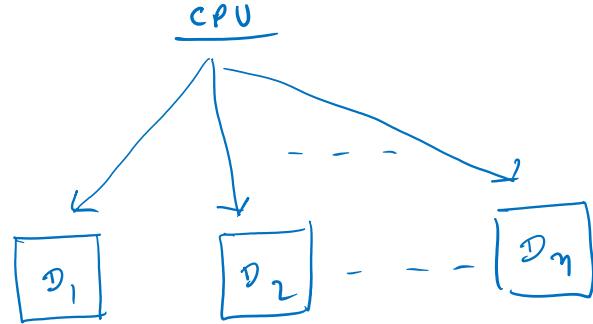
I/O - Transfer Techniques

- (1) Programmed I/O ✓
- (2) Interrupt initiated I/O ✓
- (3) DMA (Direct Memory Access) ✓

ISR

Interrupt Service Program ✓

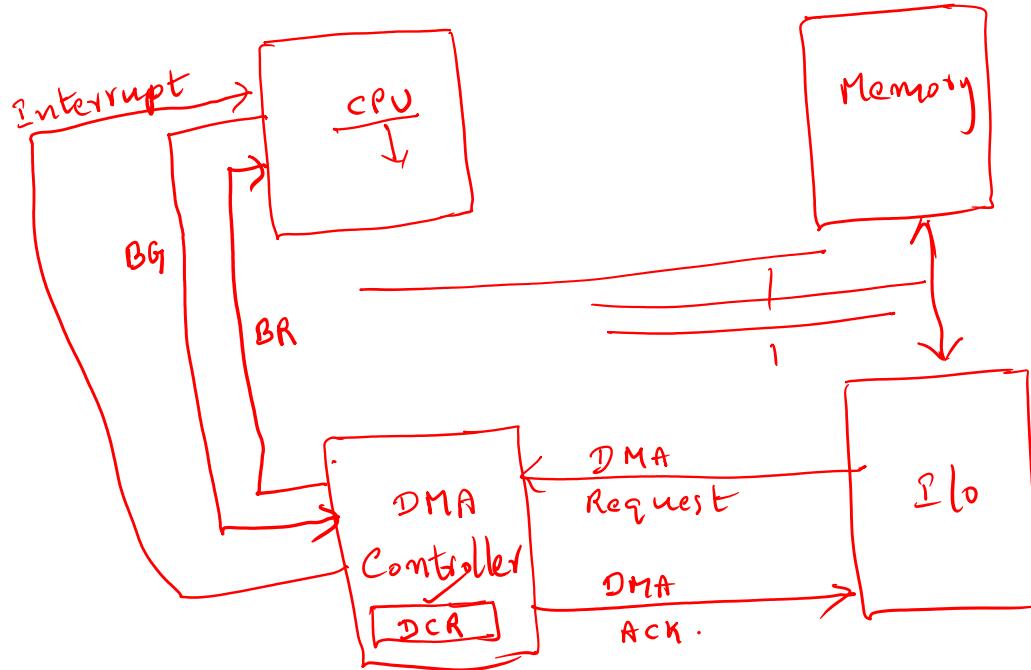
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 DMA
 DMA Controller



I/O organization part-1

DMA Controller

1024
1000



I/O organization part-1

H/W :- ① A Hard disk has 1024 tracks per surface with 16 recording surfaces. Each track can have 512 sectors. Each sector can store data of 1024 Bytes. what is the size of the Hard Disk ?

② If Disk is rotating at a Speed of 10000 RPM, what is the average rotational latency ?