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# Computer Organization and Architecture

**Basic computer  
organization and  
design Part-2**

# ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

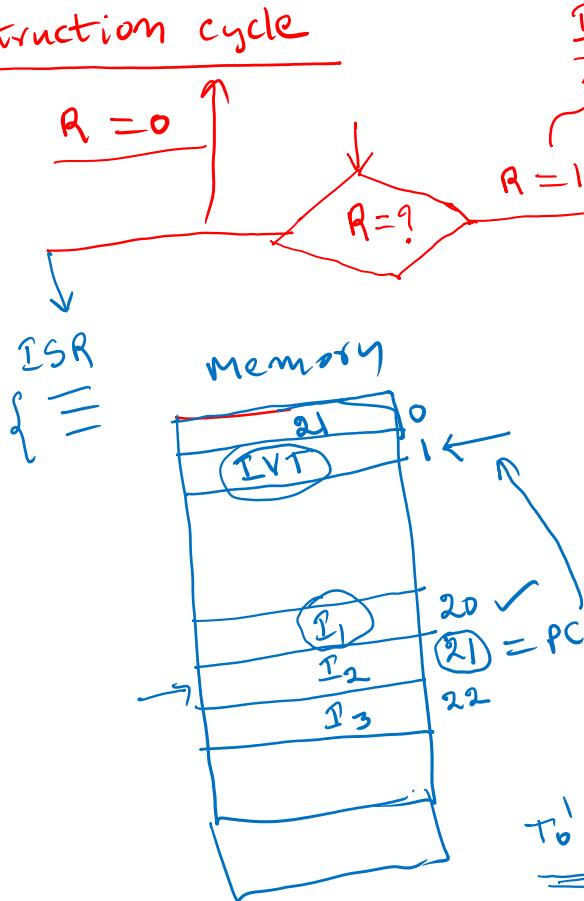
- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



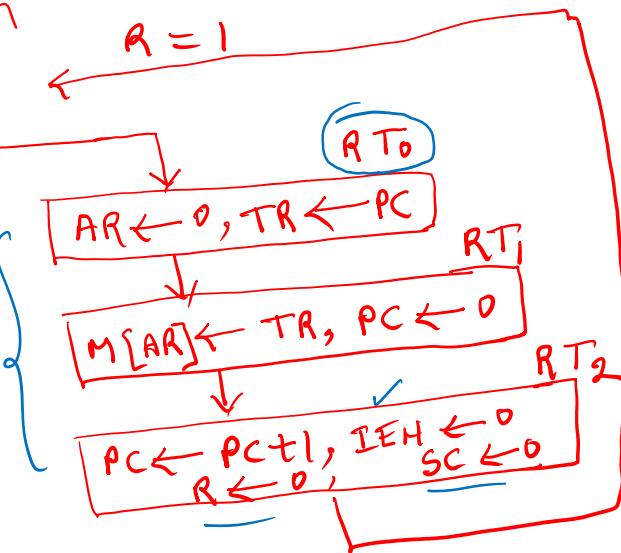
# Basic computer organization and design part-2

$R^1 T_0 : AR \leftarrow PC$   
 $R^1 T_1 : IR \leftarrow M[AR], PC++$   
 $R^1 T_2 :$   
 $\vdots$

## Instruction cycle

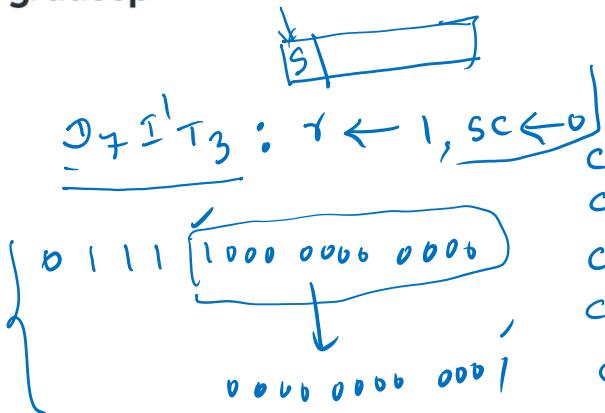


## Interrupt cycle



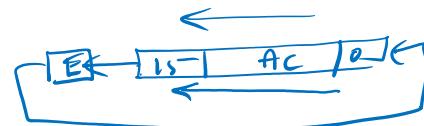
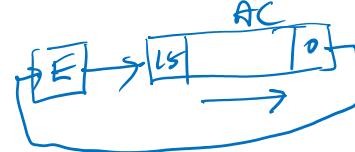
$T_0^1 T_1^1 T_2^1 (IEN) (FGI + FG0) :$   
 $R \leftarrow 1$

# Basic computer organization and design part-2



## Register - Reference

- CLA  $\rightarrow TB_{11}$  :  $AC \leftarrow 0,$
- CLE  $\rightarrow TB_{10}$  :  $E \leftarrow 0$
- CMA  $\rightarrow TB_9$  :  $AC \leftarrow \overline{AC}$
- CME  $\rightarrow TB_8$  :  $E \leftarrow \overline{E}$
- CIR  $\rightarrow TB_7$  :  $AC \leftarrow \text{shl}(AC), AC(15) \leftarrow E, E \leftarrow AC(0)$
- CIL  $\rightarrow TB_6$  :  $AC \leftarrow \text{shl}(AC), E \leftarrow AC(15), AC(0) \leftarrow E$
- INC  $\rightarrow TB_5$  :  $AC \leftarrow AC + 1$
- SPA  $\rightarrow TB_4$  : If  $(AC(15) = 0)$  then  $PC \leftarrow PC + 1$
- SNA  $\rightarrow TB_3$  : If  $(AC(15) = 1)$  then  $PC \leftarrow PC + 1$
- SZA  $\rightarrow TB_2$  : If  $(AC = 0)$  then  $PC \leftarrow PC + 1$
- SZE  $\rightarrow TB_1$  : If  $(E = 0)$  then  $PC \leftarrow PC + 1$
- HLT  $\rightarrow TB_0$  :  $S \leftarrow 0$



# Basic computer organization and design part-2

## I/o - Reference

D<sub>7</sub> I T<sub>3</sub>: P ← 1

I III

- { INP → PB<sub>11</sub> : AC(0-7) ← INPR , FG1 ← 0
- OUT → PB<sub>10</sub> : OUTR ← AC(0-7), FG0 ← 0
- SKI → PB<sub>9</sub> : If (FG1 = 1) then PC ← PC + 1
- SKO → PB<sub>8</sub> : If (FG0 = 1) then PC ← PC + 1
- ION → PB<sub>7</sub> : IEN ← 1
- IOP → PB<sub>6</sub> : IEN ← 0

# Basic computer organization and design part-2

## RISC

- (1) Relatively few instructions in the instruction set
- (2) " " Addressing Modes
- (3) Mem. Access is limited to only load and store.
- (4) All operations done with in the registers of CPU.
- ✓(5) Fixed Length and easily decodable instructions
- (6) Single cycle instruction execution
- (7) It used H/W C.V rather than Micro-programme.

## CISC (Complex Instruction set Computer)

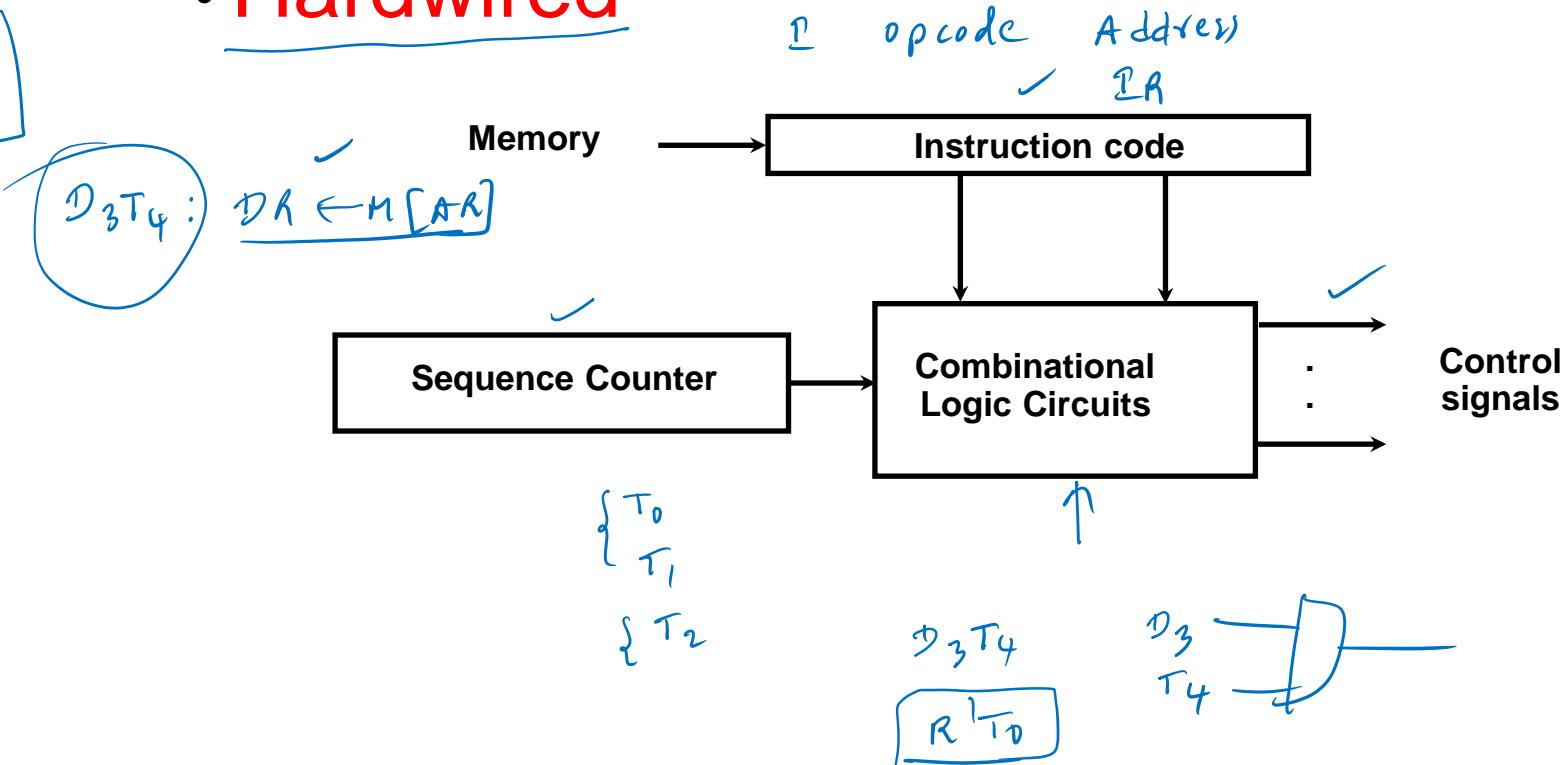
- (4) Instructions that manipulates Operands in memory.
- (5) Micro-programmed

- (1) Large Number of instructions
- (2) Large Variety of Addressing modes
- (3) Variable Length instruction format

# Basic computer organization and design part-2

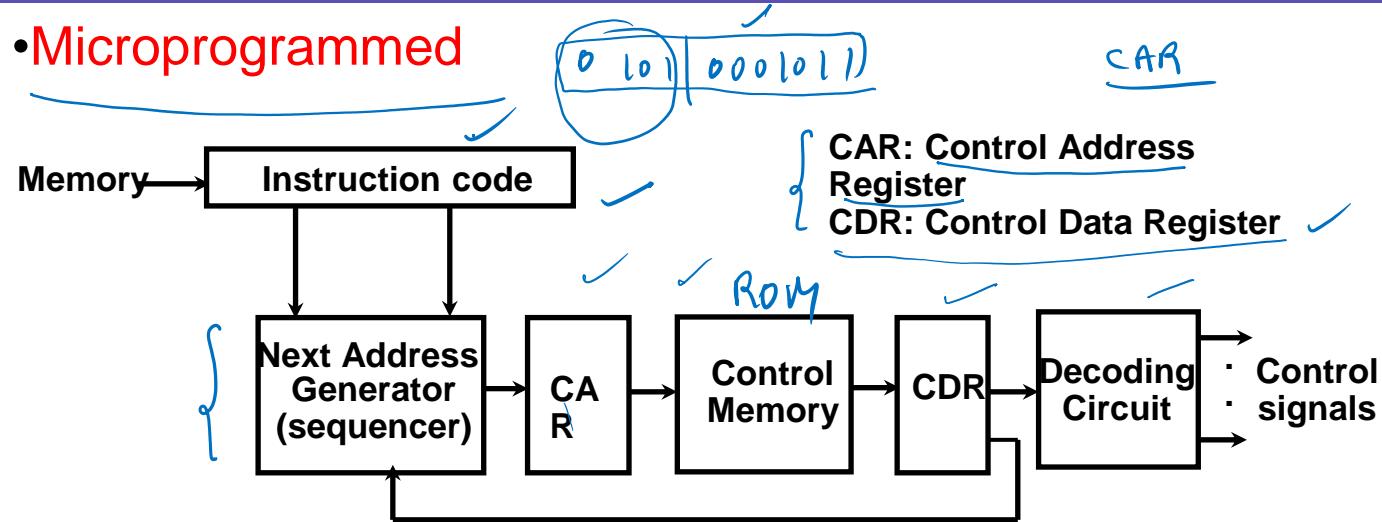
- Hardwired

RISC  
CISC



# Basic computer organization and design part-2

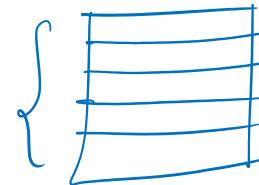
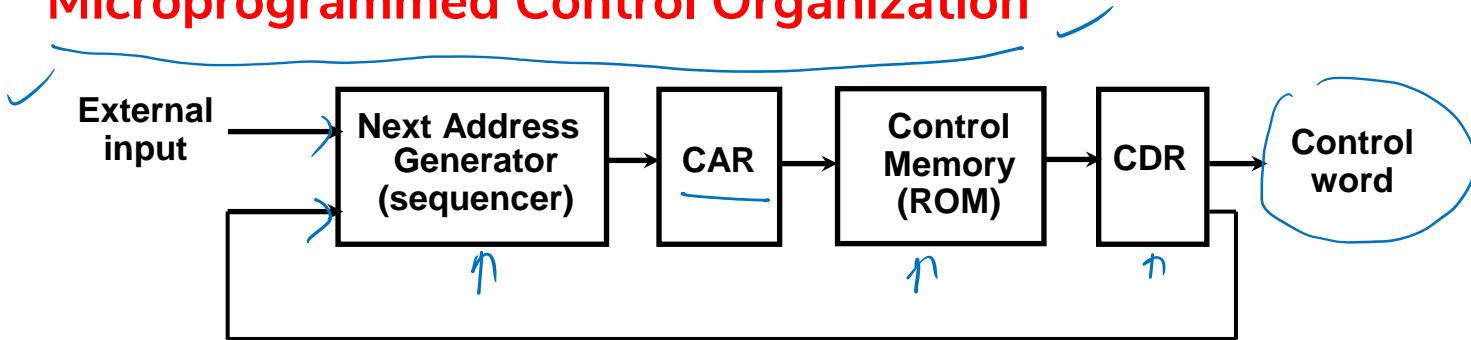
• Microprogrammed



Micro - Programs

Set of Micro-instructions

## Microprogrammed Control Organization



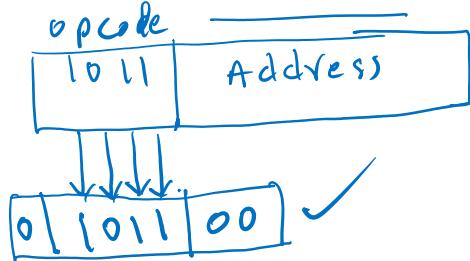
# Basic computer organization and design part-2

CAR

Address of Micro-instruction.

## Mapping Process

Binary Instruction code

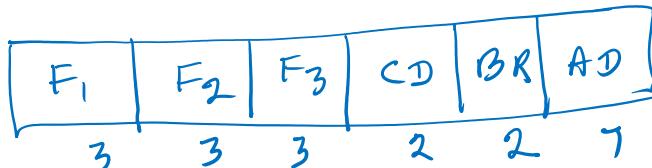


## Control Memory

$\left\{ \begin{array}{l} 128 \text{ words} \\ 2^7 \text{ words} \end{array} \right.$

7 - bits

## Micro-instruction code



F<sub>1</sub>: ✓  
 F<sub>2</sub>: ✓  
 F<sub>3</sub>: ✓

20 bits      Micro-instruction.

# Basic computer organization and design part-2

- ① Horizontal micro-Programming
- ② Vertical

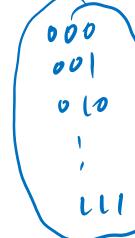
1 | 1 | 1 | -

Parallelism.

3 bits



3-bits



200 operations

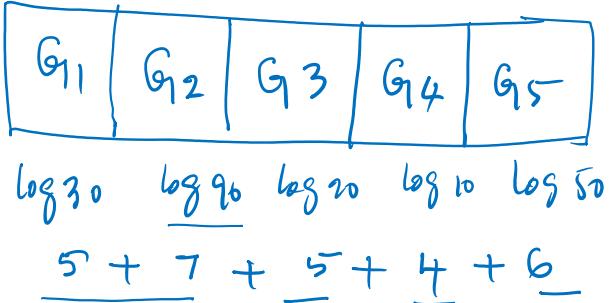
200

$2^3$

8 bits

$\log_2 200$

# Basic computer organization and design part-2



- An instruction set of a processor has 200 signals which can be divided into 5 groups of mutually exclusive signals as follows.

- Group 1 : 30 signals
- Group 2 : 90 signals
- Group 3 : 20 signals
- Group 4 : 10 signals
- Group 5 : 50 signals



How many bits of the control words can be saved by using vertical micro → programming over horizontal micro-programming ?

- A. 170      B. 227      C. 200      D. 173

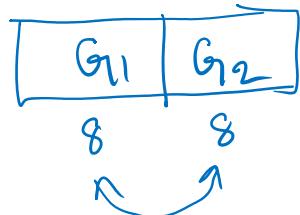
$$\begin{array}{r} 200 - 27 \\ \hline 173 \end{array}$$

27 bits

# Basic computer organization and design part-2

250 control signals

2. A micro programmed control unit supports 250 control signals, it is required that 2 of them should be active at the same time then what is the minimum size of the control field in the instruction?

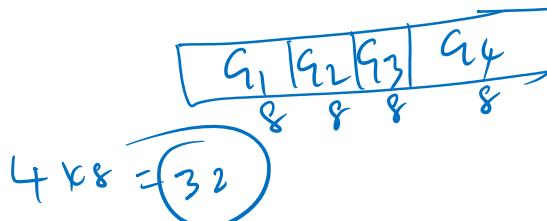


16 bits

$\log 250$

8

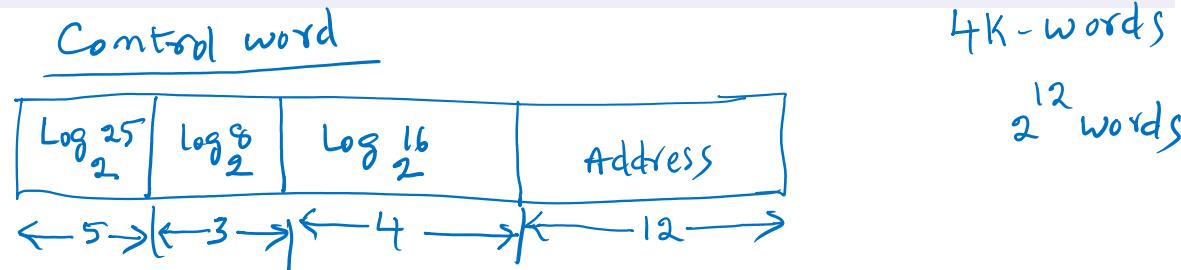
4



# Basic computer organization and design part-2

4 K-words

3. Consider a hypothetical control unit which supports 4K control words, Hardware has 25 control signals, 8 flags and 16 branch conditions are used to the control branch logic. What is the size of the control memory required using vertical micro-programming ?



$$12 + 4 + 3 + 5 = 24 \text{ bits} \quad \checkmark$$

$4K \times 24 \text{ bits}$

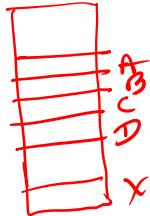
$4K \times 3 \text{ Bytes}$   
 $= 12 \text{ K Bytes}$  ✓

# Basic computer organization and design part-2

## RISC characteristics

### Reduced instruction Set Computer

$$x = (A + B) * (C + D)$$



{

Load	<u><math>R_1, A</math></u>	$; R_1 \leftarrow M[A]$
Load	<u><math>R_2, B</math></u>	$; R_2 \leftarrow M[B]$
ADD	<u><math>R_1, R_2</math></u>	$; R_1 \leftarrow R_1 + R_2$
Load	<u><math>R_3, C</math></u>	$; R_3 \leftarrow M[C]$
Load	<u><math>R_4, D</math></u>	$; R_4 \leftarrow M[D]$
ADD	<u><math>R_3, R_4</math></u>	$; R_3 \leftarrow R_3 + R_4$
MUL	<u><math>R_1, R_3</math></u>	$; R_1 \leftarrow R_1 * R_3$
STORE	<u><math>X, R_1</math></u>	$; M[X] \leftarrow R_1$