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Computer Organization and Architecture

Combinational circuits

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

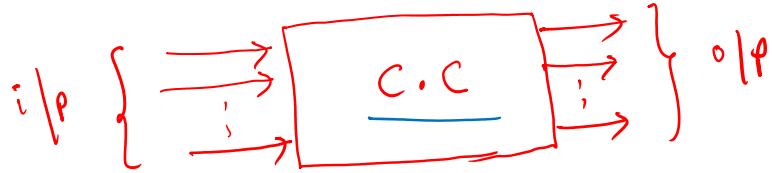
- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



Combinational Circuits

→ Connected arrangement of Logic GATES with some set of i/p's and o/p's.

Combinational Circuit

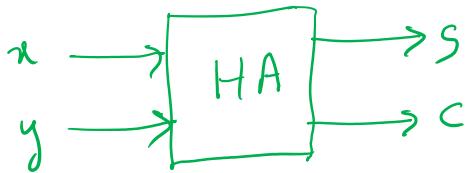


- (1) Problem Statement
- (2) Assign letter symbols for i/p's and o/p's
- (3) Define truth Table.
- (4) Get Minimized equation for all o/p's
- (5) Draw the Logic Circuit.

Examples :- HA, FA, Decoder, MUX -- etc..

Combinational Circuits

Design of Half Adder



It is a Combinational Circuit for the addition of two binary bits.

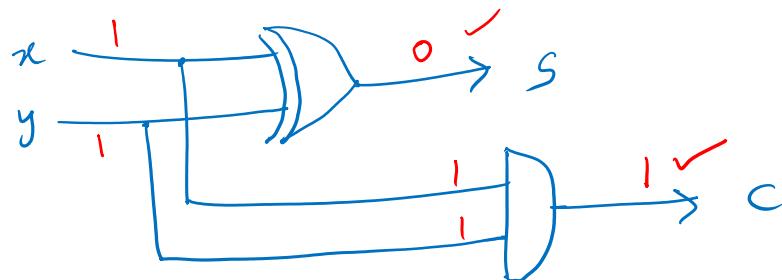
x	y	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$S = \bar{x}\bar{y} + xy'$$

$$S = x \oplus y$$

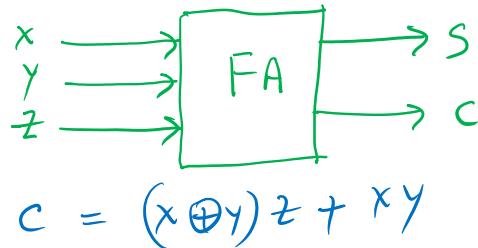
$$C = xy$$

$$\begin{array}{l} 1+1=2 \\ \quad \uparrow \\ \quad \underline{\underline{10}} \end{array}$$



Combinational Circuits

→ Design of FULL Adder



It is a C.C for the addition of 3 binary bits
 [two bits to be added and Previous Carry]

x	y	z	S	C
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$1+1+1=3 \begin{matrix} 11 \\ 11 \end{matrix}$$

$$\begin{aligned} S &= x'y'z + x'yz' \\ &\quad + xy'z' + xyz \end{aligned}$$

$$\begin{aligned} S &= x'(y'z + yz') + x(y'z' + yz) \\ &= \underline{x'(y \oplus z)} + \underline{x(y \otimes z)} \end{aligned}$$

$$S = x \oplus y \oplus z$$

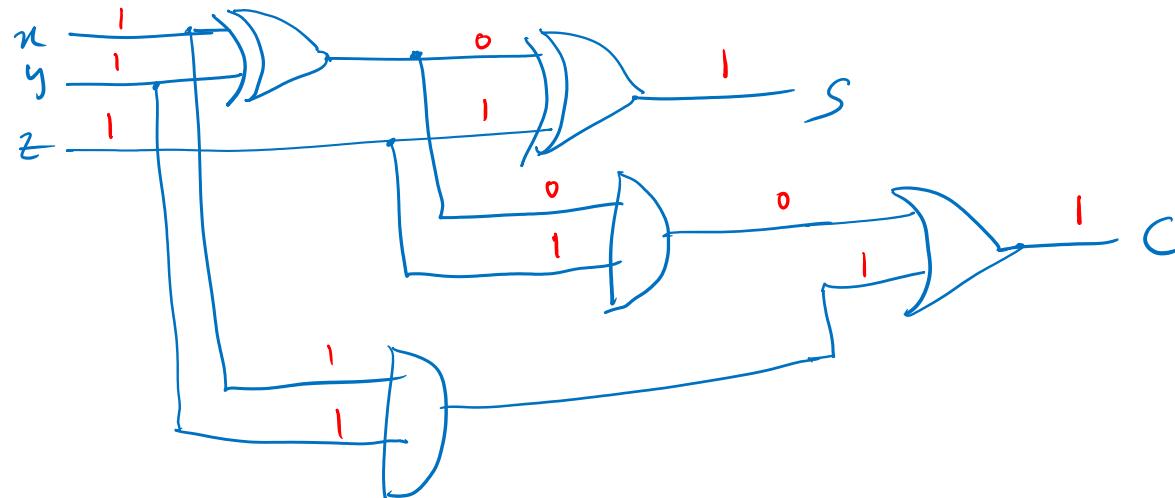
$$\begin{aligned} C &= x'yz + xy'z + xyz' + xyz \\ &= (x'y + xy')z + xy(z' + z) \end{aligned}$$

Combinational Circuits

Logic-Diagram

$$S = x \oplus y \oplus z$$

$$C = (x \oplus y)z + xy$$



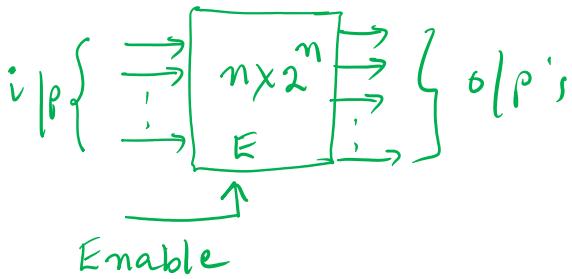
$$1+1+1=3 \text{ (11)}$$

$$S=1, C=1$$

→ Full Adder Can be designed by using two Half Adders and one OR GATE.

Combinational Circuits

Decoder



1×2

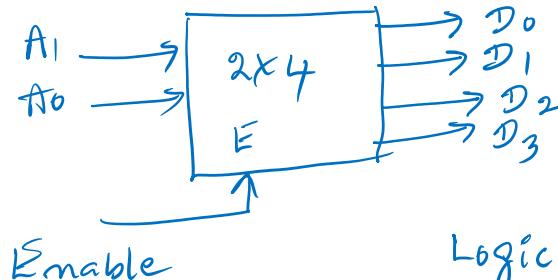
2×4

3×8

4×16

⋮

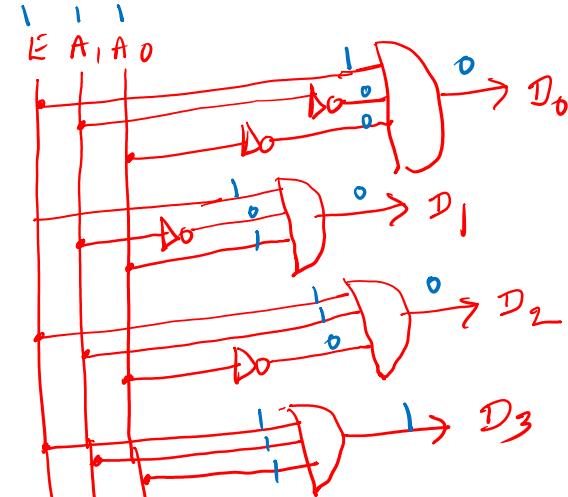
Design of 2×4 Decoder



Truth Table

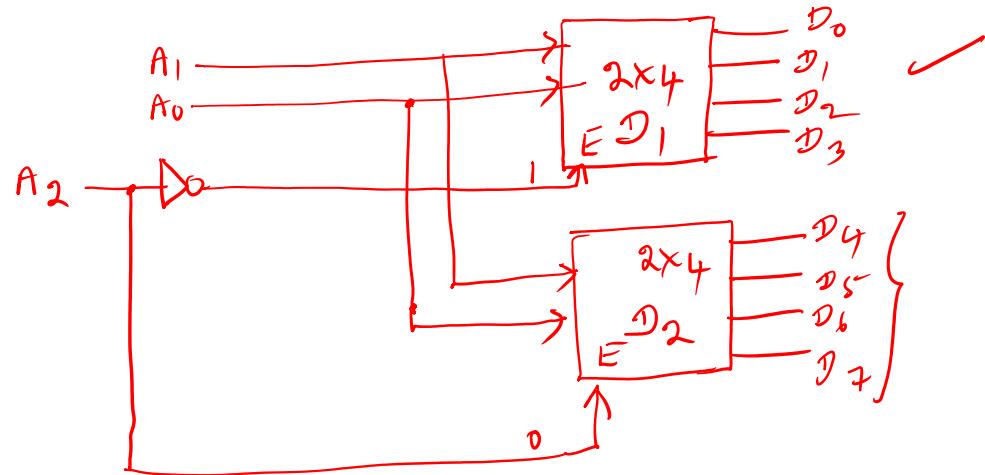
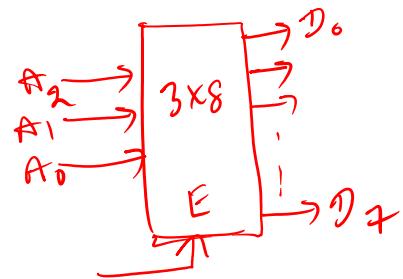
E	$A_1 A_0$	D_0	D_1	D_2	D_3
0	XX	0	0	0	0
1	00	1	0	0	0
1	01	0	1	0	0
1	10	0	0	1	0
1	11	0	0	0	1

Logic Diagram



Combinational Circuits

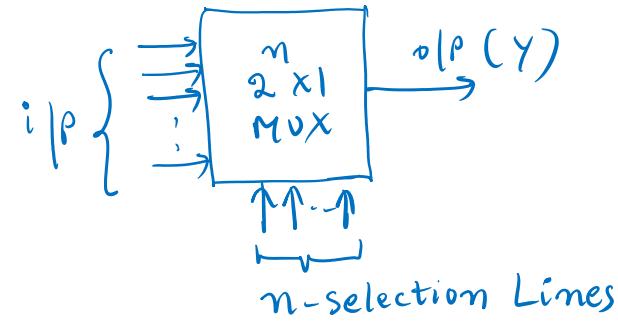
Design of 3×8 Line Decoder by using two 2×4 Line decoders



A ₂	A ₁	A ₀	D ₆	D ₅	D ₄	D ₃	D ₂	D ₁	D ₀
0	0	0	1	0	-	-	-	-	0
0	0	1	0	1	-	-	-	-	0
1	1	1	0	0	-	-	-	-	1

Combinational Circuits

Multiplexers

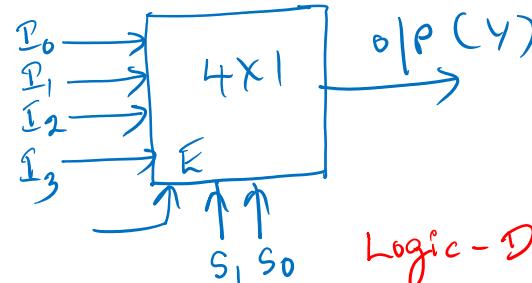


$$\begin{array}{c} 2 \times 1 \\ 4 \times 1 \\ \hline 8 \times 1 \\ \hline 16 \times 1 \end{array}$$

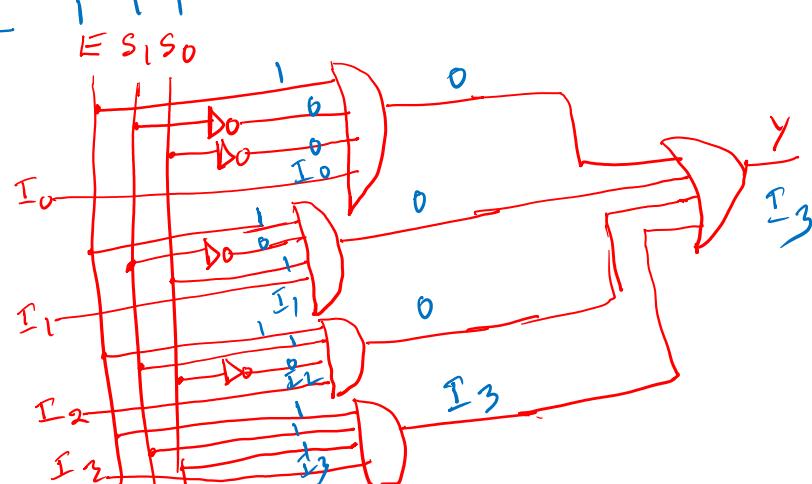
Truth Table

E S ₁ S ₀	Y
0 XX	0
1 0 0	I ₀
1 0 1	I ₁
1 1 0	I ₂
1 1 1	I ₃

Design of 4x1 MUX

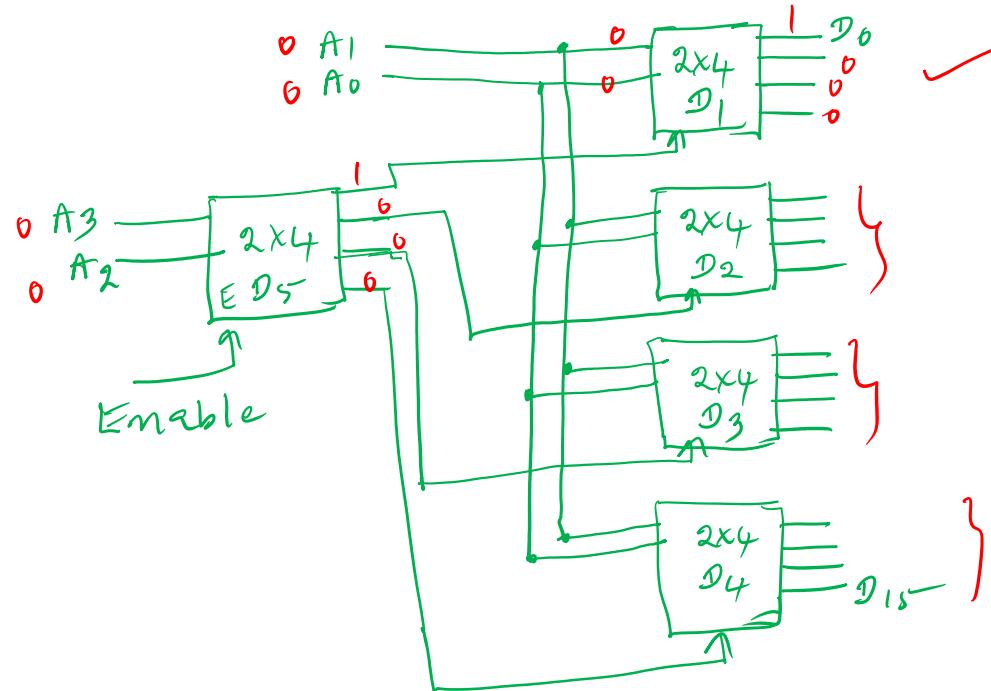
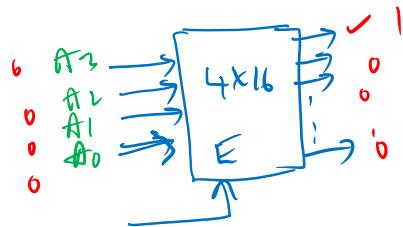


Logic-Diagram



Combinational Circuits

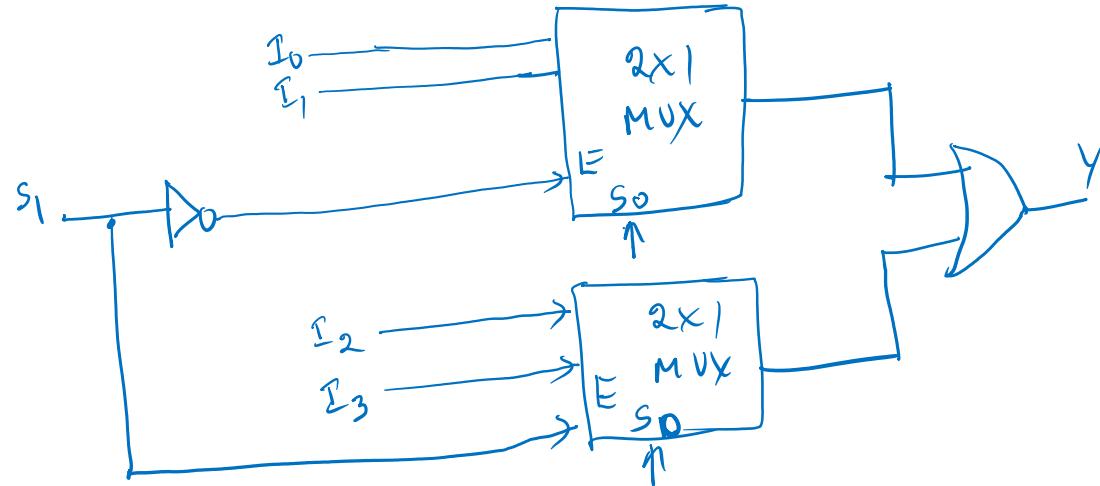
→ Design of 4×16 Decoder by using only 2×4 Decoders.



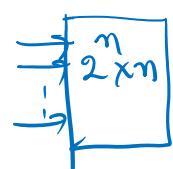
Combinational Circuits

Design of 4×1 MUX using two 2×1 MUX and OR Gate

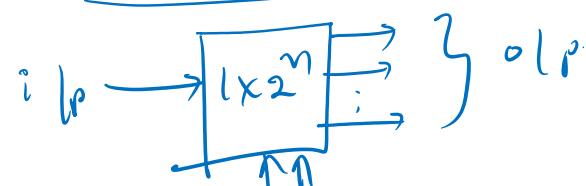
S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3



Encoder



D - MUX

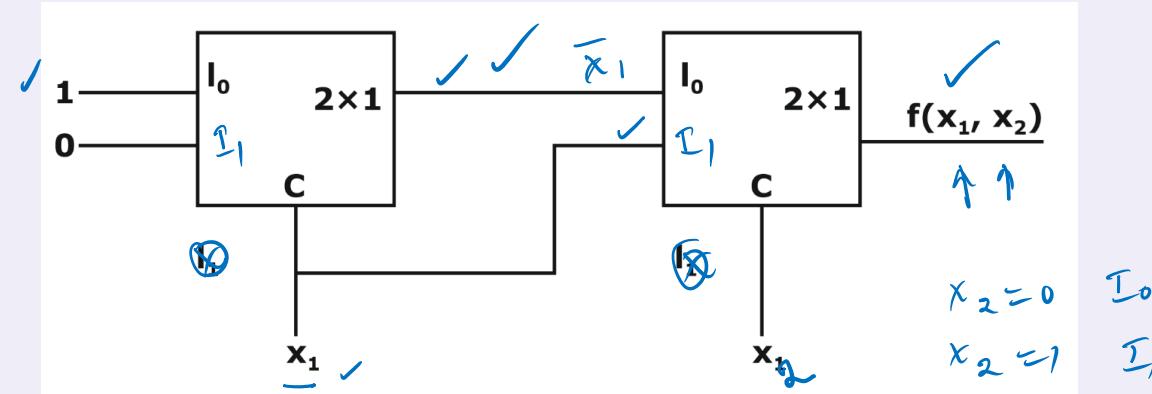


Combinational Circuits

$$\begin{array}{ll} x_1 = 0 & (1) \\ x_1 = 1 & (0) \end{array}$$

1. Consider

Which of the following is true ?



- A. f is independent of x_2
- B. $f = x'_1 x_2 + x'_2 x_1$
- C. $f = x'_1 + x_2$
- D. $f = \underline{x'_1 x'_2} + \underline{x_1 x_2}$

$$\bar{x}_1 \cdot 1 + x_1 \cdot 0 = \bar{x}_1$$

$$\begin{aligned} f &= \frac{\bar{x}_2 \bar{x}_1 + x_2 x_1}{x_2 \oplus x_1} \\ &= \underline{x_2 \oplus x_1} \end{aligned}$$

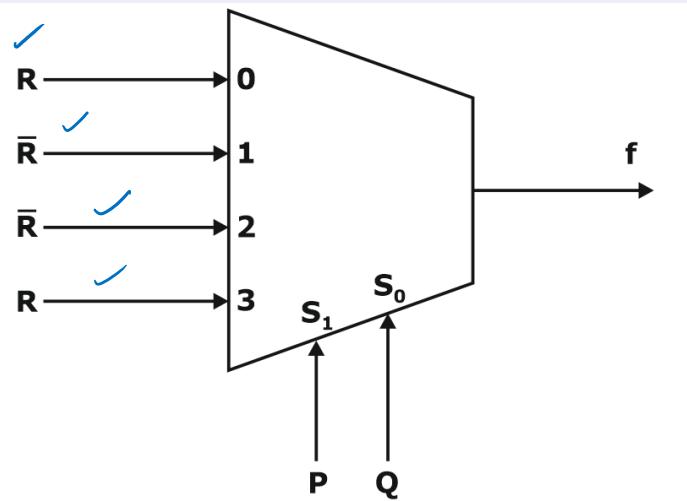
$$\begin{array}{ll} x_2 = 0 & I_0 \\ x_2 = 1 & I_1 \end{array}$$

Combinational Circuits

$$\begin{aligned}
 f &= \bar{P}\bar{Q}R + \bar{P}Q\bar{R} + P\bar{Q}\bar{R} + PQR \\
 &= \bar{P}(\bar{Q}R + Q\bar{R}) + P(\bar{Q}\bar{R} + QR) \\
 &= \bar{P}(Q \oplus R) + P(Q \oplus R) \\
 &= P \oplus Q \oplus R
 \end{aligned}$$

2. The Boolean expression for the output f of the multiplexer shown below is

- A. $\overline{P \oplus Q \oplus R}$
- B. $P \oplus Q \oplus R$
- C. $P + Q + R$
- D. $\overline{P + Q + R}$



00	$\bar{P}\bar{Q}$
01	$\bar{P}Q$
10	$P\bar{Q}$
11	PQ

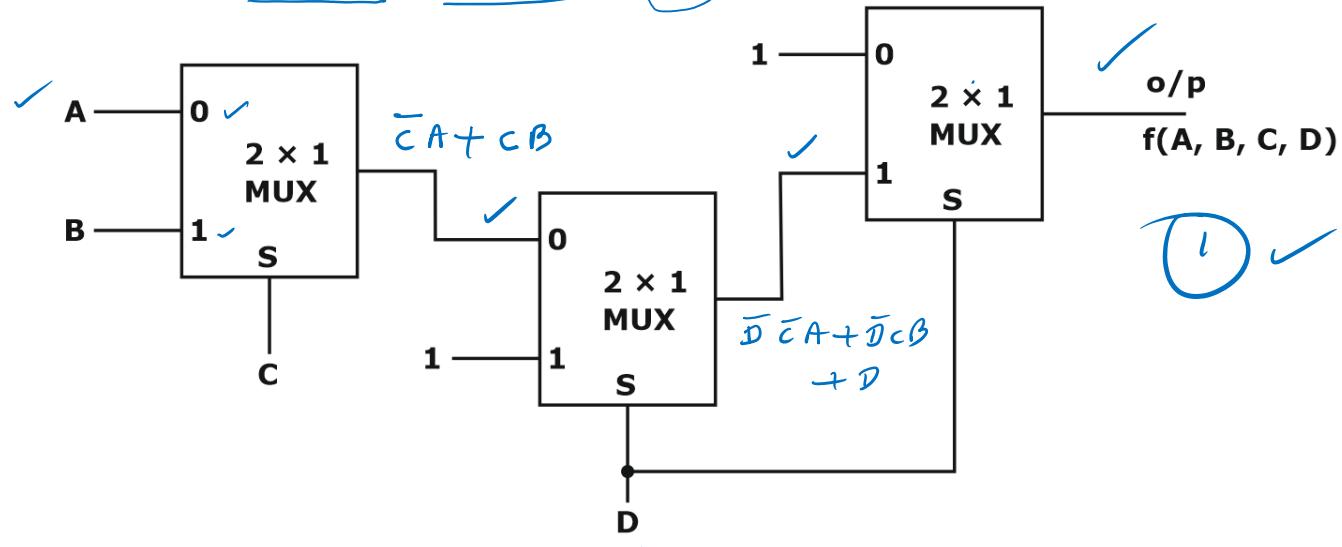
Combinational Circuits

3. Identify the function represented by the following MUX combination.

$$\overline{D} \cdot 1 + D \left[\overline{D} \overline{C} A + \overline{D} C B + D \right] = \overline{D} + \underline{D \overline{D} \overline{C} A} + \underline{D \overline{D} C B} + (\overline{D} D)$$

$\boxed{\overline{D} + D}$

$\boxed{1}$



$$\begin{aligned} & \overline{D} (\overline{C} A + C B) + D \cdot 1 \\ & \overline{D} \overline{C} A + \overline{D} C B + D \end{aligned}$$

Combinational Circuits

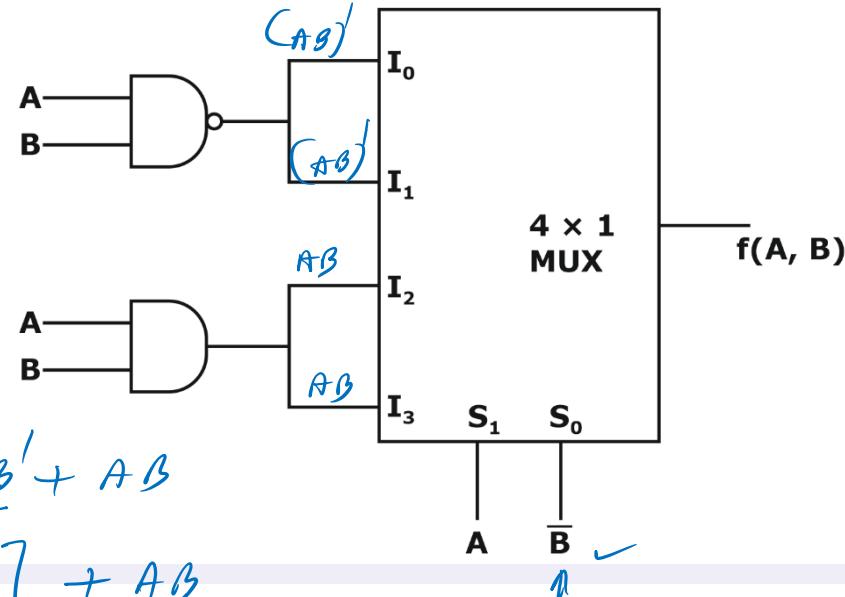
$$\begin{aligned}
 & \bar{A}B(A\bar{B})' + \bar{A}\bar{B}(A\bar{B})' \\
 & + \underline{AB(A\bar{B})} + \underline{A\bar{B}(AB)} \\
 = & A'B(A' + B') + A'B'(A + B') \\
 & + AB \\
 & A'B + \underline{A'B'} + \underline{A'B'} + AB
 \end{aligned}$$

4. The function realized by following circuit is

- A. $B + \bar{A}$
- B. 1
- C. $B \oplus C$
- D. $A + B + C$

$$\begin{aligned}
 & \underline{A'B + A'B'} + AB \\
 = & A' [B + B'] + AB
 \end{aligned}$$

$$\begin{aligned}
 A' + AB &= (A' + A)(A' + B) \\
 &= (A' + B)
 \end{aligned}$$



$S_1 S_0$	\overline{AB}
00	\overline{AB}
01	\overline{AB}
10	AB
11	AB

Combinational Circuits

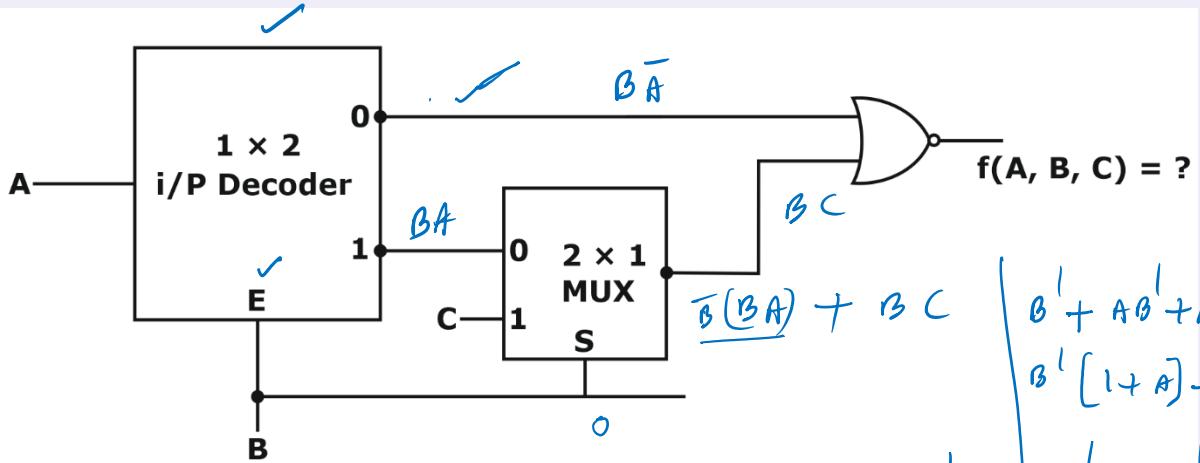
$$A = 0$$

$$A = 1$$

$$\bar{B} \bar{A} +$$

$$\bar{B} A$$

5. What will be the output function for the given logic design ?



A. $\bar{A}B + C$

B. $A\bar{B} + \bar{C}$

C. $\bar{B} + \bar{A}C$

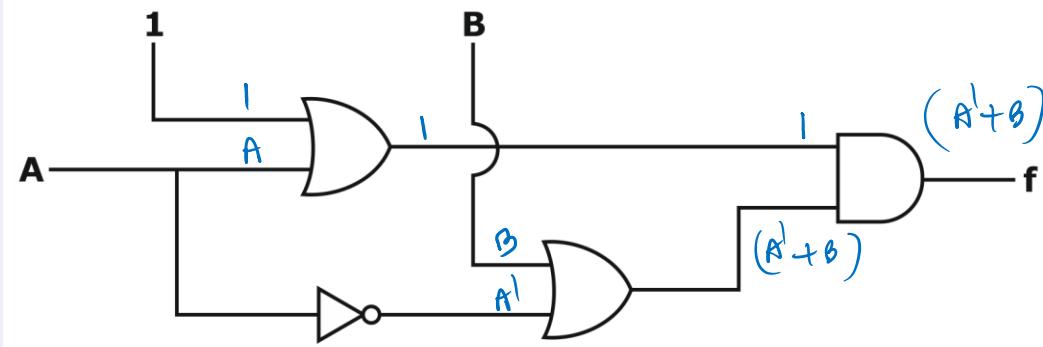
D. $\bar{B} + A\bar{C}$

$$\begin{aligned} & \bar{B} \cdot 0 \quad (\bar{B} \bar{A} + BC) \\ & (\bar{B} \bar{A})' (\bar{B} C)' \\ & (\bar{B}' + A) (\bar{B}' + C') \\ & \bar{B}' + \bar{B}' C' + A \bar{B}' + A C' \end{aligned}$$

Combinational Circuits

$$f = A' + B$$

6. Consider the following circuit :



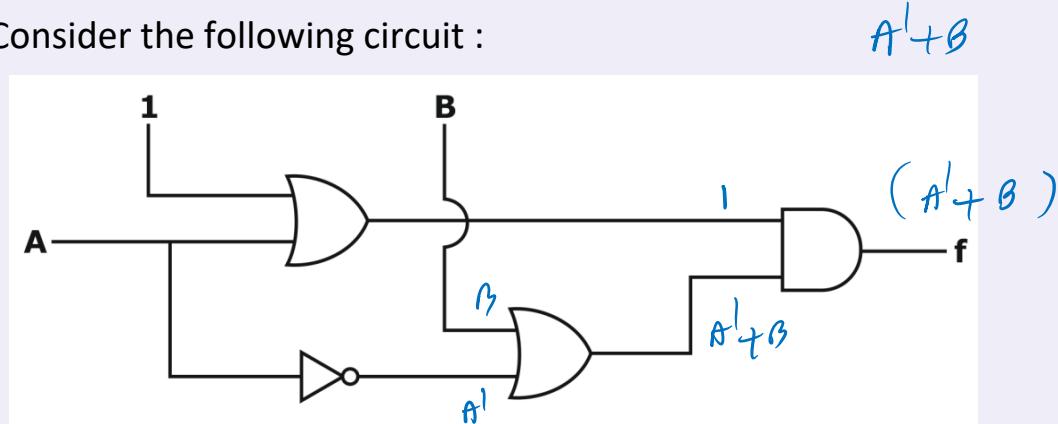
Determine the expression of the output function f

- A. $A + B$
- B. $A' + B$
- C. AB
- D. $A' + B'$

Combinational Circuits

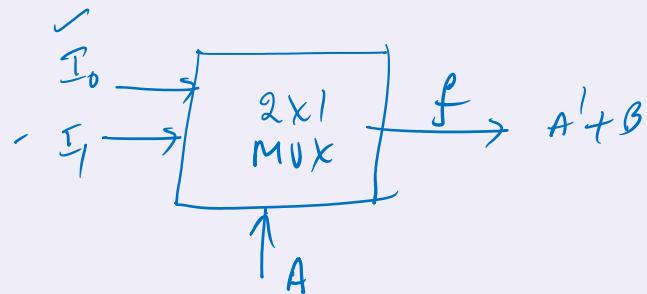
$$\begin{aligned}
 & \bar{A} \cdot I_0 + A \cdot I_1 = A' + B \\
 & \bar{A} \cdot 1 + A \cdot B \\
 & \bar{A} + AB = (\bar{A} + A)(A' + B) \\
 & = (A' + B) \checkmark
 \end{aligned}$$

7. Consider the following circuit :



To implement the function using a 2×1 multiplexer with A as the selection line, determine the value of I_0 and I_1 respectively of the multiplexer.

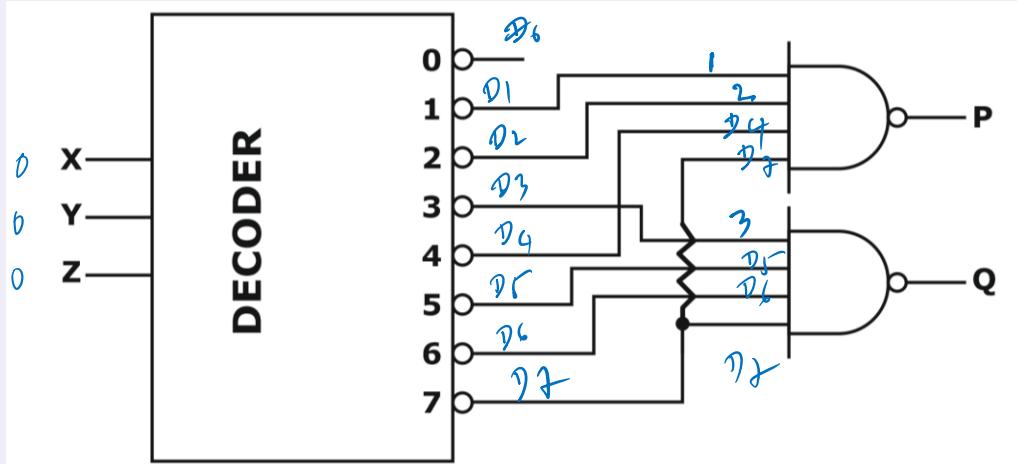
- A. B, 1
- B. 1, B
- C. 0, B
- D. 1, B'



Combinational Circuits

$$\begin{aligned}
 & \bar{x}\bar{y}z + \bar{x}y\bar{z} + x\bar{y}\bar{z} + xy\bar{z} \\
 & \underline{\bar{x}(\bar{y}z + y\bar{z}) + x(\bar{y}\bar{z} + yz)} \\
 P = & \quad x \oplus y \oplus z
 \end{aligned}$$

8. Identify the pair of correct equations for P and Q shown in the following figure.

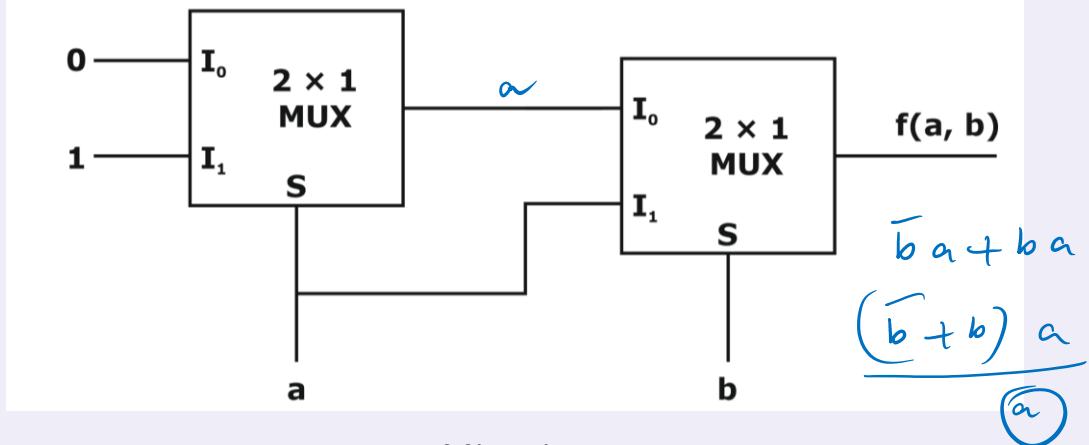


- A. $P = x \odot y \odot z \quad Q = \bar{x}y + xz + yz$
- B. $P = x \oplus y \oplus z \quad Q = x\bar{y} + xz + yz$
- C. $\checkmark \quad P = x \oplus y \oplus z \quad Q = \underline{xy + xz + yz}$
- D. $P = x \odot y \odot z \quad Q = \bar{x}y + \bar{x}z + yz$

Combinational Circuits

$$\bar{a} \cdot 0 + a \cdot 1 = a$$

9. Consider the following multiplexer circuit:



Determine the expression of $f(a, b)$

- A. ab
- B. $a' + b$
- C. b
- D. a

$$\bar{b} \cdot a + b \cdot a$$

Combinational Circuits

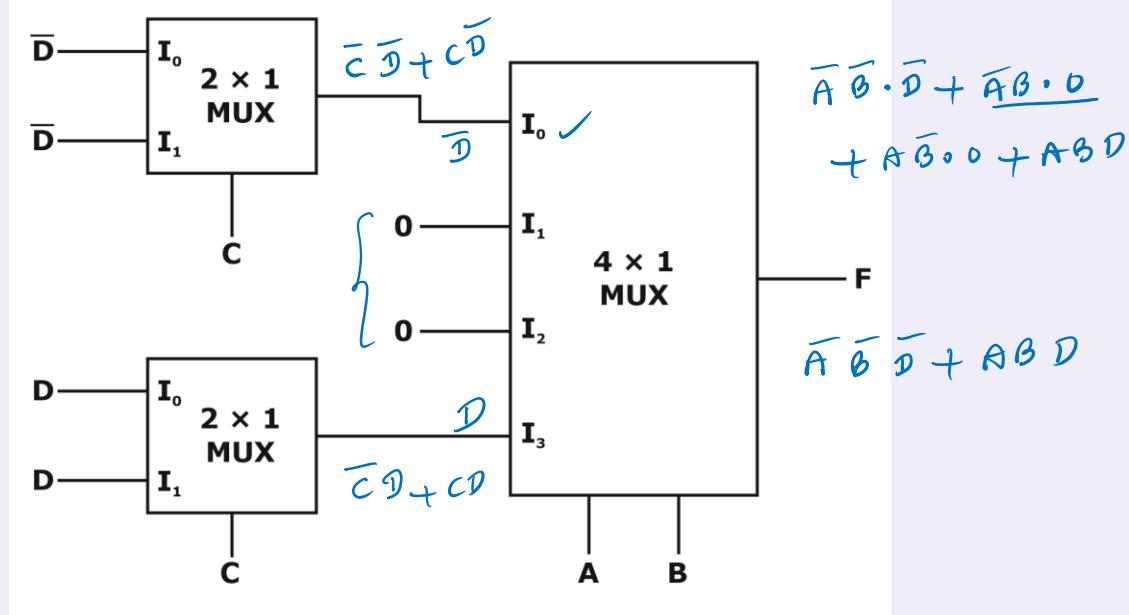
$$\bar{c}\bar{d} + c\bar{d}$$

$$(\bar{c}+c)\bar{d} = \bar{d}$$

$$\bar{c}d + cd$$

$$(\bar{c}+c)d = d$$

10. Determine the output of the following 4×1 multiplexer.



- A. $D(A \oplus B)$
- B. $\bar{A}\bar{B}C + ABD$
- C. $\underline{\bar{A}\bar{B}D + ABD}$
- D. None of these