



Computer Organization and Architecture

**Basic computer
organization and
design Part-1**

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

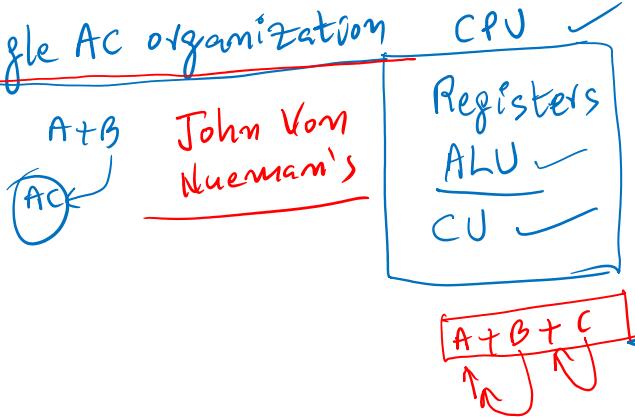
- M.Tech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



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Control Unit of a Basic Computer

(1) Single AC organization

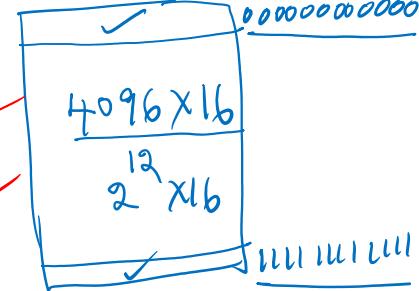


Registers [Special Purpose]

- (1) AR = Address Register
- (2) PC = Program Counter
- (3) DR = Data Register
- (4) AC = Accumulator
- (5) IR = Instruction Register
- (6) TR = Temporary Register
- (7) INPR = Input Register
- (8) OUTR = Output Register

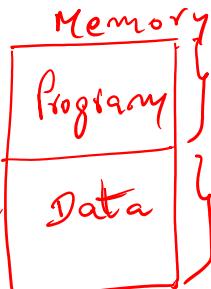
opcode | address

Main Memory



12 → Address bits

16 → Data bits



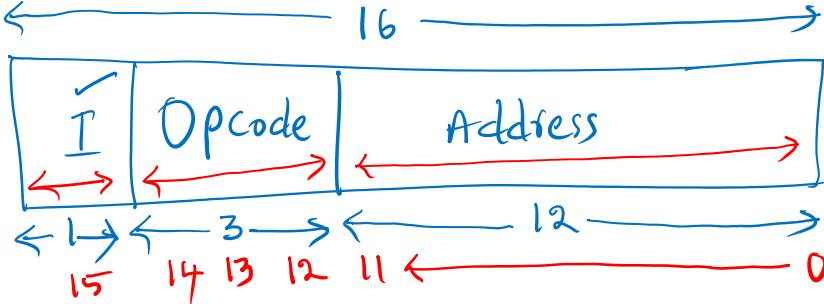
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One-Address Instructions

I = Indirect bit

Opcode = Operation code.

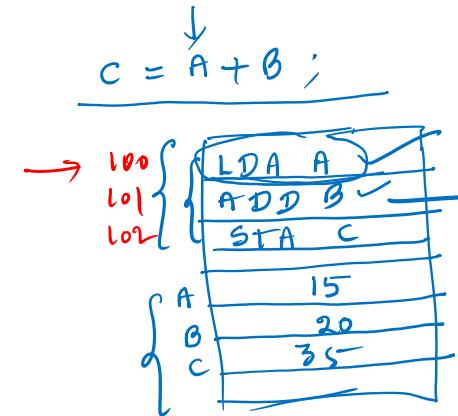
Address = Memory Address



$$\begin{cases} \text{LDA } A ; & AC \leftarrow M[A] \\ \text{ADD } B ; & AC \leftarrow AC + M[B] \\ \text{STA } C ; & M[C] \leftarrow AC \end{cases}$$

$I = 0$ (Direct Mode)

$I = 1$ (Indirect Mode)



LDA : Load the AC register with a Mem. Word

STA : store the AC content in Memory

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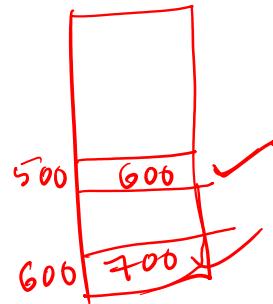
I Opcode, Address

Effective Address

Address of Memory
where Operand
resided.

Instruction Cycle

- (1) Fetching the instruction
- (2) Decoding of "
- (3) Fetching the Operand
- (4) Executing the instruction.



Direct Mode



$$AC \leftarrow AC + M[500]$$

↑

Indirect Mode

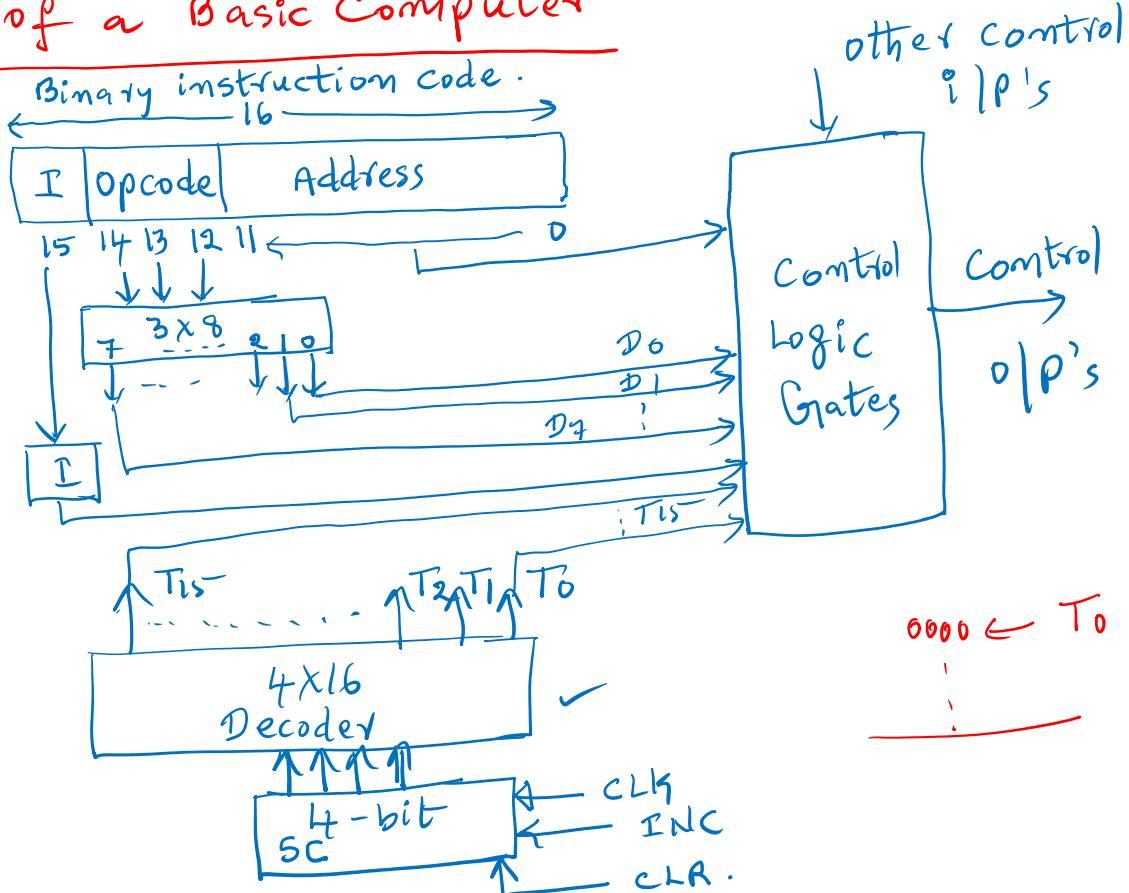


$$AC \leftarrow AC + M[M(500)]$$

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- 000 - D_0 ✓
- 001 - D_1 ✓ $I = 0$ (Direct Mode)
- 010 - D_2 ✓ $I = 1$ (Indirect)
- 111 - D_7 ✓

Control Unit of a Basic Computer



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Instruction Fetch

Fetch

$$\left\{ \begin{array}{l} T_0 : AR \leftarrow PC \\ T_1 : IR \leftarrow M[AR], PC \leftarrow PC + 1 \end{array} \right.$$

$$\left\{ \begin{array}{l} T_0 \\ T_1 \\ \vdots \\ T_2 \end{array} \right.$$

Decoding instruction

$$\underline{T_2} : D_0, D_1, \dots, D_7 \leftarrow \text{Decode } IR(12-14), \\ I \leftarrow IR(15), AR \leftarrow IR(0-11)$$

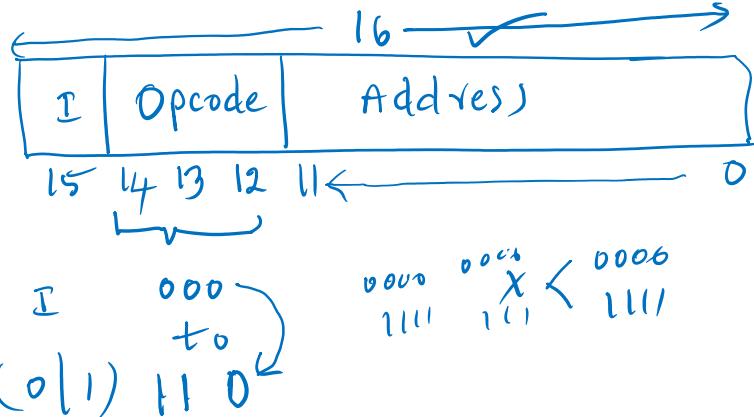
Categories of instructions

- (1) Memory Reference
- (2) Register Reference
- (3) I/O - Reference

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Code	$I = 0$	$I = 1$
D ₀	0 XXX	8 XXX
D ₁	1 XXX	9 X X 1
D ₂	2 X XX	A XXX
D ₃	3 X XX	B XXX
D ₄	4 XXX X	C XXX
D ₅	5 X XX	D XXX
D ₆	6 X XX	E XXX

Memory Reference Instructions



	$I = 0$
D ₀	0 000
D ₁	0 001
D ₂	0 010
D ₃	0 011
D ₄	0 100
D ₅	0 101
D ₆	0 110

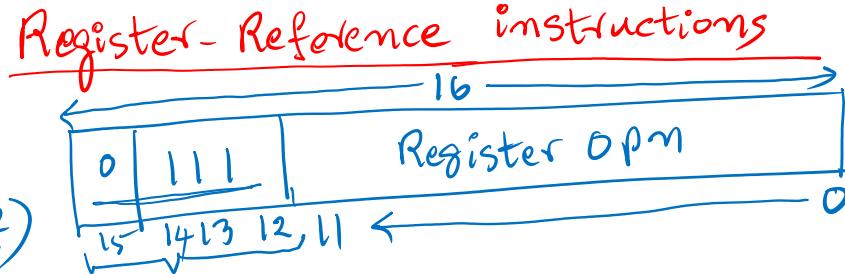
	$I = 1$
D ₀	1 000
D ₁	1 001
D ₂	1 010
D ₃	1 011
D ₄	1 100
D ₅	1 101
D ₆	1 110

- D₀ - AND
- D₁ - ADD
- D₂ - LDA
- D₃ - STA
- D₄ - BUN
- D₅ - BSA
- D₆ - ISZ

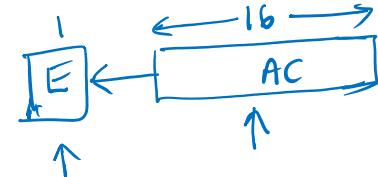
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✓
 $D_7 = 1$

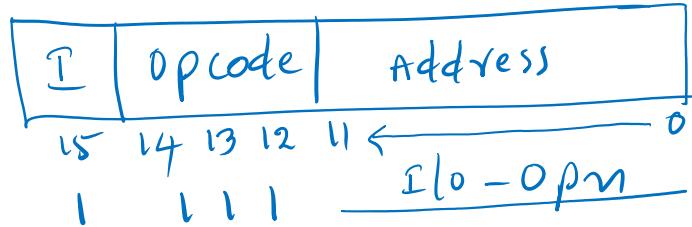
$I = 0$ (Register-Ref)



0111	1000	0000	0000
0111	0100	0000	0000
0111	0010	0000	0000
0111	0001	0000	0000
0111	0000	1000	0000
0111	0000	0100	0000
0111	0000	0010	0000
0111	0000	0001	0000
0111	0000	0000	1000
0111	0000	0000	0100
0111	0000	0000	0010
0111	0000	0000	0001



- 7800 → CLA
- 7400 → CLE
- 7200 → CMA
- 7100 → CME
- 7080 → CIR
- 7040 → CIL
- 7020 → INC
- 7010 → SPA
- 7008 → SNA
- 7004 → SZA
- 7002 → SZE
- 7001 → HALT

I/O- Reference Instructions

1111	1000 0000 0000	<u>F800</u>	<u>INP</u>
1111	0100 0000 0000	<u>F400</u>	<u>OUT</u>
1111	0010 0000 0000	<u>F200</u>	<u>SKI</u>
1111	0001 0000 0000	<u>F100</u>	<u>SKO</u>
1111	0000 1000 0000	<u>F080</u>	<u>ION</u>
1111	0000 0100 0000	<u>F040</u>	<u>IOF</u>