



Computer Organization and Architecture

Cache memory organization part-2

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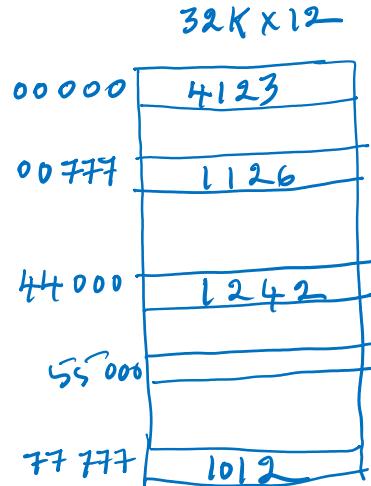
- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



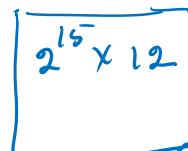
Cache memory organization part-2

15-bits 9 bits

SET-Associative Mapping

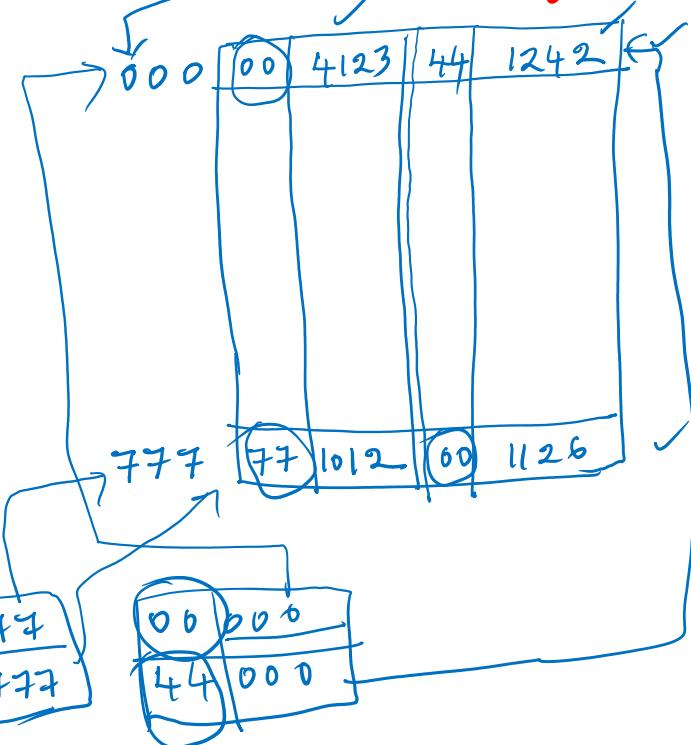


Main Memory



Cache Miss

2-way Set Associative



Cache memory organization part-2

No. of Sets in the Cache = $\frac{\text{No. of Blocks}}{n}$ [For n-way set associative]

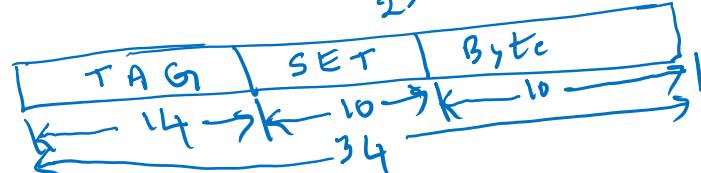
An n-way set associative Cache Contains n-blocks Per Set.



Example :— Cache Size 8 M bytes, Block Size = 1Kbytes
34 bits Addresses, 8-way set-associative

$$\text{No. of Blocks} = \frac{8\text{MB}}{1\text{KB}} = \frac{2^{23}}{2^{10}} = 2^{13}$$

$$\text{No. of Sets} = \frac{2^{13}}{8} = \frac{2^{13}}{2^3} = 2^{10} \text{ sets}$$



Cache memory organization part-2

Example:-

16 blocks,

4-way set-Associative

Cache Block Placement via Set-Associative Mapping

$$\text{Cache Set. Number} = \frac{(\text{Main. Memory}) \bmod (\text{No. of sets in Cache})}{\text{Block. No.}}$$

$$\text{No. of sets} = \frac{16}{4} = 4$$

14, 13, 5, 4, 8, 17, 7, 19,
 6, 5, 21, 23, 34, 23

$$14 \bmod 4 = 2$$

$$13 \bmod 4 = 1$$

$$5 \bmod 4 = 1$$

$$4 \bmod 4 = 0$$

Cache memory

S0	4, 8
S1	33, 23, 5, 17, 21
S2	14, 6, 34
S3	7, 19, 23

LRU

Cache memory organization part-2

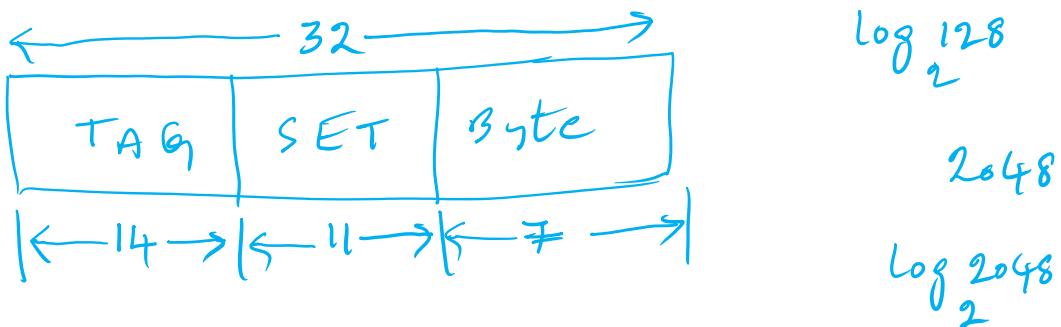
1 Mbytes

Cache Size

$$2048 \times 4 \times 128 \text{ Bytes}$$

$$2^{11} 2^2 2^7 = 2^{20}$$

→ A 4-way set-associative Cache has block size of 128 Bytes. It has total 2048 sets. If main memory address is 32 bits, what are the no. of bits used for TAG, set-offset, byte offset respectively?



(14, 5, 7)

Cache memory organization part-2

2-way
4-way
8-way
16-way

→ If the associativity of a processor cache is doubled while keeping the capacity and block size unchanged, which one of the following is guaranteed to be NOT affected?

- (A) Width of tag comparator
- (B) Width of SET index decoder
- (C) Width of way selection multiplexor
- (D) Width of processor to main memory data bus

Cache memory organization part-2

$$\frac{256 \text{ KBytes}}{32 \text{ Bytes}}$$

- A computer has a 256 KByte, 4-way set associative, write back data cache with entry block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

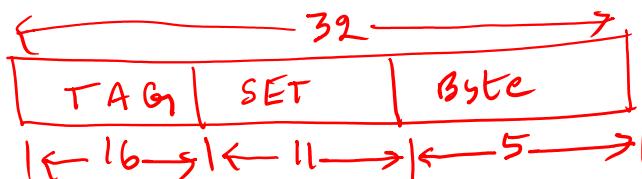
The number of bits in the tag field of an address is

- A. 11
- B. 14
- C. 16
- D. 27

$$\text{No. of Blocks} = \frac{256 \text{ KB}}{32 \text{ B}}$$

$$= \frac{2^{18}}{2^5} = 2^{13}$$

$$\text{No. of Sets} = \frac{2^{13}}{4} = \boxed{2 \text{ sets}}$$



Cache memory organization part-2

$$16 + 2 + 1 + 1$$

20 bits

- A computer has a 256 KByte, 4-way set associative, write back data cache with entry block size of 32 Bytes. The processor sends 32 bit addresses to the cache controller. Each cache tag directory entry contains, in addition to address tag, 2 valid bits, 1 modified bit and 1 replacement bit.

The size of the cache tag directory is

- A. 160 Kbits
- B. 136 Kbits
- C. 40 Kbits
- D. 32 Kbits

$$16 + 2 + 1 + 1$$

20 bits

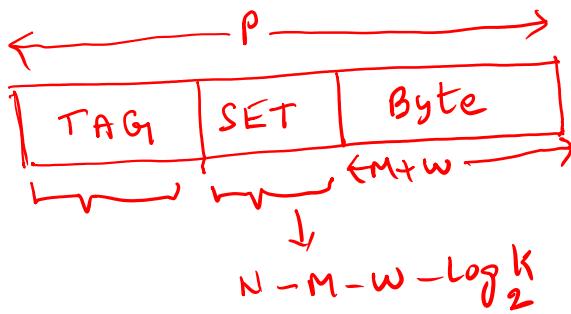
2^{13} Blocks

$2^{13} \times 20$ bits

$2^{10} \times 2^3 \times 20$ bits

160 K bits

Cache memory organization part-2



$$P = [N - M - W - \log_2 K + M + W]$$

$$P = [N - \log_2 K]$$

$$P = N + \log_2 K$$

- The size of the physical address space of a processor is 2^P bytes. The word length is 2^W bytes. The capacity of cache memory is 2^N bytes. The size of each cache block is 2^M words. For a K -way set-associative cache memory, the length (in number of bits) of the tag field is

- A. $P - N - \log_2 K$
- B. $P - N + \log_2 K$
- C. $P - N - M - W - \log_2 K$
- D. $P - N - M - W + \log_2 K$

$$\begin{aligned} \text{Block Size} &= 2^M \times 2^W \text{ bytes} \\ &= 2^{M+W} \text{ bytes} \end{aligned}$$

$$\text{No. of Blocks} = \frac{2^N}{2^{M+W}} = 2^{N-M-W}$$

$$\text{No. of Sets} = \frac{2^{N-M-W}}{K} = \frac{2^{N-M-W}}{2^{\log_2 K}}$$

$$= 2^{N-M-W-\log_2 K}$$

Cache memory organization part-2

4-way Set-Associativity

16384-Blocks

256 Bytes

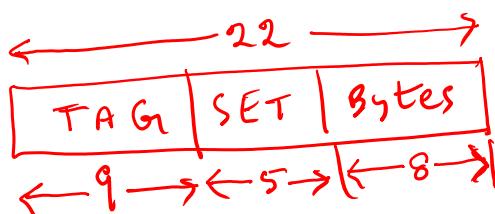
- A cache memory has 128 blocks and organizes 4-way set associativity. Main memory contains 16384 blocks. Each block contains 256, 8 bit words. How many bits are required for physical address and how many for tag comparator? [22 bits, 9 bits] ✓

$$2^{14}$$

$$\begin{aligned} \text{Size of Main Memory} &= \frac{16384}{2^{14}} \times \underline{256 \text{ Bytes}} \\ &= \underline{2^8} \end{aligned}$$

$$= 2^{22} \text{ Bytes}$$

$$\text{No. of Sets in Cache} = \frac{128}{4} = \frac{2^7}{2^2} = 2^5$$



Cache memory organization part-2

→ Cache Line and Cache block are same.

→ How big is a 8 – way SET- associative cache made up of 32 bit words, 4 words per line and having 2048 set-s?

- A. 128 kB
- B. 256 kB
- C. 512 kB
- D. 1024 kB

Cache Size
$$= (\text{No. of Sets}) \times (\text{size of each set}) \times (\text{size of each blocks})$$

$$\text{Cache Size} = 2048 \times 8 \times 4 \times \underline{32 \text{ bits}}$$

$$= 2048 \times 8 \times 4 \times 4 \text{ Bytes}$$

$$= 2^{11} \times 2^3 \times 2^2 \times 2^2 \quad ^{11}$$

$$= 2^{18} \text{ Bytes}$$

256 KBytes

Cache memory organization part-2

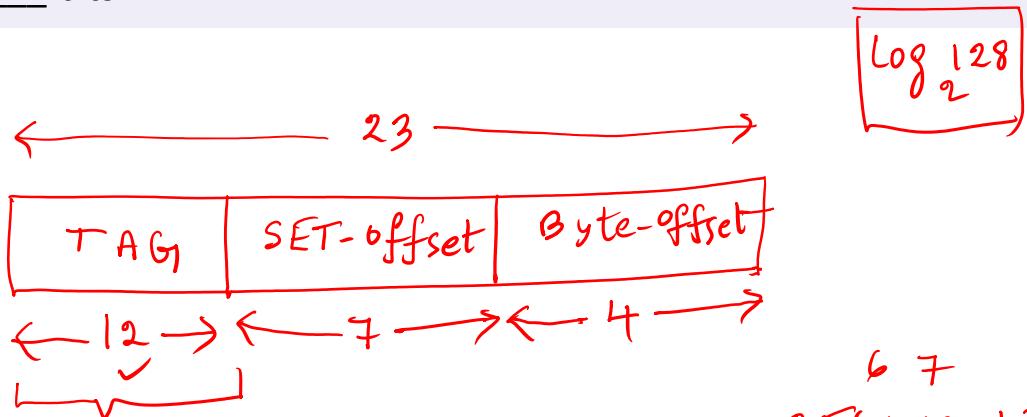
Block Size = 16 Bytes

2-way set

128 sets

23-bits

- A cache has a block size of 16 Bytes, and two way set-associative, Number of set-s is 128. CPU generates 23 bit addresses. The extra memory required in cache controller to store the TAG information is (3072) bits.



$$\begin{aligned} \text{No. of Blocks} &= \frac{128}{2} \times 2 \text{ blocks} \\ &= \underline{\underline{256 \text{ blocks}}} \end{aligned}$$

$$\begin{aligned} &\frac{256 \times 12}{3072} \text{ bits} \\ &\underline{\underline{3072 \text{ bits}}} \end{aligned}$$

Cache memory organization part-2

16-way Set associative Cache

2^m -way Set Associative

n -bits

direct
mapped

- A cache memory unit with a capacity of N words and block size of B words is to be designed. If it is designed as a direct mapped cache, the length of the TAG field is 10 bits. If the cache unit is now designed as a 16-way set-associative cache, the length of the TAG field is 14 bits.

16-way

Cache Capacity = N words

2⁴-way

Block Size = B words

$10 + 4 = 14$

Direct Mapped [TAG = 10 bits]

↑



Cache memory organization part-2

* what is the size of extra memory required in the Cache Controller for storing TAG info?

$$2^9 \text{ blocks} \times 20 \text{ bits} = 10 \text{ Kbits}$$

- A 4-way set-associative cache memory unit with a capacity of 16KB is built using a block size of 8 words. The word length is 32 bits. The size of the physical address space is 4 GB. The number of bits for the TAG field is ? 20

$$\text{Block Size} = 8 \times 32 \text{ bits} = 32 \text{ Bytes}$$

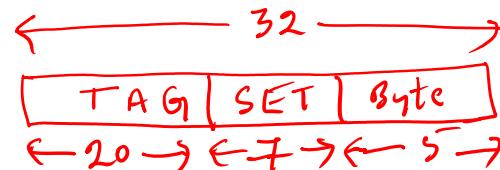
4-way Set
16 Kbytes

$$\text{No. of Blocks} = \frac{16 \text{ KB}}{32 \text{ B}} = \frac{14}{256} = 2^9 \text{ blocks}$$

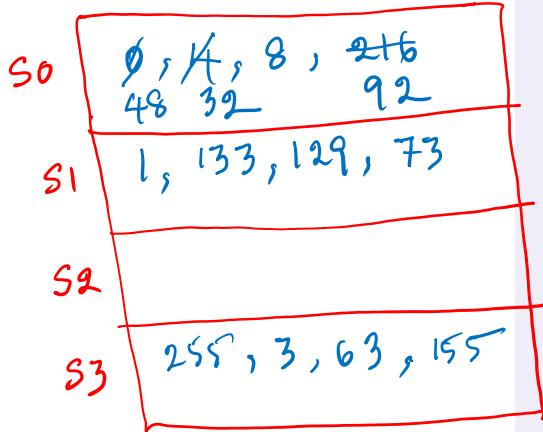
$$\text{No. of Sets} = \frac{2^9}{4} = 2^7 \text{ sets}$$

$$= 2^9 \text{ blocks}$$

$$4 \text{ GB} = 2^{32}$$



Cache memory organization part-2



→ Consider a 4 way set associative cache (initially empty) with total of 16 cache blocks . The main memory consists of 256 blocks and the requests for memory blocks is in the following order : 0,255,1,4,3,8,133,~~159~~,216,63,8,48,32,73,92,155. Which of the following memory blocks will NOT be in cache if LRU replacement policy is used ?

- A. 3 X
- B. 8 X
- C. 129 X
- D. 216

16 blocks
 $\text{No. of Sets} = \frac{16}{4} = 4 \text{ Sets}$

Cache Set No = $\left(\frac{\text{Main Mem.}}{\text{Block. No.}} \right) \bmod \left(\frac{\text{No. of Sets}}{\text{in Cache}} \right)$

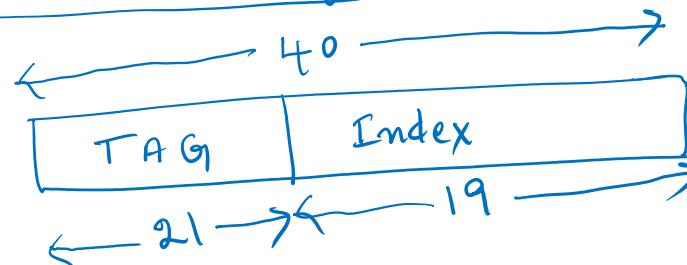
Cache memory organization part-2

40 bits
 512 K bytes
 8-way set-Associative
 $8 = 2^3$

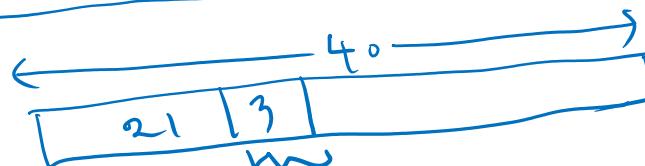
→ The width of the physical address on a machine is 40 bits. The width of the tag field in a 512 KB 8-way set associative cache is 24 bits.

$$\underline{512 \text{ bytes}} = \underline{2^{19} \text{ bytes}}$$

Direct-mapping



set-Associative Mapping



8-way set

2^n way
SET

n - bits

21 + 3

(24)