



Computer Organization and Architecture

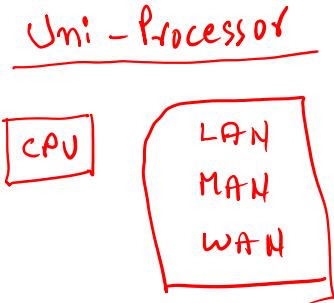
Basics of Multiprocessors

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

- MTech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD

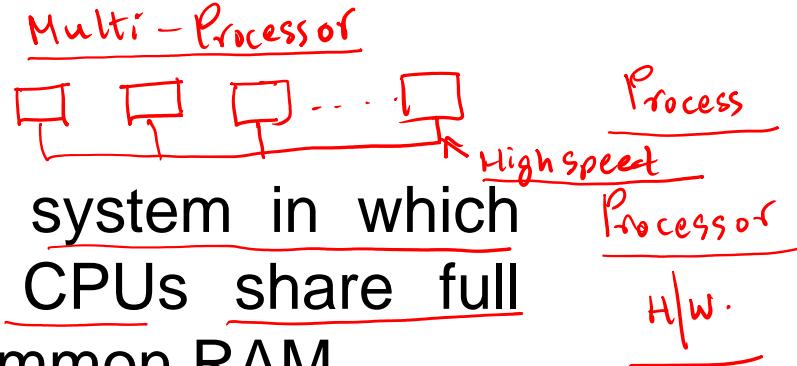


Basics of multiprocessors



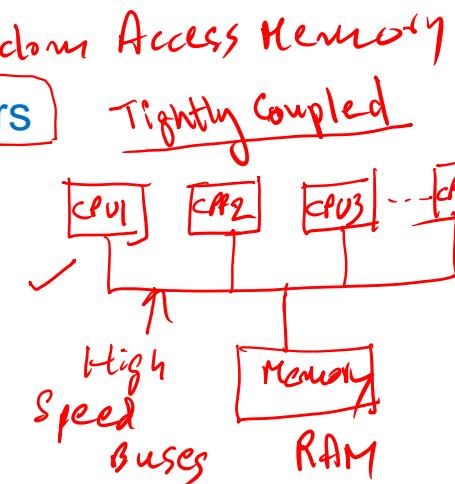
Definition:

- ✓ → A computer system in which two or more CPUs share full access to a common RAM



Continuous need for faster computers

- shared memory model ✓
- message passing multiprocessor
- wide area distributed system ✓

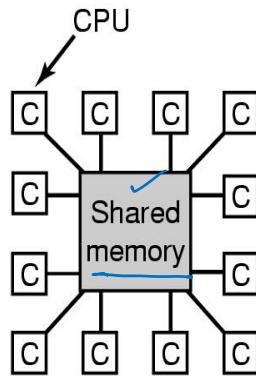


Basics of multiprocessors

Multiprocessor Systems

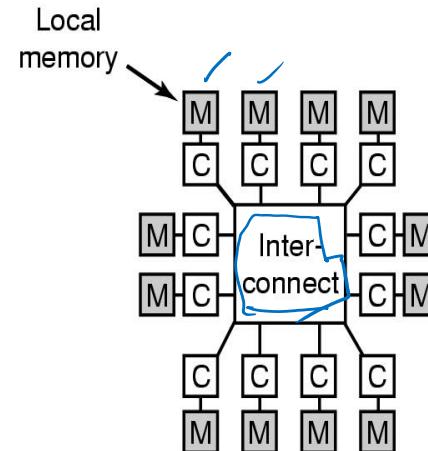
Shared Memory

Critical task

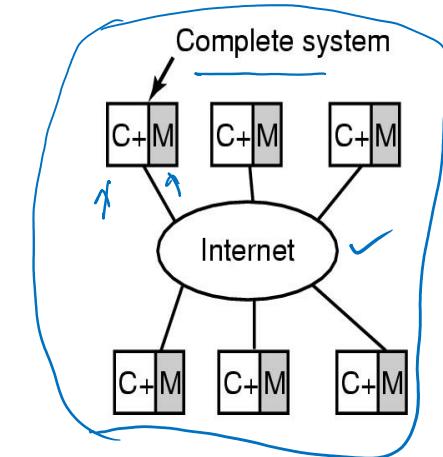


(a)

C - CPU
M - Memory (RAM)



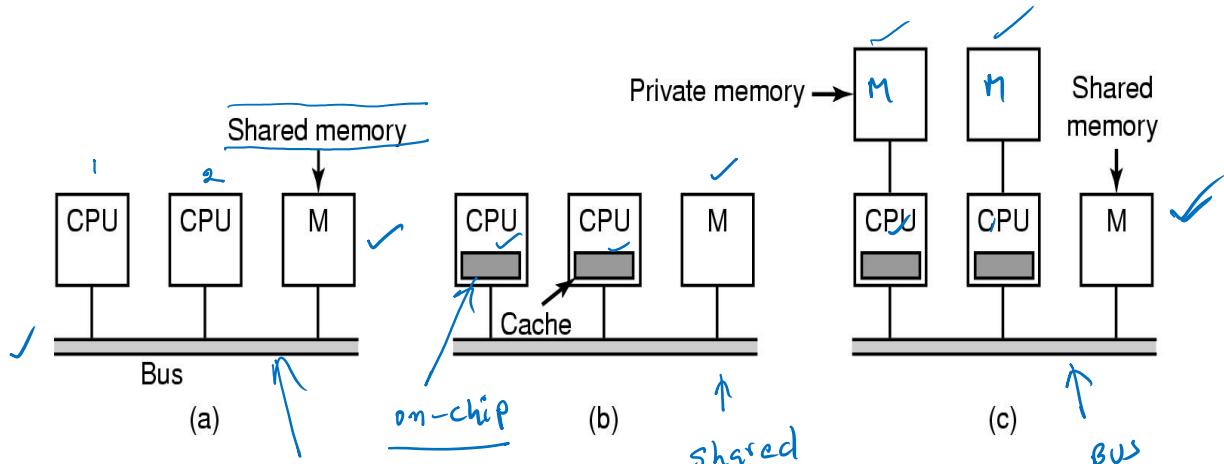
(b)



(c)

Basics of multiprocessors

Bus-based multiprocessors



→ Medium to Transfer the data among the processors

Basics of multiprocessors

Hardware

n inputs

m - output

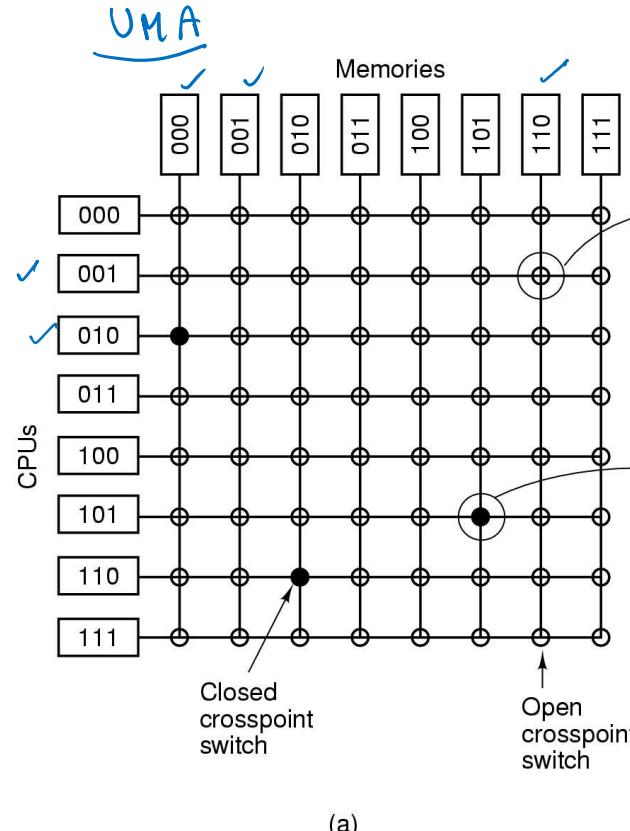
$n \times m$.

8x8
64

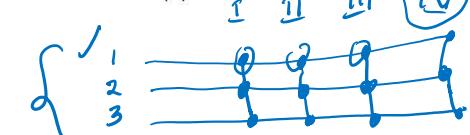
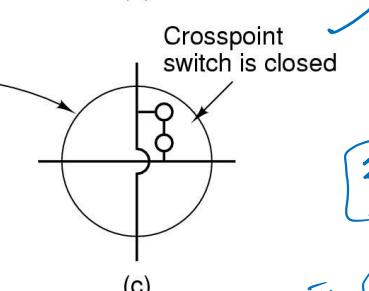
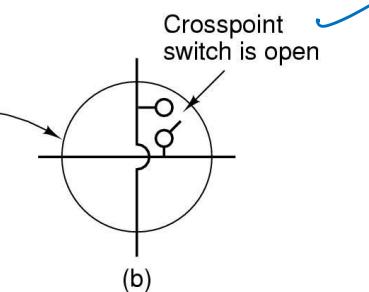
Cross - points

001 To 110

Uniform memory access multiprocessor using a crossbar switch



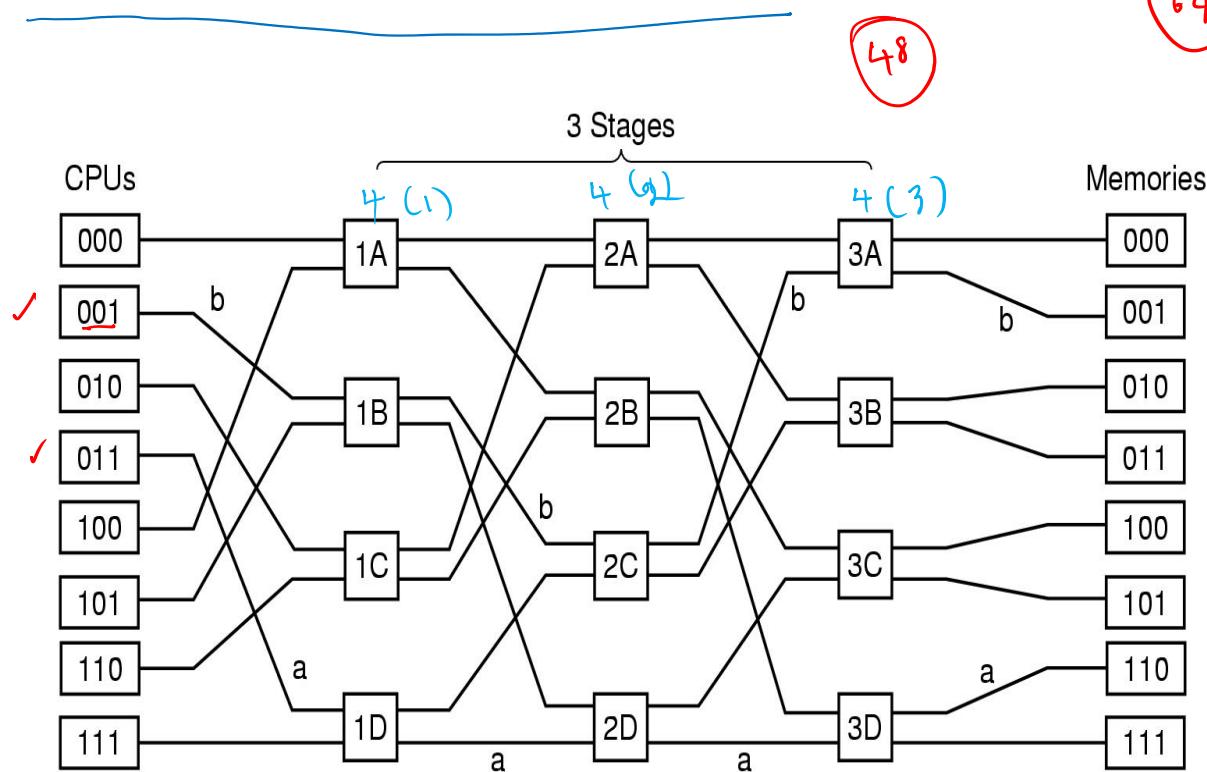
Electronic Micro-switches



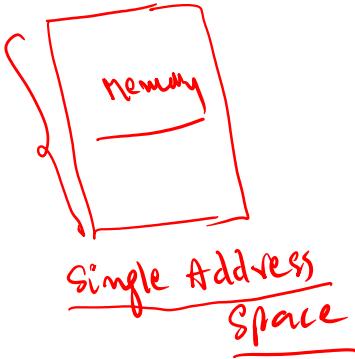
Basics of multiprocessors

UMA multiprocessors using multistage switching networks can be built from 2x2 switches

$$\begin{array}{r} 64 \\ \times f \\ \hline \end{array}$$



Basics of multiprocessors



Non-Uniform memory access Multiprocessor

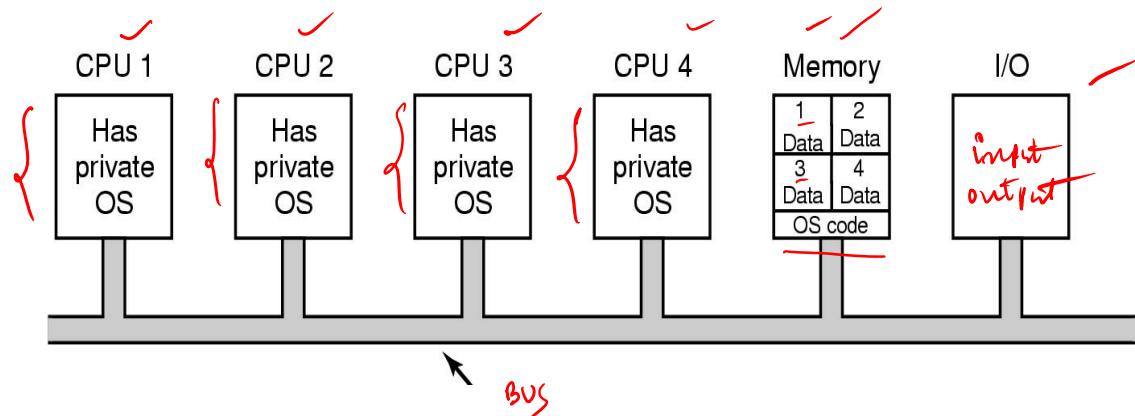
Characteristics

1. Single address space visible to all CPUs
2. Access to remote memory via commands
 - LOAD ✓
 - STORE ✓
3. Access to remote memory slower than to local

Basics of multiprocessors

Asymmetric Multiprocessors

Multiprocessor OS Types

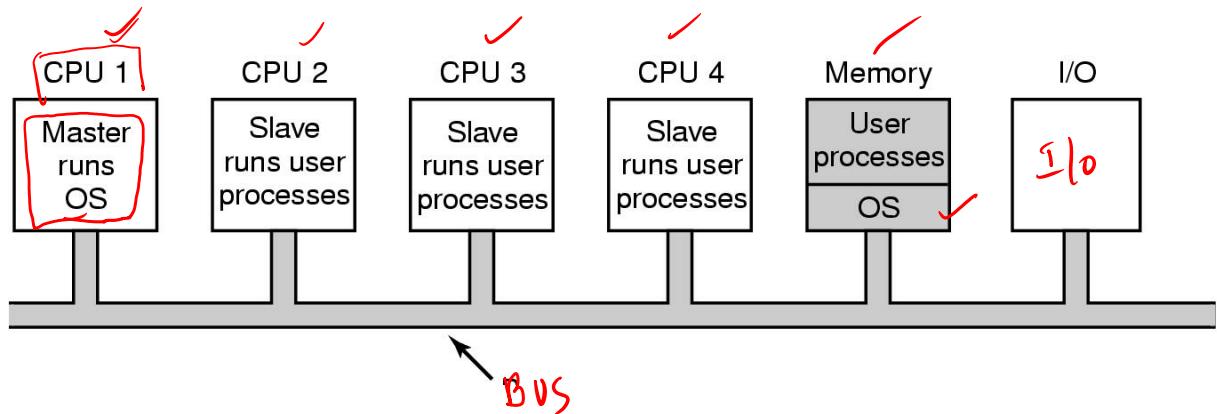


Each CPU has its own operating system

Basics of multiprocessors

Privileged [OS]

Master slave Multi-processor

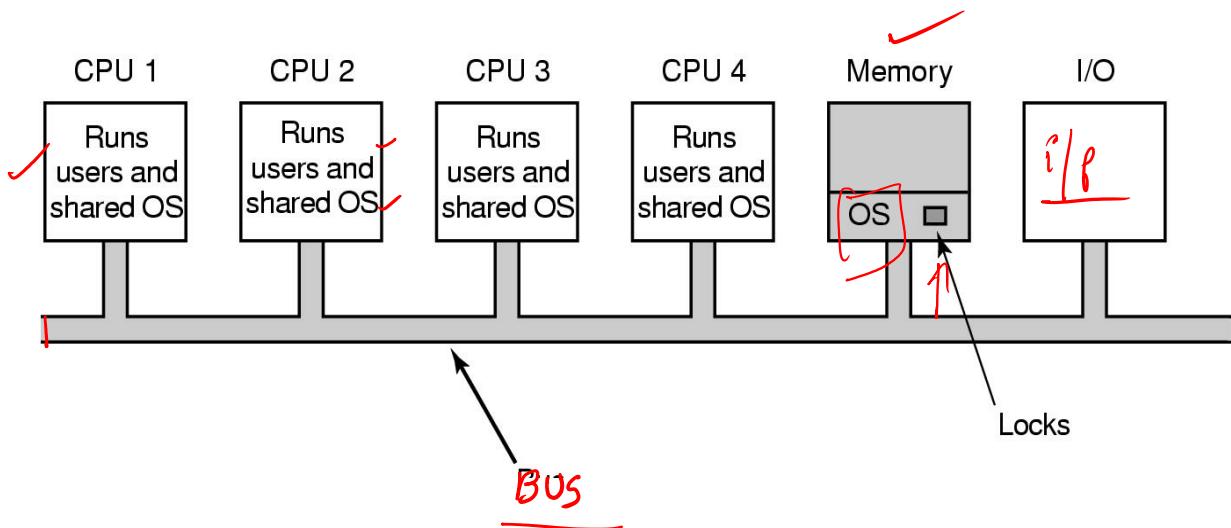


Basics of multiprocessors

- Symmetric Multiprocessors

Identical Copy of OS
is available at every
Processor.

Privileged
Nom. Privileged

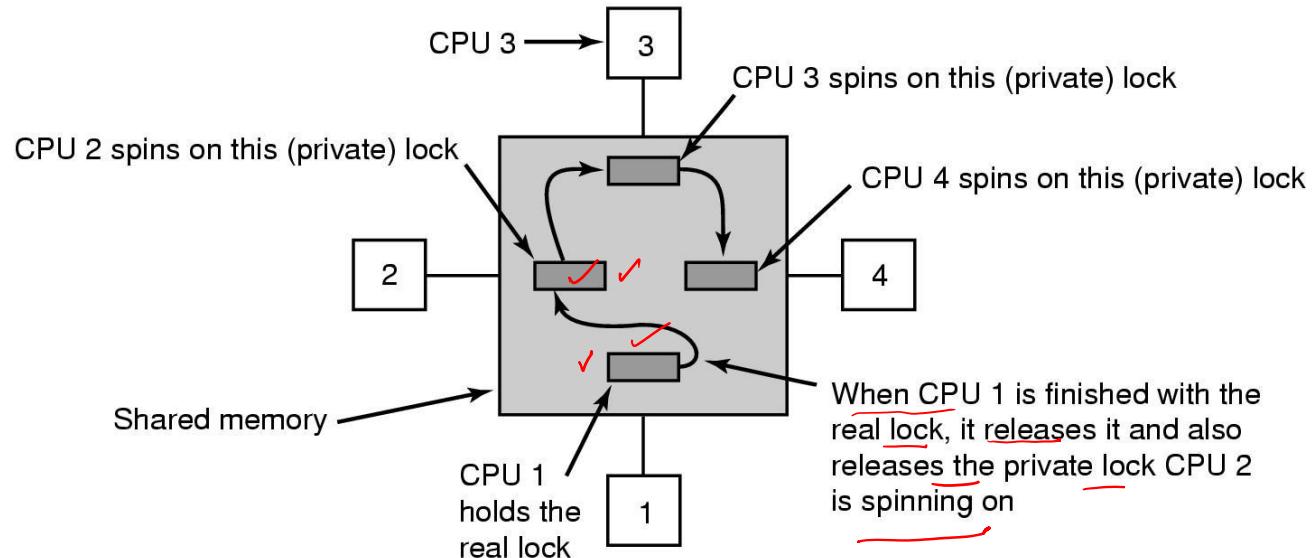


Basics of multiprocessors

Multiprocessor Synchronization

Uni-Processor

0.5



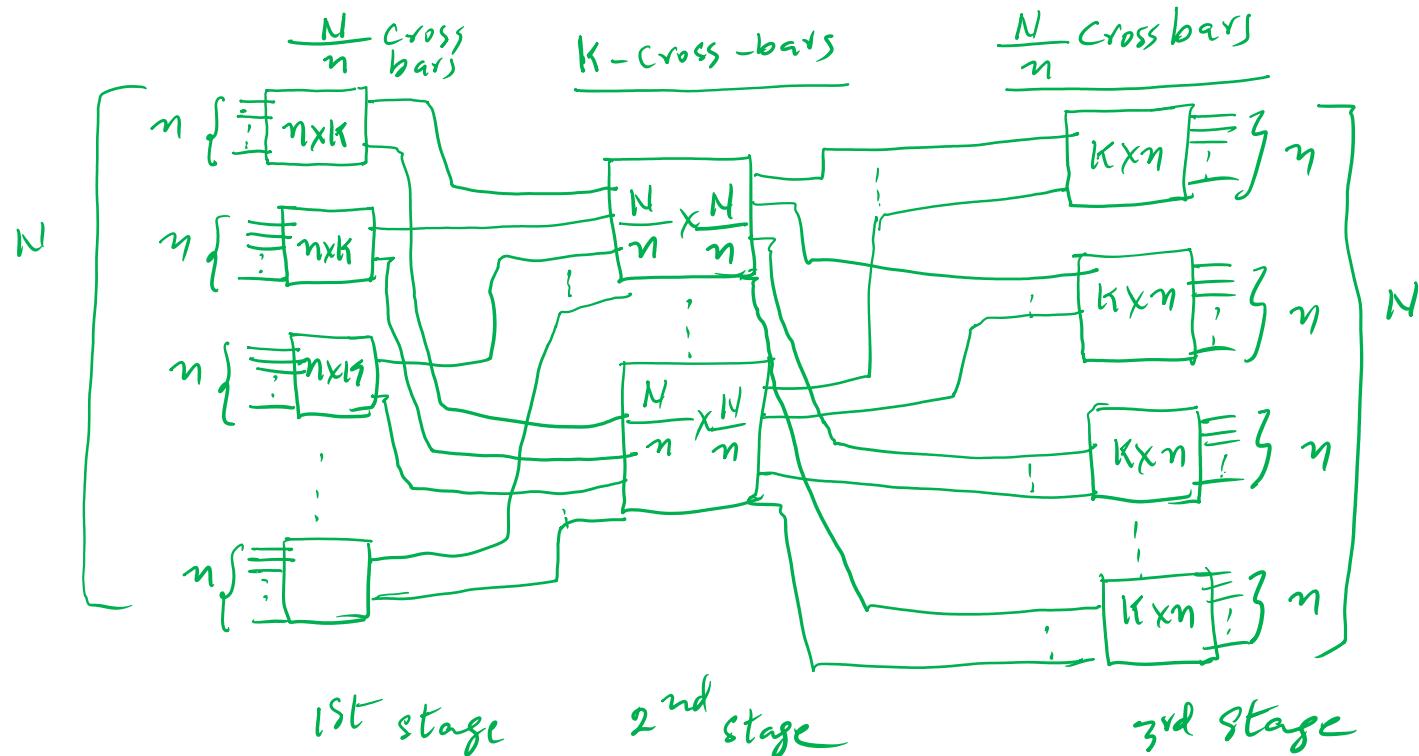
Basics of multiprocessors

Cross-bar switch

$$N \times N = N^2$$

Multi stage Cross-bar Switch

N to N



Basics of multiprocessors

Example:- 200×200

$$N = 200$$

Multi-stage

$$= 2 \times 200 \times 4 + 4 \left[\frac{200}{20} \right]$$

$$N \times N = \underline{N^2 \text{ cross-Points}} \cdot [\text{single stage}] \rightarrow$$

40000

Total cross-Points in Multistage

38000

$$= \frac{N}{n} [n \times k] + k \left[\frac{N}{n} \times \frac{N}{n} \right] + \frac{N}{n} [k \times n]$$

$$= NK + K \left[\frac{N}{n} \right]^2 + NK$$

$$K = 4$$

$$n = 20$$

$$= 2NK + K \left[\frac{N}{n} \right]^2$$

$$200$$

(20)

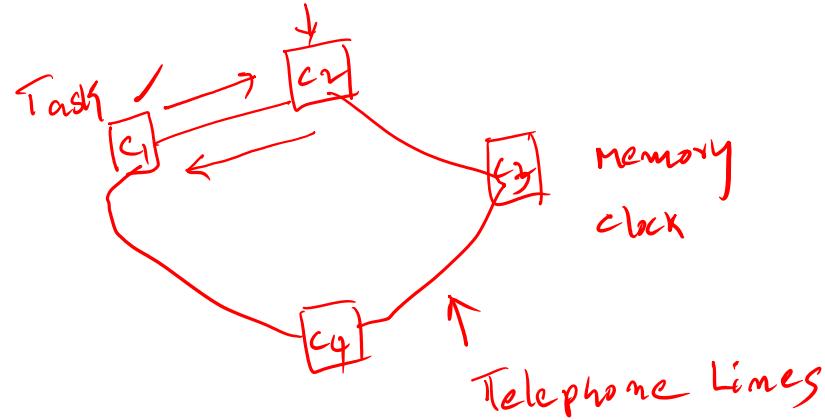
$$= 1600 + 4 \times 100$$

$$= \underline{2000 \text{ cross-Points}}$$

Basics of multiprocessors

LAN
MAN
WAN

Distributed System (Loosely Coupled System)



Basics of multiprocessors

Example :-

$$\begin{array}{r}
 +10 \\
 +10 \\
 \hline
 +20
 \end{array}
 \quad
 \begin{array}{r}
 +10 \\
 +10 \\
 \hline
 +20
 \end{array}
 \quad
 \begin{array}{r}
 001010 \\
 010100 \\
 \hline
 010100
 \end{array}$$

(0) ↑ V = 0 ⊕ 0 = 0
 z = 0 C = 0 S = 0

Processor-status word.

S	C	V	Z
---	---	---	---



$$\begin{array}{r}
 A = A_3 A_2 A_1 A_0 \\
 B = B_3 B_2 B_1 B_0 \\
 \hline
 C = C_3 C_2 C_1 C_0
 \end{array}$$

A+B

$$\begin{array}{r}
 C_4 \\
 \hline
 S_3 S_2 S_1 S_0
 \end{array}$$



$$\begin{array}{r}
 V = C_3 \oplus C_4 \\
 Z = 1 [0000]
 \end{array}$$

$$\begin{array}{r}
 S_3 S_2 S_1 S_0 \\
 \hline
 0
 \end{array}$$

Signed integer

$$\begin{array}{r}
 +10 \\
 +10 \\
 \hline
 +20
 \end{array}$$

(0) ↓
 0 1010
 0 1010
 1 01
 1 0100

S = 1

$$C = 0, \quad V = 0 \oplus 1 = 1$$

Basics of multiprocessors

Assume that

$$R_1 = 100$$

R_1 is a 8-bit register.

$$V = ?$$

$$S = ?$$

$$C = ?$$

$$Z = ?$$

$$CF = 0$$

$$SF = 1$$

$$OV = 0 \oplus 1 = 1$$

$$ZF = 0$$

ADD $R_1, \# -50 ; R_1 \leftarrow R_1 + -50$

$$\begin{array}{r}
 & 100 \\
 + & 50 \\
 \hline
 & 150
 \end{array}$$

64
 32
 4
 100

0 1100100
 0 0110010
 1 1
 1 0010110

50

① ↑
 ↗

$$\begin{array}{r}
 & 32 \\
 & 16 \\
 & 12 \\
 \hline
 & 50
 \end{array}$$