



gradeup

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Computer Organization and Architecture

Sequential Circuits

ABOUT ME : MURALIKRISHNA BUKKASAMUDRAM

- M.Tech with 20 years of Experience in Teaching GATE and Engineering colleges
- IIT NPTEL Course topper in Theory of computation with 96 %
- IGIP Certified (Certification on International Engineering educator)
- GATE Qualified
- Trained more than 50 Thousand students across the country
- Area of Expertise : TOC,OS,COA,CN,DLD



Sequential Circuits

Counter

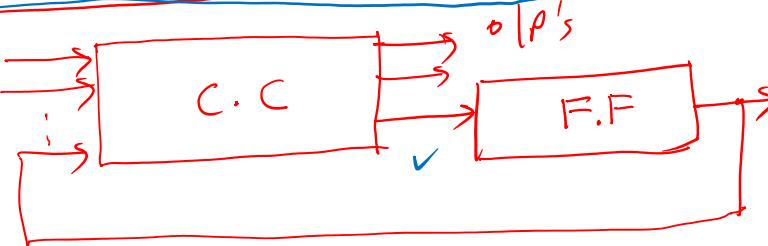
Up-Counter

- ✓ 00
- ✓ 01
- ✓ 10
- ✓ 11

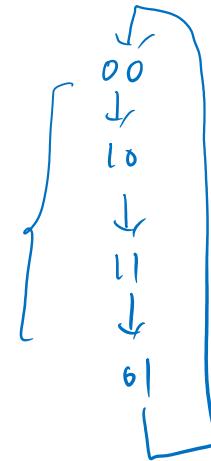
(2 bits)
Down-Counter

- 00
- ↓
- 11 → 10 → 01

SEQUENTIAL Circuit Block Diagram



- (1) Synchronous Sequential Circuits
- (2) Asynchronous

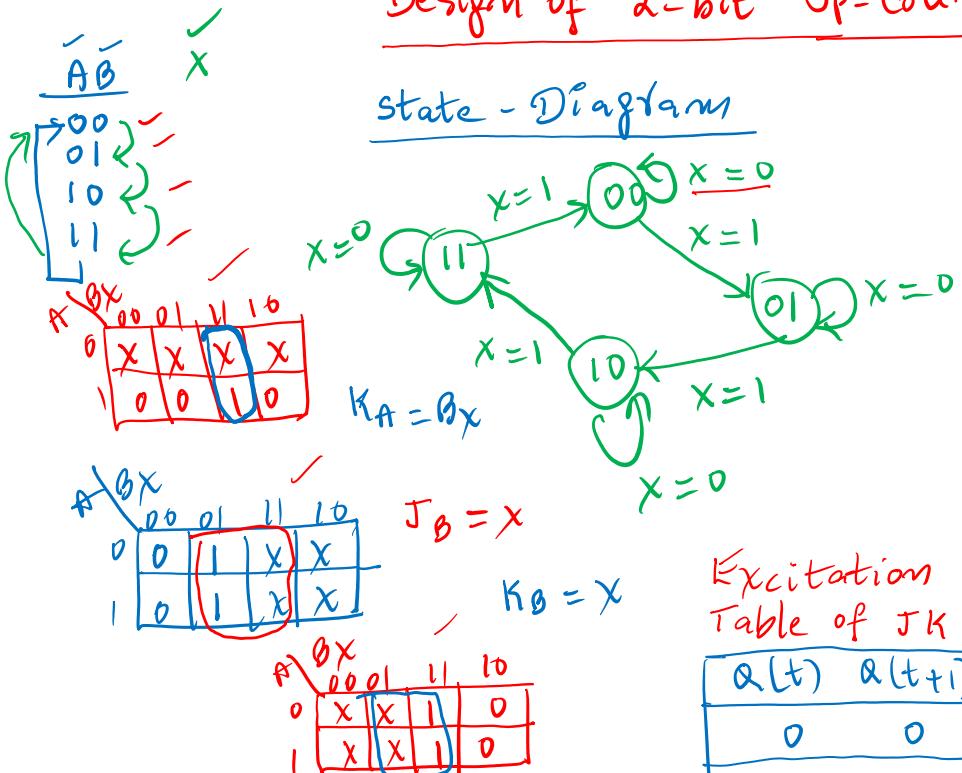


Design Process

- (1) Problem statement
- (2) state Diagram
- (3) Select flip flops
- (4) Flip Flop i/p's
- (5) Circuit Diagram

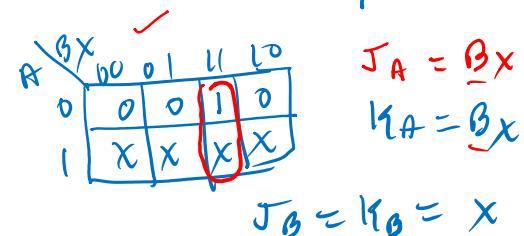
Sequential Circuits

Design of 2-bit Up-counter using JK-flip flops



$Q(t)$	$Q(t+1)$	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

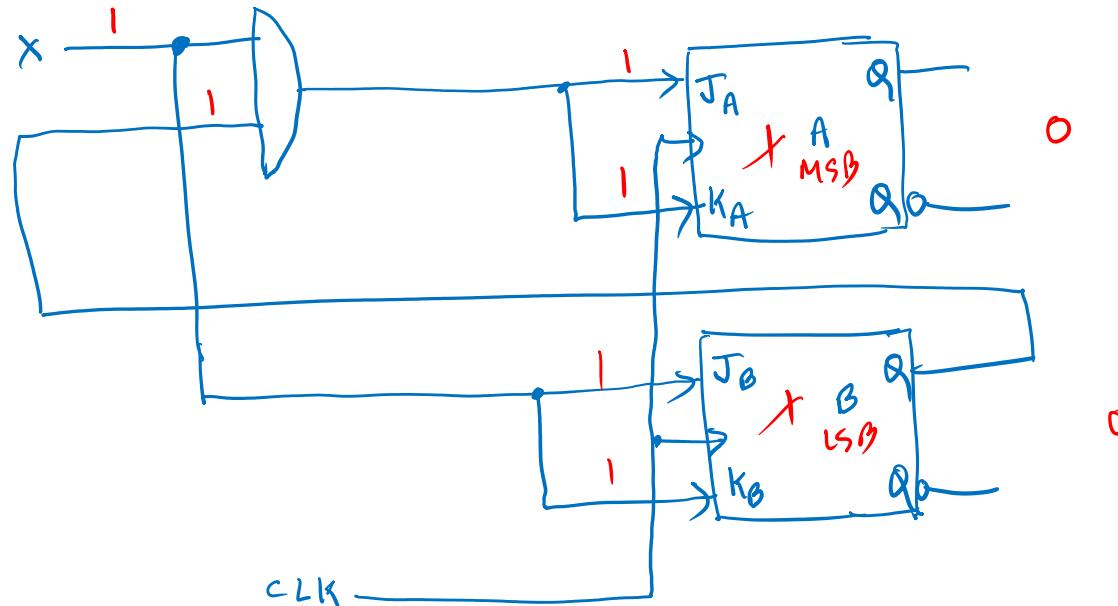
Present		$i \mid p$	Next state		Flip Flop i p's			
A	B		A	B	J _A	K _A	J _B	K _B
0	0	0	0	0	0	X	0	X
0	0	1	0	1	0	X	1	X
0	1	0	0	1	0	X	X	0
0	1	1	1	0	1	X	X	1
1	0	0	1	0	1	X	0	X
1	0	1	1	1	X	0	1	X
1	1	0	1	1	X	0	X	0
1	1	1	0	0	0	1	X	0



Sequential Circuits

Logic Circuit of 2-bit Upcounter

$\begin{array}{l} \text{A} \\ \text{B} \end{array}$
11
00



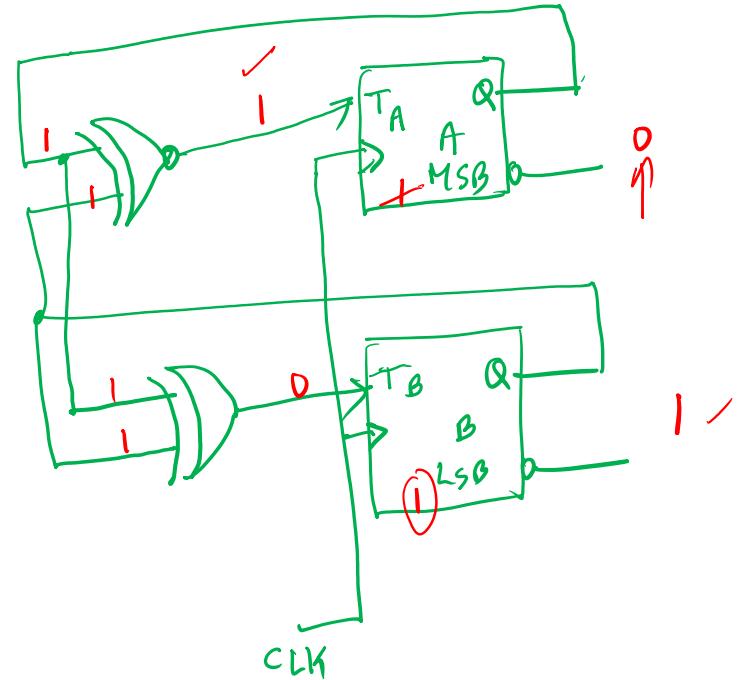
Sequential Circuits

→ Design a Circuit for the Count Sequence 0-2-3-1-0---
 using T-flip flops



(1) ✓
 (0) ✓

Present		Next		FF i/p's	
A	B	A	B	T _A	T _B
0✓ 0		1✓ 0		1	0
1✓ 0		1✓ 1		0	1✓
1✓ 1		0✓ 1		1	0
0✓ 1		0✓ 0		0	1✓



$$T_A = A'B' + AB$$

$$T_A = \underline{A \oplus B} \quad \checkmark$$

$$T_B = AB' + A'B$$

$$T_B = \underline{A \oplus B} \quad \checkmark$$

Sequential Circuits

Design of 2-bit binary Down Counter using T-flip flops



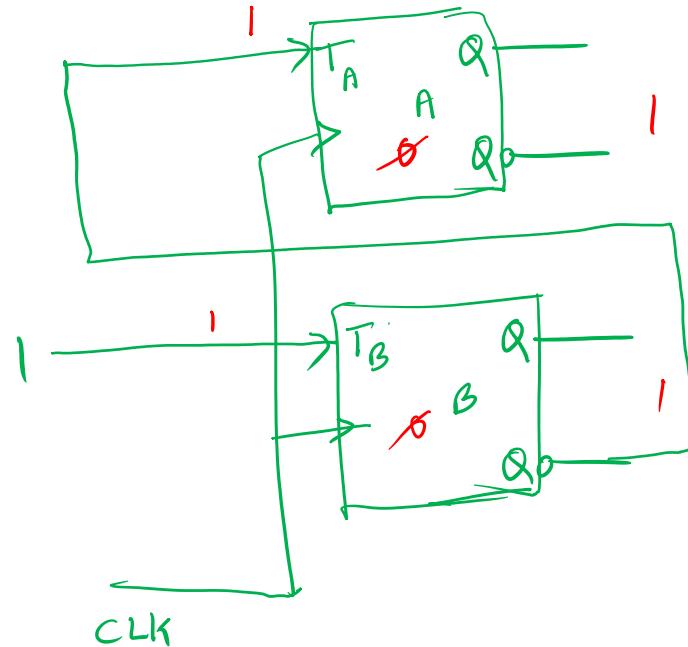
Present		Next		FF i/p's	
A	B	A	B	T _A	T _B
0✓	0✓	1✓	1✓	1✓	1
1✓	1✓	1✓	0✓	0	1
1✓	0✓	0✓	1✓	1✓	1
0✓	1✓	0✓	0✓	0	1

$$T_A = A'B' + AB'$$

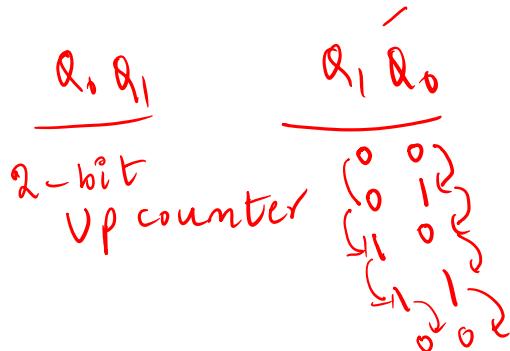
$$T_A = (A' + A)B'$$

$$T_A = B'$$

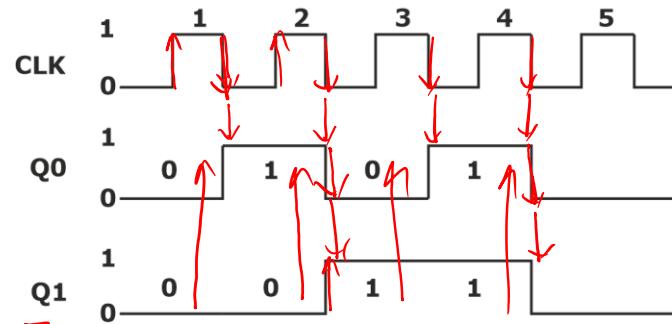
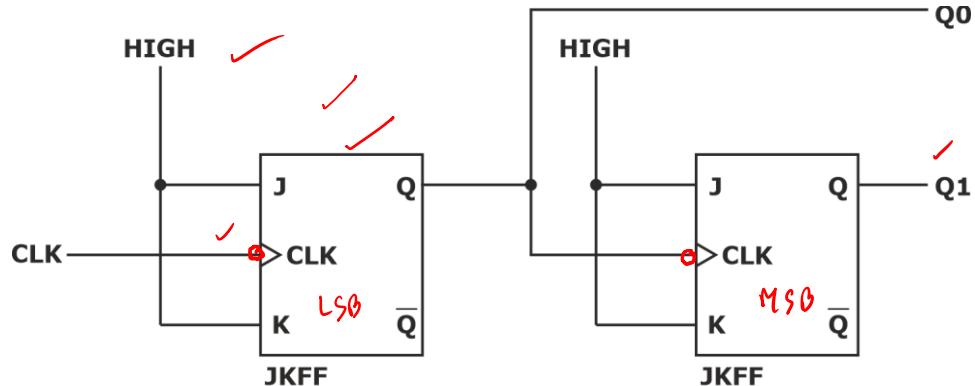
$$T_B = 1$$



Asynchronous sequential circuits



2-Bit Asynchronous Counter (ripple counter)

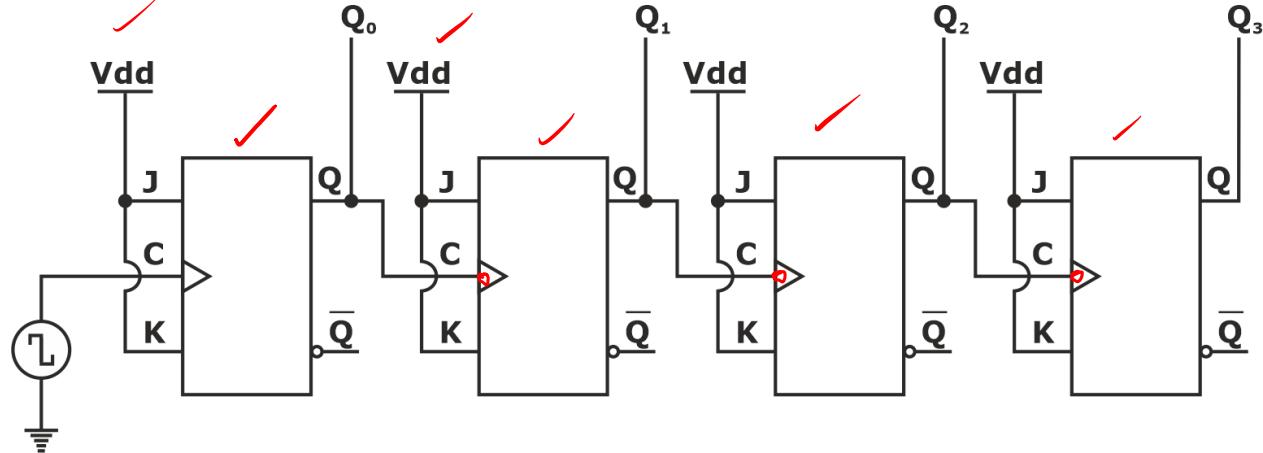


Asynchronous sequential circuits

$Q_3 Q_2 Q_1 Q_0$

Voltage

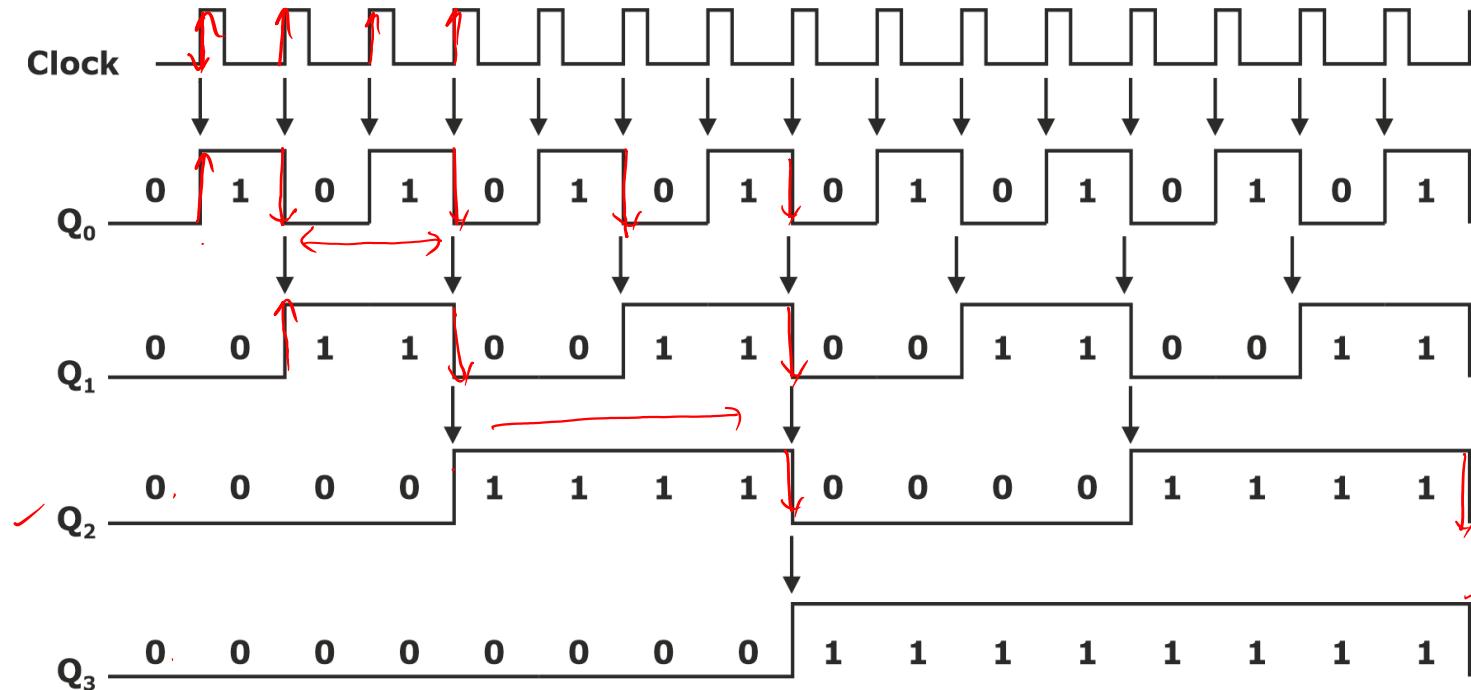
Four-bit Up-Counter



Asynchronous sequential circuits

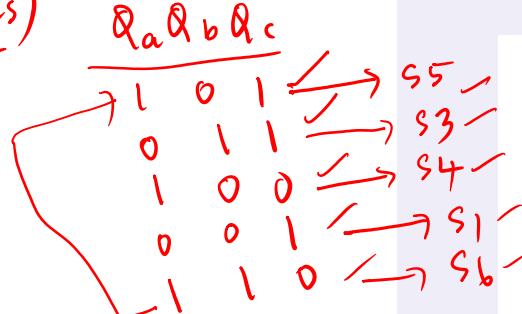
$Q_3 Q_2 Q_1 Q_0$

0	0	0	0
0	0	0	1
⋮	⋮	⋮	⋮

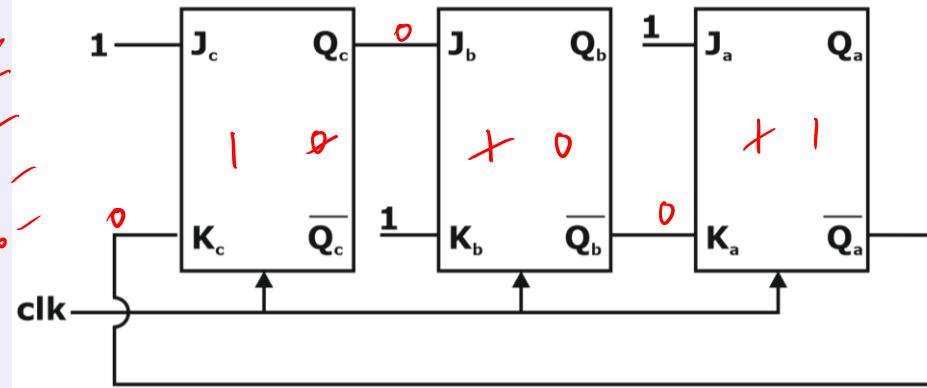


Sequential Circuits

n-different States
n (modulus)



1. Consider the following counter. Here Q_a denotes MSB.

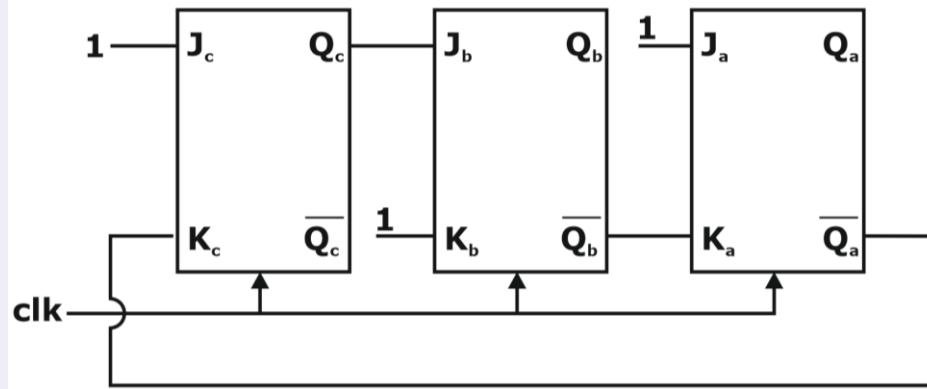


Assume initial state as S_5 (i.e. 101) what would be the modulus of the counter ?

- A. 7
- B. 4
- C. 5
- D. 8

Sequential Circuits

2. Consider the following counter. Here Q_a denotes MSB.



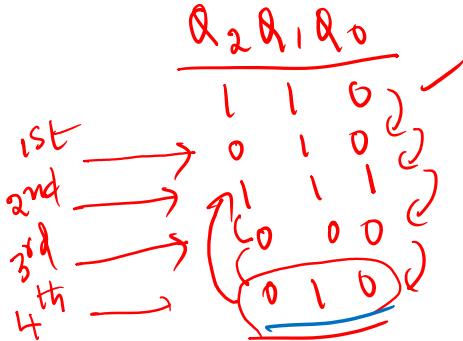
In the above case which of the following states are not reached ?

- A. S_0, S_1, S_6, S_3
- B. S_0, S_2, S_7
- C. S_0 only
- D. All states are reached

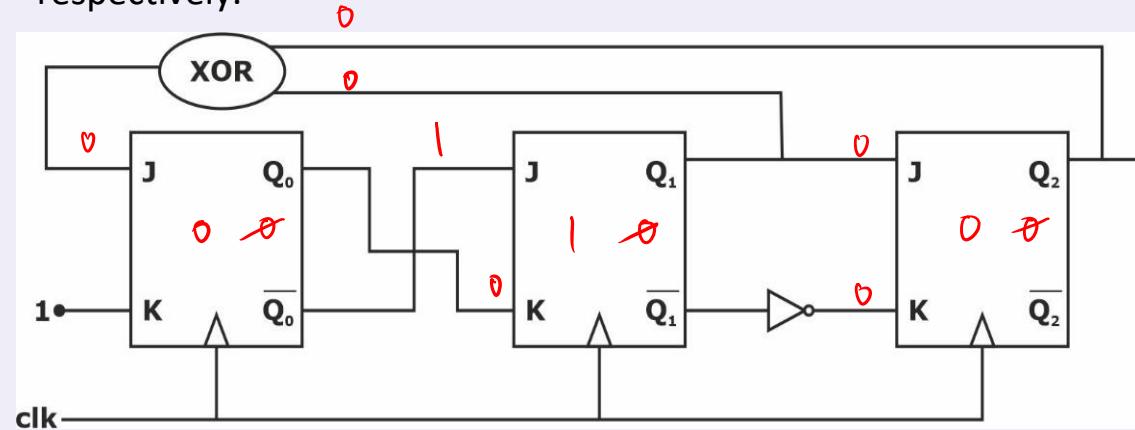
S_1, S_3, S_4, S_1, S_6

S_0, S_2, S_7

Sequential Circuits



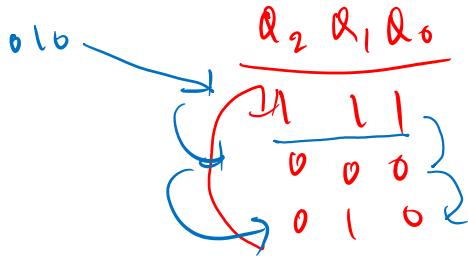
3. Consider the following circuit with initial state Q_2, Q_1, Q_0 as 110 respectively.



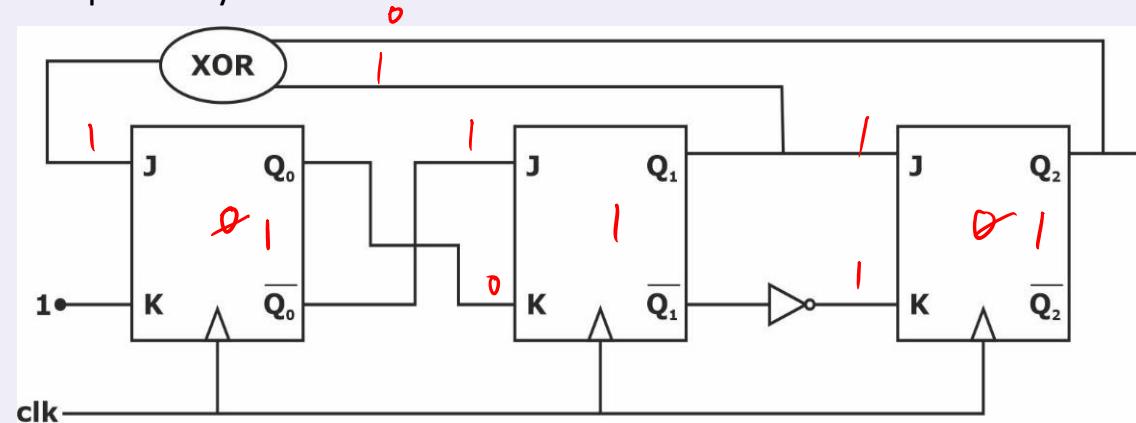
What is the contents of Q_2, Q_1, Q_0 after 4th clock cycle ?

- A. 000
- B. 111
- C. 011
- D. 010

Sequential Circuits



4. Consider the following circuit with initial state Q_2, Q_1, Q_0 as 110 respectively.



After reaching the state (as obtained from above), after how many clock pulse will reach the initial state (110) for the second time ?

- A. 3
- B. 4
- C. 5
- D. None of these

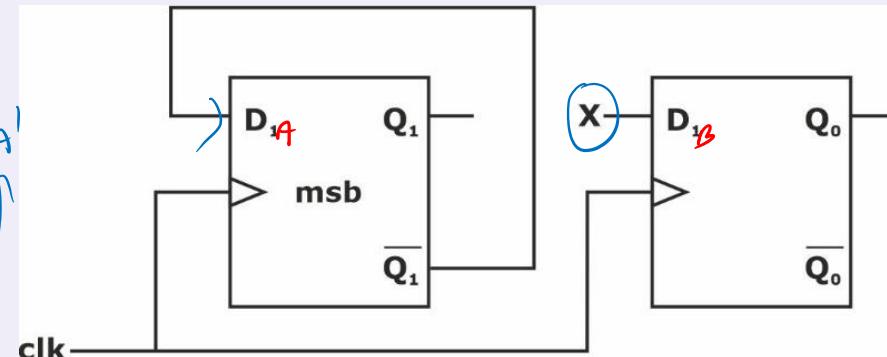
Sequential Circuits

<u>Present</u>	<u>Next</u>	<u>FF i/p's</u>
A B	A B	D _A D _B
0 0	1 0	1 0
1 0	0 1	0 1
0 1	1 1	1 1
1 1	0 0	0 0

$D_B = A'B + AB = A \oplus B$
 $D_A = A'B' + A'B = A'$

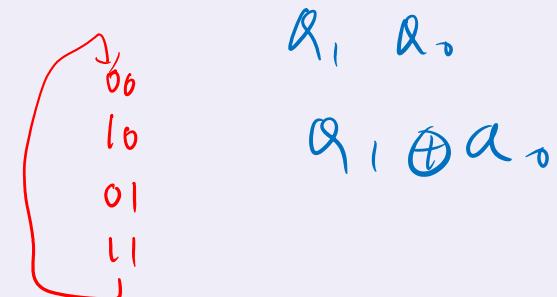
5. A 2-bit synchronous counter is to be designed using D-flip-flops, that passes through the sequence 0, 2, 1, 3, 0, 2,

Following is the partial implementation of the flip-flop.

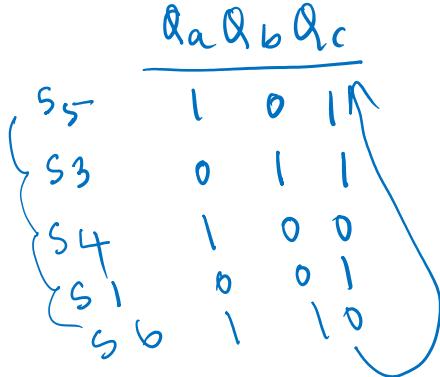


Determine x i.e., D₀ input.

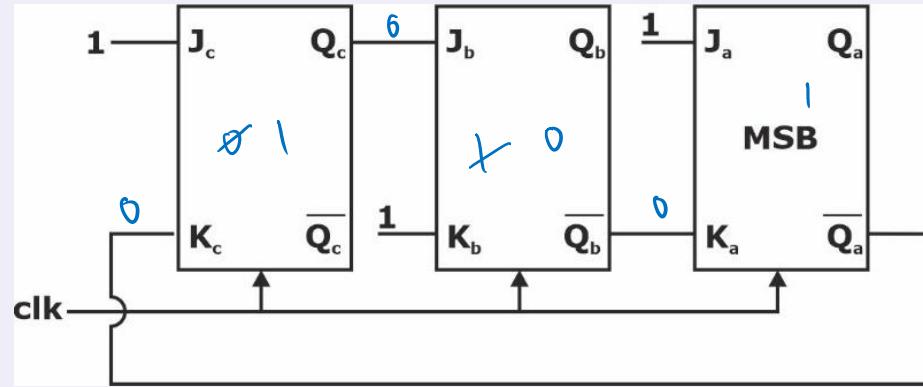
- A. Q₁
- B. $\overline{Q_0}$
- C. $Q_1 \oplus Q_0$
- D. $Q_1 \odot Q_0$



Sequential Circuits



6. Consider the following circuit of counter:



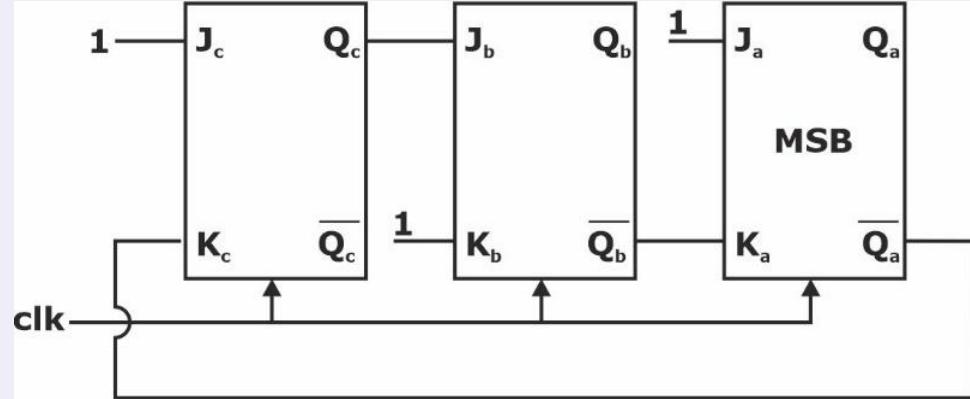
Which of the following is true regarding the above counter?

- A. $S_5 \rightarrow S_3 \rightarrow S_4 \rightarrow S_1 \rightarrow S_6$
- B. $S_3 \rightarrow S_5 \rightarrow S_4 \rightarrow S_1 \rightarrow S_6$
- C. $S_5 \rightarrow S_3 \rightarrow S_4 \rightarrow S_6 \rightarrow S_1$
- D. $S_5 \rightarrow S_4 \rightarrow S_3 \rightarrow S_1 \rightarrow S_6$

Sequential Circuits

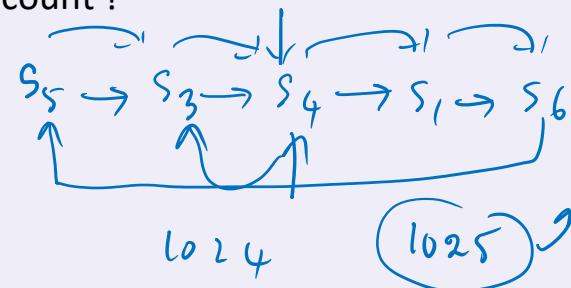
1020 (S_4)
 1021 (S_1)
 1022 (S_6)
 1023 (S_5)
 1024 (S_2)

7. Consider the following circuit of counter:



If current state is S_4 then after applying 1024 clock pulses what will be the state of sequential count ?

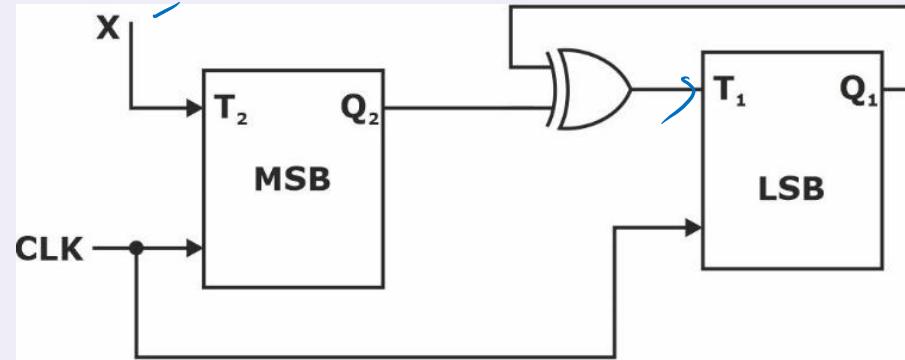
- A. S_4
- B. S_3
- C. S_2
- D. S_2S_1



Sequential Circuits

Present	Next	FF i P
$Q_2\ Q_1$	$Q_2\ Q_1$	$T_2\ T_1$
0 0	1 0	1 0
1 0	1 1	0 1
1 1	0 1	1 0
0 1	0 0	0 1

8. Consider partial implementation of the 2-bit counter using T-FFs for the sequence 0-2-3-1-0



The X in terms of Q_1, Q_2 is

- A. \bar{Q}_1
- B. $Q_1 \oplus Q_2$
- C. $Q_1 \odot Q_2$
- D. $\bar{Q}_1 + Q_2$

0 - 2 - 3 - 1 - 0

$$\bar{Q}_2 \bar{Q}_1 + Q_2 Q_1$$

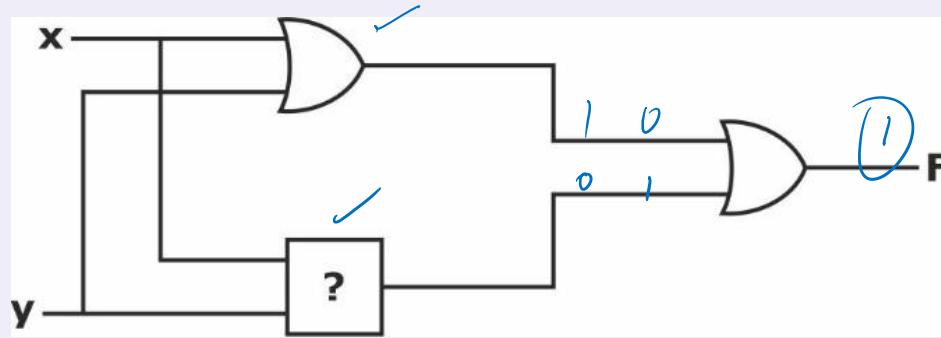
↑ ↑ ↑ ↑
00 10 11 01

$$Q_1 \oplus Q_2$$

Sequential Circuits

9. Consider the following circuit

In order to make it tautology the '?' Marked box should be replaced by



- A. OR gate
- B. AND gate
- C. XOR gate
- D. NOR gate

No R

