gradeup

Function of OSI and TCP/IP Layers Part-3

Functions of OSI and TCP/IP Part -3

Content :

1. Hamming code
2. Structure of Hamming Code
3. ARQ Technique
4. Flow Control

Hamming Code : It is linear block codes. The family of (n,k) hamming codes of m>= 3 is defined by the following equation:

- **Block length :** $n = 2^m - 1$
- **Number of message bits :** $k = 2^m - m - 1$
- **Number of parity bits :** $(n-k) = m$
- **Where . i.e. minimum number of parity in** 3.
- **The minimum distance** $d_{min} = 3$.
- **The code rate or code efficiency** = $k/n = (2^m - m-1) /2^{m-1} = 1 - m / 2^m-1$

  If m >> 1 then code rate r = 1 .

Error Detection And Correction Capabilities Of Hamming Code:

For the minimum distance $d_{min} = 3$

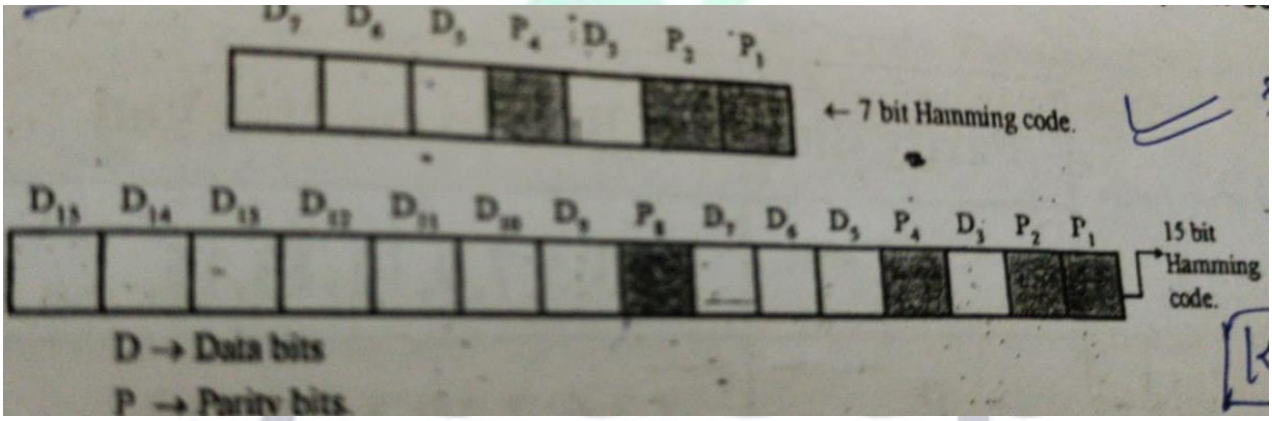
1. The number of errors that can be detected per word = 2
   Since d_{min}>= (s+1) i.e. 3 >=s+1 i.e. s<= 2

2. The number of errors that can be corrected per word = 1
   Since d_{min} >= (2t +1) i.e. 3>=(2t+1) t<= 2

Thus , with d_{min} = 3 it is possible to detect upto 2 errors and it is possible to correct upto only 1 error

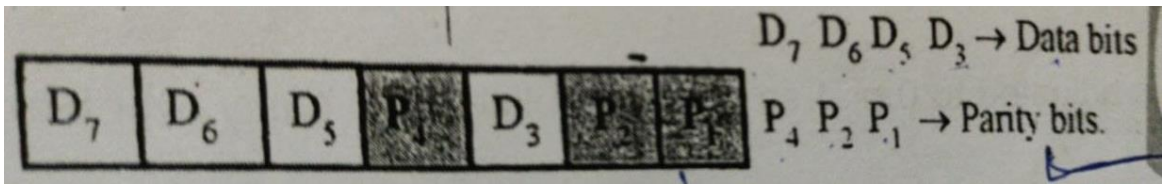
Hamming Code Structure :

- Hamming code is basically a linear block code named after its inventor .It is an error correcting code. The parity bits are instead in between the data bits as shown below
- The 7-bit hamming code is used commonly , but the concept can be extended to any number of bits .
- Note that the parity bits are inserted at each 2 bit where n = 0,1,2,3 …….. . Thus P_1 is at
  2^0 =1 i.e. at first bit , P_2 is at 2^2 and P_8 is at 2^3 as shown below



7-Bit hamming code

- A scientist named R.W. Hamming developed a coding system which was easy to implement . Assuming that four data bits are to be transmitted , he suggested a code word pattern as shown below :



- The D bits in above figure are data bits , where P bits are parity bits. The parity bits P_1,P_2, P_4 and adjusted in a particular was as explained below .

Minimum Number of Parity :

- Below table gives a listing of minimum number of parity bits needed for various range of "m" information bits.

Number of information bits	Number of parity bits
2 to 4	3
5 to 11	4
12 to 26	5
27 to 57	6
58 to 120	7

Deciding the value of parity bits :

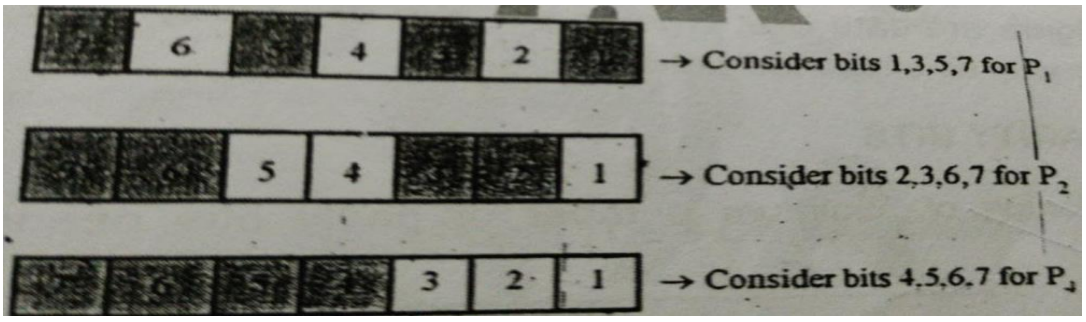
- Below table indicates which bit positions are associated with each parity bit in order to establish required parity (even or odd) over the selected bits positions.

Parity Bit	Bits to be checked
P_1	1,3,5,9,11,13,15….
P_2	2,3,6,7,10,11,14,15…
P_3	4,5,6,7,12,13,14,15….
P_4	8,9,10,11,12,13,14,15…..

Selection of Parity Bits :

Selection of P_1 : P_1 is adjusted to 0 or 1 so as to establish even parity over bits 1,3,5,and 7 i.e. P_1 , D_3 ,D_5,,D_7

Photo : 53



Select of P_2 :P_2 is adjusted to 0 or 1 so as to set even parity over bits 2,3,6,and 7 (P_2,D_3 , D_6, and D_7)

Select P_4 :P_4 is adjusted to 0 or 1 so as to set even parity over bits 4,5,6, and 7 (P_4 ,D_5, D_6 and D_7)

Example : 1

A bit word 1011 is to be transmitted .Construct the even parity seven-bit hamming code for this data.

Example : 2

Encode the data bit 0101 into seven bit even parity hamming code .

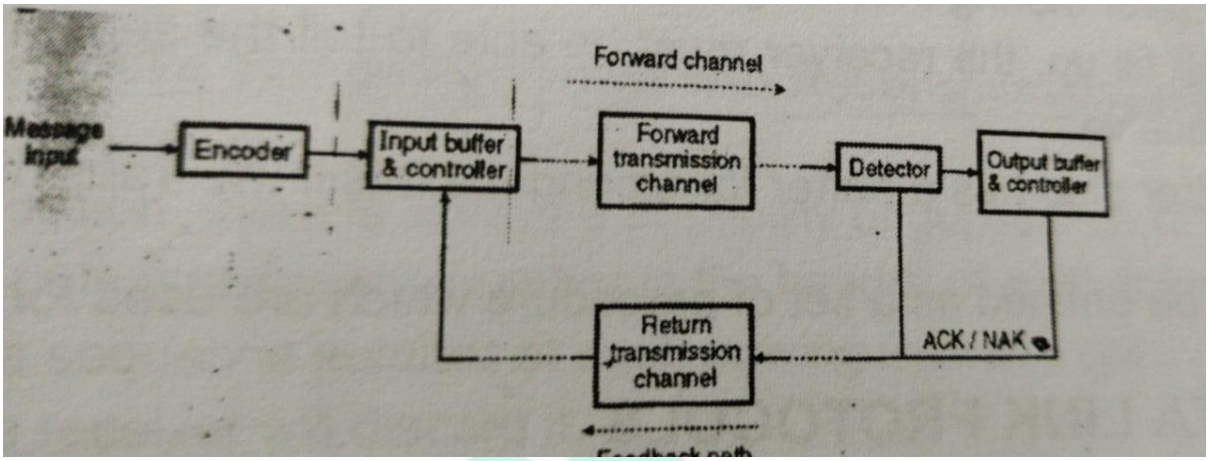
ARQ Technique :

- There are two basic systems of error detection and correction . The first on being the forward error correction(FEC) system and the second one is the automatic repeat request (ARQ) system .
- In the ARQ system of error control , when an error is detected a request is made for the retransmission on that signal. Therefore a feedback channel is required for sending the request for retransmission .
- The ARQ systems different from the FEC systems in three important respects. They are as follows:
  1. In ARQ system less number of check bits(parity bits) are required to be requested to be sent . This will increase the (k/n) ratio for n (n,k) block code if transmitted using the ARQ system
  2. A return transmission path and additional hardware in order to implement repeat transmission of code words will needed .
  3. The bit rate of forward transmission must make allowance for the backward repeat transmission .

Basic ARQ system :

The block diagram of the basic ARQ system as shown below:

Photo -54



peration of ARQ System :

- The encoder procedures code words for each message signal at its input. Each code word at the encoder output is stored temporarily and transmitted over the forward transmission channel .
- At the destination a decoder will decode the code words and look for errors
- The decoder will output a “positive acknowledgement “(ACK) if no errors are detected and it will output a negative acknowledgment (NAK) if errors are detected
- On receiving a negative acknowledgment(NAK) signal via the return transmission path the “controller” will retransmit the appropriate word from the word stored by the input buffer
- A particular word may be retransmitted only once or it may be transmitted twice or more number of times
- The output controller and buffer on the receiver side assemble the output bit stream from the code words accepted by the decoder .

Flow Control :

- This is another important design issue related to the data link layer
- The problem to be handled is what to do with the sender which systematically wants to transmit frames at the faster rate than the capacity of the receiver
- This happen s when the sender is using a faster computer than the receiver . This will completely swamp the receiver
- This receiver will keep losing some of the frames simply because they are arriving too quickly .
- The solution to this problem is to introduce the flow control
- The flow control will control the rate of frames transmission to a value which can be handled by the receiver
- It requires some kind of a feedback mechanism from the receiver to sender
- We are going to discuss some flow control techniques based on this principle
- It is set of procedures that tells the sender how much data it can transmit before it must wait for an acknowledgement from the receiver , otherwise there will be overflow of data .
- The data flow should not be fast that the receiver is over-whelmed
- The speed of processing any receiving device is limited and it also has a limited amount of memory storage space , for storing the incoming data .
- There has to be some system , for reverse communication from the receiver to transmitted. The receiver can tell the transmitter about adjusting the data flow rate to suit is speed or even stop temporarily
- As the rate of processing is generally slower than the rate of transmission , each receiver has block of memory called buffer
- The buffer is reserved for storing incoming data until they are processes
- If the buffer beings to fill up , the receiver must be able to tell the sender to step transmission until it is once again able to receive
- Similarly the transmitter also has a buffer for sorting the bits if the transmission is stopped

Note: Flow control can be defined as a set of procedure which are used for restricting the amount of data

gradeup SUPER

Gradeup UGC NET

Super Superscription

Features:

1. 7+ Structured Courses for UGC NET Exam
2. 200+ Mock Tests for UGC NET & MHSET Exams
3. Separate Batches in Hindi & English
4. Mock Tests are available in Hindi & English
5. Available on Mobile & Desktop

Gradeup Super Subscription, Enroll Now

gradeup.co