WIP - please ignore document

The IObundle Timer core includes a 64-bit counter for returning the time in clock cycles. It is written in Verilog and includes a C software driver. With the knowledge of the clock frequency in its software driver, it is also possible to print the time in microseconds, milliseconds or seconds. The IP is currently supported for use in ASICs and FPGAs.

Features

- Verilog 64-bit time counter in clock cycles.
- C software driver.
- Reset, enable and time read functions.
- IOb-SoC native CPU interface.
- AXI4 Lite CPU interface (premium option).

Benefits

- Compact hardware implementation
- Can fit many instances in low cost FPGAs
- Can fit many instances in small ASICs
- Low power consumption

Deliverables

- Verilog source code
- User documentation for easy system integration
- Example integration in IOb-SoC (premium)
- FPGA synthesis and implementation scripts (premium)
- ASIC synthesis and place and route scripts (premium)

Block Diagram

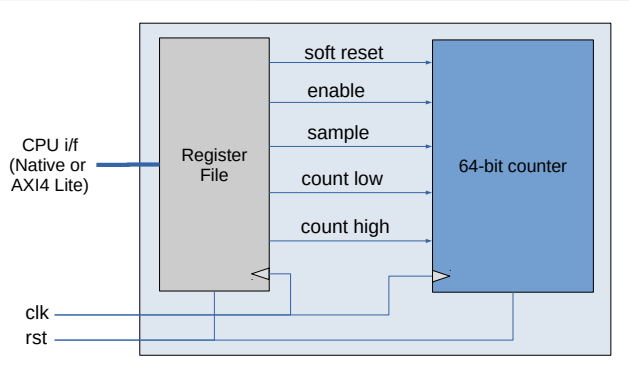

Figure 1: High-level block diagram

FPGA Results

The following are FPGA implementation results for two FPGA device families.

Resource	Used
LUTs	97
Registers	92
DSPs	0
BRAM	0

Resource	Used
ALM	81
FF	101
DSP	0
BRAM blocks	0
BRAM bits	

Table 1: Kintex Ultrascale (left) and Cyclone V GT (right)

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.