Overview

The IOb-SoC is an RISC-V-based System-on-Chip Platform written in Verilog, which users can download for free, modify, simulate and implement in FPGA or ASIC. It supports stand-alone and booting modes, and can use internal RAM or an external DDR controller via L1/L2 cache systems. The IP is currently supported in ASICs and FPGAs. Licensable commercial versions are available.

Features

- 1 32-bit RISC-V control CPU
- Support for Integer (I), atomic (A) and multiply/divide extensions (M)
- Instruction and data caches
- RS232 interfaces for viewing runtime messages
- Optional timer peripheral
- Optional Ethernet peripheral
- Frequency of operation at 167MHz on FPGA
- Needs external DDR4 memory controller IP

Benefits

- Compact hardware implementation
- Can fit in low cost FPGAs
- Can fit in small ASICs
- Very low power consumption

Deliverables

- HDL netlist or source code optionally
- Software object or C++ source code optionally
- Simulation testbench
- Implementation constraints for map, place and route
- Demo files for commercial FPGA board with Ethernet connectivity
- User documentation for system integration

Block Diagram

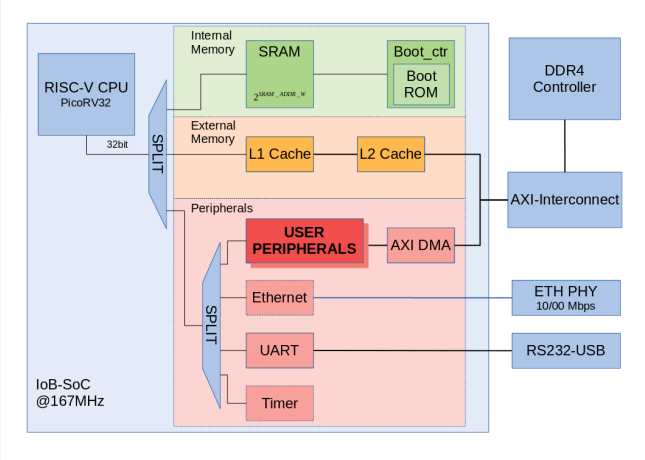

Figure 1: IOb-SoC high-level block diagram

FPGA Resources

Resource	Used
LUTs	1869
Registers	1029
DSPs	4
BRAM	5
PIN	6

Table 1: Implementation Resources for Xilinx Kintex Ultrascale Devices

Resource	Used
ALM	1,335
FF	1177
DSP	3
BRAM blocks	22
BRAM bits	165,888
PIN	6

Table 2: Implementation Resources for Intel Cyclone V Devices

Disclaimer: IObundle reserves the right to modify the current technical specifications without notice.