Overview

IOb-SoC is a RISC-V-based System-on-Chip Platform written in Verilog, which users can download for free, modify, simulate and implement in FPGA or ASIC. It supports stand-alone and boot loading modes, and can use an internal RAM or an external DDR controller via an L1/L2 cache system. The IP is currently supported in ASICs and FPGAs. Licensable commercial versions are available.

Features

- 32-bit RISC-V control CPU
- Support for Integer (I), atomic (A) and multiply/divide extensions (M)
- Instruction and data caches
- RS232 interfaces for viewing runtime messages
- Optional timer peripheral
- Optional Ethernet peripheral
- Frequency of operation at 167MHz on FPGA
- Needs external DDR4 memory controller IP

Benefits

- Compact and easy to integrate hardware and software implementation
- Can fit many instances in low cost FPGAs and ASICs
- Low power consumption

Deliverables

- ASIC or FPGA synthesized netlist or Verilog source code, and respective synthesis and implementation scripts
- ASIC or FPGA verification environment by simulation and emulation
- Bare-metal software driver and example user software
- User documentation for easy system integration
- Example integration in IOb-SoC (optional)

Block Diagram

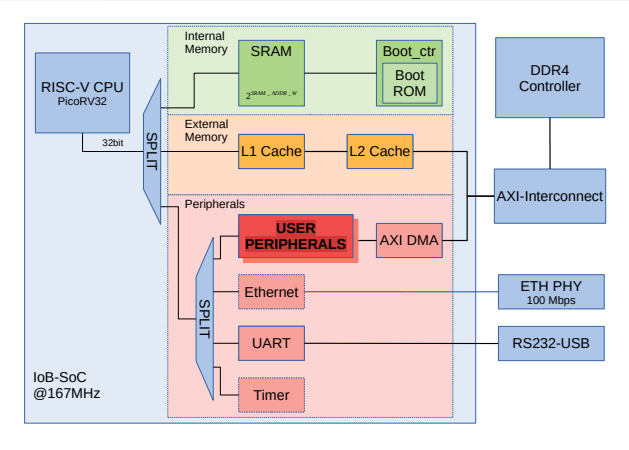

Figure 1: High-Level Block Diagram.

Implementation Results

The following are FPGA implementation results for two FPGA families. The results have been obtained using all the default user configurable parameters, which affect the RAM usage results.

Resource	Used
LUTs	2072
Registers	1074
DSPs	4
BRAM	9

Resource	Used
ALM	1,542
FF	1214
DSP	3
BRAM blocks	38
BRAM bits	296,960

Table 1: FPGA results for Kintex Ultrascale (left) and Cyclone V GT (right).