EC551 Project: Microfluidic Flow Control

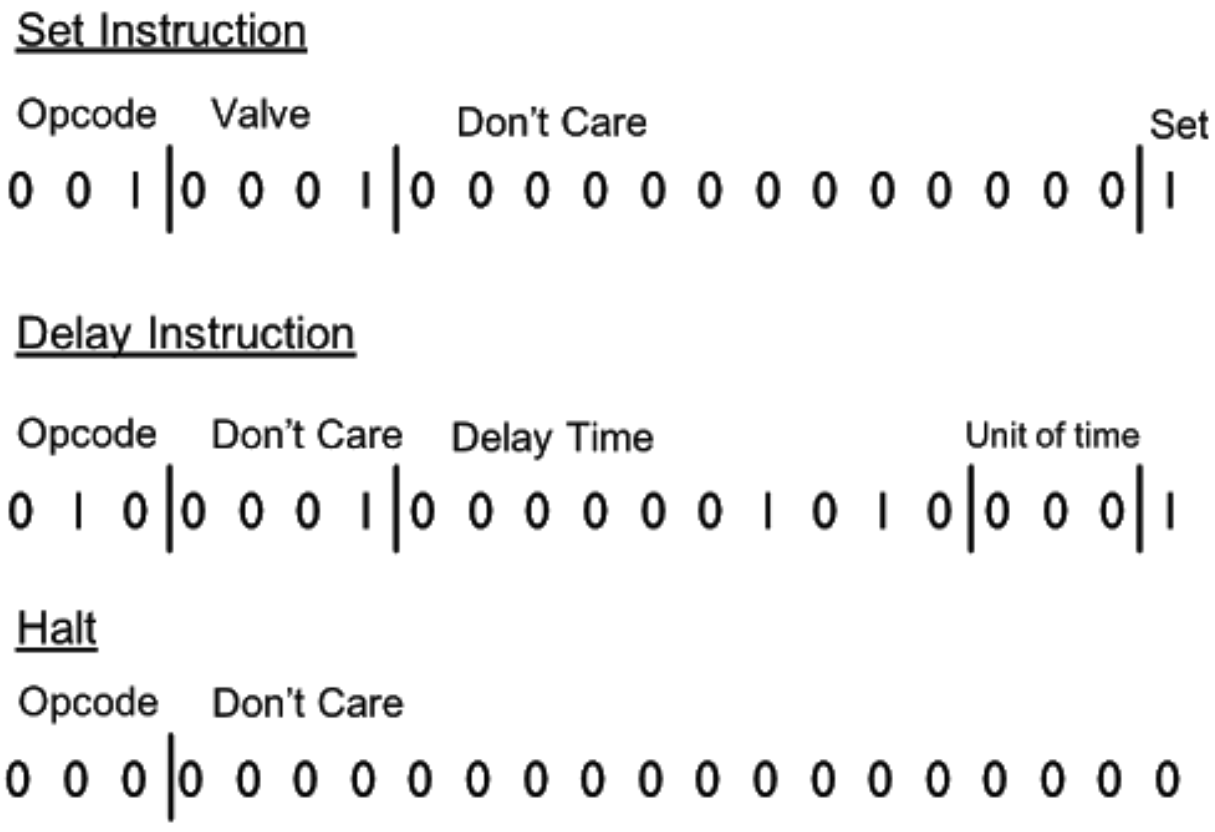
1. Instructions for replicating:

1. Download or Clone the repo.
2. In your Vivado project, add the (.v) files from **Source_codes** folder as Verilog sources.
3. Then add (.v) files from the **TestBenches** folder as Verilog Simulation sources.
4. Now, for simulation set **Top_mod.v** and **top_mod_test.v** as your top module.

For Synthesis and Implementation:

1. Add the constraints file **ec551proj.xdc** from the **Constraints** folder to your project.
2. Run synthesis and Implementation.
3. Generate bitstream and burn the code onto your FPGA.

2. Instruction format for the processor:



Unit of time: 001 – milliseconds (ms)
010 – seconds (secs)
011 – minutes (mins)
100 – hours (hrs)
101 – days