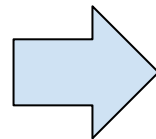
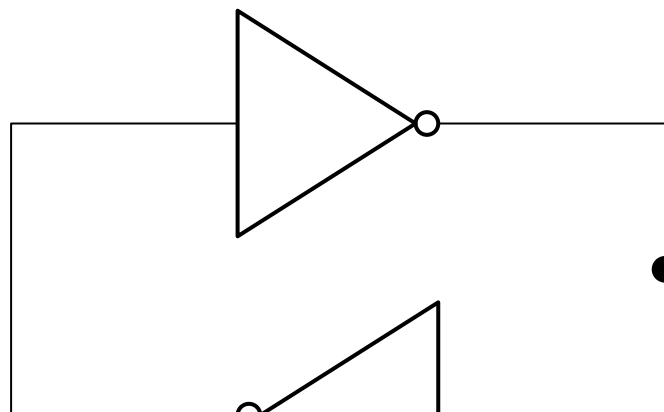
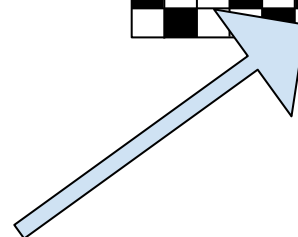
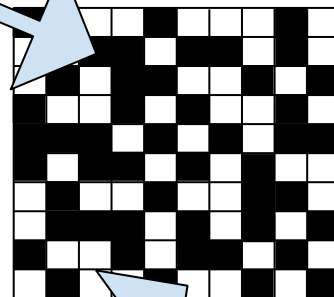


SRAM Cell



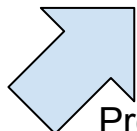
1

SRAM array (r)



0

Power up (c)



Process
variation

