

# Electrochemical water quality monitoring

## Design Review

USA 5



THE UNIVERSITY OF  
**TENNESSEE**  
KNOXVILLE



# Project Motivation

- A global social problem directly affecting health outcomes
- Effect of heavy metals and pharmaceutical contamination
- Electrochemical measurements are routinely used to quantify and identify various chemical particles using benchtop instruments in the lab
- Primary tasks are to design the potentiostat and the wireless transceiver, and to successfully fabricate our chip

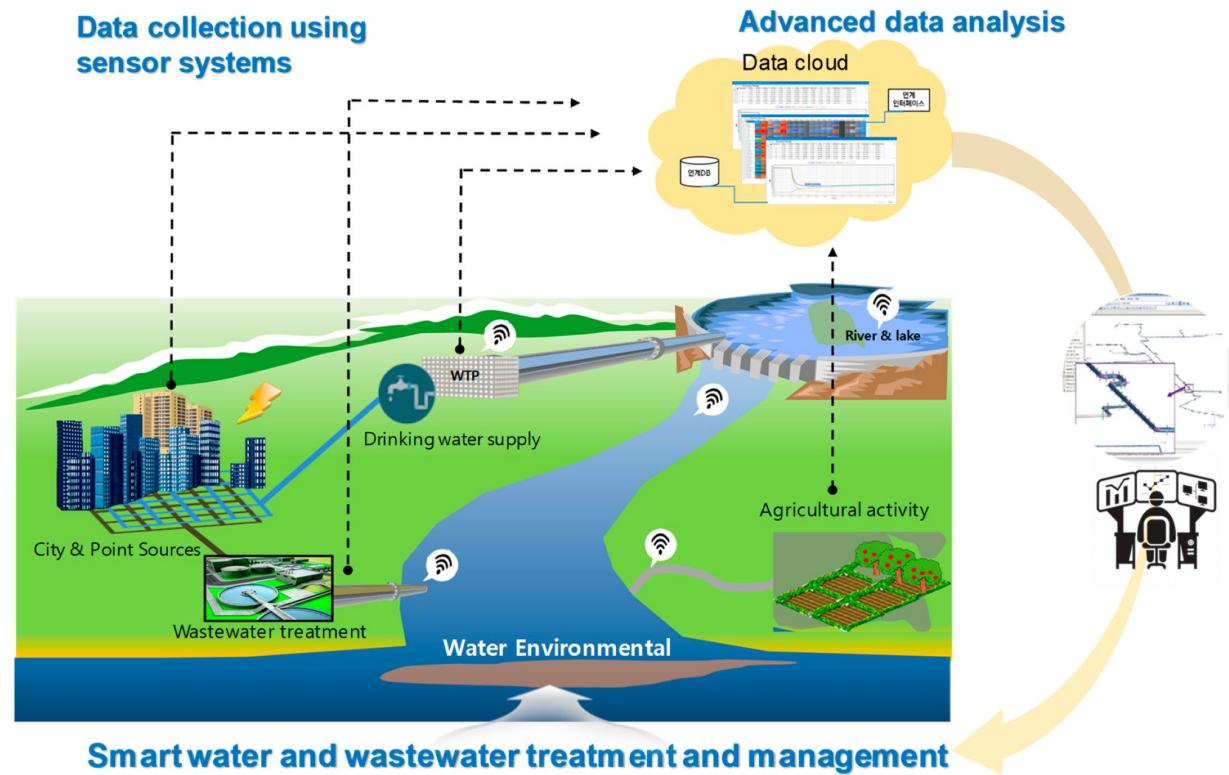


Figure 1: A typical water management system with real-time monitoring, transmission, and advanced data management system

Image source: J. Park et al. "Recent Advances in Information and Communications Technology (ICT) and Sensor Technology for Monitoring Water Quality" <https://doi.org/10.3390/w12020510>

# Design overview

- Design and fabricate a low power, low cost potentiostat electrochemical sensing system
- A three-electrode electrochemical sensor will perform amperometry and cyclic voltammetry and send the captured signal into the analog front-end module.
- The analog signal will be amplified, digitized, and transmitted wirelessly off chip using a transceiver
- On-chip processing will provide calibration and control with the help of an open source RISC-V processor

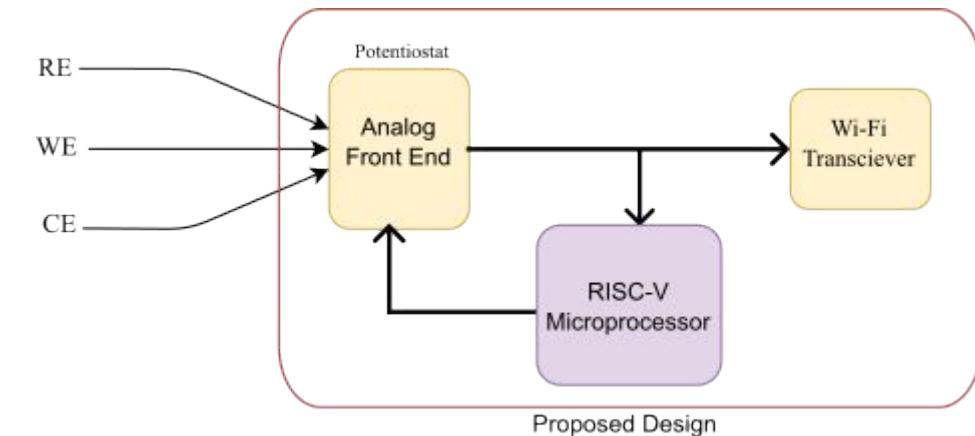
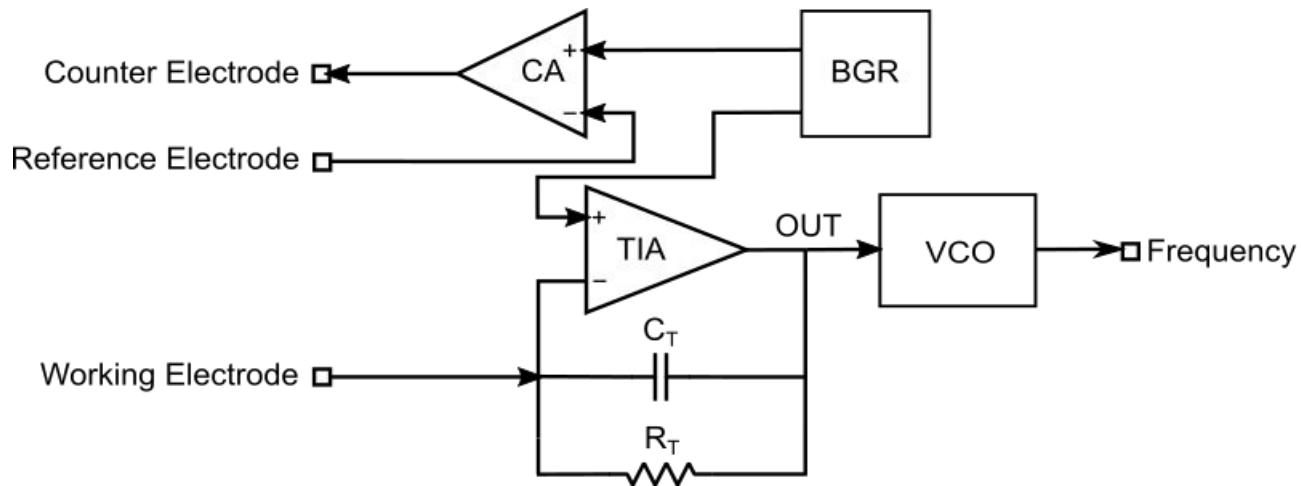


Figure 2: Block diagram of the proposed system

# Analog Front-End: Block Diagram

- The analog front-end consists of two amplifiers (CA and TIA), a voltage-controlled oscillator (VCO), and a band-gap reference (BGR) circuits
- The CA provides the bias voltage for the EC-cell through the Counter electrode
- The TIA converts the cell current from the working electrode into an output voltage
- The VCO converts the analog output into a quasi-digital rail-to-rail pulse with variable frequency, which is then fed to the wireless transceiver and the microprocessor

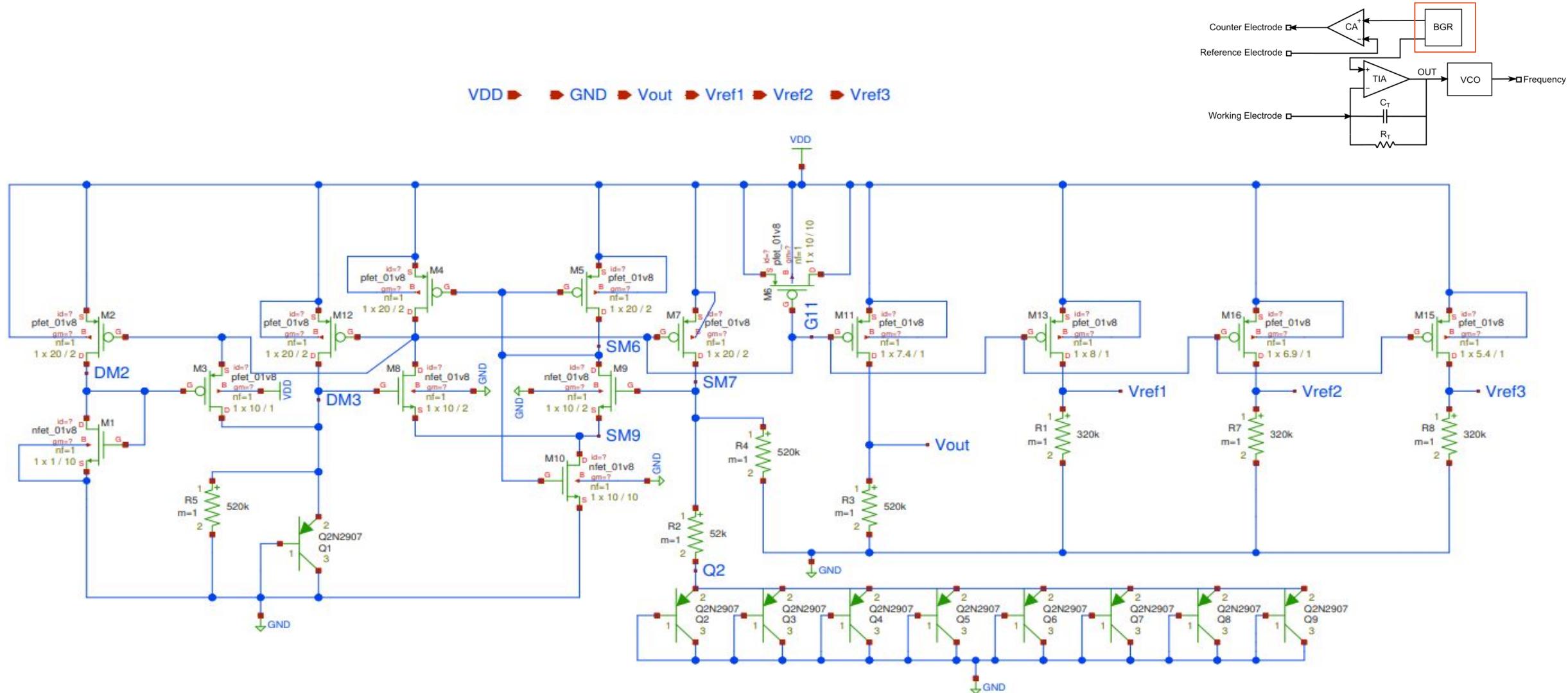


# Analog Front-End: Bandgap Reference (BGR)

- The Voltage Reference was designed to be a Bandgap Reference (BGR) so temperature would not affect the voltage reference points
- The BJT Q1 and Q2 are acting as diodes and together with the resistor (R3) form PTAT current generator
- Eight BJTs were added in series with Q2 because to obtain the correct  $V_{out}$ , you have to choose N, L, and K parameters. For the values you have, K is 8. So you should have 8 of those BJTs in parallel for Q2.
- A self-biased amplifier was used to hold the voltage across BJT (Q1) to the same voltage as across the 25k resistor(R2) and BJT (Q2)
- To form a CTAT current sum with the PTAT current, a resistor (R4) was added
- As temperature increases, the voltage decreases, which causes the current to through R4 to decrease the CTAT
- Current mirrors were used in the last stage of the BGR to get several more voltages that would not be affected by temperature
- The resistor values were adjusted so specific voltages would be produced on each of the voltage reference points
- This circuit will provide specific DC voltages to the Bias Control Amplifier (CA) and the Transimpedance Amplifier (TIA)

Reference: CMOS Circuit Design, Layout, and Simulation Fourth Edition by R Jacob Baker

# Analog Front-End: Bandgap Reference (BGR)



# Analog Front-End: Bandgap Reference (BGR)

DC Analysis Data:

Outputs:

Net1=Vout  
Net2=Vref1  
Net3=Vref2  
Net4=Vref3

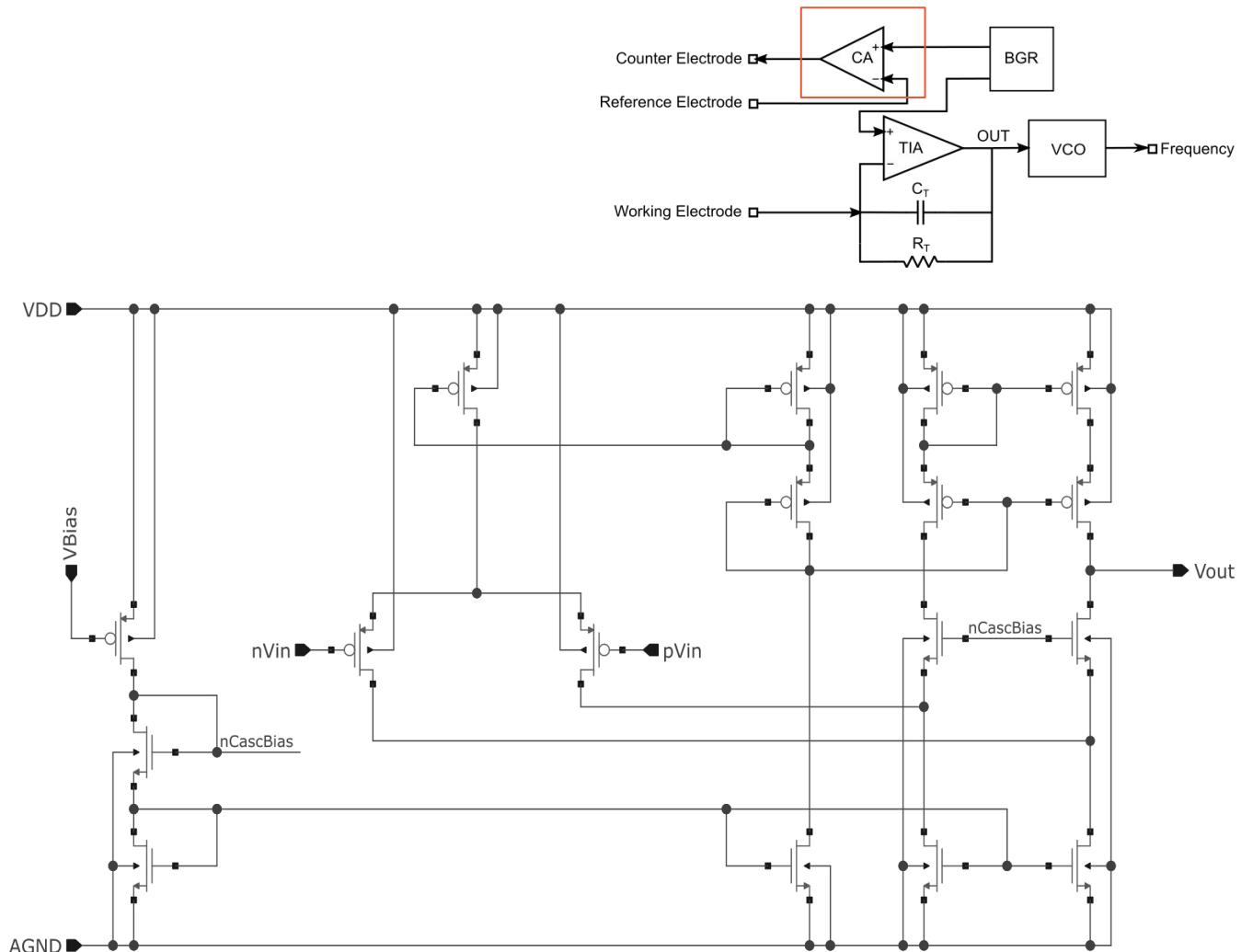
Node	Voltage
-----	-----
vdd	1.8
x1.dm2	1.00377
x1.g11	0.724891
x1.dm3	0.596028
x1.sm9	0.0375586
x1.sm6	0.767962
x1.sm7	0.595758
x1.q2	0.542256
net1	1.20082
net2	0.804097
net4	0.608407
net3	0.70897
v1#branch	-1.7588e-05

BTJ model:

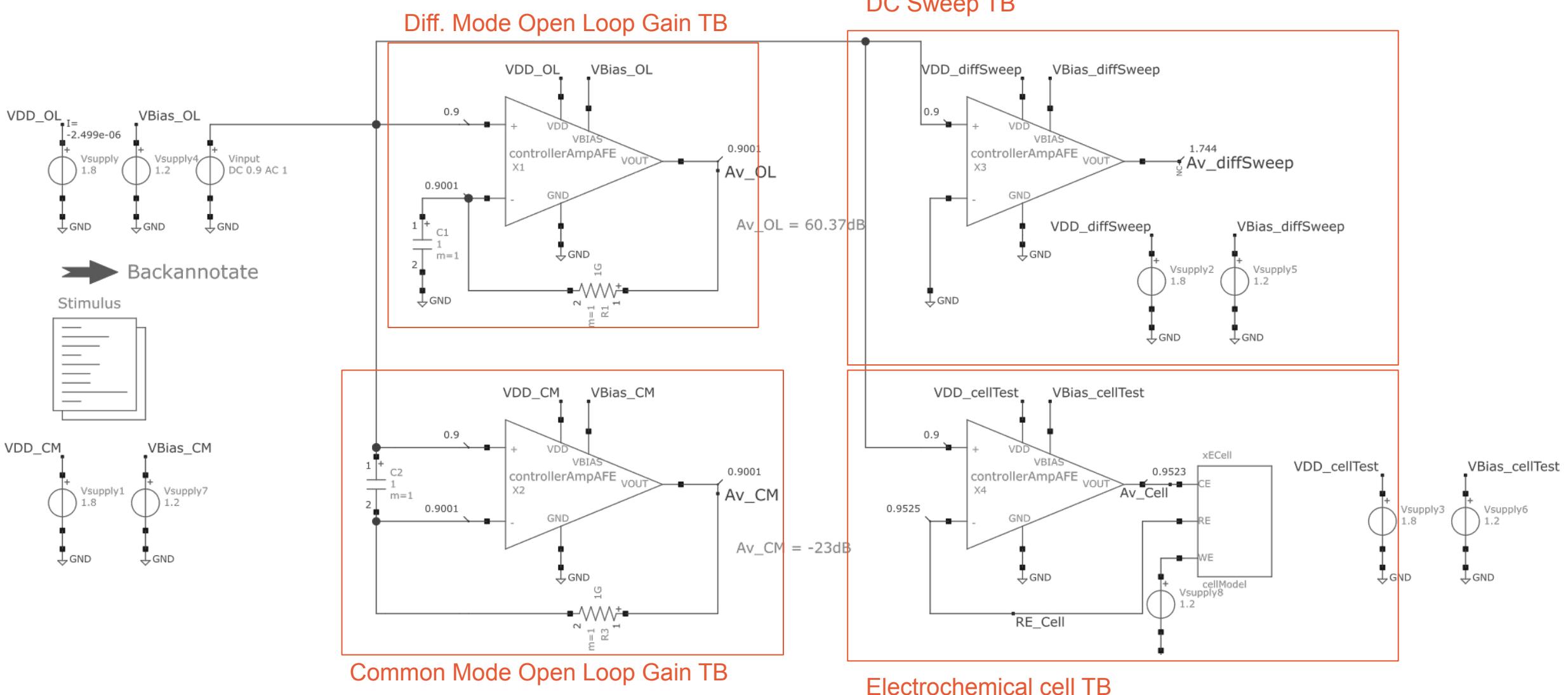
.model Q2N2907  
PNP(IS=1E-14 VAF=120 BF=250 IKF=0.3 XTB=1.5  
BR=3 CJC=8E-12 CJE=30E-12 TR=100E-9  
TF=400E-12 ITF=1 VTF=2 XTF=3 RB=10  
RC=.3 RE=.2 Vceo=40 Icrating=600m mfg=Philips)

# Analog Front-End: Bias Control Amplifier (CA)

- Regulates reference electrode potential
  - Must regulate 0.2V-1.2V
  - Used to sweep the voltage between WE and RE during amperometry and cyclic voltammetry
- PMOS input, folded cascode amp
  - Wide input common mode range
  - High differential gain (60.34dB)
  - Low common-mode gain (-18.51dB)
  - Self-compensating (cap. load)
  - DC Negative Feedback results
    - $-3\text{dB}_{OL} = 155\text{kHz}$
    - Unity Gain @ 80.9MHz
    - PM = 47.9°
  - Low input-referred offset voltage
    - < 100uV structural w/ output at midrail
  - Low power (4.5uW)
    - $V_{DD} = 1.8\text{V}$
    - $I_Q = 2.5\mu\text{A}$
  - Requires only one bias voltage

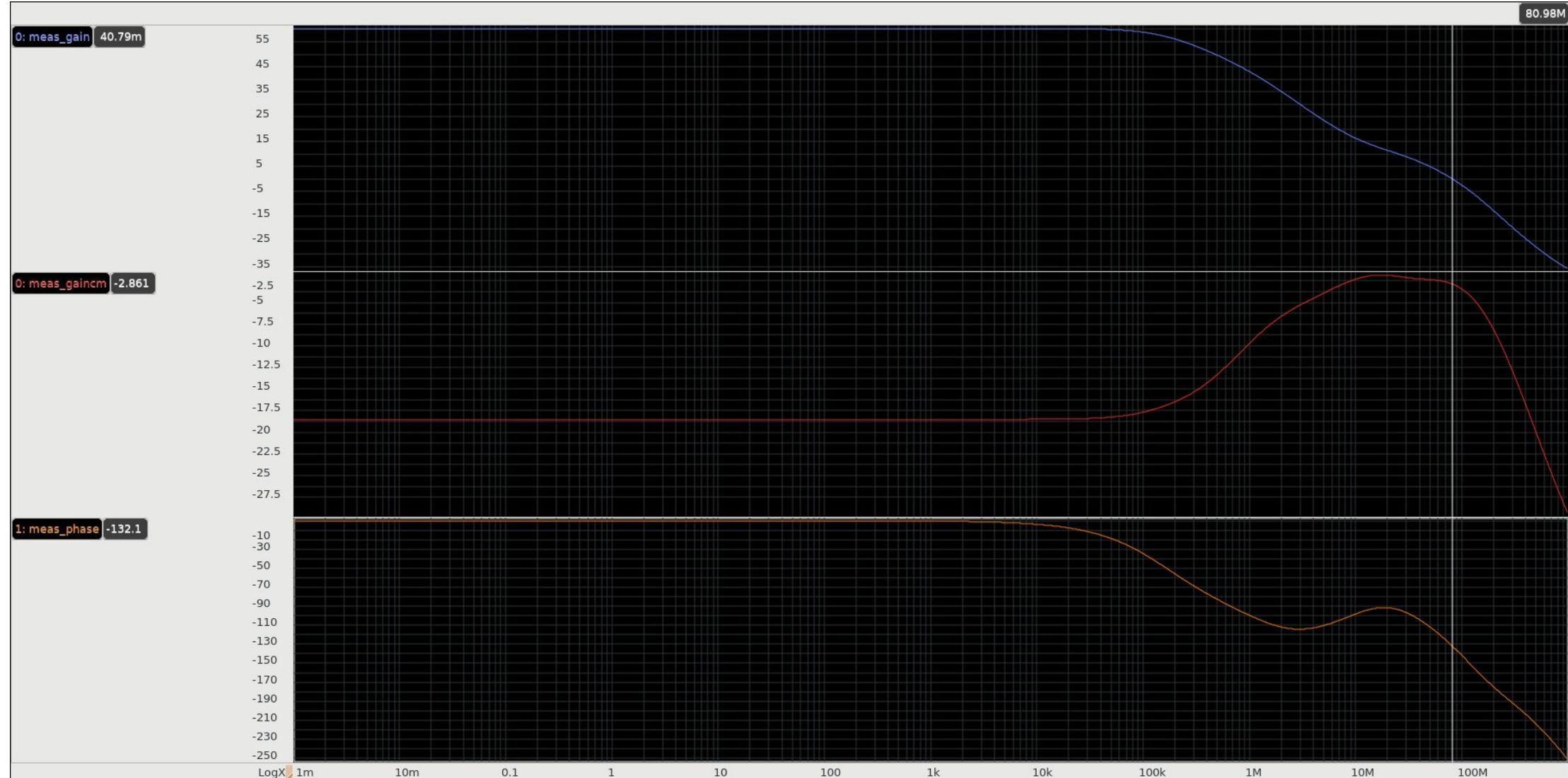


# Analog Front-End: Bias Control Amp. (Testbench)



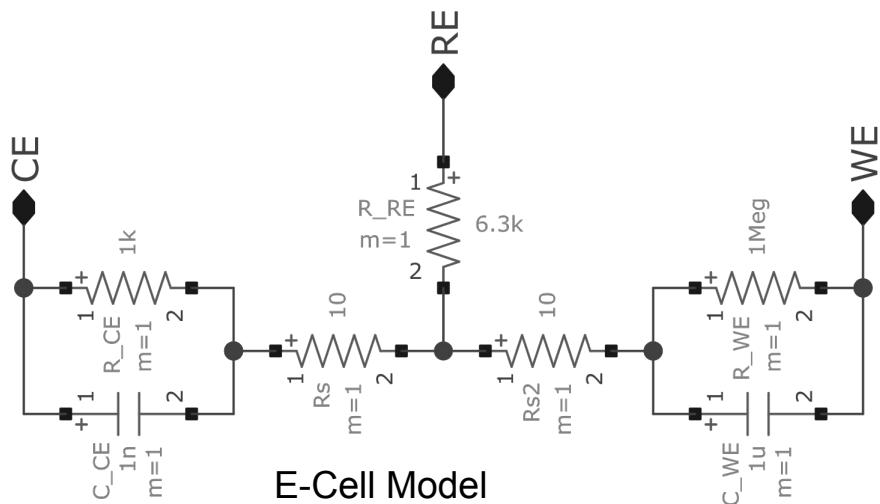
# Analog Front-End: Bias Control Amp. (Open Loop Response)

(Gain in dB and Phase in Degrees)

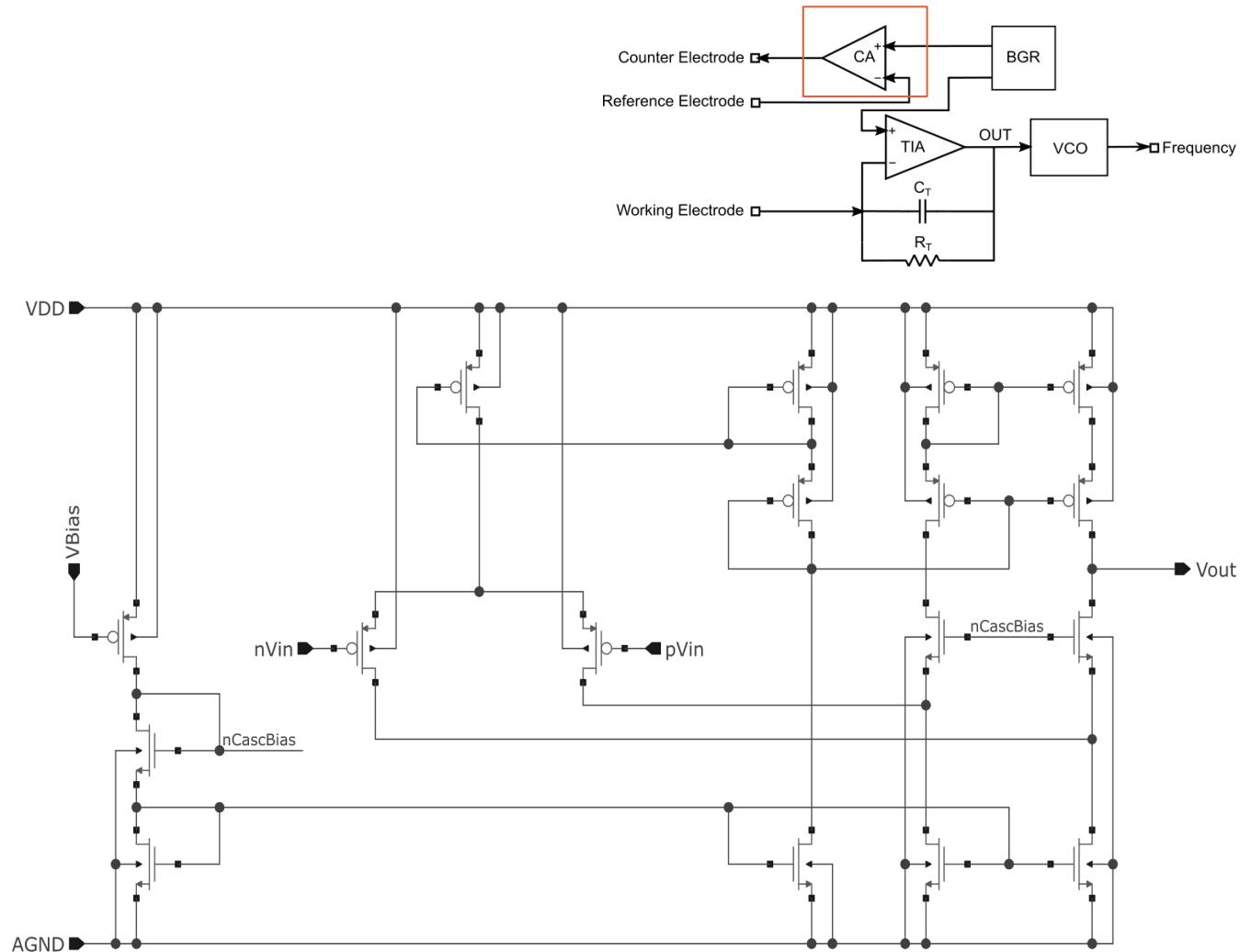


# Analog Front-End: Bias Control Amplifier (CA)

- Next steps:
  - Electrochemical cell presents resistive load of about 1MΩ
    - An output stage capable of driving the resistive load must be added
    - Design is underway



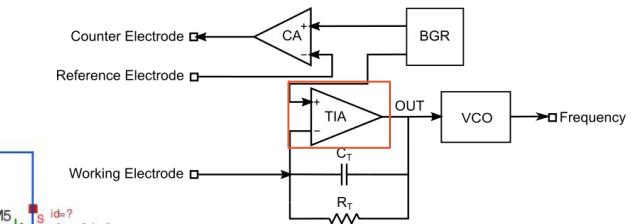
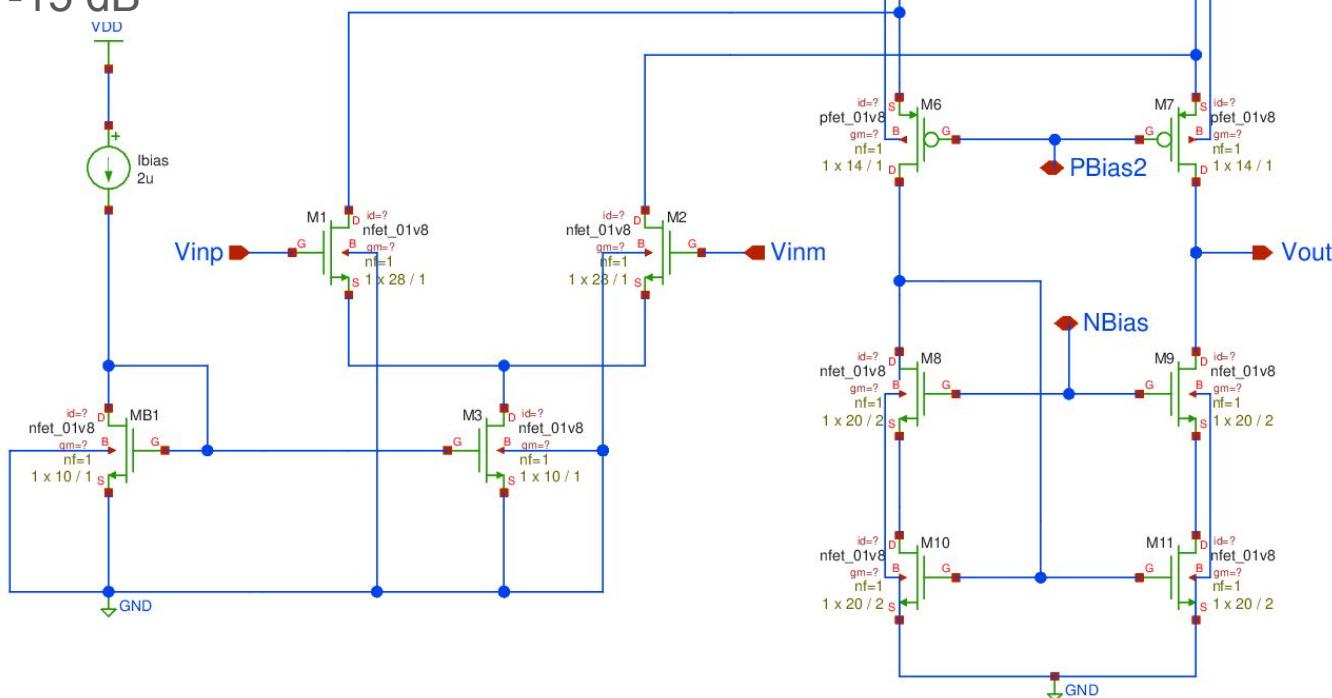
E-Cell Model



# Analog Front-End: Transimpedance Amplifier (TIA)

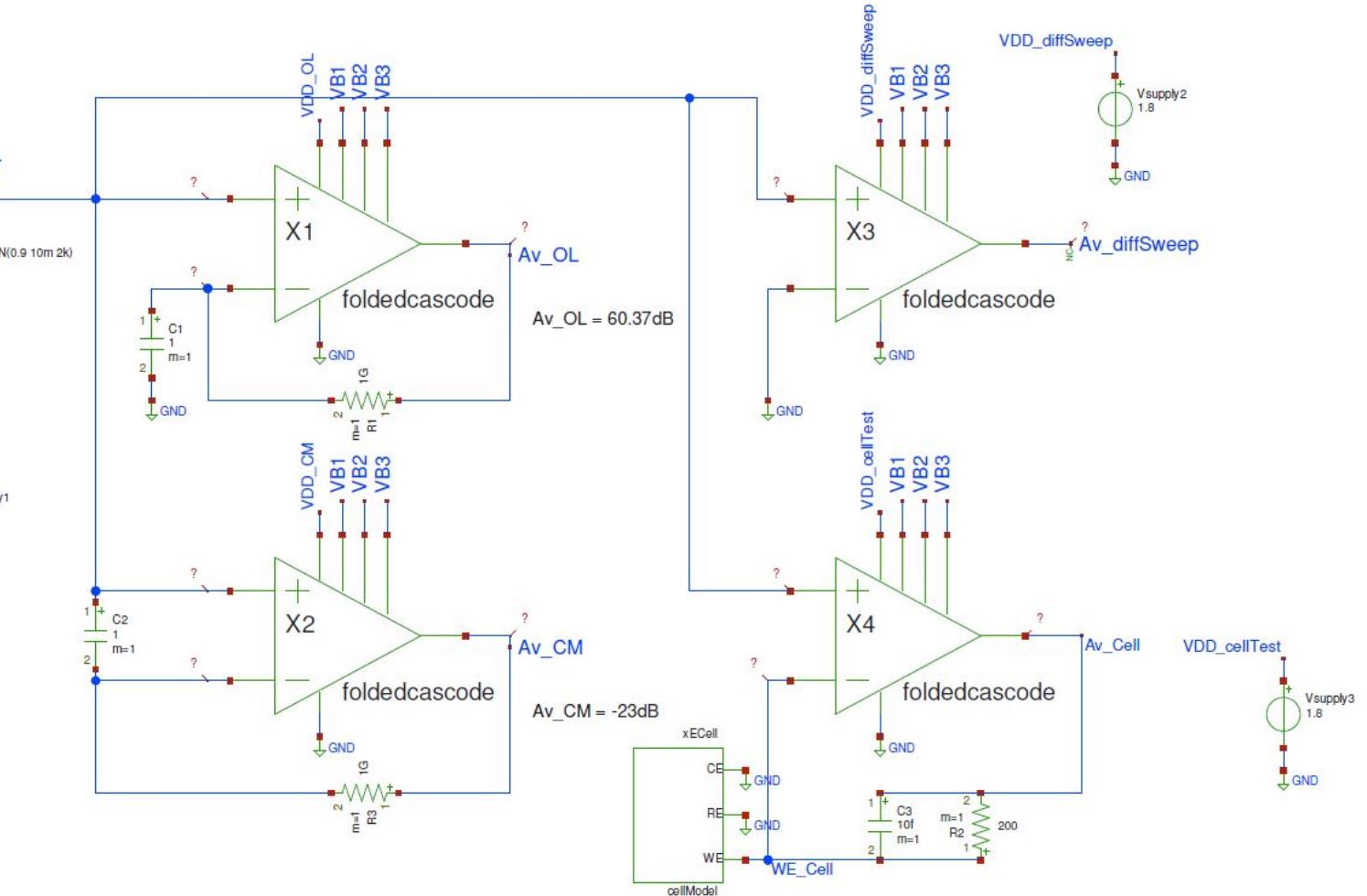
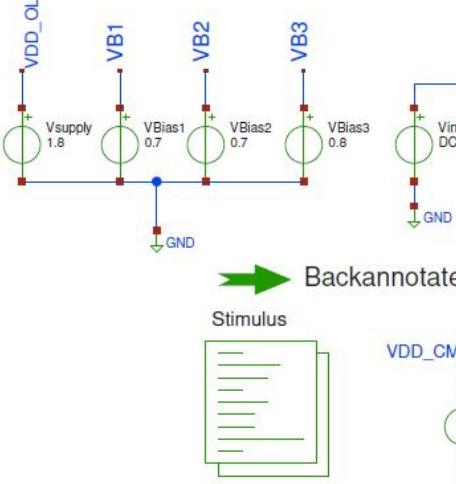
## Design Specifications

- Requires two DC bias voltages: 0.7 V and 0.8 V
- Ibias:  $2 \mu\text{A}$
- Differential gain: 65 dB
- Bandwidth: 30 KHz
- Common-mode gain: -15 dB
- CMRR: 78 dB
- Power:  $3.6 \mu\text{W}$



# Analog Front-End: Transimpedance Amplifier (TIA)

## Testbenches

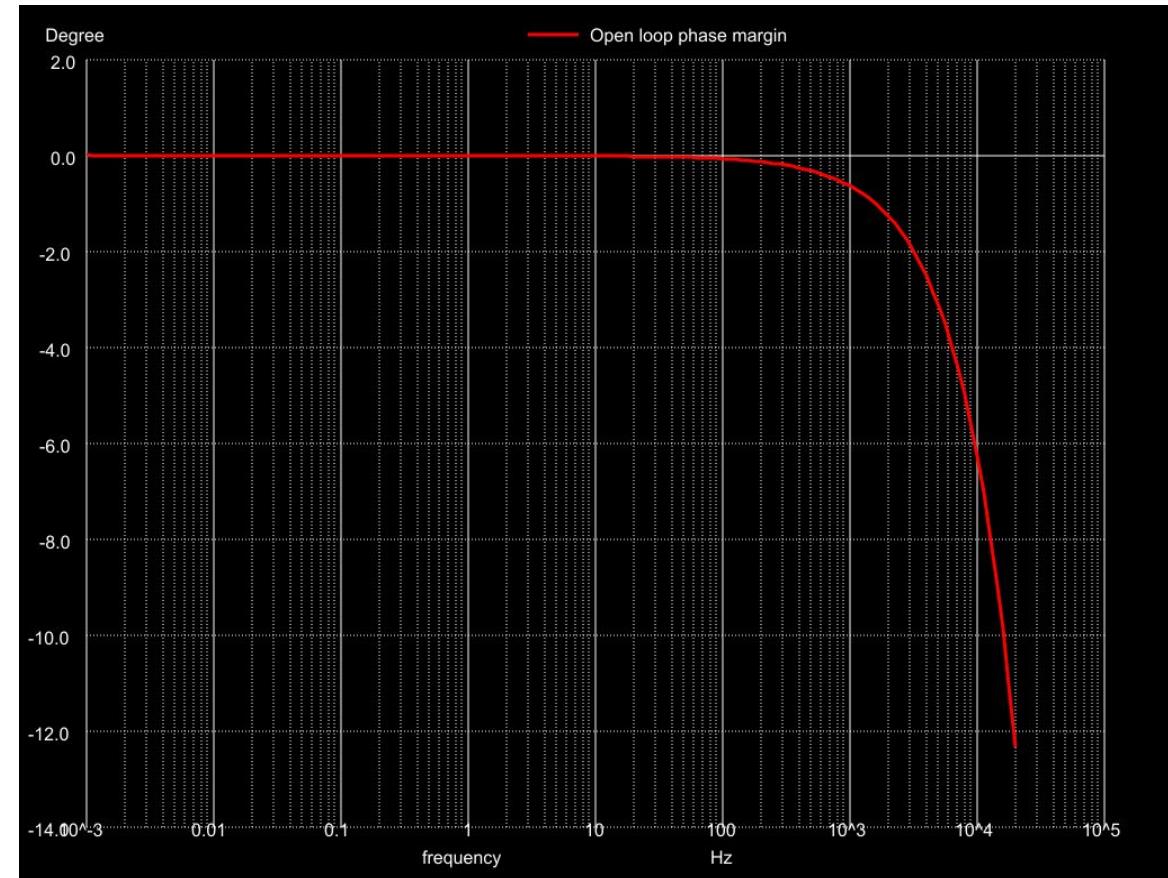
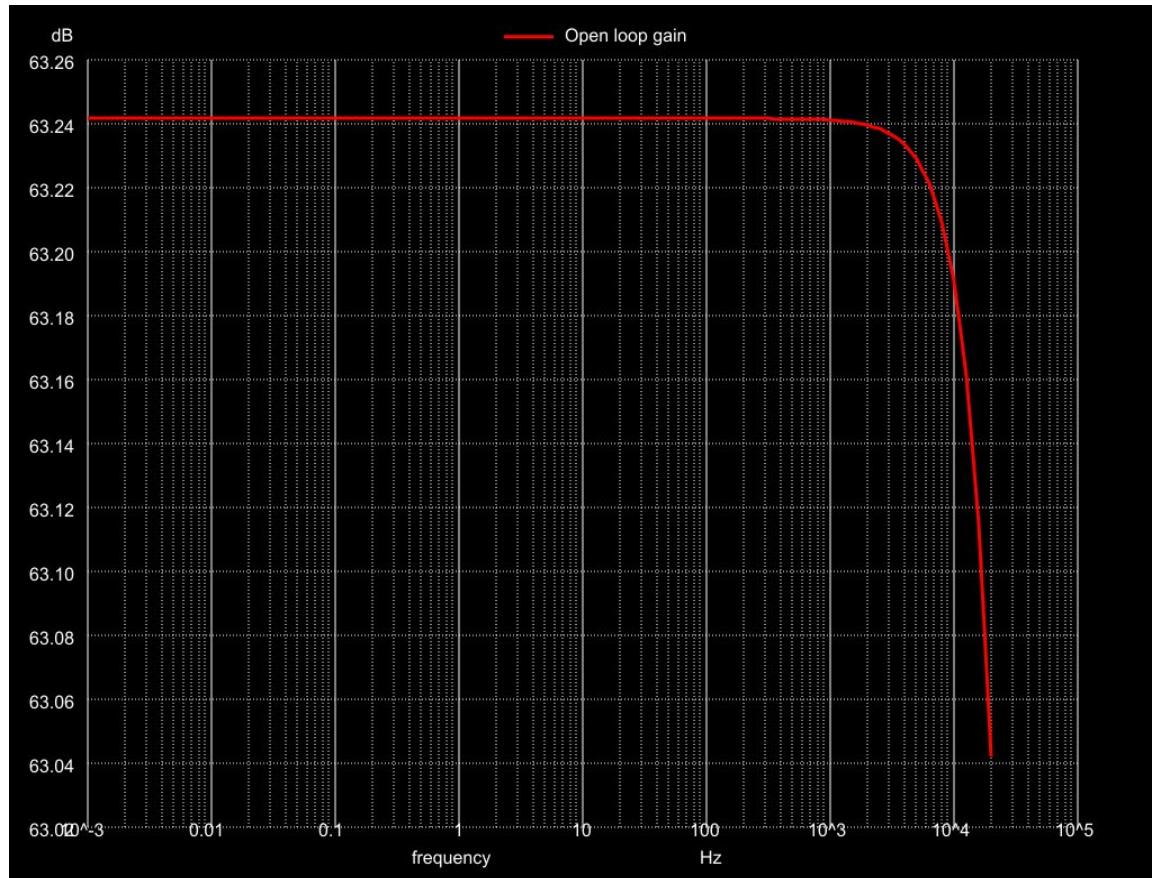


## Next steps:

- Test with the Electrochemical cell model: (ongoing)

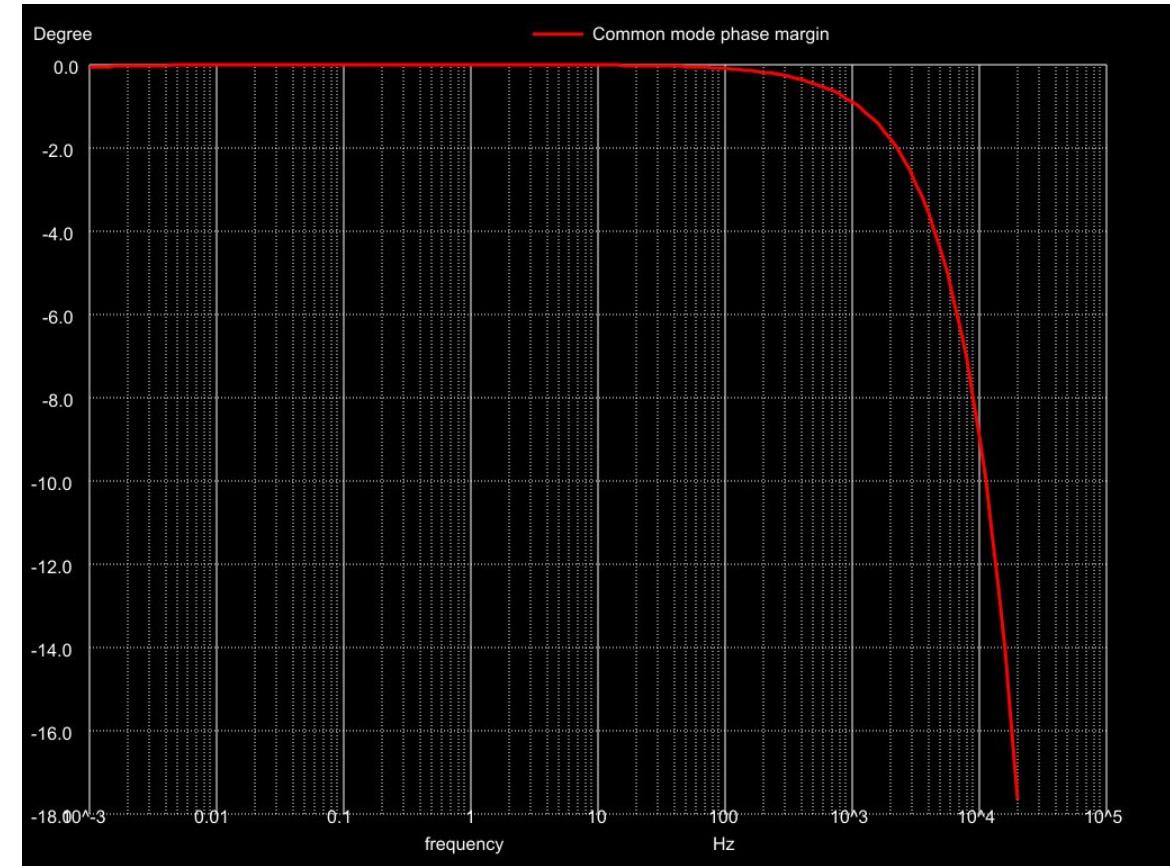
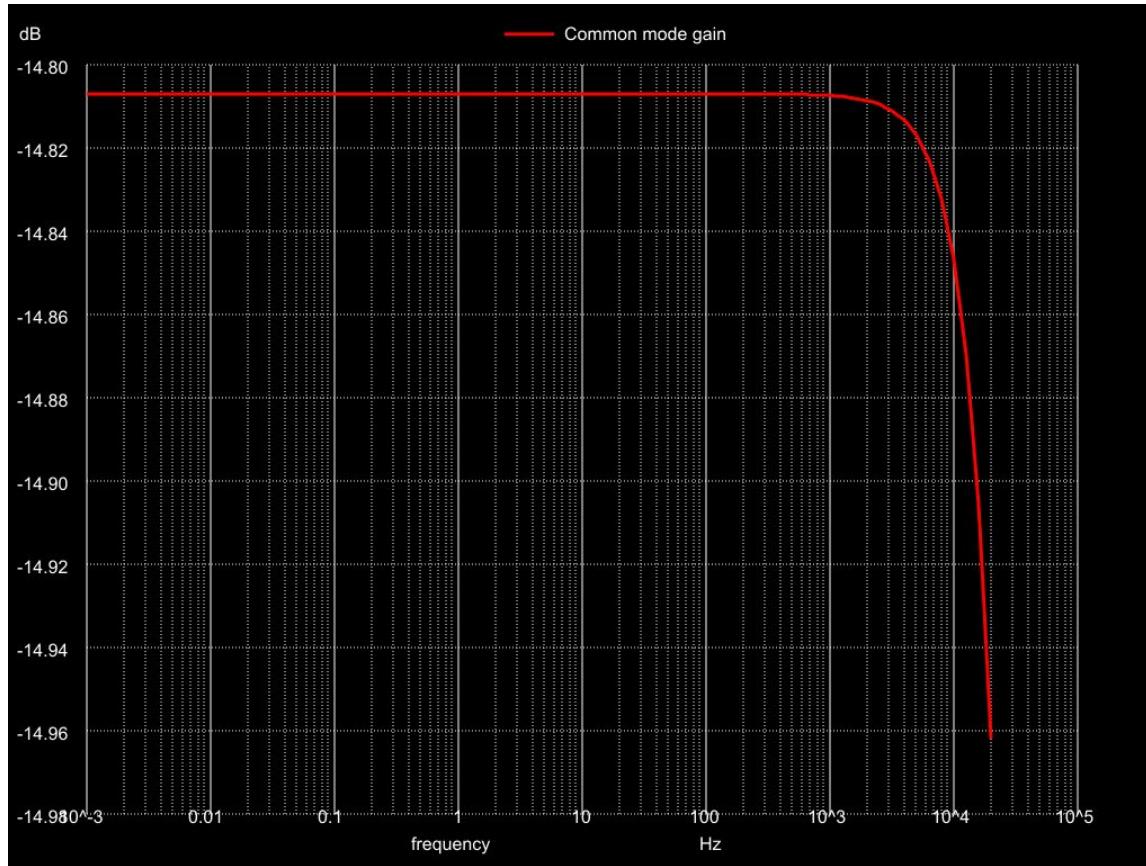
# Analog Front-End: Transimpedance Amplifier (TIA)

Open-loop gain and phase margin



# Analog Front-End: Transimpedance Amplifier (TIA)

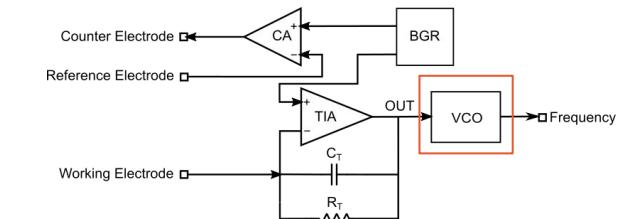
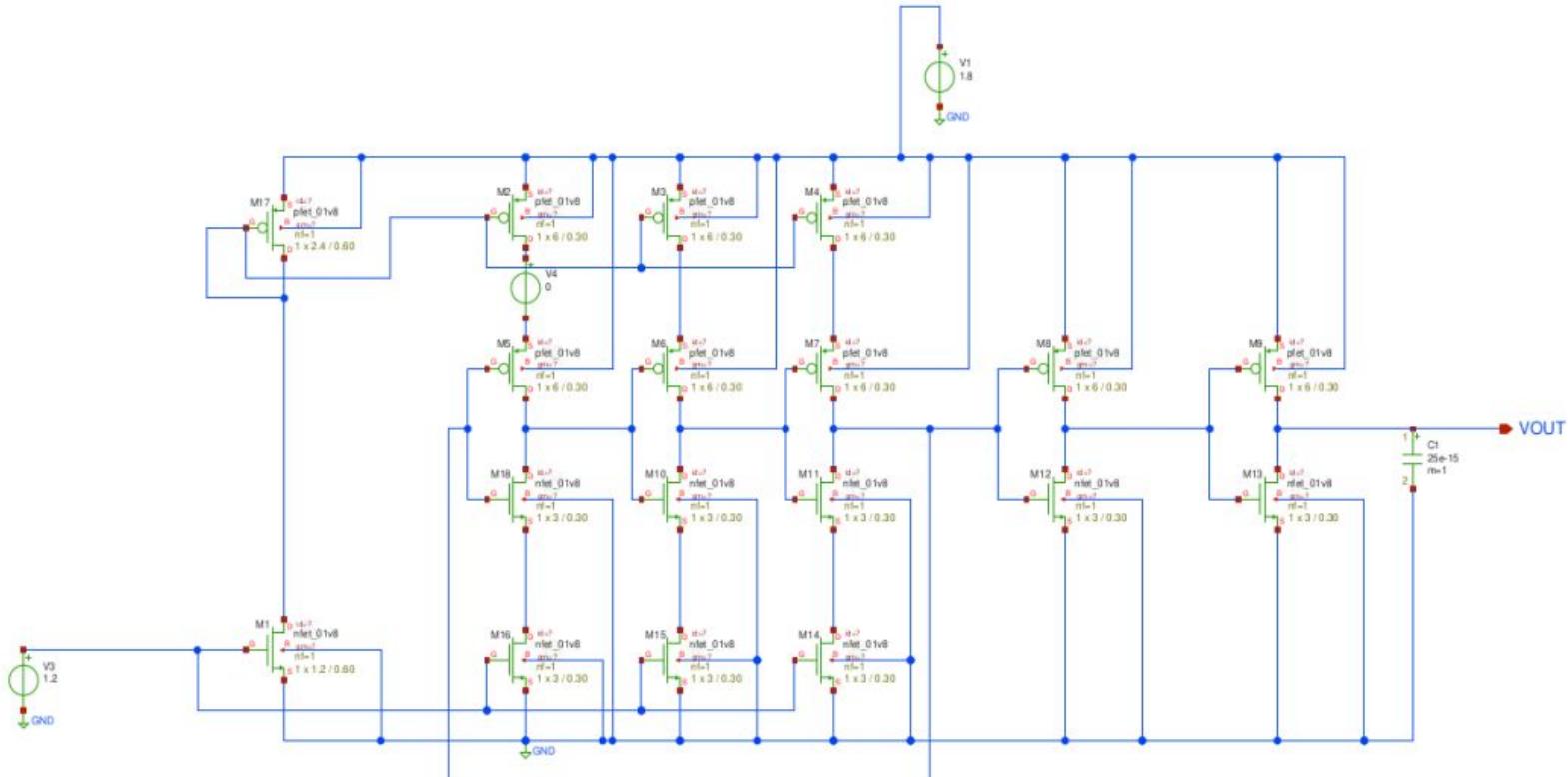
## Common-mode gain and phase margin



# Analog Front-End: Voltage-Controlled Oscillator (VCO)

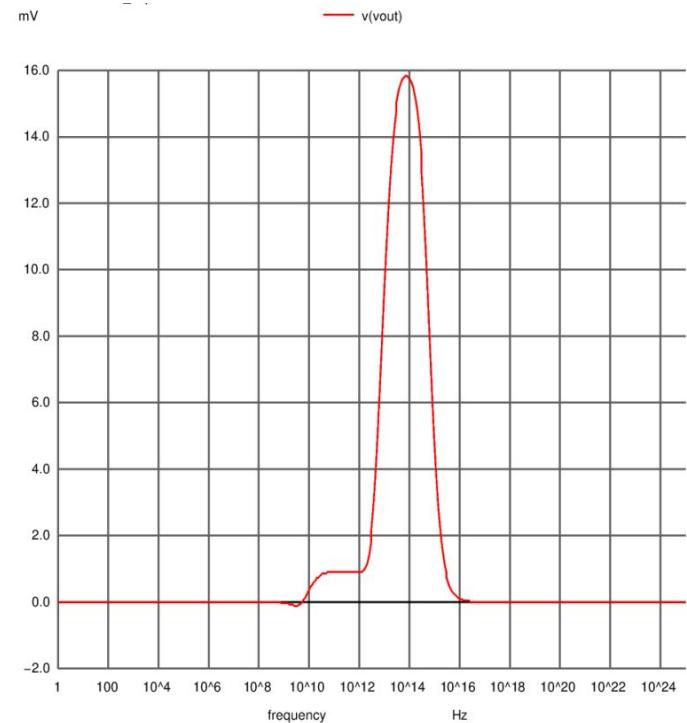
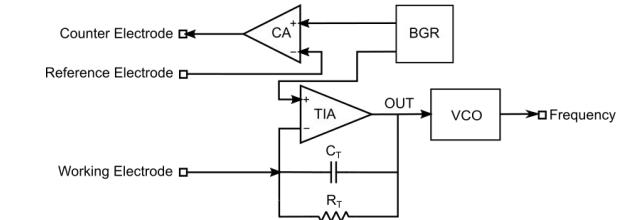
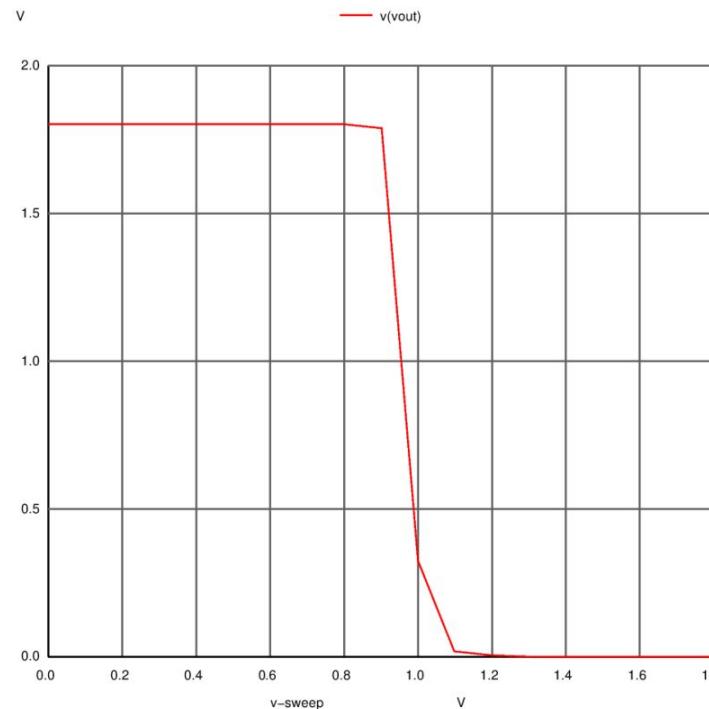
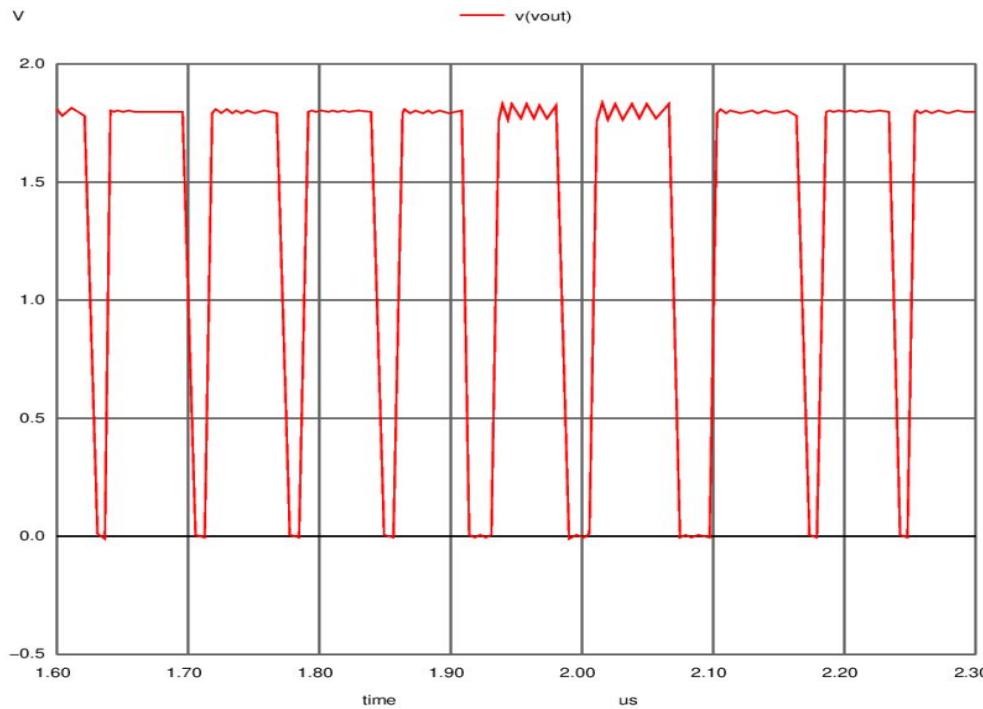
## Design Specifications

- Current starved VCO topology with 3 inverter stage and a buffer connected at the output
- One input control voltage:  $V_{ctrlN} = 0.9V$  (can be varied from 0V to 1.8V to get different oscillating frequency)
- Supply voltage,  $VDD = 1.8V$
- Optimum output Oscillation frequency,  $Fosc = 416.67MHz$
- DC Operating point= 0.9V
- Operating range of frequency= 14.29MHz - 909.1MHz
- Load capacitance,  $C1= 25fF$



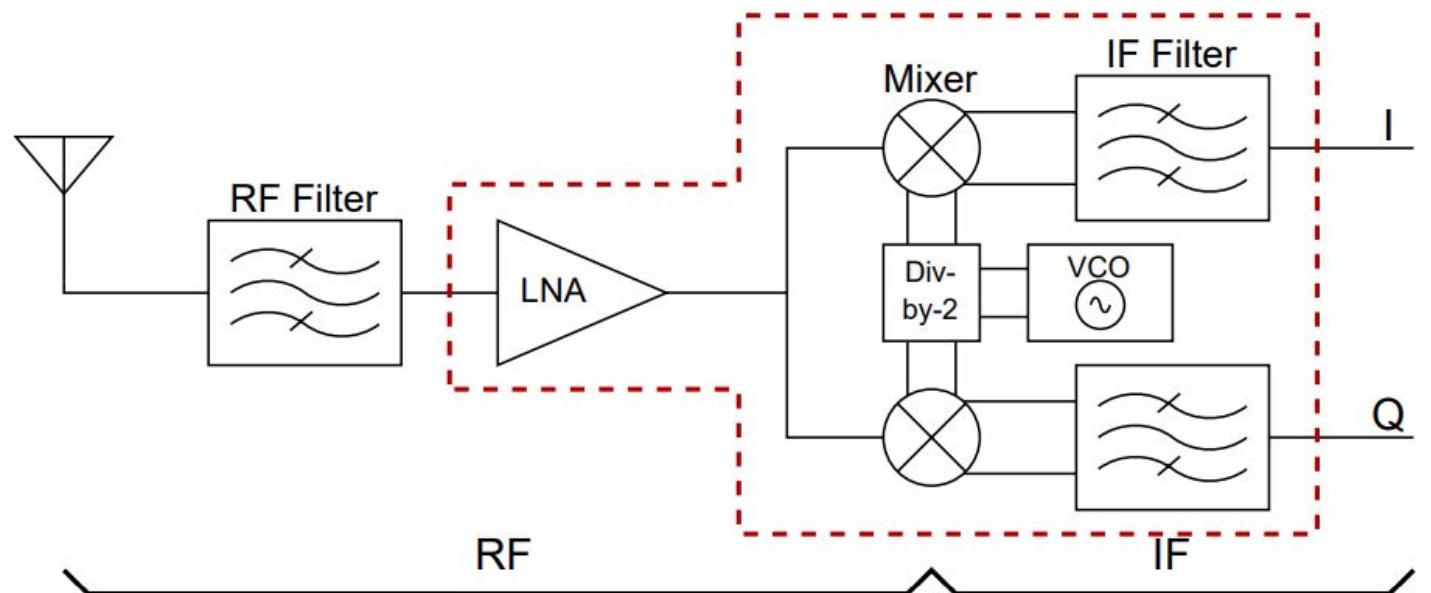
# Analog Front-End: Voltage-Controlled Oscillator (VCO)

Transient analysis, DC operating point and AC analysis plot



# Wireless Transceiver: Block Diagram

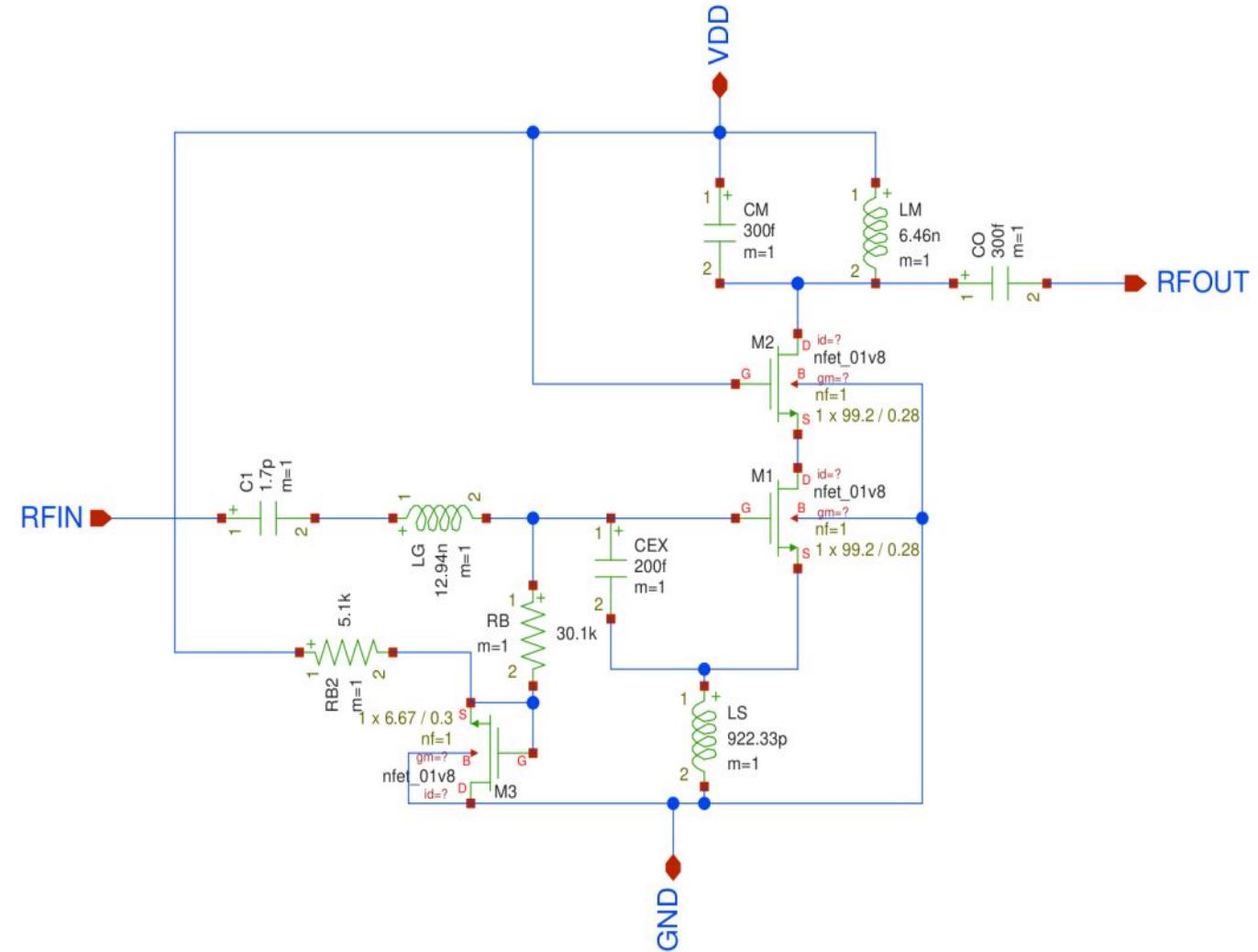
- Wireless transceiver module consists of Low Noise Amplifier (LNA), Power Amplifier, Mixer, Divide by 2, Voltage Controlled Oscillator (VCO) and Intermediate Frequency (IF) Filter.
- The VCO output from AFE passes through the receiver LNA that amplifies the signal to 2.4GHz.



# Wireless Transceiver: Low Noise Amplifier (LNA)

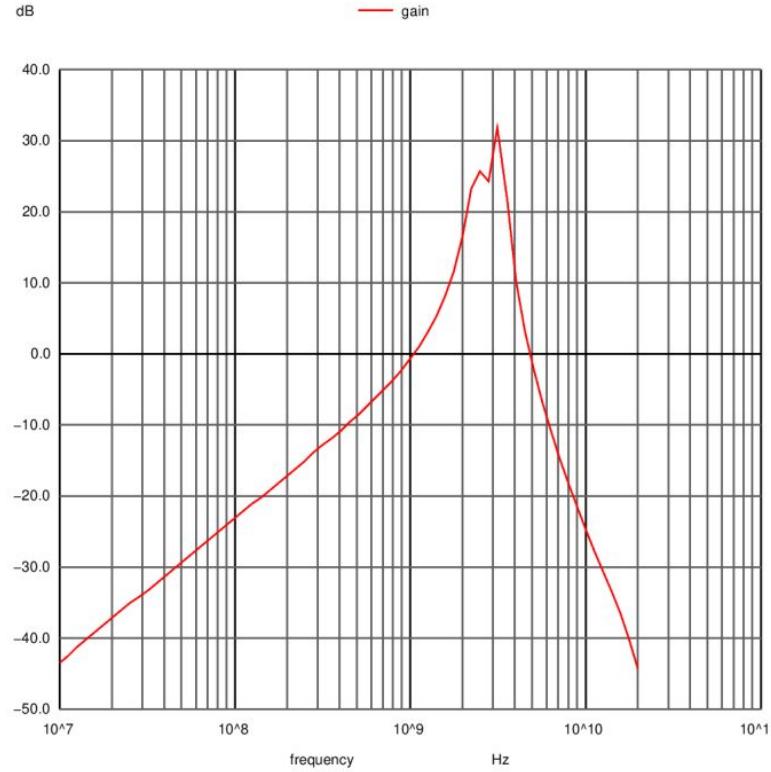
## Design Specification

- Common-source configuration with inductive degeneration
- At 2.4GHz,
- Input reflection ( $S_{11}$ ): -10dB
- Gain ( $S_{21}$ ): 25dB
- Noise Factor (NF): 8dB

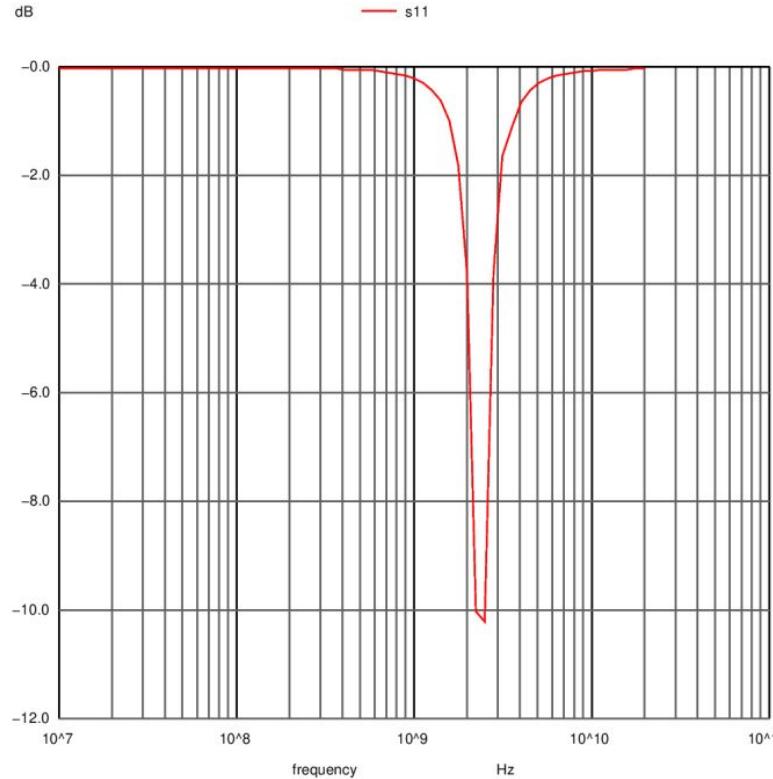


Reference: M.R. Smalley, "Development of a Fully Integrated Wireless Sensor System for Biomedical Applications," M.S. thesis, Dept. of Elect. Eng. and Comp. Sci., Univ. Tennessee, Knoxville. 2022.

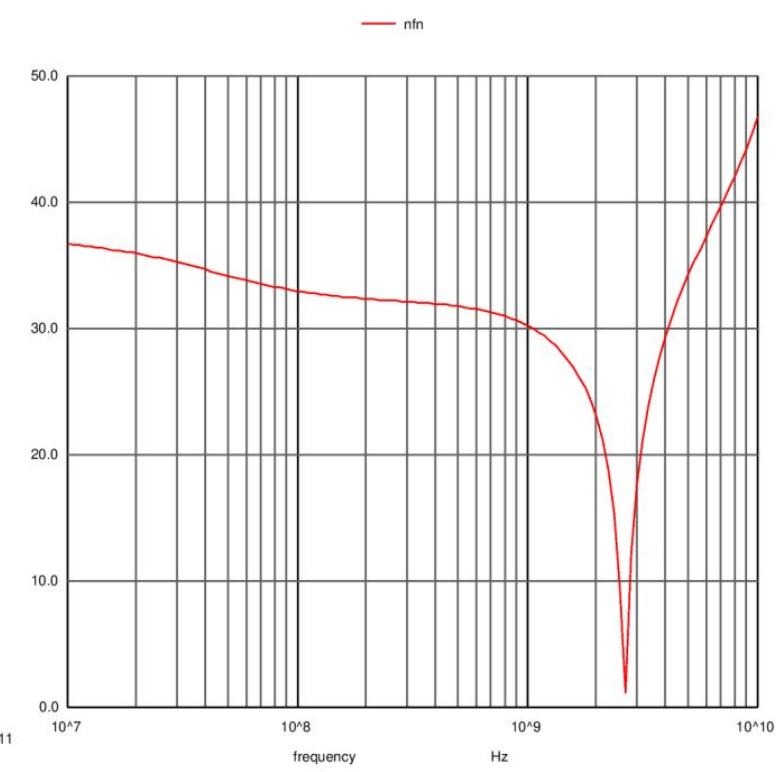
# Wireless Transceiver: Low Noise Amplifier (LNA)



Gain



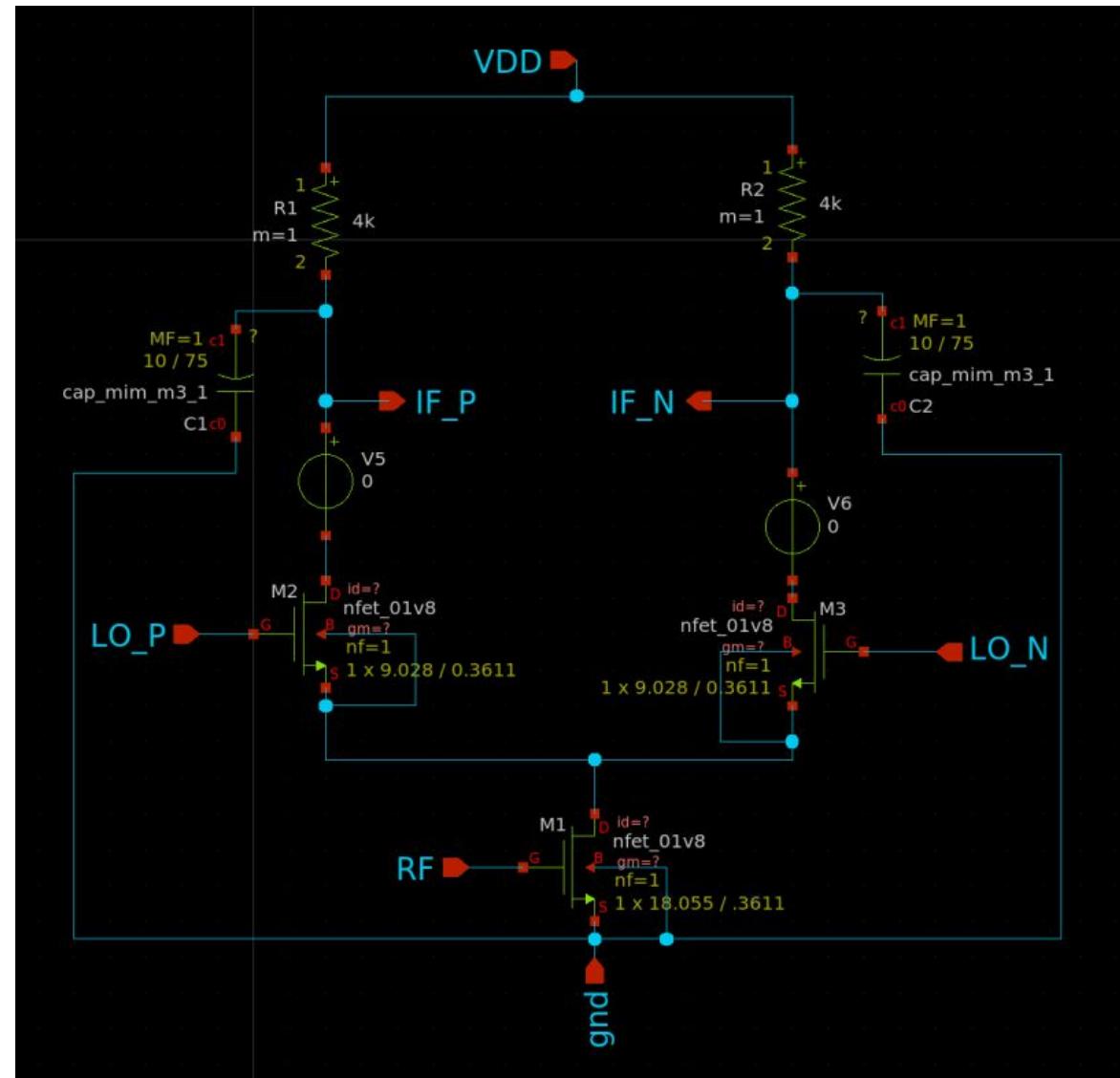
S11



NF

# Wireless Transceiver: Mixer

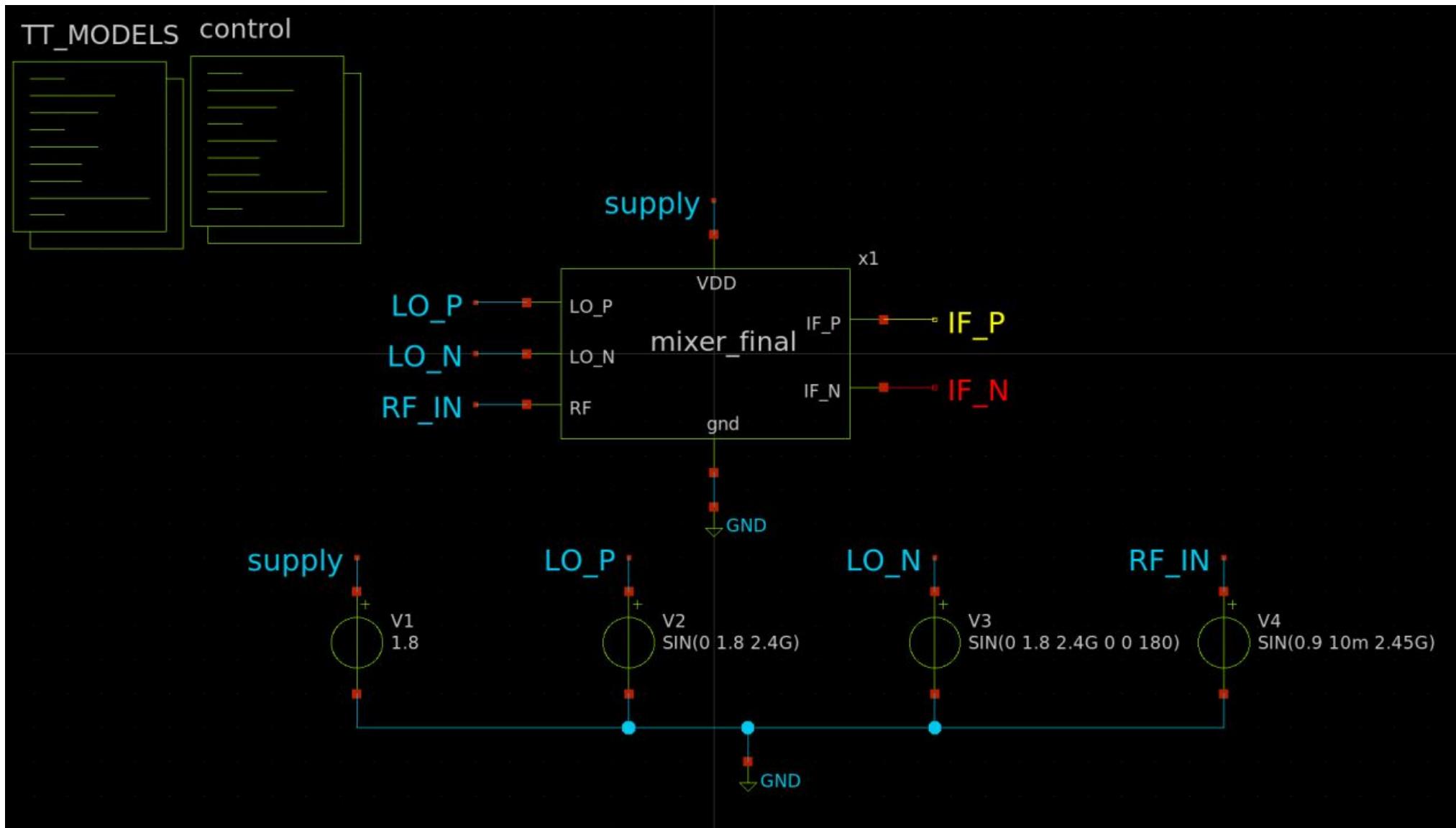
- **Single Balanced Active Mixer Topology**
  - Differential amplifier with a NMOS current source
  - Converts the RF signal into a current through the differential amplifier
  - LO signals control the switching of the differential amplifier downconverting the RF signal to an intermediate frequency
  - Design is inspired by previous UTK student Matthew Smalley's Master's thesis and the information in Razavi's *RF Microelectronics* book
  - V5 and V6 are used for current measurement
  - The resistors are sized such that the DC offset of the IF outputs is at midrail



Reference: M.R. Smalley, "Development of a Fully Integrated Wireless Sensor System for Biomedical Applications," M.S. thesis, Dept. of Elect. Eng. and Comp. Sci., Univ. Tennessee, Knoxville. 2022.

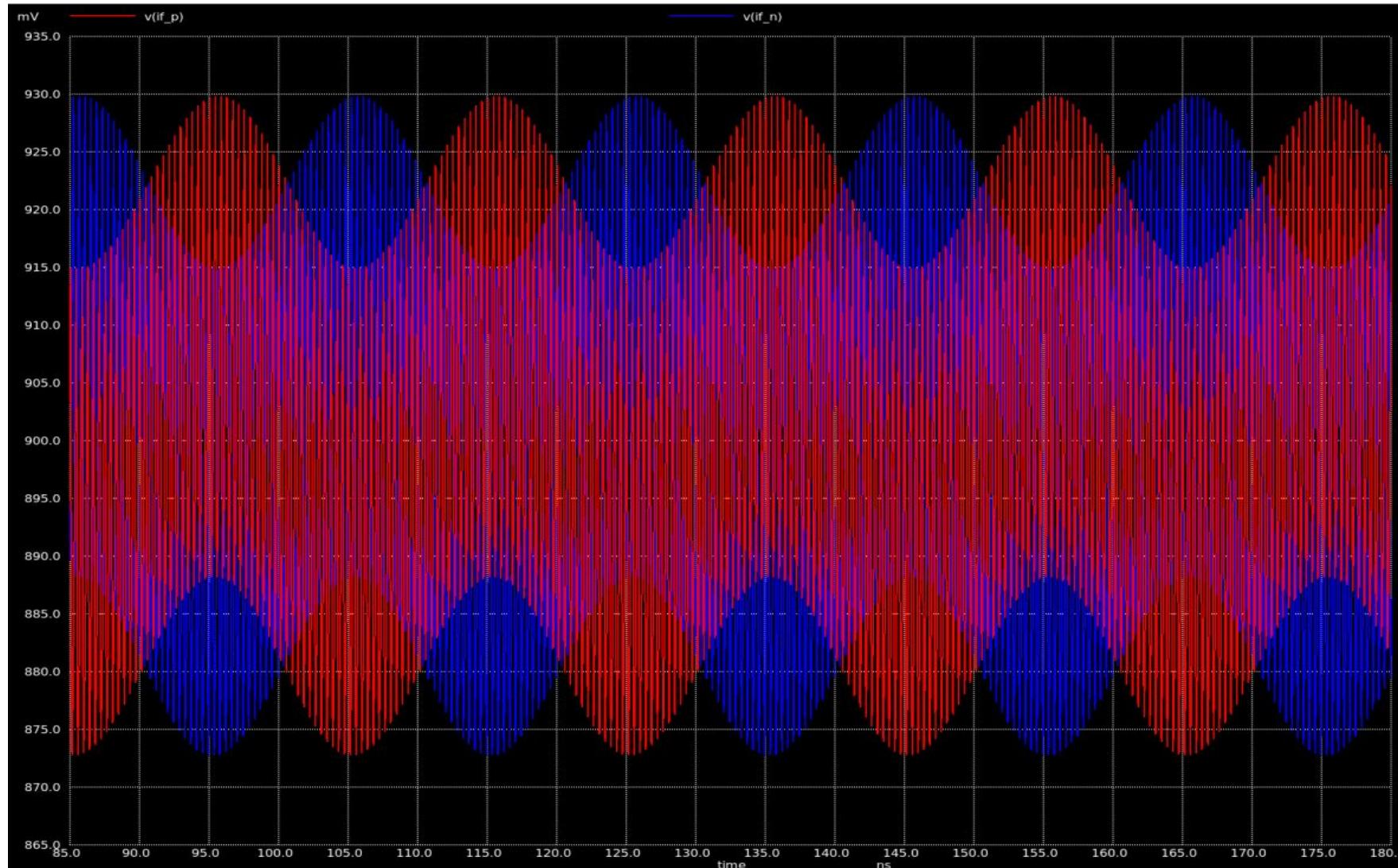
B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, US: Prentice Hall, 1998.

# Wireless Transceiver: Mixer Test Bench



# Wireless Transceiver: Mixer Simulation

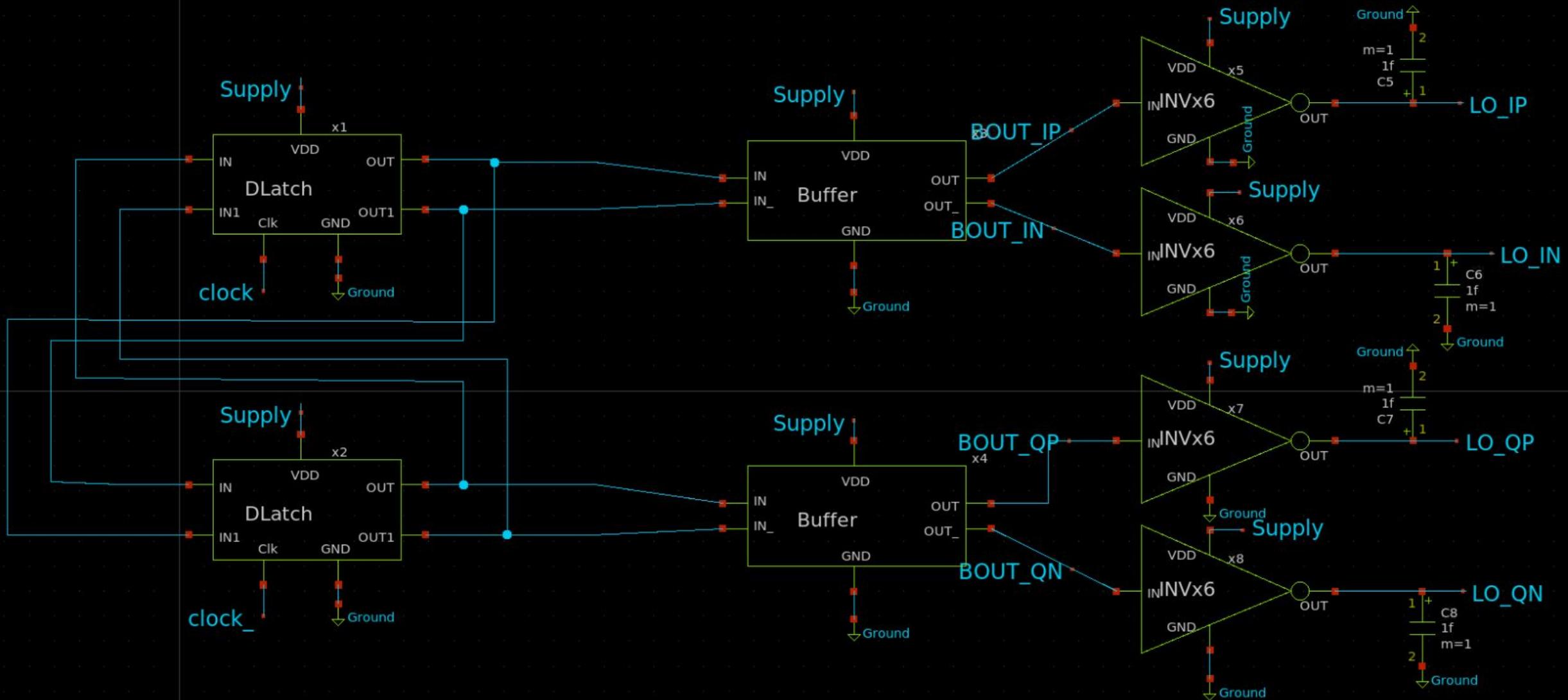
- Envelope has 50MHz frequency
- $2.5\text{G} - 2.45\text{G} = 50\text{MHz}$
- RF - LO = IF
- Steady state has  $\sim 0.9\text{V}$  DC offset



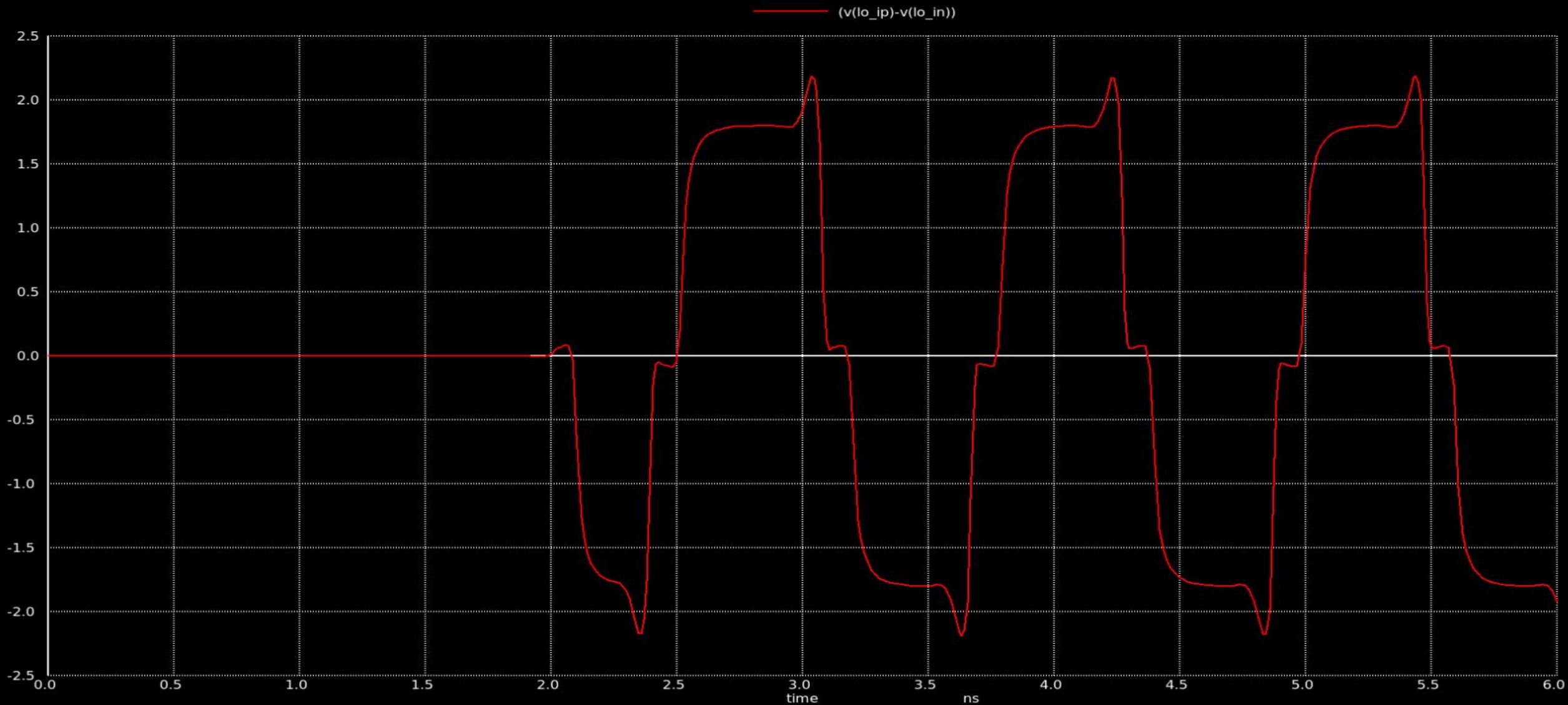
# Wireless Transceiver: Divide By 2

- The divide by two circuit was adapted from Matthew Smalley's previous work
- It takes a high frequency signal from the VCO, lowers the frequency and provides in-phase (I) and quadrature (Q) components for the mixer
- The divide by two is necessary for the direct conversion mixing topology chosen
- It uses two D latches, 2 buffers, and 2 inverter chains to accomplish this
- The current design needs further adjustments
  - the output frequency is lower than the expected 2.5 GHz
  - the output waveform has voltage spikes caused by the inverter circuit

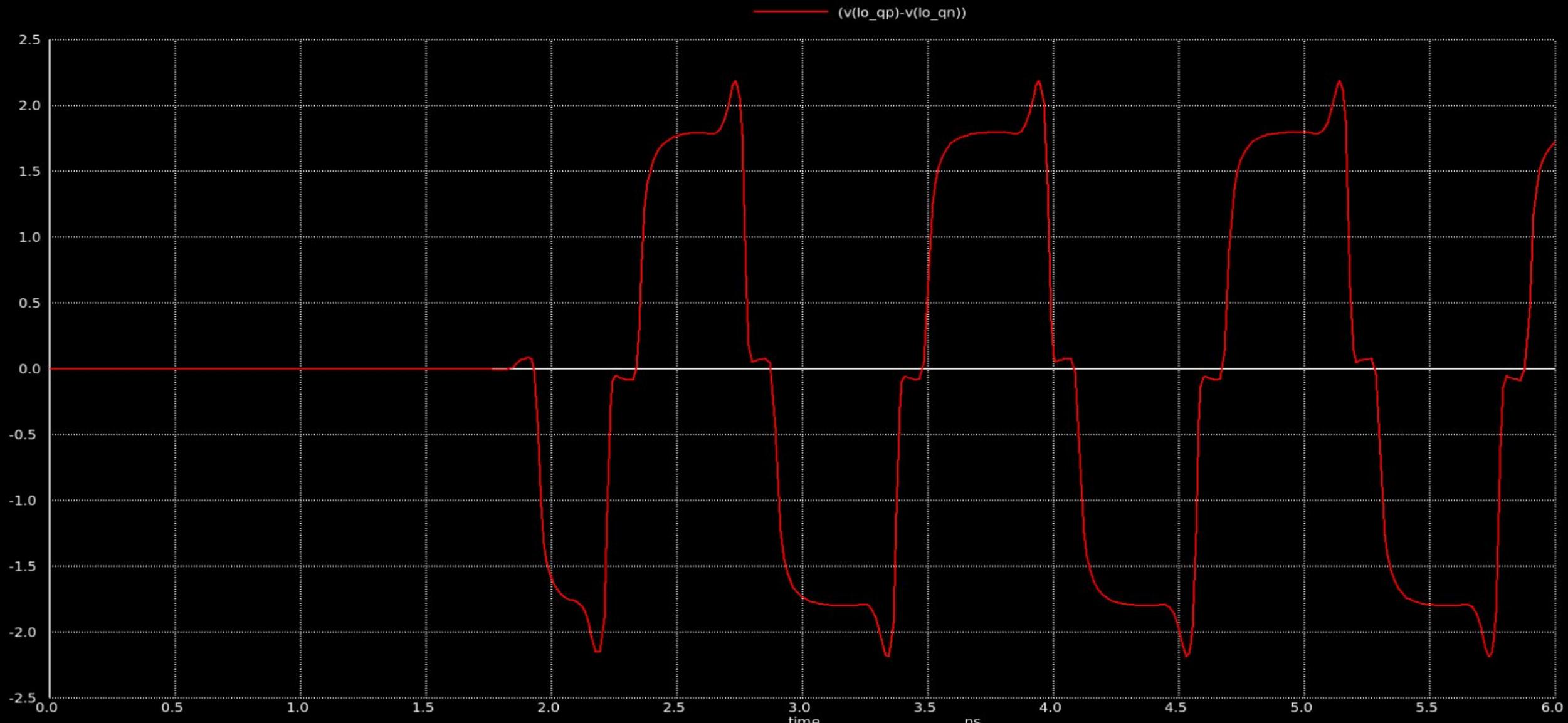
# Wireless Transceiver: Divide by 2



# Divide by 2 Simulation: In-phase Output Waveform



# Divide by 2 Simulation: Quadrature Output Waveform



# Wireless Transceiver-Divide by 2:D-Latch & Buffer Schematic

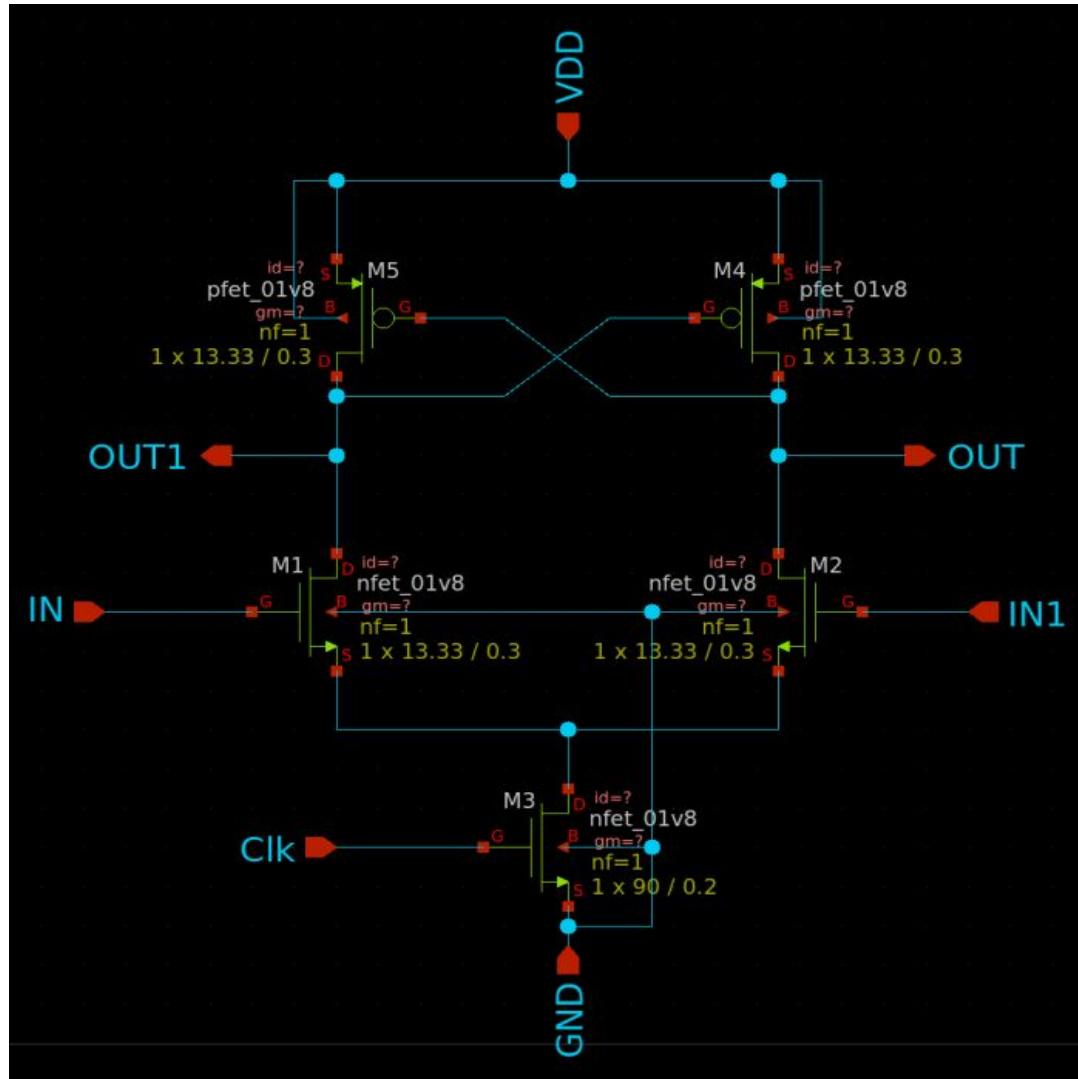


Figure: D-Latch

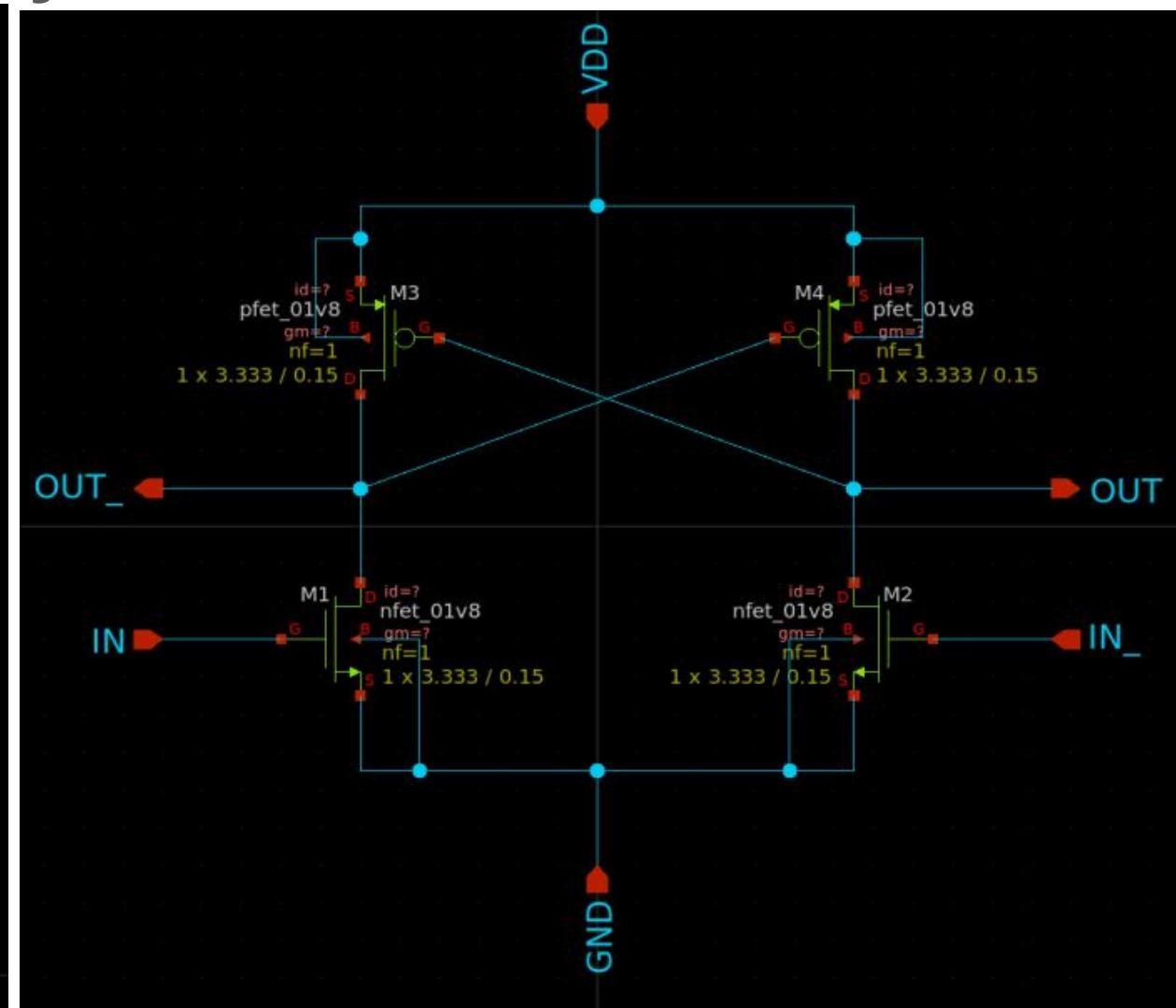
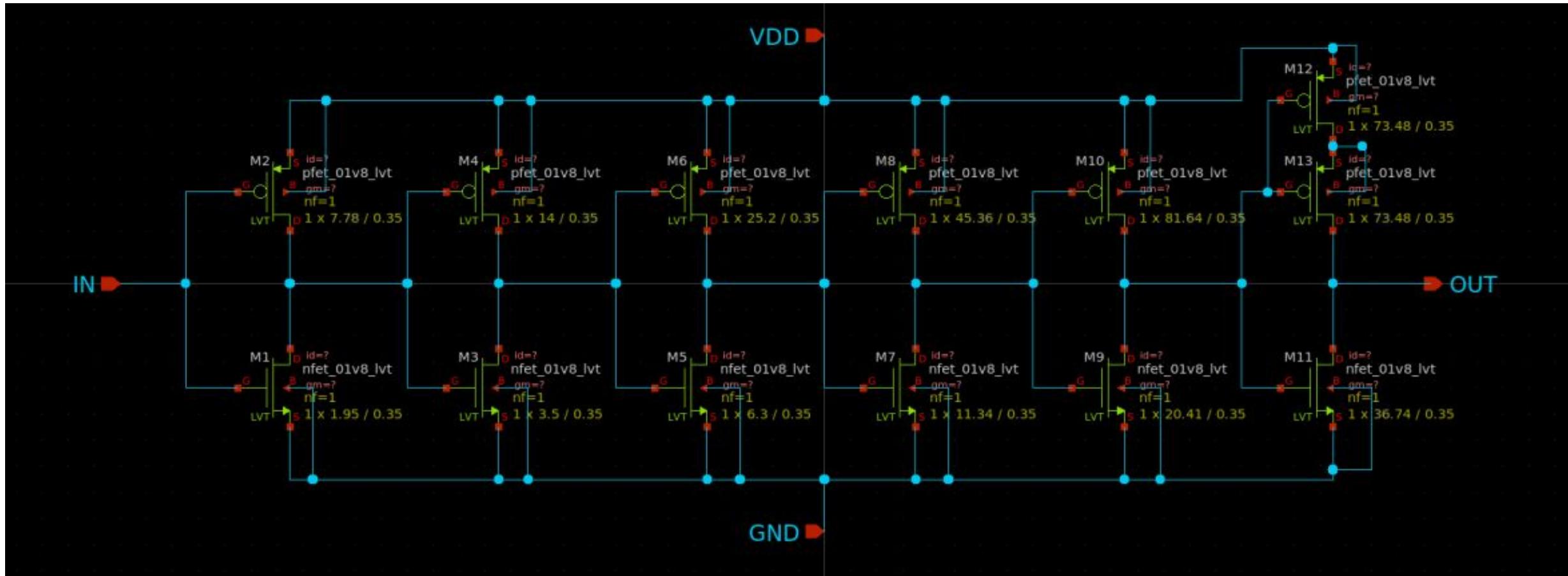


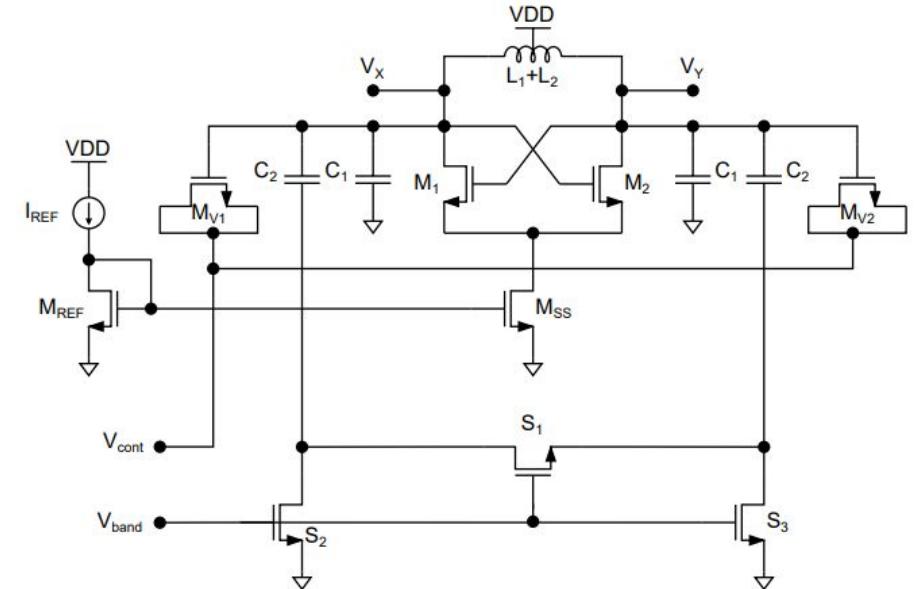
Figure: Buffer

# Wireless Transceiver-Divide by 2:Inverter Schematic



# Wireless Transceiver: Voltage-Controlled Oscillator (VCO)

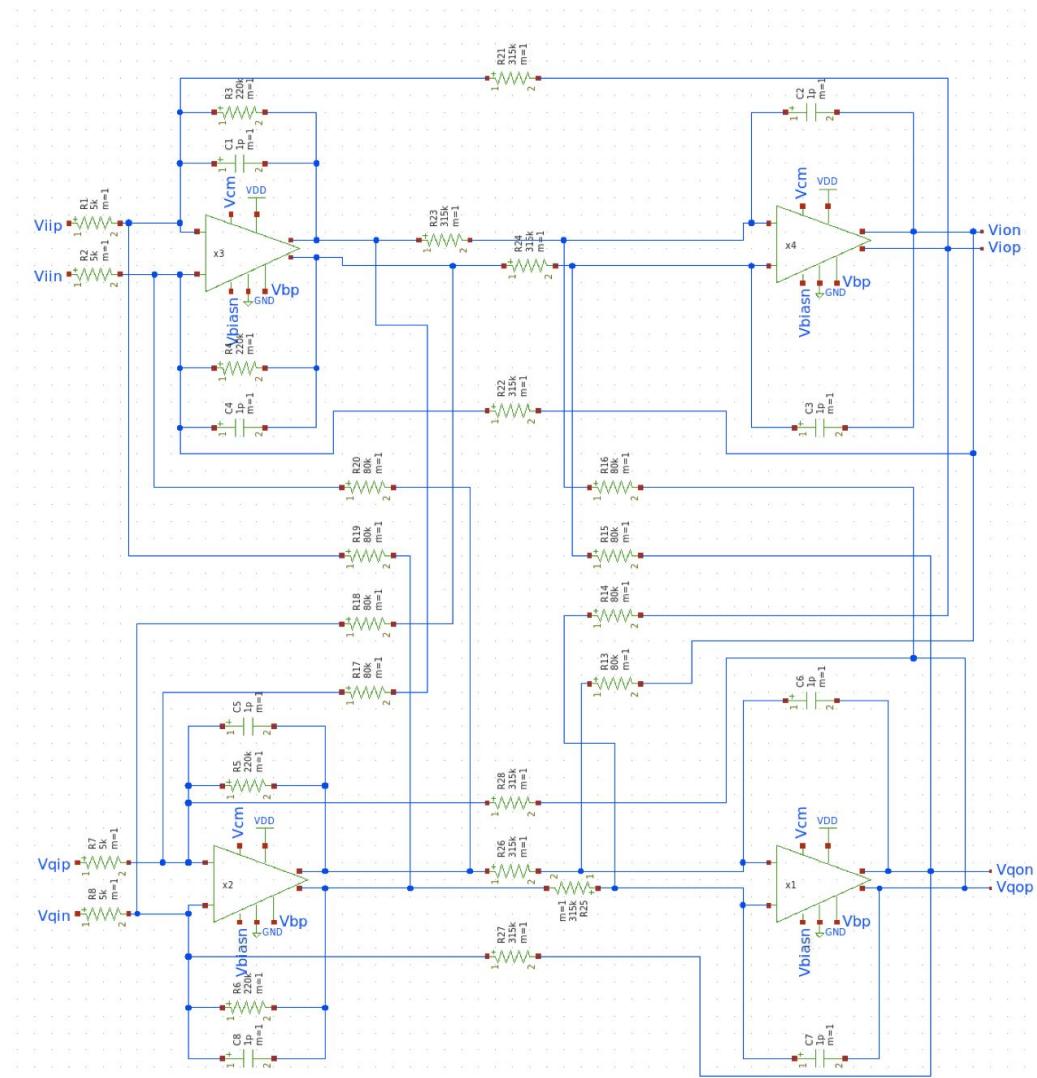
- Cross-coupled oscillator with symmetric inductor topology
- Symmetric spiral inductor excited by differential signals exhibits a higher Q than the single-ended version
- The cross-coupled oscillator consists of two tuned amplifiers with LC tank loads
- Each tuned amplifier realizes a  $180^\circ$  phase shift, so when cascading two together in a feedback loop, the phase shift becomes  $360^\circ$  at the resonant frequency
- If the loop gain is also greater than unity than the circuit will oscillate
- Simulation: (on going)



# Wireless Transceiver: Intermediate Frequency Filter

- **IF Polyphase Filter:**

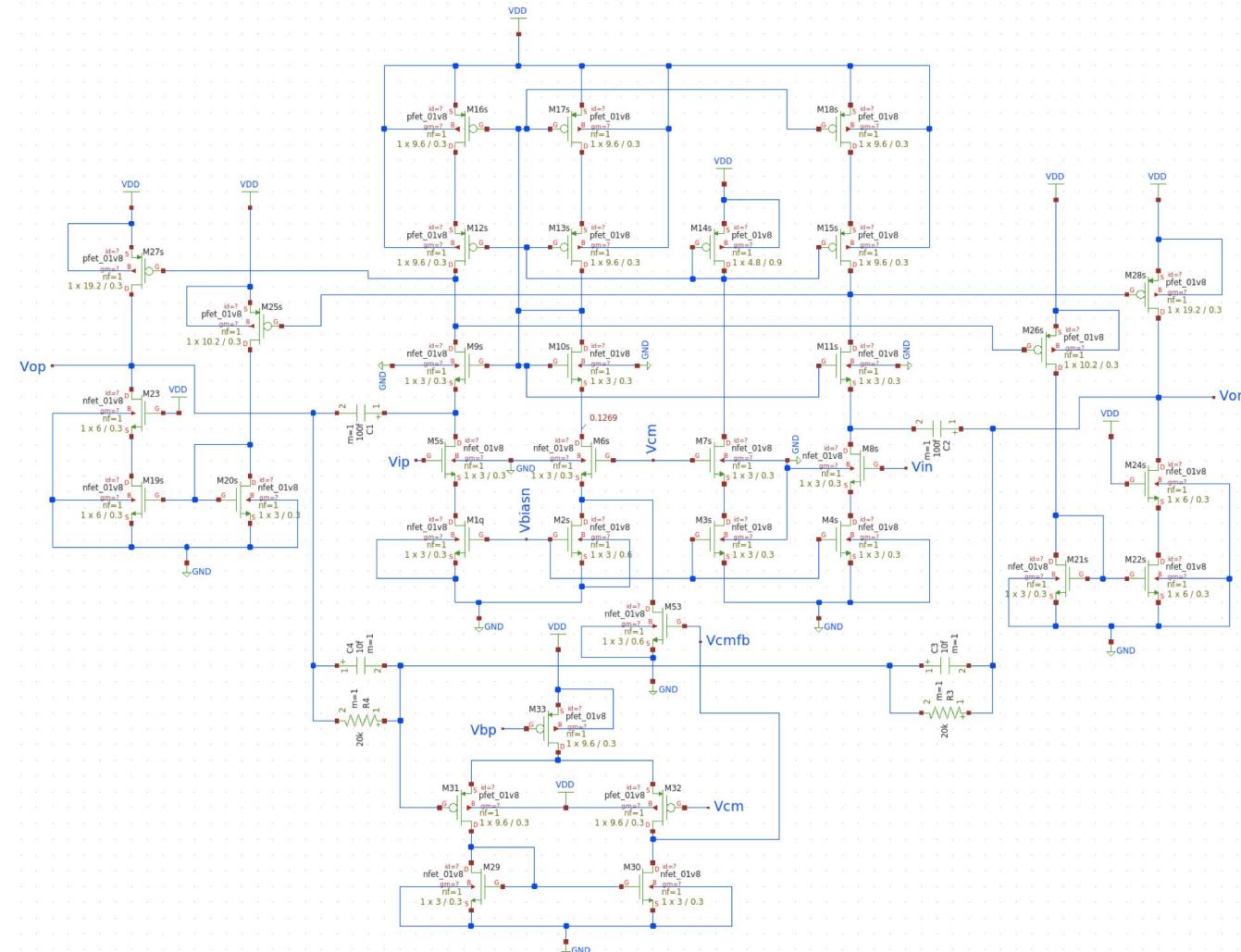
- Low Pass Tow-Thomas Biquad with applied polyphase transformation
- Realized by shifting the poles of a low pass filter by the center frequency of the polyphase filter using fully differential op amps as active elements
- Provides channel selection for only desired IF band, applying attenuation to all other frequencies for in-phase and quadrature modulation
- Simulation: (on-going)



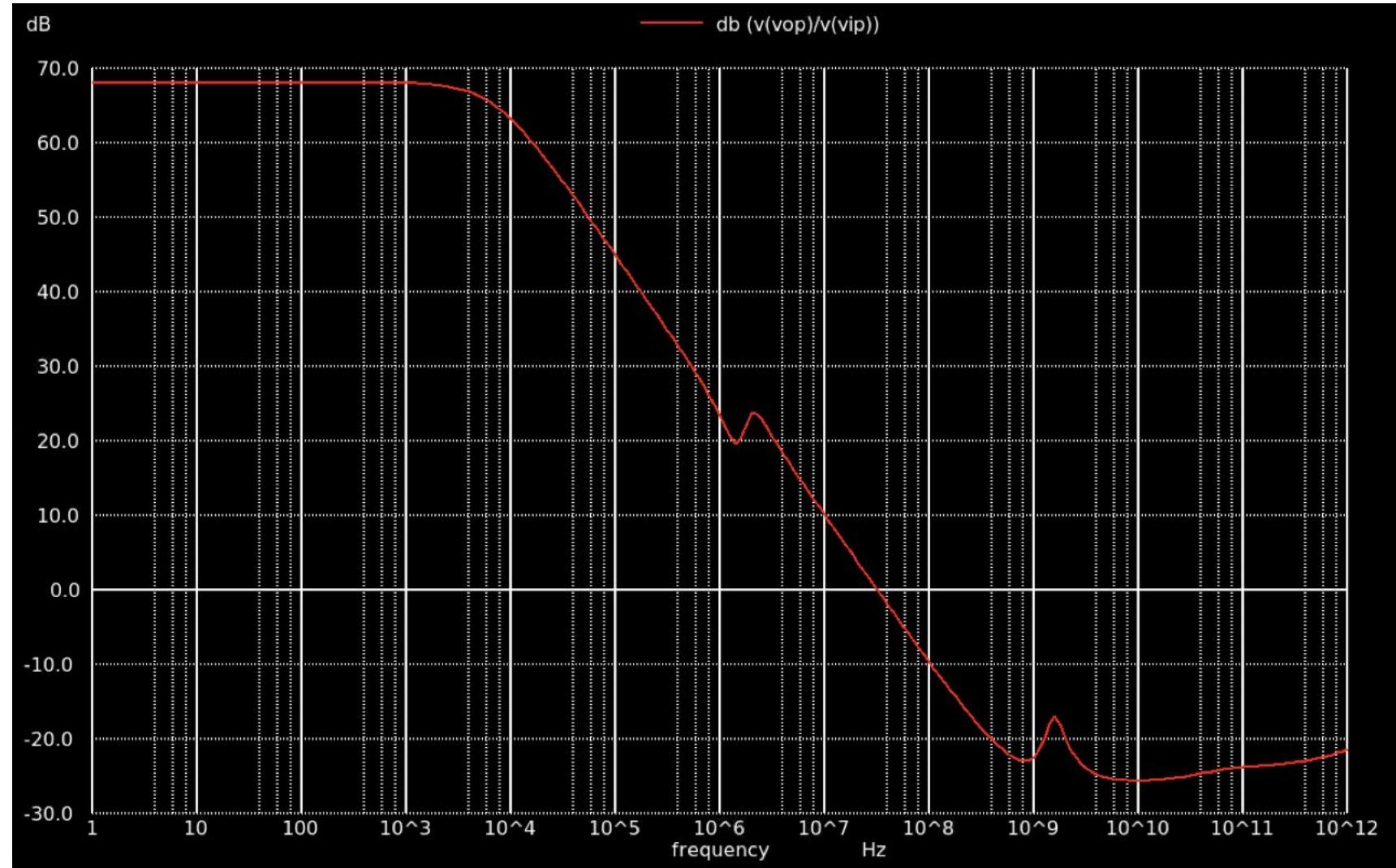
# Wireless Transceiver: Intermediate Frequency Filter

- Op Amp Design Specifications:

- Two-stage with a cascode loaded differential amplifier stage, followed by a class-AB output stage
- Common-mode feedback is applied to fix the common-mode output voltage level to be mid-rail
- Increase in the differential amplifier's output voltage lowers the current flowing through the output buffers, causing the output voltage to move down.
- The buffer stage devices are made larger to compensate for the gain decrease from the averaging resistors from the CMFB amplifier



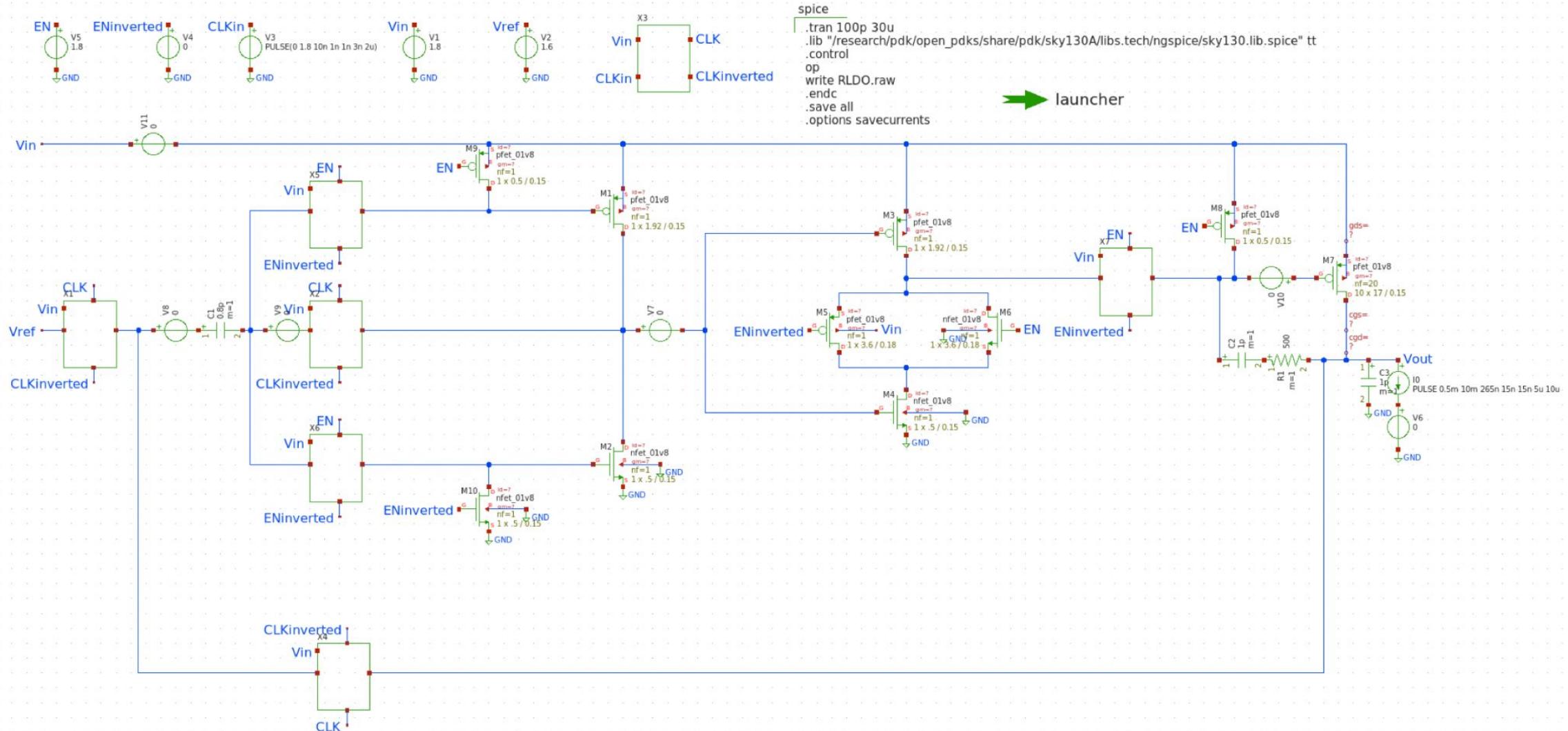
# Wireless Transceiver: IF Filter Simulation: (on-going)



# Ring Amplifier-Based LDO (RLDO)

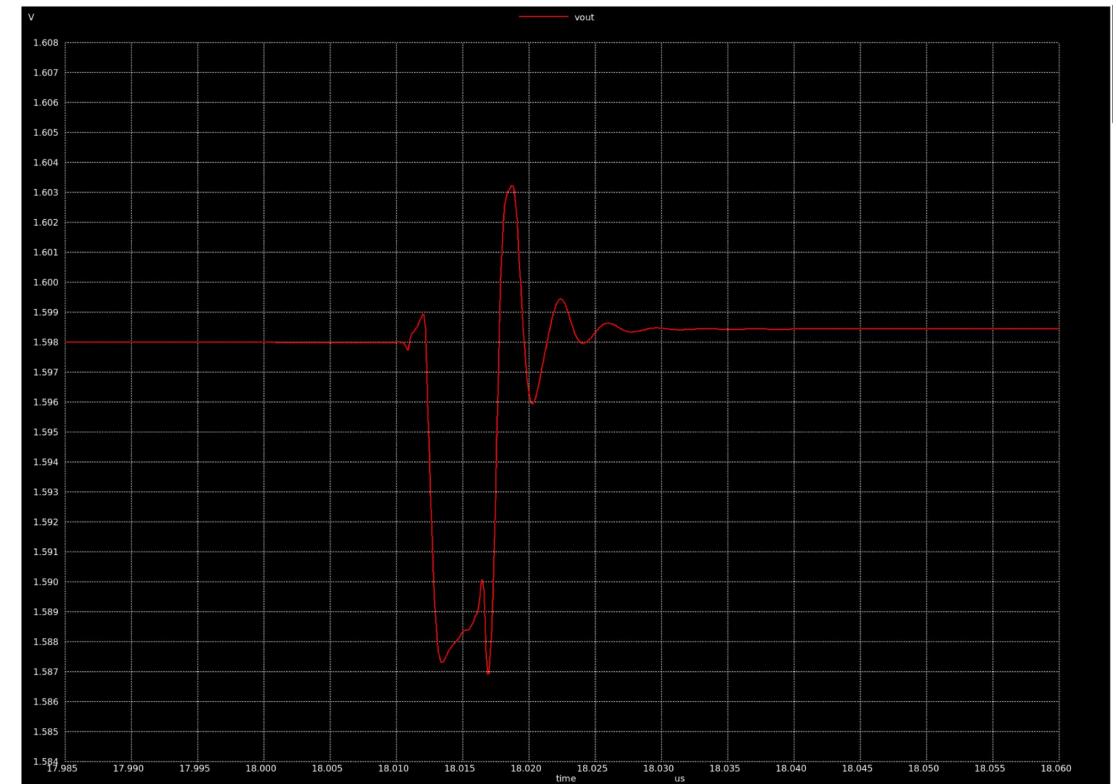
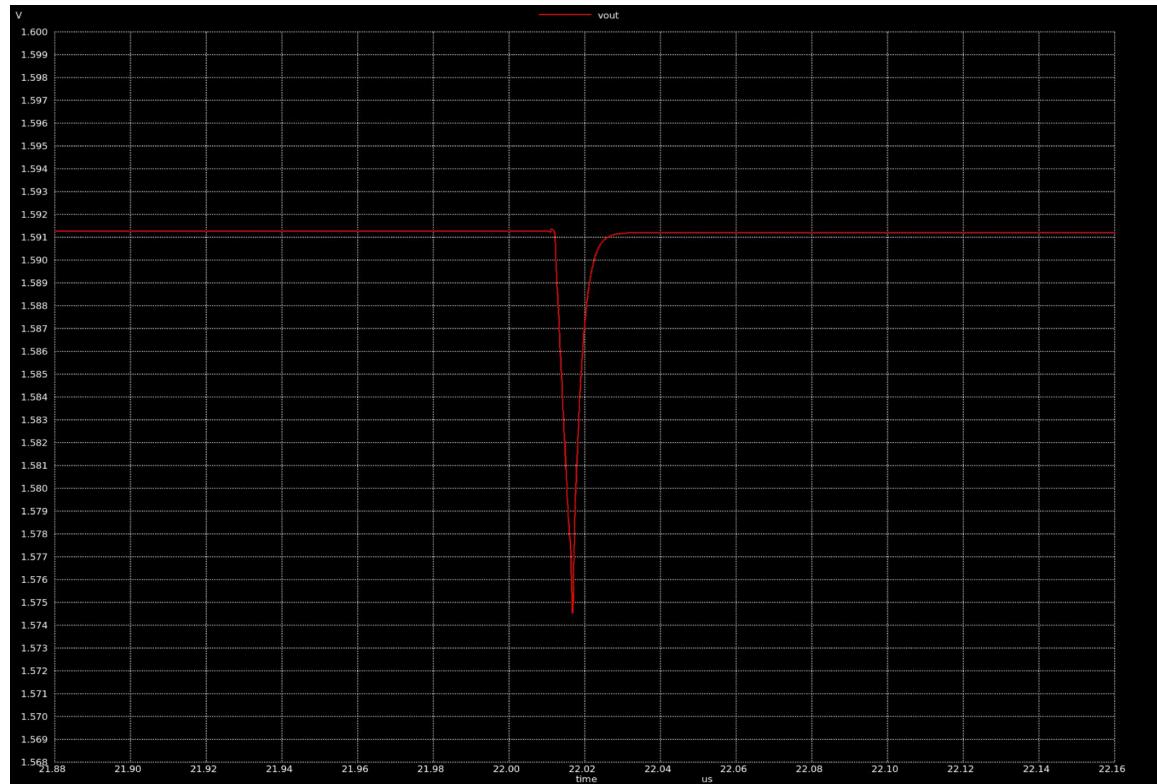
- The power supply is input into the RLDO, and the output, which should be about 1.6V, is passed onto power the transceiver and other biasing circuitry
- The ring amplifier is made up of two inverter stages (M1, M2, M3, M4)
- A pass device (M7) is used as an inverter for the third stage, and it supplies current to the loads
- A floating battery is implemented for shutdown and prevention of current leakage into the gate of the pass device (M5, M6)
- All of the switches are made using T-Gates (X1, X2, X4, X5, X6)
- The differential clock signal is generated by a pseudo-differential switch driver (X3)
- The RLDO has two phases: a sampling period and an amplifying period. Ideally, the output voltage should be 1.6V, or VREF, during the amplifying period.

# RLDO Schematic



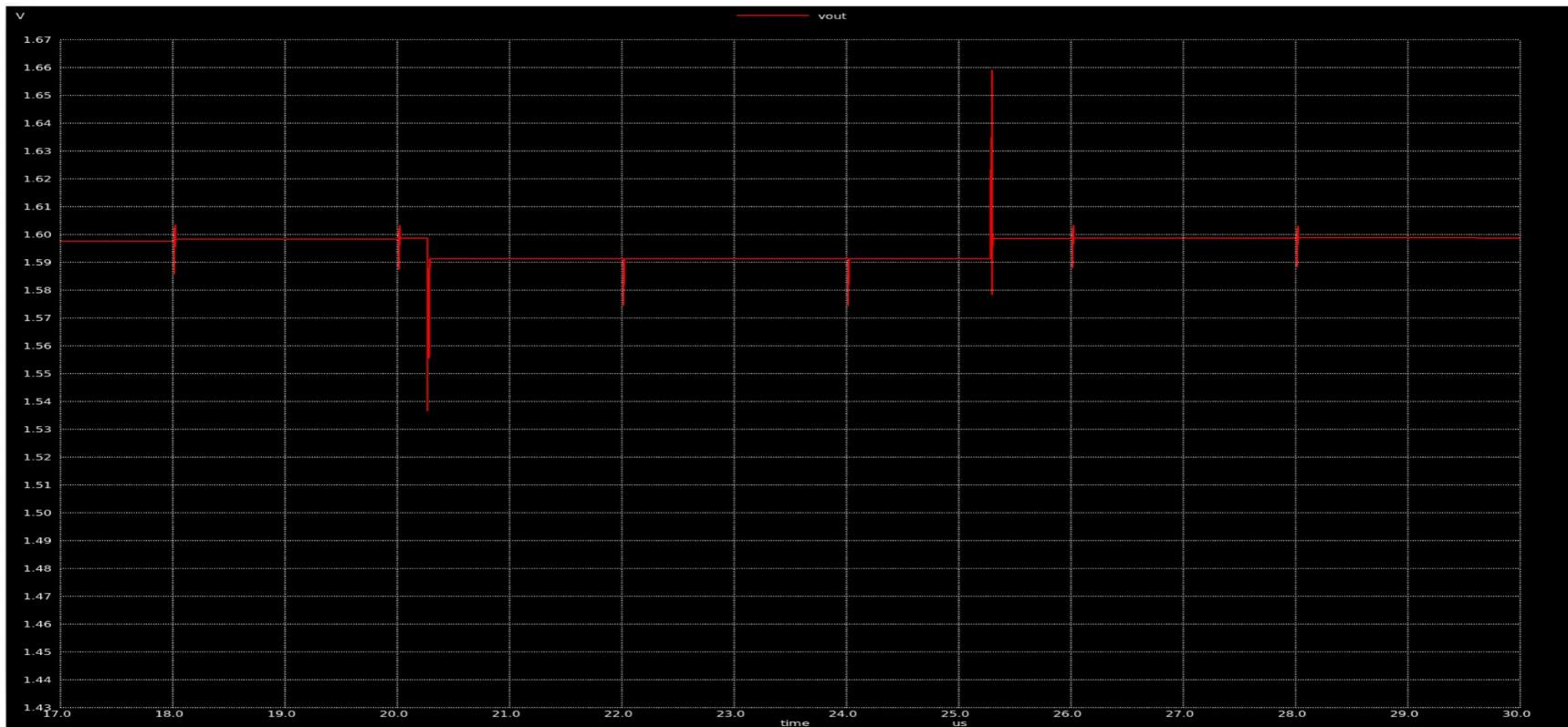
# RLDO Simulation Results

- Transient results: Vout holds high, with the only dips occurring during the sampling time
- The right image shows the sampling period for low load current (0.5mA)
- The left image shows the sampling period for high load current (10mA)

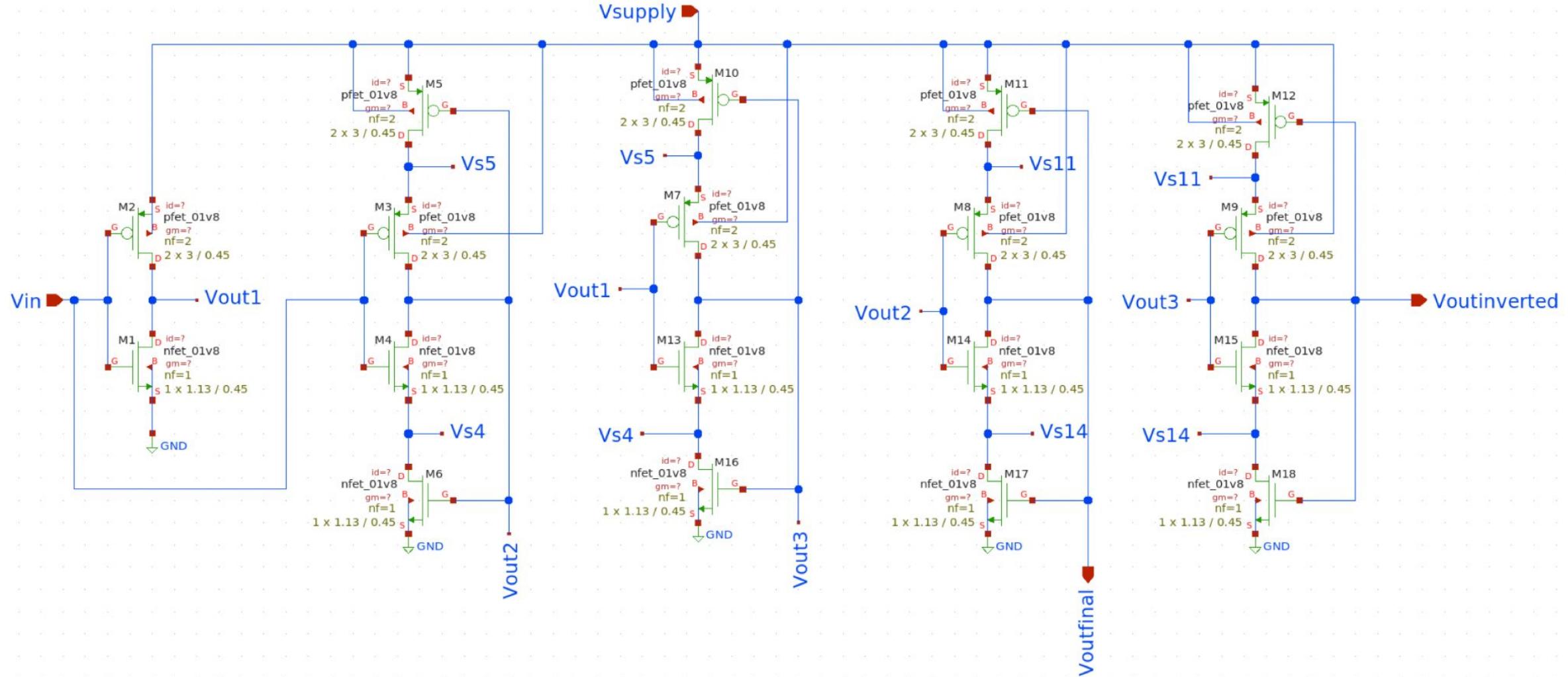


# RLDO Simulation Results

- The image below shows a more complete view of the output voltage
- Still left to test: Periodic Steady State simulation
  - This test will confirm the gain margin and phase margin. It is estimated that both are reasonable in this design, but we don't have specific numbers yet

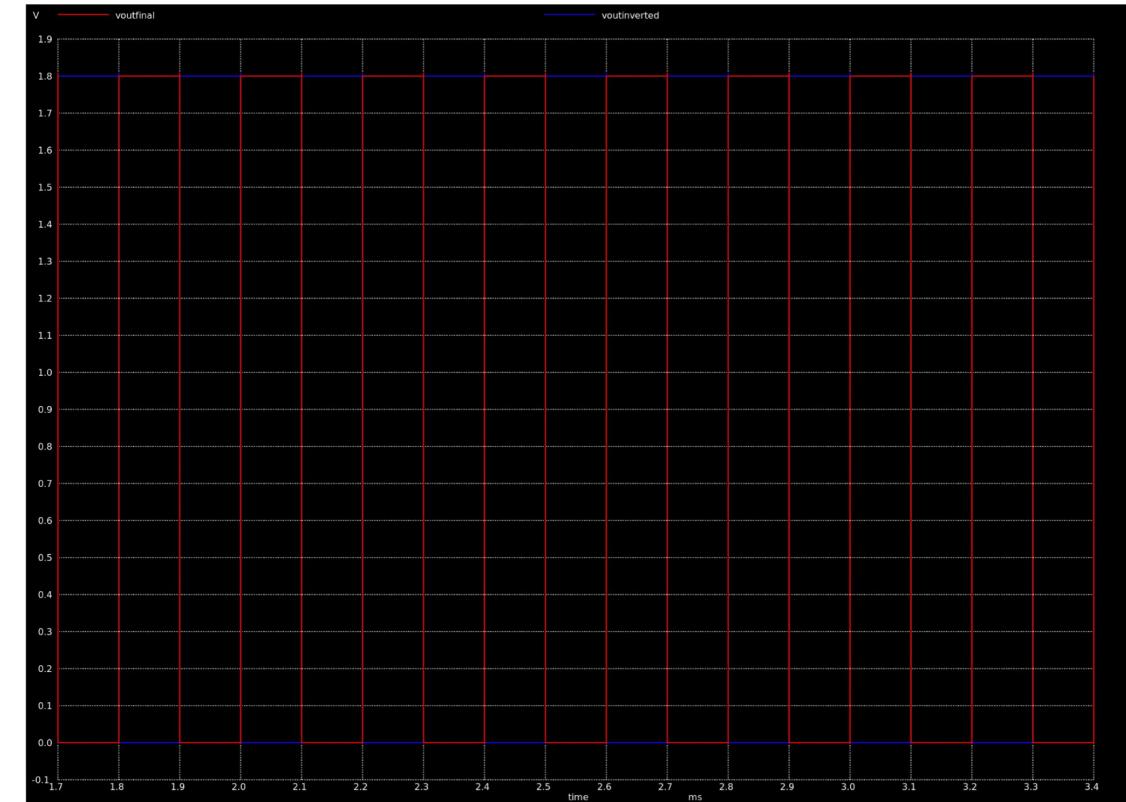
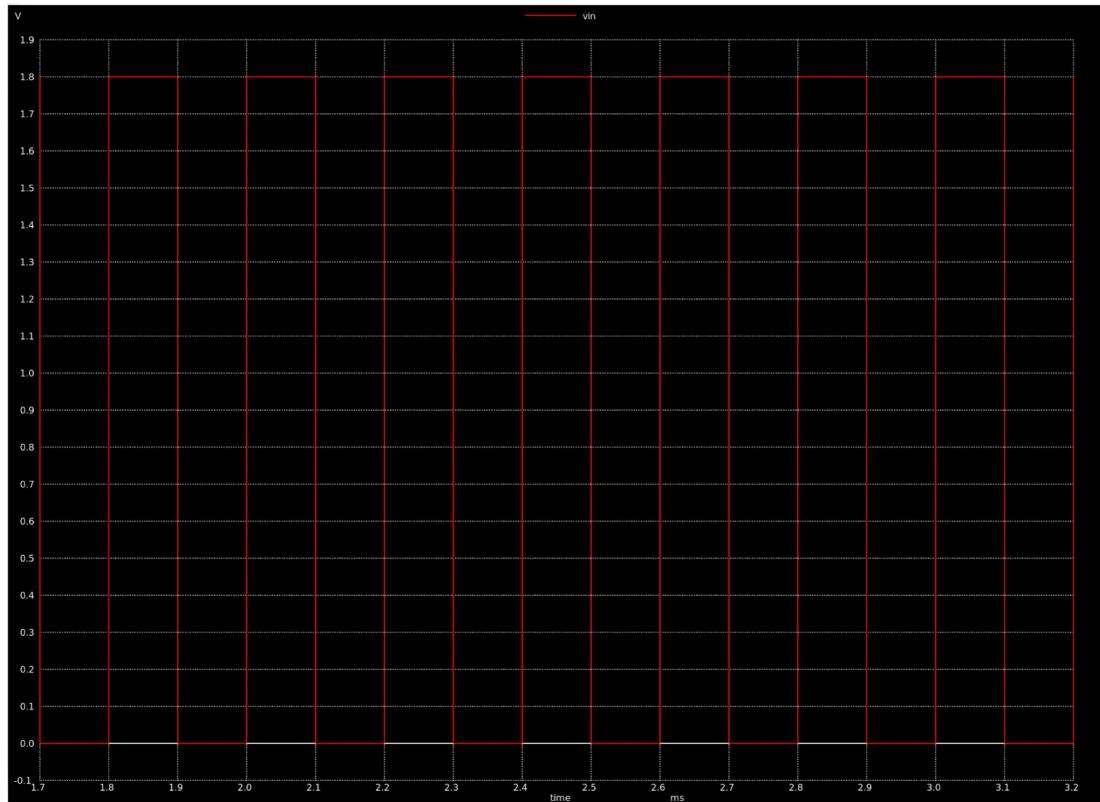


# RLDO - Pseudo-Differential Switch Driver



# Pseudo-Differential Switch Driver Simulation Results

- The idea behind the circuit is to take a clock input and output a differential clock signal
- The simulation results below show the clock input (left) as well as the two outputs that make up the differential clock signal (right)
- The test was successful, and no further testing is needed



# Progress Summary

Circuit Blocks	Design status	TO DO
Analog Front-End	All Individual blocks are done. Tests: 80%, ongoing	Integration and combined simulation
Wireless Transceiver	One block (PA) will be designed next week. Tests: 70%, ongoing	Complete design and combined simulation
Microprocessor	On-chip MP connectivity under review.	Finalize connections to AFE and WT

# Project Milestones (Internal)

Tasks	Target deadline
Finalize Schematics with complete analysis	Oct 7
Initial layout of each block	Oct 14
Finalize layout, start LVS	Oct 24
Complete LVS, finalize layout	Oct 31
Caravel integration and final GDS ready	Nov 7

# Pin list and area estimate

Pin #	Description	I/O/Bidir/Sup	Pin Name	User area supply	GPIO used as analog	GPIO used as digital
1	Analog GND	Sup	gnd	x		
2	Analog VDD	Sup	vdd	x		
3	Reference Electrode	I	re		x	
4	Working Electrode	I	we		x	
5	Counter Electrode	O	ce		x	
6	TIA Output	O	tia		x	
7	VCO Output	O	vco_out			x
8	VCO Digital Supply	Sup	vco_vdd			x
9	Reset	I	cap_reset			x
10	LNA Input	I	rf_in		x	
11	LNA Output/Mixer Input	Bidir	mix_in		x	
12	Mixer In-phase positive output/Filter Input	Bidir	vif_inp_pos_in		x	
13	Mixer In-phase negative output/Filter Input	Bidir	vif_inp_neg_in		x	
14	Mixer quadrature negative output/Filter Input	Bidir	vif_q_pos_in		x	
15	Mixer quadrature negative output/Filter Input	Bidir	vif_q_neg_in		x	
16	Filter In-phase Output (Positive)	O	vif_inp_pos_out		x	
17	Filter In-phase Output (Negative)	O	vif_inp_neg_out		x	
18	Filter quadrature Output (Positive)	O	vif_q_pos_out		x	
19	Filter quadrature Output (Negative)	O	vif_q_neg_out		x	
20	VCO band select voltage - ON/OFF	I	v_band			x
21	VCO control voltage for varactors 0-1.2V	I	v_ctrl			x
22	VCO positive frequency output	O	f_vx			x
23	VCO negative frequency output	O	f_vy			x
24	LDO VDD	Sup	ldo_vdd		x	
25	LDO VOUT	O	ldo_vout		x	
26	LDO ENABLE	I	ldo_enable			x
27	CLOCK	I	clk			x
28	VREF	I	ldo_vref		x	
29	Deadzone PMOS VREF	I	ldo_dzone_pm_vref		x	
30	Deadzone NMOS VREF	I	ldo_dzone_nm_vref		x	
31	Pass Device Gate	Bidir	ldo_pass_gate		x	

- Estimated area:  
AFE: 0.3x0.5 mm<sup>2</sup>  
WT: 2x2.5 mm<sup>2</sup>  
RLDO: 0.6 mm<sup>2</sup>
- Total: ~ 7.1 mm<sup>2</sup>

Github:  
<https://github.com/AndalibN/Electrochemical-Water-Quality-Monitoring>