Anderson Hsieh

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Skills

Hardware: Xilinx Spartan 7 FPGA, Vivado, Cadence Virtuoso, Cocotb, Proteus, Modelsim, Frontend Architecture Design
Software: Linux**,** Android, Spring Boot, MySQL, React, Next.js, Redux, Docker, Git
Programming languages: Verilog, VHDL, Python, C, C++, Java, Kotlin, SQL, JavaScript, HTML, CSS

Projects

8-bit softcore CPU (On Going) | Github | Schematic Diagram

- Designed an 8-bit **accumulator based** CPU in Verilog targeting Xilinx Spartan 7 FPGA with custom ISA.
- Built **2 stage pipeline** (fetch, decode + execute) datapath with ALU, synchronous RAM with clock gating, CPU bus, 8 available registers, and instruction decode logic control blocks. Average CPI is 2.16 targeting 90 MHz clock frequency.

EEPROM reader | Github

- Implemented IP that reads data from **24 series I2C EEPROM** using Verilog and Vivado, hex data is displayed with LEDs
- Created System Verilog testbenches and simulated "random read" with Vivado simulator, debugged with USB logic analyzer

Systolic array matrix multiplier

- Implemented 8-bit number matrix multiplication in Verilog, simulated with Modelsim and deployed to PYNQ-Z1 board
- Entered **class Hall of Fame** by achieving 25 X 25 matrix MACC running on 105 MHz with limited hardware resources on Xilinx Zynq®-7000 SoC with compiler attributes and Parallel Multiplication with Single DSP Slice (PMSDS)

More Projects…

Work Experience

AI Hardware Architecture Engineer @ UntetherAI | Toronto ON, Canada — May 2023 - Aug 2022

- Implemented **core IPs with SystemVerilog**, including the matrix multiplication processing element, architecture-specific and number format datapath control, 2s complement to floating point conversion block, and custom SRAM control logic.
- Created VCD generation **test benches with Cocotb and Python** for MACC and number format conversion operations
- Developed Python and Google app scripts for parsing hierarchical power/area numbers generated from **Design Compiler and ICC2** into readable dropdown lists. Saved the team a tremendous amount of time from copy and pasting.
- Created **test benches with Cadence Virtuoso** and characterized TSMC 5nm library transistors with Synopsys PrimeSim, recorded spice simulation I-V curves with different parameters for circuit design engineers.

Full Stack Software Developer @ FleetComplete | Waterloo ON, Canada — Apr 2022 - Aug 2022

- Designed and implemented data mapping across microservices, feature shipped to over **35000 subscribers** around the world
- Implemented searching, filtering, sorting, and pagination of entities with JDBC, SQL, and Protobuf with unit tests.
- **Reduced 70% + code redundancy** by refactoring code around error code mapping and Kafka connection between services

Assistant Engineer @ KKtream Ltd. | Taipei City, Taiwan — Aug 2021 - Dec 2021

- Optimized testing efficiency by 30% by rebuilding Android automation testing in Jenkins pipeline with Espresso and Java
- Developed all test cases for two major features on Android & IOS music app with TestRail and exploratory testing, features shipped to **3.5 million Japanese users** and usage of the two modules increased by 10%

Firmware Test Engineer Intern @ Barco N.V | New Taipei City, Taiwan — Dec 2020 - Apr 2021

- Supported new testing environment integration for TLS/TTLS authentication with Linux, FreeRadius, switches and routers
- Coached interns in onboarding and testing tool usage like Android ADB, Linux commands, Samba and Xlight FTP server setup

Volunteer Experience

President @ WLOOSERVE | Waterloo, ON — May 2022 - Present

- Lead 15 execs to run a **300+ member** volleyball club, including drop-in sessions, tournaments, social media, merch, skill clinic

Education

Candidate for Bachelor of Applied Science in Computer Engineering, University of Waterloo — Sep 2020 – Apr 2025

- Relevant courses: Computer Architecture, Digital Hardware Sys, Semiconductor Physics — Average: 84.39 %, GPA 3.7 / 4.0