PIC18F97J60 FAMILY

Flash Microcontroller Programming Specification

1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F66J60
- PIC18F66J65
- PIC18F67J60
- PIC18F86J60
- PIC18F86J65
- PIC18F87J60
- PIC18F96J60
- PIC18F96J65
- PIC18F97J60

2.0 PROGRAMMING OVERVIEW OF THE PIC18F97J60 FAMILY

The PIC18F97J60 family devices are programmed using In-Circuit Serial Programming™ (ICSP™). This programming specification applies to devices of the PIC18F97J60 family in all package types.

2.1 Pin Diagrams

The pin diagrams for the PIC18F97J60 family are shown in Figure 2-1 through Figure 2-3. The pins that are required for programming are listed in Table 2-1 and shown in darker lettering in the figures.

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F97J60 FAMILY

Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
$\overline{MCLR}$	$\overline{MCLR}$	P	Programming Enable
VDD and AVDD(1)	VDD	P	Power Supply
VSS and AVSS(1)	VSS	P	Ground
ENVREG	ENVREG	P	Internal Voltage Regulator Enable
VDDCORE/VCAP	VDDCORE	P	Regulated Power Supply for Microcontroller Core
	VCAP	I	Filter Capacitor for On-Chip Voltage Regulator
RB6	PGC	I	Serial Clock
RB7	PGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power

Note 1: All power supply and ground pins must be connected, including analog and Ethernet supplies (AVDD, VDDPLL, VDDRX, VDDTX) and grounds (AVSS, VSSPLL, VSSRX, VSSTX).

FIGURE 2-1: PIC18F97J60 FAMILY PIN DIAGRAMS

64-Pin TQFP

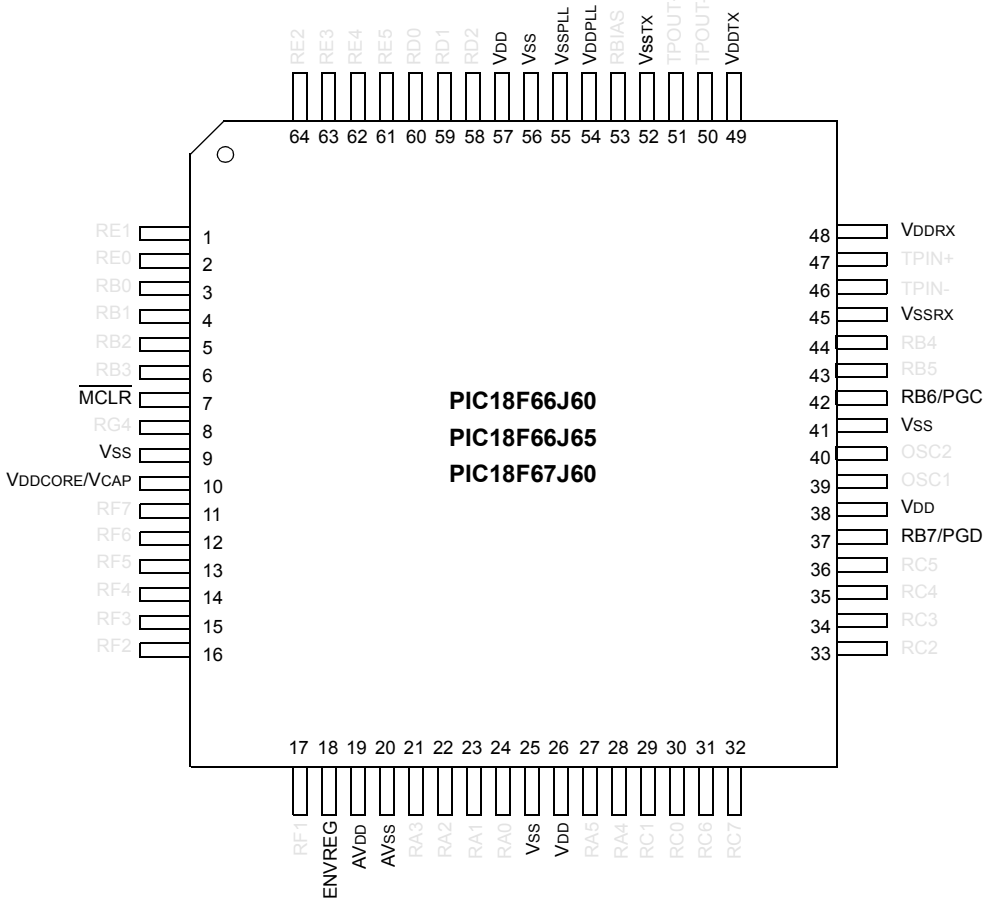


FIGURE 2-2: PIC18F97J60 FAMILY PIN DIAGRAMS (CONTINUED)

80-Pin TQFP

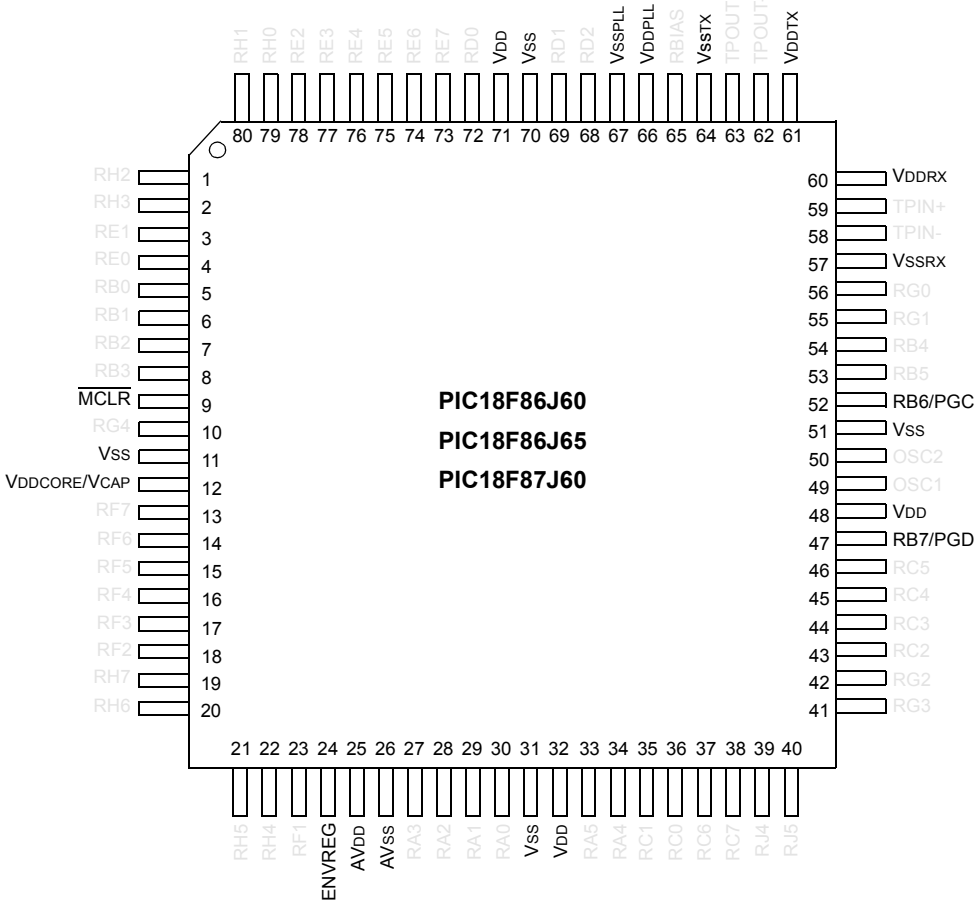
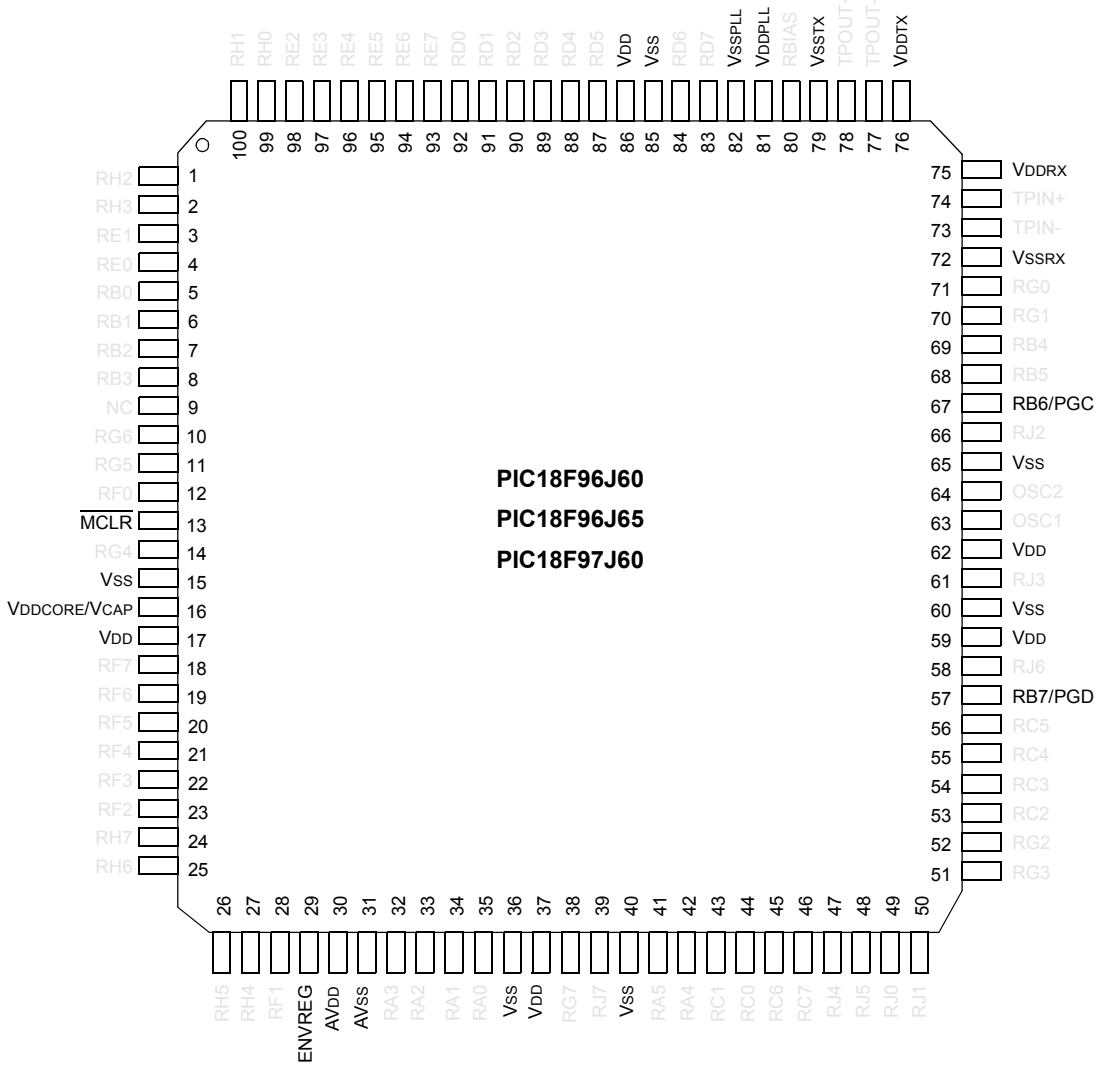


FIGURE 2-3: PIC18F97J60 FAMILY PIN DIAGRAMS (CONTINUED)

100-Pin TQFP



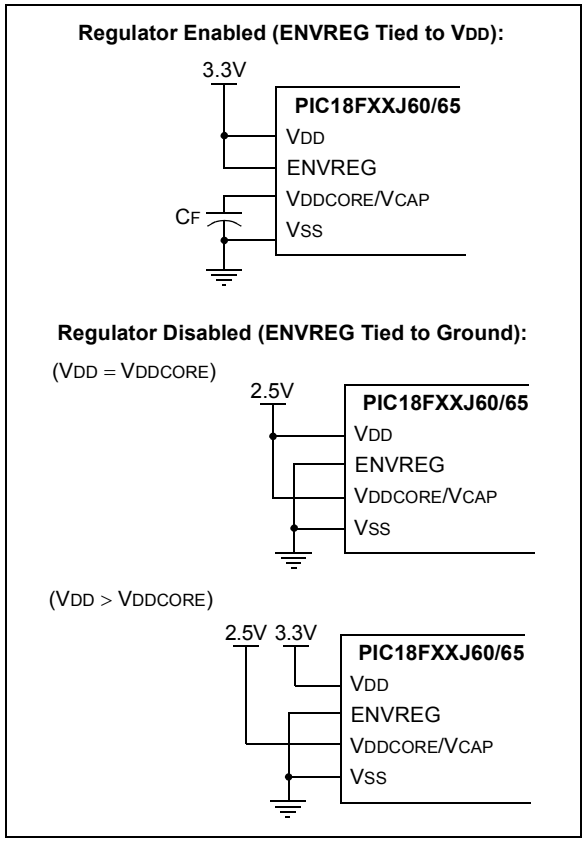
2.1.1 ON-CHIP VOLTAGE REGULATOR

The microcontroller core of PIC18F97J60 family devices can be powered either from an external source, or from an on-chip regulator, which derives power from VDD. Both sources use the common VDDCORE/VCAP pin.

The regulator is enabled by connecting VDD to the ENVREG pin. In this case, a low-ESR capacitor must be connected to the VDDCORE/VCAP pin for proper device operation. If the regulator is disabled, power to the core must be supplied on VDDCORE/VCAP. Where VDD exceeds VDDCOREMAX, power to the core must be supplied separately on VDDCORE/VCAP. Examples are shown in Figure 2-4. Whether or not the regulator is used, it is always good design practice to have sufficient capacitance on all supply pins.

The specifications for core voltage and capacitance are listed in **Section 6.0 "AC/DC Characteristics Timing Requirements for Program/Verify Test Mode"**.

FIGURE 2-4: CONNECTIONS FOR THE ON-CHIP REGULATOR



2.2 Memory Maps

PIC18F97J60 family devices are available in three program memory sizes: 64 Kbytes, 96 Kbytes and 128 Kbytes. The overall memory maps for all devices are shown in Figure 2-5.

For purposes of code protection, the program memory for every device is treated as a single block. Enabling code protection thus protects the entire code memory and not individual segments.

The Configuration Words for these devices are located at addresses 300000h through 300005h. These are implemented as three pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the top four words of the code space (also called the Flash Configuration Words) should be written with configuration data and not executable code. The addresses of the Flash Configuration Words are also listed in Table 2-2. Refer to **Section 5.0 "Configuration Word"** for more information.

Locations 3FFFFEh and 3FFFFFh are reserved for the device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.1 "Device ID Word"**. These device ID bits read out normally, even after code protection.

TABLE 2-2: PROGRAM MEMORY SIZES FOR PIC18F97J60 FAMILY DEVICES

Device	Program Memory (Kbytes)	Location of Flash Configuration Words
PIC18F66J60	64	FFF8h:FFFFh
PIC18F86J60		
PIC18F96J60		
PIC18F66J65	96	17FF8h:17FFFh
PIC18F86J65		
PIC18F96J65		
PIC18F67J60	128	1FFF8h:1FFFFh
PIC18F87J60		
PIC18F97J60		

2.2.1 MEMORY ADDRESS POINTER

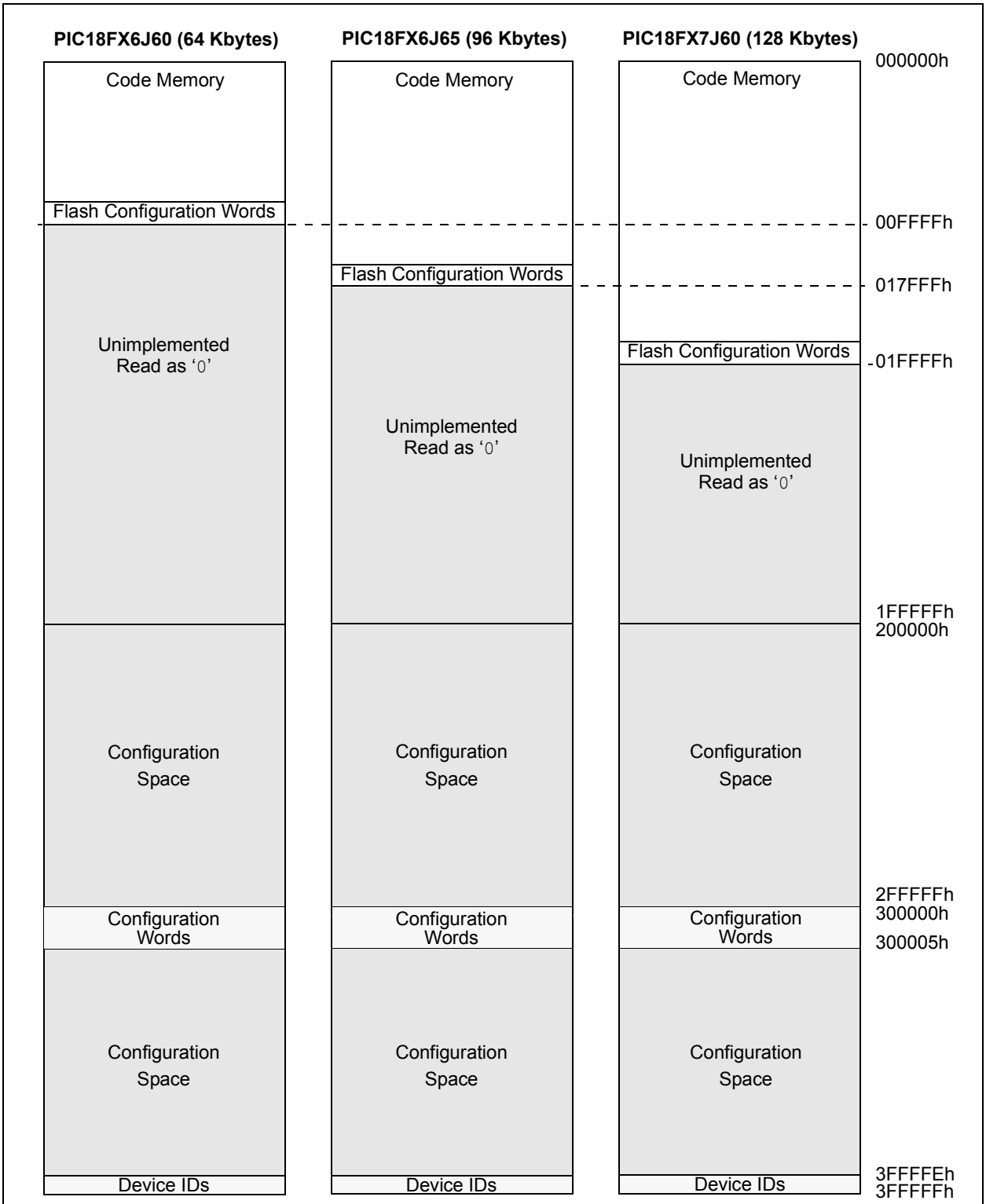
Memory in the device address space (000000h to 3FFFFFh) is addressed via the Table Pointer register, which in turn is comprised of three registers:

- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

FIGURE 2-5: MEMORY MAPS FOR PIC18F97J60 FAMILY DEVICES

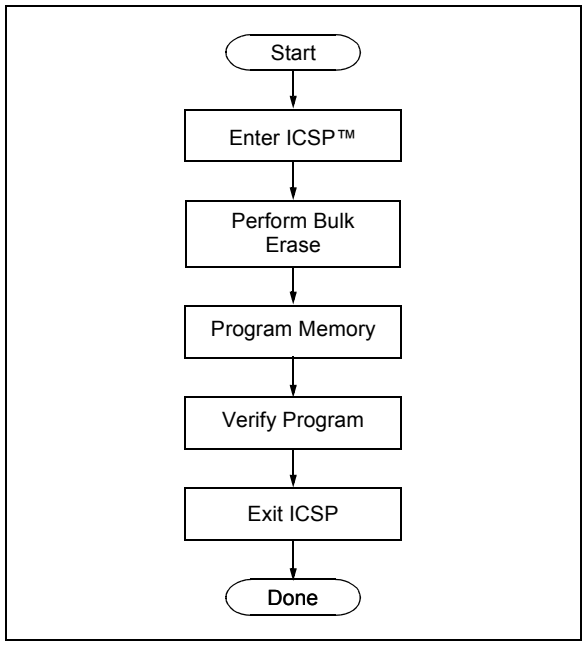


Note: Sizes of memory areas are not to scale. Sizes of accessible memory areas are enhanced to show detail.

2.3 Overview of the Programming Process

Figure 2-6 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory is programmed. Since the only nonvolatile Configuration Words are within the code memory space, they too are programmed as if they were code. Code memory (including the Configuration Words) is then verified to ensure that programming was successful.

FIGURE 2-6: HIGH-LEVEL PROGRAMMING FLOW



2.4 Entering and Exiting ICSP Program/Verify Mode

Entry into ICSP modes for PIC18F97J60 family devices is somewhat different than previous PIC18 devices. As shown in Figure 2-7, entering ICSP Program/Verify mode requires three steps:

1. Voltage is briefly applied to the $\overline{MCLR}$ pin.
2. A 32-bit key sequence is presented on PGD.
3. Voltage is reapplied to $\overline{MCLR}$ within a specific period of time and held.

The programming voltage applied to $\overline{MCLR}$ is V_{IH}, or essentially, V_{DD}. There is no minimum time requirement for holding at V_{IH}. After V_{IH} is removed, an interval of at least P19 must elapse before presenting the key sequence on PGD.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as 4D434850h in hexadecimal). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the most significant nibble must be shifted in first.

Once the key sequence is complete, V_{IH} must be applied to $\overline{MCLR}$ and held at that level for as long as Program/Verify mode is to be maintained. An interval of at least time P20 and P12 must elapse before presenting data on PGD. Signals appearing on PGD before P12 has elapsed will not be interpreted as valid.

On successful entry, the program memory can be accessed and programmed in serial fashion. While in the Program/Verify mode, all unused I/Os are placed in the high-impedance state.

Exiting Program/Verify mode is done by removing V_{IH} from $\overline{MCLR}$, as shown in Figure 2-8. The only requirement for exit is that an interval, P16, should elapse between the last clock and program signals on PGC and PGD before removing V_{IH}.

FIGURE 2-7: ENTERING PROGRAM/VERIFY MODE

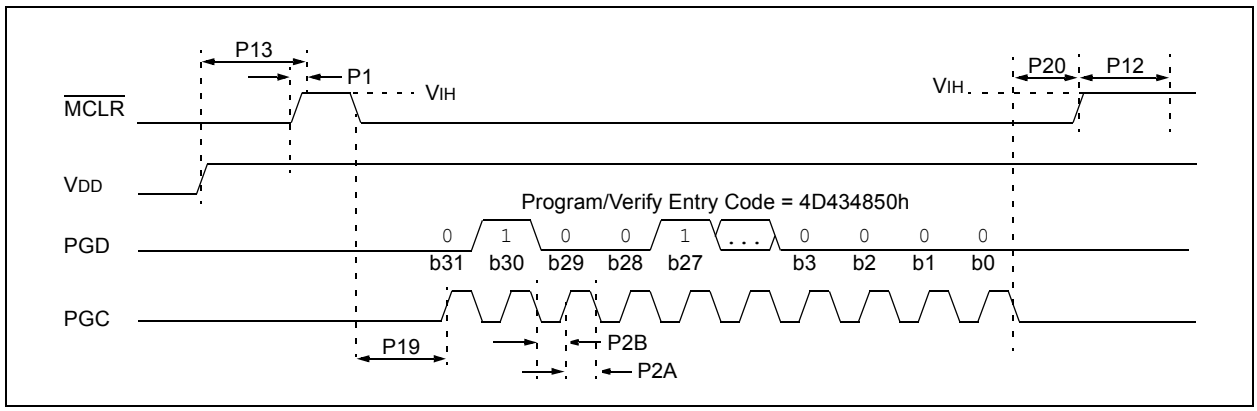
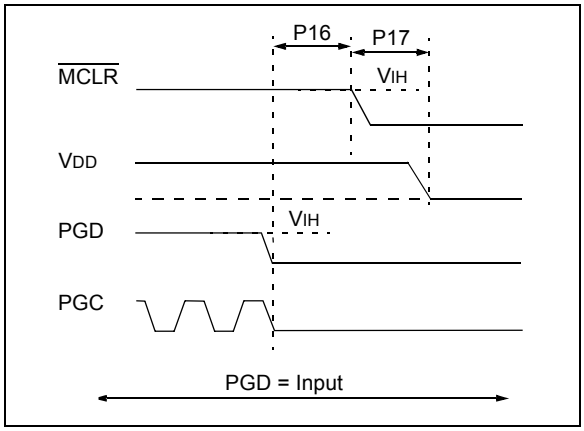


FIGURE 2-8: EXITING PROGRAM/ VERIFY MODE



2.5 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/ output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.5.1 4-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command, followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown Most Significant bit (MSb) first. The command operand, or "Data Payload", is shown <MSB><LSB>. Figure 2-9 demonstrates how to serially present a 20-bit command/operand to the device.

2.5.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

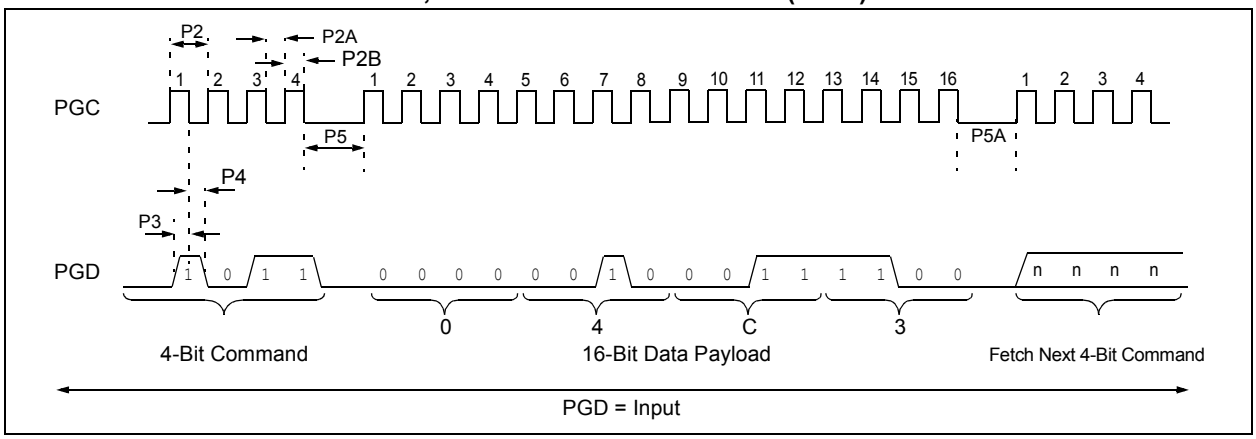
TABLE 2-3: COMMANDS FOR PROGRAMMING

Description	4-Bit Command
Core Instruction (Shift in 16-bit instruction)	0000
Shift Out TABLAT Register	0010
Table Read	1000
Table Read, Post-Increment	1001
Table Read, Post-Decrement	1010
Table Read, Pre-Increment	1011
Table Write	1100
Table Write, Post-Increment by 2	1101
Table Write, Start Programming, Post-Increment by 2	1110
Table Write, Start Programming	1111

TABLE 2-4: SAMPLE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
1101	3C 40	Table Write, post-increment by 2

FIGURE 2-9: TABLE WRITE, POST-INCREMENT TIMING (1101)



3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the memory within the device.

The EECON1 register is used to control write or row erase operations. The WREN bit must be set to enable writes; this must be done prior to initiating a write sequence. It is strongly recommended that the WREN bit only be set immediately prior to a program erase.

The FREE bit must be set in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit.

3.1 ICSP Erase

3.1.1 ICSP BULK ERASE

Devices of the PIC18F97J60 family may be Bulk Erased by writing 0180h to the register pair, 3C0005h:3C0004h. The basic sequence is shown in Figure 3-1 and demonstrated in Table 3-1.

Since the code-protect Configuration bit is stored in the program code within code memory, a Bulk Erase operation will also clear any code-protect settings for the device.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the `NOP` command), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

Note:	A Bulk Erase is the only way to reprogram the code-protect Configuration bit from an ON state to an OFF state.

TABLE 3-1: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	01 01	Write 01h to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	80 80	Write 80h TO 3C0004h to erase entire device.
0000	00 00	NOP
0000	00 00	Hold PGD low until erase completes.

FIGURE 3-1: BULK ERASE FLOW

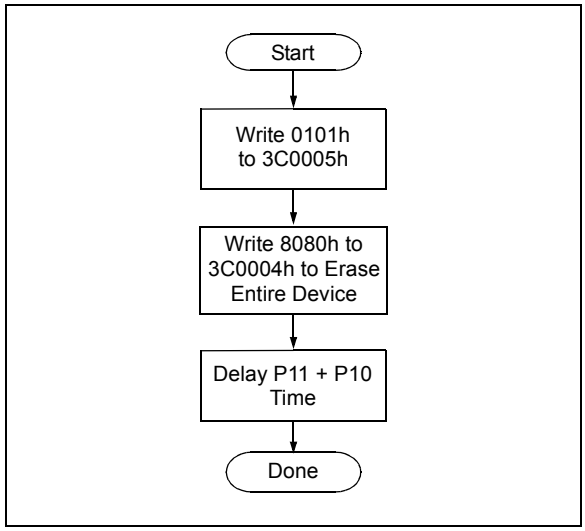
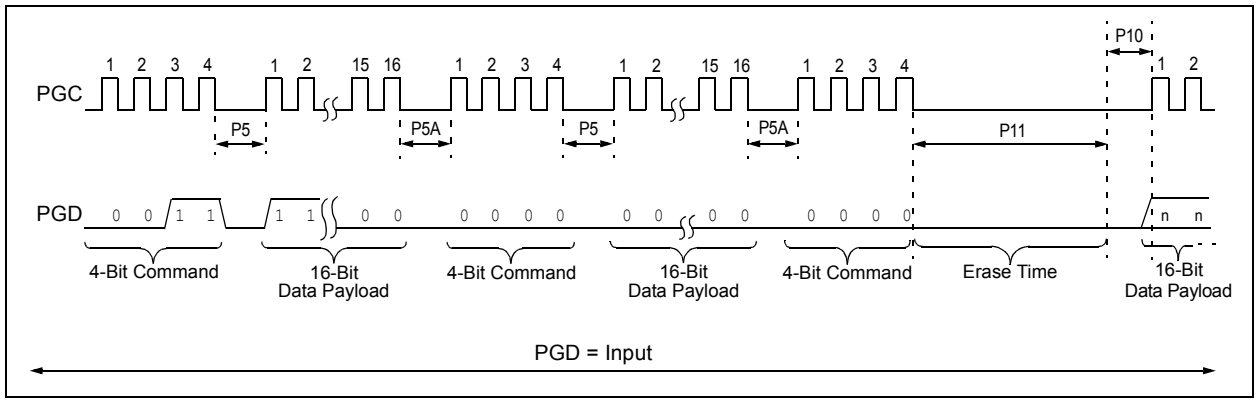


FIGURE 3-2: BULK ERASE TIMING



3.1.2 ICSP ROW ERASE

It is possible to erase a single row (1024 bytes of data), provided the block is not code-protected. Rows are located at static boundaries beginning at program memory address 000000h, extending to the internal program memory limit (see **Section 2.2 "Memory Maps"**).

The Row Erase duration is externally timed and is controlled by PGC. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

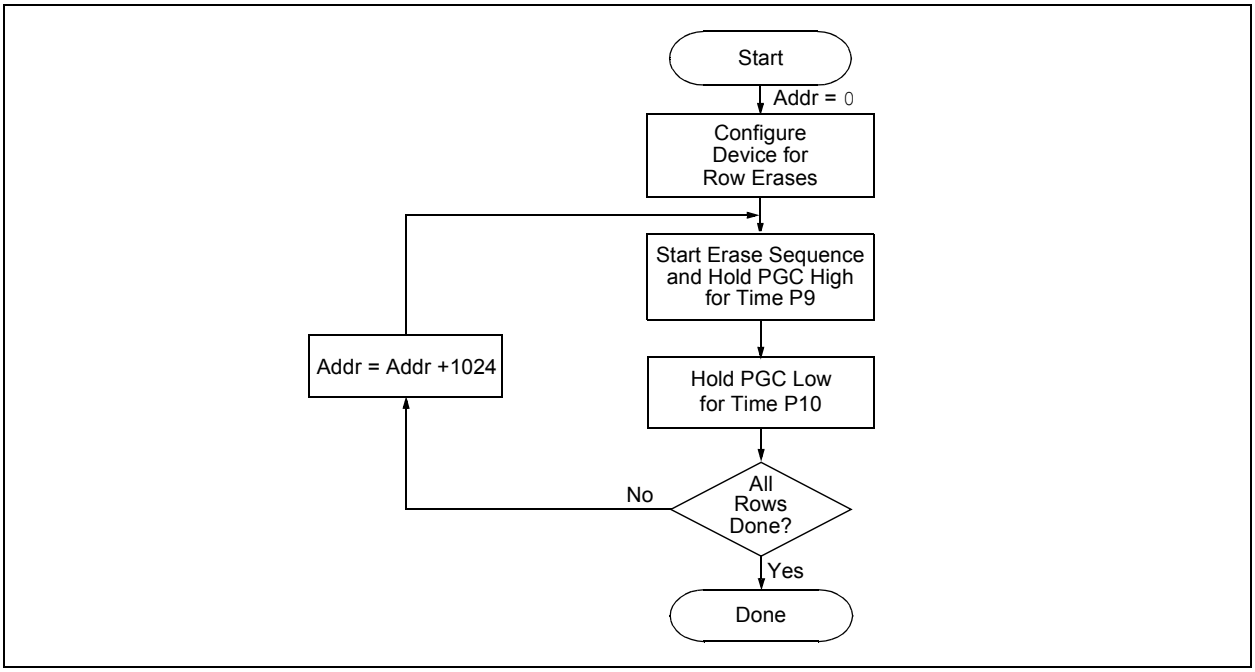
The code sequence to Row Erase a PIC18F97J60 family device is shown in Table 3-2. The flowchart shown in Figure 3-3 depicts the logic necessary to completely erase a PIC18F97J60 family device. The timing diagram that details the "Start Programming" command and parameters P9 and P10 is shown in Figure 3-5.

Note 1:	If the last row of program memory is erased, the FOSC2 Configuration bit should also be programmed as '0'. This ensures the device will be able to start and run using the internal oscillator.
2:	The TBLPTR register can point at any byte within the row intended for erase.

TABLE 3-2: ERASE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable memory writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000 0000 0000	6A F8 6A F7 6A F6	CLRF TBLPTRU CLRF TBLPTRH CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000 0000 0000	88 A6 82 A6 00 00	BSF EECON1, FREE BSF EECON1, WR NOP - hold PGC high for time P9 and low for time P10.
Step 4: Repeat step 3, with Address Pointer incremented by 1024 until all rows are erased.		

FIGURE 3-3: SINGLE ROW ERASE CODE MEMORY FLOW



3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write buffer for all devices in the PIC18F97J60 family is 64 bytes; it can be mapped to any location of the same size beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the proper amount of code memory that contains the Table Pointer.

Write buffer locations are not cleared following a write operation; the buffer retains its data after the write is complete. This means that the buffer must be written with 64 bytes on each operation. If there are locations in the code memory that are to remain empty, the corresponding locations in the buffer must be filled with FFFFh. This avoids rewriting old data from the previous cycle.

The programming duration is externally timed and is controlled by PGC. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to program a PIC18F97J60 family device is shown in Table 3-3. The flowchart shown in Figure 3-4 depicts the logic necessary to completely write a PIC18F97J60 family device. The timing diagram that details the Start Programming command and parameters P9 and P10 is shown in Figure 3-5.

Note 1: To maintain the endurance specification of the Flash program memory cells, each 64-byte block of program memory should never be programmed more than once between erase operations. If any byte within a 64-byte block of program memory is written, that entire block must not be written to again until a Bulk Erase on the part, or a Row Erase on the row containing the modified 64-byte block, has been performed.

2: The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

TABLE 3-3: WRITE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Load write buffer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 3: Repeat for all but the last two bytes. Any unused locations should be filled with FFFFh.		
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
Step 4: Load write buffer for last two bytes.		
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
To continue writing data, repeat steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop.		

FIGURE 3-4: PROGRAM CODE MEMORY FLOW

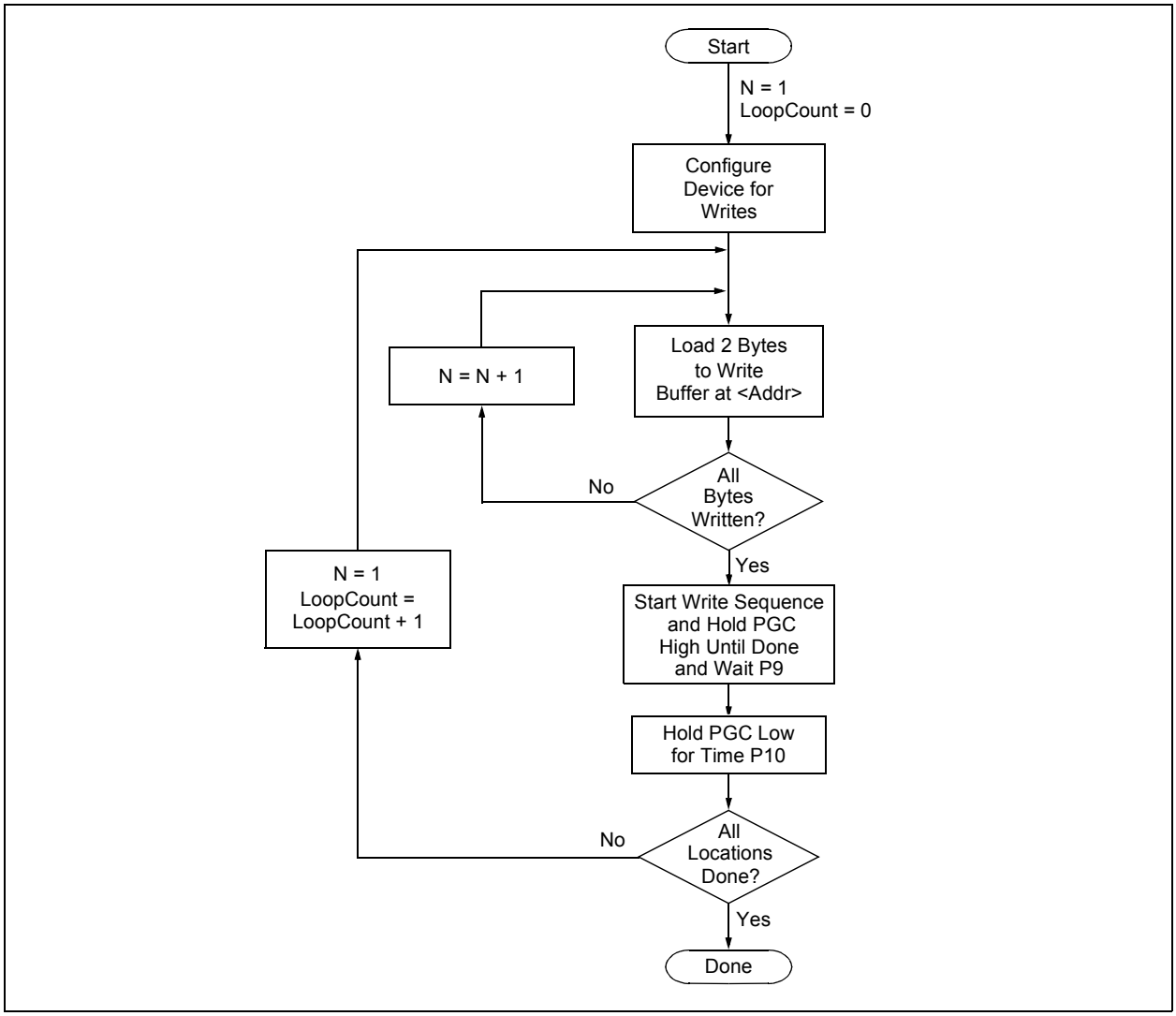
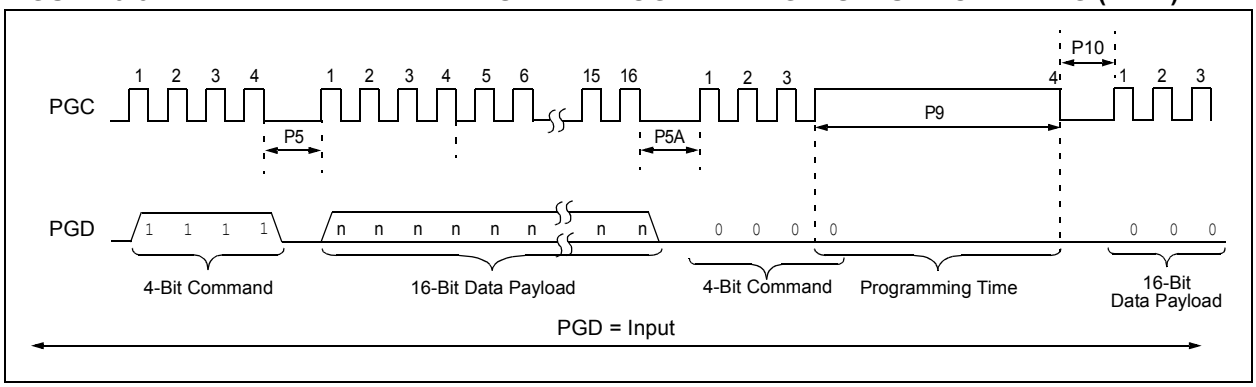


FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming. It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in **Section 4.2 "Verify Code Memory and Configuration Word"**) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data. The code sequence is shown in Table 3-4.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

3.2.2 CONFIGURATION WORD PROGRAMMING

Since the Flash Configuration Words are stored in program memory, they are programmed as if they were program data. Refer to **Section 3.2 "Code Memory Programming"** and **Section 3.2.1 "Modifying Code Memory"** for methods and examples on programming or modifying program memory. See also **Section 5.0 "Configuration Word"** for additional information on the Configuration Words.

TABLE 3-4: MODIFYING CODE MEMORY

4-Bit Command	Data Payload	Core Instruction
Step 1: Set the Table Pointer for the block to be erased.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Enable memory writes and set up an erase.		
0000	84 A6	BSF EECON1, WREN
0000	88 A6	BSF EECON1, FREE
Step 3: Initiate erase.		
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
Step 4: Load write buffer. The correct bytes will be selected based on the Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
.	.	
.	.	Repeat write operation 30 more times to fill the write buffer
.	.	
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
Step 5: Repeat Step 4, for a total of 16 times, to completely rewrite the 1024 bytes of the erase buffer.		
Step 6: To continue modifying data, repeat Steps 1 through 4, where the Address Pointer is incremented by 1024 bytes at each iteration of the loop.		
Step 7: Disable writes.		
0000	94 A6	BCF EECON1, WREN

4.0 READING THE DEVICE

4.1 Read Code Memory

Code memory is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

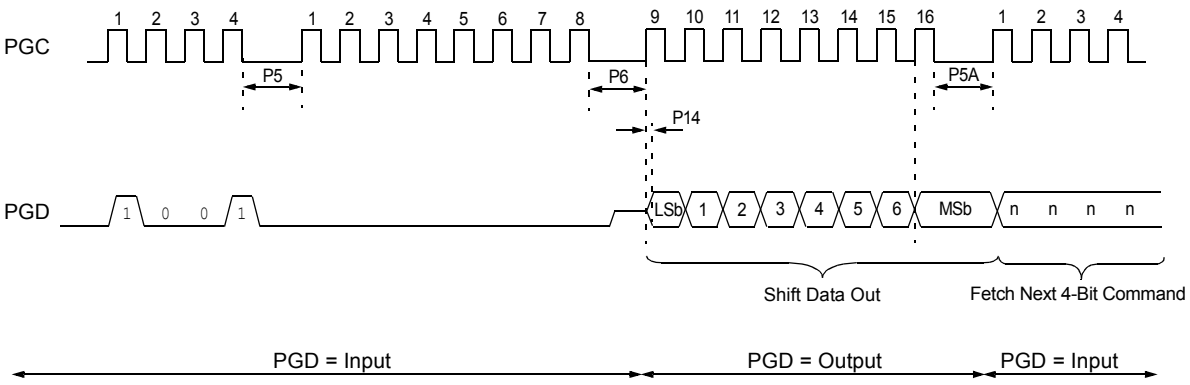
The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to the reading of the Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ, POST-INCREMENT INSTRUCTION TIMING (1001)



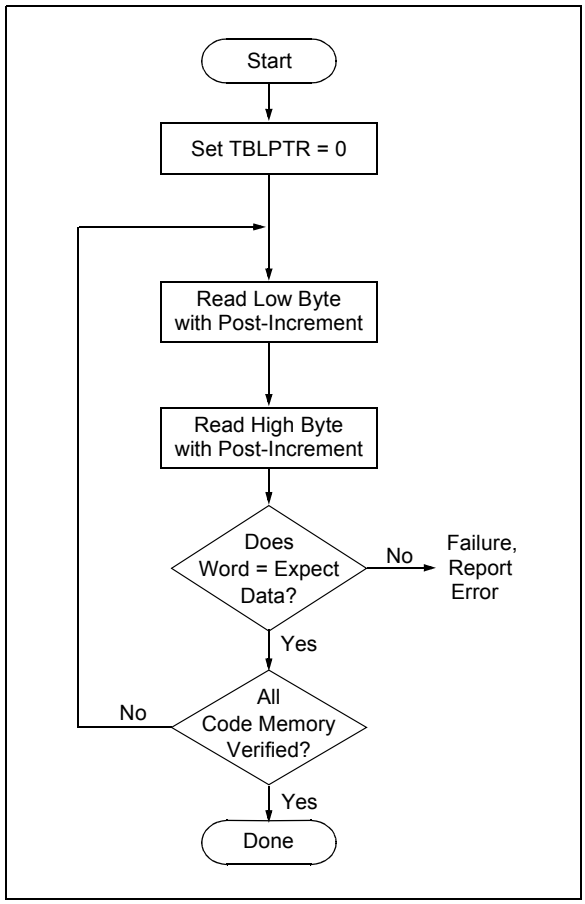
4.2 Verify Code Memory and Configuration Word

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Because the Flash Configuration Words are stored in the top of program memory, it is verified with the rest of the code at this time.

The verify process is shown in the flowchart in Figure 4-2. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory"** for implementation details of reading code memory.

Note:	Because the Flash Configuration Word contains the device code protection bit, code memory should be verified immediately after writing if code protection is enabled. This is because the device will not be readable or verifiable if a device Reset occurs after the Flash Configuration Word (and the CP0 bit) have been cleared.

FIGURE 4-2: VERIFY CODE MEMORY FLOW



4.3 Blank Check

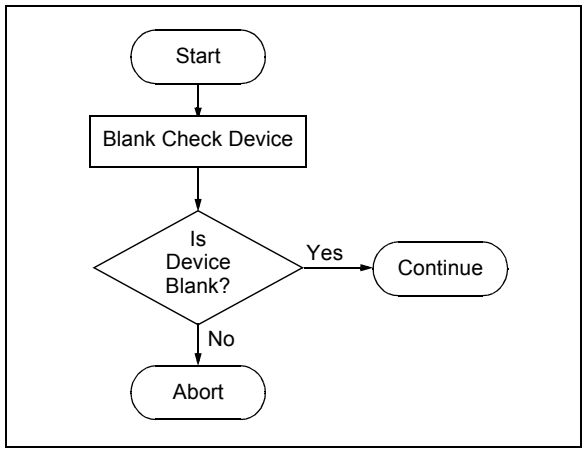
The term "Blank Check" means to verify that the device has no programmed memory cells. All memories must be verified: code memory and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as a '1'. So, Blank Checking a device merely means to verify that all bytes read as FFh. The overall process flow is shown in Figure 4-3.

Note:	Following a device Bulk Erase, the Configuration Words will read as shown in Table 5-2.

Given that Blank Checking is merely code verification with FFh expect data, refer to **Section 4.2 "Verify Code Memory and Configuration Word"** for implementation details.

FIGURE 4-3: BLANK CHECK FLOW



5.0 CONFIGURATION WORD

The Configuration Words of the PIC18F97J60 family devices are implemented as volatile memory registers, as opposed to the programmable nonvolatile memory used in other PIC18 devices. All of the Configuration registers (CONFIG1L, CONFIG1H, CONFIG2L, CONFIG2H, CONFIG3L and CONFIG3H) are automatically loaded following each device Reset.

The data for these registers is taken from the four Flash Configuration Words located at the top of program memory. Configuration data is stored in order, starting with CONFIG1L in the lowest Flash address and ending with CONFIG4H in the highest. The mapping to specific Configuration Words is shown in Table 5-1. While four words are reserved in program memory, only three words (CONFIG1L through CONFIG3H) are used for device configuration. Users should always reserve these locations for Configuration Word data and write their application code accordingly.

The upper four bits of each Configuration Word should always be stored in program memory as '1111'. This is done so these program memory addresses will always be '1111 xxxx xxxx xxxx' and interpreted as a NOP instruction if they were ever to be executed. Because the corresponding bits in the Configuration Word are unimplemented, they will not be written to.

The Configuration and Device ID registers are summarized in Table 5-2. A listing of the individual Configuration bits and their options is provided in Table 5-3.

TABLE 5-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS

Configuration Byte	Code Space Address(1)	Configuration Register Address
CONFIG1L	XXXF8h	300000h
CONFIG1H	XXXF9h	300001h
CONFIG2L	XXXFAh	300002h
CONFIG2H	XXXFBh	300003h
CONFIG3L	XXXFCh	300004h
CONFIG3H	XXXFDh	300005h
CONFIG4L(2)	XXXFEh	300006h
CONFIG4H(2)	XXXFFh	300007h

Note 1: See Table 2-2 for the complete addresses within code space for specific devices and memory sizes.

2: Unimplemented in PIC18F97J60 family devices.

TABLE 5-2: CONFIGURATION BITS AND DEVICE IDS

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	$\overline{\text{DEBUG}}$	XINST	STVREN	—	—	—	—	WDTEN	111- ---1
300001h	CONFIG1H	—(1)	—(1)	—(1)	—(1)	—(2)	CP0	—	—	---- 01--
300002h	CONFIG2L	IESO	FCMEN	—	—	—	FOSC2	FOSC1	FOSC0	11-- -111
300003h	CONFIG2H	—(1)	—(1)	—(1)	—(1)	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300004h	CONFIG3L	WAIT(3)	BW(3)	EMB1(3)	EMB0(3)	EASHFT(3)	—	—	—	1111 1---
300005h	CONFIG3H	—(1)	—(1)	—(1)	—(1)	—	ETHLED	ECCPMX(4)	CCP2MX(4)	---- -111
3FFFFEh	DEVID1(5)	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	See Table 5-4
3FFFFFh	DEVID2(5)	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	See Table 5-4

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.
Shaded cells are unimplemented, read as '0'.

Note 1: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

2: This bit should always be maintained as '0'.

3: Implemented in 100-pin devices only.

4: Implemented in 80-pin and 100-pin devices only. This bit should always be maintained as '1' for 64-pin devices.

5: DEVID registers are read-only and cannot be programmed by the user.

TABLE 5-3: PIC18F97J60 FAMILY BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
$\overline{\text{DEBUG}}$	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)
CP0	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
IESO	CONFIG2L	Internal/External Oscillator Switchover bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
FOSC2	CONFIG2L	Primary Oscillator Select bit 1 = Default primary oscillator on start-up is EC or HS, depending on settings of FOSC1:FOSC0; INTRC selected when OSCCON<1:0> = 11 0 = Default primary oscillator on start-up is INTRC; INTRC also selected when OSCCON<1:0> = 11 or 00
FOSC1:FOSC0	CONFIG2L	Oscillator Selection bits 11 = EC oscillator, PLL enabled and under software control, CLKO function on OSC2 10 = EC oscillator, CLKO function on OSC2 01 = HS oscillator, PLL enabled and under software control 00 = HS oscillator

TABLE 5-3: PIC18F97J60 FAMILY BIT DESCRIPTIONS (CONTINUED)

Bit Name	Configuration Words	Description
WDTPS3:WDTPS0	CONFIG2H	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
WAIT	CONFIG3L	External Bus Wait Enable bit 1 = Wait states for operations on external memory bus disabled 0 = Wait states for operations on external memory bus enabled
BW	CONFIG3L	Data Bus Width Select bit 1 = 16-Bit External Bus mode 0 = 8-Bit External Bus mode
EMB1:EMB0	CONFIG3L	External Memory Bus Configuration bits 11 = Microcontroller mode – external bus disabled 10 = Extended Microcontroller mode,12-Bit Address mode 01 = Extended Microcontroller mode,16-Bit Address mode 00 = Extended Microcontroller mode, 20-Bit Address mode
EASHFT	CONFIG3L	External Address Bus Shift Enable bit 1 = Address shifting enabled; address on external bus is offset to start at 000000h 0 = Address shifting disabled; address on external bus reflects the PC value
ETHLED	CONFIG3H	Ethernet LED Enable bit 1 = RA0/RA1 are multiplexed with LEDA/LEDB when Ethernet module is enabled and function as I/O when Ethernet is disabled 0 = RA0/RA1 function as I/O regardless of Ethernet module status
ECCPMX	CONFIG3H	ECCP MUX bit 1 = ECCP1 outputs (P1B/P1C) are multiplexed with RE6 and RE5; ECCP3 outputs (P3B/P3C) are multiplexed with RE4 and RE3 0 = ECCP1 outputs (P1B/P1C) are multiplexed with RH7 and RH6; ECCP3 outputs (P3B/P3C) are multiplexed with RH5 and RH4
CCP2MX	CONFIG3H	CCP2 MUX bit 1 = ECCP2/P2A is multiplexed with RC1 0 = ECCP2/P2A is multiplexed with RE7 in Microcontroller mode or with RB3 in Extended Microcontroller mode (100-pin devices only)

5.1 Device ID Word

The device ID word for the PIC18F97J60 family devices is located at 3FFFFEh:3FFFFFh. These read-only bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code or read-protected. The process for reading the device IDs is shown in Figure 5-1. A complete list of device ID values for the PIC18F97J60 family is presented in Table 5-4.

FIGURE 5-1: READ DEVICE ID WORD FLOW

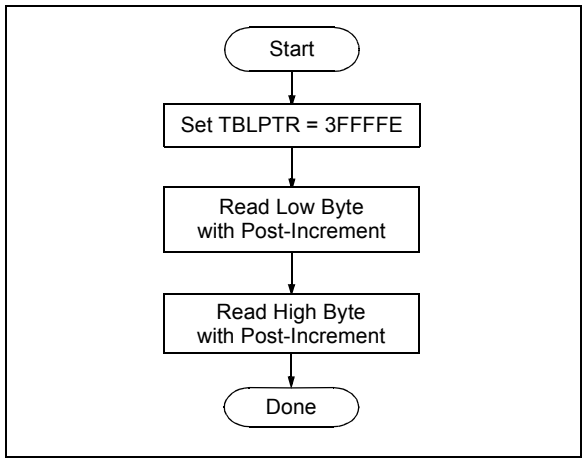


TABLE 5-4: DEVICE ID VALUES

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F66J60	18h	000x xxxx
PIC18F66J65	1Fh	000x xxxx
PIC18F67J60	1Fh	001x xxxx
PIC18F86J60	18h	001x xxxx
PIC18F86J65	1Fh	010x xxxx
PIC18F87J60	1Fh	011x xxxx
PIC18F96J60	18h	010x xxxx
PIC18F96J65	1Fh	100x xxxx
PIC18F97J60	1Fh	101x xxxx

Legend: The 'x's in DEVID1 are reserved for the device revision code.

5.2 Checksum Computation

The checksum is calculated by summing the contents of all code memory locations and the device Configuration Words, appropriately masked. The Least Significant 16 bits of this sum are the checksum.

The checksum calculation differs depending on whether or not code protection is enabled. Since the code memory locations read out differently depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Words can always be read.

Table 5-5 describes how to calculate the checksum for each device.

TABLE 5-5: CHECKSUM COMPUTATION

Device	Code Protection	Checksum
PIC18F66J60	Off	SUM[000000:00FFF7] + ([00FFF8] & E1h) + ([00FFF9] & 0Ch) + ([00FFFA] & C7h) + ([00FFFB] & 0Fh) + ([00FFFD] & 04h)
	On	0000h
PIC18F66J65	Off	SUM[000000:017FF7] + ([00FFF8] & E1h) + ([00FFF9] & 0Ch) + ([00FFFA] & C7h) + ([00FFFB] & 0Fh) + ([00FFFD] & 04h)
	On	0000h
PIC18F67J60	Off	SUM[000000:01FFF7] + ([00FFF8] & E1h) + ([00FFF9] & 0Ch) + ([00FFFA] & C7h) + ([00FFFB] & 0Fh) + ([00FFFD] & 04h)
	On	0000h
PIC18F86J60	Off	SUM[000000:00FFF7] + ([017FF8] & E1h) + ([017FF9] & 0Ch) + ([017FFA] & C7h) + ([017FFB] & 0Fh) + ([017FFD] & 07h)
	On	0000h
PIC18F86J65	Off	SUM[000000:017FF7] + ([017FF8] & E1h) + ([017FF9] & 0Ch) + ([017FFA] & C7h) + ([017FFB] & 0Fh) + ([017FFD] & 07h)
	On	0000h
PIC18F87J60	Off	SUM[000000:01FFF7] + ([017FF8] & E1h) + ([017FF9] & 0Ch) + ([017FFA] & C7h) + ([017FFB] & 0Fh) + ([017FFD] & 07h)
	On	0000h
PIC18F96J60	Off	SUM[000000:00FFF7] + ([01FFF8] & E1h) + ([01FFF9] & 0Ch) + ([01FFFA] & C7h) + ([01FFFB] & 0Fh) + ([01FFFC] & F8h) + ([01FFFD] & 07h)
	On	0000h
PIC18F96J65	Off	SUM[000000:017FF7] + ([01FFF8] & E1h) + ([01FFF9] & 0Ch) + ([01FFFA] & C7h) + ([01FFFB] & 0Fh) + ([01FFFC] & F8h) + ([01FFFD] & 07h)
	On	0000h
PIC18F97J60	Off	SUM[000000:01FFF7] + ([01FFF8] & E1h) + ([01FFF9] & 0Ch) + ([01FFFA] & C7h) + ([01FFFB] & 0Fh) + ([01FFFC] & F8h) + ([01FFFD] & 07h)
	On	0000h

Legend: [a] = Value at address a; SUM[a:b] = Sum of locations a to b inclusive; + = Addition; & = Bitwise AND. All addresses are hexadecimal.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Sym	Characteristic		Min	Max	Units	Conditions
	VDDCORE	External Supply Voltage for Microcontroller Core		2.00	2.70	V	**(Note 1)**
D111	VDD	Supply Voltage During Programming	ENVREG = VSS	VDDCORE	3.60	V	Normal programming **(Note 2)**
			ENVREG = VDD	2.65	3.60		
D112	IPP	Programming Current on $\overline{MCLR}$		—	5	μA	
D113	IDDP	Supply Current During Programming		—	10	mA	
D031	VIL	Input Low Voltage		VSS	0.2 VDD	V	
D041	VIH	Input High Voltage		0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage		—	0.6	V	IOL = 8.5 mA @ 3.6V
D090	VOH	Output High Voltage		VDD – 0.7	—	V	IOH = -3.0 mA @ 3.6V
D012	CIO	Capacitive Loading on I/O pin (PGD)		—	50	pF	To meet AC specifications
	CF	Filter Capacitor Value on VCAP		1	10	μF	Required for controller core operation when voltage regulator is enabled

Note 1: VDDCORE must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 "On-Chip Voltage Regulator"** for more information.

2: VDD must also be supplied to the AVDD pins during programming and to the ENVREG if the on-chip voltage regulator is used. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Sym	Characteristic	Min	Max	Units	Conditions
P1	TR	$\overline{MCLR}$ Rise Time to Enter Program/Verify mode	—	1.0	μs	
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay between 4-bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay between 4-bit Command Operand and Next 4-bit Command	40	—	ns	
P6	TDLY2	Delay between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	2.8	—	ms	
P10	TDLY6	PGC Low Time after Programming	400	—	ns	
P11	TDLY7	Delay to allow Bulk Erase to Occur	400	—	ms	
P12	THLD2	Input Data Hold Time from $\overline{MCLR}$ ↑	400	—	μs	
P13	TSET2	VDD ↑ Setup Time to $\overline{MCLR}$ ↑	100	—	ns	
P14	TVALID	Data Out Valid from PGC ↑	10	—	ns	
P16	TDLY8	Delay between Last PGC ↓ and $\overline{MCLR}$ ↓	0	—	s	
P17	THLD3	$\overline{MCLR}$ ↓ to VDD ↓	—	100	ns	
P19	TKEY1	Delay from First $\overline{MCLR}$ ↓ to First PGC ↑ for Key Sequence on PGD	1	—	ms	
P20	TKEY2	Delay from Last PGC ↓ for Key Sequence on PGD to Second $\overline{MCLR}$ ↑	40	—	ns	

Note 1: VDDCORE must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 "On-Chip Voltage Regulator"** for more information.

2: VDD must also be supplied to the AVDD pins during programming and to the ENVREG if the on-chip voltage regulator is used. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

Trademarks

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
ISO/TS 16949:2002

Microchip received ISO/TS-16949:2002 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona, Gresham, Oregon and Mountain View, California. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

WORLDWIDE SALES AND SERVICE

AMERICAS

Corporate Office
2355 West Chandler Blvd.
Chandler, AZ 85224-6199
Tel: 480-792-7200
Fax: 480-792-7277
Technical Support:
http://support.microchip.com
Web Address:
www.microchip.com

Atlanta
Duluth, GA
Tel: 678-957-9614
Fax: 678-957-1455

Boston
Westborough, MA
Tel: 774-760-0087
Fax: 774-760-0088

Chicago
Itasca, IL
Tel: 630-285-0071
Fax: 630-285-0075

Dallas
Addison, TX
Tel: 972-818-7423
Fax: 972-818-2924

Detroit
Farmington Hills, MI
Tel: 248-538-2250
Fax: 248-538-2260

Kokomo
Kokomo, IN
Tel: 765-864-8360
Fax: 765-864-8387

Los Angeles
Mission Viejo, CA
Tel: 949-462-9523
Fax: 949-462-9608

Santa Clara
Santa Clara, CA
Tel: 408-961-6444
Fax: 408-961-6445

Toronto
Mississauga, Ontario,
Canada
Tel: 905-673-0699
Fax: 905-673-6509

ASIA/PACIFIC

Asia Pacific Office
Suites 3707-14, 37th Floor
Tower 6, The Gateway
Habour City, Kowloon
Hong Kong
Tel: 852-2401-1200
Fax: 852-2401-3431

Australia - Sydney
Tel: 61-2-9868-6733
Fax: 61-2-9868-6755

China - Beijing
Tel: 86-10-8528-2100
Fax: 86-10-8528-2104

China - Chengdu
Tel: 86-28-8665-5511
Fax: 86-28-8665-7889

China - Fuzhou
Tel: 86-591-8750-3506
Fax: 86-591-8750-3521

China - Hong Kong SAR
Tel: 852-2401-1200
Fax: 852-2401-3431

China - Qingdao
Tel: 86-532-8502-7355
Fax: 86-532-8502-7205

China - Shanghai
Tel: 86-21-5407-5533
Fax: 86-21-5407-5066

China - Shenyang
Tel: 86-24-2334-2829
Fax: 86-24-2334-2393

China - Shenzhen
Tel: 86-755-8203-2660
Fax: 86-755-8203-1760

China - Shunde
Tel: 86-757-2839-5507
Fax: 86-757-2839-5571

China - Wuhan
Tel: 86-27-5980-5300
Fax: 86-27-5980-5118

China - Xian
Tel: 86-29-8833-7250
Fax: 86-29-8833-7256

ASIA/PACIFIC

India - Bangalore
Tel: 91-80-4182-8400
Fax: 91-80-4182-8422

India - New Delhi
Tel: 91-11-4160-8631
Fax: 91-11-4160-8632

India - Pune
Tel: 91-20-2566-1512
Fax: 91-20-2566-1513

Japan - Yokohama
Tel: 81-45-471- 6166
Fax: 81-45-471-6122

Korea - Gumi
Tel: 82-54-473-4301
Fax: 82-54-473-4302

Korea - Seoul
Tel: 82-2-554-7200
Fax: 82-2-558-5932 or
82-2-558-5934

Malaysia - Penang
Tel: 60-4-646-8870
Fax: 60-4-646-5086

Philippines - Manila
Tel: 63-2-634-9065
Fax: 63-2-634-9069

Singapore
Tel: 65-6334-8870
Fax: 65-6334-8850

Taiwan - Hsin Chu
Tel: 886-3-572-9526
Fax: 886-3-572-6459

Taiwan - Kaohsiung
Tel: 886-7-536-4818
Fax: 886-7-536-4803

Taiwan - Taipei
Tel: 886-2-2500-6610
Fax: 886-2-2508-0102

Thailand - Bangkok
Tel: 66-2-694-1351
Fax: 66-2-694-1350

EUROPE

Austria - Wels
Tel: 43-7242-2244-39
Fax: 43-7242-2244-393

Denmark - Copenhagen
Tel: 45-4450-2828
Fax: 45-4485-2829

France - Paris
Tel: 33-1-69-53-63-20
Fax: 33-1-69-30-90-79

Germany - Munich
Tel: 49-89-627-144-0
Fax: 49-89-627-144-44

Italy - Milan
Tel: 39-0331-742611
Fax: 39-0331-466781

Netherlands - Drunen
Tel: 31-416-690399
Fax: 31-416-690340

Spain - Madrid
Tel: 34-91-708-08-90
Fax: 34-91-708-08-91

UK - Wokingham
Tel: 44-118-921-5869
Fax: 44-118-921-5820

12/08/06