PIC16F72X Memory Programming Specification

This document includes the programming specifications for the following devices:

- PIC16F722
- PIC16F723
- PIC16F724
- PIC16F726
- PIC16F727
- PIC16LF722
- PIC16LF723
- PIC16LF724
- PIC16LF726
- PIC16LF727

1.0 OVERVIEW

The PIC16F72X and PIC16LF72X devices are programmed using In-Circuit Serial Programming™ (ICSP™). This programming specification applies to the PIC16F72X and PIC16LF72X devices in all packages.

The PIC16F72X devices operate from 1.8 to 5.5 volts and the PIC16LF72X devices operate from 1.8 to 3.6 volts. All other aspects of the PIC16F72X with regards to the PIC16LF72X devices are identical.

1.1 Hardware Requirements

PIC16F72X and PIC16LF72X devices require one power supply for VDD and one for VPP. (See **Section 8.0 "Electrical Specifications"** for more details.)

1.2 Pin Utilization

Five pins are needed for ICSP™ programming. The pins are listed in Table 1-1.

TABLE 1-1: PIN DESCRIPTIONS DURING PROGRAMMING

Pin Name	During Programming		
	Function	Pin Type	Pin Description
RB6	ICSPCLK	I	Clock Input – Schmitt Trigger Input
RB7	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}$/VPP	Program/Verify mode	P(1)	Program Mode Select/Programming power supply
VDD	VDD	P	Power Supply
VSS	VSS	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: To activate the Program/Verify mode, high voltage needs to be applied to $\overline{MCLR}$/VPP input. Since the $\overline{MCLR}$ /VPP is used to provide high voltage during programming, the programmer must be able to supply current on this pin.

2.0 DEVICE PINOUTS

The pin diagrams for the PIC16F72X/PIC16LF72X family are shown in Figure 2-1 through Figure 2-5. The pins that are required for programming are listed in Table 1-1 and shown in bold lettering in the pin diagrams.

FIGURE 2-1: 28-PIN PDIP/SOIC/SSOP DIAGRAM FOR PIC16F722/723/726 AND PIC16LF722/723/726

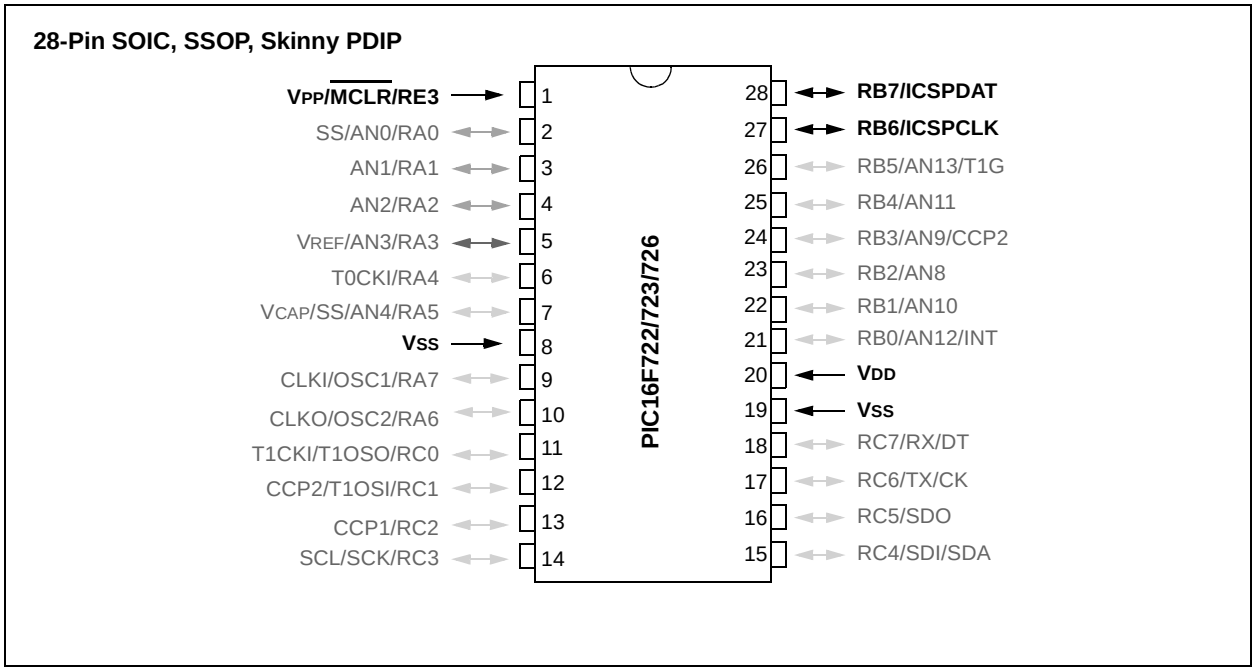


FIGURE 2-2: 28-PIN QFN PACKAGE DIAGRAM FOR PIC16F722/723/726 AND PIC16LF722/723/726

28-Pin QFN

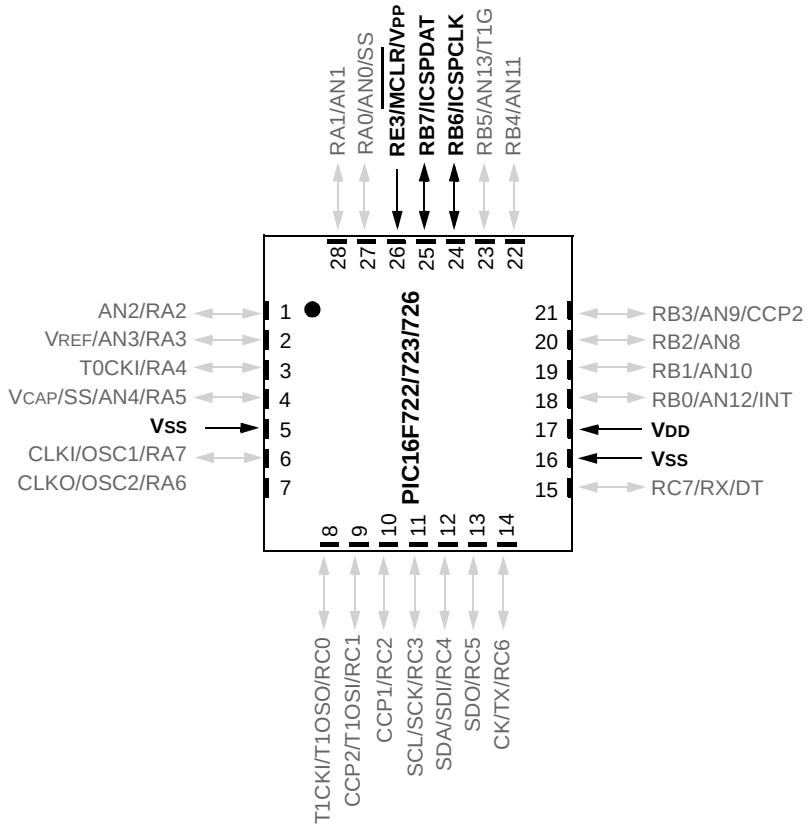


FIGURE 2-3: 40-PIN PDIP PACKAGE DIAGRAM FOR PIC16F724/727 AND PIC16LF724/727

40-Pin PDIP

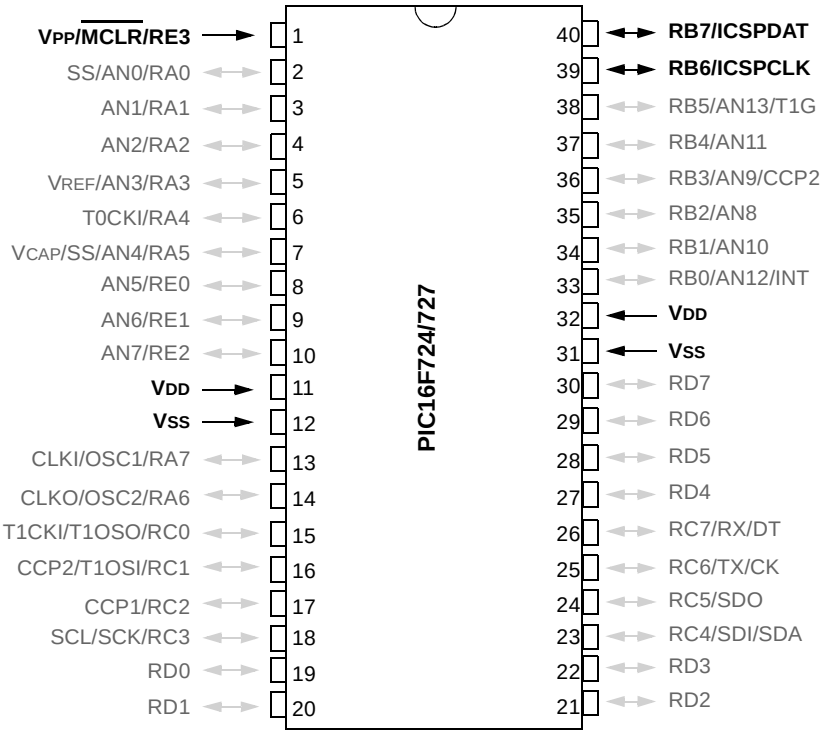


FIGURE 2-4: 44-PIN QFN PACKAGE DIAGRAM FOR PIC16F724/727 AND PIC16LF724/727

44-Pin QFN

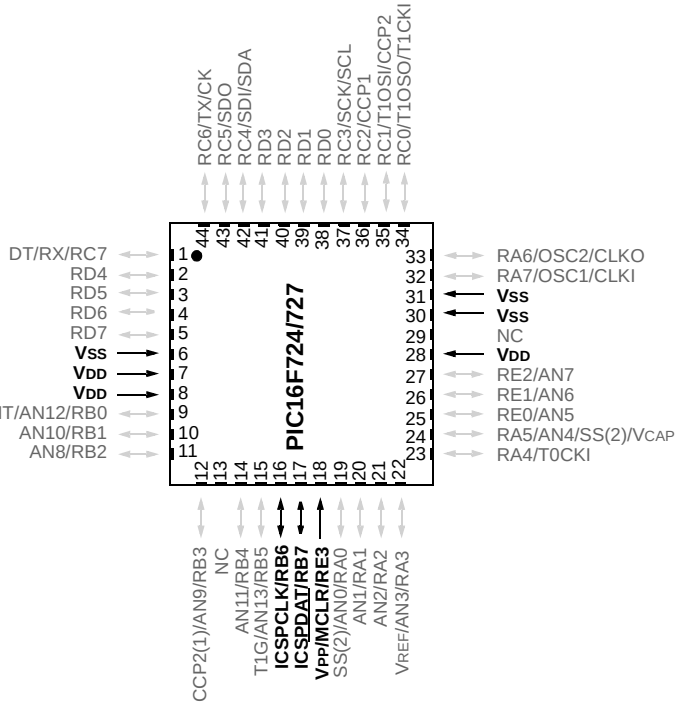
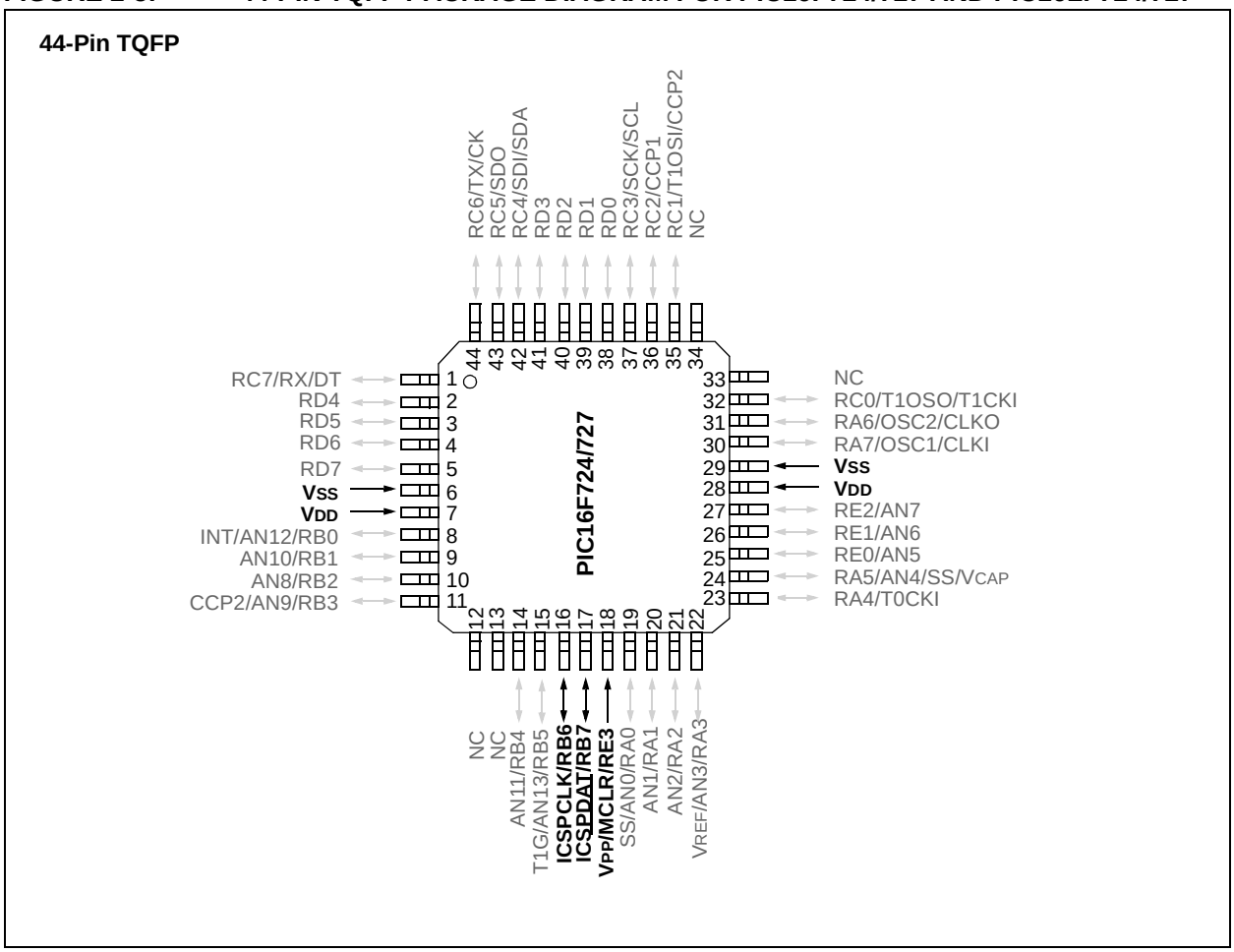


FIGURE 2-5: 44-PIN TQFP PACKAGE DIAGRAM FOR PIC16F724/727 AND PIC16LF724/727



3.0 MEMORY MAP

The memory for the PIC16F72X/PIC16LF72X devices is broken into two sections: program memory and configuration memory. Only the size of the program memory changes between devices; the configuration memory remains the same.

FIGURE 3-1: PIC16F722/PIC16LF722 PROGRAM MEMORY MAPPING

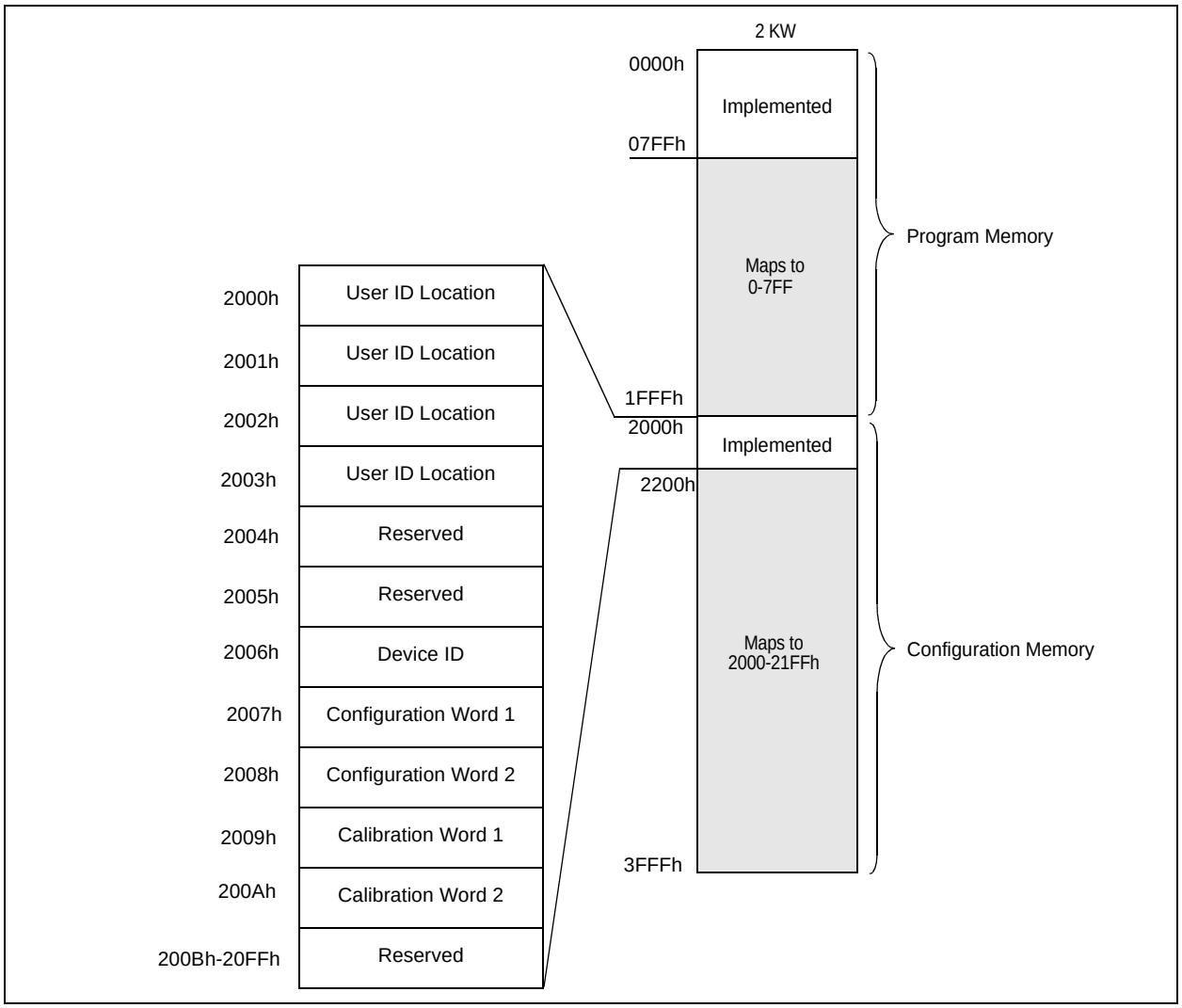


FIGURE 3-2: PIC16F723/PIC16F724/PIC16LF723/PIC16LF724 PROGRAM MEMORY MAPPING

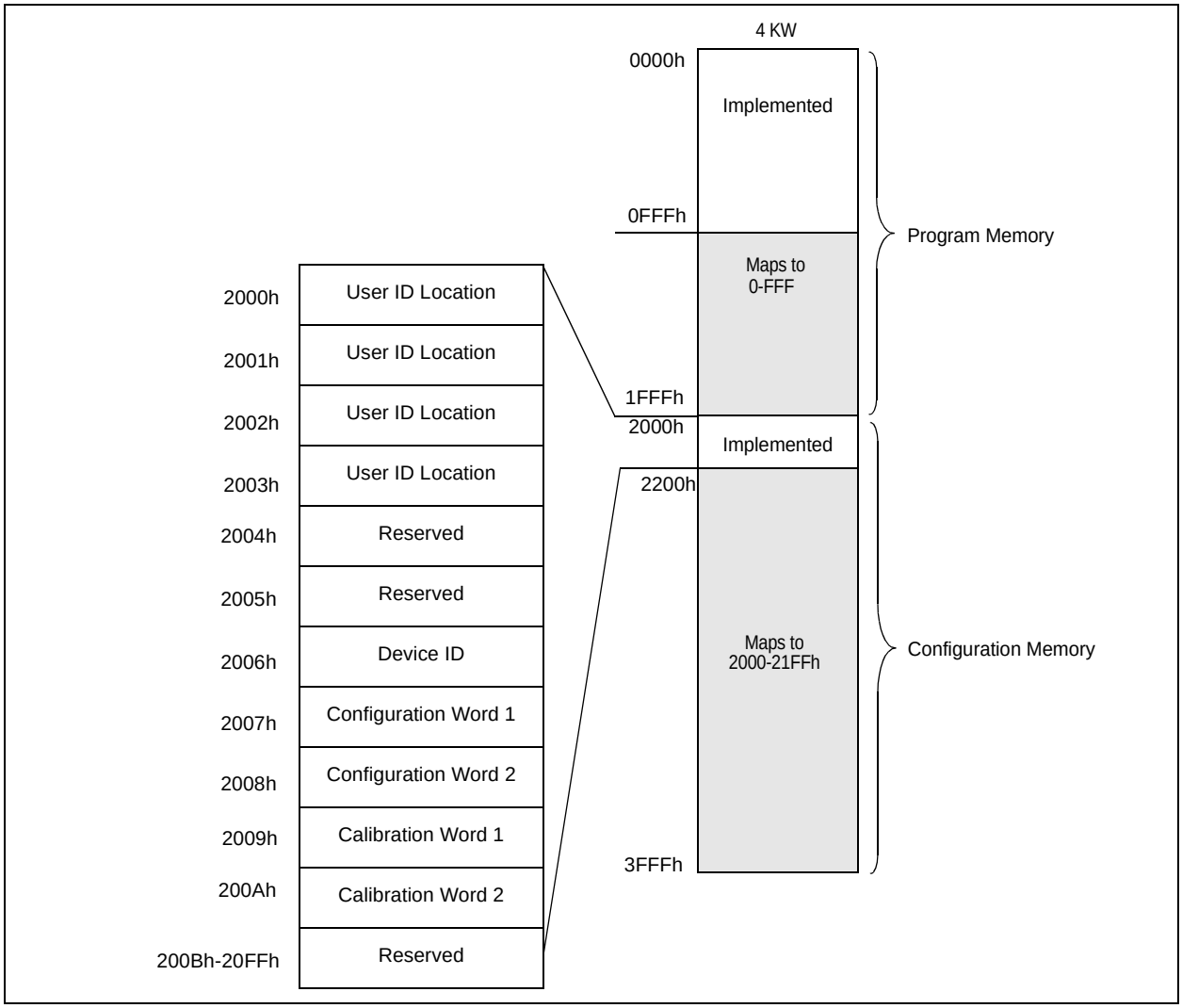
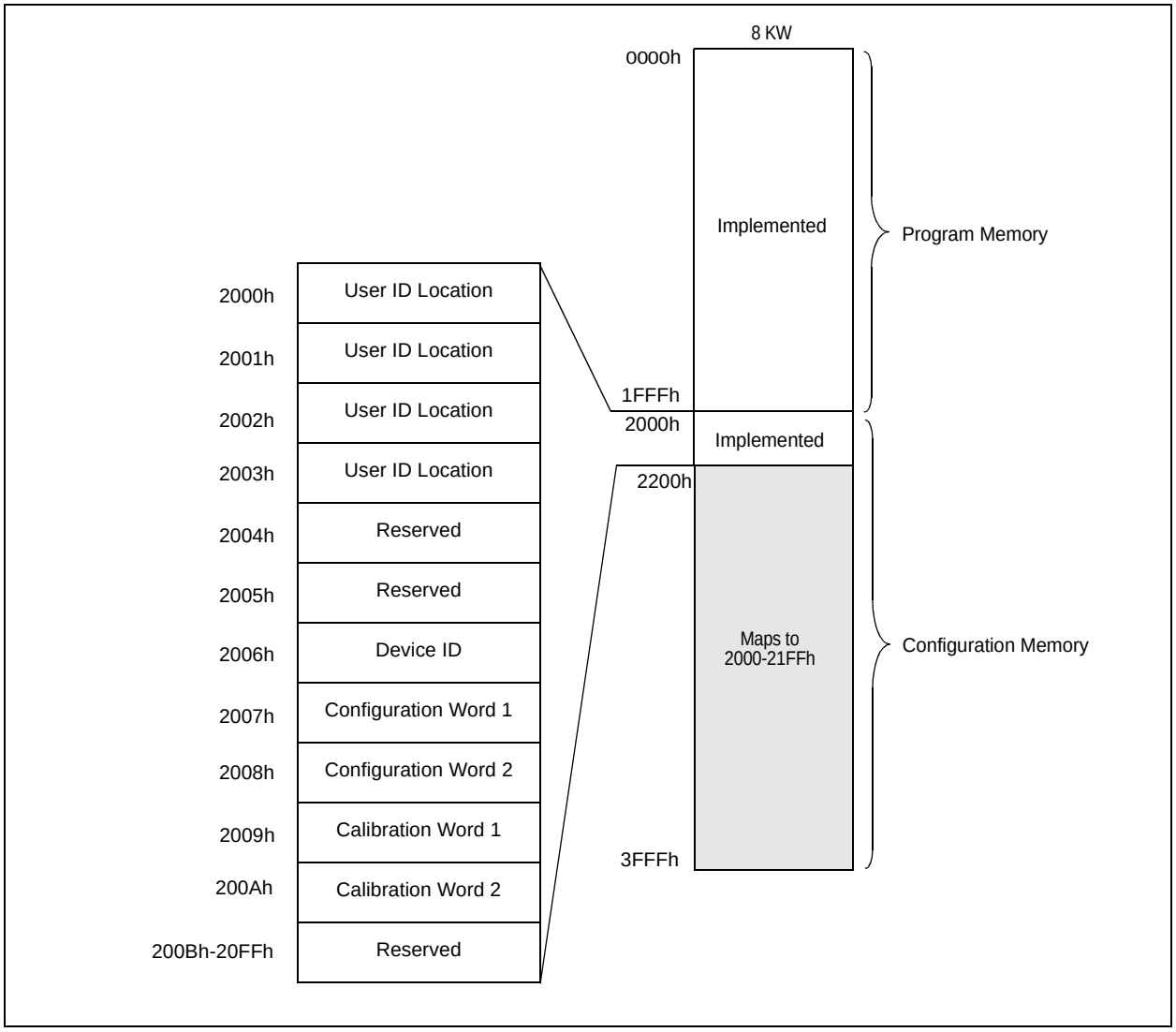


FIGURE 3-3: PIC16F726/PIC16F727/PIC16LF726/PIC16LF727 PROGRAM MEMORY MAPPING



3.1 User ID Location

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped to 2000h-2003h. Each location is 14 bits in length. Code protection has no effect on these memory locations. Each location may be read with code protection enabled or disabled.

Note:	MPLAB® IDE only displays the 7 Least Significant bits (LSb) of each user ID location, the upper bits are not read. It is recommended that only the 7 LSb's be used if MPLAB IDE is the primary tool used to read these addresses.

3.2 Device ID

The device ID word for the PIC16F72X and the PIC16LF72X is located at 2006h. This location can not be erased or modified.

TABLE 3-1: DEVICE ID VALUES

DEVICE	DEVICE ID VALUES	
	DEV	REV
PIC16F722	01 1000 100	x xxxx
PIC16F723	01 1000 011	x xxxx
PIC16F724	01 1000 010	x xxxx
PIC16F726	01 1000 001	x xxxx
PIC16F727	01 1000 000	x xxxx
PIC16LF722	01 1001 100	x xxxx
PIC16LF723	01 1001 011	x xxxx
PIC16LF724	01 1001 010	x xxxx
PIC16LF726	01 1001 001	x xxxx
PIC16LF727	01 1001 000	x xxxx

3.3 Configuration Words

The PIC16F72X/PIC16LF72X has two Configuration Words, Configuration Word 1 (2007h) and Configuration Word 2 (2008h). The individual bits within these Configuration Words are used to enable or disable device functions such as the Brown-out Reset, code protection and Power-up Timer.

3.4 Calibration Words

For the PIC16F72X/PIC16LF72X devices, the 16 MHz internal oscillator (INTOSC), and the Brown-out reset (BOR), are factory calibrated and stored in Calibration Words 1 and 2 (2009h and 200Ah).

The Calibration Words do not participate in erase operations. The device can be erased without affecting the Calibration Words.

REGISTER 3-1: CONFIGURATION WORD 1

R/P-1	R/P-1	U-1	R/P-1	R/P-1	R/P-1	U-1
$\overline{\text{DEBUG}}$(1)	PLLEN	—	BORV	BOREN1	BOREN0	—
bit 13						

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
$\overline{\text{CP}}$	MCLRE	$\overline{\text{PWRTE}}$	WDTE	FOSC2	FOSC1	FOSC0
						bit 0

Legend:	P = Programmable	x = Bit is unknown
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’
-n = Default value	‘1’ = Bit is written to ‘1’	‘0’ = Bit is written to ‘0’

bit 13 **$\overline{\text{DEBUG}}$:** Debugger Mode bit(1)
- 1 = Background debugger is disabled
- 0 = Background debugger is enabled

bit 12 **PLLEN:** INTOSC PLL Enable bit
- 1 = INTOSC frequency is 16 MHz
- 0 = INTOSC frequency is 500 kHz

bit 11 **Unimplemented:** Read as ‘1’

bit 10 **BORV:** Brown-out Reset Voltage Selection bit
- 1 = Brown-out Reset Voltage (V_{BOR}) set to 1.9V
- 0 = Brown-out Reset Voltage (V_{BOR}) set to 2.5V

bit 9-8 **BOREN<1:0>:** Brown-out Reset Enable bits
- 0x = Brown-out Reset disabled
- 10 = Brown-out Reset enabled during operation and disabled in Sleep
- 11 = Brown-out Reset enabled

bit 7 **Unimplemented:** Read as ‘1’

bit 6 **$\overline{\text{CP}}$:** Flash Program Memory Code Protection bit

For PIC16F726/727:
- 0 = 0000h to 1FFFh code protection on
- 1 = Code protection off

For PIC16F723/724:
- 0 = 0000h to 0FFFh code protection on
- 1 = Code protection off

For PIC16F722:
- 0 = 0000h to 07FFh code protection on
- 1 = Code protection off

bit 5 **MCLRE:** RE3/$\overline{\text{MCLR}}$/V_{PP} Pin Function Select bit
- 1 = RE3/$\overline{\text{MCLR}}$/V_{PP} pin function is $\overline{\text{MCLR}}$; Weak pull-up enabled.
- 0 = RE3/$\overline{\text{MCLR}}$/V_{PP} pin function is digital input; $\overline{\text{MCLR}}$ internally disabled; Weak pull-up disabled.

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit
- 1 = PWRT disabled
- 0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
- 1 = WDT enabled
- 0 = WDT disabled

Note 1: $\overline{\text{DEBUG}}$ bit is ignored when code-protect is enabled ($\overline{\text{CP}}$ = 0)

REGISTER 3-1: CONFIGURATION WORD 1 (CONTINUED)

bit 2-0 **FOSC<2:0>:** Oscillator Selection bits

111 = RC with CLKOUT oscillator: CLKO function on RA6/OSC2/CLKO pin, RC on RA7/OSC1/CLKI
110 = RC NO CLKOUT oscillator: I/O function on RA6/OSC2/CLKO pin, RC on RA7/OSC1/CLKI
101 = INTOSC with CLKOUT oscillator: CLKO function on RA6/OSC2/CLKO pin, I/O function on RA7/OSC1/CLKI
100 = INTOSC NO CLKOUT oscillator: I/O function on RA6/OSC2/CLKO pin, I/O function on RA7/OSC1/CLKI
011 = EC oscillator: I/O function on RA6/OSC2/CLKO pin, CLKI on RA7/OSC1/CLKI
010 = HS oscillator: High-speed crystal/resonator on RA6/OSC2/CLKO pin and RA7/OSC1/CLKI
001 = XT oscillator: Crystal/resonator on RA6/OSC2/CLKO pin and RA7/OSC1/CLKI
000 = LP oscillator: Low-power crystal on RA6/OSC2/CLKO pin and RA7/OSC1/CLKI

Note 1: $\overline{\text{DEBUG}}$ bit is ignored when code-protect is enabled ($\overline{\text{CP}}$ = 0)

REGISTER 3-2: CONFIGURATION WORD 2

U-1	U-1	U-1	U-1	U-1	U-1	U-1
—	—	—	—	—	—	—
bit 13						

U-1	R/P-1	R/P-1	U-1	U-1	U-1	U-1
—	VCAPEN1	VCAPEN0	—	—	—	—
						bit 0

Legend:	P = Programmable	x = Bit is unknown
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘1’
-n = Default value	‘1’ = Bit is written to ‘1’	‘0’ = Bit is written to ‘0’

bit 13-6 **Unimplemented:** Read as ‘1’

bit 5-4 **VCAPEN<1:0>:** Voltage Regulator Capacitor Enable bits

For PIC16LF72X:
These bits are ignored. All VCAP pin functions are disabled.

For PIC16F72X:
00 = VCAP functionality is enabled on RA0
01 = VCAP functionality is enabled on RA5
10 = VCAP functionality is enabled on RA6
11 = All VCAP pin functions are disabled

bit 3-0 **Unimplemented:** Read as ‘1’

4.0 PROGRAM/VERIFY MODE

In Program/Verify mode, the program memory and the configuration memory can be accessed and programmed in serial fashion. ICSPDAT and ICSPCLK are used for the data and the clock, respectively. All commands and data words are transmitted LSb first. Data changes on the rising edge of the ICSPCLK and latched on the falling edge. In Program/Verify mode both the ISCPDAT and ICSPCLK are Schmitt Trigger inputs. The sequence that enters the device into Program/Verify mode places all other logic into the Reset state. Upon entering Program/Verify mode, all I/O's are automatically configured as high-impedance inputs and the Program Counter (PC) is cleared.

4.1 Program/Verify Mode Entry and Exit

There are 2 different methods of entering Program/Verify mode:

- VPP – First entry mode
- VDD – First entry mode

4.1.1 VPP – FIRST ENTRY MODE

To enter Program/Verify mode via the VPP-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low. All other pins should be unpowered.
2. Raise the voltage on $\overline{\text{MCLR}}$ from 0V to VIHH.
3. Raise the voltage on VDD from 0V to the desired operating voltage.

The VPP-first entry prevents the device from executing code prior to entering Program/Verify mode (e.g., When the Configuration Word has $\overline{\text{MCLR}}$ disabled (MCLRE = 0), the power-up time disabled ($\overline{\text{PWRTE}}$ = 0), and the internal oscillator is selected (FOSC = 10x), VPP-first entry mode is strongly recommended for this reason. ICSPCLK or ICSPDAT is driven high by the user code. See the timing diagram in Figure 8-4.

4.1.2 VDD–FIRST ENTRY MODE

To enter Program/Verify mode via the VDD-first method the following sequence must be followed:

1. Hold ICSPCLK and ICSPDAT low.
2. Raise the voltage on VDD from 0V to the desired operating voltage.
3. Raise the voltage on $\overline{\text{MCLR}}$ from below VDD to VPP.

The VDD-first method is useful when programming the device when VDD is already applied, for it is not necessary to disconnect VDD to enter Program/Verify mode. See the timing diagram in Figure 8-5.

4.1.3 PROGRAM/VERIFY MODE EXIT

To exit Program/Verify mode take $\overline{\text{MCLR}}$ to VDD or lower.

4.2 Program/Verify Commands

The PIC16F72X and PIC16LF72X implement 10 programming commands, each six bits in length. The commands are summarized in Table 4-1.

Commands that have data associated with them are specified to have a minimum delay of T_{DLY} between the command and the data. After this delay 16 clocks are required to either clock in or clock out the 14-bit data word. The first clock is for the Start bit and the last clock is for the Stop bit.

TABLE 4-1: COMMAND MAPPING FOR PIC16F72X

Command	Mapping							Data/Note
	Binary (MSb … LSb)						Hex	
Load Configuration	x	0	0	0	0	0	00h	0, data (14), 0
Load Data For Program Memory	x	0	0	0	1	0	02h	0, data (14), 0
Read Data From Program Memory	x	0	0	1	0	0	04h	0, data (14), 0
Increment Address	x	0	0	1	1	0	06h	
Reset Address	x	1	0	1	1	0	16h	
Begin Internally Timed Programming	x	0	1	0	0	0	08h	
Begin Externally Timed Programming	x	1	1	0	0	0	18h	
End Externally Timed Programming	x	0	1	0	1	0	0Ah	
Bulk Erase Program Memory	x	0	1	0	0	1	09h	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	11h	Internally Timed

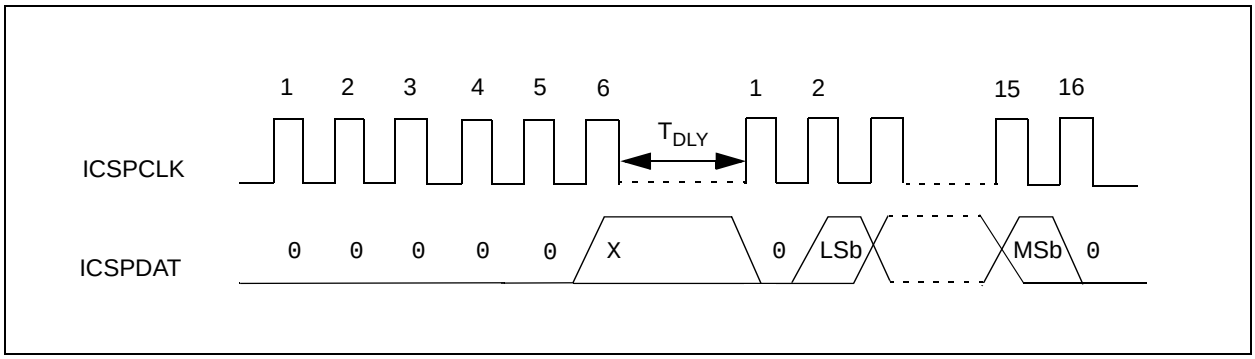
4.2.1 LOAD CONFIGURATION

The Load Configuration command is used to access the configuration memory (User ID Locations, Configuration Words, Calibration Words). The Load Configuration command sets the Program Counter (PC) to address 2000h and loads the data latches with one word of data.

After issuing the Load Configuration command, use the Increment Address command until the proper address to be programmed is reached. The address is then programmed by issuing either the Begin Internally Timed Programming or Begin Externally Timed Programming command.

After the configuration memory has been accessed by the Load Configuration command, the only way to get back to the program memory is to exit Program/Verify mode or issue the Reset Address command.

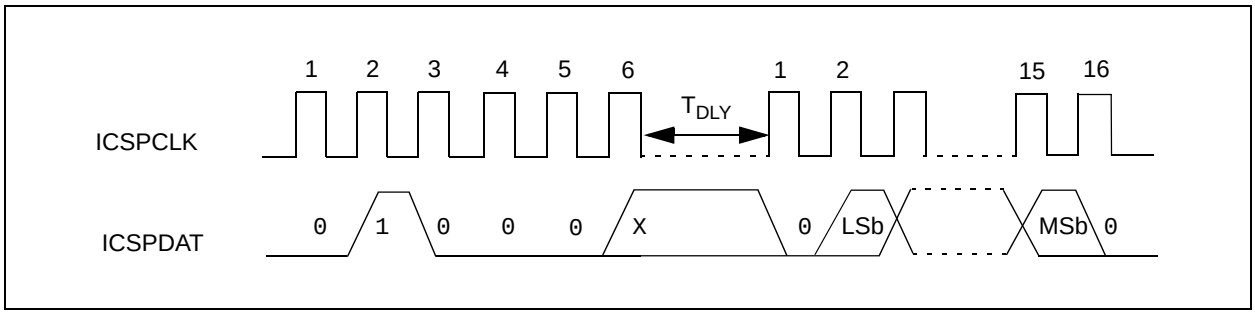
FIGURE 4-1: LOAD CONFIGURATION



4.2.2 LOAD DATA FOR PROGRAM MEMORY

The Load Data for Program Memory command is used to load one 14-bit word into the data latches. The word in placed into program memory after the Begin Internally Timed Programming or Begin Externally Timed Programming command is isssued.

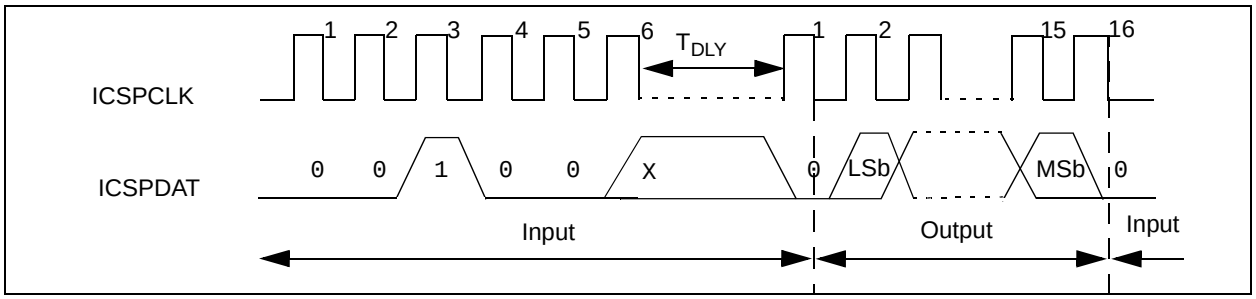
FIGURE 4-2: LOAD DATA FOR PROGRAM MEMORY



4.2.3 READ DATA FROM PROGRAM MEMORY

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the first falling clock edge, and it will revert to Input mode (high-impedance) after the 16th falling edge of the clock. If the program memory is code-protected ($\overline{CP}$), the data will be read as zeros.

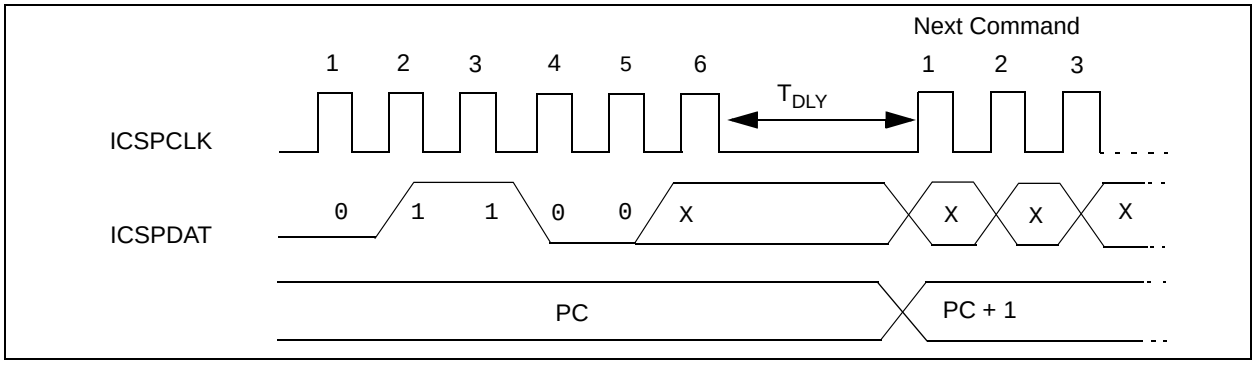
FIGURE 4-3: READ DATA FROM PROGRAM MEMORY



4.2.4 INCREMENT ADDRESS

The Program Counter (PC) is incremented when this command is received. It is not possible to decrement the PC. To reset this counter, the user must exit Program/Verify mode and re-enter it or use the Reset Address command.

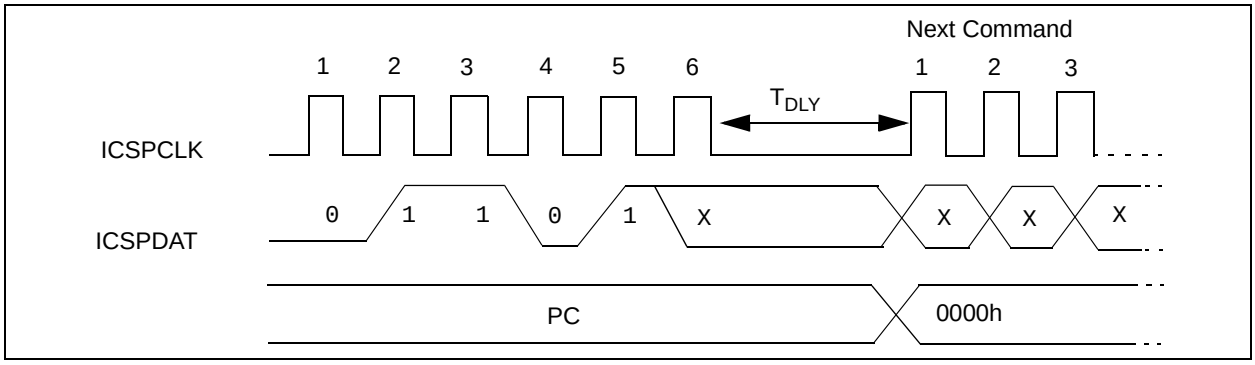
FIGURE 4-4: INCREMENT ADDRESS



4.2.5 RESET ADDRESS

After receiving this command the Program Counter (PC) is set to 0000h. The PC will be reset independent of addressing the program memory or the configuration memory.

FIGURE 4-5: RESET ADDRESS

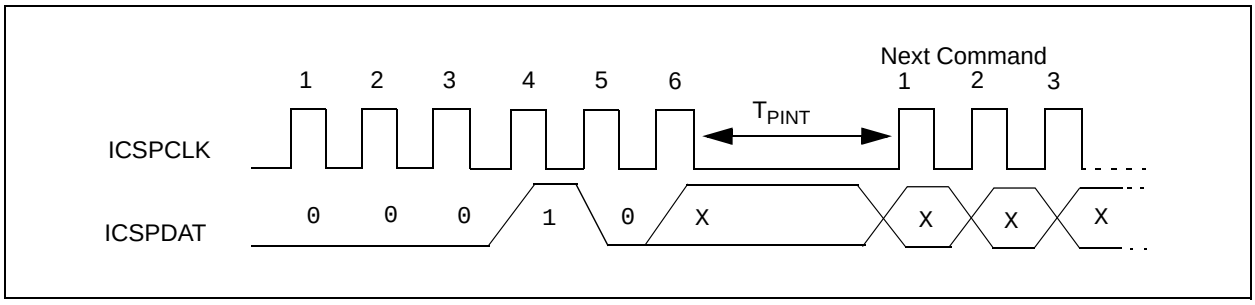


4.2.6 BEGIN INTERNALLY TIMED PROGRAMMING

A Load Configuration or Load Data for Program Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. An internal timing mechanism executes the write. The user must allow for the program cycle time for the programming to complete. The address that is being programmed is not erased prior to being programmed.

The End Externally Timed Programming command is not needed when the Begin Internally Timed Programming is used to start the programming.

FIGURE 4-6: BEGIN INTERNALLY TIMED PROGRAMMING

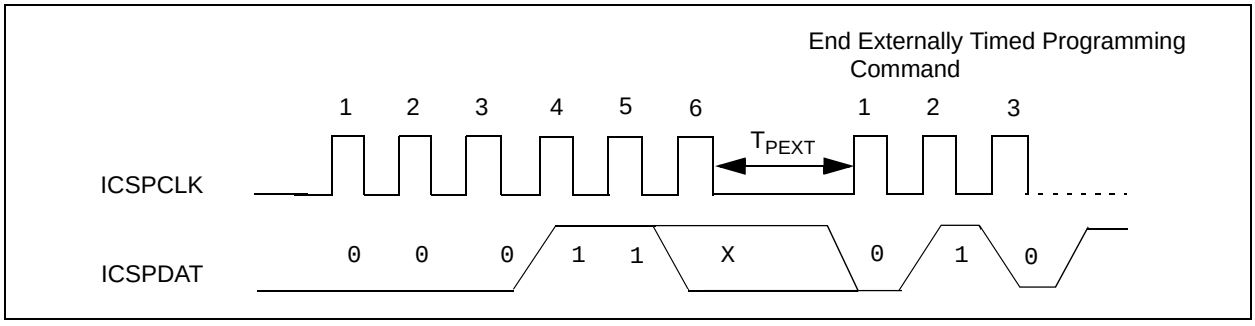


4.2.7 BEGIN EXTERNALLY TIMED PROGRAMMING

A Load Configuration, Load Data for Program Memory or Load Data for Data Memory command must be given before every Begin Programming command. Programming of the addressed memory will begin after this command is received. To complete the programming of the address, the End Externally Timed Programming command must be sent in the specified time window defined by T_{PEXT}.

The Begin Externally Timed Programming command can not be used for programming the Configuration Words.

FIGURE 4-7: BEGIN EXTERNALLY TIMED PROGRAMMING

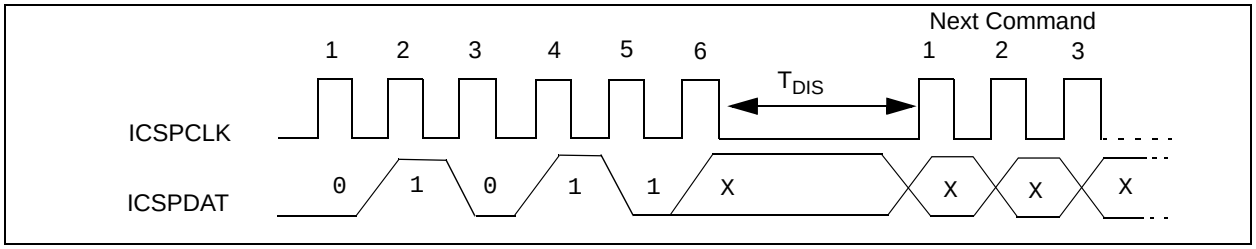


4.2.8 END EXTERNALLY TIMED PROGRAMMING

This command is required after a Begin Externally Timed Programming command is given. This command must be sent within the time window specified by T_{PEXT} after the Begin Externally Timed Programming command is sent.

After sending the End Externally Timed Programming command, an additional delay (T_{DIS}) is required before sending the next command. This delay is longer than the delay ordinarily required between other commands.

FIGURE 4-8: END EXTERNALLY TIMED PROGRAMMING



4.2.9 BULK ERASE PROGRAM MEMORY

The Bulk Erase Program Memory command performs two different functions, dependant on the current state of the Program Counter (PC).

PC 0000h-1FFFh:

- Program Memory is erased
- Configuration words are erased

PC 2000h-2008h:

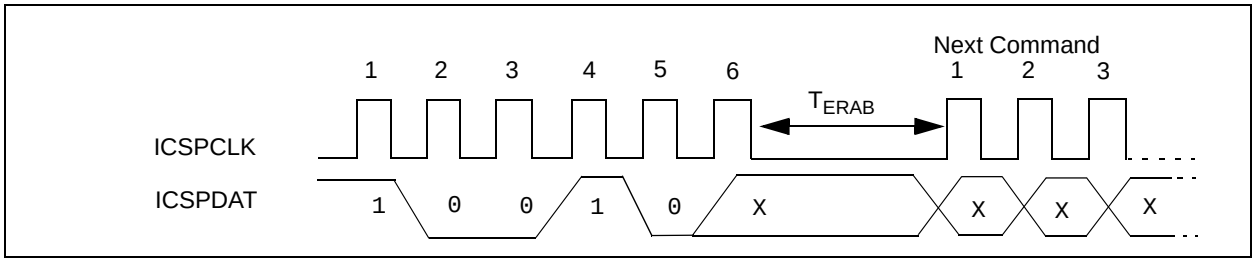
- Program Memory is erased
- Configuration Words are erased
- User ID Locations are erased

After receiving the Bulk Erase Program Memory command, the erase will not complete until the time interval, T_{ERAB}, has expired.

Note 1: The code protection Configuration bit ($\overline{CP}$) has no effect on the Bulk Erase Program Memory command.

Note 2: A Bulk Erase Program Memory command should not be issued when the PC is greater than 2008h.

FIGURE 4-9: BULK ERASE PROGRAM MEMORY

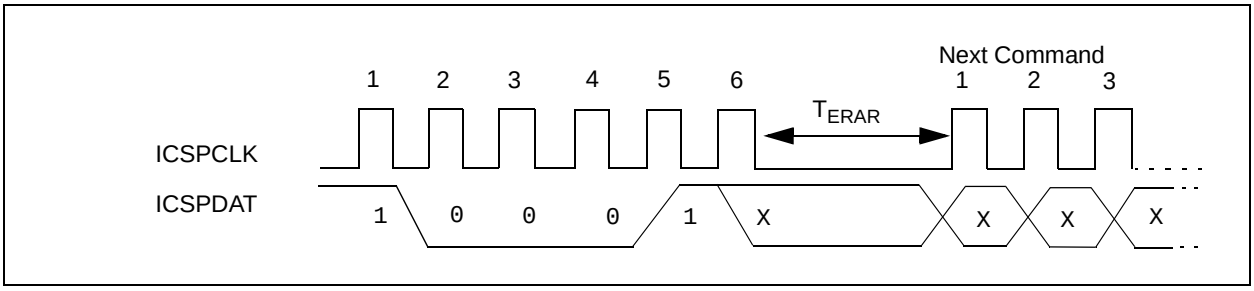


4.2.10 ROW ERASE PROGRAM MEMORY

A row of program memory consists of 32 consecutive 14-bit words. A row is addressed by the Program Counter PC<13:5>. The Row Erase Program Memory command can be used to erase an individual row. If the program memory is code protected the Row Erase Program Memory command will be ignored. When the PC is 2000h-2008h the Row Erase Program Memory command will only erase the user ID locations, independent of the setting of the $\overline{CP}$ Configuration bit.

After receiving the Row Erase Program Memory command, the erase will not complete until the time interval, T_{ERAR}, has expired.

FIGURE 4-10: ROW ERASE PROGRAM MEMORY



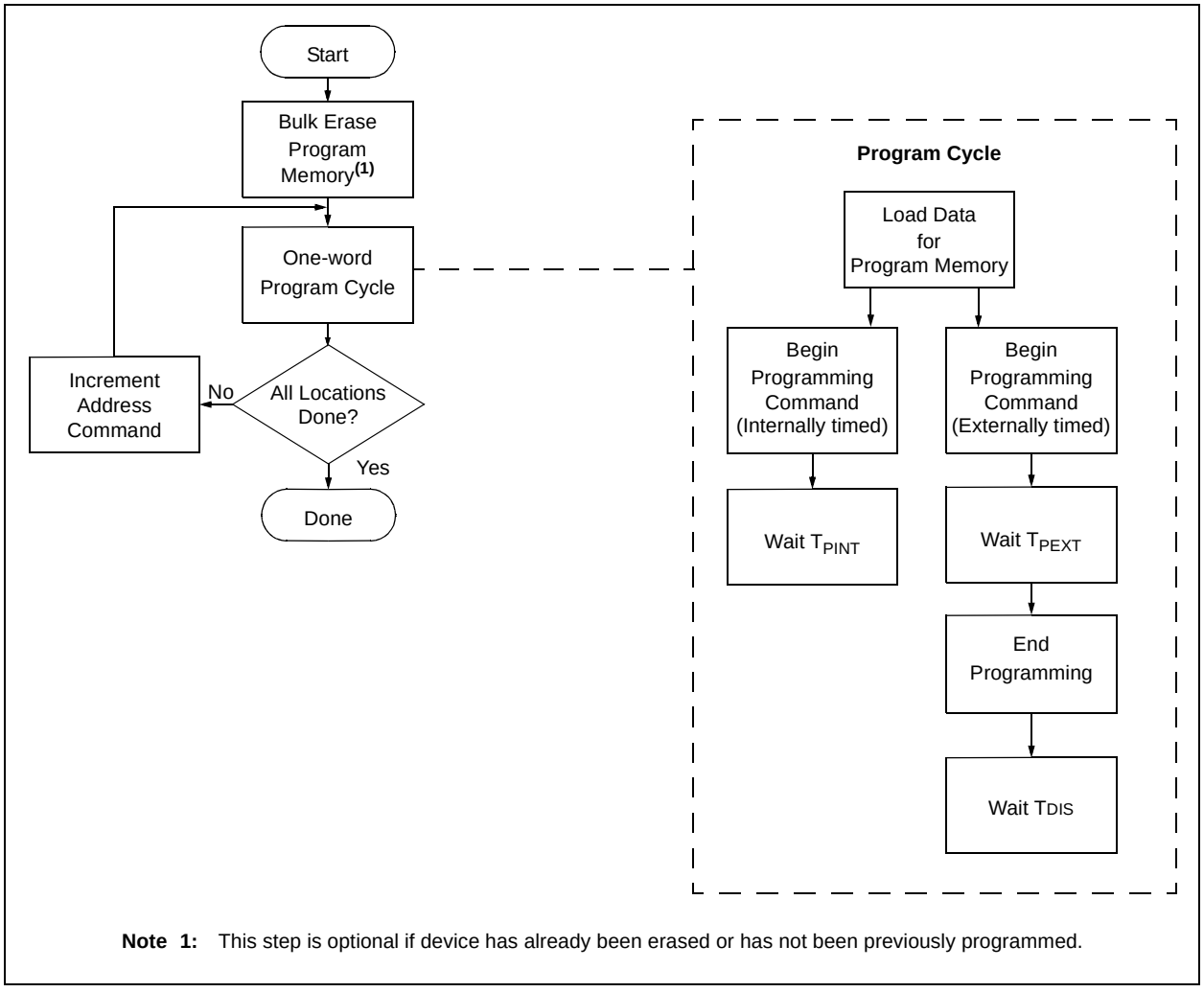
5.0 PROGRAMMING ALGORITHMS

The PIC16F72X/PIC16LF72X devices have the capability of storing eight 14-bit words in its data latches. The data latches are internal to the PIC16F72X/PIC16LF72X devices and are only used for programming. The data latches allow the user to program up to eight program words with a single Begin Externally Timed Programming or Begin Internally Timed Programming command. The Load Program Data or the Load Configuration Word command is used to load a single data latch. The data latch will hold the data until Begin Externally Timed Programming or Begin Internally Timed Programming command is given.

The data latches are aligned with the 3 LSb of the PC. The address of the PC, at the time the Begin Externally Timed Programming or Begin Internally Timed Programming command is given, will determine which location(s) in memory are written. Writes can not cross a physical eight-word boundary. For example, attempting to write from PC 0002h-0009h will result in data being written to 0008h-000Fh.

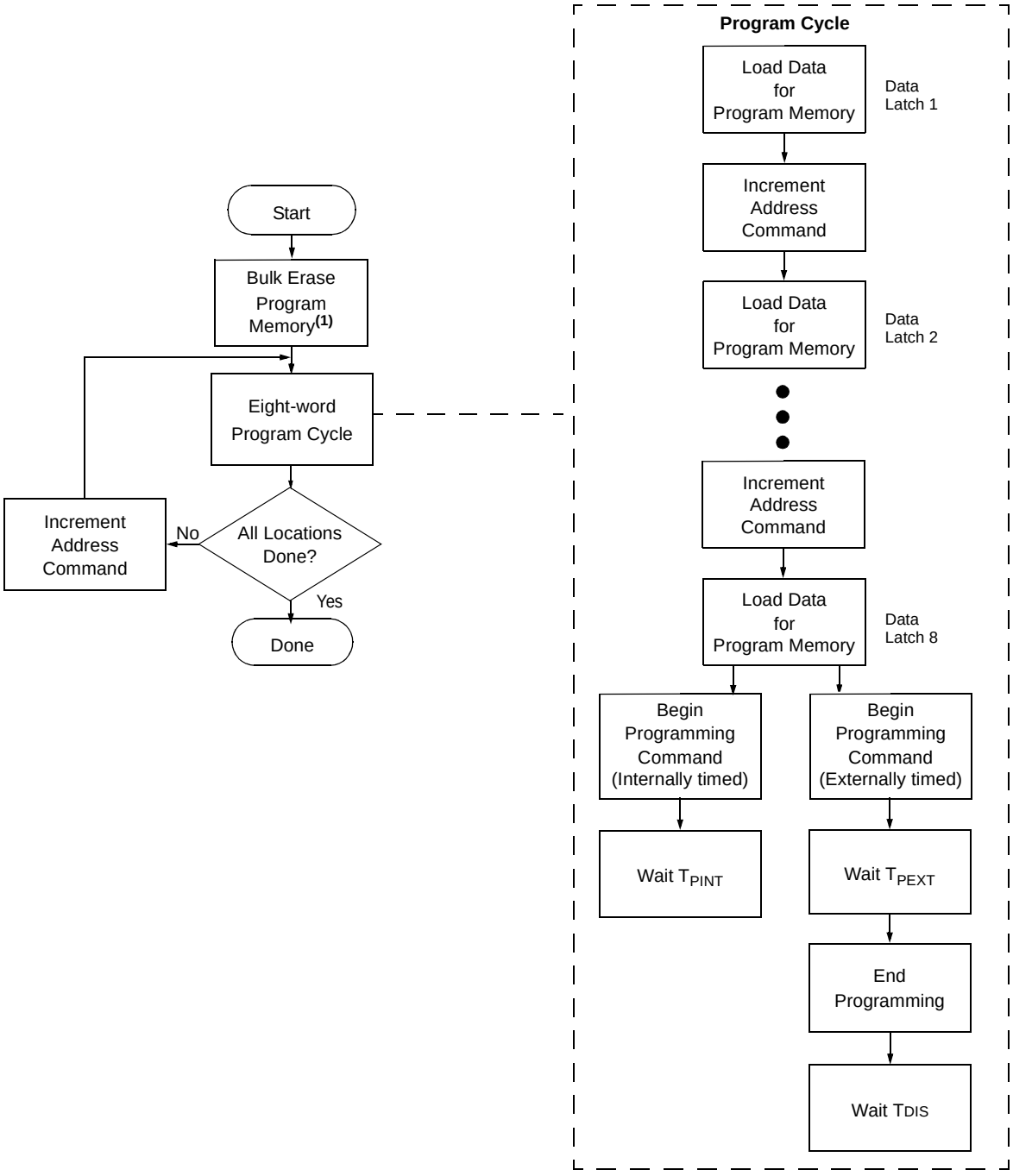
If more than 8 data latches are written without a Begin Externally Timed Programming or Begin Internally Timed Programming command the data in the data latches will be overwritten. The following diagrams show the recommended flowcharts for programming.

FIGURE 5-1: ONE-WORD PROGRAMMING FLOWCHART



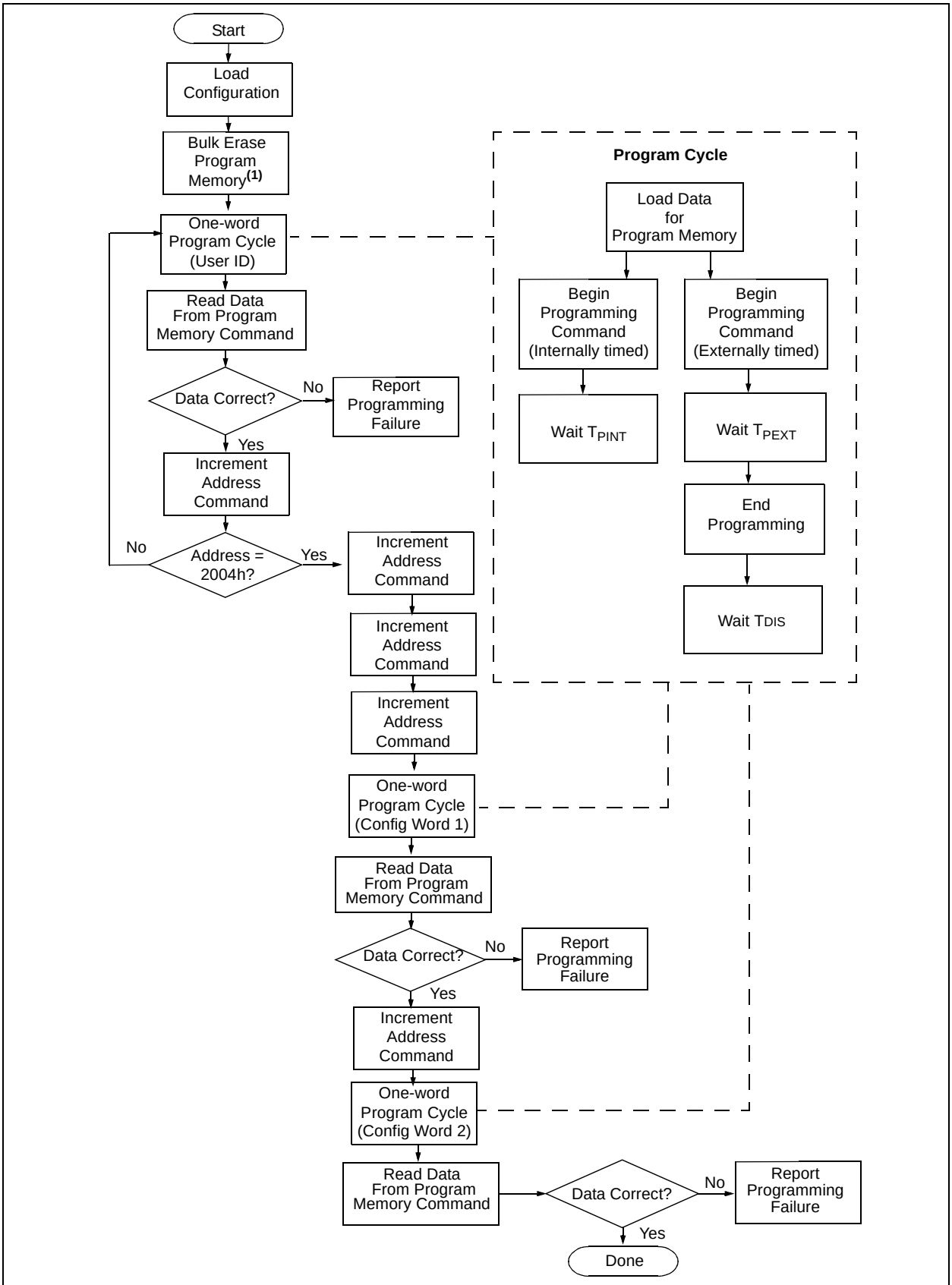
Note 1: This step is optional if device has already been erased or has not been previously programmed.

FIGURE 5-2: EIGHT-WORD PROGRAMMING FLOWCHART



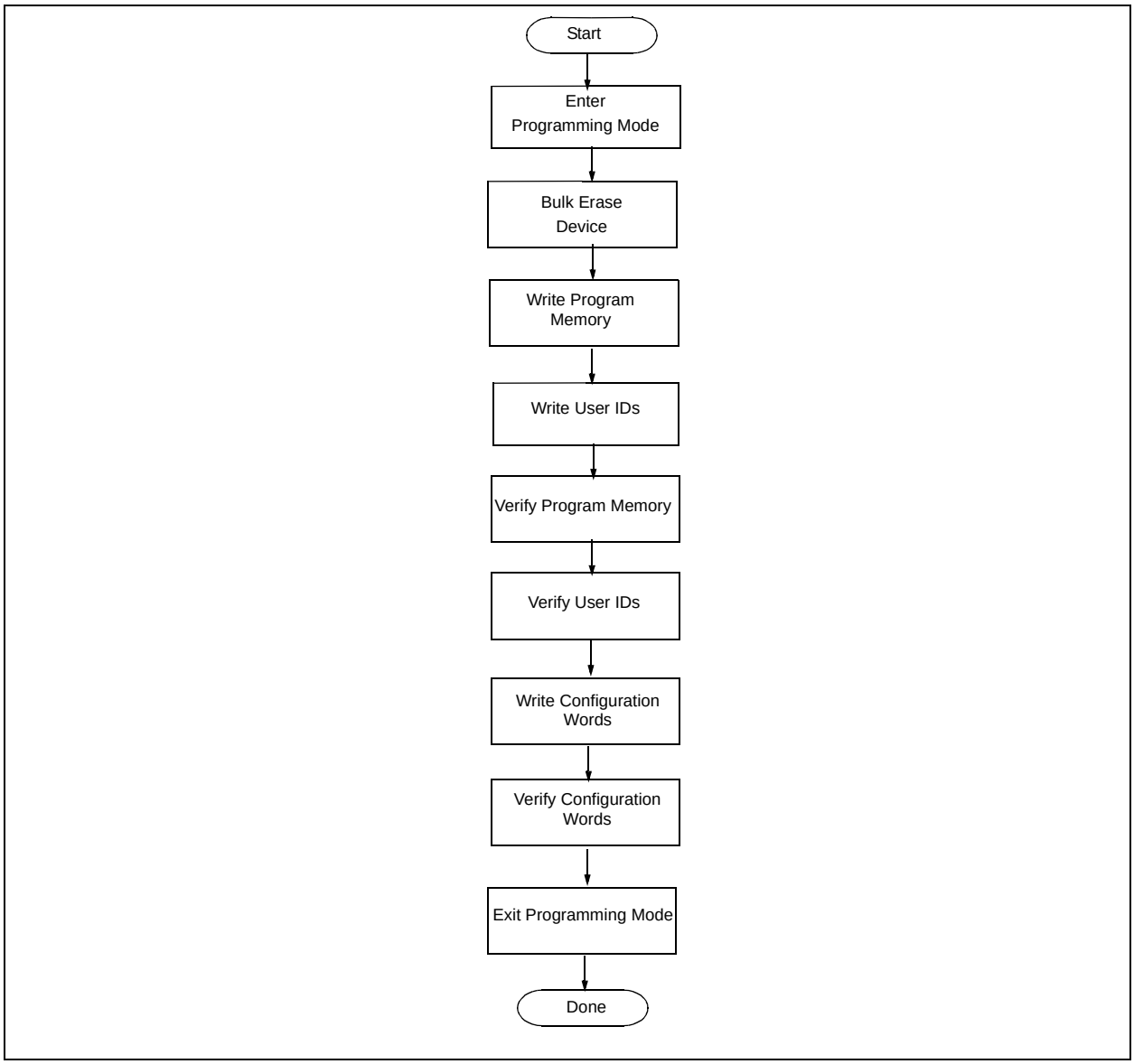
Note 1: This step is optional if device is erased or not previously programmed.

FIGURE 5-3: PROGRAM FLOWCHART – PIC16F72X CONFIGURATION MEMORY



Note 1: This step is optional if device is erased or not previously programmed.

FIGURE 5-4: VERIFY FLOWCHART



6.0 CODE PROTECTION

Code protection is controlled using the $\overline{CP}$ bit in Configuration Word 1. When code protection is enabled, all program memory locations (0000h-1FFFh) read as all '0'. Further programming is disabled for the program memory (0000h-1FFFh).

The user ID locations and Configuration Words can be programmed and read out regardless of the code protection settings.

6.1 Enabling Code Protection

Code protection is enabled by programming the $\overline{CP}$ bit in Configuration Word 1 to '0'.

6.2 Disabling Code Protection

The only way to disable code protection is to use the Bulk Erase Program Memory command.

7.0 HEX FILE USAGE

In the hex file there are two bytes per program word stored in the Intel® INH8M hex format. Data is stored LSB first, MSB second. Because there are two bytes per word, the addresses in the hex file are 2x the address in program memory. (Example: The Configuration Word 1 is stored at 2007h on the PIC16F72X/PIC16LF72X. In the hex file this will be at location 400Eh-400Fh).

7.1 Configuration Word

To allow portability of code, it is strongly recommended that the programmer is able to read the Configuration Words and user ID locations from the hex file. If the Configuration Words information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Words and user ID information should be included.

7.2 Device ID and Revision

If a device ID is present in the hex file at 400Ch-400Dh (2006h on the part), the programmer should verify the device ID/revision against the value read from the part. On a mismatch condition, the programmer should generate a warning message.

7.3 Checksum Computation

The checksum is calculated by two different methods, dependent on the setting of the CP Configuration bit.

7.3.1 CODE PROTECTION DISABLED

With the code protection disabled, the checksum is computed by reading the contents of the PIC16F72X/PIC16LF72X program memory locations and adding up the program memory data, starting at address 0000h, up to the maximum user addressable location (e.g., 1FFFH for the PIC16F726). Any Carry bit exceeding 16 bits are neglected. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unused Configuration bits are masked to '0'.

EXAMPLE 7-1: CHECKSUM COMPUTED WITH CODE PROTECTION DISABLED

PIC16F726	Sum of Memory addresses 0000h-1FFFh	2534h
	Configuration Word 1	2AC3h
	Configuration Word 1 mask	3F7Fh
	Configuration Word 2	3FEFh
	Configuration Word 2 mask	0030h
	Checksum = 2534h + (2AC3h and 3F7Fh) + (3FEFh and 0030h)	
	= 2534h + 2A43h + 0020h	
	= 4F97h	

7.3.2 CODE PROTECTION ENABLED

With the code protection enabled, the checksum is computed in the following manner. The Configuration Words are summed (all unused Configuration bits are masked to '0') with the Least Significant nibble of the user ID's.

EXAMPLE 7-2: CHECKSUM COMPUTED WITH CODE PROTECTION ENABLED

PIC16F726	Configuration Word 1	2A83h
	Configuration Word 1 mask	3F7Fh
	Configuration Word 2	3FEFh
	Configuration Word 2 mask	0030h
	User ID (2000h)	0123h
	User ID (2001h)	4567h
	User ID (2002h)	89ABh
	User ID (2003h)	CDEFh

Checksum = (2A83h and 3F7Fh) + (3FEFh and 0030h) + (0123h and 000Fh) + (4567h and 000Fh) + (89ABh and 000Fh) +(CDEFh and 000Fh)

= 2A03h +0020h + 0003h + 0007h + 000Bh + 000Fh

= 2A47h

8.0 ELECTRICAL SPECIFICATIONS

Refer to device specific data sheet for absolute maximum ratings.

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature +10°C ≤ TA ≤ +40°C				
Sym.	**Characteristics**	**Min.**	**Type.**	**Max.**	**Units**	**Conditions/Comments**
Supply Voltages and currents						
VDD	**VDD**					
	PIC16F72X (excluding Bulk Erase)	1.8	—	5.5	V	
	PIC16LF72X (excluding Bulk Erase)	1.8	—	3.6	V	
	PIC16F72X/PIC16LF72X Bulk Erase	2.7		—	V	
IDDI	Current on VDD, Idle			1.0	mA	
IDDA	Current on VDD, program cycle or Bulk Erase in progress			5.0	mA	
VIHH	**VPP**					
	High voltage on $\overline{MCLR}$/VPP for Program/Verify mode entry	8.0	—	9.0	V	
TVHHR	$\overline{MCLR}$ rise time (VDD to VIHH) for Program/Verify mode entry	—	—	1.0	µs	
IPP	Current on $\overline{MCLR}$/VPP			5.0	mA	
	I/O pins					
VIH	(ICSPCLK, ICSPDAT) input high level	0.8 VDD	—	—	V	
VIL	(ICSPCLK, ICSPDAT) input low level	—	—	0.2 VDD	V	
VOH	ICSPDAT output high level	VDD-0.7 VDD-0.7 VDD-0.7		VDD	V	IOH = 3.5 mA, VDD = 5V IOH = 3 mA, VDD = 3.3V IOH = 2 mA, VDD = 1.8V
VOL	ICSPDAT output low level	VSS		VSS+0.6 VSS+0.6 VSS+0.6	V	IOH = 8 mA, VDD = 5V IOH = 6 mA, VDD = 3.3V IOH = 3 mA, VDD = 1.8V
Programming mode entry and exit						
TENTS	Programing mode entry setup time: ICSPCLK, ICSPDAT setup time before VDD or $\overline{MCLR}$↑	100	—	—	ns	
TENTH	Programing mode entry hold time: ICSPCLK, ICSPDAT hold time after VDD or $\overline{MCLR}$↑	250			µs	
Serial Program/Verify						
TCKL	Clock Low Pulse Width	100	—	—	ns	
TCKH	Clock High Pulse Width	100	—	—	ns	
TDS	Data in setup time before clock↓	100	—	—	ns	
TDH	Data in hold time after clock↓	100	—	—	ns	
TCO	Clock↑ to data out valid (during a Read Data command)	0	—	80	ns	
TLZD	Clock↓ to data low-impedance (during a Read Data command)	0	—	80	ns	
THZD	Clock↓ to data high-impedance (during a Read Data command)	0	—	80	ns	

TABLE 8-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE (CONTINUED)

AC/DC CHARACTERISTICS		Standard Operating Conditions (unless otherwise stated) Operating Temperature +10°C ≤ TA ≤ +40°C				
Sym.	**Characteristics**	**Min.**	**Type.**	**Max.**	**Units**	**Conditions/Comments**
T_{DLY}	Data input not driven to next clock input (delay required between command/data or command/ command)	1.0	—	—	µs	
T_{ERAB}	Bulk Erase cycle time	—	—	5	ms	
T_{ERAR}	Row erase cycle time	—	—	2.5	ms	
T_{PINT}	Internally timed programming operation time	— —	— —	2.5 5	ms ms	Program memory Configuration fuses
T_{PEXT}	Externally timed programming pulse	1.0	—	2.1	ms	10°C ≤ TA ≤ +40°C Program memory
T_{DIS}	Time delay from program to compare (HV discharge time)	100	—	—	µs	
T_{EXIT}	Time delay when exiting Program/Verify mode	1	—	—	µs	

8.1 AC Timing Diagrams

FIGURE 8-2: PROGRAMMING MODE ENTRY – VDD FIRST

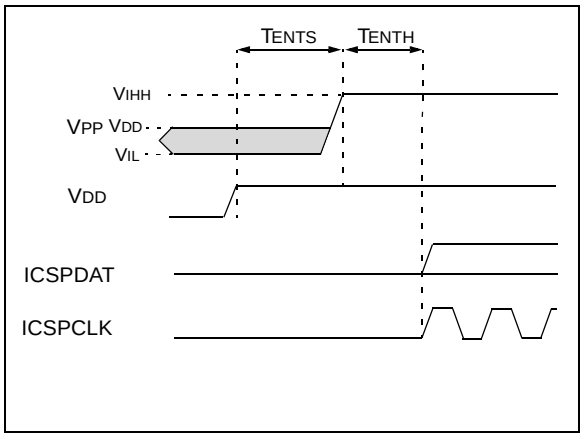


FIGURE 8-3: PROGRAMMING MODE ENTRY – VPP FIRST

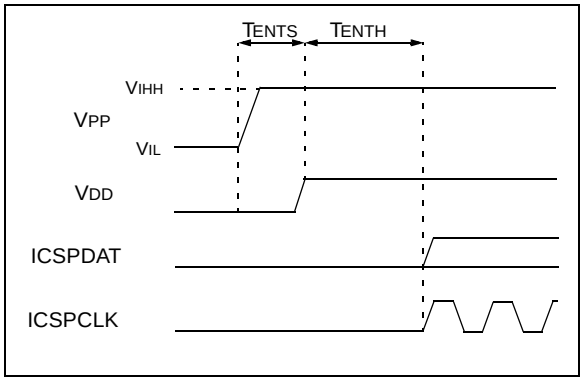


FIGURE 8-4: PROGRAMMING MODE EXIT – VPP LAST

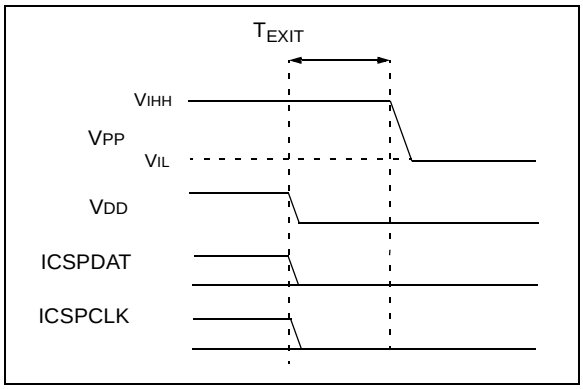


FIGURE 8-5: PROGRAMMING MODE EXIT – VDD LAST

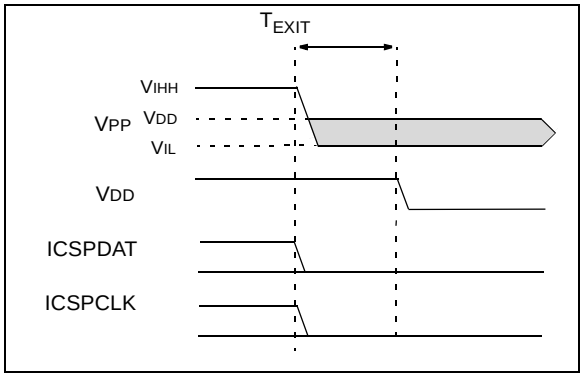


FIGURE 8-6: CLOCK AND DATA TIMING

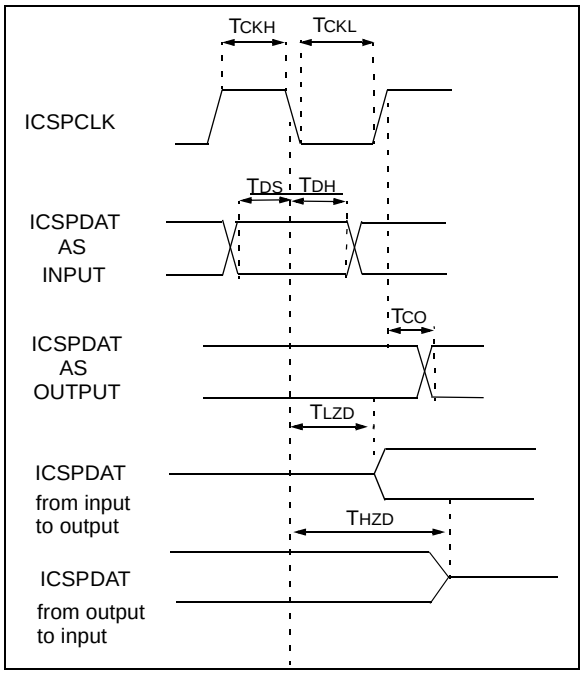
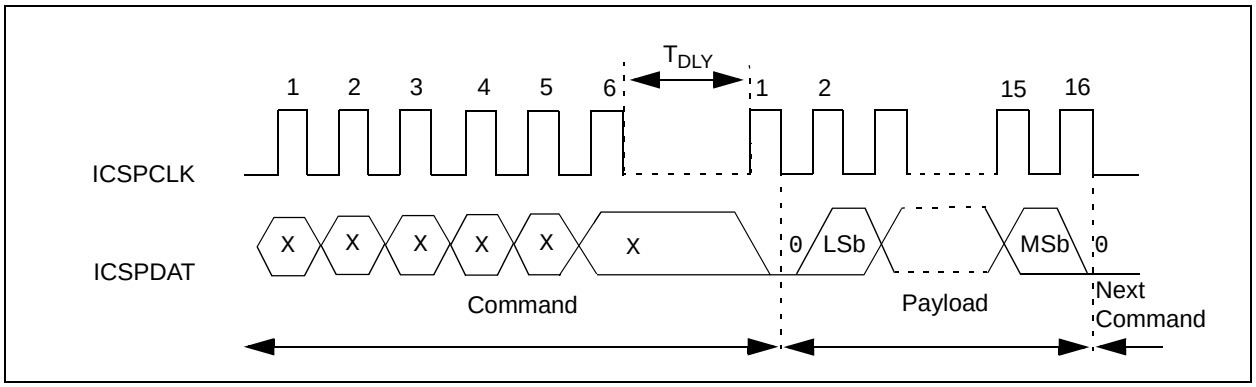


FIGURE 8-7: COMMAND-PAYLOAD TIMING



APPENDIX A: REVISION HISTORY

Revision A (11/2007)

Original release of this document.

Revision B (02/2009)

Updated minimum VDD for Bulk Erase in Table 8-1. Various minor edits.

Clarified time of transition from input to output in Figure 4-3.

Corrected Reserved area range in Figures 3-1, 3-2, and 3-3.

Corrected low-voltage range for Programming modes shown in Figures 8-3 and 8-5.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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