PIC18F45J10 FAMILY

Flash Microcontroller Programming Specification

1.0 DEVICE OVERVIEW

This document includes the programming specifications for the following devices:

- PIC18F24J10
- PIC18F25J10
- PIC18F44J10
- PIC18F45J10
- PIC18LF24J10
- PIC18LF25J10
- PIC18LF44J10
- PIC18LF45J10

2.0 PROGRAMMING OVERVIEW OF THE PIC18F45J10 FAMILY

The PIC18F45J10 family devices are programmed using In-Circuit Serial Programming™ (ICSP™). This programming specification applies to devices of the PIC18F45J10 family in all package types.

2.1 Pin Diagrams

The pin diagrams for the PIC18F45J10 family are shown in Figure 2-1 and Figure 2-2. The pins that are required for programming are listed in Table 2-1 and shown in darker lettering in the diagrams.

TABLE 2-1: PIN DESCRIPTIONS (DURING PROGRAMMING): PIC18F45J10 FAMILY

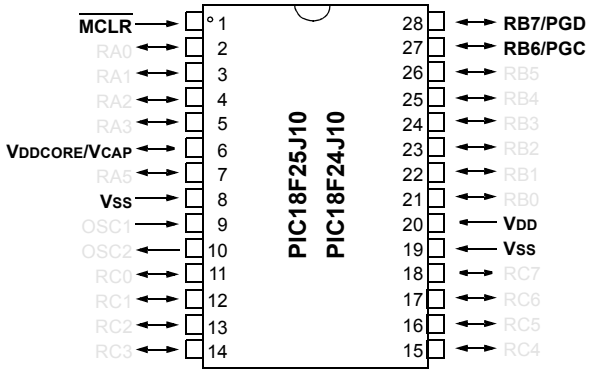
Pin Name	During Programming		
	Pin Name	Pin Type	Pin Description
$\overline{MCLR}$	$\overline{MCLR}$	P	Programming Enable
VDD and AVDD(1)	VDD	P	Power Supply
VSS and AVSS(1)	VSS	P	Ground
VDDCORE/VCAP	VDDCORE	P	Regulated Power Supply for Microcontroller Core
	VCAP	I	Filter Capacitor for On-Chip Voltage Regulator
RB6	PGC	I	Serial Clock
RB7	PGD	I/O	Serial Data

Legend: I = Input, O = Output, P = Power

Note 1: All power supply and ground pins must be connected, including analog supplies (AVDD) and ground (AVSS).

FIGURE 2-1: PIC18F45J10 FAMILY PIN DIAGRAMS

28-Pin SPDIP, SOIC, SSOP



28-Pin QFN

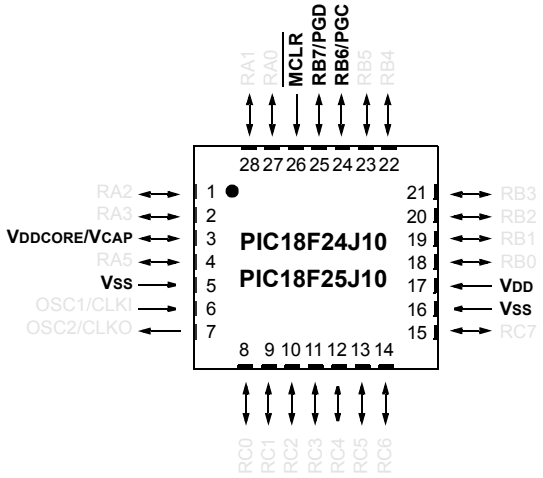
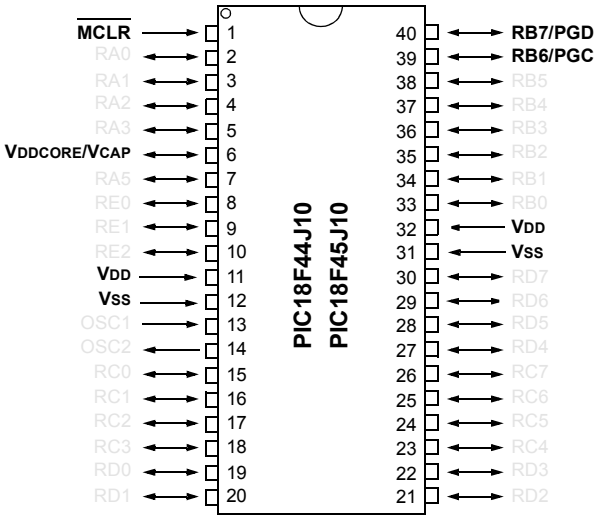
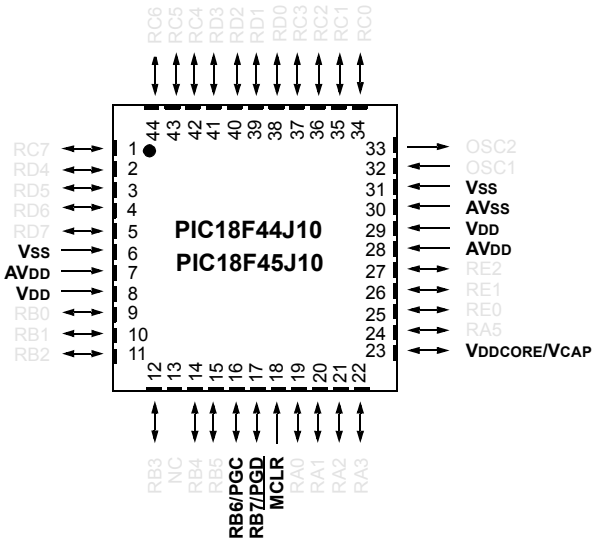


FIGURE 2-2: PIC18F45J10 FAMILY PIN DIAGRAMS (CONTINUED)

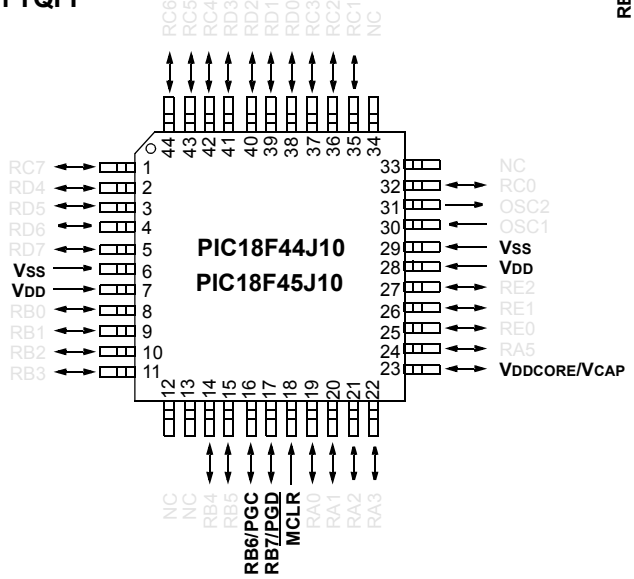
40-Pin PDIP



44-Pin QFN



44-Pin TQFP



2.1.1 PIC18FXXJ10/LFXXJ10 DEVICES AND THE ON-CHIP VOLTAGE REGULATOR

Depending on the particular PIC18F45J10 family device, the core is either powered from an external source or from an on-chip voltage regulator which derives power from VDD. Both methods use the common VDDCORE/VCAP pin.

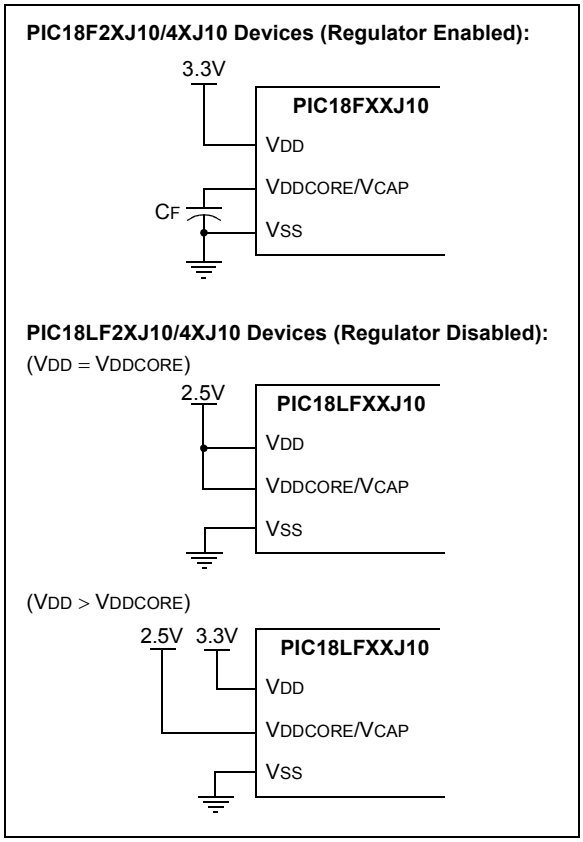
Baseline devices in this family, with a standard VDD range (e.g., PIC18F45J10), are permanently configured with their regulators in an always ON state. All power for the device is provided by the VDD pins, up to a voltage level of VDDMAX. For proper device operation, a low ESR capacitor must connect the VDDCORE/VCAP pin to ground for proper device operation.

Devices with an extended VDD range (e.g., PIC18LF45J10) are permanently configured with the on-chip regulator disabled. If VDD exceeds VDDCOREMAX, power to the core must be supplied separately on the VDDCORE/VCAP pin.

Whether or not the regulator is used, it is always good design practice to have sufficient capacitance on all supply pins. Examples are shown in Figure 2-3.

The specifications for core voltage and capacitance are listed in **Section 6.0 "AC/DC Characteristics Timing Requirements for Program/Verify Test Mode"**.

FIGURE 2-3: CONNECTIONS FOR THE ON-CHIP REGULATOR



2.2 Memory Maps

The PIC18F45J10 family of devices offers program memory sizes of 16 and 32 Kbytes. The memory sizes for different members of the family are shown in Table 2-2. The overall memory maps for all the devices are shown in Figure 2-4.

TABLE 2-2: PROGRAM MEMORY SIZES FOR PIC18F45J10 FAMILY DEVICES

Device*	Program Memory (Kbytes)	Location of Flash Configuration Words
PIC18F24J10	16	3FF8h:3FFFh
PIC18F44J10		
PIC18F25J10	32	7FF8h:7FFFh
PIC18F45J10		

* Includes PIC18F and PIC18LF devices.

For purposes of code protection, the program memory for every device is treated as a single block. Enabling code protection thus protects the entire code memory and not individual segments.

The Configuration Words for these devices are located at addresses 300000h through 300005h. These are implemented as three pairs of volatile memory registers. Each register is automatically loaded from a copy stored at the end of program memory. For this reason, the top four words (or eight bytes) of the code space (also called the Flash Configuration Words) should be written with configuration data and not executable code. The addresses of the Flash Configuration Words are also listed in Table 2-2. Refer to section **Section 5.0 "Configuration Word"** for more information.

Locations 3FFFFEh and 3FFFFFh are reserved for the device ID bits. These bits may be used by the programmer to identify what device type is being programmed and are described in **Section 5.1 "Device ID Word"**. These device ID bits read out normally, even after code protection.

2.2.1 MEMORY ADDRESS POINTER

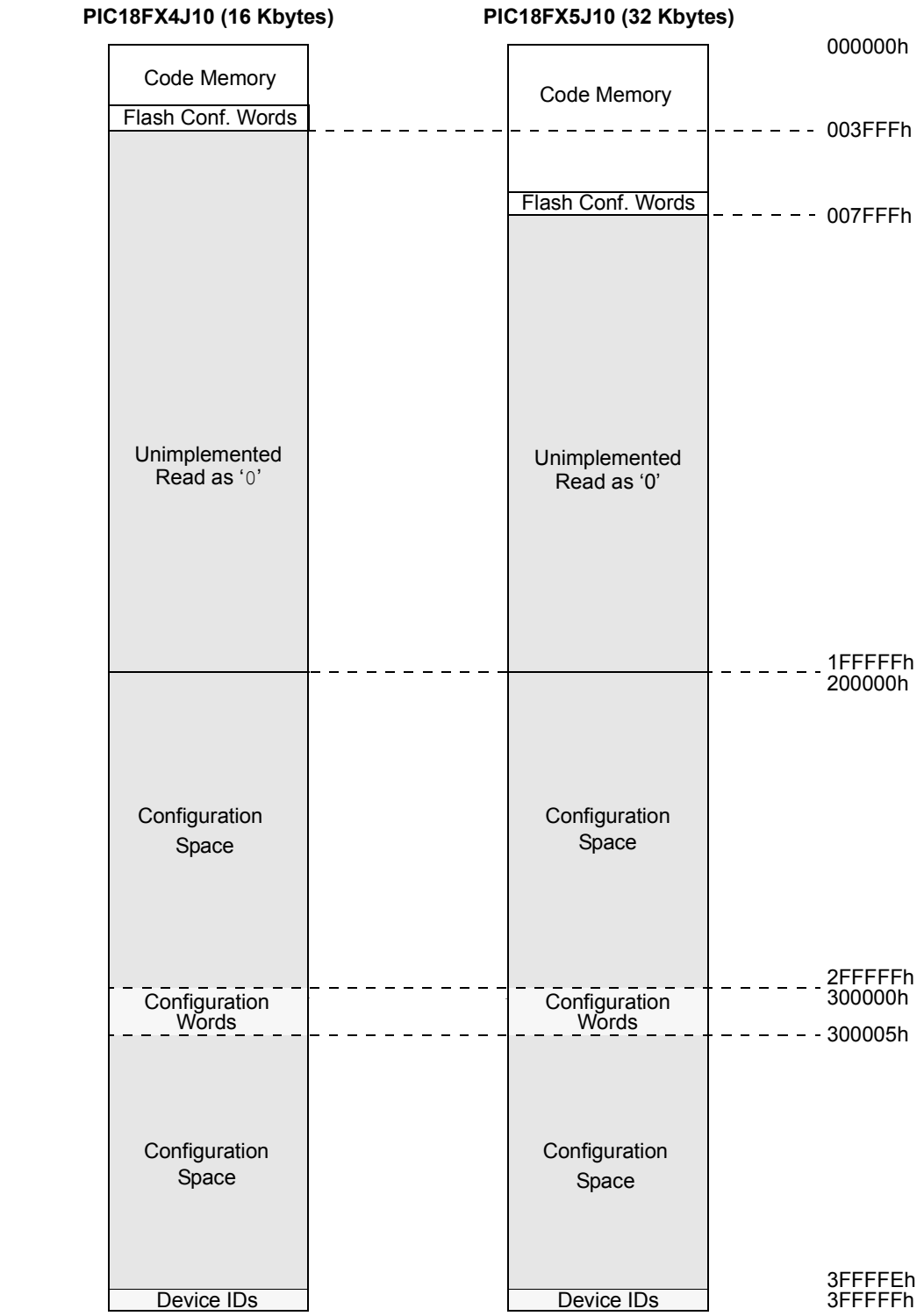
Memory in the device address space (000000h to 3FFFFFh) is addressed via the Table Pointer register, which in turn is comprised of three registers:

- TBLPTRU at RAM address 0FF8h
- TBLPTRH at RAM address 0FF7h
- TBLPTRL at RAM address 0FF6h

TBLPTRU	TBLPTRH	TBLPTRL
Addr[21:16]	Addr[15:8]	Addr[7:0]

The 4-bit command, '0000' (core instruction), is used to load the Table Pointer prior to using many read or write operations.

FIGURE 2-4: MEMORY MAPS FOR PIC18F45J10 FAMILY DEVICES



Memory spaces are unimplemented or unavailable in normal execution mode and read as '0'.

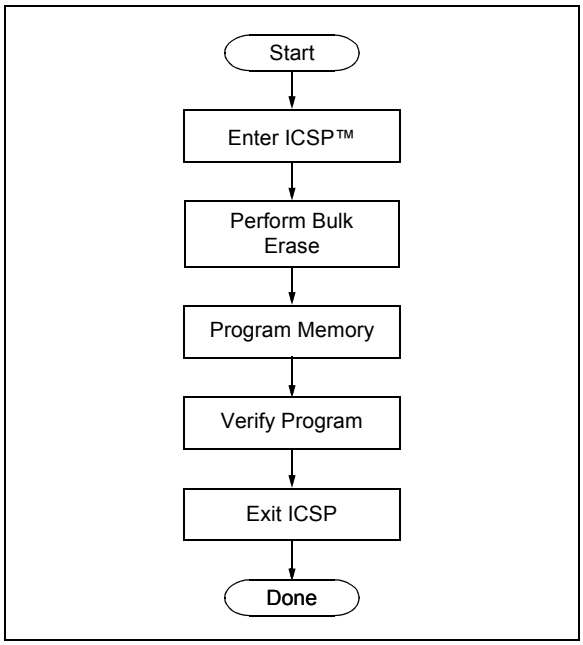
Memory spaces are read-only (device IDs) or cannot be directly programmed by ICSP™ (Configuration Words).

Note: Sizes of memory areas are not to scale. Sizes of accessible memory areas are enhanced to show detail.

2.3 Overview of the Programming Process

Figure 2-5 shows the high-level overview of the programming process. First, a Bulk Erase is performed. Next, the code memory is programmed. Since the only nonvolatile Configuration Words are within the code memory space, they too are programmed as if they were code. Code memory (including the Configuration Words) is then verified to ensure that programming was successful.

FIGURE 2-5: HIGH-LEVEL PROGRAMMING FLOW



2.4 Entering and Exiting ICSP™ Program/Verify Mode

Entry into ICSP modes for PIC18F45J10 family devices is somewhat different than previous PIC18 devices. As shown in Figure 2-6, entering ICSP Program/Verify mode requires three steps:

1. Voltage is briefly applied to the $\overline{MCLR}$ pin.
2. A 32-bit key sequence is presented on PGD.
3. Voltage is reapplied to $\overline{MCLR}$ within a specific period of time and held.

The programming voltage applied to $\overline{MCLR}$ is V_{IH}, or essentially, V_{DD}. There is no minimum time requirement for holding at V_{IH}. After V_{IH} is removed, an interval of at least P19 must elapse before presenting the key sequence on PGD.

The key sequence is a specific 32-bit pattern, '0100 1101 0100 0011 0100 1000 0101 0000' (more easily remembered as 4D434850h in hexadecimal). The device will enter Program/Verify mode only if the sequence is valid. The Most Significant bit of the most significant nibble must be shifted in first.

Once the key sequence is complete, V_{IH} must be applied to $\overline{MCLR}$ and held at that level for as long as Program/Verify mode is to be maintained. An interval of at least time P20 and P12 must elapse before presenting data on PGD. Signals appearing on PGD before P12 has elapsed will not be interpreted as valid.

On successful entry, the program memory can be accessed and programmed in serial fashion. While in the Program/Verify mode, all unused I/Os are placed in the high-impedance state.

Exiting Program/Verify mode is done by removing V_{IH} from $\overline{MCLR}$, as shown in Figure 2-7. The only requirement for exit is that an interval P16 should elapse between the last clock and program signals on PGC and PGD before removing V_{IH}.

FIGURE 2-6: ENTERING PROGRAM/VERIFY MODE

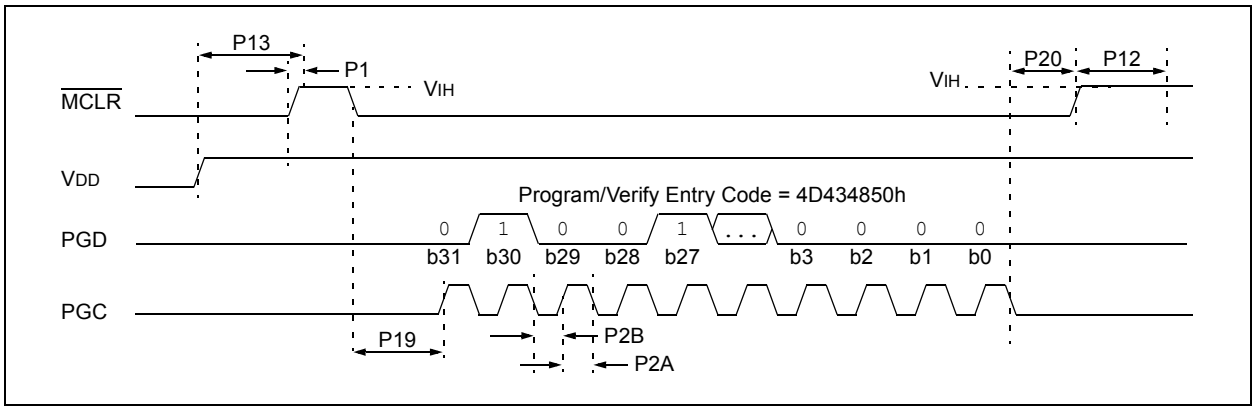
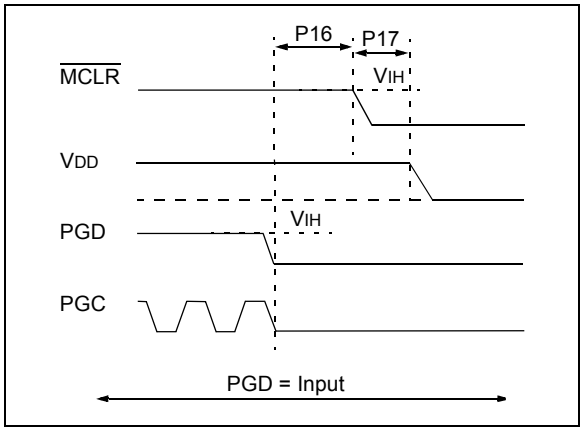


FIGURE 2-7: EXITING PROGRAM/VERIFY MODE



2.5 Serial Program/Verify Operation

The PGC pin is used as a clock input pin and the PGD pin is used for entering command bits and data input/output during serial operation. Commands and data are transmitted on the rising edge of PGC, latched on the falling edge of PGC and are Least Significant bit (LSb) first.

2.5.1 FOUR-BIT COMMANDS

All instructions are 20 bits, consisting of a leading 4-bit command followed by a 16-bit operand, which depends on the type of command being executed. To input a command, PGC is cycled four times. The commands needed for programming and verification are shown in Table 2-3.

Depending on the 4-bit command, the 16-bit operand represents 16 bits of input data or 8 bits of input data and 8 bits of output data.

Throughout this specification, commands and data are presented as illustrated in Table 2-4. The 4-bit command is shown Most Significant bit (MSb) first. The command operand, or "Data Payload", is shown <MSB><LSB>. Figure 2-8 demonstrates how to serially present a 20-bit command/operand to the device.

2.5.2 CORE INSTRUCTION

The core instruction passes a 16-bit instruction to the CPU core for execution. This is needed to set up registers as appropriate for use with other commands.

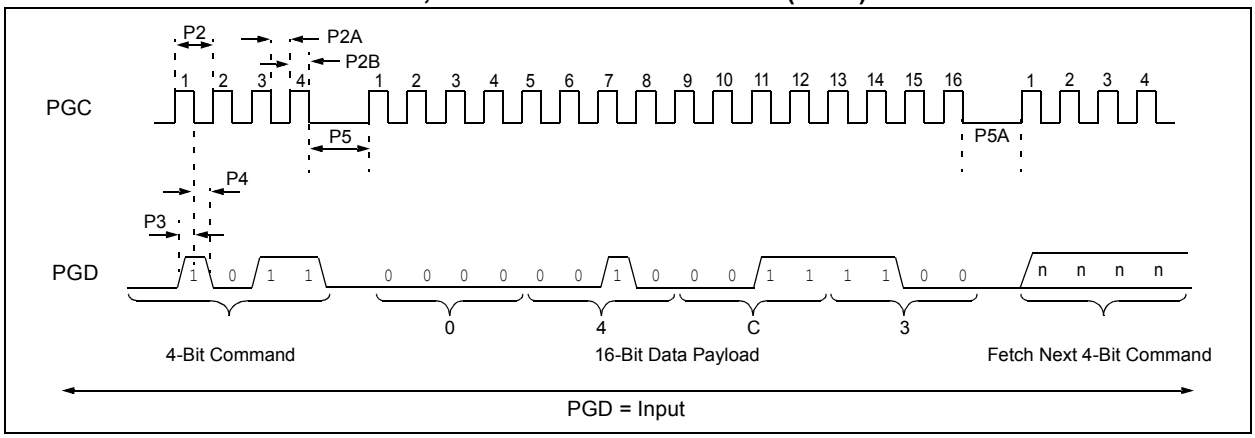
TABLE 2-3: COMMANDS FOR PROGRAMMING

Description	4-Bit Command
Core Instruction (Shift in 16-bit instruction)	0000
Shift out TABLAT register	0010
Table Read	1000
Table Read, post-increment	1001
Table Read, post-decrement	1010
Table Read, pre-increment	1011
Table Write	1100
Table Write, post-increment by 2	1101
Table Write, start programming, post-increment by 2	1110
Table Write, start programming	1111

TABLE 2-4: SAMPLE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
1101	3C 40	Table Write, post-increment by 2

FIGURE 2-8: TABLE WRITE, POST-INCREMENT TIMING (1101)



3.0 DEVICE PROGRAMMING

Programming includes the ability to erase or write the memory within the device.

The EECON1 register is used to control Write or Row Erase operations. The WREN bit must be set to enable writes; this must be done prior to initiating a write sequence. It is strongly recommended that the WREN bit only be set immediately prior to a program erase.

The FREE bit must be set in order to erase the program space being pointed to by the Table Pointer. The erase or write sequence is initiated by setting the WR bit.

3.1 ICSP™ Erase

3.1.1 ICSP™ BULK ERASE

Devices of the PIC18F45J10 family may be Bulk Erased by writing 0180h to the register pair, 3C0005h:3C0004h. The basic sequence is shown in Table 3-1 and demonstrated in Figure 3-1.

Since the code-protect Configuration bit is stored in the program code within code memory, a Bulk Erase operation will also clear any code-protect settings for the device.

The actual Bulk Erase function is a self-timed operation. Once the erase has started (falling edge of the 4th PGC after the `NOP` command), serial execution will cease until the erase completes (parameter P11). During this time, PGC may continue to toggle but PGD must be held low.

Note:	A Bulk Erase is the only way to reprogram the code-protect Configuration bit from an ON state to an OFF state.

TABLE 3-1: BULK ERASE COMMAND SEQUENCE

4-Bit Command	Data Payload	Core Instruction
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 05	MOVLW 05h
0000	6E F6	MOVWF TBLPTRL
1100	01 01	Write 01h to 3C0005h
0000	0E 3C	MOVLW 3Ch
0000	6E F8	MOVWF TBLPTRU
0000	0E 00	MOVLW 00h
0000	6E F7	MOVWF TBLPTRH
0000	0E 04	MOVLW 04h
0000	6E F6	MOVWF TBLPTRL
1100	80 80	Write 80h TO 3C0004h to erase entire device. NOP
0000	00 00	Hold PGD low until erase
0000	00 00	completes.

FIGURE 3-1: BULK ERASE FLOW

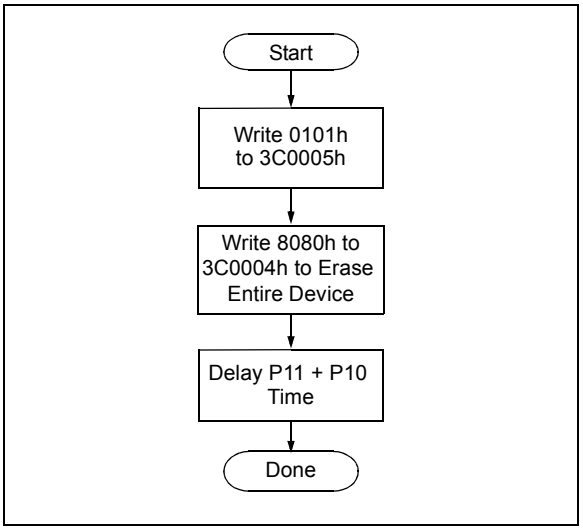
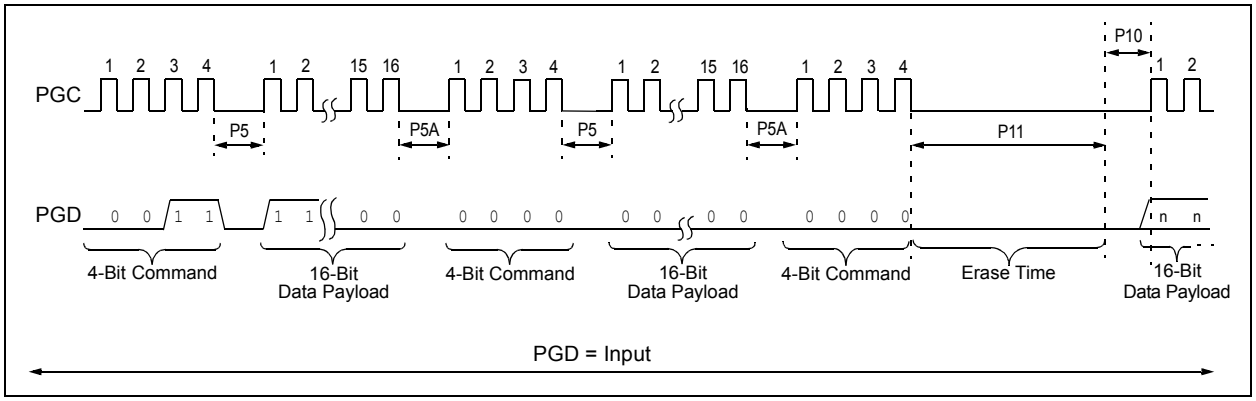


FIGURE 3-2: BULK ERASE TIMING



3.1.2 ICSP™ ROW ERASE

It is possible to erase one row (1024 bytes of data), provided the block is not code-protected. Rows are located at static boundaries beginning at program memory address 000000h, extending to the internal program memory limit (see **Section 2.2 "Memory Maps"**).

The Row Erase duration is externally timed and is controlled by PGC. After the WR bit in EECON1 is set, a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

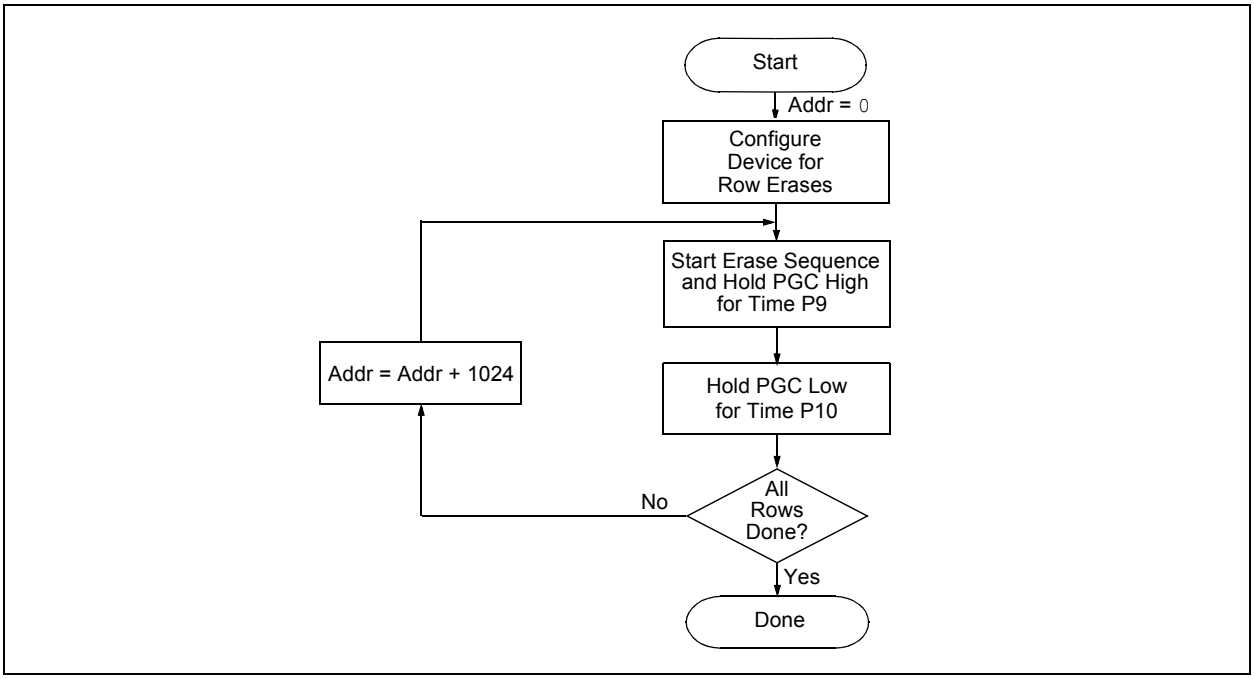
The code sequence to Row Erase a PIC18F45J10 family device is shown in Table 3-2. The flowchart shown in Figure 3-3 depicts the logic necessary to completely erase a PIC18F45J10 family device. The timing diagram that details the "Start Programming" command and parameters P9 and P10 is shown in Figure 3-5.

Note 1:	If the last row of program memory is erased, bit 2 of CONFIG1H must also be programmed as '0'.
2:	The TBLPTR register can point at any byte within the row intended for erase.

TABLE 3-2: ERASE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable memory writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Point to first row in code memory.		
0000 0000 0000	6A F8 6A F7 6A F6	CLRF TBLPTRU CLRF TBLPTRH CLRF TBLPTRL
Step 3: Enable erase and erase single row.		
0000 0000 0000	88 A6 82 A6 00 00	BSF EECON1, FREE BSF EECON1, WR NOP - hold PGC high for time P9 and low for time P10.
Step 4: Repeat step 3, with Address Pointer incremented by 1024 until all rows are erased.		

FIGURE 3-3: SINGLE ROW ERASE CODE MEMORY FLOW



3.2 Code Memory Programming

Programming code memory is accomplished by first loading data into the write buffer and then initiating a programming sequence. The write buffer for all devices in the PIC18F45J10 family is 64 bytes. It can be mapped to any location of the same size beginning at 000000h. The actual memory write sequence takes the contents of this buffer and programs the proper amount of code memory.

Write buffer locations are not cleared following a write operation; the buffer retains its data after the write is complete. This means that the buffer must be written with 64 bytes on each operation. If there are locations in the code memory that are to remain empty, the corresponding locations in the buffer must be filled with FFFFh. This avoids rewriting old data from the previous cycle.

The programming duration is externally timed and is controlled by PGC. After a Start Programming command is issued (4-bit command, '1111'), a NOP is issued, where the 4th PGC is held high for the duration of the programming time, P9.

After PGC is brought low, the programming sequence is terminated. PGC must be held low for the time specified by parameter P10 to allow high-voltage discharge of the memory array.

The code sequence to program a PIC18F45J10 family device is shown in Table 3-3. The flowchart shown in Figure 3-4 depicts the logic necessary to completely write a PIC18F45J10 family device. The timing diagram that details the Start Programming command and parameters P9 and P10 is shown in Figure 3-5.

Note 1: To maintain the endurance specification of the Flash program memory cells, each byte should never be reprogrammed more than twice between erase operations. Before attempting to reprogram any portion of the program memory a third time, an erase operation (either a Bulk Erase or a Row Erase of that section) must be performed.

2: The TBLPTR register must point to the same region when initiating the programming sequence as it did when the write buffers were loaded.

TABLE 3-3: WRITE CODE MEMORY CODE SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Enable writes.		
0000	84 A6	BSF EECON1, WREN
Step 2: Load write buffer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 3: Repeat for all but the last two bytes. Any unused locations should be filled with FFFFh.		
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
Step 4: Load write buffer for last two bytes.		
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
To continue writing data, repeat steps 2 through 4, where the Address Pointer is incremented by 2 at each iteration of the loop.		

FIGURE 3-4: PROGRAM CODE MEMORY FLOW

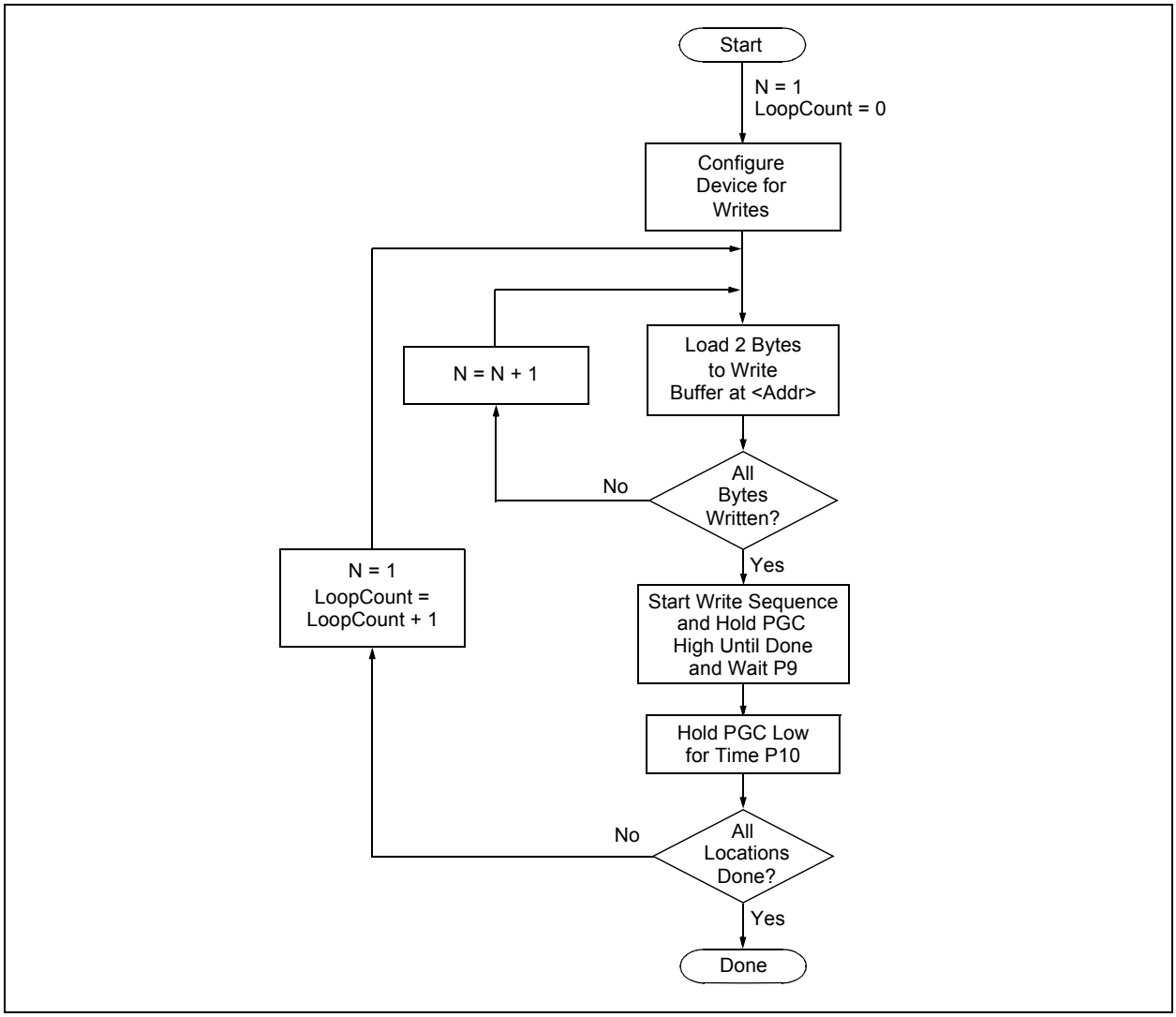
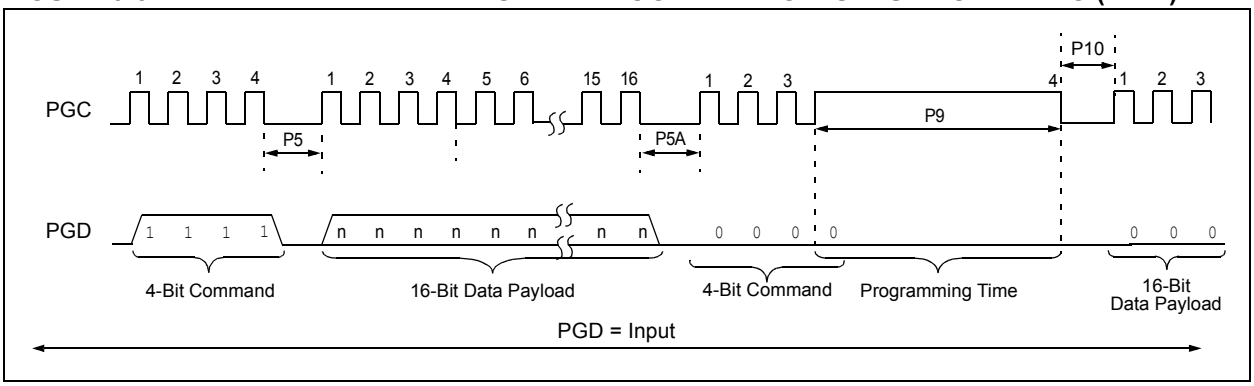


FIGURE 3-5: TABLE WRITE AND START PROGRAMMING INSTRUCTION TIMING (1111)



3.2.1 MODIFYING CODE MEMORY

The previous programming example assumed that the device had been Bulk Erased prior to programming. It may be the case, however, that the user wishes to modify only a section of an already programmed device.

The appropriate number of bytes required for the erase buffer must be read out of code memory (as described in **Section 4.2 "Verify Code Memory and Configuration Word"**) and buffered. Modifications can be made on this buffer. Then, the block of code memory that was read out must be erased and rewritten with the modified data. The code sequence is shown in Table 3-4.

The WREN bit must be set if the WR bit in EECON1 is used to initiate a write sequence.

3.2.2 CONFIGURATION WORD PROGRAMMING

Since the Flash Configuration Words are stored in program memory, they are programmed as if they were program data. Refer to **Section 3.2 "Code Memory Programming"** and **Section 3.2.1 "Modifying Code Memory"** for methods and examples on programming or modifying program memory. See also **Section 5.0 "Configuration Word"** for additional information on the Configuration Words.

TABLE 3-4: MODIFYING CODE MEMORY

4-Bit Command	Data Payload	Core Instruction
Step 1: Set the Table Pointer for the block to be erased.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Enable memory writes and set up an erase.		
0000	84 A6	BSF EECON1, WREN
0000	88 A6	BSF EECON1, FREE
Step 3: Initiate erase.		
0000	82 A6	BSF EECON1, WR
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
Step 4: Load write buffer. The correct bytes will be selected based on the Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW <Addr[21:16]>
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[8:15]>	MOVLW <Addr[8:15]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
1101	<MSB><LSB>	Write 2 bytes and post-increment address by 2.
.	.	
.	.	Repeat write operation 30 more times to fill the write buffer
.	.	
1111	<MSB><LSB>	Write 2 bytes and start programming.
0000	00 00	NOP - hold PGC high for time P9 and low for time P10.
Step 5: Repeat Step 4 for a total of 16 times, to completely rewrite the 1024 bytes of the erase buffer.		
Step 6: To continue modifying data, repeat Steps 1 through 4, where the Address Pointer is incremented by 1024 bytes at each iteration of the loop.		
Step 7: Disable writes.		
0000	94 A6	BCF EECON1, WREN

4.0 READING THE DEVICE

4.1 Read Code Memory

Code memory is accessed one byte at a time via the 4-bit command, '1001' (table read, post-increment). The contents of memory pointed to by the Table Pointer (TBLPTRU:TBLPTRH:TBLPTRL) are serially output on PGD.

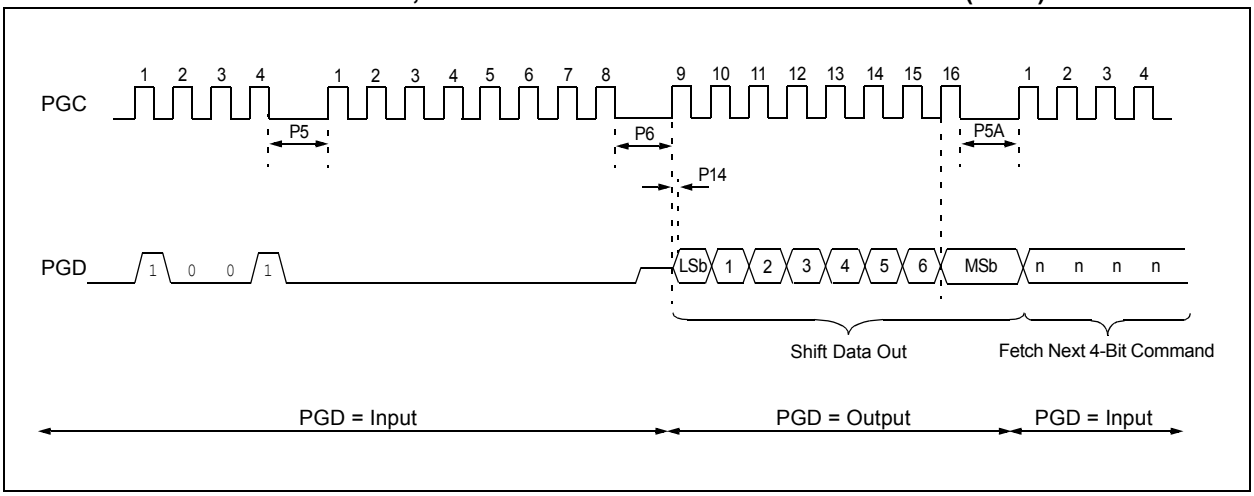
The 4-bit command is shifted in LSb first. The read is executed during the next 8 clocks, then shifted out on PGD during the last 8 clocks, LSb to MSb. A delay of P6 must be introduced after the falling edge of the 8th PGC of the operand to allow PGD to transition from an input to an output. During this time, PGC must be held low (see Figure 4-1). This operation also increments the Table Pointer by one, pointing to the next byte in code memory for the next read.

This technique will work to read any memory in the 000000h to 3FFFFFh address space, so it also applies to reading the Configuration registers.

TABLE 4-1: READ CODE MEMORY SEQUENCE

4-Bit Command	Data Payload	Core Instruction
Step 1: Set Table Pointer.		
0000	0E <Addr[21:16]>	MOVLW Addr[21:16]
0000	6E F8	MOVWF TBLPTRU
0000	0E <Addr[15:8]>	MOVLW <Addr[15:8]>
0000	6E F7	MOVWF TBLPTRH
0000	0E <Addr[7:0]>	MOVLW <Addr[7:0]>
0000	6E F6	MOVWF TBLPTRL
Step 2: Read memory and then shift out on PGD, LSb to MSb.		
1001	00 00	TBLRD *+

FIGURE 4-1: TABLE READ, POST-INCREMENT INSTRUCTION TIMING (1001)



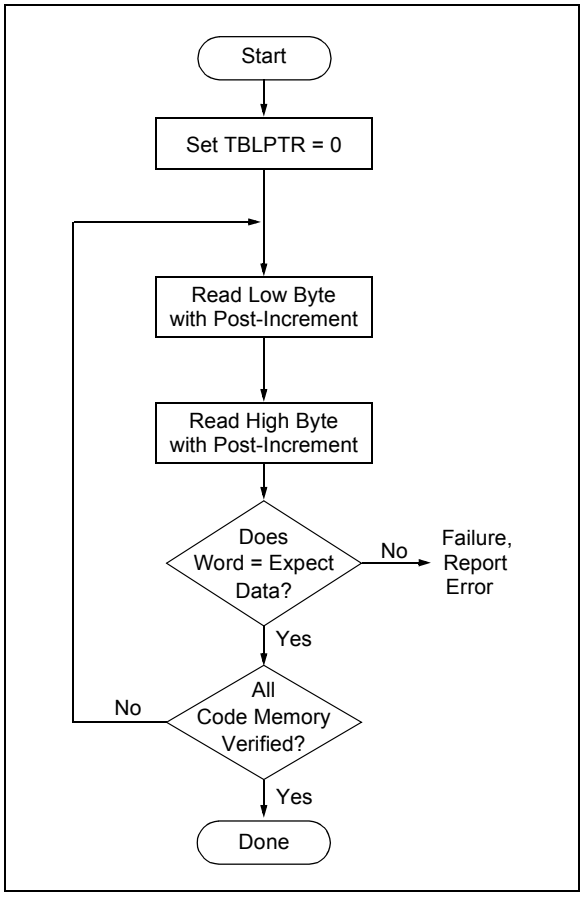
4.2 Verify Code Memory and Configuration Word

The verify step involves reading back the code memory space and comparing it against the copy held in the programmer's buffer. Because the Flash Configuration Words are stored in the top of program memory, it is verified with the rest of the code at this time.

The verify process is shown in the flowchart in Figure 4-2. Memory reads occur a single byte at a time, so two bytes must be read to compare against the word in the programmer's buffer. Refer to **Section 4.1 "Read Code Memory"** for implementation details of reading code memory.

Note:	Because the Flash Configuration Word contains the device code protection bit, code memory should be verified immediately after writing if code protection is enabled. This is because the device will not be readable or verifiable if a device Reset occurs after the Flash Configuration Word (and the CP0 bit) has been cleared.

FIGURE 4-2: VERIFY CODE MEMORY FLOW



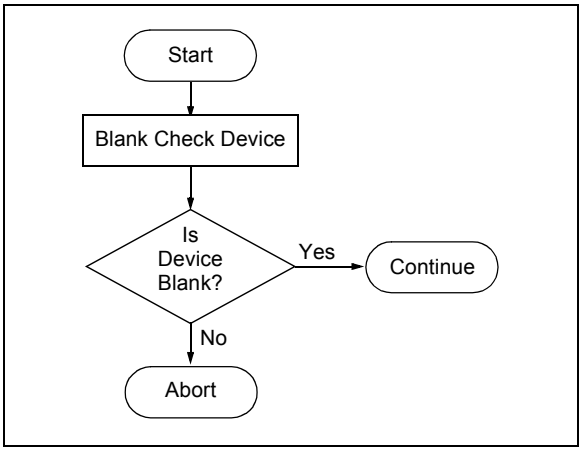
4.3 Blank Check

The term "Blank Check" means to verify that the device has no programmed memory cells. All memories must be verified: code memory and Configuration bits. The Device ID registers (3FFFFEh:3FFFFFh) should be ignored.

A "blank" or "erased" memory cell will read as a '1', so Blank Checking a device merely means to verify that all bytes read as FFh. The overall process flow is shown in Figure 4-3.

Given that Blank Checking is merely code verification with FFh expect data, refer to **Section 4.2 "Verify Code Memory and Configuration Word"** for implementation details.

FIGURE 4-3: BLANK CHECK FLOW



5.0 CONFIGURATION WORD

The Configuration Words of the PIC18F45J10 family devices are implemented as volatile memory registers. All of the Configuration registers (CONFIG1L, CONFIG1H, CONFIG2L, CONFIG2H, CONFIG3L and CONFIG3H) are automatically loaded following each device Reset.

The data for these registers is taken from the four Flash Configuration Words located at the top of program memory. Configuration data is stored in order, starting with CONFIG1L in the lowest Flash address and ending with CONFIG4H in the highest. The mapping to specific Configuration Words is shown in Table 5-1. While four words are reserved in program memory, only three words (CONFIG1L through CONFIG3H) are used for device configuration. Users should always reserve these locations for Configuration Word data and write their application code accordingly.

The upper four bits of each Configuration Word should always be stored in program memory as '1111'. This is done so these program memory addresses will always be '1111 xxxx xxxx xxxx' and interpreted as a NOP instruction if they were ever to be executed. Because the corresponding bits in the Configuration Word are unimplemented, they will not be written to.

The Configuration and Device ID registers are summarized in Table 5-2. A listing of the individual Configuration bits and their options is provided in Table 5-3.

TABLE 5-1: MAPPING OF THE FLASH CONFIGURATION WORDS TO THE CONFIGURATION REGISTERS

Configuration Byte	Code Space Address(1)	Configuration Register Address
CONFIG1L	XFF8h	300000h
CONFIG1H	XFF9h	300001h
CONFIG2L	XFFAh	300002h
CONFIG2H	XFFBh	300003h
CONFIG3L	XFFCh	300004h
CONFIG3H	XFFDh	300005h
CONFIG4L(2)	XFFEh	300006h
CONFIG4H(2)	XFFFh	300007h

Note 1: See Table 2-2 for the complete addresses within code space for specific devices and memory sizes.

2: Unimplemented in PIC18F45J10 family devices.

TABLE 5-2: CONFIGURATION BITS AND DEVICE IDs

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300000h	CONFIG1L	$\overline{\text{DEBUG}}$	XINST	STVREN	—	—	—	—	WDTEN	111- ---1
300001h	CONFIG1H	—(1)	—(1)	—(1)	—(1)	—(2)	CP0	—	—	---- 01--
300002h	CONFIG2L	IESO	FCMEN	—	—	—	FOSC2	FOSC1	FOSC0	11-- -111
300003h	CONFIG2H	—(1)	—(1)	—(1)	—(1)	WDTPS3	WDTPS2	WDTPS1	WDTPS0	---- 1111
300005h	CONFIG3H	—(1)	—(1)	—(1)	—(1)	—	—	—	CCP2MX	---- ---1
3FFFFEh	DEVID1(3)	DEV2	DEV1	DEV0	REV4	REV3	REV2	REV1	REV0	See Table 5-4
3FFFFFh	DEVID2(3)	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	See Table 5-4

Legend: - = unimplemented. Shaded cells are unimplemented, read as '0'.

Note 1: The value of these bits in program memory should always be '1'. This ensures that the location is executed as a NOP if it is accidentally executed.

2: This bit should always be maintained at '0'.

3: DEVID registers are read-only and cannot be programmed by the user.

TABLE 5-3: PIC18F45J10 FAMILY BIT DESCRIPTIONS

Bit Name	Configuration Words	Description
$\overline{\text{DEBUG}}$	CONFIG1L	Background Debugger Enable bit 1 = Background debugger disabled, RB6 and RB7 configured as general purpose I/O pins 0 = Background debugger enabled, RB6 and RB7 are dedicated to in-circuit debug
XINST	CONFIG1L	Extended Instruction Set Enable bit 1 = Instruction set extension and Indexed Addressing mode enabled 0 = Instruction set extension and Indexed Addressing mode disabled (Legacy mode)
STVREN	CONFIG1L	Stack Overflow/Underflow Reset Enable bit 1 = Reset on stack overflow/underflow enabled 0 = Reset on stack overflow/underflow disabled
WDTEN	CONFIG1L	Watchdog Timer Enable bit 1 = WDT enabled 0 = WDT disabled (control is placed on SWDTEN bit)
CP0	CONFIG1H	Code Protection bit 1 = Program memory is not code-protected 0 = Program memory is code-protected
IESO	CONFIG2L	Internal/External Oscillator Switchover bit 1 = Oscillator Switchover mode enabled 0 = Oscillator Switchover mode disabled
FCMEN	CONFIG2L	Fail-Safe Clock Monitor Enable bit 1 = Fail-Safe Clock Monitor enabled 0 = Fail-Safe Clock Monitor disabled
FOSC2	CONFIG2L	Default Oscillator Select bit 1 = Clock designated by FOSC1:FOSC0 is enabled as system clock when OSCCON<1:0> = 00 0 = INTRC is enabled as system clock when OSCCON<1:0> = 00
FOSC1:FOSC0	CONFIG2L	Primary Oscillator Select bits 11 = EC oscillator, PLL enabled and under software control, CLKO function on OSC2 10 = EC oscillator, CLKO function on OSC2 01 = HS oscillator, PLL enabled and under software control 00 = HS oscillator
WDTPS3:WDTPS0	CONFIG2H	Watchdog Timer Postscale Select bits 1111 = 1:32,768 1110 = 1:16,384 1101 = 1:8,192 1100 = 1:4,096 1011 = 1:2,048 1010 = 1:1,024 1001 = 1:512 1000 = 1:256 0111 = 1:128 0110 = 1:64 0101 = 1:32 0100 = 1:16 0011 = 1:8 0010 = 1:4 0001 = 1:2 0000 = 1:1
CCP2MX	CONFIG3H	CCP2 Mux bit 1 = CCP2 is multiplexed with RC1 0 = CCP2 is multiplexed with RB3

5.1 Device ID Word

The device ID word for the PIC18F45J10 family devices is located at 3FFFFEh:3FFFFFh. These read-only bits may be used by the programmer to identify what device type is being programmed and read out normally, even after code or read-protected. The process for reading the device IDs is shown in Figure 5-1. A complete list of device ID values for the PIC18F45J10 family is presented in Table 5-4.

FIGURE 5-1: READ DEVICE ID WORD FLOW

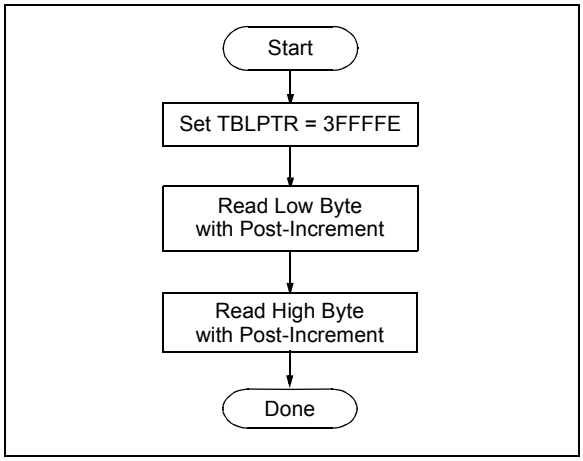


TABLE 5-4: DEVICE ID VALUE

Device	Device ID Value	
	DEVID2	DEVID1
PIC18F24J10	1Dh	000x xxxx
PIC18F25J10	1Ch	000x xxxx
PIC18F44J10	1Dh	001x xxxx
PIC18F45J10	1Ch	001x xxxx
PIC18LF24J10	1Dh	010x xxxx
PIC18LF25J10	1Ch	010x xxxx
PIC18LF44J10	1Dh	011x xxxx
PIC18LF45J10	1Ch	011x xxxx

5.2 Checksum Computation

The checksum is calculated by summing the contents of all code memory locations and the device Configuration Words, appropriately masked. The Least Significant 16 bits of this sum are the checksum.

The checksum calculation differs depending on whether or not code protection is enabled. Since the code memory locations read out differently depending on the code-protect setting, the table describes how to manipulate the actual code memory values to simulate the values that would be read from a protected device. When calculating a checksum by reading a device, the entire code memory can simply be read and summed. The Configuration Words can always be read.

Table 5-5 describes how to calculate the checksum for each device.

TABLE 5-5: CHECKSUM COMPUTATION

Device	Code Protection	Checksum
PIC18F24J10 PIC18F44J10	Off	SUM[000000:003FF7] + ([003FF8] & E1h) + ([003FF9] & 04h) + ([003FFA] & C7h) + ([003FFB] & 0Fh) + ([003FFD] & 01h)
	On	0000h
PIC18F25J10 PIC18F45J10	Off	SUM[000000:007FF7] + ([007FF8] & E1h) + ([007FF9] & 04h) + ([007FFA] & C7h) + ([007FFB] & 0Fh) + ([007FFD] & 01h)
	On	0000h

Legend: [a] = Value at address a; SUM[a:b] = Sum of locations a to b inclusive; + = Addition; & = Bitwise AND. All addresses are hexadecimal.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Symbol	Characteristic		Min	Max	Units	Conditions
	VDDCORE	External Supply Voltage for Microcontroller Core		2.00	2.75	V	**(Note 1)**
D111	VDD	Supply Voltage During Programming	PIC18**LF**XXJXX	2.25	3.60	V	Normal programming **(Note 2)**
			PIC18**F**XXJXX	2.70	3.60	v	
D112	IPP	Programming Current on $\overline{MCLR}$		—	5	μA	
D113	IDDP	Supply Current During Programming		—	10	mA	
D031	VIL	Input Low Voltage		VSS	0.2 VDD	V	
D041	VIH	Input High Voltage		0.8 VDD	VDD	V	
D080	VOL	Output Low Voltage		—	0.4	V	IOL = 3.4 mA @ 3.3V
D090	VOH	Output High Voltage		2.4	—	V	IOH = -2.0 mA @ 3.3V
D012	CIO	Capacitive Loading on I/O pin (PGD)		—	50	pF	To meet AC specifications
	CF	Filter Capacitor Value on VCAP		1	10	μF	Required for controller core operation on PIC18F2XJ10/4XJ10 devices

Note 1: VDDCORE must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 "PIC18FXXJ10/LFXXJ10 Devices and the On-Chip Voltage Regulator"** for more information.

2: VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

6.0 AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY TEST MODE (CONTINUED)

Standard Operating Conditions
Operating Temperature: 25°C is recommended

Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
P1	TR	$\overline{MCLR}$ Rise Time to Enter Program/Verify mode	—	1.0	μs	
P2	TPGC	Serial Clock (PGC) Period	100	—	ns	
P2A	TPGCL	Serial Clock (PGC) Low Time	40	—	ns	
P2B	TPGCH	Serial Clock (PGC) High Time	40	—	ns	
P3	TSET1	Input Data Setup Time to Serial Clock ↓	15	—	ns	
P4	THLD1	Input Data Hold Time from PGC ↓	15	—	ns	
P5	TDLY1	Delay Between 4-Bit Command and Command Operand	40	—	ns	
P5A	TDLY1A	Delay Between 4-Bit Command Operand and Next 4-Bit Command	40	—	ns	
P6	TDLY2	Delay Between Last PGC ↓ of Command Byte to First PGC ↑ of Read of Data Word	20	—	ns	
P9	TDLY5	PGC High Time (minimum programming time)	10	—	ms	
P10	TDLY6	PGC Low Time after Programming	400	—	ns	
P11	TDLY7	Delay to allow Bulk Erase to Occur	400	—	ms	
P12	THLD2	Input Data Hold Time from $\overline{MCLR}$ ↑	400	—	μs	
P13	TSET2	VDD ↑ Setup Time to $\overline{MCLR}$ ↑	100	—	ns	
P14	TVALID	Data Out Valid from PGC ↑	10	—	ns	
P16	TDLY8	Delay Between Last PGC ↓ and $\overline{MCLR}$ ↓	0	—	s	
P17	THLD3	$\overline{MCLR}$ ↓ to VDD ↓	—	100	ns	
P19	TKEY1	Delay from First $\overline{MCLR}$ ↓ to First PGC ↑ for Key Sequence on PGD	40	—	ns	
P20	TKEY2	Delay from Last PGC ↓ for Key Sequence on PGD to Second $\overline{MCLR}$ ↑	40	—	ns	

Note 1: VDDCORE must be supplied to the VDDCORE/VCAP pin if the on-chip voltage regulator is disabled. See **Section 2.1.1 "PIC18FXXJ10/LFXXJ10 Devices and the On-Chip Voltage Regulator"** for more information.

2: VDD must also be supplied to the AVDD pins during programming. AVDD and AVSS should always be within ±0.3V of VDD and VSS, respectively.

NOTES:

Note the following details of the code protection feature on Microchip devices:

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