Translation of an Existing VMM-based SystemVerilog Testbench to OVM

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ABSTRACT

Many features built into the SystemVerilog language make it an extremely effective high-level verification language. Using class libraries with SystemVerilog can take this a step further by enhancing productivity, and enabling better, more efficient reuse between engineers and between projects. The Verification Methodology Manual (VMM) class library was one of the first SystemVerilog class libraries available, and has been widely adopted. The Open Verification Methodology (OVM) class library has just recently become available, and while it is similar to VMM in many respects, there are also some important differences. This paper will describe the process of converting an existing testbench based on VMM class libraries, to one based on OVM class libraries.

The VMM testbench selected for the conversion to OVM was developed for the verification of a custom memory controller for a general purpose DSP SOC. The EBIU (External Bus Interface Unit) is complex enough to require a non-trivial testbench, and the large number of system busses makes it an interesting candidate for a randomized SystemVerilog testbench approach.

This paper will begin by describing the conversion process of the basic testbench components, including transaction classes and bus functional models. The next step is converting the testbench environment, and adding the extra layers of abstraction which are part of the OVM methodology. Finally, the conversion of the actual tests is described, including the configuration phase, and the transaction generation. The paper will conclude by summarizing the similarities and differences between the two approaches, and highlight which aspects of the conversion were straight forward, and which aspects required more attention.

Categories and Subject Descriptors

B.5.2 [**Register-Transfer-Level Implementation**]: Design Aids – *verification.*

General Terms

Verification

Keywords

SystemVerilog, VMM, OVM, Testbenches

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