Vishay Siliconix

N-Channel 30 V (D-S) 175 °C MOSFET

Top View

Bottom View

PRODUCT SUMMARY					
V _{DS} (V)	30				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 10 \text{ V}$	0.00047				
$R_{DS(on)}$ max. (Ω) at $V_{GS} = 4.5 \text{ V}$	0.00068				
Q _g typ. (nC)	54.3				
I _D (A)	421 ^a				
Configuration	Single				

FEATURES

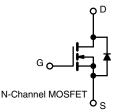
- TrenchFET® Gen V power MOSFET
- Very low R_{DS} x Q_g figure-of-merit (FOM)



- Enables higher power density with very low R_{DS(on)} and thermally enhanced compact package
- 100 % R_q and UIS tested
- Material categorization: for definitions of compliance please see <u>www.vishay.com/doc?99912</u>

APPLICATIONS

- DC/DC converter
- POL
- · Synchronous rectification
- · Power and load switch
- Battery management



ORDERING INFORMATION	
Package	PowerPAK SO-8DC
Lead (Pb)-free and halogen-free	SiDR500EP-T1-RE3

PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-source voltage		V _{DS}	30	V	
Gate-source voltage		V _{GS}	+16 / -12	V	
	T _C = 25 °C		421		
Continuous drain current (T _J = 150 °C)	T _C = 70 °C	1. —	352		
	T _A = 25 °C	I _D	94 b, c		
	T _A = 70 °C	1 -	78 ^{b, c}		
Pulsed drain current (t = 100 μs)		I _{DM}	500	A	
Continuous source-drain diode current	T _C = 25 °C		136		
	T _A = 25 °C	ls s	95 ^{b, c}		
Single pulse avalanche current		I _{AS}	50		
Single pulse avalanche energy L = 0.1 mH		E _{AS}	125	mJ	
	T _C = 25 °C		150		
Marriagona a consequidada de estada	T _C = 70 °C	1 5 -	105	14/	
Maximum power dissipation	T _A = 25 °C	P _D	7.5 ^{b, c}	- W	
	T _A = 70 °C	†	5.25 ^{b, c}		
Operating junction and storage temperature range		T _J , T _{stg}	-55 to +175	%0	
Soldering recommendations (peak temperature) c			260	°C	

THERMAL RESISTANCE RATI	NGS				
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient ^b	t ≤ 10 s	R _{thJA}	15	20	
Maximum junction-to-case (drain)	Steady state	R_{thJC}	0.8	1	°C/W
Maximum junction-to-case (source)	Steady state	R_{thJC}	1.1	1.4	

Notes

- a. $T_C = 25$ °C
- b. Surface mounted on 1" x 1" FR4 board
- c. t = 10 s
- d. See solder profile (www.vishav.com/doc?73257). The PowerPAK SO-8DC is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- f. Maximum under steady state conditions is 54 °C/W

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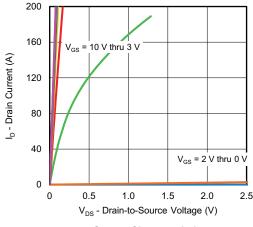
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_{D} = 1 \text{ mA}$	30	-	-	V
V _{DS} temperature coefficient	$\Delta V_{DS}/T_{J}$	I _D = 10 mA	-	20	-	>//00
V _{GS(th)} temperature coefficient	$\Delta V_{GS(th)}/T_J$	I _D = 250 μA	-	-0.42	-	mV/°C
Gate-source threshold voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	-	2.2	V
Gate-source leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = +16 V, -12 V	-	-	± 100	nA
Zana mata waltana alumin awanant		V _{DS} = 24 V, V _{GS} = 0 V	-	-	1	
Zero gate voltage drain current	I _{DSS}	V _{DS} = 24 V, V _{GS} = 0 V, T _J = 70 °C	-	-	15	μA
D		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	0.00039	0.00047	
Drain-source on-state resistance a	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	0.00057	0.00068	Ω
Forward transconductance a	9 _{fs}	$V_{DS} = 15 \text{ V}, I_{D} = 20 \text{ A}$	-	210	-	S
Dynamic ^b			1			
Input capacitance	C _{iss}		-	8960	-	
Output capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	2990	-	pF
Reverse transfer capacitance	C _{rss}		-	168	-	
		$V_{DS} = 15 \text{ V}, V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$	-	120	180	
Total gate charge	Qg	, 40 , 5	-	54.3	82	nC
Gate-source charge	Q _{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$	-	25.6	-	
Gate-drain charge	Q _{gd}		-	8.7	-	
Output charge	Q _{oss}	V _{DS} = 15 V, V _{GS} = 0 V	-	105	-	
Gate resistance	R_g	f = 1 MHz	0.4	0.9	1.6	Ω
Turn-on delay time	t _{d(on)}		-	18	36	
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 0.75 \Omega$	-	11	22	1
Turn-off delay time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 10 \text{ V}, R_g = 1 \Omega$	-	47	94	
Fall time	t _f		-	11	22	1
Turn-on delay time	t _{d(on)}		-	47	94	ns
Rise time	t _r	$V_{DD} = 15 \text{ V}, R_{L} = 0.75 \Omega$	-	102	200	
Turn-off delay time	t _{d(off)}	$I_D \cong 20 \text{ A}, V_{GEN} = 4.5 \text{ V}, R_g = 1 \Omega$	-	50	100	
Fall time	t _f		-	20	40	
Drain-Source Body Diode Characteristic	s					
Continuous source-drain diode current	I _S	T _C = 25 °C	-	-	136	^
Pulse diode forward current ($t_p = 100 \mu s$)	I _{SM}		-	-	500	A
Body diode voltage	V _{SD}	I _S = 10 A	-	0.69	1.1	V
Body diode reverse recovery time	t _{rr}		-	65	130	ns
Body diode reverse recovery charge	Q _{rr}			86	172	nC
Reverse recovery fall time	t _a	T _J = 25 °C	-	34	-	
Reverse recovery rise time	t _b		-	31	-	ns

Notes

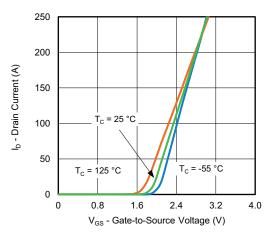
- g. Pulse test; pulse width $\leq 300~\mu s,~duty~cycle \leq 2~\%$
- h. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

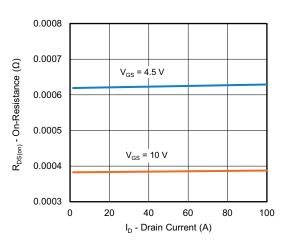




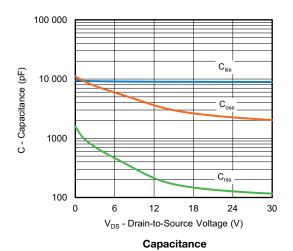


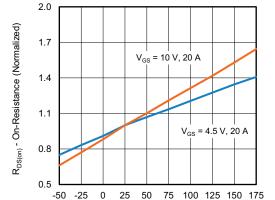


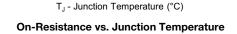
Transfer Characteristics

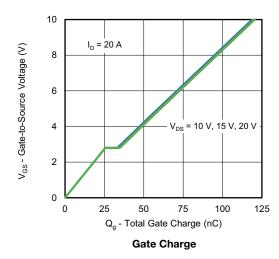


On-Resistance vs. Drain Current and Gate Voltage

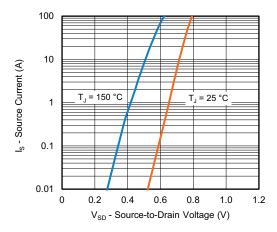




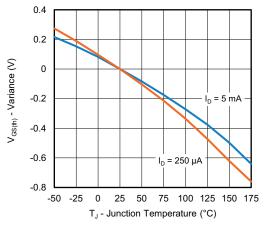




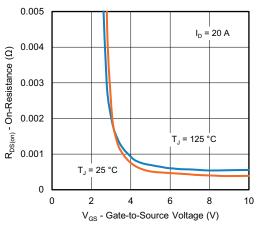




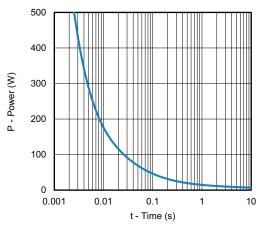
Source-Drain Diode Forward Voltage



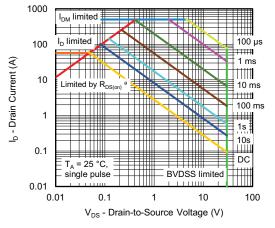
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage

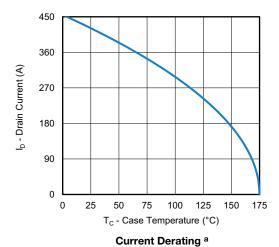


Single Pulse Power, Junction-to-Ambient



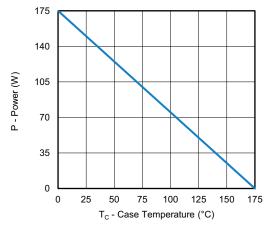
Safe Operating Area, Junction-to-Ambient



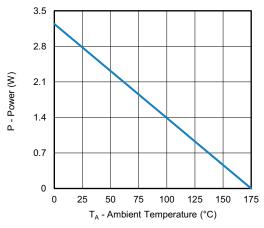


Nota

a. The power dissipation P_D is based on T_J max. = 175 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

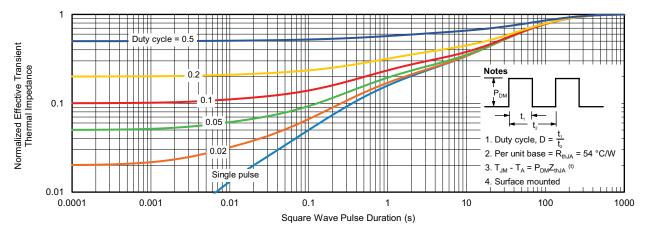


Power, Junction-to-Case

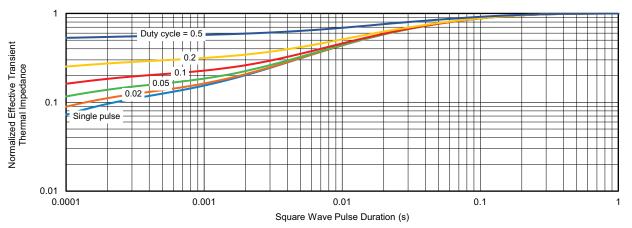


Power, Junction-to-Ambient





Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?63158.



PowerPAK® SO-8 Double Cooling Case Outline





DIM.	MILLIMETERS			INCHES			
DIM.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	
Α	0.51	0.56	0.61	0.020	0.022	0.024	
A1	0.00	0.02	0.05	0.000	0.001	0.002	
b	0.36	0.41	0.46	0.014	0.016	0.018	
С	0.15	0.20	0.25	0.006	0.008	0.010	
D	4.90	5.00	5.10	0.193	0.197	0.201	
D1	3.71	3.76	3.81	0.146	0.148	0.150	
е		1.27 BSC			0.050 BSC		
E	5.90	6.00	6.10	0.232	0.236	0.240	
E1	3.60	3.65	3.70	0.142	0.144	0.146	
E2	0.46 typ.			0.018 typ.			
Н	0.49	0.54	0.59	0.019	0.021	0.023	
K	1.22	1.27	1.32	0.048	0.050	0.052	
K1		0.64 typ.		0.025 typ.			
L	0.49	0.54	0.59	0.019	0.021	0.023	
M1	3.8	3.90	4.00	0.150	0.154	0.158	
M2	2.69	2.79	2.89	0.106	0.110	0.114	
МЗ	1.01	1.11	1.21	0.040	0.044	0.048	
M4	0.56 typ.			0.022 typ.			
N		8		8			
T1	4.46	4.56	4.66	0.176	0.180	0.184	
T2	2.53	2.63	2.73	0.100	0.104	0.108	
T3	1.83	1.93	2.03	0.072	0.076	0.080	
T4	0.97 typ.			0.038 typ.			
T5	0.48 typ.			0.019 typ.			
N: T24-0304-R G: 6048	ev. C, 29-Jul-2024						

Revison: 29-Jul-2024 1 Document Number: 75846



RECOMMENDED MINIMUM PADS FOR PowerPAK® SO-8 Single



Recommended Minimum Pads Dimensions in Inches/(mm)

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APPLICATION NOTE



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