IET Circuits, Devices & Systems

Research Article

IET Journals
The Institution of Engineering and Technology

Integer-*N* charge pump phase locked loop for 2.4 GHz application with a novel design of phase frequency detector

ISSN 1751-858X
Received on 5th May 2019
Revised 17th August 2019
Accepted on 2nd October 2019
E-First on 13th January 2020
doi: 10.1049/iet-cds.2019.0189
www.ietdl.org

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Abstract: In this article, a novel design is presented, for an Integer-*N* charge pump phase locked loop (PLL). The design is with a resetless phase frequency detector, and with the differential design of charge pump. The voltage-controlled oscillator is of current starved type. The proposed PLL is not having any blind zone and is having near-zero dead zone. When compared to the conventional design, the current mismatch in the charge pump is reduced by 3.21%, and the lock time of the PLL is reduced by 79%. The PLL is intended for 2.4 GHz application, and the obtained lock time is 1.7 µs. The implementation is done with the three-stage ring oscillator, with divider of modulus as 24, in 180 nm TSMC technology. At 1.8 V supply voltage, the circuit consumes 9.72 mW of power.

1 Introduction

In any electronic communication system, phase locked loop (PLL) is an essential component. In digital systems, it is used for clock data recovery, and in hybrid transceiver systems, it is used for frequency multiplication. Apart from these usages, it is also used for phase synchronisation. Out of the various architectures that are available for a PLL, the charge pump PLL (CP-PLL) remains a motivation as of now, as it provides a highly stable source for the operating frequency of an electronic system with the following characteristics: lesser phase noise, lesser spur, lesser lock time, larger tuning range. In addition, the communication industry requires this radio frequency (RF) source with the following features: compact layout, lesser power consumption, suitable for IEEE 802.11 applications, scalable technology. In Fig. 1 the general and traditional diagram of CP-PLL is shown.

The RF output produced by the voltage-controlled oscillator (VCO) contains phase noise, because of the device noises as well as the switching noises that are within the VCO. For reducing the phase noise, the output frequency of VCO is divided with a certain modulus. An external highly stable frequency is used as reference, for comparison with the divided output, and PFD is made use of, for this purpose. For the lagging or leading outputs of the VCO, the PFD produces UP or DOWN pulses, respectively, which are utilised at the CP to source or to sink current. These current pulses are filtered and then are converted into voltage. This DC waveform is used as control voltage to the VCO, to bring the RF output back into phase; thus the CP-PLL's output achieves phase lock. Here, if the divider modulus is larger, it takes a longer time for the loop to lock. The lock time can be reduced by using fractional-*N* architecture, which uses a smaller divider ratio; but as the switching becomes faster, additional spurs get introduced at the output, for which spur reduction techniques need to be employed. Hence, for low-frequency applications, Integer-*N* architecture is preferred [1–4].

For charging and discharging of the loop filter capacitor, the CP sources and sinks the current respectively. For this purpose, two D flip–flops generate the required pulses, as shown in Fig. 2. The flip–flops are reset, when both UP and DOWN pulses attain the state '1', and the AND gate is used to produce the reset signal. The small delay t_d is introduced to avoid the dead zone, at the AND gate's output. In order to overcome dead zone, this delay should be long enough. However, in order to have control of the output of the VCO, this delay should be short enough [5, 6]. Therefore, the choice of this particular delay is critical for the design of conventional PFD.

The requirement is that the control voltage for the VCO should be smooth enough, such that the VCO output does not contain considerable spur content. Primarily, the mismatch between the charge and discharge currents is the cause for the ripple in the control voltage of the VCO. The switching of metal oxide semiconductor field-effect transistors (MOSFETs) causes non-ideal effects in the CP, named as charge injection, charge sharing and clock feedthrough. These effects occur because of the parasitic capacitances of the switches. Therefore, to have a smooth control voltage for the VCO, it is necessary to arrive at an effective design of CP. Many techniques in the literature have been reported, for the purpose of reducing the current mismatch in CP.

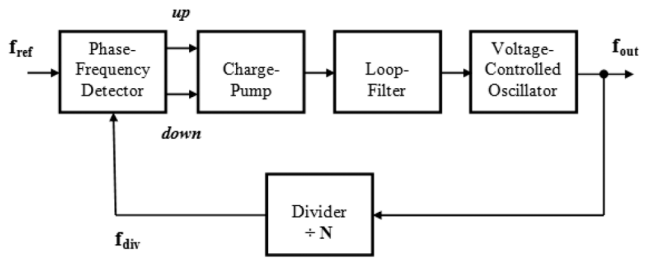

Fig. 1 *General block diagram of a CP-PLL*

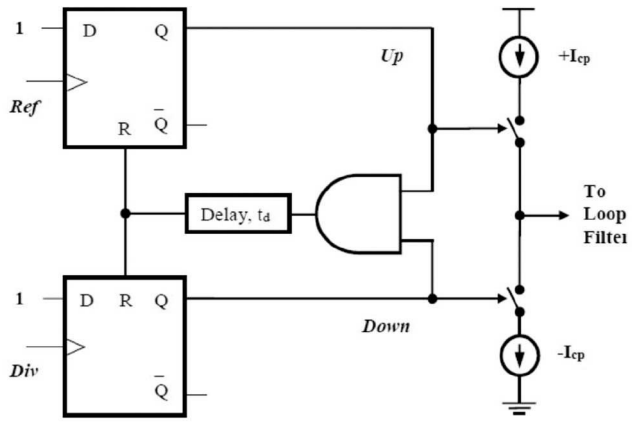

Fig. 2 *Generic diagram of PFD with CP*

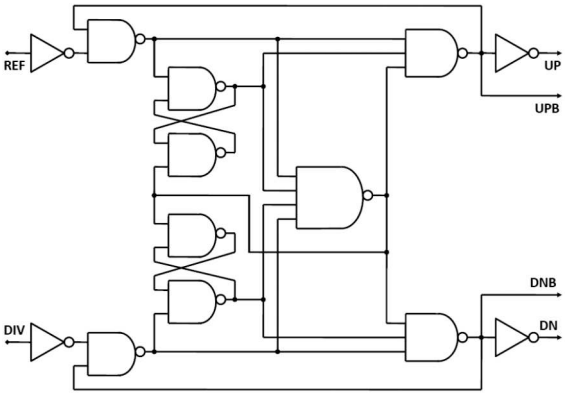

Fig. 3 *Circuit diagram of conventional PFD*

This article is organised as follows: the literature survey related to the PLL architecture and design is dealt with, in Section 2. The design of the novel PFD is discussed in Section 3. Similarly, Section 4 discusses the designs of CP and VCO. For the complete block diagram of the PLL, Section 5 elaborates the results of simulation. Section 6 concludes the results, along with the discussion of future work.

2 Related previous work

The two terms, blind zone and dead zone, are of specific interest, with respect to the performance of the PFD. These two zones correspond to the time lag between the phase difference of inputs and the control voltage of VCO. This time lag, in turn, increases the lock time of the PLL. The definition of Blind zone is the insensitivity of the PFD for any transitions at the input. The PFD is not active for the inputs during its reset condition, and this leads to a minute time lag. Further, the definition of dead zone is the minimum width of the output pulse that is required to turn the CP on. Therefore, unlike blind zone, the time duration of dead zone depends on the bandwidth of the loop.

There have been substantial efforts put forth by the researchers to tackle both of these issues. For the reduction of the blind zone, dynamic design of the flip–flop and the reordering of the NAND inputs had been tried out [7, 8]. However, this did not reduce the dead zone duration. To tackle this problem, frequency-to-digital converter and high-resolution phase detector were made use of [9, 10]. These solutions are more complicated, and they also do not solve the issue fully. To combat both of the issues, PFD design without the reset signal had been implemented and has been proved to be quite satisfactory [11]. However, as the solution offered is for dynamic design, it is suitable only for high-speed applications. By means of the utilisation of the device parasitic capacitances, the open-loop configuration is also suggested [12]. A suitable solution is required for static designs as well.

With the design of CP, there are three charge related issues mentioned earlier, which cause the current mismatch. Charge injection occurs because of the ON to OFF state switching of the MOSFET, whereas charge sharing occurs because of the OFF to ON state switching. Within the MOSFET, the finite rise, as well as, fall times of the gate pulses results in clock feedthrough. To reduce these non-ideal effects, cascode topology was used, which also helped in reducing the reference spurs. To reduce the effect of clock feedthrough, transmission gates were utilised; this topology was enhanced further, by making use of the self-biased current mirror [13, 14].

In addition to the three issues mentioned above, the channel length modulation also causes the current mismatch in CP. When the UP pulse is high, the increase in control voltage causes reduction in source current. To circumvent this problem, the charge pump was split into two branches, and an opamp was used as a buffer between the two branches [15]. This method of current steering was enhanced and improved, by using adaptive body bias tuning, and by reducing the threshold voltage of the p-MOSFET [16]. Alternatively, the opamp was used in open-loop configuration, and to eliminate the residual channel charges, dummy switches were included [17]. By including the miller compensation network, and by removing the dummy switches, this topology was improved in [18], along with the additional capacitors for glitch suppression.

Cascode configuration, current steering and open-loop configuration – these are the predominant techniques that are being utilised, for the current mismatch reduction. However, larger device dimensions are required with cascode configuration, and additional compensation circuitry is required with open loop configuration. In this particular work, a combination of these methods is utilised, so as to reduce the current mismatch in CP as well as to maintain stability.

Finally, as far as the design of VCO is concerned, it can be constructed using either LC oscillator or ring oscillator. LC oscillator has the advantage of lesser phase noise, whereas it consumes larger area because of the spiral inductor. In addition, it has a lesser frequency tuning range [19, 20]. Therefore, ring oscillator is chosen for the present application. The ring oscillator's output frequency value is primarily decided by the stage delay of each inverter [21]. Thus, any external RC components are not required with the ring oscillator, unless a low-frequency output is required with lesser number of stages. There have been two methods reported in the literature, for the computation of the stage delay: one is in terms of the dynamic current and the net capacitance [22–25], and the other is in terms of the total capacitance and the effective resistance [26, 27]. However, the submicron parasitic effects are not included in these models, as these models are primarily utilised with the micrometer device dimensions. Therefore, in our work, an effort has been made to model the ring oscillator for the submicron device dimensions.

3 Proposed PFD

In Fig. 3 the conventional circuit diagram that is used for the PFD is shown. D flip-flop is constituted by the cross-coupled 2-input NAND pair along with another cross-coupled set of 2-input and 3-input NAND gates. For the purpose of producing the reset signal, the 4-input NAND gate is made use of. Through the careful choice of its device dimensions, this particular NAND gate can also be utilised to generate the delay that is required to alleviate the dead zone problem. Alternatively, the required delay can also be generated by inserting additional buffers at the output of the 4-input NAND gate. However, this conventional circuit suffers from blind zone as well as dead zone, due to the limitations on the duration of the reset signal, which can neither be too long nor be too short.

As is evident, the design of PFD without the reset signal is definitely an advantage. Even though it is not possible to obtain a zero dead zone, achieving a near-zero dead zone is possible. A PFD circuit that does not contain reset signal is proposed herewith, and it facilitates zero blind zone. As this is a static one, it is suitable to be used with low-frequency applications as well. Here, an exclusive OR (EXOR) gate, along with two transmission gates, is utilised to capture the phase difference between the REF and DIV signals, and then to generate the UP and DN signals. During this difference in phase, two cross-coupled inverter cells are utilised to store the temporary levels of reference (REF) and division (DIV), which are called as L2 and L1, respectively. In Fig. 4 is shown the circuit diagram for the same.

The requirements for the generation of UP and DN, with respect to the input waveforms, are summarised in Table 1. The logical expressions for the computation of these signals are indicated below

$$\mathrm{UP} = \mathrm{REF} \cdot \mathrm{DIV} \cdot \overline{\mathrm{L1}} \cdot \mathrm{L2} + \overline{\mathrm{REF}} \cdot \overline{\mathrm{DIV}} \cdot \mathrm{L1} \cdot \overline{\mathrm{L2}} \quad (1)$$

$$\mathrm{DN} = \mathrm{REF} \cdot \mathrm{DIV} \cdot \mathrm{L1} \cdot \overline{\mathrm{L2}} + \overline{\mathrm{REF}} \cdot \overline{\mathrm{DIV}} \cdot \overline{\mathrm{L1}} \cdot \mathrm{L2} \quad (2)$$

When the EXOR output becomes 0, the stored levels are utilised to compute the output waveforms. This computation is intentionally avoided when the EXOR output is 1, because of the changes at the input affecting the output. As the circuits are designed as edge-

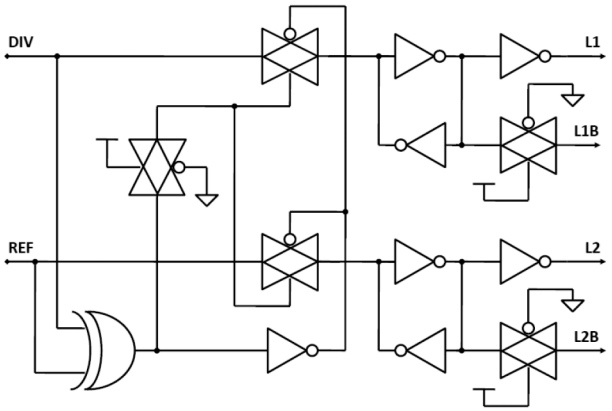

Fig. 4 *Capture of phase difference between REF and DIV*

Table 1 Generation of UP and DN with respect to the input

State	Edge	DIV	REF	L2	L1	DN	UP
lag	rising	1	1	1	0	0	1
lag	falling	0	0	0	1	0	1
lead	rising	1	1	0	1	1	0
lead	falling	0	0	1	0	1	0

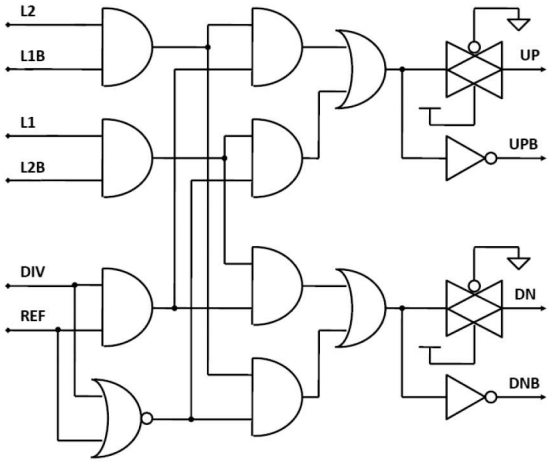

Fig. 5 *Generation of switching signals*

sensitive, the computation completes before the next edge transition. The circuit for this computation is shown in Fig. 5.

During both the edges of the input waveforms, the phase difference is detected. The complete circuit comprising of Figs. 4 and 5 detects the same, and thus consecutively generates the UP and DN signals. As the CP contains two limbs of switches, the complements of these signals are utilised for switching the counterpart transistors in the CP. The transmission gates are included in the circuit, so as to have an equal delay in between the true and complementary forms.

4 Designs of CP and VCO

As discussed earlier, when the outputs of the PFD are utilised in the CP, to turn the switches ON and OFF, the lagging or the leading state between the REF and DIV signals gets translated into source or sink current, which in turn is utilised by the loop filter to convert the same into a voltage waveform. The second order loop filter that is required for the generation of control voltage is designed as per the procedures that are discussed in [28]. The CP circuit is simulated as per the conventional design initially. The current steering method that is mentioned in Section 2 is made use of in the next design, in which the CP contains two limbs, with the usage of a unity gain amplifier in between the two limbs of switches. A differential amplifier was utilised as buffer amplifier by the authors, in their earlier work on charge pump [29].

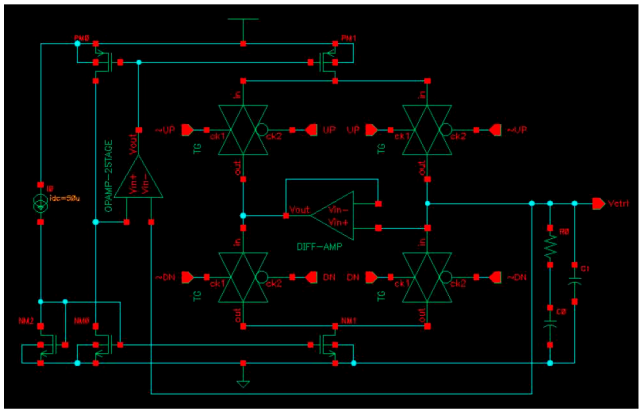

Fig. 6 *Proposed charge pump's circuit diagram*

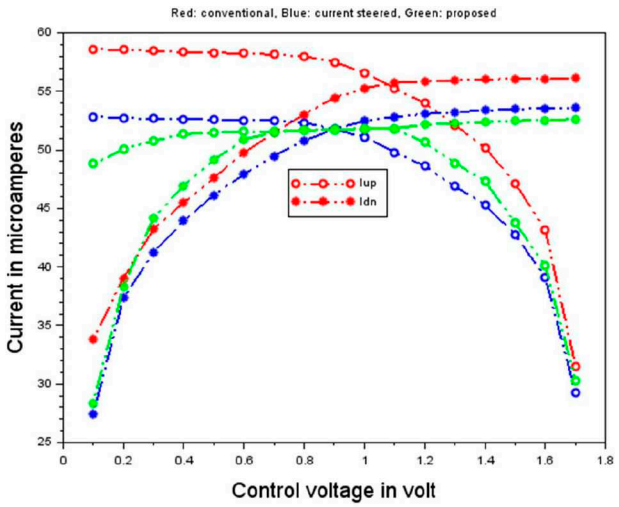

Fig. 7 *Current mismatch in the three designs of CP*

The current steering method increases the switching speed and reduces the charge sharing effect. To improve upon the results, the switches are replaced with transmission gates, due to which the effects of charge injection and clock feedthrough are reduced. To reduce the current mismatch further, a two-stage opamp with high gain is used as the compensation method. This circuit is shown in Fig. 6. The reference frequency for the designed PLL is selected as 100 MHz and the specifications of the required opamp are chosen accordingly. The two-stage opamp is designed as per the standard procedures [30], for ±1.8 V supply voltage.

The results obtained from the simulation of all three designs of charge pump are plotted in Fig. 7. For the range of control voltage in between 0.1 and 1.7 V, the average current mismatch of the traditional CP is 6.31%, that of the current steered one is 1.66%, and that of the proposed CP is 0.93%. In addition, with the proposed charge pump, it can be seen that the current mismatch is negligible around the crossover point in the transition curve.

As mentioned in Section 2, VCO that is based on ring oscillator is chosen for this work, whose frequency of operation depends on the parasitic device elements, which is unlike the LC oscillator. Equation (3) is the conventional form of expression, where t_d indicates the stage delay, with N indicating the number of stages

$$f_{osc} = \frac{1}{2\,N\,t_d} \tag{3}$$

With the submicron dimensions, for each type of MOSFET, there are >200 parameters being specified in the BSIM SPICE model. Therefore, if the designer of the circuit is willing to utilise these parameters, it is an extraordinarily tedious job to use such a large number, for the purpose of hand calculations. Primarily, these parameters are utilised by the EDA tool for the purpose of circuit simulation [31]. Usage of the first-order design equations, along

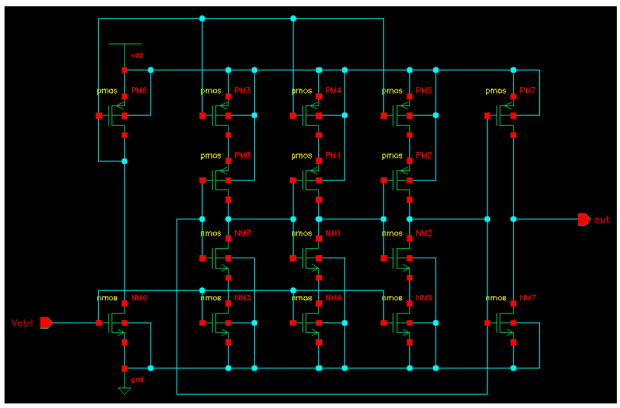

Fig. 8 *Three-stage current starved VCO*

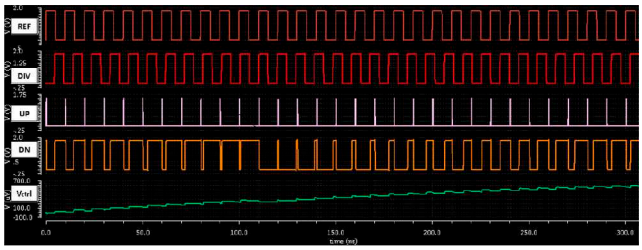

Fig. 9 *Waveforms with the conventional PFD*

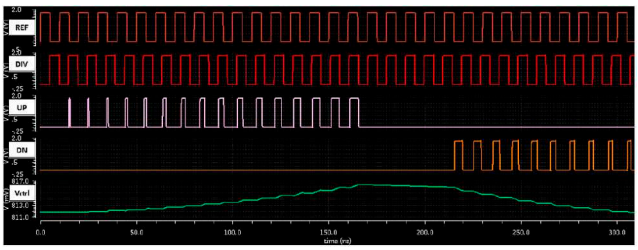

Fig. 10 *Waveforms with the proposed PFD*

with the consideration of the second-order effects, would be far easier for the designer to use.

Therefore, an effort is made by the authors, to obtain an expression for the value of the output frequency of ring oscillator, which is in terms of the device dimensions. Thus, for the two states of output, the resistances and the capacitances that are required for the computation of stage delay are computed. This is performed with respect to each node, by computing the R and C individually [32, 33]. Finally, when $W_p/W_n = 2.3$, the output frequency of the ring oscillator is expressed as

$$f_{\text{osc}} = \frac{1}{2000NL^2} \tag{4}$$

Equation (4) helps the circuit designer during simulation, for arriving at the required value of the frequency. As shown in Fig. 8, for our purpose of the PLL, a current starved VCO is designed using three-stage ring oscillator. In this circuit, the current starving transistors will be operating in the saturation region, whereas the inverter transistors will be operating in all three regions.

5 Simulation results of the PLL

After the functional verification of the individual blocks, the blocks are combined together for the functionality of the PLL. The divider modulus is 24, and the divider's design is based on TSPC D flip–flops. Initially, the simulation of the PLL along with the conventional PFD is performed, and later on, the same is performed with the proposed PFD. The results are shown in Figs. 9 and 10, respectively.

It can be noted from Fig. 9 that, the control voltage waveform's amplitude keeps on increasing until the onset of locking. Whenever

Table 2 Output voltage of loop filter

Conventional PFD		Proposed PFD	
Phase difference, ns	LF output, mV	Phase difference, ns	LF output, mV
−1.68	0.0426	−1.71	0.25
−1.14	0.0451	−1.14	0.17
+1.64	0.0424	+0.96	0.11
+2.20	0.0452	+1.56	0.19
+2.77	0.0443	+2.9	0.36

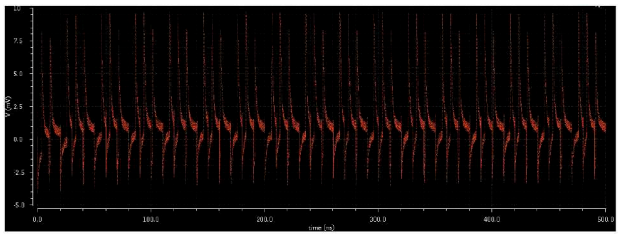

Fig. 11 *Control voltage waveform of the conventional PFD*

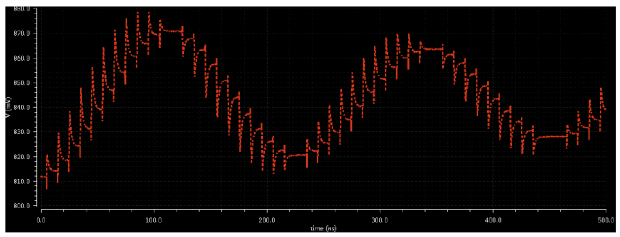

Fig. 12 *Control voltage waveform of the proposed PFD*

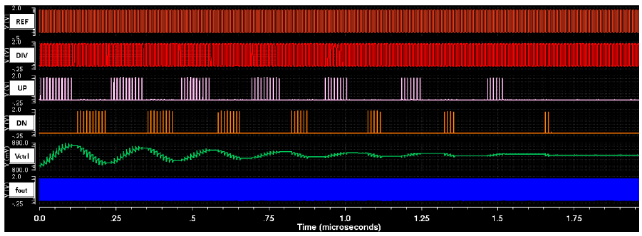

Fig. 13 *Waveforms of PLL's locked condition*

UP and DN both are high, the PFD is reset and is operating in the blind zone until reset goes low. Conversely, it can be observed from Fig. 10 that UP and DN pulses do not go 'high' together. They go into 'high' state only when there is phase lag and phase lead, respectively, at the input. Hence, due to the absence of reset signal, the proposed PLL has near-zero dead zone, and the PLL is free from blind zone [34].

For arriving at better conclusions, the simulated outputs of both conventional, as well as, proposed PFDs are compared in terms of the loop filter's output voltage. The measurements are summarised in Table 2, for varied phase differences in between REF and DIV waveforms. It is observed that the proposed PFD produces larger values of control voltage than the conventional PFD for a given delay. This results in a faster response time of the PLL. The control voltage waveforms, due to the action of both traditional as well as proposed PFDs, are shown in Figs. 11 and 12, respectively.

It can be noted that, with the proposed PFD, the control voltage amplitude keeps on getting reduced, which indicates the onset of locking. It can also be noted that the control voltage is centered near $V_{\text{DD}}/2$ with the proposed PFD, whereas it is centered near zero in case of the conventional PFD. Thus it is evident that the traditional PFD takes much longer time to settle.

The status of the PLL's locked condition, with the proposed PFD and CP, is as shown in Fig. 13, and the phase noise measurement is shown in Fig. 14. It is indicated in Fig. 13 that the PLL with the proposed PFD settles within 1.7 µs.

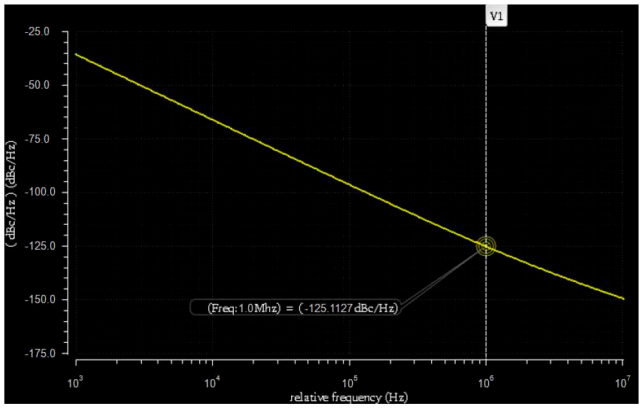

Fig. 14 *Phase noise measurement of PLL*

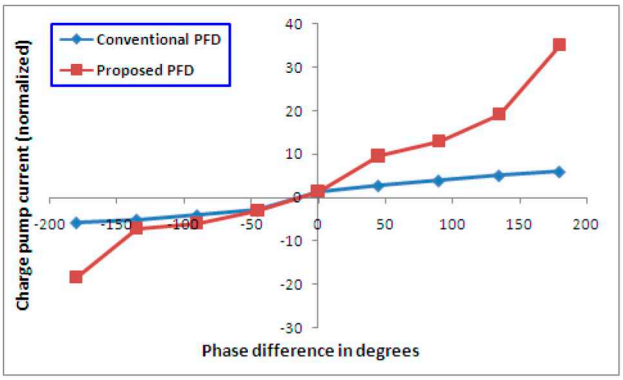

Fig. 15 *Comparison of static characteristics*

Table 3 Comparison between traditional and proposed PLL

Factor under consideration	Traditional PLL	Proposed PLL
avg. swing in control voltage	12.96 mV	2.03 mV
avg. duration of control voltage	190 ns	39.5 ns
avg. consumption of power	13.32 mW	10.98 mW

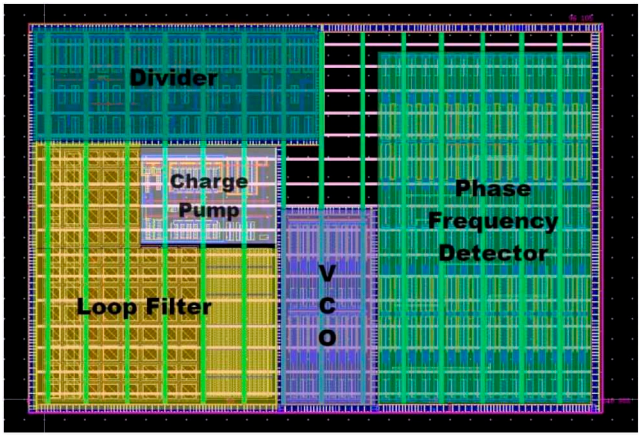

Fig. 16 *Layout of the proposed PLL*

6 Conclusion and future work

At the input of the PFD, for the phase difference from −180° till +180°, the CP output is measured, and the static characteristics of PLL with both PFD circuits are plotted in Fig. 15. During zero crossover, the proposed PFD is observed to be more sensitive than the conventional PFD. With the proposed PFD, the UP and DN pulses are produced in accordance with the phase differences, and hence their periods do not have any relationship with the logic status of REF and DIV signals. Thus, even though it seems as if the proposed PFD is of non-linear nature, the loop has similar functionality as that of the other resetless PLL circuits. The advantage with the proposed PFD is that it is applicable to lower frequencies as well, unlike the other resetless circuits. Finally, as the PFD output results in larger magnitude CP current, it results in faster locking of the PLL.

Table 4 Comparison of overall results

Parameter	[35]	[36]	[37]	This work
tech. node, nm	180	45	130	180
supply, V	0.8	1.0	1.2	1.8
phase noise @ 1 MHz, dBc/Hz	−110	−113.8	−120.7	−125.1
tuning range, MHz	250	200	—	270
ref. spur, dBc	—	−65	—	−72.4
lock time, µs	25	—	—	1.7

For estimating the lock time, the swing and the duration of the control voltage were measured for a much larger duration, and the measured results are enumerated in Table 3. As the generation of the UP and DN pulses is not continuous, the proposed PLL produces the control voltage whose duration is much lesser, and for the same reason, it consumes lesser power, when compared with the conventional one. In addition, there is a substantial decrease in lock time. Consecutively, the reduction in control voltage swing results in the reduction of spur content.

Fig. 16 shows the layout of the proposed PLL. The full die area including the guard rings is 141 µm × 96 µm. Table 4 summarises the final results, in comparison with the latest works. It is observed that the proposed PLL is achieving a lesser phase noise and spur, along with a larger tuning range.

As a future enhancement, the PLL can be designed with a differential topology ring oscillator so as to obtain a better noise performance. In addition, an effort can be made to reduce the current mismatch further, by adopting novel techniques for overcoming the second order effects.

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