A Sub-mW Fractional-*N* ADPLL With FOM of −246 dB for IoT Applications

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***Abstract*— This paper presents a sub-mW fractional-*N* all-digital phase-locked loop (ADPLL) with scalable power consumption, which achieves an figure of merit (FOM) of −246 dB. The proposed 10-b ultralow-power isolated constant-slope digital-to-time converter (DTC) achieves a 580-fs resolution and a measured integral nonlinearity (INL) of 870 fs with 0.14-mW power consumption at 52 MS/s. A narrow-range time amplifier (TA)-time-to-digital converter (TDC) with gain calibration minimizes both the in-band phase noise degradation and the loop-bandwidth variation. In addition, a coarse-DPLL is introduced with dead-zone function, which reduces the phase lock time to 4.2 μs at a 13-MHz frequency error. The coarse-DPLL monitors large frequency and phase jump in the background while consuming almost zero power. In an ultralow power mode, the proposed fractional-*N* ADPLL consumes a 0.65-mW power with a 26-MHz reference. A rms jitter of 1.00 ps and −50-dBc in-band fractional spur are achieved with a −242-dB FOM. In high-performance mode, a reference doubler is utilized, the jitter and spurs can be improved to 535 fs and −56 dBc, respectively, while consuming 0.98 mW. The proposed ADPLL with scalable power and jitter performance can be utilized for Internet-of-Things (IoT) applications, such as Bluetooth low energy (BLE) and Wi-Fi networks.**

***Index Terms*— All-digital phase-locked loop (ADPLL), bluetooth low energy (BLE), Bluetooth, constant-slope, digital PLL, digital-to-time converter (DTC), DPLL, fast lock, FOM, fractional-*N*, frequency synthesizer, gain calibration, Internet-of-Things (IoT), jitter, phase-locked loops (PLLs), sub-mW, time amplifier (TA), time-to-digital converter (TDC), ultralow power (ULP).**

I. Introduction

INTERNET of Things (IoT) shows great potentials for enhancing the communication capabilities for millions of people around the world. It enables us to communicate with the personal devices, nearby sensor nodes, machines, and even city infrastructures. Integrated wireless transceiver (TRX) is the key to realize such wireless connections. Ultralow-power (ULP) TRXs will be the key elements in a variety of short-range wireless standards, e.g., bluetooth low energy (BLE), Zigbee, WPAN/WBAN, and Wi-Fi network. The radio frequency phase-locked loop (RF-PLL), as one of the most critical elements in TRX, consumes a significant amount of power [1] due to the phase noise and spurious requirement. Hence, a reduction in PLL's power will significantly lower the ULP TRX power consumption. The all-digital PLL (ADPLL) [2]–[10], which takes advantage of the scaling of CMOS technology, is more promising than its analog counterpart in advanced CMOS process. It shrinks the required chip size while providing easily accessed analog/digital inputs/outputs (IO), which can be used for digital-intensive calibrations and modulations.

While the benefits of ADPLL are obvious, there are still barriers for realizing a sub-mW fractional-*N* ADPLL. In the initial proposal of the ADPLL design [9], as shown in Fig. 1(a), a full-range time-to-digital converter (TDC) and a counter (CNT) are utilized as the fractional and integer phase quantizer that measures the phase difference between the digitally controlled oscillator (DCO) and reference (REF). The TDC is required to cover at least one DCO cycle. The power consumption will increase, as we enlarge the TDC quantization range while maintaining a good linearity and resolution. This fundamental tradeoff makes it very difficult to realize the low-power operation with good jitter and spurious

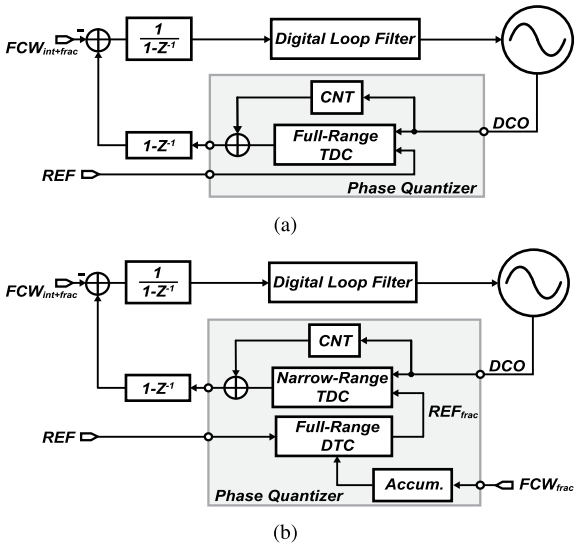

Fig. 1. (a) ADPLL with the full-range TDC to perform fractional-*N* operation. (b) ADPLL with the full-range DTC to perform fractional-*N* operation that reduces total power consumption.

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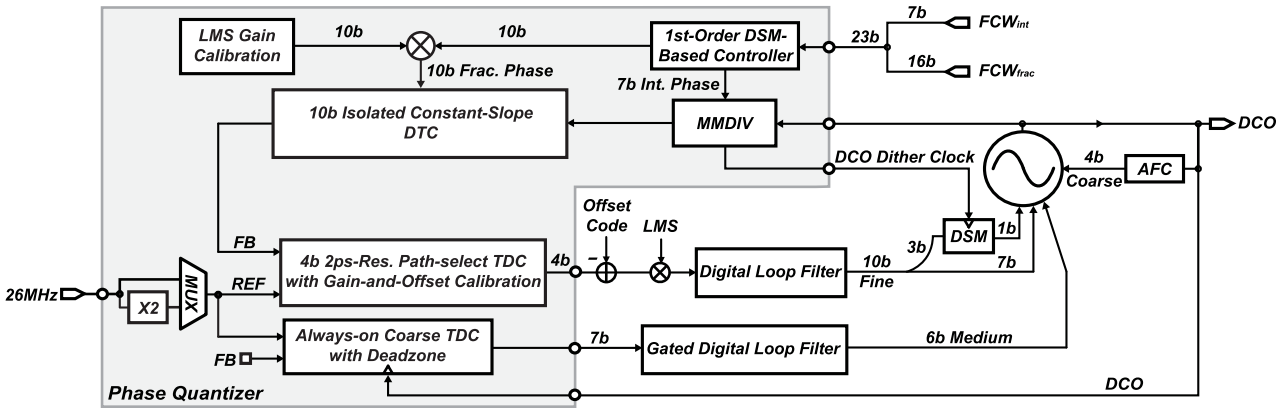


Fig. 2. Detailed block diagram of the proposed ULP ADPLL with the proposed 10b isolate constant-slope DTC.

performance [3], [9]. In Fig. 2(b), instead of using a full-range TDC, a full-range digital-to-time converter (DTC) can be placed in the REF path. It is controlled by the fractional part of frequency-controlled word (FCW), i.e., (FCW_{frac}), and produces a reference with a fractional phase REF_{frac} to the TDC input. It minimizes the phase error between REF_{frac} and DCO [4]–[8]. It basically mimics the operation of the fractional-*N* analog sub-sampling PLL [11]–[13]. This phase-prediction mechanism helps shrink the TDC range to only several DTC LSBs. As a result, even a bang–bang phase detector (BBPD) [8] can be used for achieving the fractional-*N* operation. In contrast with the TDC that quantizes time difference, DTC generates variable delays. Owing to this, the DTC consumes much less power than TDC when the same linearity and resolution are presented. With the help of the low-power DTC, a sub-mW ADPLL is realized for the first time in [4].

However, the DTC also suffers from poor linearity and resolution when considering the limited power budget. The integral nonlinearity (INL) of the DTC generates fractional spurs due to the periodic phase modulation. In [4], an ADPLL of 860 μW is realized with a worst fractional spur of −37 dBc and 1.71-ps rms jitter. It could potentially degrade the transmitter (TX) error vector magnitude (EVM), the receiver (RX) sensitivity, as well as the RX blocker tolerance. In [5], a DTC phase dithering technique is utilized to scramble the INL periodicity, which spreads the spur power into a white spectrum. The fractional spurs can be reduced by the dithering while it degrades the in-band phase noise. As a result, a 1.98-ps rms jitter is achieved with a 670-μW power. Because the DTC linearity is the most significant contributor of fractional spurs, a highly linear DTC with small power consumption is highly demanded. Constant-slope charging method is proposed [14] to fundamentally improve the DTC linearity. This method mitigates the nonlinearity arising from the inverter-based comparator. However, the integrated digital-to-analog converter (DAC) consumes a significant amount of power. Another issue of conventional DTC is that V_{TH} of the inverter-based comparator directly suffers from the supply variation, which greatly degrades the linearity. In order to keep the linear operation, the comparison should be independent of V_{TH}. TDC resolution is also important to minimize the jitter of the ADPLL. A time amplifier (TA) [7] can serve this purpose to improve the TDC resolution. However, the narrow-range TDC can only quantize a limited phase difference, which will significantly slow down the phase locking process [7], [8]. The lock-up time of the ADPLL is also critical for frequency hopping applications, such as BLE, and hence, it needs to be minimized.

The ADPLL presented in this paper uses a delta–sigma modulator (DSM) and multi-modulus divider (MMDIV) in the feedback path for realizing fractional-*N* operation. A DTC is used for canceling the quantization noise produced by MMDIV [8]. The analysis carried out in this paper reveals that a first-order DSM working in conjunction with a highly linear DTC is capable of realizing low-jitter fractional-*N* PLL with low power consumption, thus realizing high FOM. An isolated constant-slope DTC is proposed in this paper, which is capable of providing high linearity with low power consumption. While in the pre-charge and compare steps are combined in the conventional constant-slope DTC [14], in the proposed isolated constant-slope DTC, the pre-charge and the compare steps are isolated to maintain high linearity in a noisy supply environment and assure lower power consumption. A TA-based TDC [7] is adopted to achieve high TDC resolution to improve the in-band phase noise. To speed up the phase-locking process, an always-on coarse DPLL is proposed. The ADPLL achieves a fast locking, while the coarse DPLL consumes almost zero power after phase lock is achieved. The proposed fractional-*N* ADPLL achieves a 535-fs jitter and an in-band fractional spur of −56 dBc with only 0.98-mW power, thanks to the proposed DTC. It is also capable of 0.65-mW power operation while achieving a 1.00-ps jitter and a −50-dBc spur.

II. Sub-mW Fractional-*N* ADPLL Architecture

To realize low-power, low-jitter, and low-spur performances simultaneously in a fractional-*N* ADPLL, the selection of the architecture and the specifications of each building block are crucial in system level design. A detailed architecture-level block diagram of the proposed ADPLL is shown in Fig. 2. To improve the in-band phase noise, a 4b 2-ps-resolution

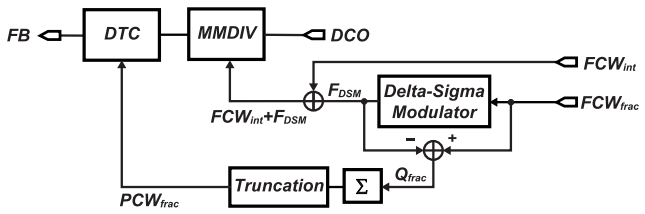


Fig. 3. DSM-based fractional controller.

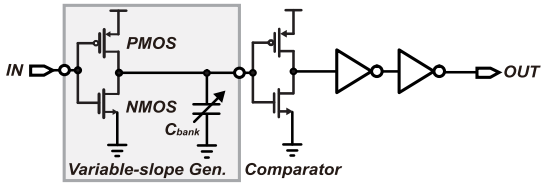


Fig. 4. Variable-slope DTC.

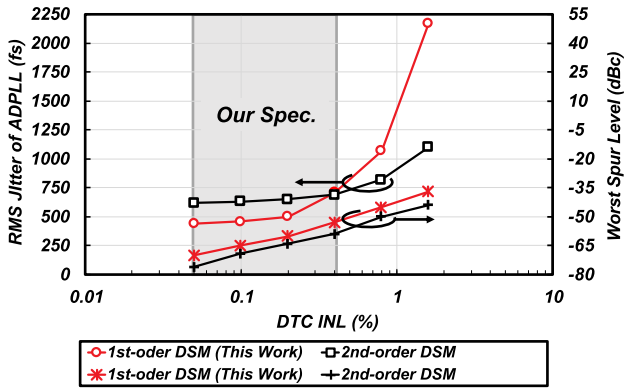


Fig. 5. System level analysis of first- and second-order DSM-based fractional controller for low-power ADPLL.

TA-TDC [7] and a reference doubler are implemented. The duty cycle issue of the doubler [15] is calibrated by using the method proposed in [16]. The proposed 10b isolated constant-slope DTC enhances the FOM of the fractional-N ADPLL, thanks to the good linearity and power efficiency. An MMDIV is used to perform the phase accumulation and frequency division simultaneously. Both MMDIV and DTC are controlled by the DSM-based controller [8], as shown in Fig. 3.

As compared with second-order DSM used in [8] and [13], a first-order DSM-based architecture can accept a much simpler digital implementation, which saves power consumption and area. It also reduces the DTC range from two DCO periods to only one DCO period. While the issue of using the first-order DSM is that the DTC gain calibration cannot adequately converge if a small fractional number is used [8]. However, for typical IoT applications, such as BLE and Wi-Fi with over 1-MHz channel spacing, such a small fractional numbers are not required, and the gain calibration can correctly converge even with the first-order DSM. In order to discuss the power, jitter, and spur tradeoffs using different DSMs, we compared the performance differences between the first-order DSM and the second-order DSM. The variable-slope DTC shown in Fig. 4 is used in [4]–[8], [17], and [18], where the delay range (DR_{DTC}) can be written as

$$DR_{\mathrm{DTC}} = V_{\mathrm{TH}} / \frac{I_{\mathrm{NMOS}}}{C_{\mathrm{bank}}} = V_{\mathrm{TH}} \cdot \frac{C_{\mathrm{bank}}}{I_{\mathrm{NMOS}}}. \tag{1}$$

I_{NMOS} is the current flowing through the NMOS of the inverter, C_{bank} is the variable capacitor loads, and V_{TH} is the inverter threshold voltage. If we assume that the current is constant during charging and discharging C_{bank}, we can write the DTC power consumption as

$$P_{\mathrm{DTC}} = V_{\mathrm{DD}} \cdot I_{\mathrm{NMOS}} \cdot f \cdot V_{\mathrm{DD}} / \frac{I_{\mathrm{NMOS}}}{C_{\mathrm{bank}}} = {V_{\mathrm{DD}}}^2 \cdot C_{\mathrm{bank}} \cdot f \tag{2}$$

where f is the operating frequency of the DTC. To double the delay range while keeping the same power consumption, C_{bank} cannot be changed as shown in (2). Hence, the only possible option is to change I_{NMOS} by half, as shown in (1). The variance of the timing jitter of the DTC can be analyzed as in [19]. The jitter variance of the DTC can be written as

$$\begin{aligned} \sigma_{\mathrm{DTC}}^2 &= \frac{4\mathrm{kT}\gamma_{\mathrm{NMOS}} DR_{\mathrm{DTC}}}{I_{\mathrm{NMOS}}(V_{\mathrm{DD}} - V_{\mathrm{TH}})} + \frac{\mathrm{kT}C_{\mathrm{bank}}}{I_{\mathrm{NMOS}}^2} \\ &= \frac{\mathrm{kT}C_{\mathrm{bank}}}{I_{\mathrm{NMOS}}^2} \cdot \left(1 + \frac{4\gamma_{\mathrm{NMOS}}}{V_{\mathrm{DD}}/V_{\mathrm{TH}} - 1}\right) \end{aligned} \tag{3}$$

where k is the Boltzmann's constant and T is the temperature. As discussed earlier, doubling the delay range DR_{DTC} will halve I_{NMOS}. Equation (3) shows that it will double the jitter contribution. This is the tradeoff between the delay range and jitter of the delay element, such as a DTC. For the low-power design, the jitter from each component should be optimized in consideration of the power budget. For a system-level estimation and a transistor-level simulation, a worst case rms jitter of 0.7 ps is expected at DTC output for the first-order DSM, while the rms jitter will become 1.4 ps using the second-order DSM. All blocks shown in Fig. 2 are modeled with pre-determined parameters, and only the DTC and the order of the DSM are changed. The DTC INL is modeled in a sinusoid shape with a lookup table. The relative INLs of both DTCs are swept, and the rms jitter and the worst spurs (in-band fractional spurs) of the ADPLL are recorded, as shown in Fig. 5. The ADPLL loop bandwidth is optimized to 600 kHz at a 52-MHz reference, and the first in-band fractional spur is located at 200 kHz. At a very small INL, the first-order DSM demonstrates around 190-fs better rms jitter. This is expected because the periodic jitter is not dominant in output, while the doubled DTC jitter contributes more to the output using the second-order DSM. However, when the INL increases to over 0.4%, the periodic jitter caused by spurs becomes dominant, and the output jitter in the first-order DSM becomes worse. The second-order DSM randomizes the spur energy into white spectrum, hence can be filtered by the loop filter [13]. For achieving better FOM performance, the rms jitter should be kept as low as possible, which is the motivation behind using the first-order DSM. The INL specification of DTC is from 0.05% to 0.4%, which contributes to a maximum of 2.8-dB improvement in FOM for a 1-mW operation of the ADPLL.

To estimate the phase noise, both phase-domain and time-domain methods are used, as shown in Fig. 6. In the

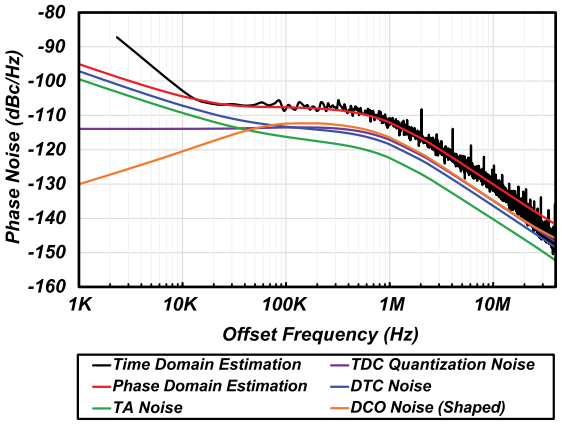


Fig. 6. Phase noise estimation of the ADPLL in the phase-domain (without fractional spurs) and the time-domain phase noise simulation at 2442 MHz using 52-MHz reference (with fractional spurs).

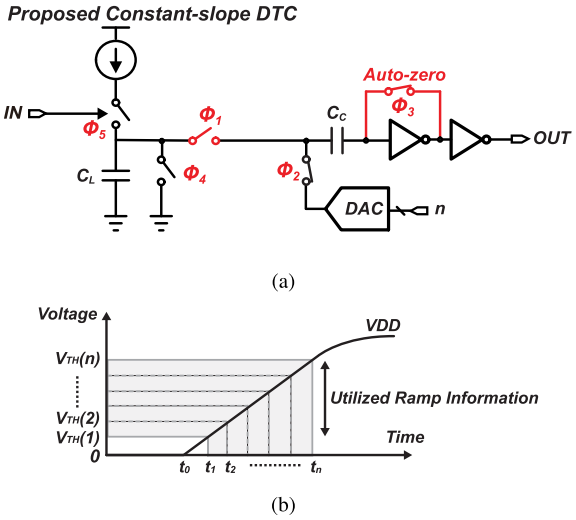


Fig. 7. (a) Proposed isolated constant-slope DTC. (b) Concept operation of the proposed DTC.

phase-domain simulation, the phase noise of each building block is simulated in the transistor level. Noise transfer functions are used to calculate their contributions at PLL output. The red line shows the total phase noise of the fractional-*N* ADPLL. As shown in Fig. 6, there are four major noise contributors, i.e., TA noise with 10% contribution, TDC quantization noise with 27% contribution, DTC noise with 30% contribution, and DCO noise with 33% contribution. The black line shows the time-domain simulation of the ADPLL that operates at 2442 MHz using a 52-MHz reference clock. This simulation is performed in the Verilog environment, and all building blocks of the ADPLL are modeled in Verilog. The noises of the DTC, TA, and DCO estimated from the transistor-level simulations are included in the models. The digitally controlled variable delays of the DTC are modeled in Verilog by using a lookup table, the variable delays are expressed as

$$Delay_{\mathrm{DTC}} = 1\mathrm{ns} + \frac{DR_{\mathrm{DTC}}}{2^n - 1} \cdot k + INL_{\mathrm{peak}} \cdot \sin\left(\frac{2\pi}{2^n - 1} \cdot k\right) \quad (4)$$

where 1 ns is the fixed delay of the DTC, $n(=10)$ is the number of bits, k is the control code ranging from 0 to 1023, $DR_{\mathrm{DTC}}(=560$ ps) is the delay range, and $\mathrm{INL}_{\mathrm{peak}}$ is the worst case peak INL of 450 fs, as shown in the DTC-linearity simulations in Section III. This DTC nonlinearity is the dominant source of the fractional spurs. The fractional spurs are expected to be at approximately 2 MHz and its harmonics, which can be observed in Fig. 6. The time-domain simulation matches with the phase-domain simulation, which proves to be a good estimation of the overall output phase noise. The overall power consumption is estimated as 1 mW at a 52-MHz reference according to the post-layout simulation. A 435-fs estimated jitter contributes to a −247-dB FOM.

III. Proposed Isolated Constant-Slope DTC

A. Concept of Operations

Since the DTC linearity performance will greatly influence the jitter and spur performances of the proposed ADPLL using a first-order DSM, as analyzed in Section II, the DTC design becomes more challenging than TDC at a limited power budget. Constant-slope DTC method is proposed in [14] to mitigate the inverter-induced nonlinearity. It demonstrates a fundamental improvement in the linearity of the delay generation over the conventional variable-slope DTC [4]–[8], [17], [18]. In the concept of the original constant-slope DTC, the digital controlled delays are acquired by varying the starting voltages V_{ST} of the slopes, which are generated by a fixed current source. V_{ST} is acquired by pre-charging the loading capacitor C_{L} using a DAC before the input signal triggering the current source. Since the charging slopes across the inverter $V_{\mathrm{TH,inv}}$ share the same slew-rate (SR), the inverter-induced nonlinearity will be mitigated [14]. However, in order to reduce the jitter of DTC, the charging current used for slope generation should be enlarged according to (3). To acquire the desired delay range, the ratio of the current and load capacitor C_{L} should be kept the same according to (1). Hence, the value of C_{L} will also increase. A significant amount of the energy $E_{\mathrm{PreChg}} = C_{\mathrm{L}} \cdot V_{\mathrm{ST}}^2/2$ will be consumed to acquire V_{ST} caused by a large C_{L}. Furthermore, because a charge current cannot be fully turned on instantaneously, a different V_{ST} will cause different startup behaviors for a practical current source, as explained in [14]. A high V_{ST} will significantly degrade the INL of the DTC [14]. The original constant-slope DTC consumes almost 1-mW power on DAC for V_{ST} settling at a 55-MHz clock and utilizes a 1.2 V for current source V_{DD} in order to achieve an INL of 0.15% [14].

Fig. 7 shows the proposed 10b DTC utilizing constant-slope method [2]. Instead of varying the V_{ST} of the constant-slopes, which will potentially distort the current source, a concept of the ramp division architecture is adopted, as shown in Fig. 7(b), whose $V_{\mathrm{TH}}(n)$ of the comparator is shifted. The comparator will output a corresponding edge at t_{n} and produces a delay of $t_{\mathrm{n}} - t_0$. By always using the same slope generated by the current source, the linearity degradation from the current source can be mitigated, and any higher supply voltage is not required. Furthermore, the slope information in the center portion can be used for nearly 600 mV/1 V = 60%

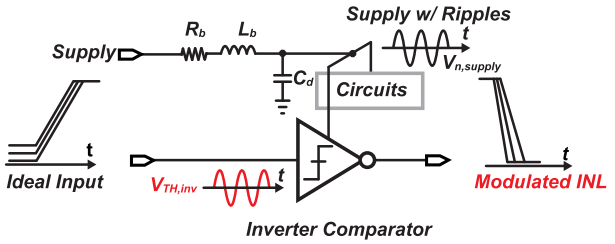


Fig. 8. V_{TH} offset caused INL, which is induced by noisy supply.

for a 1-V supply, while for the conventional constant-slope DTC, only 200 mV/1.2 V $\approx$ 17% in [14] can be utilized using a 1.2 V-supply. The current source linearity can be improved almost 3.5 times by the isolation operation. $V_{TH}(n)$ is shifted by isolating the pre-charge step with the comparing step by using a series capacitor C_C and DAC. C_C is small enough not to degrade the pre-charge time on both sides of the C_C by DAC and Φ_3. The reduced pre-charging capacitance can minimize the DAC power consumption even in a high-speed operation. Another important issue is raised from the comparator, which essentially is an inverter in most of the state-of-the-art DTCs [8], [14], [18], [20]. As shown in Fig. 8, other circuits in the same supply line will cause ripples because of the supply environment, such as the series inductors and resistors. Those ripples will remain because of the limited area for the decoupling capacitor and limited power budget for on-chip regulators in IoT applications and will strongly couple to the threshold of the inverter-based comparator. The linearity will be greatly influenced by the threshold variation and degrades the ADPLL jitter performance when the first-order DSM architecture is utilized. In the proposed architecture, this issue is solved by auto-zero switch Φ_3, which mitigates the inverter $V_{TH,inv}$ offset in every conversion, hence greatly improves the INL.

Fig. 9 shows the conceptual operation of the proposed DTC. In pre-charge step, as shown in Fig. 9(a), the nodes A and B of C_C will discharge from the saturated voltage of previous slopes. Node A will discharge to the desired DAC voltage, and node B will discharge to $V_{TH,inv}$. As we have noticed that the pre-charge step is a discharge process that causes no extra power consumption from DAC, the pre-charge speed will be limited by the output resistance of R_{DAC} from DAC and C_C. Because C_C is small, R_{DAC} can be chosen to be large to minimize the power consumption from the DAC. In set step, as shown in Fig. 9(b), Φ_1 and Φ_4 are closed to short node A to 0 V. Node B will drop the same amount of voltage, which results in a new $V_{ST} = V_{TH,inv} - V_{DAC}$ at inverter input. At the final step, shown in Fig. 9(c), Φ_1 is closed and Φ_5 is triggered by input rising edge. The current source starts to charge C_{load} to acquire a slope at node A from 0 V to VDD, and node B will copy the slope of node A while starting from V_{ST} generated by set step. The rising edge will reach the decision point of the inverter-based comparator at t_{N+1} and produces rising edges with variable delays. If we consider a noisy supply environment, as shown in Fig. 8, $V_{n,Supply}$ is presented at the supply line, which modulates the $V_{TH,inv}(t_N)$ and $V_{TH,inv}(t_{N+1})$ at t_N and t_{N+1}, respectively. The digitally controlled $V_{TH}(n)$

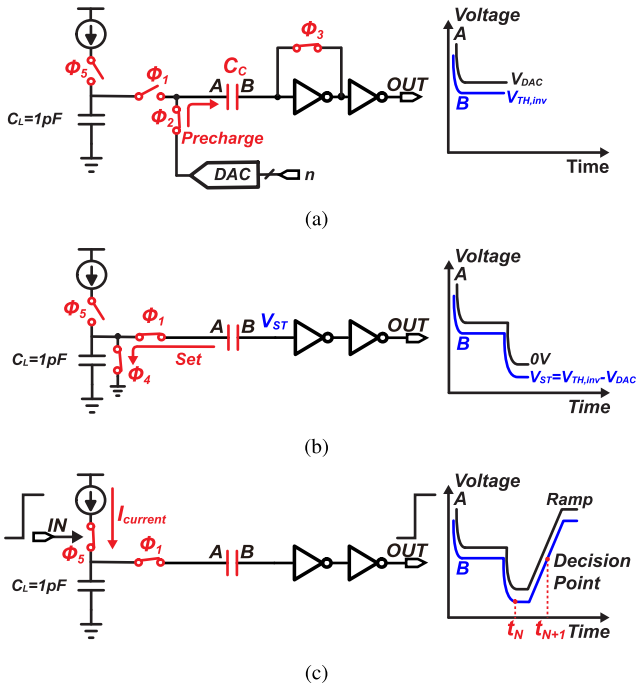


Fig. 9. Conceptual operation diagrams of proposed 10b isolated constant-slope DTC. (a) C_L is isolated from DAC during DAC operation (Pre-charge step). (b) Charge in C_C is shorted to ground, which set new V_{ST} at node B (Set step). (c) Constant slope with new V_{ST} is compared in inverter (Compare step).

can be written as

$$\begin{aligned} V_{TH}(n) &= V_{TH,inv}(t_{N+1}) - V_{TH,inv}(t_N) + V_{DAC}(n) \\ &= \alpha(f) \cdot V_{n,Supply} + V_{DAC}(n) \end{aligned} \tag{5}$$

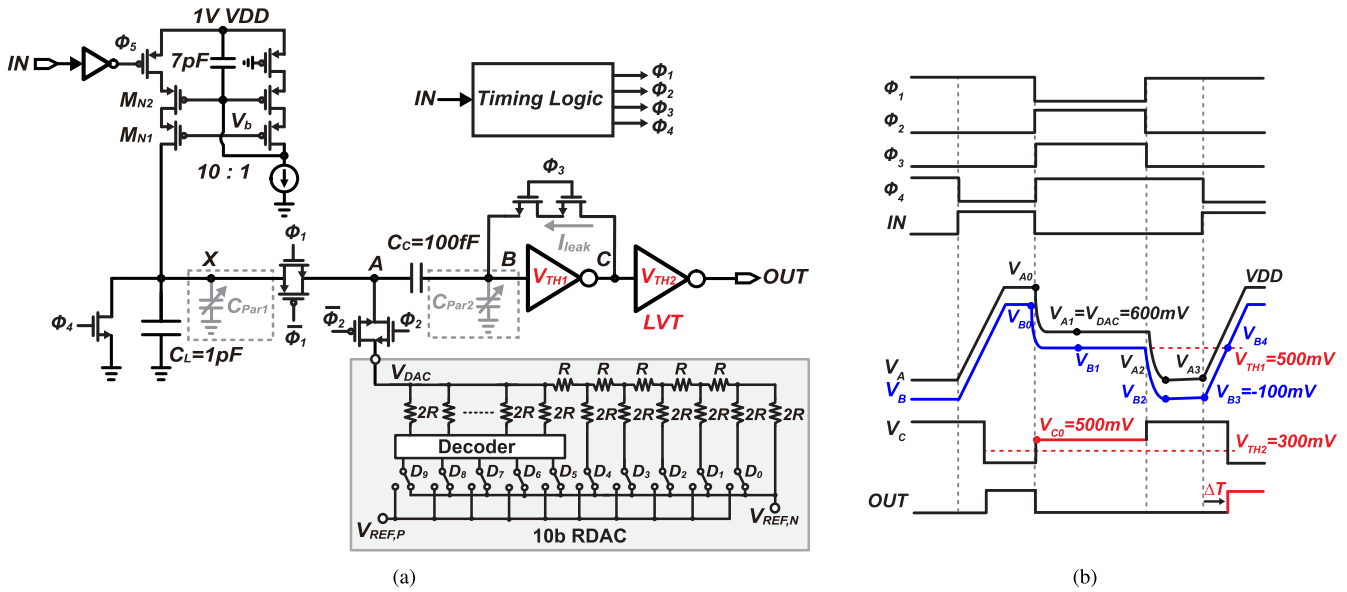
where $\alpha(f)$ is a frequency-dependent factor with a value of less than 1, and it also depends on the difference between t_N and t_{N+1}. According to (5), the DTC samples the power noise at t_N, and then, the power supply noise is subtracted at t_{N+1}. A smaller $t_{N+1} - t_N$ will greatly reduce $\alpha(f)$. Ideally, if $t_{N+1} = t_N$, $\alpha(f)$ will be 0. The variable delay for each control code will be

$$t_n = V_{TH}(n) \cdot \frac{C_L}{I_{current}} = (\alpha(f) \cdot V_{n,Supply} + V_{DAC}(n)) \cdot \frac{C_L}{I_{current}}. \tag{6}$$

Equation (6) shows that the delay is no longer determined by the inverter threshold if $\alpha(f) = 0$, thanks to the auto-zero function in an ideal condition.

B. Nonlinear Sources and Circuit Implementations

Since the linearity of the DTC affects both the rms jitter and fractional spurs of the proposed ADPLL, the linearity degradation from nonlinear sources should be minimized. The detailed DTC core implementation is shown in Fig. 10(a). A cascode current source is utilized to improve the current source linearity. As shown in Fig. 7(b), the slope will be interpolated by $V_{TH}(n)$. Any nonlinearity in the slope will transfer to the DTC INL. Long-channel devices of M_{N1} and M_{N2} are chosen to minimize this error. Since the utilized



(a) (b)

Fig. 10. Detailed circuit of (a) isolated constant-slope DTC with 10b RDAC and (b) its timing chart.

slope information, as shown in Fig. 7(b), contributes to most of the nonlinearity of the proposed DTC, any improvement in the current source linearity will directly improve the DTC linearity.

Another primary nonlinear source is from the junction capacitors C_{Par1} and C_{Par2} at nodes X and B, where all transistors connected to these nodes will contribute to C_{Par1} and C_{Par2}. $C_{\mathrm{Par1}}(V_{\mathrm{X}})$ will be negligible if C_{L} is sufficiently larger and will not degrade the INL, while as for C_{Par2}, it acts as a voltage divider capacitor in series with C_{C}. In other words, the slope at node B in the compare step will not follow the slope at node A exactly. The waveform distortion at node B will degrade the INL of the DTC if the value of C_{C} is not sized adequately. A large C_{C} is desired to minimize the effect from C_{Par2}. However, a large C_{C} will potentially increase the settling time and the power consumption of the DAC, which limits the maximum operation frequency. C_{C} is optimized to a value of 100 fF when considering sufficient margin to cover process, voltage, and temperature (PVT) variations of the above-mentioned issues. Furthermore, the node A always drops from $V_{\mathrm{DAC}}(n)$ to 0 V; hence, C_{Par2} is a function of $V_{\mathrm{DAC}}(n)$, i.e., $C_{\mathrm{Par2}}(V_{\mathrm{DAC}}(n))$. This dependence limits the maximum output range from DAC. In this design, an optimized range of 350 mV is chosen for the better DTC linearity when both the current source linearity and effects from C_{Par2} are considered.

One more major source of nonlinearity is from the leakage current I_{leak} of the auto-zero switch Φ_3 during the set step. Φ_3 is opened to hold V_{ST} values before the slope arrives. However, due to the limited off-resistance r_{off} of the CMOS switch, the current will leak from node C to node B from the inverter's supply. It charges C_{Par2} and C_{C} simultaneously and causes nonlinear error voltages at node B. This error is highly depending on $V_{\mathrm{DAC}}(n)$ as well as the operation time of the set step and compare step $(t_{\mathrm{N+1}} - t_{\mathrm{N}})$. To minimize this error, two switches are implemented in series to increase the effective r_{off}, while the $t_{\mathrm{N+1}} - t_{\mathrm{N}}$ is minimized to 1/10 of the DTC period. The shortened $t_{\mathrm{N+1}} - t_{\mathrm{N}}$ also contributes to the supply noise suppression.

Last but not least is the nonlinearity of the 10b resistor-DAC (RDAC). The 5b binary code is designed for LSB to save the chip area, while the 5b thermal code is designed for MSB to maintain good linearity. The mismatch of the resistors and the non-ideal reference voltage will cause the linearity degradation of the RDAC. It will directly transfer to DTC INL. Other non-major nonlinear sources, such as charge sharing of CMOS switches, can be minimized by proper sizing of the transistors in simulations.

The detailed timing chart of the proposed DTC is shown in Fig. 10(b). During the period when the auto-zero switch is closed in pre-charge step, node B will be set to the inverter V_{TH1}, which is around 500 mV. At node C, the voltage will also be shorted to node B and producing a 500 mV. If the second inverter V_{TH2} is also around 500 mV, the DTC output OUT will produce multiple zeros and ones due to the noise. To maintain a robust operation, an low-voltage threshold (LVT) inverter, whose $V_{\mathrm{TH}} = 300$ mV, is placed at the output of the DTC.

C. Simulation Results

The simulated results of the proposed DTC are shown in Fig. 11. In the typical–typical corner with 1.0-V VDD and a temperature of 25 °C, it achieves a 10b range of 560 ps with a 550-fs resolution. The peak INL is 0.05% (200 fs) at 52 MS/s with 140-μW power. Other corners and temperature conditions are also applied, as shown in Fig. 11(a) and (c). The worst case is observed while using a 0.9-V supply voltage, as shown in Fig. 11(b), due to the linearity degradation of the current source. The post-layout Monte Carlo simulations are performed, as shown in Fig. 11(d). These simulations indicate a +450-fs peak INL. To evaluate the effect from the supply noise, the deterministic jitter variance σ^2 with and without an auto-zero offset switch is shown in Fig. 12 when noise

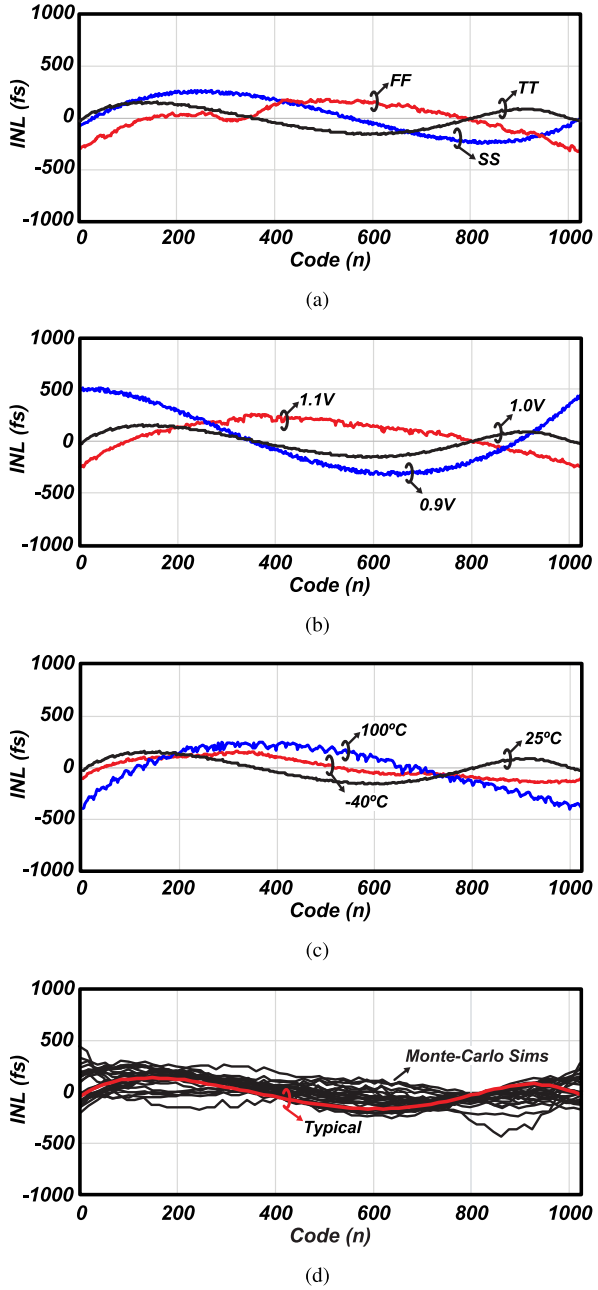


Fig. 11. Post-layout INL simulations of the proposed DTC with (a) corner conditions, (b) supply voltage variations, (c) temperature variations, and (d) Monte Carlo simulations.

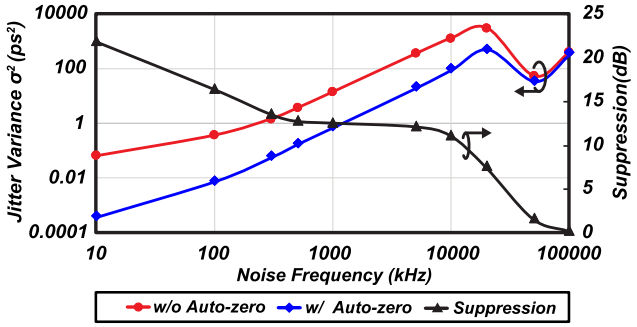


Fig. 12. Simulated deterministic jitter power w/ and w/o auto-zero switch when noisy supply with different frequencies are presented, and the deterministic jitter power suppression w/ auto zero switch.

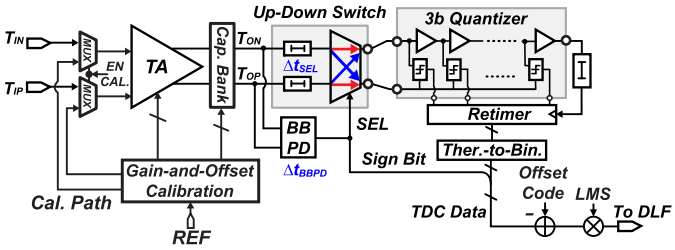


Fig. 13. Path-select TDC.

is added. In the post-layout simulation, 20-mV_{pp} sine waves with different frequencies are applied to the supply of DTC core. The jitter variance and the corresponding suppression in dB with and without auto-zero function are recorded. From the simulation results, the suppression is larger if the supply noise frequency is lower. This matches with the analysis from (5). The smaller the noise frequency, the smaller will be the $V_{TH,inv}(t_{N+1}) - V_{TH,inv}(t_N)$.

IV. Building Blocks of the Proposed ADPLL

A. Path-Select TA-TDC and TA Gain Calibration

A path-select TA-TDC is implemented shown in Fig. 13. A BBPD derives the sign of the phase error after TA, a path select logic is used to switch the up and down paths of TA output based on the results from BBPD. If T_{ON} leads T_{OP}, the up–down switch will be transparent for both signals. If T_{ON} lags T_{OP}, the up–down switch will switch the two signal paths to avoid outputting all zeros. The up–down switch function can make sure both lead and lag conditions between T_{ON} and T_{OP} quantized by a 3b 16-ps-resolution coarse TDC. At the output of the TDC, the quantizer output will be combined to 4b with the BBPD output. As compared with [7], which adopted two 3b quantizers for the same purpose, the path-select technique saves almost half of the power and area. Notice that to properly switch up and down signals, the BBPD should output selection signal before T_{OP} and T_{ON} coming to the up–down switch. While in practice, the BBPD takes Δt_{BBPD} to derive the selection signal. Two extra delays of Δt_{SEL} are added before two inputs of the up–down switch. If Δt_{SEL} is longer than Δt_{BBPD}, T_{OP} and T_{ON} can be properly switched. However, the path mismatch introduced by two extra delays bring a time error at 0 code and cause INL degradation. The TA can minimize the time error using its gain. To completely mitigate this issue, a constant offset code is added at the TDC output. After phase locked, the TDC will not use codes around 0 to avoid the potential linearity degradation. This constant offset is decided by the jitter of the ADPLL itself. A post-layout simulation of the path-select TDC shows a +50-/−220-fs peak INL with around 2.1-ps/LSB resolution.

As widely known, TA gain G_{TA} is very sensitive to PVT variation [21]–[23]. G_{TA} will influence on the PLL phase noise in two directions, the first is the loop bandwidth and the second is the in-band phase noise due to the quantization noise. As shown in Fig. 13, the loop bandwidth can be compensated by LMS calibration [24]. However, the in-band phase noise will be influenced by the effective resolution

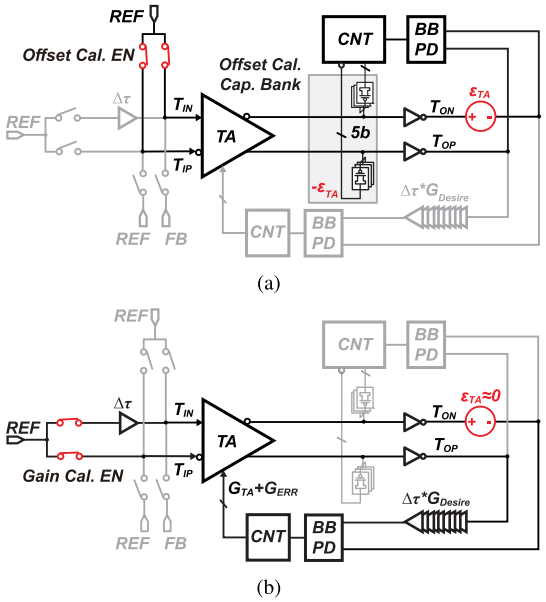


Fig. 14. Proposed TA gain-and-offset calibration technique. (a) TA time-offset calibration. (b) TA gain calibration.

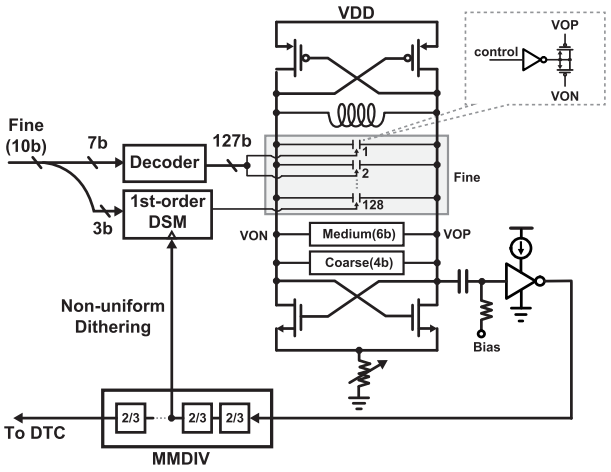


Fig. 15. Detailed schematic of the *LC*-DCO and the non-uniform dithering.

t_{res} of the TDC [25], where, in this design, it is the ratio between the resolution of the coarse TDC (a buffer delay) and G_{TA}. Hence, the in-band phase noise will not be improved by the LMS calibration of TDC gain. In post-layout simulations of this paper, a buffer delay varies from 16.3 to 16.9 ps across the temperature variation from −40 °C to 100 °C, while G_{TA} varies from 9.7 to 6.2. Hence, t_{res} varies from 1.7 to 2.7-ps/LSB. In addition, buffer delay varies from 17.1 to 16.1 ps when supply varies from 0.9 to 1.1 V, while G_{TA} varies from 9.0 to 7.0. t_{res} varies from 1.9 to 2.3 ps/LSB. If G_{TA} is calibrated in both cases, t_{res} will be stabilized at around 2.1 ps/LSB across the temperature and supply variations. However, the TA gain calibration will not be effective to the corner conditions, where t_{res} will still vary from 1.8 to 2.5 ps after calibration in FF and SS condition, respectively. The conventional TA gain calibration [22] is done by inserting a delay of $\Delta\tau$ at input and then computing the delay at the output. However, the process mismatch-induced time offset ϵ_{TA} will cause an extra gain error of $G_{ERR} = \epsilon_{TA}/\Delta\tau$. In a low-power design of the TA, ϵ_{TA} can be as large as ±140 ps in a Monte Carlo simulation. Due to the limited linear amplification range of TA, $\Delta\tau$ cannot be too large. Hence, $\Delta\tau$ of 27 ps will result in a G_{ERR} of over ±65% if a worst time offset is presented. The conventional offset calibration [23] utilizes a replica TA to compute the offset time but introduces the area overhead and the mismatch between original TA and replica TA. In Fig. 14, a gain-and-offset calibration is proposed. First, ϵ_{TA} is calibrated by a 0 time delay at the input. The output of TA should be 0 as well if $\epsilon_{TA} = 0$. If $\epsilon_{TA} \neq 0$, BBPD will detect the errors and adjust the capacitor bank at TA output. After the offset calibration, the gain calibration begins, as shown in Fig. 14(b). By the proposed two-step calibration, G_{ERR} will be minimized from 64.5% to 6.25% in the simulation. Even though TA gain calibration affects the linear range of the gain itself, a sufficient margin of the linear range is designed to ensure a good linearity of the TDC within its quantization range in this paper.

B. Digital Controlled Oscillator

Fig. 15 shows the implementation of the DCO [26]. A CMOS-type *LC*-oscillator is implemented to maintain a robust oscillation with low current consumption. A CMOS-type buffer with a bias is implemented to further lower the buffer power. The 10b digital control code for the fine frequency bank is separated into 7b MSB with a frequency resolution of 50 kHz/LSB and 3b LSB to further improve the resolution to about 7 kHz/LSB by using the first-order DSM. The high-frequency dithering clock for DSM is directly taken from the middle stage of the MMDIV [27], which saves the power from an additional high frequency divider. A 6b medium bank with a resolution of 1.25 MHz/LSB for the coarse PLL and a 4b coarse bank with around 50 MHz/LSB are designed, respectively.

C. Coarse PLL Loop

For narrow-range TDC, the phase-locked time is generally very long when a large frequency error is presented. For a DPLL with a BBPD [8], a 1 ms is reported for phase lock in case of large-frequency step. A lock time of around 40 μs is required for a TDC with 16-ps range even when no frequency error is presented [7]. In ADPLLs using the narrow-range TDC [5], [28], the frequency locked loop is shut down for further power saving, which makes the loop easily suffer from large frequency and phase disturbances.

In this design, to lock the frequency of ADPLL, the 4b coarse bank of the DCO is controlled by auto frequency control (AFC) function [29]. However, even the frequency is locked, the gain of the narrow-range TDC will be almost 0 if large phase errors are presented. The 0 gain will degrade the convergence speed of the PLL. In this paper, an always-on coarse-DPLL shown in Fig. 16 works simultaneously with the main PLL loop. A dead-zone logic is inserted after the phase/frequency detector (PFD), which produces an enable

TABLE I
COMPARISON TABLE OF THE STATE-OF-THE-ART DTCS

	This work	[14]	[20]	[8]	[18]
Architecture	Isolated constant slope	Constant slope	Variable slope	Variable slope	Variable slope
Technology	65nm	65nm	65nm	65nm	28nm
Delay range	593ps	189ps	186ps	338ps	563ps
Resolution	580fs	185fs	4700fs	330fs	550fs
INL	**870fs (0.15%)**	328fs (0.17%)	1900fs (1%)	3000 (1%)	990fs (0.18%)
Worst Jitter	630fs	210fs	300fs	400fs	250fs
Power(mW)	**0.14@52MHz**	0.8+1.0@55MHz	0.22@48MHz	2.2@40MHz	0.5@40MHz

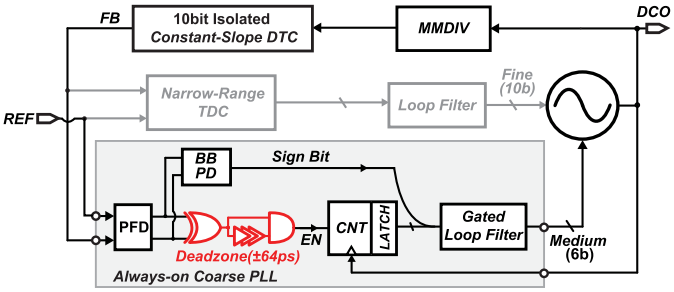


Fig. 16. Always-on coarse PLL with a dead zone of ±64 ps, which consumes almost zero power after phase locked.

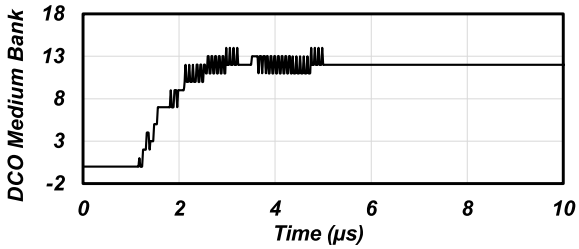


Fig. 17. Simulated lock transient of the proposed coarse-DPLL.

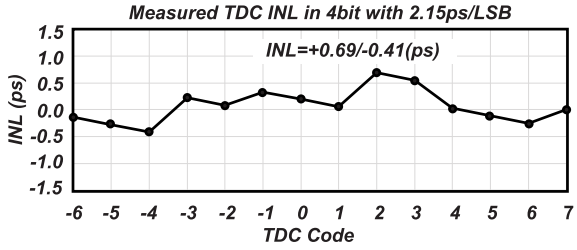


Fig. 18. Measurement result of the 4b TDC at 52 MS/s.

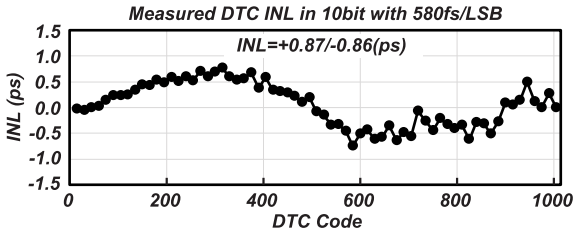


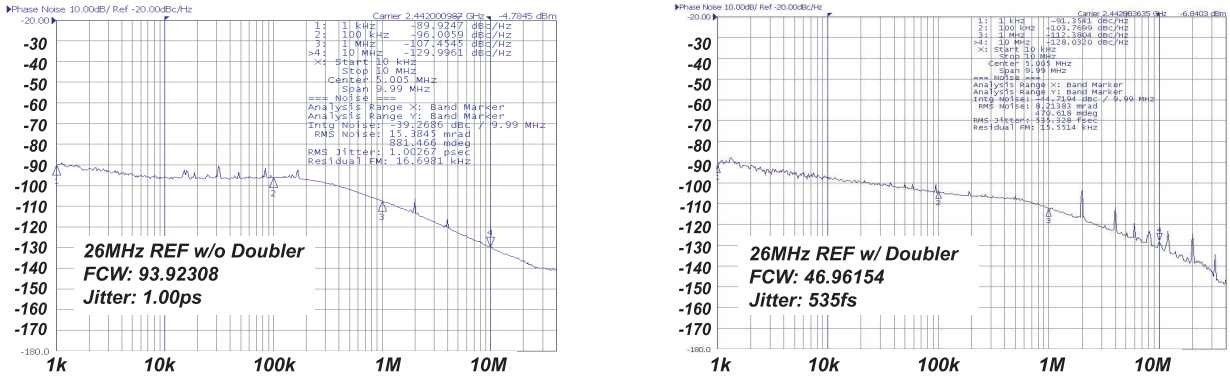
Fig. 19. Measurement result of the proposed DTC at 52 MS/s.

signal to turn on the CNT when the magnitude of the phase error is larger than the dead-zone of 64 ps. The CNT quantizes the length of the EN signal and produces phase error information to the filter. The large phase error will saturate the 4b narrow-range TDC, and the main PLL will be idle. When the phase error is sufficiently small, the main loop will lock the residue phase error. The EN signal is low after the phase locked and the CNT stop working. The loop filter will be automatically disabled, and the gating logic will minimize its power consumption. Since this loop will never be turned off, the ADPLL will not suffer from the sudden large frequency and phase jump. The simulated power consumption of the coarse-DPLL is 5 μW after phase locked. The transient simulation result of the coarse-DPLL is shown in Fig. 17. A frequency error of 13 MHz is assumed before phase locked, and the coarse-DPLL only takes 3 μs to assist the main PLL frequency and phase locking process.

V. MEASUREMENT

The proposed fractional-N ADPLL prototype was fabricated in a 65-nm CMOS process. The proposed 10b isolated constant-slope DTC and path-select TDC are also fabricated in 65-nm CMOS process as individual test circuits for INL measurement. In Fig. 18, the path-select TDC realized a 4b with 2.15-ps resolution at 52 MS/s. The peak INL is around 0.65 ps, thanks to the reduction of TDC range by the assist of DTC. The linear operation of the TA and TA gain also helps to reduce the linearity degradation coming from the coarse quantizer. Sub-ps resolution DTC is not easy to measure due to the finite sampling frequency of the oscilloscope. A frequency-domain-based measurement method was introduced in [30]. Fig. 19 shows the measurement results of the proposed 10b DTC. The DTC achieves a 580-fs time resolution with a peak INL of 0.87 ps. It corresponds to an effective resolution of 9.4b regarding the linearity performance, and the DTC only consumes 140 μW at 52 MS/s. The detailed comparison of the proposed DTC with the state-of-the-art DTC is listed in Table I. Among the DTC architecture, our proposed DTC achieves the best linearity while consuming the lowest power consumption.

The fractional-N ADPLL is measured under one of the BLE channels at 2442 MHz, as shown in Fig. 20. To save the power consumption, reference doubler is bypassed by the MUX logic. The 26-MHz reference is directly used for DTC, TDC, and digital circuits. The phase noise plot is shown in Fig. 20(a),



(a) (b)

Fig. 20. (a) Measurement result of the proposed ADPLL w/o reference doubler at a BLE channel. (b) Measurement result of the proposed ADPLL w/ reference doubler at a BLE channel.

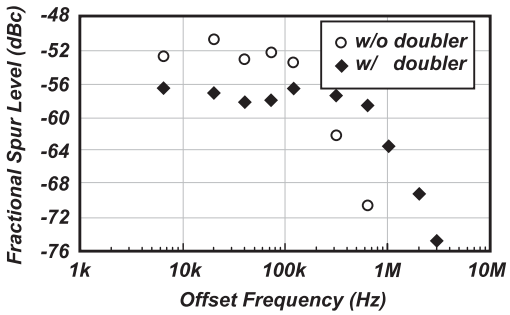


Fig. 21. Measurement result of the fractional spurs versus spur frequencies.

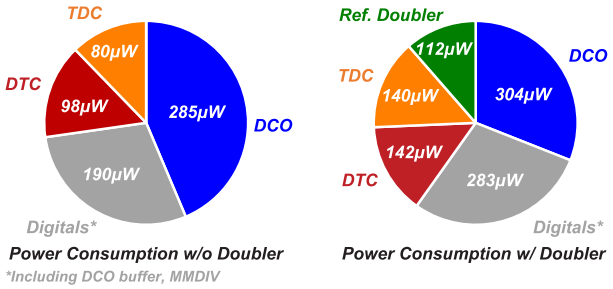


Fig. 22. Measured power breakdown of the proposed fractional-*N* ADPLL.

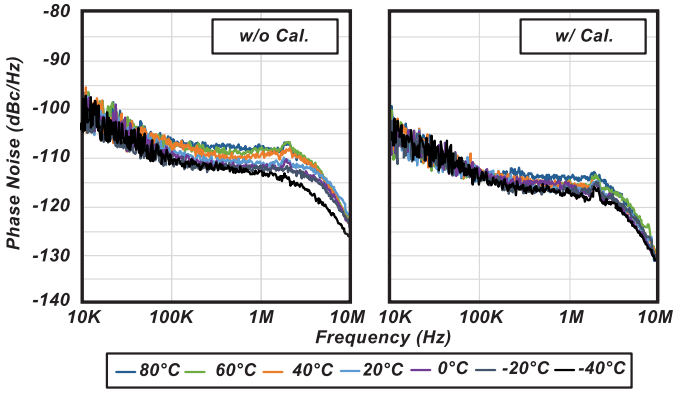


Fig. 23. Measured ADPLL phase noise under the temperature variation w/ and w/o the TDC gain calibration scheme.

and an integrated jitter from 10 kHz to 10 MHz of 1.00 ps is achieved. The measured fractional spurs are shown in Fig. 21 by sweeping the FCW. A worst case spur of −50 dBc is achieved without reference doubler. The power consumption is extremely low for the achieved spur and jitter performances, which can be adopted for BLE applications. To boost the effective resolution of the TDC by increasing the sampling frequency, reference doubler is utilized. Fig. 20(b) shows the phase noise plot at the same BLE channel of 2442 MHz. An integrated jitter of 535 fs is achieved. The integrated phase noise from 10 kHz to 10 MHz is −44 dBc, which is demanded for IEEE802.11b/g/n applications. When a small FCW of 47.000112 is used, the measured worst integrated jitter is 590 fs. However, for the target applications, such as BLE and Wi-Fi, such a small fractional number is not required.

A worst fractional spur of −56 dBc is measured, as shown in Fig. 21, with the reference doubler. The detailed power breakdown of each building block in the signal path of the proposed ADPLL is shown in Fig. 22. The supply voltage for DTC and TDC are 1.0 V to maintain a good linearity. A 0.8-V supply is assigned to the DCO and the digital parts, which include the DCO buffer, MMDIV, and the synthesized digital circuits, in order to keep a low power consumption. At a sampling rate of 26 MS/s, the DTC and TDC consume 98 and 80 μW. The DCO bias is optimized for very low power operation of 285 μW. The digital parts consume 190 μW with a 20-μW calibration. The total power is 0.65 mW for the jitter performance in Fig. 20(a). For a sampling rate of 52 MS/s, the DTC and TDC consume 142 and 140 μW. An additional power of 112 μW from the reference doubler is consumed to double 26–52 MHz with a 1.0-V supply. The DCO bias is optimized for achieving a better out-of-band phase noise. The digital parts consume 283 μW with a 40-μW calibration. The total consumed power is 0.98 mW for the jitter performance in Fig. 20(b).

To demonstrate the effectiveness of the proposed TDC gain calibration, in-band phase noises under temperature variations are measured, as shown in Fig. 23. The phase noise of ADPLL in integer-*N* mode with wide loop-bandwidth is measured,

TABLE II
COMPARISON TABLE OF THE STATE-OF-THE-ART FRACTIONAL-*N* ADPLLS

Reference	This Work		[3]	[4]	[5]	[6]	[7]	[8]
Technology	65nm		28nm	40nm	40nm	28nm	65nm	130nm
Architecture	Isolated constant-slope DTC + 4b TDC		Full range TDC	VS[1]-DTC +TDC	VS-DTC +TDC	VS-DTC TDC	VS-DTC +TDC	VS-DTC +BBPD
Ref. frequency	26MHz w/ Doubler	26MHz w/o Doubler	40MHz	32MHz	N.A.	40MHz	50MHz	40MHz
Frequency	2.0-2.8GHz		2.05 -2.55GHz	2.1 -2.7GHz	1.8 -2.5GHz	2.7 -4.33GHz	4.4 -5.2GHz	2.9 -4.0GHz
Integrated Jitter (Integrated BW)	**0.53ps** (10k-10M)	1.00ps (10k-10M)	0.86ps (10k-10M)	1.71ps (1k-100M)	1.98ps (10k-10M)	0.16ps (10k-10M)	0.49ps (10k-20M)	0.56ps (30k-30M)
In-band fractional spur	**-56dBc**	-50dBc	N.A.	-37dBc	-56dBc	-54dBc	-51.5dBc	-42dBc
Power	**0.98mW**	**0.65mW**	1.6mW	0.86mW	0.67mW	8.2mW	3.7mW	4.5mW
Ref. spur	-72dBc	-68dBc	-78dBc	-70dBc	-62dBc	-78dBc	-69dBc	-72dBc
FOM	**-246dB**	**-242dB**	-239.3dB	-236dB	-236dB	-246.8dB	-240.5dB	-238.5dB
Active area	0.23mm^2		0.33mm^2	0.2mm^2	0.18mm^2	N.A.	0.22mm^2	0.22mm^2

1. Variable-slope.

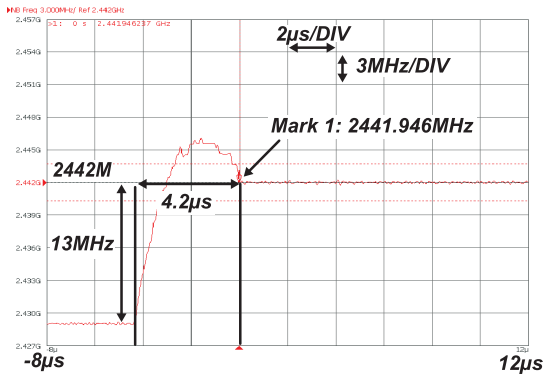


Fig. 24. Measured lock transient from an initial frequency error of 13 MHz.

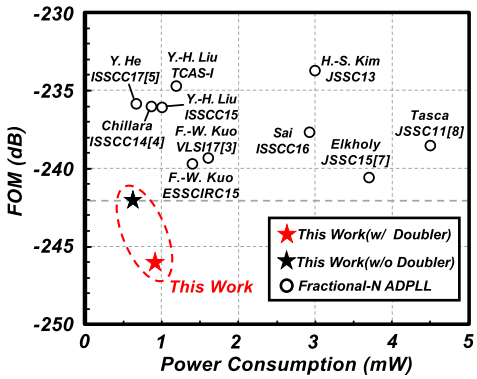


Fig. 26. FOM comparison with the state-of-the-art fractional-*N* ADPLLs under 5 mW.

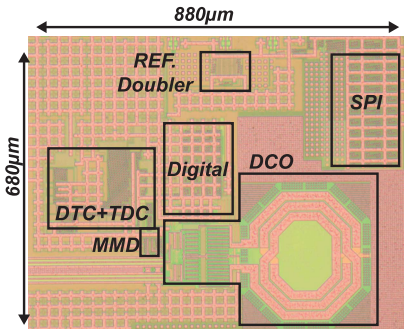


Fig. 25. Chip micrograph.

where the in-band phase noise is purely decided by the TDC resolution. When increasing the temperature from −40 °C to 80 °C, the in-band phase noise varies from −112 to −108 dBc/Hz at 500-kHz offset frequency without the calibration scheme. The in-band phase noise varies from −111 to −109 dBc/Hz at 500-kHz offset frequency with the calibration. Fig. 24 shows the measured phase locking transient of the ADPLL. A 13-MHz frequency error is input to the FCW of the ADPLL, which is over twice of the entire frequency coverage of the DCO fine bank. With the help of the proposed coarse PLL, a measured lock-up time of 4.2 μs is achieved when the ADPLL locks to the 54 kHz away from the target frequency. The fast phase converges speed can be adopted in frequency hopping applications [31], such as BLE. The frequency hopping will cause the LMS calibration of the DTC gain to re-lock again for the new synthesized frequency. The simulated re-lock time for the LMS calibration takes less than 15 μs to converge to a 0.3% gain error with 13-MHz frequency jump. However, even if the LMS does not converge to the final value, the PLL will still lock to the target frequency without any issue, while the fractional spur will be degraded during settling. The chip photograph of the fractional-*N* ADPLL is shown in Fig. 25. The detailed performance comparison with the state-of-the-art fractional-*N* ADPLLs is shown in Table II. Fig. 26 compares the FOM performance when only fractional-*N* ADPLLs under 5 mW are included. The proposed ADPLL achieves a 10-dB better FOM than the conventional sub-mW ADPLLs.

VI. Conclusion

To realize the sub-mW fractional-*N* ADPLL with low jitter and low spurs, the first-order DSM-based fractional controller works in conjunction with a highly linear DTC is introduced. The rms jitter can be improved, compared to use higher-order DSM, while a DTC with high linearity is required. To realize a linear and high-energy efficient DTC, an isolated constant-slope method is proposed. Thanks to the isolated operation of DTC, the proposed DTC can potentially work at a high sampling frequency with small power consumption while maintaining good linearity with high energy efficiency. Furthermore, the auto-zero offset switch mitigates part of the supply noise, which can improve the linearity in the SoC environment. The proposed fractional-*N* ADPLL achieves good fractional spurs while maintaining a low jitter performance and low power, which proves the linearity and power efficiency of the DTC. The gain calibration of TA demonstrates a steady in-band phase noise of the ADPLL over the temperature variations. The measurement of lock time proves the effectiveness of the always-on a coarse PLL in the feedback loop.

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