ELectronics EXpress

LETTER

IEICE Electronics Express, Vol.14, No.8, 1–8

A 2.4 GHz fractional-N PLL with a low-power true single-phase clock prescaler

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Abstract: A 2.4 GHz fractional-N PLL implemented in 65-nm CMOS process is presented in this letter. A TSPC dual-modulus prescaler is proposed to reduce the PLL's power consumption by merging one of the branches of the true single-phase clocked (TSPC) D flip-flops. The measured synthesizer output frequency ranges from 2.16 to 2.7 GHz, and consumes 8 mW from a 1.3 V power supply. The in-band phase noise is −98 dBc/Hz at 100 kHz offset, and −115 dBc/Hz at 1 MHz offset at a carrier frequency of 2.438 GHz. The circuit achieves the RMS jitter of 0.86 ps and figure of merit of −230 dB, with the fractional spurs below −55 dBc.

Keywords: fractional-N frequency synthesizer, TSPC prescaler, low power, PLL

Classification: Integrated circuits

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DOI: 10.1587/elex.14.20170065
Received January 21, 2017
Accepted January 31, 2017
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1 Introduction

The PLL frequency synthesizer in 2.4 GHz ISM band has been widely employed in RF transceivers, such as for Zigbee and 802.11b/g WLAN standards, et al. As the process scale down, the main challenge of the frequency synthesizer lies in the phase noise performance and the power consumption. The integrated phase noise or jitter degrades the signal error-vector-magnitude (EVM) of the transceiver [1, 2]. The in-band noise can be suppressed by increasing the Charge Pump current and loop filter size, and the out-band noise can be suppressed by increasing the VCO's tank Q and current, while both needs more chip area and power consumption.

The VCO and the divider are the power-intensive blocks in the synthesizer design. With the improved speed of the MOS devices, in several GHz applications, the current-mode-logic (CML) divider can be replaced with the true single-phase clocked (TSPC) logic to reduce the power consumption. Several TSPC prescaler topologies have been proposed to offer high speed and low power [3, 4, 5, 6, 7]. In [5] a dual-modulus divide-by-2/3 prescaler exploiting the forced-discharging method in the second branch of a TSPC flip-flop, can substantially improves the maximum speed of the standalone prescaler. And in [6], one of the branches of TSPC D flip-flops is merged based on this circuit, to further reduce the power consumption. Alternatively, a charge-control technique in the DFF branch is proposed to eliminate the short current in divide-by-3 mode [7].

In this letter, a new TSPC prescaler with a low power consumption is proposed by merging one of the branches of the TSPC prescaler. Compared with the conventional ones, the prescaler contains fewer transistors. In section 2, the fractional-N synthesizer design for 2.4 GHz ISM band applications is presented. The dual-modulus prescaler and other building blocks of the PLL are introduced in Section 3 and Section 4, respectively. Section 5 discusses the experimental results, and the conclusions follow in Section 6.

2 PLL architecture

The block diagram of the PLL frequency synthesizer is shown in Fig. 1. To avoid the frequency pulling from the power amplifier, the PLL operates at 3.2-GHz, provides the 2.4 GHz ISM band through frequency mixing. The PLL output is divided by two and then up-converted with the original 3.2-GHz signal to generate a 4.8-GHz frequency. The 4.8-GHz signal is then divided by two to generate the 2.4-GHz I/Q LO signals for the transceiver. Thus the VCO runs at 4/3 of the RF channel, far from the multiples of the RF frequency.

DOI: 10.1587/elex.14.20170065
Received January 21, 2017
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The main building blocks of the PLL include the PFD, the charge pump (CP), the programmable loop filter (LF), the VCO, the sigma-delta modulator (SDM), and the divider. A 40 MHz crystal oscillator is adopted as the reference frequency generator, and a 3-bit MASH-1-1-1 architecture is used for the SDM. The $\sum\Delta$ modulator employs a 24-bit digital word, producing a minimum frequency step of 23.8 Hz relative to the VCO frequency. The divider consists of a dual-modulus prescaler and digital programmable counter. For the synthesizer, the divider input frequency is around 3.2 GHz, a TSPC divide-by-4/5 prescaler is chosen for its low power consumption.

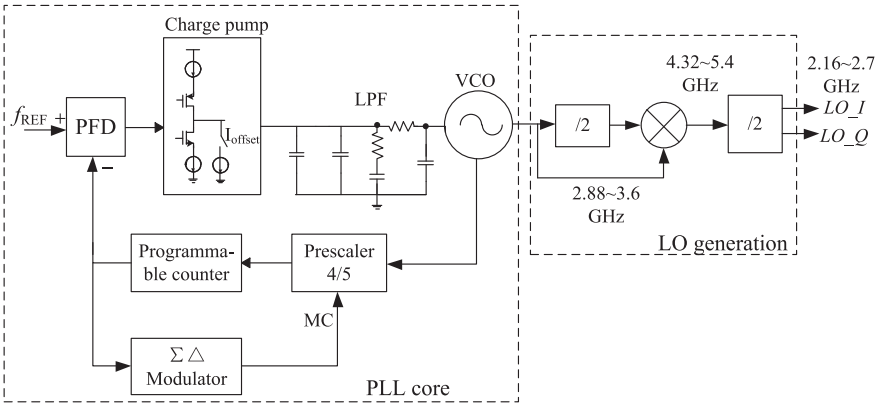

Fig. 1. Frequency synthesizer architecture.

3 Dual-modulus prescaler

The divider is the main power block in the synthesizer design. The conventional 2/3 prescaler proposed in [7], shown in Fig. 2, can improve the division speed with reduced power consumption. The prescaler consists of two TSPC DFFs (DFF1 and DFF2). When "MC" is "low", the prescaler operates in the divide-by-3 mode. Once the DFF1 output "Q1B" gets high, the DFF2 precharge node "P2" is delayed by one clock cycle, extending the division ratio to 3. From Fig. 2, the first branch of the two DFFs are both connected with the prescaler output "Q2B", and shows the same switching activity when "MC" is "low". Thus the branches consisting of M2, M4 and M5 can be merged with the branches consisting of M12, M13 and M14. The transistor M1 and M3 for modulus control can be absorbed in the second branch of DFF1.

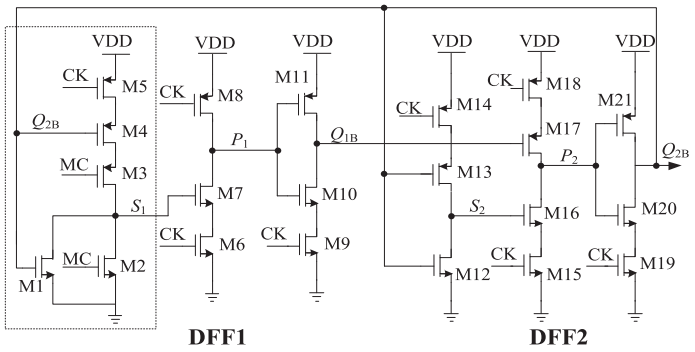

Fig. 2. Conventional divide-by-2/3 prescaler from [7]

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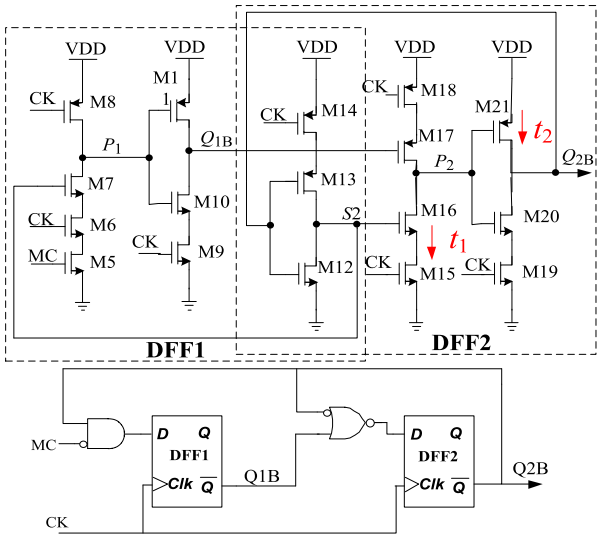

Fig. 3. Proposed divide-by-2/3 prescaler and topology

The proposed 2/3 prescaler is shown in Fig. 3. The latch composed of M12, M13 and M14, is shared by the two DFFs. This allows the load transistors of the output "Q2B" reducing from four to a half. The transistor M17 added in the precharge branch, series with the transistor, is to create an NOR gate at the DFF2 input. The modulus control logic is absorbed by the second stage of DFF1, where the transistor M5 is in series with the second branch of DFF1. The transistor M5 series in the node P1 creates an equivalent AND logic gate at the DFF1 input. When MC is low, the DFF1 output Q1B is tied to a low voltage, and the prescaler works in divide-by-2 mode.

As in [3], the maximum operating frequency is limited by the maximum propagation delay of the six phases. For a divide-by-3 operation, the maximum propagation delay is $t_1 + t_2$ as shown in Fig. 3. The load transistors and capacitance at prescaler output Q2B is reduced to a half in this work, so the propagation delay t_2 is decreased. The speed of the prescaler can benefit from the decreasing of propagation delay of t_2. Compared to the reported TSPC 2/3 prescaler [3, 4, 5, 6, 7, 8], the proposed 2/3 prescaler contains the least number of transistors, and the number of the latches is reduced from 6 to 5 stages.

The proposed TSPC 2/3 prescaler in Fig. 2 and Fig. 3 are compared with simulation results through the Cadence Spectre simulator, both carried out in a standard 65 nm CMOS process. The circuits are simulated in a typical–typical process corner with a 1.2 V supply at 290 K. Fig. 4 shows their power consumption versus operating frequency in divide-by-3 mode. It is seen that the proposed prescaler can reach up to 28.5 GHz in divide-by-3 mode, while for the prescaler in [7] the maximum operating frequency is 25.5 GHz. Thanks to the latch sharing technique, the simulated power consumption of proposed prescaler is reduced by 15% than [7].

In our designed frequency synthesizer, the synchronous divide-by-4/5 circuit is employed based on this technique as shown in Fig. 5, consisting of three TSPC DFFs. The DFF1 and DFF2 share the latch branch composed of transistors M12, M13 and M14, and the DFF3 is a conventional TSPC DFF.

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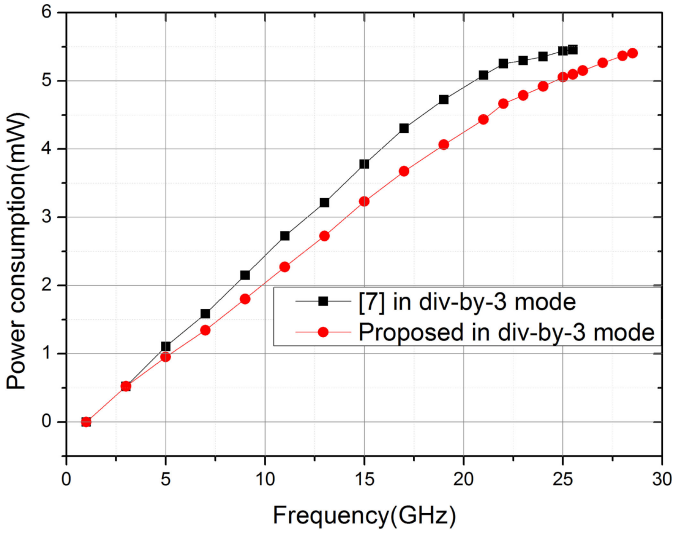

Fig. 4. Simulated power versus operating frequency

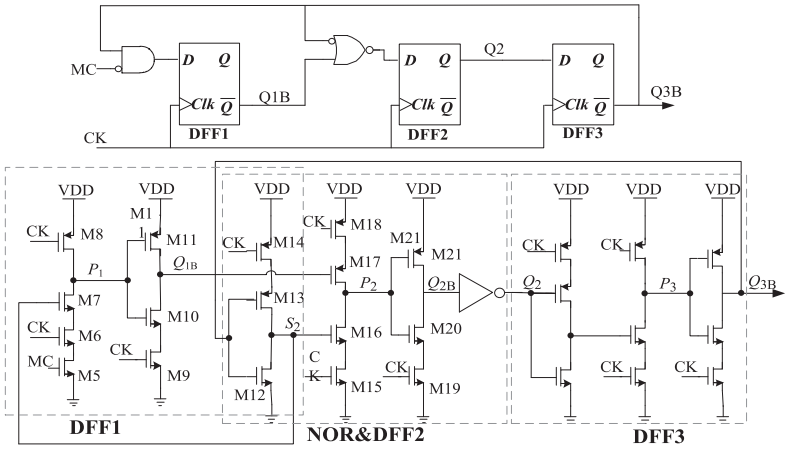

Fig. 5. Proposed divide-by-4/5 prescaler and topology

4 Other building blocks of the PLL

The circuits of the VCO and the charge pump are shown in Fig. 6. The CMOS LC-VCO architecture with both NMOS and PMOS switch pairs is chosen for its lower power consumption than single-switch-pair oscillator [9]. For the LC-VCO, the resistor-switching for the current control is used, since it contributes less flicker noise than current mirror, and the chip area of the RC filter for the bias circuits is much more reduced. The VCO current can be varied from 1 mA to 3 mA by a 3-bit resistor bank. A low-dropout regulator is employed to provide the supply voltage for the VCO. The VCO uses a 6-bit binary-weighted MIM capacitor bank for the coarse tuning and varactors for the fine-tuning of the frequency. The VCO is designed to have an average gain (K_{VCO}) of 50 MHz/V.

Fig. 6(b) shows the schematic of charge pump (CP) for PLL. The CP employs a current steering topology. The cascode current source and the dummy nodes with a unity gain buffer are adopted to minimize the charge sharing and current mismatches. The CMOS switches are used for current switching to mitigate the charge injection and clock feed-through effect. Two-bit offset current is added at the

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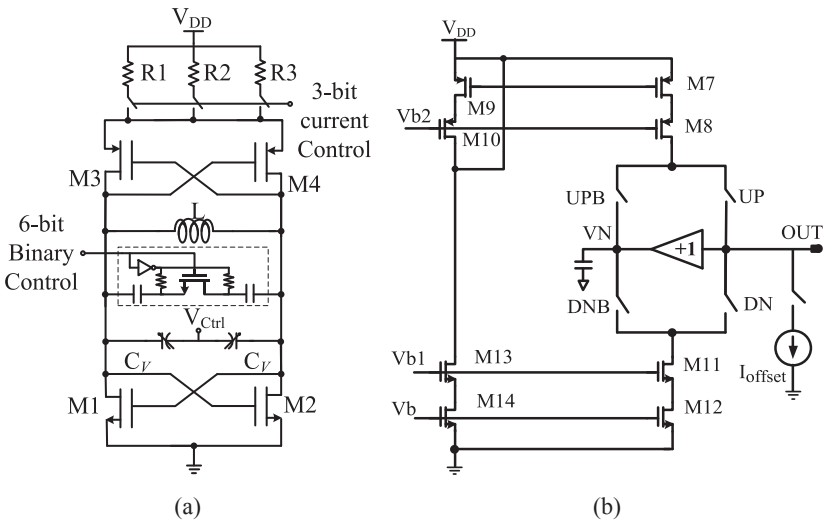

Fig. 6. (a) Schematic of the VCO
(b) Schematic of the charge pump

CP output to shift the operating point, thus avoiding the noise folding from the delta-sigma modulator due to the CP current nonlinearities. The CP current can be tuned from 80 µA to 640 µA at a step of 80 µA. A third-order passive on-chip loop filter is employed in the PLL.

5 Measured results

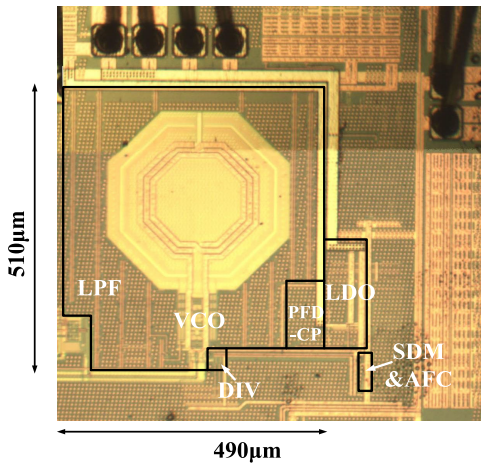

Fig. 7. Die photograph of the PLL

The fractional-N frequency synthesizer is integrated with a low power transceiver designed to support the 802.11bgn standard. Fig. 7 shows the die photograph of the prototype chip, fabricated in a 65-nm CMOS technology. The synthesizer core occupies an active area of about 0.25 mm^2 excluding the frequency mixing block. The PLL core tuning range is between 2.88 and 3.6 GHz, and provides a 2.16–2.7 GHz frequency for the transceiver through the frequency mixing block. The phase noise performance of the synthesizer is measured from the transmitter output. Fig. 8(a) and Fig. 8(c) shows the measured phase noise performance at maximum and minimum frequency, respectively. From the carrier frequency at

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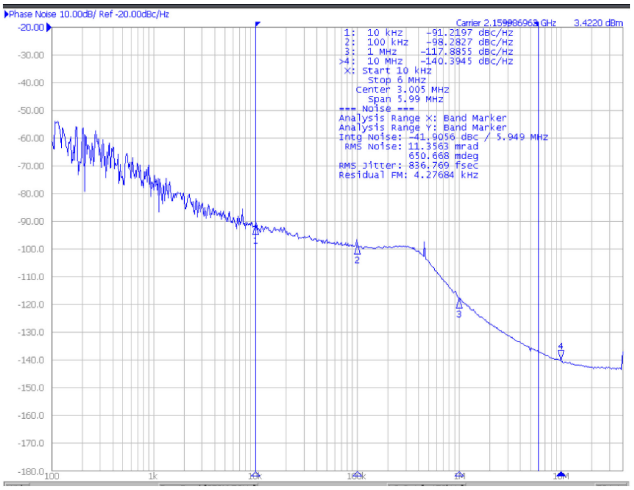
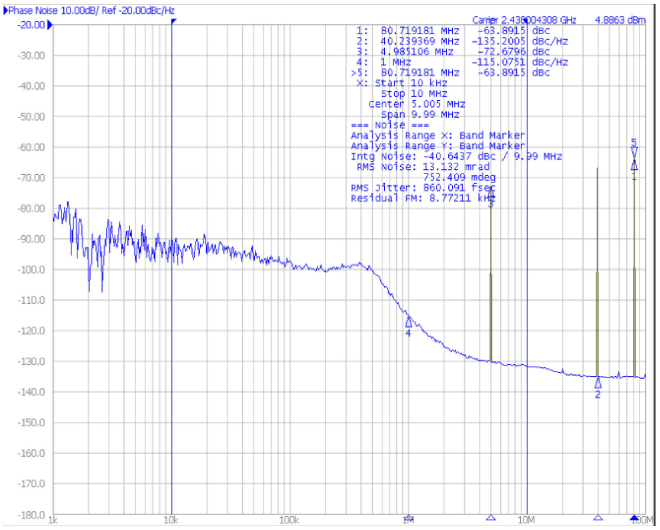
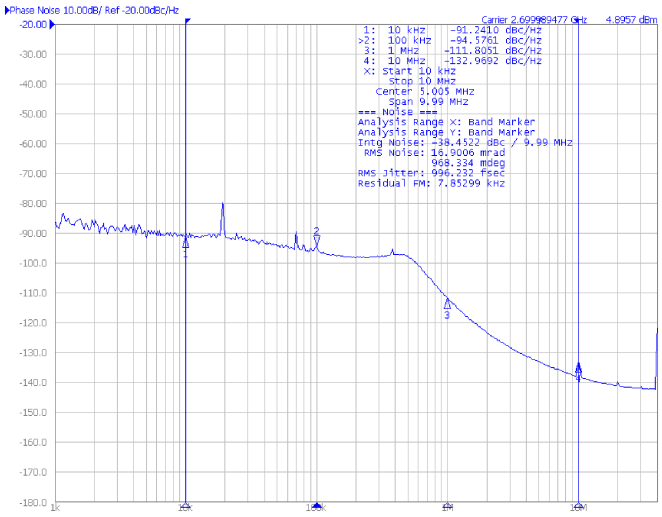


(a)



(b)



(c)

Fig. 8. Measured phase noise of the frequency synthesizer: (a) at 2.16 GHz, (b) at 2.438 GHz, (c) at 2.7 GHz

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2.438 GHz, the measured phase noise is −98 dBc/Hz at 100 kHz offset frequency, and −115 dBc/Hz at 1 MHz offset frequency as shown in Fig. 8(b). The RMS jitter integrated from 10 kHz to 10 MHz is 0.86 ps. The measured worst-case fractional spur level is −55 dBc. The reference spur is less than −67 dBc at 40 MHz offset. The total power consumption of the PLL (excluding the frequency mixing block) is 8 mW from a 1.3 V supply. The divider including the prescaler and the VCO buffer dissipate 1.5 mA. The VCO core and the LDO draw 3 mA from a 1.3 V supply voltage. The mixer for the LO generation consumes 1.5 mA. The FoM is typically used for PLLs, defined as $FoM = 20\log_{10}(\sigma_t/1\,\mathrm{s}) + 10\log_{10}(P_{\mathrm{PLL}}/1\,\mathrm{mW})$, where σ_t is the integrated RMS jitter variance in squared seconds and P_{PLL} is the dissipated power. The calculated FoM of the PLL is −230 dBc/Hz. A summary of the measured results and performance comparison are given in Table I.

Table I. Performance summary and comparison with analog fractional-N PLL

	[1]	[2]	[10]	This work
CMOS Process (nm)	40	130	65	65
Output freq. (GHz)	3.276–3.883	2.4	3.0–4.0	2.16–2.7 2.88–3.6 (PLL core)
Reference freq. (MHz)	26	60	40	40
Phase Noise (dBc/Hz)	−105 @ 100 kHz	−102 @ 100 kHz	−103.5 @ 100 kHz	−98 @ 100 kHz
	−123 @1 MHz	−130 @10 MHz	−139 @20 MHz	−115@1 MHz −132@10 MHz
RMS jitter (ps)	0.3 (1 k-10 M)	—	0.973 (3 k-30 M)	0.86 (10 k-10 M)
Power (mW)	7.2	9.6	5	8
FOM*	−242	−220	−235.1	−230
Area (mm^2)	0.29	0.46	0.22	0.25
Prescaler type	—	TSPC 8/9	CML	TSPC 4/5

6 Conclusion

This work demonstrates a fractional frequency synthesizer for 2.4 GHz ISM band applications in a 65-nm CMOS technology. A low power TSPC prescaler is proposed to reduce the PLL's power consumption by sharing one of the branches of the DFFs, which realized by the least number of transistors to the best of our knowledge. The PLL achieves an 0.86 ps RMS jitter at 2.438 GHz, integrated from 10 kHz to 10 MHz at a power consumption of 8 mW from a 1.3 V supply, with the fractional spurs below −55 dBc.

Acknowledgments

This work was supported by the Natural Science Foundation of Jiangsu Province (BK20130880 and 14KJB510025).

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