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Design and Performance Analysis of A Low Power, Low Noise 1.6GHz Charge Pump Integer-N PLL in Different PVT Corners

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Abstract— **A fast locking low phase noise 1.6GHz PLL has been presented in this paper. The PLL was designed in 28nm technology with 1V nominal supply voltage. The phase noise of the PLL has been reduced by implementing current starved ring oscillator VCO. The lock time of the PLL is reduced by using a current steering charge pump (CP). The PLL has been designed and simulated in different PVT corners. The simulation results show that the PLL achieves lock state at only 951ns in standard typical PVT (Process, Voltage and Temperature) corner. A low phase noise of only -60.67dBc/Hz at 1MHz has been achieved. It consumes a very low area of only 50u x 45u. The layout of the circuit along with pre and post layout simulation results have been incorporated in this paper.**

Keywords— Phase Frequency detector(PFD), Charge Pump(CP), Voltage controlled Oscillator(VCO), Frequency divider, lock time, phase delay

I. INTRODUCTION

The PLL is most commonly used as a frequency synthesizer in radio frequency or wireless applications and in electronics devices such as memories, hard disk drives, and wireless transceivers where it is responsible for stepping up the clock frequency by using a divider in the feedback loop [1]. It generates, stabilizes, modulates, demodulates, filters or recovers a signal from a noisy communications channel. The functional blocks of a PLL consists of five basic components, i.e. phase frequency detector (PFD), charge pump (CP), low pass filter (LPF), voltage controlled oscillator (VCO) and Frequency Divider (FD). Modern communication demands high speed performance in data transmission with low power consumption, low jitter, low cost, and small chip area [2]. The PFD plays a critical role affecting important performance parameters, such as jitters, phase noise and lock time. Basic PFD consists of dead zone due to which the PFD fails to detect below a certain phase difference which results in increased phase noise [3]. The high value of loop gain of VCO (KVCO) contributes to high jitter of the PLL [4]. Various non-idealities are caused by The Charge Pump such as DC mismatch of the charging/discharging currents and glitches, which degrade the performance of the overall loop thus, results in slower performance and increased phase noise [5].

Considering all these, we have designed a PLL in 28nm CMOS technology where we implemented a tri state PFD which has zero dead zone. We adopted a current steering CP technology to achieve fast-locking PLL and a low noise current starved CMOS VCO which greatly reduces the output noise and thus increases the stability of the PLL.

The paper has been organized in the following way: In section 2 the proposed topology of all the PLL blocks has been discussed. section 3 presents the functional operation of a conventional PLL. Section 4 comprises of the simulation results obtained from pre layout and post layout simulations and finally, in section 5, a summary of all the findings has been made to conclude the paper.

II. FUNCTIONAL BLOCKS OF PLL

A. Phase Frequency Detector (PFD)

Phase frequency detector is a key building block of a PLL that affects the overall performance of PLL, such as jitters, phase noise and lock time. A PFD detects both phase and frequency difference between the input reference signal and the feedback signal, which generates output voltage pulses with width proportional to the phase difference. A wide detection range of the phase difference of a PFD is a critical factor for PLL. In conventional PLL, the main problem is the presence of the dead zone which is defined as the maximum phase difference between the two inputs that cannot be detected by a PFD. Due to the presence of dead zone, the PFD fails to detect the phase error caused by a very small value of phase difference, which makes the loop essentially open and increase the phase noise of the PLL [6]. To avoid the dead zone, in this paper, a Tri state D-Flip Flop based PFD with delay logic added to reset path has been used which makes the delay in the rest path to be longer than the switching time of the charge pump currents. Due to the delay, there will be short pulses both on up and down signal, even when the PLL is in locked state. Fig. 1 shows the block diagram of the PFD architecture we have used in our PLL design.

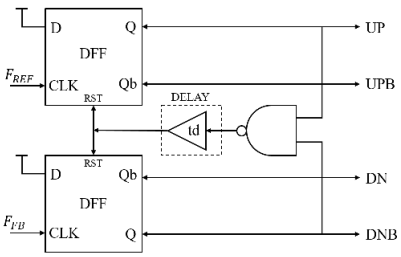

Fig. 1. Phase Frequency Detector Topology with zero dead zone.

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B. Current Steering Charge Pump (CP)

A charge pump, consisting of a current source or sink, charges or discharges the loop filter according to its inputs which are the output of the PFD. The digital outputs from the PFD is converted to current signals which turns on or turns off the current source and sinks in the charge pump. The CP maintains a continuous flow of current which changes direction only when needed. Charge-Pump PLLs offer an infinite pull-in range and zero steady-state phase error compared to classical voltage phase-detector PLL. In this paper we used a differential current steering Charge Pump which provides the advantage of operating at low swing input signals which makes it useful for PLL with a high speed reference clock [1]. Fig. 2 shows the circuit diagram of the current steering Charge Pump topology we have used.

The *up* and *dn* switch circuits of The PFD are designed with a mirror level tracking structure where the *upb* and *dnb* of *up* and *dn* are added to the output of the PFD, in order to charge shunt and increase the switching speed and effectively suppress the switching noise [7].

C. Loop Filter

The loop filter plays a vital role in PLL since inappropriate values of loop filter may cause the PLL to increase its lock time [8]. Also due to variations in the loop filter, the PLL might leave the lock state. The loop filter mainly converts the current generated by the CP to the control voltage of the VCO that controls the oscillation frequency of the VCO. A second order low pass filter has been used in this design. The second capacitor of the LPF smooths out the current spikes and the two poles, one at low and the other at high frequency and a zero altogether increases the stability of the system. Fig. 3 shows a second order low pass filter [8]. The transfer function of the loop filter is given by [9],

$$F(s) = \frac{s + \tau_1^{-1}}{C_2 s(s + \tau_2^{-1})} \qquad (1)$$

Where, $\tau_1 = RC_1,\ \tau_2 = \frac{C_1 C_2}{C_2 + C_2}$

D. Voltage Controlled Oscillator (VCO)

The VCO is a very crucial building block of a PLL since on it, depends the various important performance parameters like phase noise, jitter, tuning range, tuning linearity, power consumption, etc. of the PLL. Higher value of loop gain of VCO (K_{VCO}) contributes to higher jitter in the PLL. Compared to the several topologies of VCO available, we used the Current Starved VCO with 5 inverter stages connected in ring oscillator configuration in our design since it offers lower loop gain and thus less jitter, wider tuning range and less area requirement than the LC resonant VCO , Ring Oscillator based VCO and other topologies [4]. The added inverter architecture added the drive strength of the VCO output signal which can be used to drive higher loads. Fig. 4 shows the base circuit topology used for designing the current starved ring oscillator based VCO. The oscillation frequency of the current starved VCO (fosc) for N inverter stages is given by bias current (Id), total capacitance (*Ctot*) and control voltage (*Vctrl*) [10].

$$f_{osc} = \frac{I_d}{2NC_{tot}V_{ctrl}} \qquad (2)$$

In Fig 5, the voltage control versus frequency curve is shown from where we get the gain of the designed VCO from the slope of the curve which is 26.3Ghz/V.

E. Frequency Divider

The high-speed frequency divider is a very significant block in a PLL for generating any range of frequencies from a oscillator. The purpose of the N divider in a phase-locked loop (PLL) is to divide the high frequency of the VCO down to a frequency which closure to the reference frequency which usually generated from crystal oscillator and can generate very low frequency. In this design we used a divide by 16 divider for our 1.6GHz generating PLL, to obtain a feedback clock of 100MHz. We used D-flipflop for the divider design to obtain faster speed and reduce area and power consumption [11].

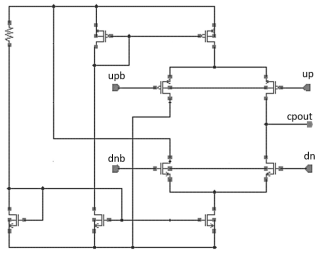

Fig. 2. Current Steering Charge Pump

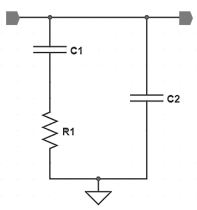

Fig. 3. Second order filter used as loop filter in this design

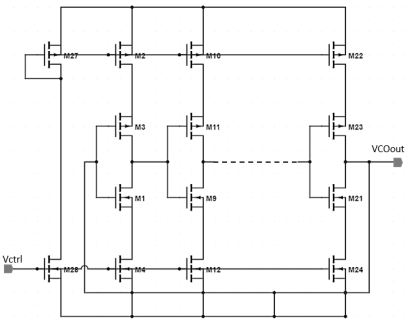

Fig. 4. Current Starved Ring Oscillator Based VCO

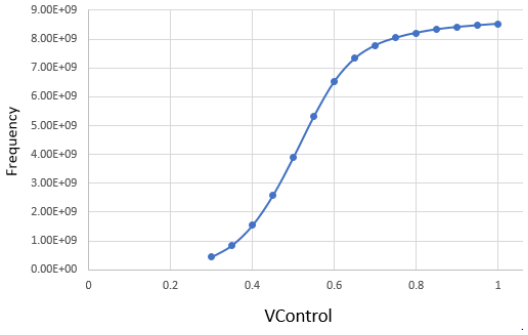

Fig. 5.VControl vs Frequency graph for VCO

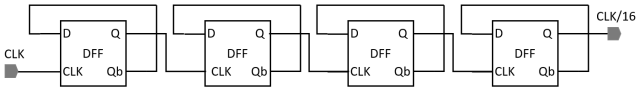

Fig. 6. 1/16 Frequency divider using positive edge triggered DFF.

III. Functional Operation

The PFD compares the reference signal F_{REF} with that of the divided down VCO signal (*Fvco/N*) and simultaneously generates up, dn, and the upb, dnb signals to control the charge pump. Based on the difference in phase between these two signals, the CP charges and discharges, thus changes the magnitude of the voltage V_C. The V_C passes through a low pass filter to eliminate all the high frequency components and is then given to the VCO as control voltage, depending on which, the VCO produces its output frequency [7].

IV. Simulations and Results

Fig. 7 shows the waveform of transient analysis of the designed PLL. It includes the reference frequency, followed by the feedback frequency, charge pump output and finally the PLL output frequency. All the simulations are carried out in different simulation model PVT corners and parasitic corners. In the figure and discussion, TT means Typical performance for both NMOS and PMOS. FF means both are fast and SS means both are slow. Generally, these threes corners cover all the significant variation of FEOL stack [12]. A broader discussion and data analysis has been carried out in the later part in this section.

A. Pre-layout simulation and result

The output frequency of the PLL is given by the equation:

$$F_{OUT} = N \times F_{REF} \quad (3)$$

In this design F_{REF}=100 MHz , N =16. So, F_{OUT} = 1.6GHz. The PLL has been simulated in TT/25C/1.0V, FF/125C/1.1V and SS/-40C/0.9V PVT corners. Table I. illustrates the pre-layout frequency data in all these corners.

B. Layout area and Post-layout performance evaluation

The layout of the designed PLL is shown in Fig. 12. The complete area of the PLL obtained after layout is (50x45) um. The PLL simulation results in all the three corners vary in the post layout simulation from the pre layout simulation to some extent. The post layout simulation data is presented in the Table II. A comparison among the pre-layout data and post-layout data can be seen from Fig. 7 to Fig. 11 in a sequence of frequency, lock time, average current and leakage current. We can see that the worst case deviation for output frequency (speed) occurs at SS/-40C/0.9V PVT corner which is 2.5%.

The phase noise analysis of the VCO shows -60.67 dBc/Hz at 1MHz at TT corner, -57.55 dBc/Hz at 1MHz at FF corner and -64.62 dBc/Hz at 1MHz at TT corner. A comparative performance study of this PLL design has been shown to the Table III with recently designed PLLs in different technology.

TABLE I. Pre-layout simulation data in different PVT corners

Process Corner	Temperature (C)	Voltage (V)	Frequency	Lock Time	Average Current	Leakage Current
TT	25	1	1.61G	986n	837u	435u
FF	125	1.1	1.62G	506n	1.2m	657u
SS	-40	0.9	1.6G	2.09u	471u	449u

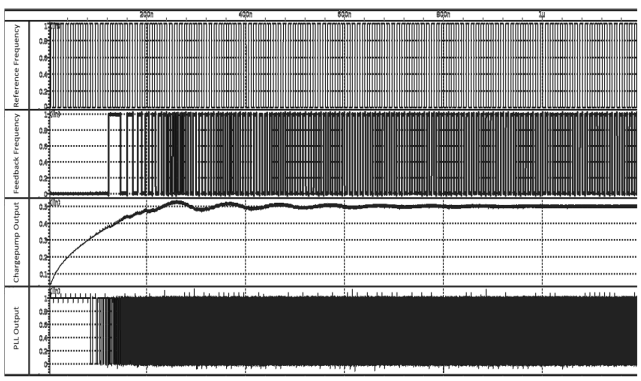

Fig. 7. Transient simulation result for 1.6GHz PLL in TT/25C/1.0V corner.

V. Conclusion

A 1.6GHz fast locking, low noise phase locked loop is designed in 28-nm technology. The design incorporated zero dead-zone PFD, current steering charge pump and current starved VCO in particular. The layout has been designed in a compact area. The pre-layout and post-layout simulation as well as their graphical comparison are presented. The designed PLL can be used as a high speed clock generator, frequency synthesizer, clock recovery circuit etc.

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TABLE II. Post Layout Simulation Data

Parasitic Corner	Process Corner	Temperature (C)	Voltage (V)	Frequency	Lock Time	Average Current	Leakage Current
Nominal	TT	25	1	1.62G	951n	878u	485u
FuncCmin	FF	125	1.1	1.62G	586n	1.21m	676u
FuncCmax	SS	-40	0.9	1.64G	2.24u	515u	379u

TABLE III. Performance analysis of recent PLL topologies

REF.	[13]	[14]	[15]	[16]	[17]	[18]	**This Work**
Tech. (nm)	28	28	28	180	180	180	28
Year (20 -)	18	18	14	20	17	20	20
Frequency (GHz)	23.3-30.2	5.5-7.3	9.2 - 12.7	0.06 - 1.9	2.4	2.4	1.62
Phase noise (dBc/Hz)	-34.6 @1M	N/A	-138 @2M	-102 @1M	N/A	-125.1 @1M	-62.6 @1M
Settling time	N/A	N/A	2us	N/A	55 ns	1.7 µs	951ns
VDD(V)	1.2	1.8	1.8	1.8	1.8	1.8	1
Power	15.4 mW	18.9 mW	13 mW	17.4 mW	13.3 mW	9.72 mW	837 uW

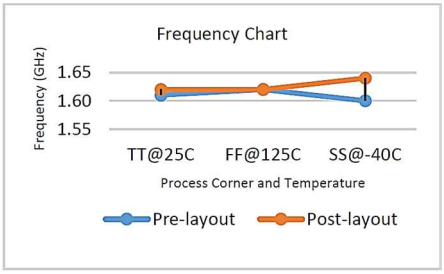

Fig. 8. Frequency plot of Pre-layout vs Post-layout data in different PVT corners

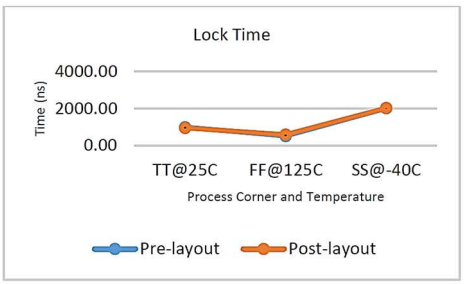

Fig. 9. Lock time plot of Pre-layout vs Post-layout data in different PVT corners

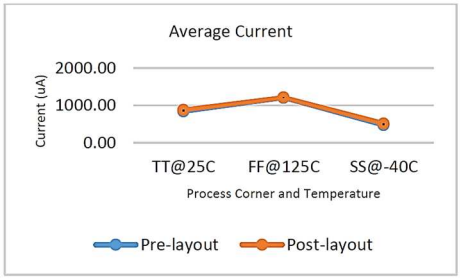

Fig. 10. Average current plot of Pre-layout vs Post-layout data in different PVT corners

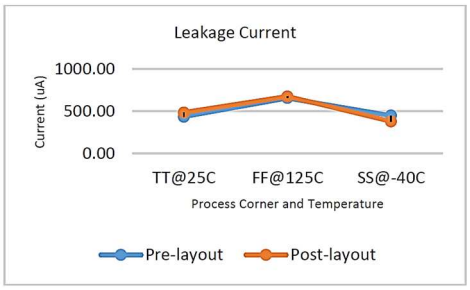

Fig. 11. Leakage current plot of Pre-layout vs Post-layout data in different PVT corners

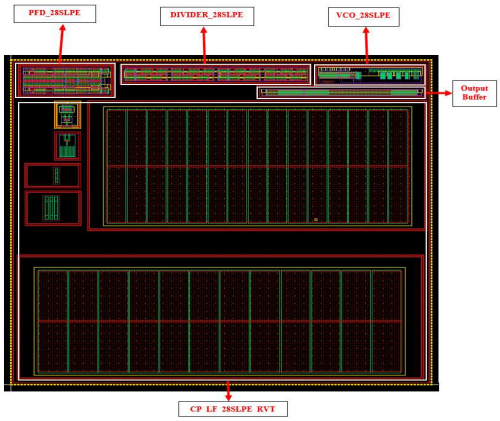

Fig. 12. Layout of the 1.6GHz PLL in 28-nm technology

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