

A 529- μ W Fractional-N All-Digital PLL Using TDC Gain Auto-Calibration and an Inverse-Class-F DCO in 65-nm CMOS

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Abstract—This paper presents an ultra-lower-power (ULP) digital-to-time-converter (DTC)-assisted fractional-N all-digital phase-locked loop (ADPLL) suitable for IoT applications. A proposed hybrid time-to-digital converter (TDC) extends the vernier-TDC input range with little power overhead in order to overcome the stability issue in the conventional architectures. The hybrid TDC also facilitates a background gain calibration to achieve a stable in-band phase noise insensitive to process, voltage, and temperature (PVT) variations. The implementation of a buffer-cascaded DTC simplifies the design complexity of the fractional-N operation. The ADPLL also features a 200 μ W low-phase-noise inverse-class-F (class-F⁻¹) digitally controlled oscillator (DCO) without the need of two-dimensional (2-D) capacitor tuning for frequency alignment of the fundamental and 2nd-harmonic. Fabricated in 65-nm CMOS, the ULP ADPLL prototype achieves 868 fs_{rms} jitter in a fractional-N channel when consuming only 529 μ W, corresponding to a figure-of-merit (FoM) of -244 dB.

Index Terms—ADPLL, Bluetooth LE (BLE), DCO, fractional-N PLL, phase noise (PN), TDC, DTC, inverse-class-F, low power, the IoT.

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I. INTRODUCTION

RECENT years have witnessed the rapid development of internet-of-things (IoT) underpinned by ultra-low power (ULP) short-range radios that can secure long battery life or can be directly powered by energy-harvesting sources. Bluetooth low energy (BLE) is currently the most popular IoT standard. A frequency synthesizer is one of the most power-hungry blocks in a typical BLE radio since it needs to be active both during the data reception and transmission [1]–[3]. Consequently, it is critical to minimize its power consumption while ensuring its stability and maintaining good phase noise (PN) with low spurious emissions.

Recent works in [4]–[16] have successfully demonstrated the advantages of fractional-N ADPLLs over their analog counterparts in reducing the power consumption while maintaining a competitive performance. By employing a digital-to-time converter (DTC)-assisted architecture proposed in [4] in order to narrow the phase error between the reference and the DCO output clocks, the input range of the following time-to-digital converter (TDC) can be substantially reduced, thus drastically improving the latter's power consumption and linearity. Since the DTC needs to generate a wide delay range covering the full oscillator period and to maintain good linearity to minimize fractional spurs, a relatively sizable power consumption is still typically required. Diverse techniques have been proposed to reduce the power and DTC nonlinearity in recent publications [17]–[20]. As a baseline, the DTC-TDC-based ADPLL in [4] achieved a worst-case fractional spur of -37 dBc and rms jitter of 1.71 ps while consuming 860 μ W. Reference [5] proposed a phase dithering technique to scramble the DTC's integral nonlinearity (INL) and an extra reset operation inside the DTC to suppress the DTC memory effect. As a result, the worst-case fractional spur was reduced to -56 dBc with an rms jitter of 1.98 ps, while burning 670 μ W. To further improve the INL of the DTC, a DAC-based constant-slope DTC architecture can be considered [6], [17], [21], [22]. In [6], the ADPLL using an isolated DAC-based constant-slope DTC with sub-1 ps INL achieves a worst-case fractional spur of -56 dBc and rms jitter of 0.53 ps, while consuming 980 μ W, resulting in an excellent FoM of -246 dB. However, the DTC consumes a relatively large power of 142 μ W, limited by its architecture. It also needs an additional bias pin for the current mirror.

On the DCO side, its PN is expected to deteriorate severely as its drawn power is reduced, thereby limiting the jitter performance of the ADPLL. A 2.4GHz complementary class-B DCO in [6] achieves PN of -110dBc/Hz at 1MHz offset when consuming $210\mu\text{W}$, corresponding to a rather inferior FoM of 185dB. Compared with the state-of-the-art LC VCOs that can achieve a high FoM of up to 197dB [23]–[29], there is still plenty of room to improve the DCO PN at low power consumption. Furthermore, even though the oscillators using waveform-shaping techniques [24]–[28] can achieve high FoMs by exploiting the multiple-resonance properties provided by high-order LC tanks which rely on a precise alignment between the tank resonance frequencies and the harmonics of the fundamental resonance. In case of misalignment between the tank resonance frequencies, the optimal PN and FoM performance cannot be maintained. Thus, the existing oscillators using waveform-shaping techniques require independent tuning of multiple capacitor banks to guarantee the alignment between the resonance frequencies, which makes their performance sensitive to the PVT variations when integrated into a PLL.

The diagram illustrates a PLL system with a Variable Step TDC. The input REF is processed by a DTC block to produce FREFdly. This signal is then delayed by an Offset delay block to produce FREFdly2. FREFdly2 is fed into the Variable Step TDC block, which outputs CKVG. CKVG is multiplied by K_{TDC} and then by the output of a counter (which is also fed by FREFdly2) to produce a signal that is added to the output of a loop filter (1/(1-z⁻¹)). The loop filter also receives a feedback signal from the output of a phase-to-frequency converter (α) and a loop delay (z⁻¹). The output of the loop filter is multiplied by K_{OTC} and then by the output of a phase-to-frequency converter (α) to produce the final output signal. A red circle highlights the output signal, and a red box highlights the Variable Step TDC block.

Figure 1 shows the top-level block diagram of the implemented ADPLL. The red blocks highlight the novel contributions of this work. Generally, the phase detection part consists of an integer path and a fractional path. The former is made up of a *reset-free* counter. The integer path is also (rather imprecisely) referred to as frequency locked-loop (FLL) in some publications, and it can be shut down after the frequency gets locked in order to stop unnecessarily burning power. For the fractional-N phase locking, the output from the combined DTC and TDC is used. With the help of phase prediction [30], a delayed version of the reference signal, i.e., FRE_{dly} is generated and its rising edge is aligned with the rising edge of the DCO output, CKV.

Various oscillators for BLE PLLs appear in the recent works [4]–[6], [31], [32]. Generally, jitter optimization can be achieved through minimizing the reference path noise *and/or* oscillator noise. This work chooses the latter option. Figure 2(a) plots the PN profile by applying various oscillators with different noise performance in the same ADPLL architecture of Fig. 1. To simplify the analysis, flicker noise upconversion in the oscillator, oscillator’s quantization noise and flicker noise in the DTC are all ignored. The DTC’s thermal noise floor is -155 dBc/Hz clocked at 32 MHz. The TDC with resolution of 7 ps is adopted for the model. By selecting the optimal bandwidth for the lowest jitter in each case, the total integrated rms jitter versus the oscillator performance is plotted in Fig. 2(b). It can be concluded that when the in-band PN is kept constant at around -103 dBc/Hz, by reducing the oscillator PN from -106 dBc/Hz to -118 dBc/Hz at 1 MHz offset, the integrated rms jitter can drop from 1.7 ps to 0.6 ps.

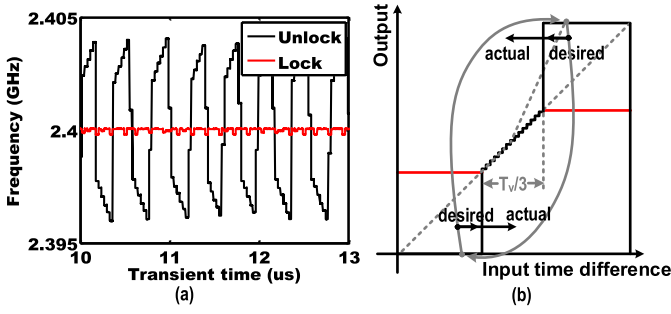


Fig. 3. Potential loop stability issue in face of a TDC out-of-range gain increase (black curves) when a wide loop bandwidth is employed: (a) PLL output frequency over time; (b) transfer function of TDC.

The rest of the paper is organized as follows. Section II introduces the hybrid TDC architecture and its calibration. The DTC with snapshot circuitry is described in Section III. Section IV presents the class- F^{-1} DCO free of the 2nd-harmonic tuning. Experimental results are given in Section V.

II. HYBRID TDC

A. Stability Issue With Narrow-Range TDC

A design trade-off exists between the TDC range and settling time in the DTC-assisted ADPLL architecture. References. [5], [31] proposed enlarging the absolute values of TDC output when the input time difference is beyond the TDC detection range. That helps speeding up the settling behavior because the loop gain is also enlarged when the TDC input is out-of-range. However, that approach can exhibit an issue of loop stability when a wider loop bandwidth is employed. As Fig.3(a) shows, when the normal loop bandwidth is comparable to the maximum allowable bandwidth of the PLL ($\sim 1/10$ of reference frequency, [33]), enlarging the TDC output codes when out-of-range will reduce the loop phase margin, which can result in the PLL going out of lock. This can happen even when the FLL is always on, and it is independent of the TDC architecture.

To demonstrate this scenario, we examine the example below. Firstly, when optimizing the loop stability, the TDC transfer function should be centered in the middle of the phase detection window with the help of a tunable offset delay, as shown in Fig.3(b). In this example, the TDC detection range covers $1/3$ of the DCO period, T_V . The initial input time difference is assumed as $(1/6 + \delta)T_V$ where δ is a vanishingly small value. Then, the ideal TDC output corresponds to a time difference of $T_V/6$ as the red transfer function illustrates. However, with the transfer function of the enlarged out-of-range gain, as the black curve shows in Fig.3(b), the TDC output corresponds to a time difference of $T_V/2$ which is $3\times$ larger than the desired value. The desired feedback force ‘gently’ drives the phase difference towards zero while the actual force is three times of the desired value in this example. The phase difference is over-pushed to the opposite direction, making the loop difficult to settle. From another perspective, the instant loop bandwidth is three times larger, resulting in an over-correction of the DCO frequency and the phase error. Therefore, the phase detection can manifest a bang-bang

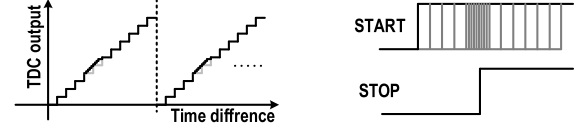


Fig. 4. Proposed idea of the TDC transfer function.

behavior, making it harder for the phase error to fall into the linear TDC detection range.

The behavioral model simulation confirms that the PLL cannot lock in this scenario of enlarging the TDC output code as per the black line indicated in Fig.3(a), in which the bandwidth equals half of the maximum value. Otherwise, the PLL can still lock (red curve) although a long settling time is needed. It can be inferred that when the phase difference is out of the TDC range, it is better to add some coarse quantization steps to ease the trade-off between the settling time and stability.

It is noted that the trajectories in Fig.3(a) are only for illustration purposes of Fig.3(b). The actual phase error trajectory will be much more complex than just bouncing between the two levels. Increasing the TDC out-of-range gain is still helpful to overcome cycle slipping when small frequency disturbance occurs in the case of narrow loop bandwidth.

B. Proposed Hybrid TDC

To alleviate the above issue, the quantized phase error fed into the digital loop filter should be close to the actual phase error [34]. For the DTC-assisted ADPLL architecture, most of the delay stages in the TDC are not used when the loop is eventually locked [4]. Therefore, considering that the coarse quantization steps added beyond the fine TDC range are only utilized during the settling process, the coarse TDC’s linearity and resolution requirements can be greatly relaxed. Figure 4 illustrates the concept of the TDC transfer function in this hybrid architecture. Coarse quantization steps extend the measurement range of the fine TDC. The wrapped phase generated by the snapshot circuit replicates the TDC transfer function along the x-axis at an interval of one oscillator period.

Figure 5(a) illustrates the schematic of the proposed hybrid TDC that embeds the above-mentioned coarse quantization function into a vernier TDC. The coarse quantization is realized by the flash TDC, which reuses the ‘slow’ path of the vernier TDC to save area and power. Specifically, during the TDC quantization, the first four delay stages in the slow path are re-used as an offset delay for the START signal. The vernier TDC highlighted in yellow contains eight unit stages, forming the fine 3-bit TDC quantization part. Regarding the coarse quantization, the flash TDC highlighted in gray is made up of twelve $(4+8)$ slow stages and flip-flops. The last eight slow delay stages are shared with the vernier TDC. Therefore, the twelve thermometer codes from the flash TDC flip-flops represent the coarse quantization information. By adopting such an arrangement, the fine steps generated by the vernier TDC can be placed around the middle of the phase detection window, while the coarse steps generated by the flash TDC extend on both of its sides.

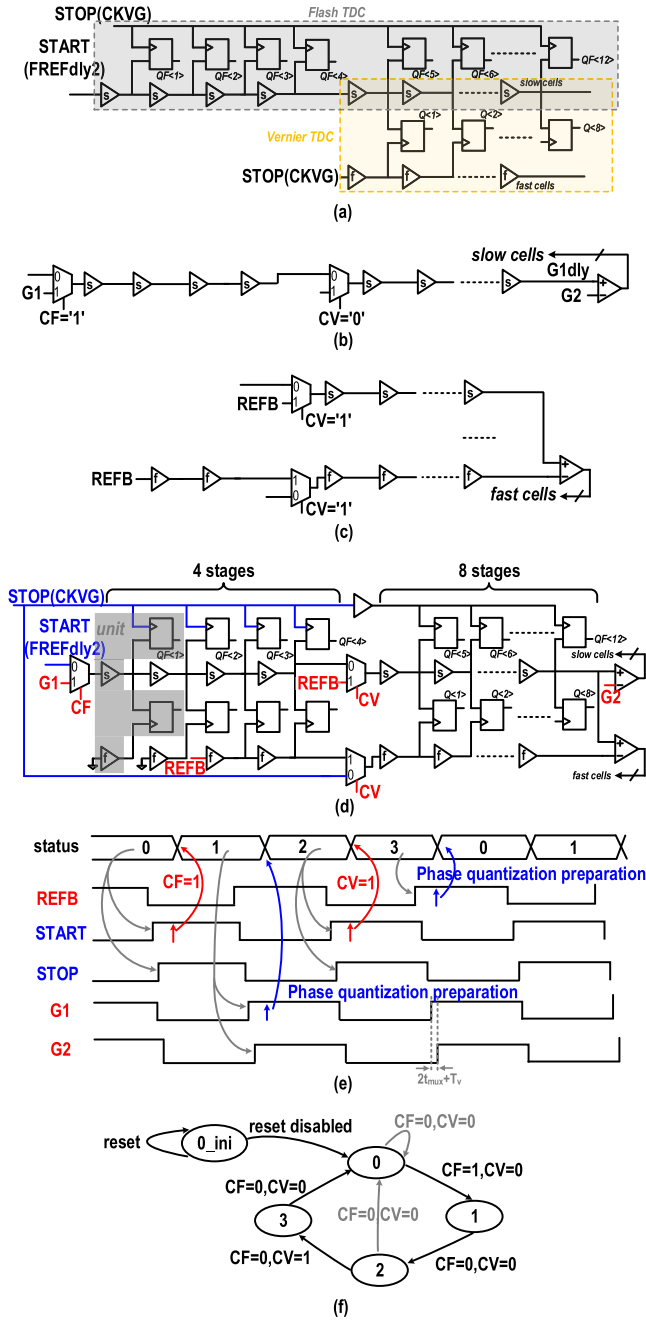


Fig. 5. Hybrid TDC: (a) effective cells in the TDC quantization mode, (b) effective cells in the flash TDC calibration mode, (c) effective cells in the vernier TDC calibration mode, (d) entire TDC schematic, (e) state transition of background TDC gain calibration, and (f) its state diagram.

C. TDC Gain Calibration

It is well known that the DTC gain K_{DTC} can be calibrated with the help of an LMS algorithm by correlating the detected phase error with the accumulated fractional value of the frequency control word PHR_F [4], [5], [35]. However, the calibration of the TDC gain K_{TDC} is difficult to perform by utilizing the current phase error information. When the ADPLL is locked, the integer phase error path always outputs zero and so the TDC gain parameter can be merged with the digital loop filter coefficients. Thus, the loop bandwidth can be affected by an error in the TDC gain. Alternatively, the TDC

gain can be used to control the loop bandwidth [5]. In the applications where the bandwidth needs a precise control, the TDC gain should be calibrated. This would also benefit a fixed in-band noise floor if the in-band noise is determined by the TDC quantization error.

This architecture also facilitates the gain calibration of the vernier TDC. The target of the calibration is to match the total delay of the twelve slow stages with one oscillator period T_v ; for simplicity, it is termed here a flash TDC calibration. Furthermore, the eight ‘slow’ stages and ten ‘fast’ (i.e. fine resolution) stages are expected to have the same delay, which is termed a vernier TDC calibration. The relationships can be expressed as follows:

$$\begin{aligned} 12\Delta_s &= T_v, \quad 8\Delta_s = 10\Delta_f \\ \Delta_{res} &= \Delta_s - \Delta_f = \frac{1}{60}T_v \end{aligned} \quad (1)$$

where Δ_s and Δ_f denote the unit delay of slow and fast stages. Δ_{res} denotes the vernier TDC resolution. After the calibration, it is fixed to $\frac{1}{60}T_v$. To make the unit delay tunable, both slow (coarse) and fast (fine) stages are controlled by 6-bit variable loading capacitances. As Fig.5(b) shows, in the flash TDC calibration mode, G1 rising edge is preset to lead G2 by $T_v + 2t_{mux}$, where t_{mux} denotes the transition time through MUX. Consequently, G1_{dly} rising edge and G2 rising edge are expected to be aligned, generating an averaged value of zero from the comparator output if the comparator outputs are coded as ‘+1’ and ‘−1’. Such averaged digital codes are intended to control the load capacitance of the slow stage. In the preset condition, the averaged zero comparator output will leave the loading of the slow stages untouched since (1) is satisfied. When the unit delay of the slow stage changes with PVT, the averaged comparator output can track this out and tune the loading of slow stages in an opposite direction. The vernier TDC calibration shown in Fig.5(c) works using a similar principle. The two TDC calibration loops of flash and vernier TDC are intrinsically delay-locked loops (DLL).

The TDC phase detection mode works alternately with the gain calibration mode. Schematic of the entire TDC is shown in Fig.5(d). In the phase detection mode, control signal CV for the vernier TDC calibration mode is disabled allowing START and STOP to propagate through the last eight stages and produce eight thermometer outputs. As for the coarse quantization, control signal CF for the flash TDC calibration is also disabled, allowing START signal to propagate through the first four stages.

This background calibration is carried out at the falling edge of the reference signal, reserving its rising edge for the conventional phase detection. The two calibration modes also work alternately. A finite state machine is adopted for the working mode shift, as shown by the timing diagram in Fig.5(e) and the state diagram in Fig.5(f).

In state 0 and 2, the TDC works in the phase detection mode. After START signal rising edge passes all the slow delay units, it triggers the state switching, yielding $CV = 1$ or $CF = 1$. The phase detection information is not affected by the state switching since the TDC output thermometer codes would have already been stored in the flip-flops. In state 1,

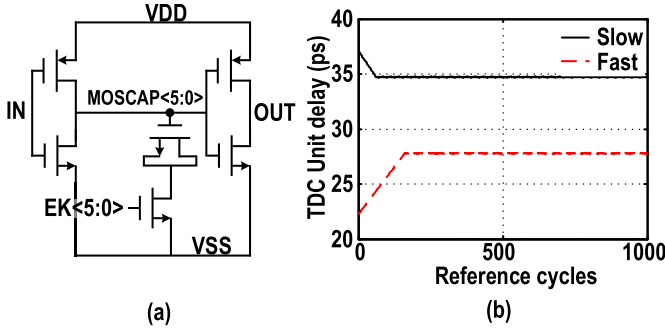


Fig. 6. (a) TDC slow/fast unit cell schematic, (b) TDC calibration settling behavior.

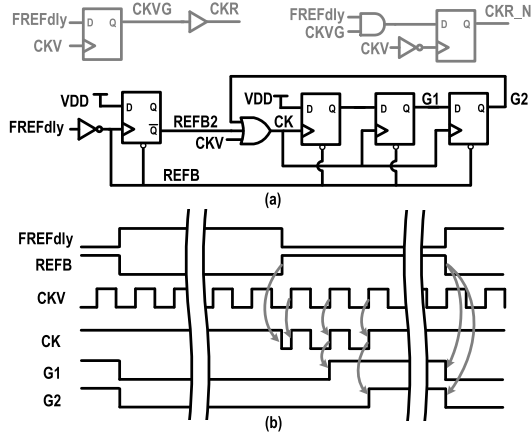


Fig. 7. Signal generation for TDC calibration in the snapshot.

the flash TDC calibration mode is enabled, yielding $CV = 0$ and $CF = 1$. After G1 propagates to the output of the last slow stage, state 2 is triggered entering the normal TDC phase detection state.

Similarly, in state 3, vernier TDC calibration is achieved. After state 3, the TDC working state enters 0, starting another round of phase detection and calibration. It can be seen that since the calibrations work at the falling edges of START and STOP, the phase error information is still updated every reference cycle.

The schematic of the TDC fast and slow unit cells is shown in Fig. 6(a). Assuming the slow and fast delays suffer from random variations, its calibration settling behavior is plotted in Fig. 6(b).

The TDC gain calibration signals (G1 and G2) are generated by the circuit shown in Fig. 7(a). The rising edge difference between G1 and G2 is one DCO period. Before sending them to the TDC, G2 is delayed by extra two dummy muxes (not shown). Both G1 and G2's falling edges are reset by REFB's falling edge in preparation for the next cycle calibration. CK drives three flip-flops rather than two. Its waveform has three rising edges every reference period. The motivation is that when the PLL is in lock, the first rising edge could be in a meta-stable condition, deteriorating the timing information. The outputs from the second and third flip-flops are more stable, constraining the flash TDC range steadily. Since the high-frequency clock CKV only feeds into the 3OR gate, G1 and G2 generation circuit consumes limited power.

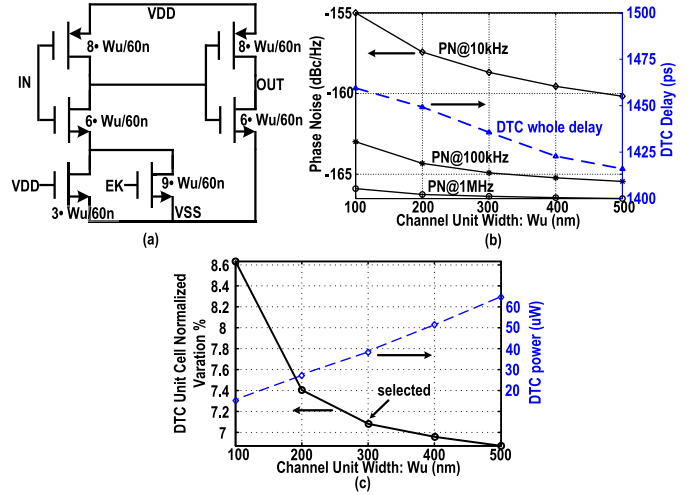


Fig. 8. (a) Schematic of the DTC unit cell. (b) Simulated overall PN and delay for different unit width W_u of transistors. (c) Simulated Monte-Carlo mismatch of the DTC unit cell across W_u .

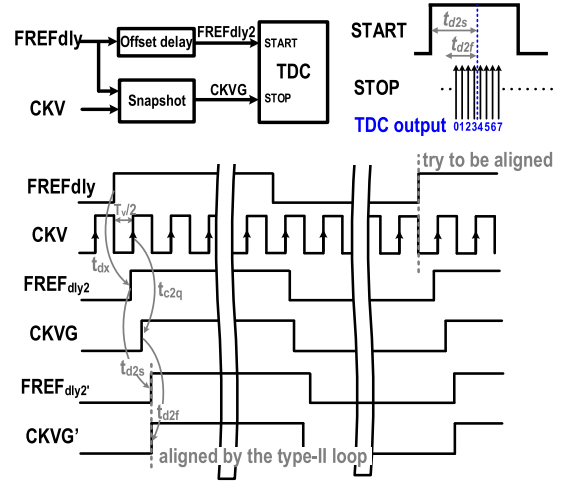


Fig. 9. Snapshot phase alignment.

III. DTC AND SNAPSHOT CIRCUIT

A buffer-cascaded DTC is a conventional way to realize the controllable delay. We have demonstrated that a $\Delta\Sigma$ dithering approach in generating digital control codes for the DTC can effectively suppress the DTC quantization induced spurs [35]. However, this would not substantially help suppressing the spurs caused by the DTC nonlinearity. The nonlinearity of the buffer-based DTC mainly comes from the device mismatches. Larger sizes are adopted to reduce the statistical mismatch. A $4\times$ power consumption can be traded for reducing the mismatch by only $2\times$. The spur performance can be roughly improved by 6 dB.

Figure 8(a) shows the schematic of the DTC unit cell. Binary-valued EK signal is used to control the DTC unit delay by varying the discharging resistance in the first inverter. Figure 8(b) shows the PN and delay of the whole DTC chain across different W_u unit width values. Figure 8(c) plots the simulated Monte-Carlo mismatch. The overall DTC delay does not change dramatically when changing the transistor channel widths. The noise and process mismatch performance

inclines to be stable when the channel unit width is >300 nm. To balance the power consumption versus mismatch, a channel unit width of 300 nm is ultimately chosen.

The DCO output CKV is clock-gated at the reference rate before being fed into the TDC in order to save power by avoiding redundant transitions. The clock gated output must obviously retain the DCO rising edge information for phase detection. This is implemented by sampling the delayed reference signal FREF_{dly} with CKV in the snapshot block, as shown in Fig. 9. The sampling delay from CKV to CKVG, which is made up of a typical flip-flop clock-to-Q delay and the delay from several buffers connecting the snapshot block and TDC, is denoted as t_{c2q} . The sampled output (CKVG) is always behind FREF_{dly} . Therefore, we cannot directly feed FREF_{dly} into the TDC due to the fact that the TDC inputs are expected to have, on average, zero time difference when the PLL is locked in a type-II mode. An offset delay block is used to provide this extra delay, retarding FREF_{dly} to $\text{FREF}_{\text{dly}2}$ by t_{dx} . In [36], the above extra delay was also implemented by a DTC. However, most DTCs suffer from a constant offset delay which is usually at the same level as the DTC tuning range. Part of the constant offset also needs to be compensated in the CKVG path by inserting extra buffers. Those operations bring in unnecessary noise and power consumption before the critical signals are quantized by the TDC. Consequently, we desire the shortest offset delay, which can be roughly compensated without degrading the loop stability [37]. To overcome the PVT variations, but also for test purposes, a coarse tunable offset delay is adopted in this work. It features a large tuning range with a small constant offset but very coarse resolution.

The offset value calculation is illustrated in Fig. 9. CKVG and $\text{FREF}_{\text{dly}2}$ are the two inputs to the TDC. A 3-bit vernier TDC in this work is taken as an example. When the PLL is locked in type-II, the stop signal (CKVG) will catch the start signal's ($\text{FREF}_{\text{dly}2}$) rising edge at the 4th/5th unit stage, producing a decoded TDC output of 3 or 4. Inside the vernier TDC, CKVG goes through the fast delay cells and is delayed by t_{d2f} as CKVG' to reach the 4th/5th unit stage. $\text{FREF}_{\text{dly}2}$ goes through the slow delay cells and is delayed by t_{d2s} as $\text{FREF}_{\text{dly}2'}$ to reach the 4th/5th unit stage. CKVG' and $\text{FREF}_{\text{dly}2'}$ are forced aligned by the loop. t_{dx} denotes the offset delay to be calculated. It is desired that the TDC transfer function falls right in the middle of its detection window, as shown in Fig. 3(b). It corresponds to the scenario in which the CKV falling edge is aligned with the FREF_{dly} rising edge. This way, the CKV clock gating can stay far away from the metastability condition. In this case, the offset delay is expressed as

$$t_{dx} = T_o/2 + t_{c2q} + t_{d2f} - t_{d2s} \quad (2)$$

Based on post-layout simulations, it is 180 ps. The offset delay is made up of three different delay lines with MUX to select the appropriate one. The whole delay for the three paths is 110 ps, 180 ps and 270 ps, respectively.

IV. DIGITALLY CONTROLLED OSCILLATOR

The class-F⁻¹ oscillator in [26] maps the low (ω_L) and high (ω_H) resonant frequencies of the transformer tank to the

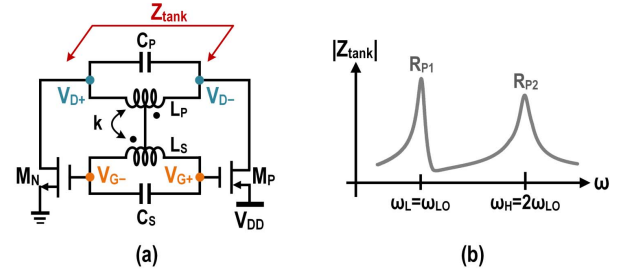


Fig. 10. Class-F⁻¹ oscillator: (a) simplified schematic, and (b) amplitude of the tank impedance.

fundamental (ω_{LO}) and 2nd-harmonic ($2\omega_{LO}$) frequencies of the oscillator, as illustrated in Fig. 10, which can effectively suppress the noise contribution from the negative g_m transistors. According to [24], [38], [39], [45], ω_L and ω_H can be expressed as

$$\begin{aligned} \omega_{L,H}^2 &= \frac{1 + \xi \mp \sqrt{(1 + \xi)^2 - 4\xi(1 - k^2)}}{2(1 - k^2)} \cdot \omega_2^2 \\ &= \Omega_{L,H}^2(\xi, k) \cdot \omega_2^2 \end{aligned} \quad (3)$$

where k is the coupling coefficient, $\xi = L_S C_S / L_P C_P$ and $\omega_2 = 1/\sqrt{L_S C_S}$. To guarantee $\omega_H/\omega_L = 2$, the transformer tank needs to satisfy [26]:

$$16\xi^2 + (100k^2 - 68)\xi + 16 = 0 \quad (4)$$

Under the constrain of (4), the $\Omega_{H,L}$ in (3) can be simplified as,

$$\Omega_H = 2\Omega_L = \sqrt{\frac{5\xi}{1 + \xi}} \quad (5)$$

Ref. [26] demonstrates that the high-Q impedance peaks at ω_{LO} and $2\omega_{LO}$ can be obtained by choosing a small k of 0.38 and a large ξ of 3, which enlarges 2nd-harmonic voltage and extends the flat span where the impulse sensitivity function (ISF) is minimum. Together with a high voltage gain from V_D to V_G provided by the transformer [Fig. 10(a)], the noise contributions from the negative g_m transistors are effectively suppressed. However, the PN and FoM of the class-F⁻¹ oscillator heavily rely on the accurate alignment between ω_H and $2\omega_{LO}$. In [26], since a loosely coupled transformer with $k = 0.38$ and $\xi = 3$ is employed, ω_L mainly depends on C_S , while ω_H mainly depends on C_P . Thus, when the oscillation frequency ω_{LO} is tuned by varying C_S , ω_H stays mostly unmoved and deviates from the 2nd-harmonic frequency ($2\omega_{LO}$) of the oscillator. To align ω_H with $2\omega_{LO}$, C_P also needs to be appropriately changed. When implemented in a PLL, this 2-D capacitor tuning scheme is difficult to realize automatically. On the other hand, if we pre-design the C_S/C_P ratio through simulations for different frequencies, the performance of the class-F⁻¹ oscillator will be sensitive to the process variation of the capacitors. According to Monte Carlo simulations, the 3σ capacitance variation of a 100-fF metal-oxide-metal (MOM) capacitor is $\pm 15\%$ in this 65 nm CMOS technology, which can cause a ξ variation from -26% to $+35\%$. As illustrated by the simulation results in [26], if the C_S/C_P ratio deviates from the optimal value by 20%, the FoM

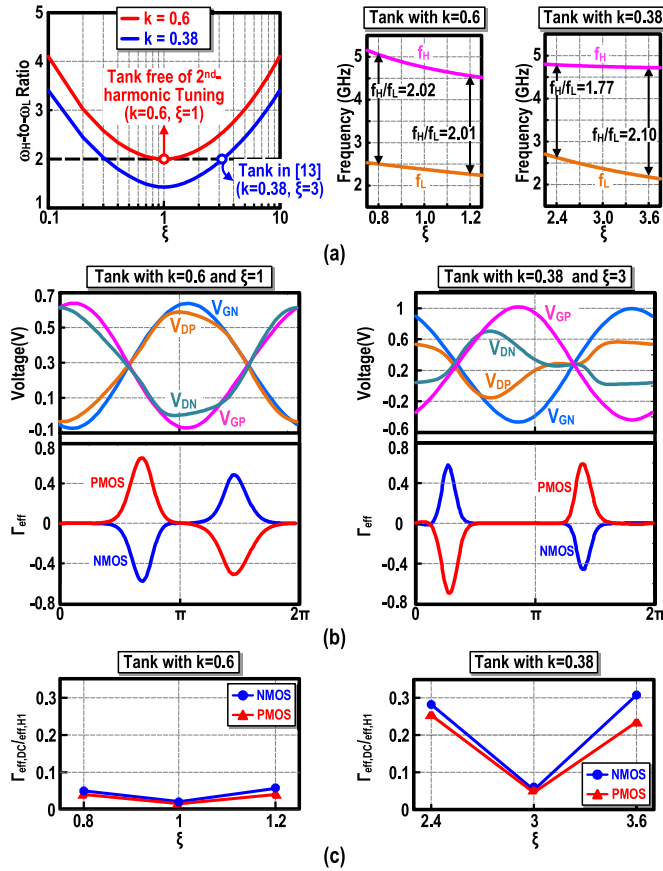


Fig. 11. (a) Relationship between ω_H/ω_L and ξ at different k . (b) Simulated voltage waveforms, effective ISFs of the NMOS and PMOS transistors. (c) $\Gamma_{eff,DC}/\Gamma_{eff,H1}$ for the class- F^{-1} oscillators using transformer tanks with $k = 0.6$ and 0.38 .

at 100kHz and 10MHz will suffer from a considerable degradation of 6.7 and 3dB, respectively, which is mainly caused by a large variation of the ω_H/ω_L ratio.

To avoid this troublesome 2-D capacitor tuning, it is preferred that both ω_L and ω_H can be simultaneously tuned when only C_S (or C_P) is changed. Intuitively, to make both ω_L and ω_H strongly dependent on C_S (or C_P), a tightly coupled transformer with a maximized k should be employed. Furthermore, if both ω_L and ω_H strongly depend on C_S , they must also strongly depend on C_P since the magnetic coupling between the primary and secondary coils is bidirectional, which implies choosing ξ close to 1. These assertions are also supported by theoretical analysis. Among all solutions of (4), the maximum k is 0.6, and the corresponding ξ is 1. As depicted in Fig. 11(a), when choosing $k = 0.38$ and $\xi = 3$, ω_H/ω_L will deviate from 2 by +5/-7% if ξ or C_S/C_P experiences a $\pm 20\%$ variation. To make ω_H/ω_L insensitive to the ξ variation, we can consider to use the transformer with $k = 0.6$ and $\xi = 1$. In this case, ω_H/ω_L only changes by +1% when ξ experiences the same $\pm 20\%$ variation. This insight inspires the development of a transformer tank emancipated from the 2nd-harmonic tuning that can desensitize the PN and FoM from the capacitor mismatch.

Fig. 11(b) compares the simulated voltage waveforms and effective ISFs for the class- F^{-1} oscillators using transformers with $k = 0.6$ and $k = 0.38$. Here, the effective ISF is

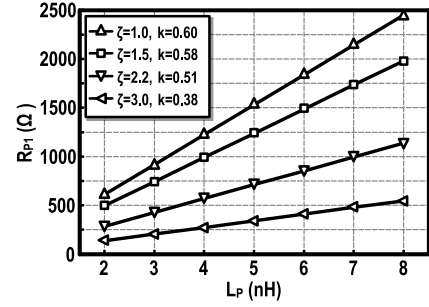


Fig. 12. Relationship between R_{P1} and L_P at different k and ξ ($Q_P = Q_S = 14$ and $\omega_{LO} = 2\pi \times 2.4$ GHz).

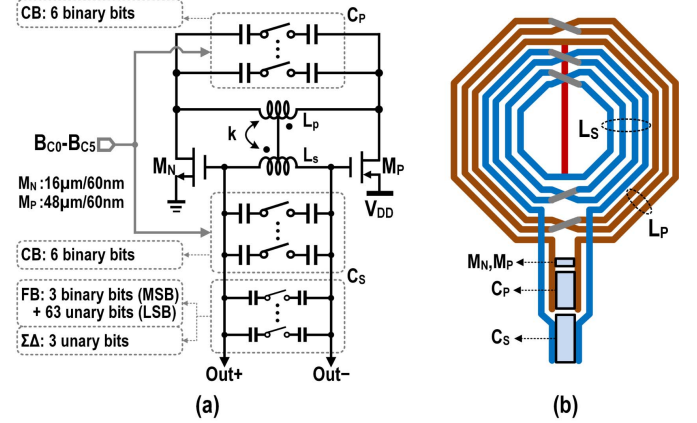


Fig. 13. Detailed schematic (a) and transformer layout (b) of the proposed ULP class- F^{-1} DCO.

defined as $\Gamma_{eff}(\omega_0 t) = \Gamma_{MOS}(\omega_0 t) \cdot g_m(\omega_0 t)/g_{m,max}$, where $\Gamma_{MOS}(\omega_0 t)$ and g_m represent the ISF and transconductance of the MOS transistor, respectively. According to [40], the ratio between the $1/f^3$ PN corner and transistor flicker noise corner is proportional to $(\Gamma_{eff,DC}/\Gamma_{eff,H1})^2$ where $\Gamma_{eff,DC}$ and $\Gamma_{eff,H1}$ are the dc and first harmonic amplitude of Γ_{eff} . Thus, the flicker noise upconversion can be effectively suppressed if $\Gamma_{eff,DC}$ is close to zero. Fig. 11(b) indicates that the Γ_{eff} waveform is symmetric and so $\Gamma_{eff,DC}$ is small for the class- F^{-1} oscillators using both tanks when $\omega_H/\omega_L = 2$. This consequently verifies that the 2nd-harmonic resonance helps to suppress the flicker noise upconversion, resulting in a low $1/f^3$ PN corner. Fig. 11(c) plots the calculated $\Gamma_{eff,DC}/\Gamma_{eff,H1}$ of the NMOS and PMOS transistors versus ξ . When ξ deviates from the optimal values by $\pm 20\%$, $\Gamma_{eff,DC}/\Gamma_{eff,H1}$ soars to 0.31 when using the tank with $k = 0.3$, while it is still suppressed to lower than 0.06 when $k = 0.6$. Therefore, the ISF analysis confirms that the $1/f^3$ PN corner is insensitive to ξ variation when using the tank with $k = 0.6$.

To secure a low power consumption, the tank's parallel impedance R_{P1} at ω_{LO} needs to be maximized. Under the constrain of (4), R_{P1} can be obtained as

$$R_{P1} = \frac{16\omega_{LO}L_PQ_P}{25} \cdot \frac{(1+\xi)^2 \cdot (4-\xi)}{4\xi^2(\frac{Q_P}{Q_S}) - \xi(1+\frac{Q_P}{Q_S}) + 4} \quad (6)$$

At a certain oscillation frequency ω_{LO} , R_{P1} only depends on L_P , ξ , Q_P , and Q_P/Q_S . Assuming $Q_P = Q_S = 14$

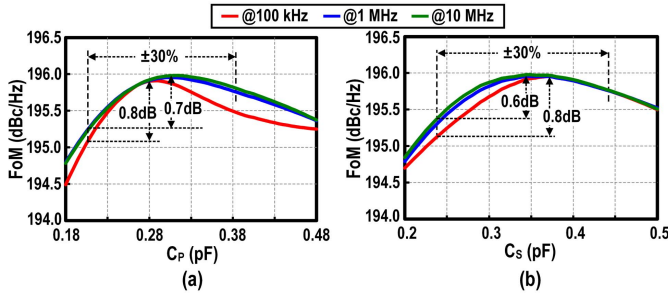
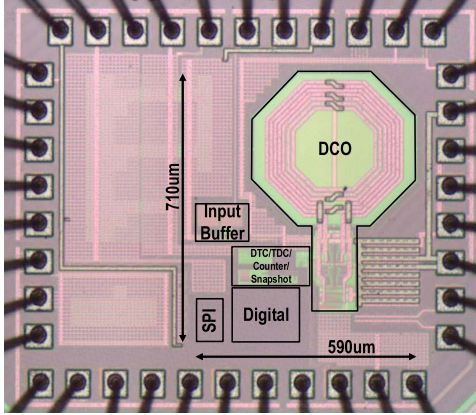
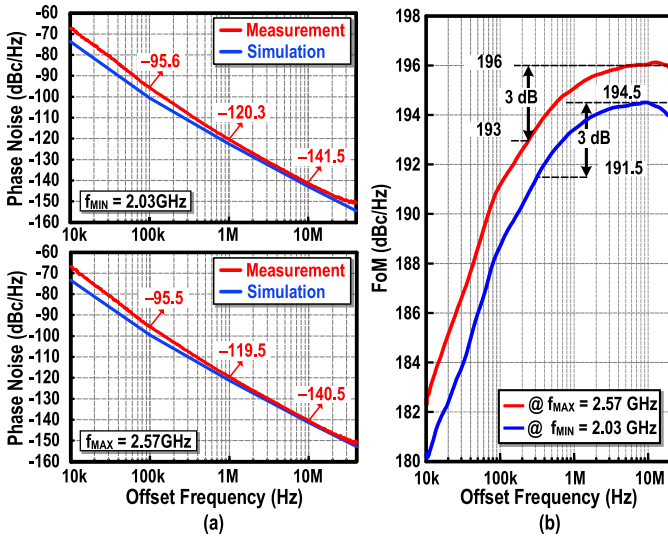
Fig. 14. Simulated FoMs against capacitor variations of (a) C_p and (b) C_s .

Fig. 15. Chip microphotograph of the proposed ULP ADPLL.

Fig. 16. (a) Simulated and measured PN profiles, and (b) measured $1/f^3$ PN corners of the DCO at $f_{\text{MIN}} = 2.03$ GHz and $f_{\text{MAX}} = 2.57$ GHz.

for simplicity, Fig.12 shows that choosing a large L_P and a small ξ helps to enlarge R_{P1} . Thus, our transformer tank employing a minimum ξ of 1 not only desensitizes ω_H/ω_L from the capacitor mismatch but also secures the lowest power consumption.

Furthermore, for the resonance at ω_{LO} , the quality factor Q_1 of the transformer tank can be larger than Q_P and Q_S since the magnetic flux coupled from L_S increases the magnetic energy stored in the tank. According to [38], the transformer tank

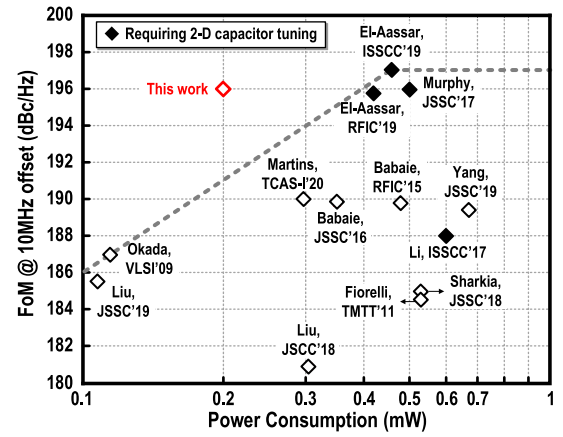


Fig. 17. FoM comparison with state-of-the-art low-power LC oscillators. The oscillator FoM is defined in Table I.

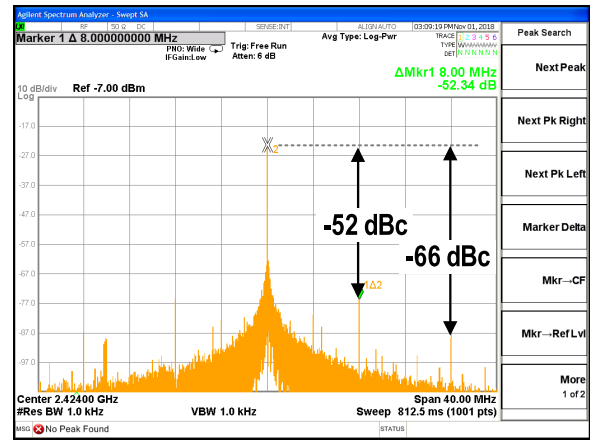


Fig. 18. Measured fractional & reference spurs at one BLE channel.

with large k can benefit from the high Q_1/Q_P ratio. Since our tank uses the peak k of 0.6 to guarantee $\omega_H/\omega_L = 2$, Q_1 is maximized. On the other hand, as pointed out by [26], using the large k and small ξ tends to reduce the tank's quality factor Q_2 at $2\omega_{LO}$ and the voltage gain from V_D to V_G . As a result, the noise contributions from the negative g_m transistors increase, degrading the FoM of the class- F^{-1} oscillator. Fortunately, the enhanced Q_1 mitigates the PN degradation due to the reduced Q_2 and the voltage gain. Therefore, a high peak FoM can still be maintained in the ULP class- F^{-1} oscillator with the natural 2nd-harmonic alignment.

Fig.13(a) depicts the detailed schematic of the proposed class- F^{-1} DCO. Two identical switched-capacitor (SC) banks for coarse frequency tuning (CB) are implemented at both primary and secondary coils and are controlled by the same digital bits ($B_{C0}-B_{C5}$). Since the DCO performance is insensitive to the capacitor mismatch between C_P and C_S , the SC banks for the fine frequency tuning (FB) and $\Sigma\Delta$ modulation are only placed in the secondary coil for a simple and compact layout. We tailor a 3-to-4-turn transformer with $L_P = 7$ nH and $L_S = 8$ nH to maintain high Q-factors for both coils ($Q_P = 14.5$ and $Q_S = 16.6$), as shown in Fig.13(b). This tightly-coupled transformer ($k = 0.6$) also saves the die area compared with the designs in [25] and [26]

TABLE I
PERFORMANCE SUMMARY AND COMPARISON OF THE PROPOSED DCO WITH STATE-OF-THE-ART

		RFIC15 [41] Babaie	JSSC17 [25] Murphy	JSSC19 [32] Liu	ISSCC19 [27] Aassar		RFIC19 [28] Aassar		TCAS-I20 [42] Martins		This Work	
Topology		Switching Current Source	CMOS CM Resonance	Stacked-gm	Folded, 4-Winding xfmr		CMOS 4-Port xfmr Resonator		CMOS Class-B/C Hybrid-Mode		Class-F ⁻¹ + xfmr Tank Free of 2 nd -Harmonic Tuning	
2-D Capacitor Tuning?		No	Yes	No	Yes		Yes		No		No	
Supply (V)		0.5	0.7	0.45	0.1		0.35		0.8		0.55	
Freq. Range (GHz)		4.0-5.03 (22.2%)	4.7-5.4 (13.8%)	2.1-3.1 (38.5%)	4.15-4.97 (18%)		4.06-4.96 (20%)		4.2-5.1 (19%)		2.03-2.57 (23.8%)	
Freq. (GHz)		5.03	5.3	2.46	4.15	4.97	4.06	4.96	4.2	5.1	2.03	2.57
Power (uW)		470	500	107	540	460	440	420	349	297	205	183
PN (dBc/Hz)	100k	-85.1	-92*	NA	-91.3	-92.3	-93.1	-91.6	-84.3	-86.1	-95.6	-95.5
	10M	-132.7*	-138*	-128	-133	-136.5	-136	-137.8	-126.7	-130.6	-141.5	-140.5
FoM** (dBc/Hz)	100k	182.4	189.5	NA	186.4	189.6	189	189.2	181.3	185.4	188.6	191
	10M	190	195.5	185.5	188	193.7	192	192.5	183.7	190.0	194.5	196
1/ <i>f</i> ³ corner (kHz)		250-420	200	NA	50-180		100-250		70	150	300	250
Freq. Pushing (MHz/V)		17	NA	NA	40		80		-12	-91	56	27
CMOS Tech. (nm)		40	28	65	22 FDSOI		22 FDSOI		65		65	
Core Area (mm ²)		0.14	0.18	0.25	0.27		0.19		0.165		0.22	

*Estimated from the PN plot. **FoM = PN - 20 log₁₀($\omega_{LO}/\Delta\omega$) + 10 log₁₀($P_{DC}/1mW$)

TABLE II
PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART ULP ADPLLs

	ISSCC14 [4] Chillara	ISSCC17 [5] He	JSSC18 [6] Liu	JSSC19 [32] Liu	JSSC18 [43] Pourmousavian	This Work
CMOS Process (nm)	40	40	65	65	28	65
Reference (MHz)	32	NA	52	10	40	32
Frequency Range (GHz)	2.1-2.7	1.8-2.5	2.0-2.8	2.1-3.1	2.1-2.6	1.9-2.6
Power (mW)	0.86	0.67	0.98	0.27	1.6	0.53
Jitter (ps)	1.71	1.98	0.53	2.8	0.86	0.87
Integration BW	1k-100M	10k-10M	10k-10M	1k-40M	10k-10M	10k-10M
Frac. Spur (dBc)	-38	-56	-56	-52	-57	-50
Ref. Spur (dBc)	-70*	-62	-72	NA	-78	-66
FoM (dB)	-236	-236	-246	-237	-239	-244
Area (mm ²)	0.20	0.18	0.60**	0.25	0.33	0.42

*Estimated from the author's Master thesis [44].

**Estimated from the chip photo.

that use loosely-coupled transformers ($k < 0.4$). Simulation results in Fig. 14 verify that the class-F⁻¹ oscillator with the natural 2nd-harmonic alignment can maintain a high peak FoM of 196dB. Even when C_P or C_S changes by $\pm 30\%$ from its optimal value, the FoM degradation is < 0.8 dB (< 0.7 dB) at the 100kHz (10MHz) offset frequency.

V. MEASUREMENT RESULTS

The presented ultra-low-power ADPLL was implemented in 65-nm bulk CMOS. The chip photo is shown in Fig. 15. The core area is 0.42mm².

The open-loop performance was measured by Agilent E5052B Signal Source Analyzer. The sizes of the g_m transistors in the DCO are 16 μ m/0.06 μ m (NMOS) and 48 μ m/0.06 μ m (PMOS). The measured PN at 2.03GHz

(f_{MIN}) and 2.57GHz (f_{MAX}) when $V_{DD} = 0.55$ V is shown in Fig. 16. The corresponding FoM at 10MHz offset slightly drops from 196dB (f_{MAX}) to 194.5dB (f_{MIN}) due to the extra tank loss from the SCAs when more switches are turned on. The measured 1/ f^3 PN corners are 250kHz (f_{MAX}) and 300kHz (f_{MIN}). Fig. 16(a) also compares the measured PN with the simulated one. The discrepancy at the low offset frequencies is likely due to the flicker noise of the transistor in the triode region not being accurately modeled. We also measured PN and FoM performance across the frequency tuning range as well as its power consumption and 1/ f^3 PN corner over 5 samples. The chip-to-chip variation of the FoM between the 100kHz to 10MHz offsets is < 1 dB, and the worst-case 1/ f^3 PN corner is < 400 kHz. The frequency pushing is < 4 MHz/V at f_{MIN} and < 44 MHz/V at f_{MAX} when

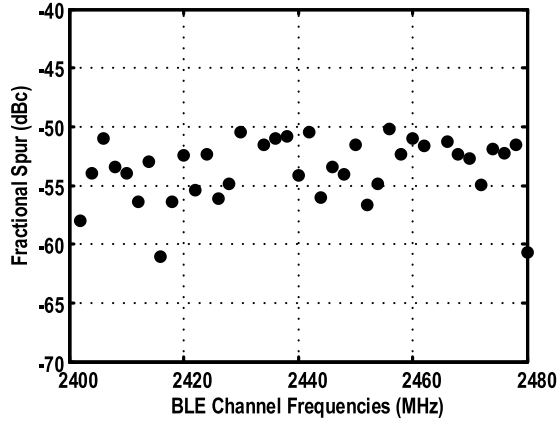


Fig. 19. Measured fractional spurs at BLE channels.

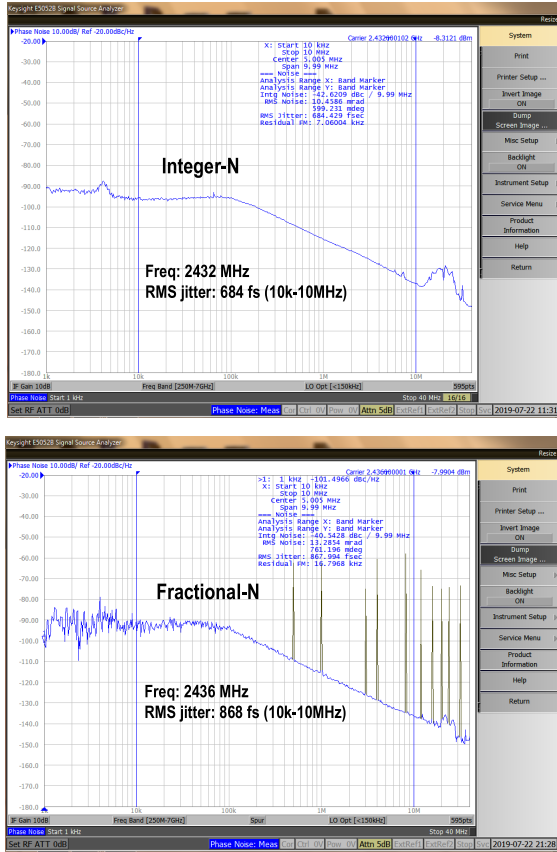


Fig. 20. Measured PN plots at integer & fractional channels.

V_{DD} changes from 0.55 to 0.65 V. This verifies the robustness of the proposed oscillator that is free from the 2nd-harmonic tuning. Benchmarked with other recently reported low-power VCOs and DCOs shown in Fig. 17 and Table I, our class-F⁻¹ DCO retains a high peak FoM of 196 dB with a low power consumption of 200 μ W without the need of the complicated 2-D capacitor tuning.

The closed-loop measurements cover the spectrum and PN. A 32 MHz reference signal is used. The measured reference and fractional spurs at one BLE channel are shown in Fig. 18. Without the power-hungry IIR filters, the spur performance

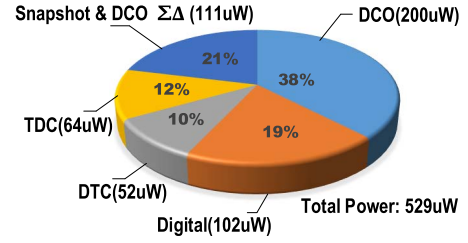


Fig. 21. Measured power breakdown of the proposed ADPLL.

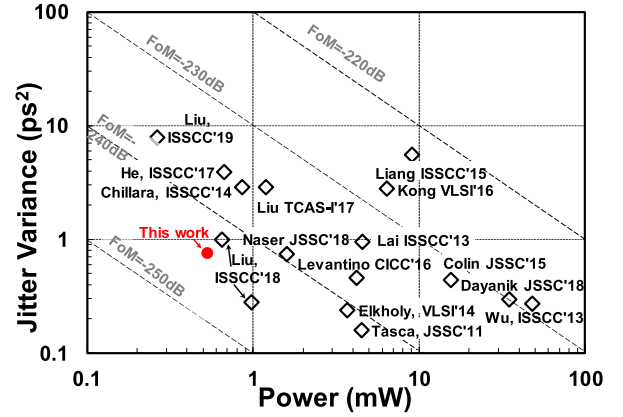


Fig. 22. FoM comparison with state-of-the-art fractional-N ADPLLs.

still satisfies the BLE requirements. Sweeping all BLE channels from 2400 to 2480 MHz, the fractional spur at 2 MHz offset is within -50 dBc, as shown in Fig. 19.

The measured PN¹ of the integer-N and fractional-N channels are plotted in Fig. 20. Integrated from 10 kHz to 10 MHz, the rms jitter in an integer-N mode is 684 fs, corresponding to an FoM of -246 dB. The integrated jitter in a fractional-N mode is 868 fs, corresponding to an FoM of -244 dB. The in-band noise floor is a bit higher than expected, degraded by the reference signal quality and supply noise of the phase detection blocks.

The detailed power consumption of each building block is shown in Fig. 21. The total power consumption is 529 μ W with analog and digital blocks operating at 0.9 V, and the DCO operating at 0.6 V.

The FoM comparison is surveyed in Fig. 22. It indicates a competitive performance of the proposed design among the ultra-low-power ADPLLs.

VI. CONCLUSION

This work demonstrated a sub-mW DTC-assisted ADPLL featuring an ultra-lower-power fractional-N operation for BLE applications. The proposed hybrid architecture of flash- and vernier- TDC extends the input range of the vernier-TDC with little power overhead. The function-reuse TDC also facilitates the background gain calibration scheme to obtain a stable bandwidth insensitive to the PVT variations. The ADPLL

¹The noise peaking around 20 MHz in the PN appears randomly and the root reason is not very clear. We suspect this could be due to WiFi or cellular interference.

features a low-phase-noise 200 μ W inverse-class-F DCO without requiring 2-D capacitor tuning. Fabricated in 65-nm CMOS, the ULP ADPLL prototype achieves sub-1 ps_{rms} jitter while consuming 529 μ W, corresponding to a figure-of-merit of -244 dB.

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