Jitter Analysis and Benchmarking Figure-of-Merit for PLLs

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Motivation

- To evaluate jitter at the output due to various blocks in terms of f_{ref}, N, loop bandwidth and power consumption.
- To calculate the optimal value of loop bandwidth to minimize the jitter at the output for a given power budget.
- To define a benchmark figure-of-merit (FOM) to evaluate the PLL jitter performance in relation to the consumed power

Outline

- Derivation of VCO Phase noise and define FOM
- Evaluation of Phase noise due to the Loop (PFD, CP, Divider) and define an FOM for the loop
- Calculation of jitter at the output
- Calculation of optimal bandwidth for min. jitter
  - Calculation of minimum jitter
- Define a FOM for the PLL

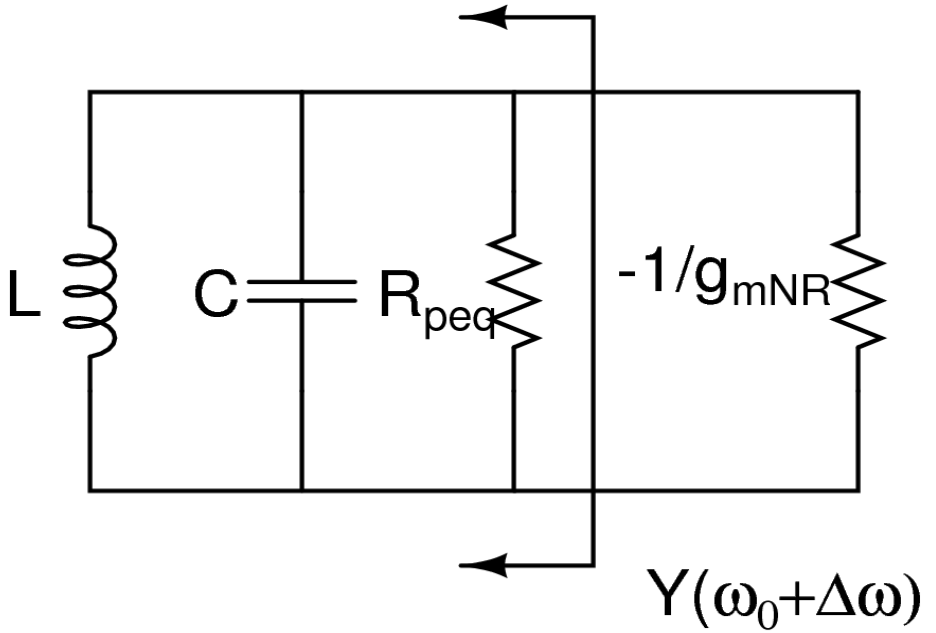
Voltage Controlled Oscillator

$$Q_T = \frac{R_{peq}}{Z_0}$$

$$Z_0 = \sqrt{\frac{L}{C}}$$

$$g_{mc} = \frac{1}{R_{peq}}$$

$$g_{mNR} = -\alpha g_{mc}$$



Start-up gain

Negative conductance

$$Y(\omega_0 + \Delta\omega) = \frac{1}{R_{peq}} + j\omega C + \frac{1}{j\omega L}$$

$$\approx \frac{1}{R_{peq}} + \frac{2j}{Z_0} \times \left(\frac{\Delta\omega}{\omega_0}\right)$$

Gets cancelled by negative conductance

Phase Noise Calculation

Noise to Carrier ratio

$$\mathcal{L}(\Delta\omega) = \frac{v_n^2}{V_{RMS}^2} = \frac{|i_{nT}^2| + |i_{nNR}^2|}{|Y(\omega_0 + \Delta\omega)|^2} \times \frac{1}{V_{RMS}^2} \longrightarrow \mathcal{L}(\Delta\omega) = kT\left(\frac{Z_o}{Q_T}\right) \times \left(\frac{\omega_0}{\Delta\omega}\right)^2 \times \frac{1+\alpha\gamma}{V_{RMS}^2}$$

Signal Power

$$V_{RMS} = \frac{1}{\sqrt{2}} \times \frac{2}{\pi} I_B R_{peq} = \frac{\sqrt{2}}{\pi} I_B Q_T Z_0$$

$$V_{RMS}^2 = \frac{32\alpha^2}{\pi^2 \left(\frac{g_m}{I}\right)^2}$$

For a given start-up gain (α)

$$\alpha = \frac{g_{mNR}}{g_{mc}} = \frac{1}{2} \times \left(\frac{g_m}{I}\right) \times \frac{I_B}{2} \times Q_T Z_0$$

$$I_B = \frac{4\alpha}{\left(\frac{g_m}{I}\right) Q_T Z_0}$$

$$\Rightarrow \mathcal{L}(\Delta\omega) = \frac{\pi^2 kT\,(1+\alpha\gamma)}{8\alpha Q_T^2} \left(\frac{g_m}{I}\right) \times \left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{I_B}$$

Quality of the oscillator

Assumptions

- LC-VCO with cross-coupled diff pair, tail current : I_B
- Current flowing into the tank is a square wave of amplitude $0.5I_B$
- Tank filters out all harmonics except fundamental component

VCO FOM

$$FOM_{VCO} = 10log_{10}\left(\mathcal{L}_{VCO}(\Delta\omega) \times \frac{P}{1mW} \times \left(\frac{\Delta\omega}{\omega_0}\right)^2\right)$$

P.Kinget, “Integrated GHz voltage controlled oscillators,” in Analog Circuit Design: (X)DSL and Other Communication Systems; RF MOST Models; Integrated Filters and Oscillators, W.Sansen, Ed. Boston, MA: Kluwer, 2002

$$\mathcal{L}_{VCO}(\Delta\omega) = \left(\frac{\omega_0}{\Delta\omega}\right)^2 \times \left(\frac{1mW}{P}\right) \times 10^{FOM_{VCO}/10}$$

Phase Noise contribution from Loop

$$\mathcal{L}_{loop} = \frac{S_{\phi,loop}}{2} = \frac{N^2}{2}\left(S_{\phi,ref} + S_{\phi,div} + S_{\phi,PD} + \frac{S_{i,CP}}{K_d^2}\right)$$

- Flicker noise is neglected. Only white thermal noise is considered
- Loop filter noise is neglected.
- Synchronizer assumed at the output of dividers
  - Noise of the retiming D-Flip Flop alone matters.
  - Power of the rest of the circuit can be scaled down.

Phase noise due to Reference Path

Noise from PFD, divider and reference have the following analysis

Spectrum of noise referred to the input of the PFD

$$\frac{\sigma_t^2}{T^2} \times (2\pi)^2 = \sigma_\phi^2 = S_\phi(f) \times \frac{f_{ref}}{2} \Rightarrow \boxed{S_\phi(f) = 8\pi^2 f_{ref} \sigma_t^2}$$

$$\sigma_t^2 = \frac{\langle v_n^2 \rangle}{SL_{out}^2} = \frac{kTF_n}{C_{out} SL_{out}^2}$$

$$P = f_{ref} C_{tot} V_{DD}^2$$

$$\sigma_t^2 = \frac{f_{ref}}{P} \left(\frac{F_n kT V_{DD}^2 C_{tot}}{SL_{out}^2 C_{out}} \right)$$

To minimize jitter, it is assumed that the sizing is done to minimize this factor.

$$\boxed{\sigma_t^2 \propto \frac{f_{ref}}{P} \Rightarrow S_\phi \propto \frac{f_{ref}^2}{P}}$$

Phase noise due to Charge Pump

$$S_{i,CP} = (S_{i,NMOS} + S_{i,PMOS}) \frac{T_{ON}}{T_{ref}} = 4kT\gamma \frac{T_{ON}}{T_{ref}} (g_{mp} + g_{mn})$$

$$g_{mp} = g_{mn} = g_m = \frac{\alpha I}{V_{gs} - V_t} \qquad P = IV_{DD} \times \frac{T_{ON}}{T_{ref}}$$

$$\frac{S_{i,CP}}{K_d^2} = \frac{f_{ref}^2}{P} \left(T_{ON}^2 \times \frac{32\pi^2 \alpha\gamma kTV_{DD}}{(V_{gs} - V_t)} \right) \propto \frac{f_{ref}^2}{P}$$

Needs to be optimized before admittance scaling

Loop Phase Noise Benchmarking

- Phase noise of all blocks scale equally with power.
- For a given power budget, relative proportions are fixed to minimize the loop's phase noise.
- Admittance scaling is performed on the loop, keeping relative power dissipation in the blocks the same.

$$\mathcal{L}_{loop} \propto N^2 \frac{f_{ref}^2}{P_{loop}} = \frac{f_{out}^2}{P_{loop}} \longrightarrow FOM_{loop} = 10log_{10}\left[\mathcal{L}_{loop}\left(\frac{1Hz}{f_{out}}\right)^2 \frac{P_{loop}}{1mW}\right]$$

$$\boxed{\mathcal{L}_{loop} = 10^{FOM_{loop}/10}\left(\frac{f_{out}}{1Hz}\right)^2 \frac{1mW}{P_{loop}}}$$

PLL Output Jitter

$$\sigma_{t,PLL}^2 = \sigma_{t,VCO}^2 + \sigma_{t,loop}^2$$

Dependent on bandwidth of the transfer function.

$$\sigma_{t,VCO}^2 = \frac{1}{2\pi^2 f_{out}^2} \int_0^\infty \mathcal{L}_{VCO}(f_m) \left| H_{VCO}(f_m) \right|^2 df_m$$

$$H_{VCO}(s) = H_{VCO,0}\left(s\frac{f_{c,0}}{f_c}\right)$$

The bandwidth is scaled from f_{c0} to fc. The shape (phase margin) is kept constant while in this scaling.

$$\mathcal{L}_{VCO}(f_m) = \frac{\mathcal{L}_{VCO}(f_r) f_r^2}{f_m^2}$$

Loop gain

$$\sigma_{t,VCO}^2 = \frac{\mathcal{L}_{VCO}(f_r) f_r^2}{\pi f_{out}^2} \times \frac{f_{c,0}}{f_c} \times \int_0^\infty \left| \frac{H_{VCO}(s)}{s} \right|^2 ds$$

$$\sigma_{t,loop}^2 = \frac{\mathcal{L}_{loop}}{2\pi^2 f_{out}^2} \times \frac{1}{2\pi} \times \frac{f_c}{f_{c,0}} \times \int_0^\infty \left| H_{loop}(s) \right|^2 ds$$

$$H_{loop}(s) = \frac{G(s)}{1+G(s)}$$

$$H_{VCO}(s) = \frac{1}{1+G(s)}$$

PLL Output Jitter

Minimizing $\sigma^2_{t,PLL}$ w.r.t f_c yields

$$f_{c,opt} = 2\pi\sqrt{\frac{\mathcal{L}_{VCO}(f_r)f_r^2}{\mathcal{L}_{loop}}} \times \sqrt{f_{c,0}^2\frac{\int_0^\infty \left|\frac{1}{s(1+G(s))}\right|^2 ds}{\int_0^\infty \left|\frac{G(s)}{(1+G(s))}\right|^2 ds}}$$

NOTE: The optimum bandwidth is for minimizing the jitter. It may not meet stability or settling time requirements.

When the bandwidth is optimum, jitter due to loop and VCO are equal.

$$\sigma^2_{t,loop} = \sigma^2_{t,VCO}$$

$$\mathcal{L}_{VCO}(f_{c,opt}) \approx \mathcal{L}_{loop}$$

$F_{c,opt}$ is approximately where the spectrum of the VCO and loop noise intersect.

PLL Output Jitter

$$\sigma^2_{t,PLL,min} = \frac{1}{2\pi}\sqrt{\frac{1}{P_{loop}P_{VCO}}}10^{\frac{FOM_{loop}+FOM_{VCO}}{20}}\sqrt{\left(\int_0^\infty \left|\frac{G(s)}{1+G(s)}\right|^2 ds\right)\left(\int_0^\infty \left|\frac{1}{s(1+G(s))}\right|^2 ds\right)}$$

For a given PLL Power Budget, to minimize jitter, $P_{loop} = P_{VCO}$

$$\sigma^2_{t,PLL,min} = \frac{1}{P_{PLL}}\left[\frac{4}{\pi}10^{\frac{FOM_{loop}+FOM_{VCO}}{20}}\right]\times \sqrt{\left(\int_0^\infty \left|\frac{G(s)}{1+G(s)}\right|^2 ds\right)\left(\int_0^\infty \left|\frac{1}{s(1+G(s))}\right|^2 ds\right)}$$

Order and Type dependent constant

PLL FOM

$$\sigma^2_{t,PLL,min} \propto 1/P_{PLL}$$

$$FOM_{PLL} = 10log\left[\left(\frac{\sigma_{t,PLL}}{1s}\right)^2 \frac{P_{PLL}}{1mW}\right]$$

- The minimum PLL jitter is independent of f_{ref}
- The design quality of VCO and the loop are equally important since they have equal contribution to power and jitter in an optimized design