Accurate Phase Noise Prediction in PLL Synthesizers

Here is a method that uses more complete modeling for wireless applications

By Lance Lascari
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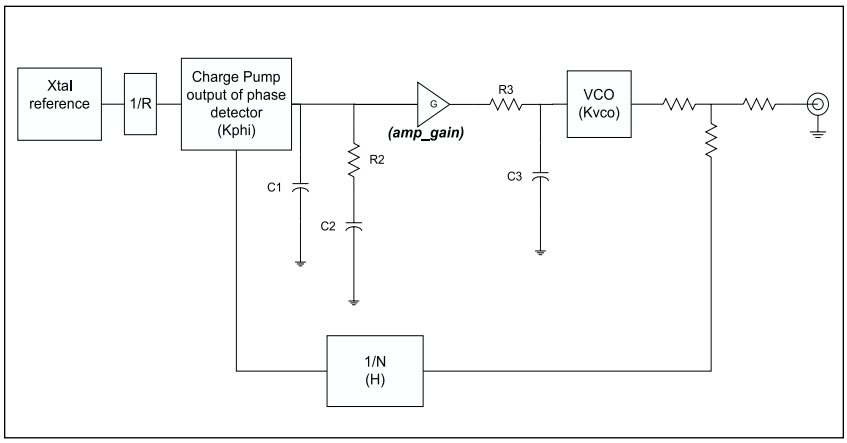
In modern wireless communications systems, the phase noise characteristics of the frequency synthesizer play a critical role in system performance. Higher than desired phase noise can cause degraded system performance by reducing the signal to noise ratio, increasing adjacent channel power, and reducing adjacent channel rejection.



▲ **Figure 1. $Z_{fil3}(f)$ with optional amplifier inserted.**

While many of the factors that affect phase noise in phase-locked frequency synthesizers are well understood, designers often overlook others. Neglecting these additional factors can cause frustration and overdesign, when a more complete up-front analysis may have yielded more elegant solutions.

The goal of this article will be to first review the models for standard noise sources and how these are analyzed, then to do the same for noise caused by the often forgotten resistors and amplifiers within the loop filter.

This is Part 1 of a two-part article. Part 2 will be published in the May 2000 issue of *Applied Microwave & Wireless* magazine.

Standard phase noise sources and analysis techniques

The basic equations describing the loop's frequency response will be given with a brief description of each. Plots that accompany the equations are from analysis of the test cases presented later in the article, and are typical for all PLL designs. The complete equations in context can be found in [1]. The equations presented here and in [1] have been drawn in part from [4], as well as [3], [6] and [7]. The amplifier within the loop will be ignored for all analysis presented here, as the implications of this amplifier will be discussed in the text.

Equation 1 describes the transfer function of the third-order loop filter. Equation 2 describes the transfer function of the second order loop filter and is applicable to systems that do not require the third pole for additional reference suppression.

$$Z_{fil3}(f) = \frac{Z_{fil}(f) \times \frac{1}{2 \times \pi \times f \times i \times C_3}}{Z_{fil}(f) + R_3 + \left(\frac{1}{2 \times \pi \times f \times i \times C_3} \right)} \quad (1)$$

$$Z_{fil}(f) = \frac{(1 + R_2 \times 2 \times \pi \times f \times i \times C_2)}{[2 \times \pi \times f \times i(C_2 + C_1 + R_2 \times 2 \times \pi \times f \times i \times C_1 \times C_2)]} \quad (2)$$

The total forward loop response, $G(f)$, includes everything from phase detector to VCO, and is represented by Equation 3. The equation for $G_{\_pd}(f)$ is not included, but it represents the transfer function of the discrete-sampling phase-frequency detector. Details on this function can be found in [7].

$$G(f) = \frac{K_\phi \times Z_{fil3}(f) \times K_{vco} \times \text{amp\_gain}}{2 \times \pi \times \text{f} \times \text{i}} \times G_{pd}(f) \quad (3)$$

The reverse loop, or feedback gain, is defined as the reciprocal of the total frequency multiplication factor in the loop, N, as shown in Equation 4.

$$H = \frac{1}{N} \quad (4)$$

Equation 5 illustrates the open loop gain, $G_{ol}(f)$. The open loop gain is the product of equations 3 and 4, showing the response around the loop. This equation is particularly useful for stability analysis. A plot of this response is shown in Figure 2.

$$G_{ol}(f) := G(f) \times H \quad (5)$$

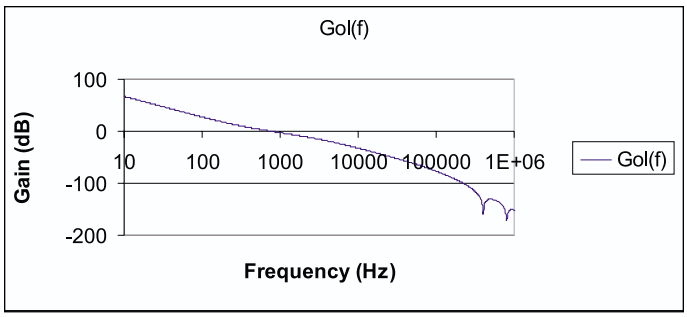
Because this is a simple negative feedback system, the closed loop response, $G_{cl}(f)$, at the VCO output is represented by the familiar feedback relationship seen in Equation 6. A plot of this response is shown in Figure 3.

$$G_{cl}(f) = \frac{G(f)}{1 + G(f) \times H} \quad (6)$$

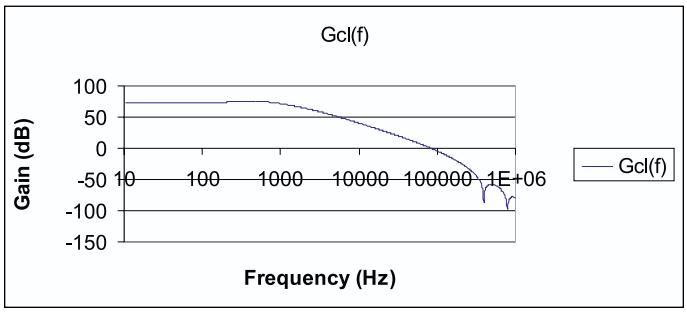
The well known noise sources (expressed in terms of equivalent noise voltage) are specifically crystal reference (TCXO) noise; phase detector noise; and VCO phase noise.

Crystal reference oscillator noise — The crystal oscillator noise is "amplified" in the loop by the gain of the closed loop transfer function. A simple approximation for this noise source due to the crystal reference itself, as with any oscillator, is that it is inversely proportional to offset frequency. Higher order approximations or actual data could be used if it were available, but the 1/f approximation is a good starting point.

Within the loop bandwidth of the synthesizer, the closed loop transfer function, $G_{cl}(f)$ is very large in magnitude, hence it increases the level of the reference oscillator noise. This gain is flat until it reaches the loop bandwidth, after which it drops off rapidly. This function represents amplification of the noise within the loop bandwidth, but attenuation of the noise above this frequency. The gain within the loop bandwidth comes largely from the ratio of the loop division ratio, N, by the reference division ratio, R. If this noise can be observed at all, it is generally seen very close to the carrier (where it is visible above the other major noise sources).



▲ **Figure 2. Open loop frequency response.**



▲ **Figure 3. Closed loop frequency response.**

If a TCXO is used, phase noise data should be obtained from the manufacturer so that reference values can be used with the models. Measuring the noise of a crystal oscillator can be quite difficult since the noise is significantly below the noise of most readily available test equipment. In fact, it may be easier to work backwards from measured PLL data to determine the TCXO noise if the data are not available from the manufacturer. Equation 7 illustrates the noise due to the reference oscillator, $N_{tcxo}(f)$, at the synthesizer output.

$$N_{tcxo}(f) = \frac{10^{\left(\frac{N_{tcxo\_ref}}{20}\right)}}{\frac{f}{f_{tcxo\_ref}}} \times \left(G_{cl}(f) \times \frac{1}{R}\right) \quad (7)$$

Phase detector noise — $N_{p\_d}(f)$, is a form of noise that represents the internal noise floor of the phase/frequency detector and frequency dividers within the PLL. This

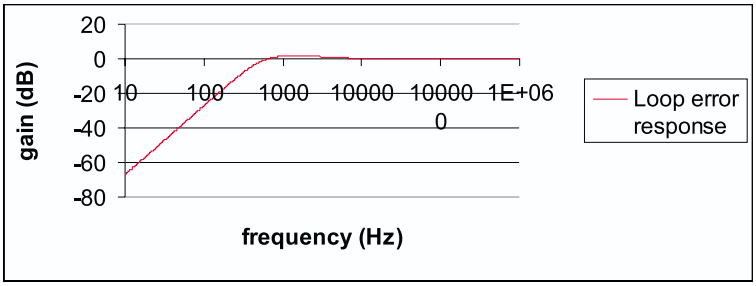
noise is modeled as flat versus frequency and the specific value for N_{pd_ref} can be obtained from the manufacturer of the synthesizer IC. For National Semiconductor synthesizers (the one used in this article, for example), the phase detector noise floor is given for an effective reference frequency of 1 Hz. The actual noise floor of the phase detector degrades proportional to 10*log(F_{ref}/1 Hz). This noise source is flat with respect to frequency, but it is shaped by the closed loop transfer function of the synthesizer, as shown in Equation 8.

$$N_{p\_d}(f) = 10^{\frac{N_{pd\_ref} + 10\log\left(\frac{f_{ref}}{Hz}\right)}{20}} \times G_{cl}(f) \quad (8)$$

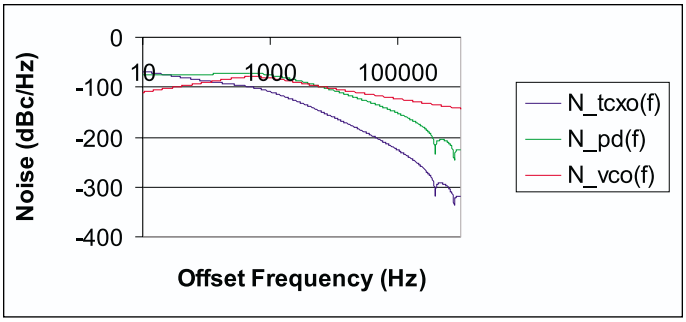
Free-running VCO noise — This tends to have the typical noise profile. The noise is inversely proportional to offset frequency from the carrier. The synthesized output, however, is the result of the PLL "cleaning up" the close in phase noise of the VCO. This composite noise is calculated in Equation 9. The noise of the VCO is effectively high-pass filtered by the PLL, providing rejection of phase noise or phase error within the bandwidth, but leaving VCO noise well outside of the loop bandwidth unaffected. A plot of this high-pass filter function provided by the PLL is shown in Figure 4.

$$N_{vco}(f) = \frac{10^{\left(\frac{N_{vco\_ref}}{20}\right)}}{\frac{f}{f_{vco\_ref}}} \times \left(\frac{1}{1 + G_{ol}(f)}\right) \quad (9)$$

A plot of the commonly analyzed phase noise sources described above at the synthesizer output is shown in Figure 5.



▲ **Figure 4. Loop error response.**



▲ **Figure 5. TCXO, phase detector and VCO noise.**

Models for noise in a typical third order loop filter

Prior to delving into the circuit equations, it is important to outline the methodology that will be employed to analyze the problem. The approach used will be to first determine the voltage at the input of the VCO due to each of the noise sources in the loop. This voltage will then be used to calculate the equivalent Frequency Modulation (FM) (i.e. phase noise) at the VCO output due to each of these sources using the VCO gain, K_{vco}.

A key parameter used to analyze frequency modulation is the modulation index, m, calculated using Equation 10.

$$m = \frac{d}{f_m} \quad (10)$$

where m = modulation index=peak phase deviation in radians; d = frequency deviation; and f_m =message or modulating frequency.

In the case of a "direct" FM system, where the modulation/message is fed directly to the VCO in the form of voltage, the frequency deviation is simply the product of the modulation voltage and the tuning sensitivity (volts × Hz/volt = Hz).

If the peak phase deviation is well below one radian, as is the case with all that will be studied here, the higher order Bessel functions can be ignored and the relative level of the sidebands on the carrier due to the modulating frequency can be calculated using Equation 11, see reference [5] for further detail on this subject.

$$\text{sideband\_level} = 20\log\left(\frac{m}{2}\right) \quad (11)$$

These simple equations for frequency/phase modulation form the basis for the analysis of phase noise due to voltage noise sources within the loop hardware.

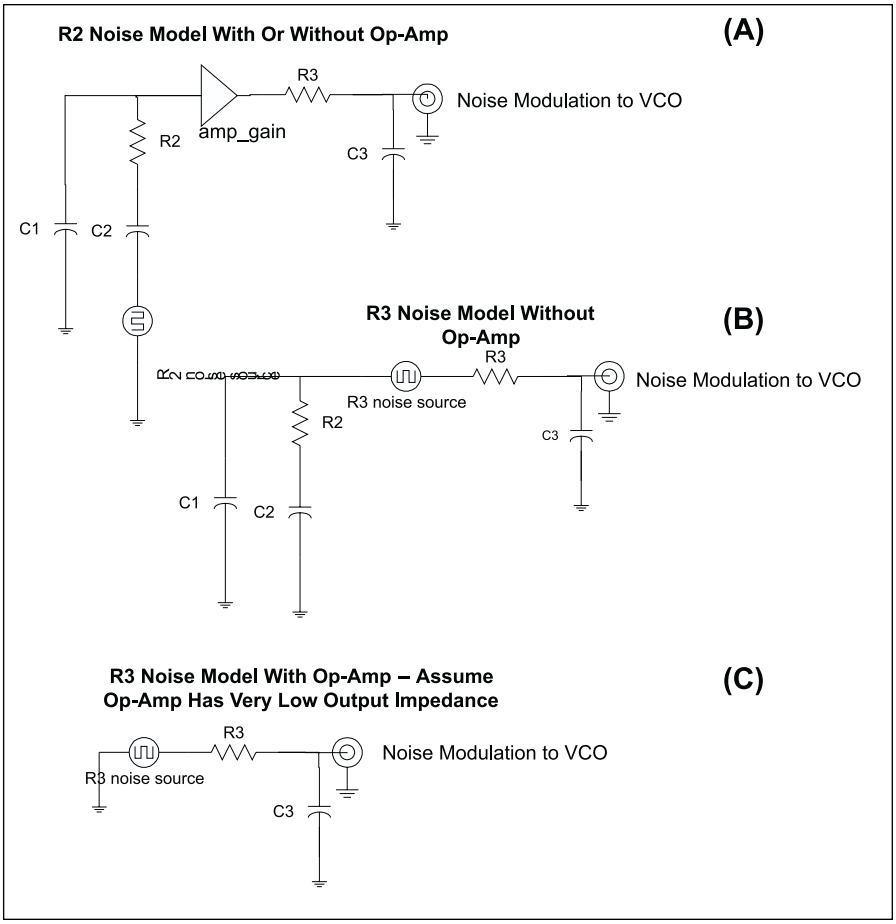
Calculating the noise voltages in the loop

Since the noise sources appear in different circuit nodes throughout the loop, the frequency response of the transfer function between each source and the VCO input will be different. This, in turn, results in modulation at the VCO output unique to each source in frequency and magnitude.

It is important to realize that in a system such as this, the resistor or op-amp noise modulates the VCO even if a PLL were not connected — so the "corruption" due to

the resistors and op-amp can be considered an open-loop phenomenon. However the net result in the synthesized output requires the closed loop response, and the analysis is identical to the analysis used to show the effect of the PLL on the stand-alone VCO phase noise in Equation 9. Valuable insight can be gained by observing the open and closed loop SSB phase noise curves rather than just looking at the total output phase noise of the closed loop system. The connection between the open and closed loop responses, is the high-pass transfer function plotted in Figure 4, sometimes referred to as the error response of the loop.

The validity of the open-loop analysis technique requires the assumption that the charge pump does not load down the loop filter excessively. The following key points support this assumption. First, when in lock, the charge pump does very little but provide very minor corrections to keep the loop locked. Second, the charge pump is made up of a current source and a current sink, both of which represent a high impedance when operating in a linear region. The closed-loop action of the synthesizer fights the resistor and op-amp noise, but that is adequately described by the analysis of the closed loop system.



▲ **Figure 6. (a) R2 noise model with or without op-amp; (b) R3 noise model without op-amp; (c) R3 noise model with op-amp, assuming that the op-amp has very low output impedance.**

Noise found in resistors

Random electron motion inside of ordinary resistors makes for a "built-in" noise source in every circuit containing resistors. The noise is white in nature [8], with it's power in watts dissipated in an equivalent 1 ohm resistor is shown in Equation 12, and the units are volts^2/Hz.

$$P_{\text{resistor\_noise}}(R) = 4 \times k \times \text{Temp} \times B \times R \quad (12)$$

Thus, Equation 13 computes the equivalent RMS noise voltage generated in a known resistance

$$V_{\text{resistor\_noise}}(R) = \sqrt{4 \times k \times \text{Temp} \times R \times B} \quad (13)$$

where k = Boltzmann's constant; Temp = temperature in kelvins; B = bandwidth in Hz; and R = resistance in ohms. For most of our analysis we will use a bandwidth of 1 Hz.

These equations simply show the equivalent noise voltage source that appears in series with each resistor. Note that the noise could just as easily be modeled as a noise current source in parallel with the resistor. References [2] and [8] provide details on the noise in resistors and op-amps. When crunching the numbers for typical resistor values, one may initially dismiss the voltages as minuscule. As we will show later, even nanovolts of noise can cause several dB of degradation in the single-sideband phase noise of a synthesizer because K_{vco} is often a very large number.

Figure 6 shows the basic PLL loop filter and where the noise sources appear. The charge pump connection to the PLL has been left out for these models because it represents a very high impedance when the loop is locked. As previously stated, the initial analysis of the resistor noise will be done "open loop," and the effects of the PLL on shaping this noise further will be investigated after the basic models are developed.

Since the noise sources are uncorrelated, each resistor is analyzed separately and the effects are added at a later stage. Deriving the actual noise voltage versus frequency at the input to the VCO tuning port is a matter of basic circuit analysis using the models in Figure 6.

Resistor noise analysis for the "case 2" example PLL in this article that will be discussed later is shown in Figure 7 and Figure 8. Figure 7 shows the baseband noise voltages at the VCO input in the open loop case, and Figure 8 shows the noise contribution to the synthesizer output. ■

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1. Complete MathCAD Analysis used in this article is available in MathCAD and PDF formats at http://home.rochester.rr.com/lascari/lancepll.zip.
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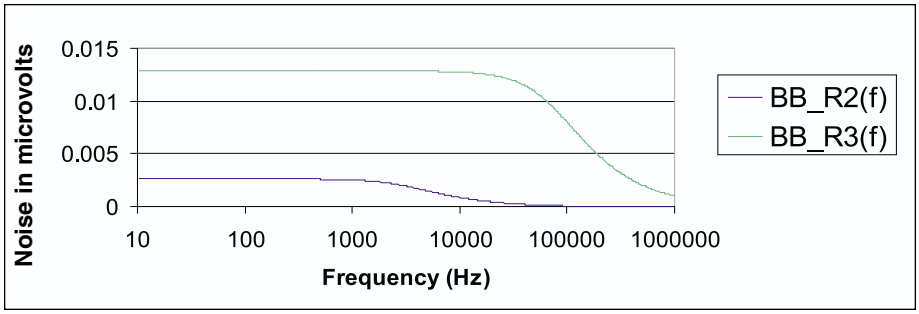
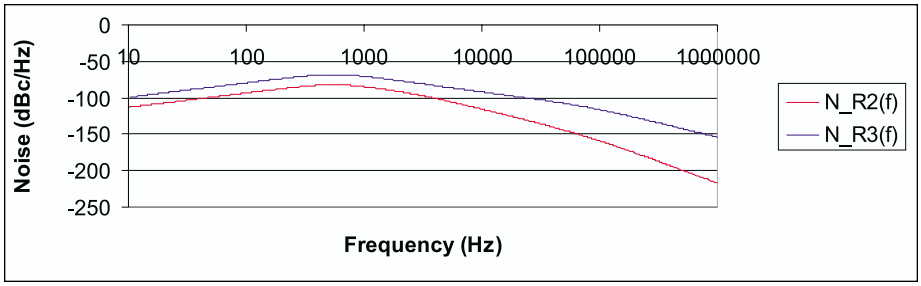
7. Jeff Blake, "Design of Wideband Frequency Synthesizers," *RF Design*, May 1988.
8. "Noise Specs Confusing," Application Note 104, National Semiconductor.

Figure	Analysis	Conditions	Comments
6a	R2	Without op-amp	Assume the op-amp is not present and the R2 noise must be calculated throught the entire network.
6a	R2	With op-amp	Assume for R2 noise analysis the op-amp input impedance is infinite, and the R2 noise out of the network consisting of R2, C1 and C2 is determined. This noise is then amplified by amp_gain before being passed through the network consisting of R3 and C3.
6b	R3	Without op-amp	In this case, the R3 noise source is "floating" in the loop filter network, and the transfer function between this source and the output of the network includes the impedances of all the filter components.
6c	R3	With op-amp	Since the op-amp output impedance will be assumed to be very low, we model this as a short. Hence, this is the simplest model of all, R3 shorted to ground.

▲ **Table 1. Description of the resistor noise models shown in Figure 6.**



▲ **Figure 7. Baseband noise voltages at the VCO input in the open-loop state.**



▲ **Figure 8. Resistor noise contributions at the VCO output after the PLL's high-pass error function is included.**

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Accurate Phase Noise Prediction in PLL Synthesizers

Part 2: Here is a method that uses more complete modeling for wireless applications

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As discussed in part one of this article, published in the April issue of *Applied Microwave & Wireless*, phase noise characteristics of the frequency synthesizer contribute greatly to system performance. In this concluding section, we will show and discuss experimental results for the op-amp in loop filter.

Design goals	Value	Comments
Output Frequency	865 MHz	
Reference Frequency	200 kHz	
Frequency Step Size	12.5 kHz	
PLL Loop bandwidth	750 Hz	Get as close as possible with available components
Phase Margin	55 degrees	
Additional Reference Frequency Attenuation Required from the Third Pole	10 dB	

▲ **Table 2. Design goals for the example loop filter design.**

Op-amp in loop filter

While the cases using the passive loop filter (no op-amp) are simply a matter of circuit analysis, the case using the active filter requires some explanation. This case will only be described here; the accompanying analysis can be found in the supporting MathCad documents.

With the op-amp in the loop, and the filter configuration shown in Figure 1, four different noise sources and important factors exist within the loop itself: R_2, the op amp itself, the gain of the op-amp, and R_3.

The noise within R_2 is the same as the cases previously mentioned. However once this noise is determined, the gain of the amplifier needs to be applied to it (amp_gain in Figure 1). The output of the op-amp is again filtered by R_3 and C_3. A schematic of this is pictured in Figure 2a.

The op-amp itself contributes noise, and this is one reason to place the op-amp after the second order filter section but before the third pole. The third pole can then provide some attenuation of the broadband noise. Manufacturer's data sheets will usually specify the input noise of the op-amp in $nV/\sqrt{Hz}$. This noise voltage is simply multiplied by the amplifier's gain (amp_gain), and then passed through the filter formed by R_3 and C_3.

Op-amps are usually regarded as very low-output-impedance devices. For this reason, the analysis of the noise due to R_3 can be greatly simplified if an op-amp is in the loop as shown in Figure 1. If it is assumed that the op-amp output impedance is virtually a short (which would be accurate, even if the op-amp output were a few hundred ohms), then the noise voltage generated in R_3 is simply connected to ground, then filtered through R_3 and C_3.

Practical design example

To show the effect of the resistor noise, two different loop filters were designed to meet the basic specifications outlined in the goals section of Table 2. The only differences between the filters were their implementation of the third

pole. The values used in each of the designs were typical of what one designer might choose over another.

Experimental setup

Equipment used in the lab setup included a Hewlett-Packard 8563E spectrum analyzer with the phase noise utility software (P/N HP85671A) installed; a PC running a custom application developed to gather tabular data after the phase noise utility was run; and the PLL synthesizer under test (modified standard product produced by Adaptive Broadband Corporation).

The results presented in Figures 9 and 10 represent five averages of each phase noise measurement. In order to show the limitations of the measuring system, (i.e. the spectrum analyzer), the phase noise of the extremely low noise HP 8642B signal generator was plotted for comparison purposes. At higher offset frequencies where the measurements and models begin to disagree, it is clear that that the noise floor of the spectrum analyzer is contributing to measurement error.

Component/Specification	Value	Comments
Synthesizer IC, National LMX2350 Fractional-N PLL	Allows 1/16th Fractional mode	
Phase Detector Noise Floor (Npd_ref from Equation 6)	–200 dBc/Hz	Data supplied by National Semiconductor.
Phase Detector Gain	1.6 mA/cycle	Set to maximum for this design.
VCO Tuning Sensitivity, K_{vco}	27 MHz/volt	Custom vendor supplied component, measured at frequency of interest.
VCO Phase Noise	–103 dBc/Hz at 10 kHz offset	Measured for this particular device using a very narrow and quiet loop.
TCXO reference oscillator Frequency	12 MHz	
TCXO reference oscillator Phase Noise (Ntxco_ref from Equation 7)	–125 dBc/Hz at 100 Hz offset	This number was estimated from measurement data from many PLLs. This is roughly 10 dB worse than published data on a similar product from the TCXO vendor. Measurements for the model used were unavailable.

▲ **Table 3. Specifications for the components available.**

Discussion of experimental results

Figures 9 and 10 show excellent agreement between the modeled phase noise of the synthesizers and the measured results. The conclusion that must be drawn is resistor noise can be a very significant contributor to synthesizer phase noise, and thus needs to be considered in all low-noise synthesizer designs. For the case of these experiments, and others performed by the author, the models presented accurately predict this noise, allowing the analysis of all of these degradations at the time the loop is designed [1].

Loop Filter Component Values	Value for Case 1	Value for Case 2
C1	0.1 μF	0.1 μF
R2	500 ohms	500 ohms
C2	1 μF	1 μF
R3	1 kohm	10 kohm
C3	1000 pF	100 pF

▲ **Table 4. Component values for the two loop filters studied.**

The loop filters for case 1 and case 2 both meet the basic requirements of the design but have drastically different phase noise characteristics. For instance, at the 10 kHz offset points, the two synthesizers differ in phase noise by almost 10 dB. For narrowband systems with channels spaced at this interval, this would equate to a difference in adjacent channel rejection of 10 dB when comparing case 1 to case 2. Although the resistors are much smaller in the case 1 analysis, the noise contribution should not be ignored.

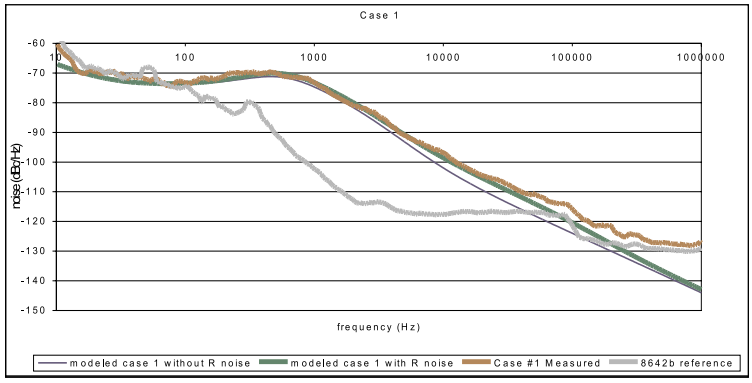
Even more significant than the agreement well outside of the loop bandwidth is the agreement near the loop bandwidth. Since the magnitude of the noise that falls near the loop corner is much larger than the noise far outside of the loop bandwidth, it contributes significantly to the RMS phase error and residual FM metrics. These metrics are very indicative of the performance degradations caused by frequency synthesizers in QAM and FM/FSK systems respectively. If the synthesizer noise were modeled without resistor noise, the results would be dramatically different, especially for case 2.

Reducing resistor and op-amp noise contributions

When designing a frequency synthesizer, there are

often several degrees of freedom that can be exercised in order to minimize the system phase noise. If there are no degrees of freedom, up-front design analysis will at least show an accurate prediction of the phase noise. This prediction may help to make system tradeoffs rather than sticking to a more stringent synthesizer specification.

In most synthesizer designs, it seems that R3 is typically the single most significant contributor to the resistor noise. This begs the question, "Is the third pole really needed?" If the reference suppression within the loop is sufficient without the third pole, it is in the designer's best interests to leave these parts out of the design. If this pole is required, the value of R_3 should be kept as small as possible without upsetting the basic filter response.



▲ **Figure 9. Measured and modeled phase noise of the example synthesizer, case 1.**

Some VCO designs themselves use resistors to supply the tuning voltage to the varactor (the similarity to the R_3 analysis is staggering). In many published VCO designs, large resistors are used to feed the varactor. This is a good choice for simple, and low-cost designs since resistors are inexpensive, resonance-free, and they don't typically degrade resonator Q if they're large relative to the other shunt resistances in the circuit. Resistors are hardly a good choice, however, if the tuning sensitivity (VCO gain) is high. The noise contribution by this resistor is proportional to its value alone in this case; a small resistor in series with a choke may be a good choice in many applications.

Op-amps, even if chosen carefully, represent significant contributions to phase noise. The synthesizer designer should be careful to determine whether an op-amp is truly required in order to meet the system requirements. If increased voltage is required, consider using an external charge pump with higher supply voltages (some synthesizer ICs still support the connections required for using an external charge pump). Obtaining good balance in an external charge pump can be difficult, leading to increased reference spurs and power supply noise at the reference frequency. A low noise charge pump potentially offers reduced noise over the op-amp, as the tuning voltage range can be increased with a designer-chosen charge pump current. This represents two degrees of freedom: lower tuning sensitivity and reduced resistor values due to potentially increased current. It would be excellent if the available synthesizer chips allowed for higher tuning voltages or specifically allowed for simple implementations of well-balanced external charge pumps.

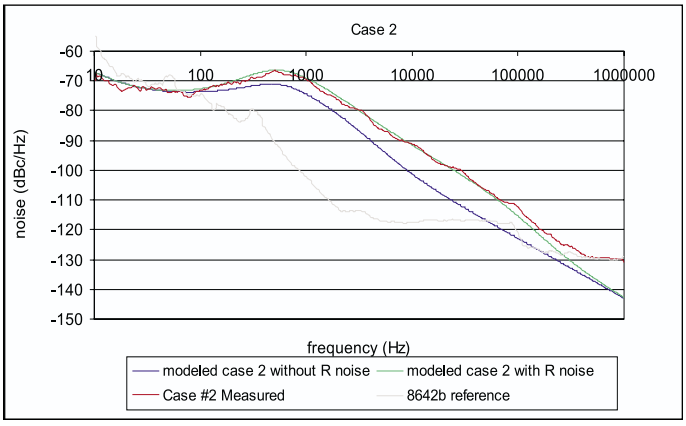
Reducing the VCO tuning sensitivity is another way to reduce the overall noise. This needs to be analyzed on a case-by-case basis, however, since the loop filter resistor values will increase with reduced tuning sensitivity. Any fixed magnitude noise sources in the loop will also drop proportionally with the VCO tuning sensitivity.

One particular option the author feels worthy of exploration is increasing charge pump current. With increased charge-pump current, the impedance (hence resistance) in the loop drops. If your synthesizer has a programmable charge pump current setting, leaving it at maximum is best in order to reduce the resistor noise contribution.

Each of the suggestions presented carries with it some design implication that needs to be carefully evaluated before tradeoffs are made. In some designs, simply increasing charge-pump current or eliminating the 3rd pole used for reference attenuation could yield dramatic improvement.

Conclusion

In order for designs to meet the increasingly demanding performance requirements in the wireless arena, a detailed understanding of every component is critical. While relatively simple, the models presented have demonstrated excellent accuracy when compared to experimental data. These circuit models represent new tools that enable the designer to make important tradeoffs during the initial synthesizer design phase, rather than on the bench using empirical and time-consuming techniques. ■



▲ **Figure 10. Measured and modeled phase noise of the example synthesizer, case 2.**

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