All-Digital TX Frequency Synthesizer and Discrete-Time Receiver for Bluetooth Radio in 130-nm CMOS

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***Abstract*—We present a single-chip fully compliant Bluetooth radio fabricated in a digital 130-nm CMOS process. The transceiver is architectured from the ground up to be compatible with digital deep-submicron CMOS processes and be readily integrated with a digital baseband and application processor. The conventional RF frequency synthesizer architecture, based on the voltage-controlled oscillator and the phase/frequency detector and charge-pump combination, has been replaced with a digitally controlled oscillator and a time-to-digital converter, respectively. The transmitter architecture takes advantage of the wideband frequency modulation capability of the all-digital phase-locked loop with built-in automatic compensation to ensure modulation accuracy. The receiver employs a discrete-time architecture in which the RF signal is directly sampled and processed using analog and digital signal processing techniques. The complete chip also integrates power management functions and a digital baseband processor. Application of the presented ideas has resulted in significant area and power savings while producing structures that are amenable to migration to more advanced deep-submicron processes, as they become available. The entire IC occupies 10 mm^2 and consumes 28 mA during transmit and 41 mA during receive at 1.5-V supply.**

***Index Terms*—All digital, Bluetooth, direct sampling, discrete time, frequency modulation, frequency synthesizers, phase domain, phase-locked loops, radio receivers, radio transmitters, sampled data circuits, single chip, system-on-chip (SoC), tranceivers.**

I. Introduction

DESIGN flow and circuit techniques of contemporary transceivers for multigigahertz mobile RF wireless applications are typically quite analog intensive and utilize process technologies that are incompatible with a *digital baseband* (DBB) and *application processor* (AP). Nowadays, the DBB and AP designs constantly migrate to the most advanced deep-submicron digital CMOS process available, which usually does not offer any analog extensions and has very limited voltage headroom. The aggressive cost and power reductions of high-volume mobile wireless solutions can only be realistically achieved by the highest level of integration, and this favors a digitally intensive approach to conventional RF functions in the most advanced deep-submicron process.

Given the task of designing highly integrated RF circuits in the digital deep-submicron process environment, we have realized that we are facing a *new paradigm*:

In a deep-submicron CMOS process, time-domain resolution of a digital signal edge transition is superior to voltage resolution of analog signals.

This is in clear contrast with the older process technologies, which rely on a high supply voltage (originally 15 V, then 5 V, and finally 3.3 V and 2.5 V) and a standalone configuration with few extraneous noise sources in order to achieve a good signal-to-noise ratio and resolution in the voltage domain, often at a cost of long settling time. In a deep-submicron process, with its low supply voltage (at and below 1.5 V), relatively high threshold voltage (0.6 V and often higher due to the MOSFET body effect), the available voltage headroom is quite small for any sophisticated analog functions. Moreover, considerable switching noise of substantial digital circuitry around makes it harder to resolve signals in the voltage domain. On the positive side, the switching characteristics of a MOS transistor, with rise and fall times on the order of tens of picoseconds, offer excellent timing accuracy at high frequencies, and the fine lithography offers precise control of capacitor ratios. Hence, we exploit this new paradigm by leveraging on these advantages while avoiding the weaknesses.

In this paper, we present details of the first ever reported all-digital RF frequency synthesizer and transmitter [1], as well as the first ever reported direct RF sampling discrete-time receiver [2] for wireless applications. Fig. 1 reveals major highlights of the proposed transceiver architecture. The design is part of a commercial single-chip Bluetooth radio constructed in a digital 130-nm CMOS process without any process enhancements. The presented technology features integration of digital baseband, RF, memory, power management and *RF built-in self-test* (RFBIST) functionality in a *system-on-chip* (SoC) that

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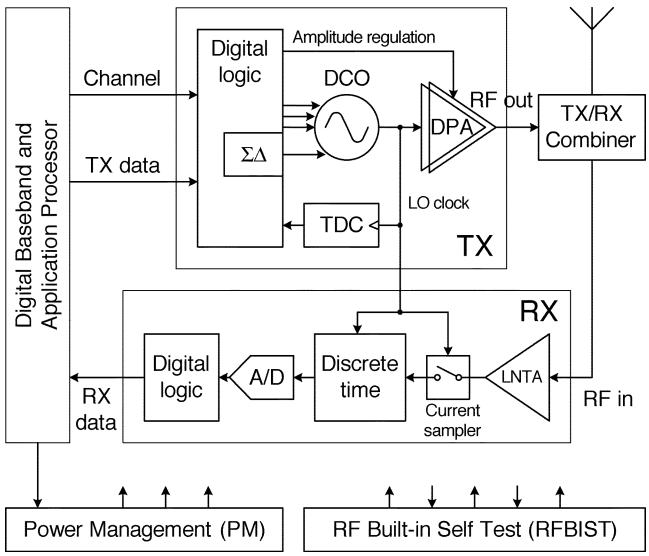

Fig. 1. Single-chip Bluetooth radio with an all-digital transmitter and a discrete-time receiver.

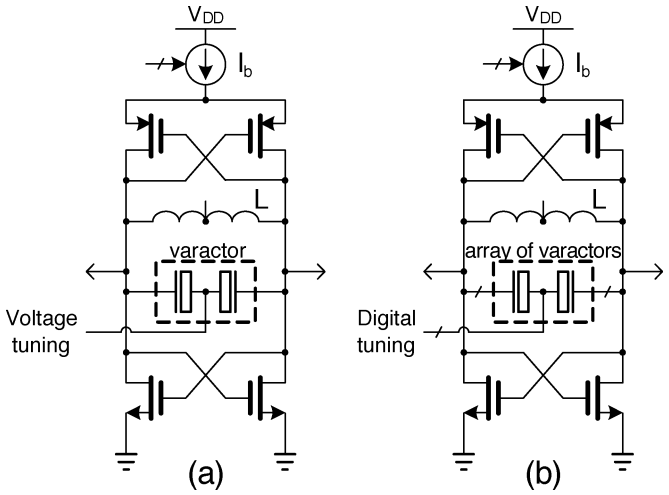

Fig. 2. Schematics of LC-tank core oscillators. (a) Voltage controlled (VCO). (b) Digitally controlled (DCO).

meets all of the Bluetooth specifications and is amenable to migration to newer deep-submicron CMOS processes.

Almost all the clocks used in the RX and TX are derived from and are synchronous to the RF oscillator clock. This helps to reduce susceptibility to the noise generated through clocking of the massive digital logic.

The organization of this paper is as follows. Section II presents the digitally controlled oscillator that lies at the heart of the all-digital frequency synthesizer. The all-digital transmitter, based on the frequency synthesizer with a wideband frequency modulation capability, is described in Section III. The direct RF sampling receiver is presented in Section IV. The implementation and measured results are covered in Section V.

II. Digitally Controlled Oscillator

A *digitally controlled oscillator* (DCO), the first ever reported in [3] for RF wireless applications, lies at the heart of the proposed *all-digital PLL* (ADPLL) frequency synthesizer. It deliberately avoids any analog tuning voltage controls and is realized as an ASIC cell with truly digital inputs and outputs. The DCO has a potential to exhibit less phase noise than a comparable voltage-controlled oscillator (VCO). Fig. 2 compares the cores of those two types of RF oscillators having identical *LC* tank topologies, two cross-coupled pairs of NMOS and PMOS transistors, and biasing circuitry. The major difference lies in the control method of the variable capacitance of the *LC* tank for the purpose of frequency tuning, and this is where their respective noise contributions differ.

The VCO relies on a developed tuning control voltage to control its oscillating frequency with the transfer function gain of $K_{\rm VCO} = \Delta f/\Delta V$ that is usually on the order of hundreds of MHz/V. This results in high susceptibility to frequency pushing and high vulnerability to power supply and ground noise. The DCO, on the other hand, is significantly more robust to such phenomena. It was shown in [4] that by biasing each of the varactors at one of the two $K_{\rm VCO} \approx 0$ flat points of the C–V curve, the frequency pushing was measured as low as 600 kHz/V, which results in the low sensitivity to noise on the supply lines, and consequently, the overall spurious tones and phase noise are vastly reduced.

The time-variant nature of the discrete-time DCO [6] could be exploited to further improve the phase noise performance gap. Applying the discrete-time tuning control words at precise instances within the resonating cycle when the *LC*-tank energy is in the inductor, causes no amplitude perturbation and, consequently, less phase noise due to the AM-to-PM conversion [5].

Advanced CMOS process lithography allows nowadays to create extremely small-sized, but well-controlled, varactors. The switchable capacitance of the finest differential varactor in this 130-nm CMOS process is 38 aF, which corresponds to a frequency step size of 23 kHz at 2.4 GHz [4]. This is still too coarse for wireless applications and requires high-speed $\Sigma\Delta$ dithering to enhance the time-averaged frequency resolution, which is described below.

The digitally controlled quantized capacitance of the *LC* tank is split into three major varactor banks that are sequentially activated during frequency locking. Large 2.3-MHz tuning steps are used during a process–voltage–temperature (PVT) calibration mode. Smaller 460-kHz steps of the acquisition bank of varactors are used during a channel select. The finest 23-kHz steps of the tracking bank (TB) are used during the actual transmit and receive of the data payloads. The unit weighted tracking bank is further partitioned into 64 integer and 8 fractional varactors, with the latter undergoing high-speed $\Sigma\Delta$ dithering for resolution enhancement. The equivalent of $K_{\rm VCO}$ is a DCO gain $K_{\rm DCO} = \Delta f/\Delta{\rm OTW}$, defined as a Δf frequency step per LSB change in the oscillator tuning word (OTW) for each of the varactor banks.

The oscillator is built as an ASIC cell (Fig. 3) with truly digital I/Os, even at the RF frequency of 2.4 GHz, which has rise and fall times faster than 50 ps. The RF signal digitizer is a differential-to-digital converter (with complementary outputs) that transforms the analog oscillator waveform into the zero-crossing digital waveform with a high degree of common-

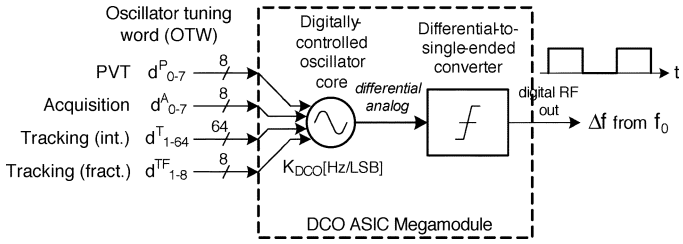

Fig. 3. DCO as an ASIC cell with digital I/Os.

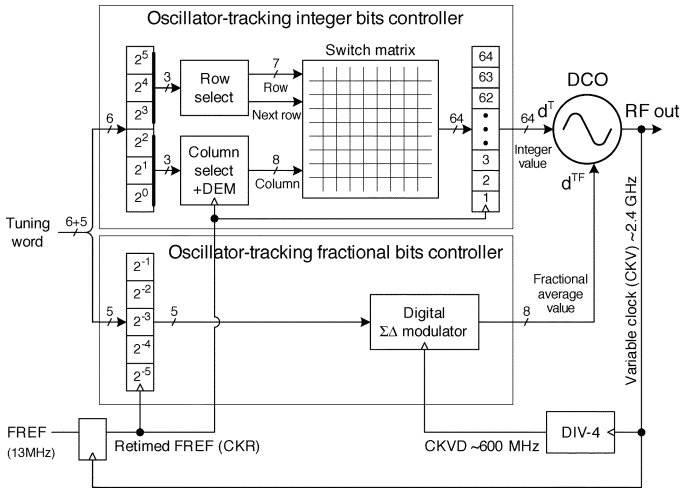

Fig. 4. Block diagram of the DCO tracking bits with DEM of the integer part and $\Sigma\Delta$ dithering of the fractional part. Critical high-speed arithmetic operations are performed in analog domain through capacitative additions inside the DCO.

mode rejection. The DCO serves as a digital-to-frequency converter (DFC). The digital circuitry is built around it to correct its phase/frequency drift in the negative feedback manner.

A. DCO Interface to Digital Logic

Fig. 4 illustrates a mechanism that improves the DCO frequency resolution beyond the basic 23-kHz frequency step of the TB varactors. The eleven fixed-point tuning word bits are split into six integer and five fractional bits. The least significant bit (LSB) of the integer part corresponds to the basic frequency step of the DCO. The integer part is thermometer encoded to control the same-size DCO varactors. This guarantees monotonicity and excellent linearity. The switch matrix, together with the row and column select logic, operates as a binary-to-unit-weighted encoder in response to the integer part of the TB word. The TB linearity is further improved with the dynamic element matching (DEM) that performs rotation of the row varactors.

The fractional part, on the other hand, employs time-averaged dithering that produces a high-rate integer stream whose average value equals the lower rate fractional input. The resulting spurious tones are randomized and pushed to high frequencies with the second or third order of the $\Sigma\Delta$ modulator. The high-rate 600-MHz modulator clock shapes the $\Sigma\Delta$ quantization energy into the out-of-band high-frequency offsets where it is easily filtered out by circuit parasitics. Consequently, the oscillator phase noise degradation is almost immeasurable [4]. With five fractional bits, the effective open-loop DCO resolution is now $23\ \text{kHz}/2^5 = 718$ Hz, which is sufficient for Bluetooth and GSM applications.

The fractional path of the DCO tracking bits is entirely separated from the lower-rate integer part and has a dedicated DCO input just to avoid "contaminating" the rest of the tracking bits with frequent transitions. The $\Sigma\Delta$ modulator is responsive to only the fractional part of the tracking tuning word. The actual merging of both parts is performed inside the oscillator through time-averaged capacitance summation at the *LC* tank.

The PVT and acquisition bank varactors have separate, but much simpler, interface hardware, since it is activated during the frequency settling and is inactive during the subsequent normal operation.

III. All-Digital PLL (ADPLL)-Based Transmitter

Fig. 5 shows the proposed RF transmitter based on an all-digital phase-locked loop (ADPLL) frequency synthesizer with a digital direct frequency modulation capability. It uses digital design and circuit techniques from the ground up. At the heart lies a DCO which deliberately avoids any analog tuning voltage controls. This allows for its loop control circuitry to be implemented in a fully digital manner as suggested in [5].

The DCO produces at its output a single-bit digital variable clock (CKV) in the RF frequency band. In the feedforward path, the CKV clock toggles an array of NMOS transistor switches constituting a near-class-E digitally-controlled RF power amplifier (DPA) that is followed by a matching network, and then terminated with an antenna. In the feedback path, the CKV clock is used for phase detection and reference retiming.

The channel and data frequency control words are in the frequency command word (FCW) format, defined as the fractional frequency division ratio N with a fine frequency resolution limited only by the FCW wordlength. With 16 fractional FCW bits, the frequency granularity is $13\ \text{MHz}/2^{16} = 198$ Hz, using a 13-MHz reference frequency, which is commonly used in GSM mobile phones.

The frequency reference (FREF) clock contains the only reference timing information for the RF frequency synthesizer to which phase and frequency of the RF output are to be synchronized. The desired RF output frequency f_V is related to the reference frequency f_R according to $f_V = N \cdot f_R$, where $N \equiv \text{FCW}$.

A. Synchronous Phase-Domain Operation

The ADPLL operates in a digitally synchronous fixed-point phase domain [1]. The variable phase $R_V[i]$ is determined by counting the number of rising clock transitions of the DCO oscillator clock CKV. The reference phase $R_R[k]$ is obtained by accumulating FCW with every cycle of the retimed frequency reference (FREF) clock input. The sampled variable phase $R_V[k]$ is subtracted from the reference phase in a synchronous arithmetic phase detector. The digital phase error $\phi_E[k]$ is filtered by a digital loop filter and then normalized by the DCO gain K_{DCO} in order to correct the DCO phase/frequency in a negative feedback manner with the loop dynamics that are independent from variations in the manufacturing process, in the supply voltage and in the operating temperature. The

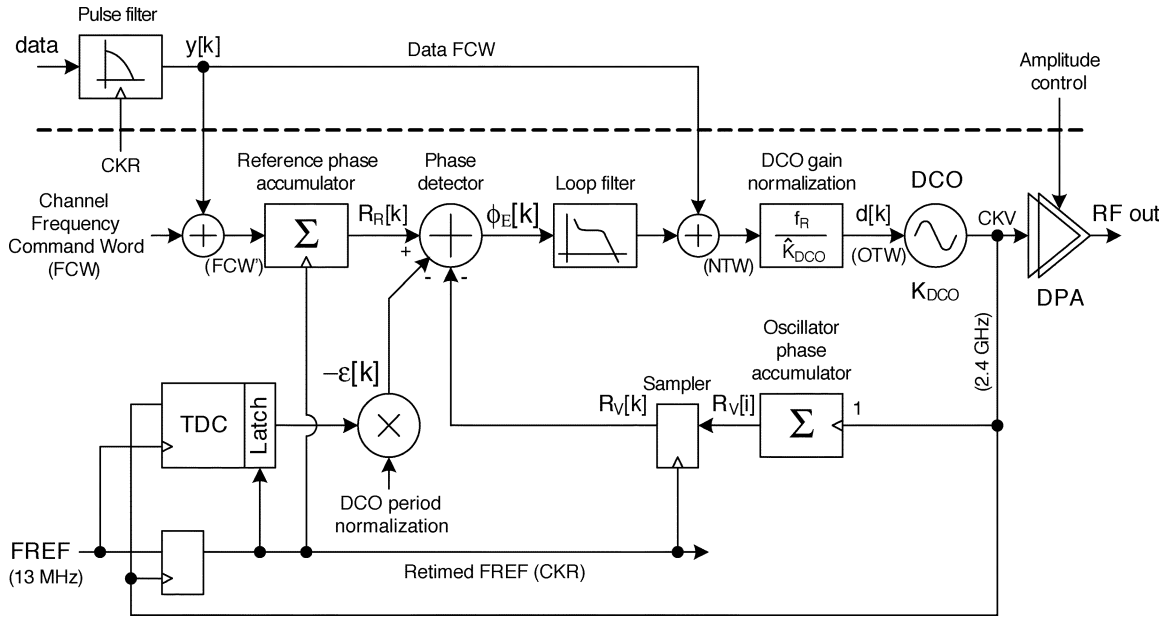

Fig. 5. Synchronous phase-domain all-digital PLL-based transmitter. Only the DCO tracking bank varactors are shown. The PVT and acquisition bank varactors have their own normalizing multipliers, which are inactive during the normal operation.

FREF retiming quantization error $\varepsilon[k]$ is determined by the time-to-digital converter (TDC) and the DCO period normalization multiplier. The TDC is built as a simple array of inverter-delay elements and flip-flops, which produces a time conversion resolution finer than 40 ps in this 130-nm process.

It must be recognized that the two clock domains, FREF and DCO, are not entirely synchronous and it is difficult to physically compare the two digital phase values without metastability problems. During the frequency acquisition interval of the ADPLL's operation, their edge relationship is not known and during the phase-lock the edges will exhibit rotation if the fractional FCW is nonzero. Consequently, the digital-word phase comparison is performed in the same clock domain. The synchronous operation is achieved by oversampling the FREF clock by the high-rate DCO clock. The resulting retimed CKR clock is thus stripped of the FREF timing information and is used throughout the system. This ensures that the massive digital logic is clocked after the quiet interval of the phase error detection performed by the TDC.

The primary advantage of keeping the phase information in fixed-point digital numbers is that, after the conversion, it cannot be further corrupted by noise. Consequently, the phase detector could be simply realized as an arithmetic subtractor that performs an exact digital operation. Thus, the number of conversion places is kept at minimum: a single point where the continuously valued clock edge delay is compared in a TDC. It should be emphasized here that it is very advantageous to operate in the phase domain for several reasons. First, the phase detector used is not a conventional correlative multiplier generating reference spurs [7]. Here, an arithmetic subtractor is used and it does not introduce any spurs into the loop. Second, the dynamic range of the phase error could be made arbitrarily wide simply by increasing the wordlength of the phase accumulators. Conventional three-state phase/frequency detectors are typically limited to only $\pm 2\pi$ of the comparison rate. Third, the phase domain operation is a lot more amenable to digital implementations than the conventional approach.

B. Time-To-Digital Converter (TDC)

Due to the DCO edge counting nature, the phase quantization resolution as described above is limited to $\pm 1/2$ of the variable or DCO clock cycle, T_V. For wireless applications, a finer phase resolution is required, which may be achieved *without* forsaking the digitally intensive approach. The whole-clock-domain quantization error ε is corrected by means of a fractional error correction circuit which is based on a TDC. The TDC measures the fractional delay difference between the reference clock and the next rising edge of the DCO clock, as shown in Fig. 6. Its resolution is a single inverter delay, Δt_{inv}, which in this deep-submicron CMOS process is considered the most stable logic-level regenerative delay and is shorter than 40 ps. This allows the implementation of a GSM-quality phase detection mechanism, as evidenced by the excellent close-in and rms phase noise measurement results presented in Section V. While other TDC architectures [8] can achieve the TDC resolution that is better than one inverter delay, they are quite complex and analog intensive and are not needed for Bluetooth and GSM applications in this CMOS process where $\Delta t_{\text{inv}} \leq 40$ ps is achieved.

The TDC operates by passing the DCO clock through a chain of inverters (Fig. 7). The delayed clock replica vector is then sampled by the FREF clock using an array of registers whose outputs form a pseudo-thermometer code. The decoded binary TDC output is normalized by the DCO clock period T_V before feeding it to the loop. The timing is shown in Fig. 8. The combination of the arithmetic phase detector and the TDC serves as a replacement for the conventional phase/frequency detector. The number of TDC taps, $L = 24$, was determined by the count of inverters needed to cover the full DCO period under the strong process corner $(\min \Delta t_{\text{inv}} = 25$ ps) plus some margin.

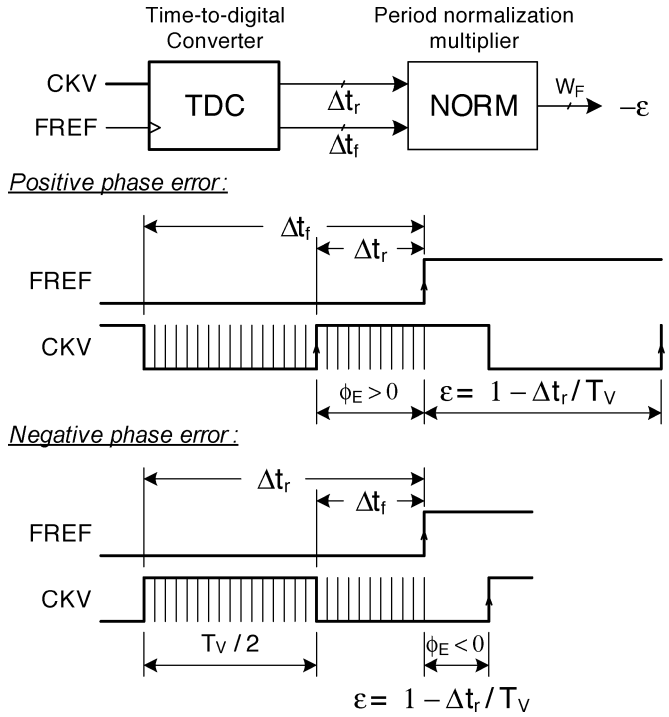

Fig. 6. Fractional phase error estimation based on a TDC. Both positive and negative phase error cases of a classical PLL are shown.

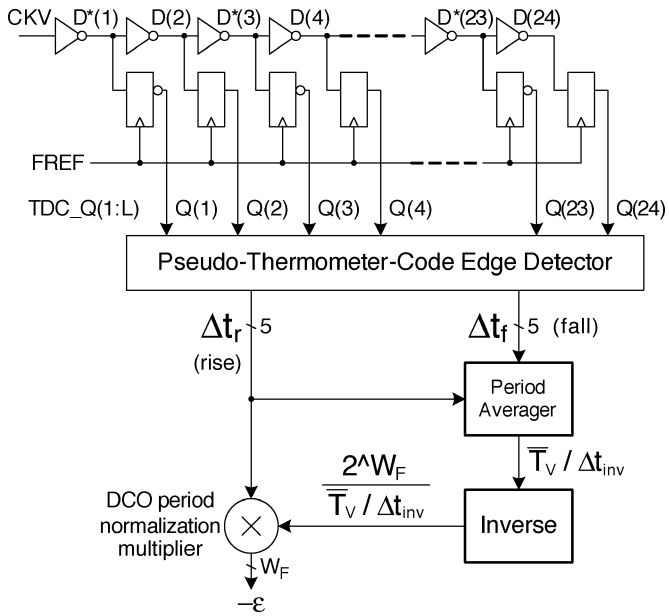

Fig. 7. Fractional error correction based on the TDC.

The normalizing factor $1/\overline{T}_V$ is obtained through longer-term averaging. The averaging time constant could be as slow as the expected drift of the inverter delay, to accommodate for possible temperature and supply voltage variations. The instantaneous value of the clock period $T_V = 2|\Delta t_r - \Delta t_f|$ is an integer, but averaging it would add significant fractional bits with longer operations:

$$\overline{T}_V = \frac{1}{N_{\text{avg}}} \sum_{k=1}^{N_{\text{avg}}} T_V[k]. \tag{1}$$

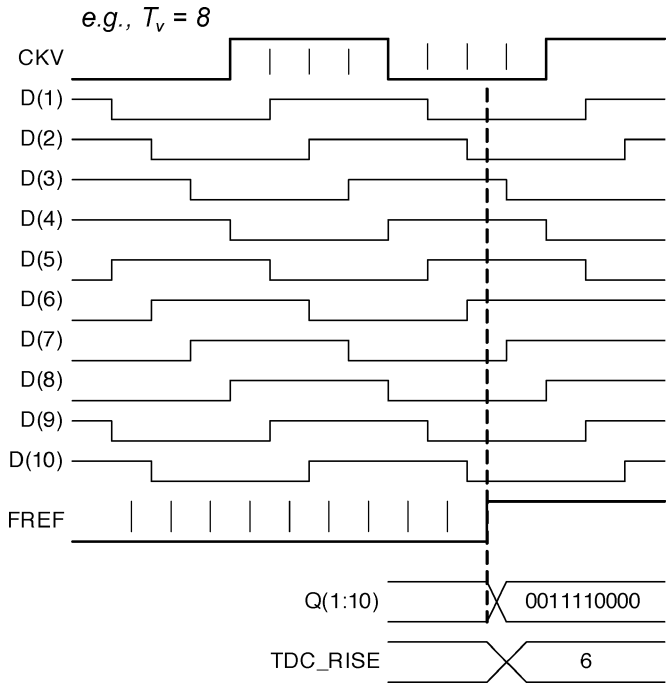

Fig. 8. Timing of the TDC signals.

It was found that accumulating 128 clock cycles would produce accuracy within 1 ps of the inverter delay. The length of the operation is chosen to be a power of 2 since the division by the number of samples N_{avg} could now be replaced with a simple right-shift operation. The calibration of the period normalization is performed at the beginning of every packet and guarantees RF performance over the full PVT extent of the inverter delay in the 25–40-ps range.

The TDC quantization of timing estimation minimally affects the phase noise at the ADPLL output. For the worst-case inverter delay of $\Delta t_{\text{inv}} = 40$ ps at $f_R = 13$ MHz, it produces the in-band phase noise of -86.3 dBc/Hz at the $f_V = 2.4$ GHz RF output, which is adequate not only for Bluetooth but also for cellular applications, such as GSM.

C. Noise and Error Sources

Due to the absence of correlative spurs, as the conventional phase/frequency detector and charge-pump combination is not used, the ADPLL can operate as a type-I first-order loop. However, in order to have an option to filter out the DCO upconverted $1/f$ noise, the loop filter has a capability to add a pole at origin such that a type-II second-order PLL characteristic is achieved [10]. Even though higher PLL orders of this fully digital implementation are possible, it was found that the adequate RF performance is achievable in the simplest type-I first-order configuration.

The ADPLL linear model in the simplest type-I setting, including the phase noise sources, is shown in Fig. 9. $\phi_{n,R}$ is the phase noise of the reference input that is external to the ADPLL. Its closed-loop transfer function is expressed by

$$H_{cl}(s) = \frac{N}{1 + \frac{s}{\alpha \cdot f_R}}. \tag{2}$$

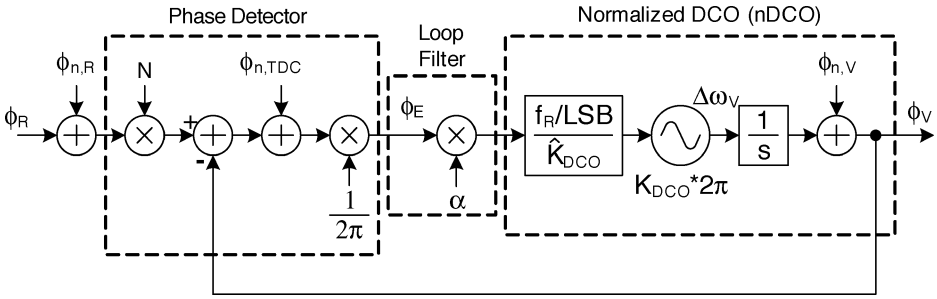

Fig. 9. Linear s-domain model with noise sources added.

From this, we obtain the bandwidth $f_{\rm BW}$ or 3-dB cut-off frequency of the low-pass closed-loop PLL (provided $f_{\rm BW} \ll f_R$ in order for the s-domain approximation to hold) to be $f_{\rm BW} = (\alpha/2\pi) \cdot f_R$.

Internally to the system, there are only two places that the noise could be injected. Due to its digital nature, the rest of the system is immune to any time-domain or amplitude-domain perturbations. The first internal noise source $\phi_{n,V}$ is the oscillator itself, which undergoes high-pass filtering by the loop. Its closed-loop transfer function is

$$H_{cl,V}(s) = \frac{1}{1+H_{ol}} = \frac{1}{1+\frac{\alpha \cdot f_R}{s}}. \tag{3}$$

The above frequency transfer function indicates that the DCO noise has a high-pass characteristic with a bandwidth or 3-dB cut-off frequency of $f_{{\rm BW},V} = (\alpha/2\pi) \cdot f_R$.

The second internal noise source $\phi_{n,{\rm TDC}}$ is the consequence of the TDC operation of calculating ε. Even thought the TDC is a digital circuit, the FREF and CKV inputs are *continuous* in the time domain. The TDC error has several contributors: quantization, nonlinearity, and random thermal effects. It should be noted that the rest of the phase detection mechanism is digital in nature and *does not* contribute any noise. The closed-loop transfer function of the TDC noise can be expressed as

$$H_{cl,{\rm TDC}}(s) = \frac{\alpha \cdot \frac{f_R}{s}}{1+H_{ol}} = \frac{1}{1+\frac{s}{\alpha \cdot f_R}}. \tag{4}$$

The TDC-contributed noise has the same transfer function as the reference noise but without the gain of N. This is simply due to the fact that the TDC phase signal is normalized to the DCO clock cycle.

D. Direct Frequency Modulation

As shown in Fig. 5, the oscillating frequency deviation Δf is dynamically controlled by directly modulating the DCO frequency in a feedforward manner with a closed loop compensation that effectively removes the loop dynamics from the modulating transmit path [9]. However, the rest of the loop, including all error sources, operates under the normal closed-loop regime. This method is similar to the two-point direct modulation scheme [11], but because of the digital nature here, it is exact and does not require any analog component matching, except for the DCO gain $K_{\rm DCO} = \Delta f/\Delta{\rm OTW}$ calibration. The "just-in-time" $K_{\rm DCO}$ calibration is carried out digitally at the beginning of every transmitted packet by forcing the PLL frequency deviation Δf (through digital word $y[k]$ in Fig. 5) and measuring the steady-state change in the oscillator tuning word [9].

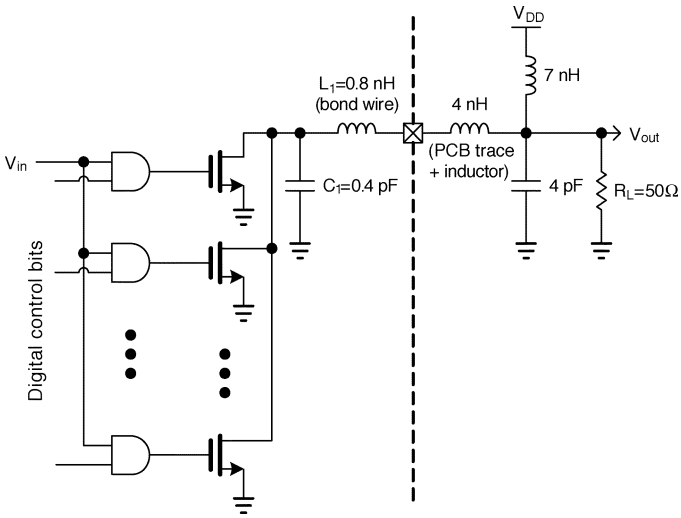

Fig. 10. Near-class-E RF power amplifier with digitally controlled amplitude regulation (half-circuit).

The fixed-point modulating data $y[k]$ (oversampled by and normalized to the reference frequency f_R) directly affects the oscillating frequency. The PLL closed-loop behavior will try to correct this perceived frequency perturbation integrated over the update period of $1/f_R$. This corrective action is compensated by the other (compensating) $y[k]$ feed that is integrated by the reference phase accumulator. If the estimated DCO gain is accurate, then the loop response to $y[k]$ is flat from dc to $f_R/2$.

In contrast to the proposed method, the other popular digitally intensive narrowband frequency modulation schemes are *indirect*, in which they modulate the instantaneous frequency division ratio of a fractional-N PLL, while compensating for the high frequency attenuation of the PLL through boosting the high frequency components of the modulating signal [12]. That architecture, however, requires precise matching between the digital precompensation filter and the analog PLL transfer function across process and temperature variations. The loop filter transfer function is set digitally in [13], but the VCO gain there still requires matching.

E. Digitally Controlled RF Power Amplifier (DPA)

Fig. 10 is a simplified diagram of a near-class-E RF power amplifier whose amplitude (power) is controlled digitally with

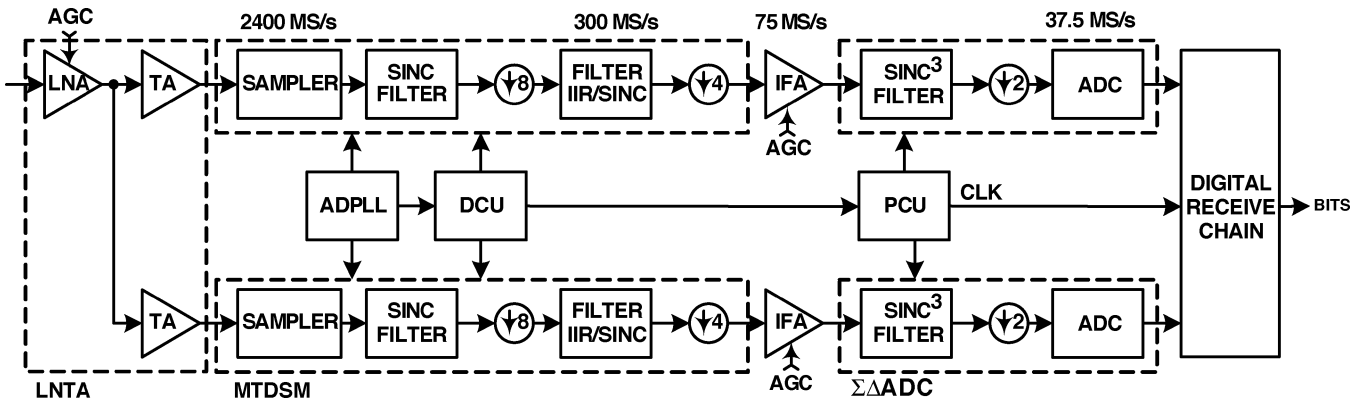

Fig. 11. Block diagram of the receiver.

a 3.5-bit precision by means of binary-weighted transistor switches followed by a matching network. A single transistor switch in a conventional class-E power amplifier is replaced with a multitude of switches. The RF amplitude is digitally controlled by regulating the number of active switches. The structure is pseudo-differential. The various levels of output power that may be produced by this DPA can be used to accommodate for power-control needs, which are typically needed in wireless system, such as Bluetooth transceivers.

IV. Discrete-Time Receiver

The receiver architecture uses direct RF sampling in the receiver front-end path. Discrete-time analog signal processing is used to sample the RF input signal as it is down-converted, down-sampled, filtered and converted from analog to digital with a discrete-time sigma-delta ADC.

While subsampling mixer receiver architectures have been demonstrated in the past, they operate at lower IF frequencies [14], [15] and suffer from noise folding and exhibit susceptibility to clock jitter. This paper demonstrates the first ever *direct RF sampling* receiver that significantly avoids those effects and achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the LO clock frequency and capacitance ratio, both of which are extremely precise in deep-submicron CMOS processes. The discrete-time filtering at each signal processing stage is followed by successive decimation. It should be noted that the successive decimation method has been studied in other fields, such as in disk-drive electronics [16].

The main philosophy in architecting the receive path is to provide all the filtering required by the standard as early as possible using a novel structure that is quite amenable to migration to the more advanced deep-submicron processes. This approach significantly relaxes the design requirements for the following baseband amplifiers. Hence, the ideas implemented in this architecture can be easily extended to meet tougher standards in deep-submicron digital processes.

The receiver architecture is shown in Fig. 11. It comprises a discrete-time front-end and back-end followed by the digital receive chain. The analog front-end (AFE) comprises a continuous-time RF amplification stage followed by a discrete-time sampler and filter. The analog back-end (ABE) comprises a nonsettling IF amplifier followed by a sigma-delta ADC. The digital receive chain filters the quantization noise of the ADC and provides suppression for residual close-in interferer energy.

The local oscillator (LO) is generated by the ADPLL, which is not modulated during reception in a time division duplex (TDD) communication system. All clocks are directly derived from the LO, hence, the most dominant current consumption pulses that are present in the clock distribution circuits occur synchronous to LO. As a result, the coupling to the front-end circuits are either tones at known frequencies or they manifest as dc. The digital control unit (DCU) provides clocks to the AFE while the passive FIR control unit (PCU) provides clocks to the ABE.

A. Analog Front-End

The received signal is amplified in the low-noise amplifier (LNA), split into I/Q paths, and converted into current using a transconductance amplifier (TA). These blocks are designed using conventional RF techniques. Together, they are referred to as a low-noise transconductance amplifier (LNTA), which is the only continuous-time block in the entire transceiver. The LNA has a nominal voltage gain of 20 dB, whereas the TA has a transconductance gain of 7.5 mS. The LNTA output current is differential; it is downconverted to a low IF of 500 kHz and integrated on a differential sampling capacitor at the LO rate (over 2400 MS/s). The positive and negative sides, together, sample the input signal at the Nyquist rate of the RF carrier. A series of decimation and filtering functions follow the RF sampling such that any decimation is preceded by the required anti-aliasing filtering. This operation is performed by a multi-tap direct-sampling mixer (MTDSM), shown in Fig. 12, which decimates the rate to LO/32. A feedback control unit (FCU) controls a current-steering DAC that establishes a proper common-mode bias for the MTDSM while canceling out differential offsets.

The direct RF sampling technique is based on current sampling, which greatly simplifies the mixer circuit design. The effects of the MOS transistor sizing and settling on the mixer performance are not as relevant here as when using voltage sampling techniques. The charge injection and clock feedthrough simply exhibit themselves as a dc offset, which is removed by the feedback path. The signal dependency of the charge sharing is taken care of by periodic hard reset of the rotating capacitors before their engagement with the history capacitors, so this effect is negligible. In the deep-submicron CMOS process, the

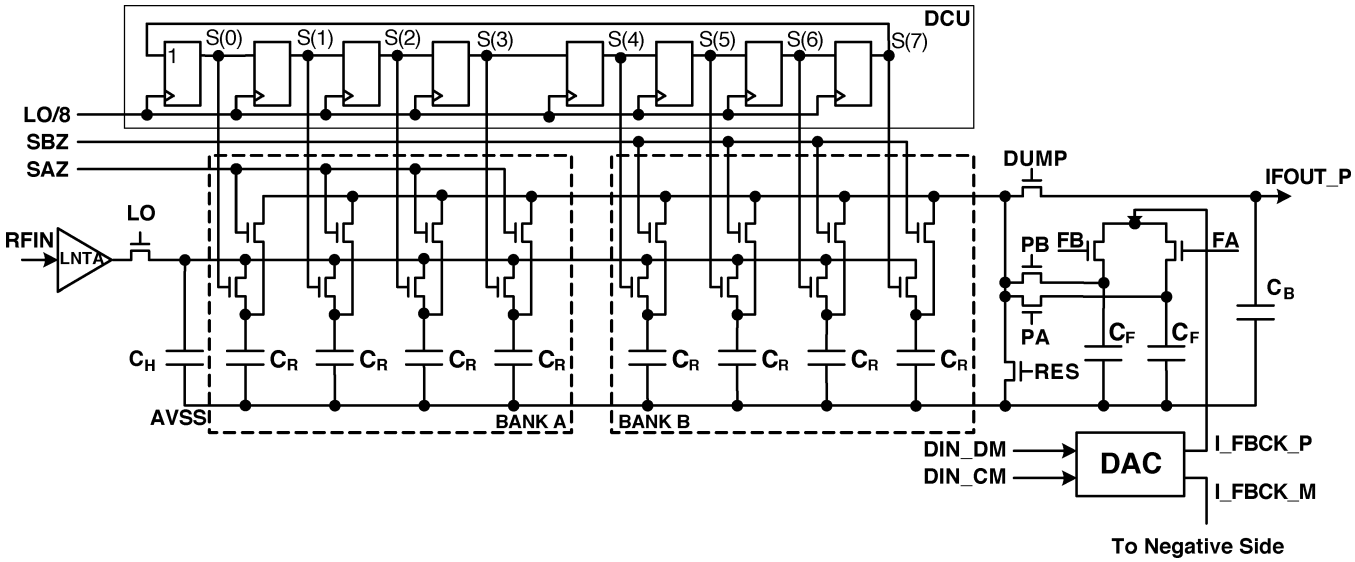

Fig. 12. Multi-tap direct sampling mixer.

clock edge positions are precisely controlled, as discussed in the Introduction. The sole operation that places severe constraints on the clock timing and jitter is the RF current sampling by the local oscillator. The rest of the MTDSM system is operating in the discrete-time domain and the only requirement there is to ensure nonoverlapping of the clock and control signals, but that is quite easy to achieve.

As shown in Fig. 12, the MTDSM comprises switched capacitors that receive timing signals from the DCU that generates clocks for the AFE. The main part of the DCU consists of a shift-register whose outputs are "one-hot" constrained as shown in Fig. 13. Two banks of four rotating capacitors are provided with the purpose of sampling the RF input together with a history capacitor (C_H).

For eight LO cycles, one out of four rotating capacitors in a bank samples the input together with C_H in parallel, while all four capacitors in the second bank are charge shared with the buffer capacitor C_B. The size of each rotating capacitor is a few hundred femtofarads while C_H and C_B are several tens of picofarads.

After the charge sharing is completed, the rotating capacitor bank is reset and precharged to a desired voltage by charge-sharing it with a feedback capacitor (C_F) [17]. During this time, input RF samples are accumulated on the capacitors in the other bank of rotating capacitors. Hence, the LNTA experiences a constant load at its output, which is equal to C_H plus one C_R.

The operation of sampling the input RF signal for eight cycles on $C_H + C_R$ creates a sinc filter with notches located at integer multiples of $2400\ \text{MHz}/8 = 300\ \text{MHz}$, which is the new sampling rate after the first decimation. The notches are located at frequencies where noise would fold back onto the channel of interest located between 0 and 1 MHz. This reduces the effect of noise folding due to decimation to being insignificant. At the same time, when C_R is disconnected from C_H, charge sharing occurs and each capacitor takes away charge proportional to its size. C_H is never discharged and retains a charge in proportion to the ratio $C_H/(C_H+C_R)$ as C_R is separated from it. This creates an IIR filter equation where the pole is ideally determined by the ratio of C_H and C_R. However, the parasitics at the output of LNTA affect this pole and a careful design is required. The DCU timing signals S(0) through S(7) perform the rotation for sampling operation.

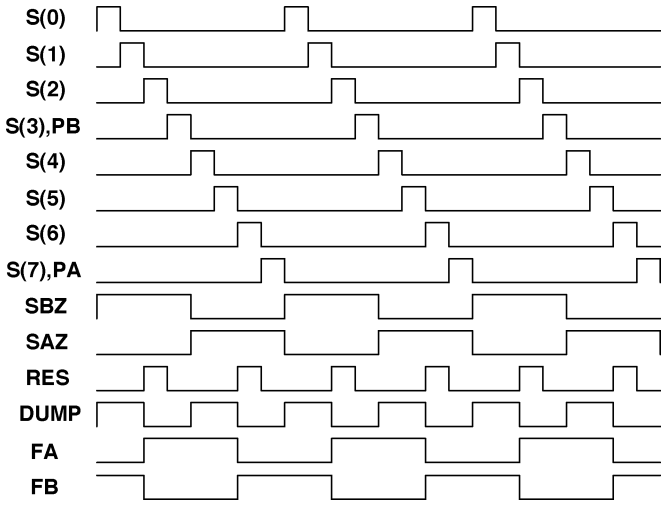

Fig. 13. DCU output signals.

In the readout operation, the four capacitors in a bank are charge-shared with C_B. The top plate of C_B is the readout node. Combining the charge creates an accumulation process, which creates a second sinc filter. The new sampling rate is $300\ \text{MHz}/4 = 75\ \text{MHz}$, hence, noise from frequencies at integer multiples of 75 MHz folds back to the channel of interest. This spatial sinc filter, created by charge combining in a capacitor bank, creates notches that protect the channel of interest from the folded noise. Simultaneously, charge combination of the capacitors in one bank with C_B creates an IIR filter whose corner frequency is determined by the ratio $C_B/(4C_R + C_B)$. The readout operation is facilitated by the DUMP signal from the DCU, while SAZ or SBZ perform the combining of charge in a bank.

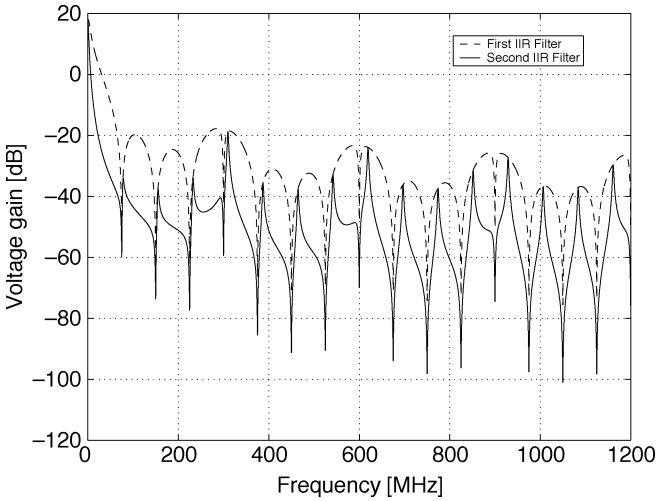

Fig. 14. MTDSM frequency response.

The frequency transfer function of the MTDSM is shown in Fig. 14. The matching circuits in the RF chain provide additional anti-aliasing filtering for far interferers. The noise figure of the MTDSM is dominated by the size of C_R and can be kept low by selecting C_R appropriately. Since all clocks are derived from the LO, this approach does not suffer from any extra degradation from clock jitter since all receivers require a mixer switch driven by an LO. Beyond this RF switch, the clock edge control only goes to the extent of ensuring nonoverlap of clocks and settling of signals.

The precharge of the MTDSM is performed using the feedback circuitry shown in Fig. 12. The DAC output current is steered into a feedback capacitor C_F differentially and places a charge on C_F. After a bank of rotating capacitors is charge-shared with C_B, it is disconnected and discharged using the RES signal from the DCU. Following the reset, it is charge-shared with C_F such that the charge is redistributed according to the ratio $C_F/(4C_R+C_F)$. This creates a first order IIR filter in the feedback path, which, if desired, can be used to reduce the noise fed back by the feedback circuit.

When more current is steered from the positive side of the DAC output to the negative side, less charge flows to the bank on the positive side than the bank on the negative side. Hence, a negative differential offset is created. Any differential offset present in the MTDSM can be cancelled by providing the necessary differential current such that the feedback control unit (FCU) detects no dc offset at the output of a decimating filter following the ADC. The average value of the differential output of the current steering structure is 5-bit programmable and is used to control the common mode of the MTDSM. The common mode is measured using the ADC in the receive chain during a calibration phase after the initial power-up of the device.

B. Analog Back-End

A discrete-time IF amplifier (IFA) provides single-pole filtering in addition to driving the anti-aliasing input stage of the ADC that operates at a rate of LO/64. The IFA is implemented as a nonsettling switched capacitor amplifier with an embedded single-stage IIR filtering running at a rate of LO/32, which was determined by a trade-off analysis of noise aliasing, bandwidth, linearity and power consumption.

The ADC operates at half the rate of the IFA for reduced power consumption. The structure of the ADC, adapted from [18], is shown in Fig. 15. The necessary anti-aliasing filtering is performed using a third-order sinc filter combined with the input stage of the ADC [19]. The sinc filter is implemented using only capacitors and switches. The quantizer has five levels.

The voltage and current references in the bandgap have four bits of programmability allowing a voltage reference accuracy of 1% and current reference accuracy of 5% without any off-chip components.

C. Digital Receive Chain

The digital receive chain shown in Fig. 16 comprises the necessary anti-aliasing filtering and decimation to lower the data rate to LO/256, which represents an oversampling ratio of about 10 for a 1 Mb/s system. Final filtering is performed using a two-stage low-power compact channel-select FIR filter that uses common sub-expression elimination to reduce the adder count. In the first stage, the output rate of the ADC is lowered to LO/256 by providing anti-aliasing filtering. The second stage removes the residual close-in interferers in addition to the quantization noise of the ADC.

The output of the first filter is used by the FCU to determine if a differential offset exists in the receive chain. The estimated dc is subtracted from the MTDSM by controlling the DAC current, steering it from positive to negative side to remove a positive dc offset and from negative to positive to remove a negative dc offset. Thus, the offsets are removed at the source where they are created by self-mixing. By the very nature of this arrangement, when the dc offset is cancelled, the common mode of both the positive and negative side is returned to the total current output of the DAC. Hence, the MTDSM common mode is returned to the correct value when the dc offset is removed by the feedback loop. This value is adjustable by the second input of the DAC shown in Fig. 12 as DAC_CM.

Next, the low-IF signal is digitally down-converted to zero-IF and the signal amplitude is used to estimate the received signal strength (RSS) that controls the AGC. The AGC output feeds back to the AFE and ABE where the gains of amplifiers are digitally controlled.

The digital GFSK detector performs the ArcTAN operation $(\text{phase} = \text{ArcTAN}(Q/I)$ to extract the phase of the received signal from which the transmitted data is to be subsequently recovered. An IF normalizer (IFN) unit compensates for drifts, frequency offsets and provides fine adjustments of dc offset and signal gain that are necessary to minimize the performance degradation of the demodulator. Since the sampling rate in the receive chain is related to the LO, it is frequency-channel dependent and, therefore, the digital baseband (DBB) processor was designed to be adaptable to the channel-dependent rate variations. This contrasts traditional receiver architectures in which the sampling and processing rates are fixed, independent of the frequency channel of interest. An advantage of this scheme is that it allows the use of a low-jitter clock on analog sampling blocks while the complexity of dealing with the variable sampling rate may be easily accommodated by the digital circuitry

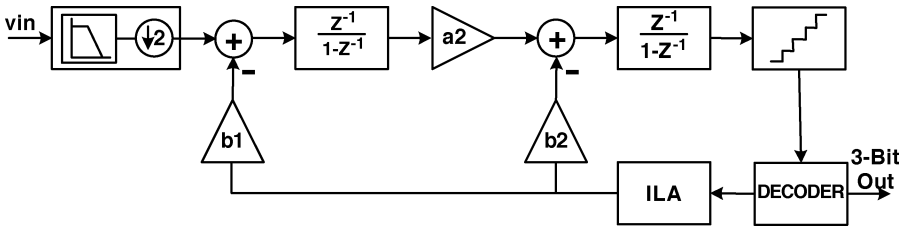

Fig. 15. $\Sigma\Delta$ ADC.

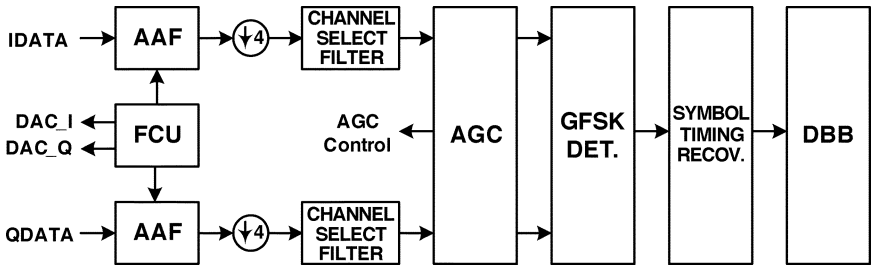

Fig. 16. Digital receive chain.

that follows. The DBB implements the various layers of the Bluetooth protocol up to the HCI, such that a truly full-system solution for Bluetooth communications is provided on a single CMOS die.

V. Experimental Results

Fig. 17 shows a microphotograph of the complete 10 mm^2 single-chip Bluetooth radio. It is fabricated in a 130-nm digital CMOS process with copper interconnects, 1.5-V transistors, 0.35-μm minimum metal pitch, 2.9-nm gate oxide thickness, and with no extra masks.

The transmitter part is located in the lower-right corner and consists of the DCO and near-class-E digitally-controlled RF power amplifier (DPA), which are designed as RF/analog blocks, and ADPLL-based frequency synthesizer and the digital circuitry for TX modulation, which are designed using fully digital flow techniques. The receiver front-end consists of the LNTA, the MTDSM, and the high-speed $\Sigma\Delta$ ADC and DAC.

The current consumption during transmission is 25 mA for the radio portion at 1.5-V supply, 13-MHz FREF clock and 2.5-dBm RF output power, plus 3 mA consumed by the DBB. The receiver typically consumes 36 mA at the supply voltage of 1.575 V plus about 4 mA consumed by the DBB. The external supply to the chip can be varied from 1.75 to 3.6 V since the chip incorporates the necessary regulation circuitry. Built-in sophisticated power management mechanisms ensure minimization of the operation duty cycle of the various consumers for maximized battery life in portable applications. The DCO was designed for phase noise performance of -110 dBc/Hz at 500-kHz offset from the 2.4-GHz carrier frequency at a current consumption cost of only 2 mA at 1.5-V supply. This level of phase noise sufficiently exceeds the necessary levels derived from the radio performance requirements in the Bluetooth specifications (e.g., adjacent channel interference performance).

The close-in synthesizer phase noise is measured at -86.2 dBc/Hz at 10-kHz offset (Fig. 18) and is dominated by the TDC quantization phase noise. The integrated rms phase noise is 0.9° and it appears adequate even for GSM applications (GSM spec: $\leq 5°$). The measured TX spectrum

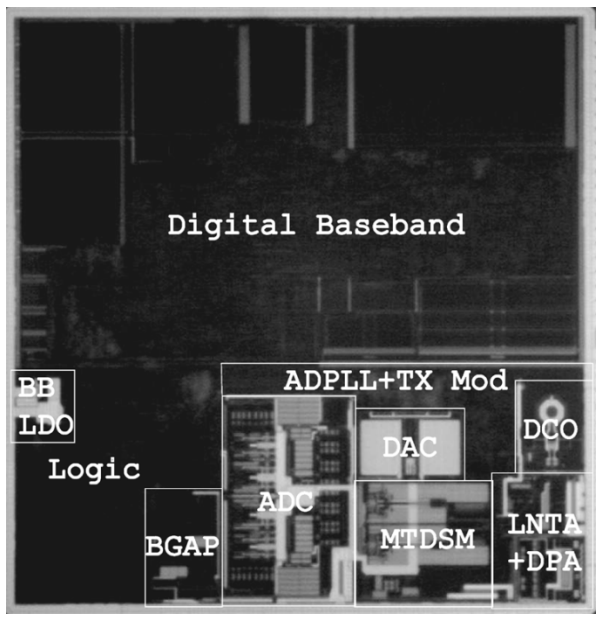

Fig. 17. Die microphotograph of the single-chip Bluetooth radio.

and eye diagram in Fig. 19 show a significant margin over the Bluetooth specifications. The RF spectrum is very close to the instrumentation-quality Rohde&Schwarz Bluetooth internal source. The close-in spurious tones are below -62 dBc and the far-out spurious tones are below -80 dBc. Settling time is ≤ 50 μs and includes the "just-in-time" DCO gain calibration.

The measured typical receiver sensitivity is -83 dBm, which exceeds the Bluetooth specification by 13 dB. The receiver front-end IIP3 is -15 dBm and the 1-dB compression is at -5 dBm. The measured maximum received signal is -5 dBm, exceeding the specifications by 15 dB, and the typical co-channel C/I is 10 dB. The performance numbers reported are typical and can be improved by increasing the current supply to certain blocks.

The feasibility of the presented discrete-time RX architecture is demonstrated in Table I, which shows the resulting performance of the radio in comparison to earlier published works

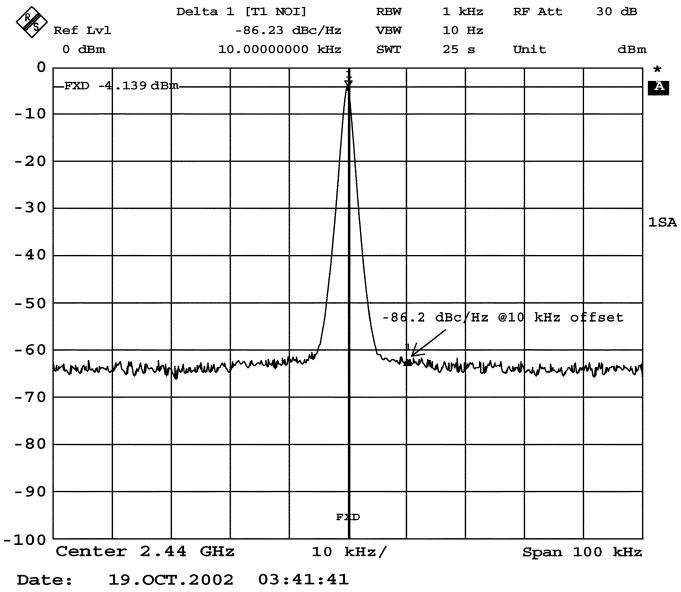

Fig. 18. Close-in spectrum of an unmodulated RF carrier at 2440 MHz.

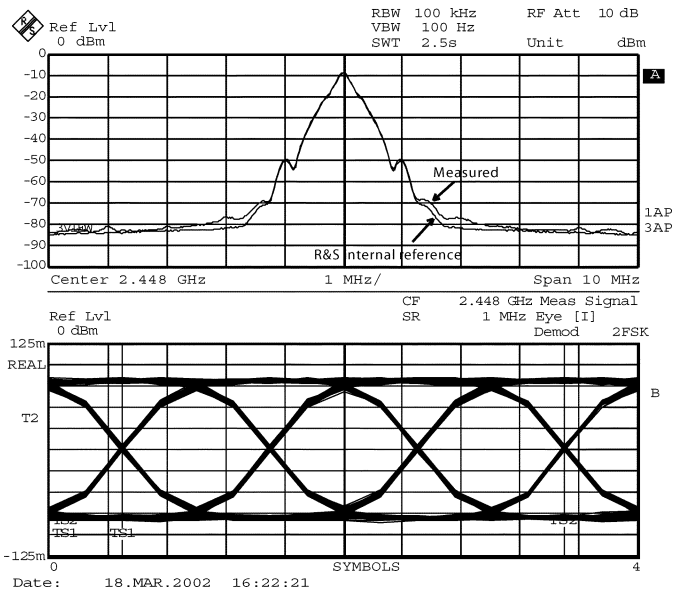

Fig. 19. Measured Bluetooth TX spectrum and eye diagram using Rohde&Schwarz FSIQ-7 signal analyzer.

[20]–[23] using continuous-time architectures. Due to the low supply voltage of 1.575 V, the power consumption is very low. It is interesting to notice that this novel architecture has been able to either match or surpass the performance of the other traditional solutions despite the reduced voltage headroom and discrete-time architecture. This chip has passed the official Bluetooth qualification tests and is in mass production.

This paper demonstrates that a digitally intensive architecture based on extensive use of discrete-time analog and digital signal processing techniques can lead to transceiver performance that competes with that of the traditional continuous-time counterparts. Further, it demonstrates the need for developing solutions where one can more than compensate the weaknesses of digital CMOS processes for traditional core analog circuits

TABLE I
RX PERFORMANCE COMPARISON TO PREVIOUS WORK

Work	Technology	RX Current mA	Sensitivity dBm
This work	0.13 μm, 1.575 V	37	-83
[20]	0.18 μm, 2.5/ 3.0 V	30.5	-78
[21]	0.18 μm, 2.7 V	39	-83
[22]	0.25 μm, ? V	45	$\leq$ -70
[23]	0.25 μm, 2.5 V	$\leq$ 50	-80

by making extensive use of mixed-signal and digital solutions. Many avenues exist for inventing new architectures that rely on the strength of such processes while avoiding their weaknesses. The strength of full integration is that it provides the opportunity to apply digital signal processing solutions to core analog functions and offers most affordable solutions. The weakness is the reduced voltage headroom, reduced drive capability of the transistors, and a process optimized for digital logic. Appropriate architecture selection coupled with judicious use of signal processing techniques level the playing field against the approach where sub-functions of communication systems are individually implemented in those technologies offering the best performance for each of the sub-functions.

VI. CONCLUSION

We have presented a novel transceiver architecture for a single-chip fully compliant Bluetooth radio fabricated in a digital 130-nm CMOS process. The transmitter and receiver architectures are built from the ground up using digital techniques that exploit the high speed and high density of a deep-submicron CMOS process, and its fine lithography and precise capacitor ratios, while avoiding its weaker handling of voltage resolution. The conventional phase/frequency detector and charge-pump combination found in most frequency synthesizers is replaced by a time-to-digital converter (TDC) and is followed by a digital loop filter that controls a digitally controlled oscillator (DCO). Due to the absence of the traditional correlation-based phase detection mechanism, the loop does not contribute to the reference spurs. The measured close-in phase noise of -86 dBc/Hz is adequate even for the more demanding GSM applications. The transmitter architecture is fully digital and takes advantage of the wideband frequency modulation capability of its all-digital PLL. The receiver uses direct RF sampling with discrete-time analog and digital signal processing. It achieves great selectivity right at the mixer level. The selectivity is digitally controlled by the LO clock frequency and the capacitance ratio, both of which are extremely precise in deep-submicron CMOS processes. Application of the presented ideas has resulted in significant area and power savings. They are extendible to other radio standards.

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