Design of a 1-V 3-mW 2.4-GHz Fractional-N PLL Synthesizer in 65nm CMOS

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***Abstract*— A fractional-N PLL synthesizer is designed in 65 nm CMOS general process for Bluetooth low-energy applications. For low-power consumption, the PLL synthesizer is designed in a single 1-V supply. The tuning range of PLL Synthesizer is 1.9-2.7 GHz to cover the ISM band for 1/5-fRF sliding-IF receiver. The simulated VCO phase noises at 1 MHz offset are -110 and -120 dBc/Hz at 2.7 and 1.9 GHz, respectively. With a fast VCO frequency calibration process included, the total lock time of the synthesizer is 12 μs. The synthesizer dissipates 3 mW from 1 V supply voltage.**

Keywords— Fractional-N, PLL, Synthesizer, Bluetooth low-energy

I. INTRODUCTION

Short-range low-data-rate wireless connectivity is an essential technology in IoT applications, and the Bluetooth low energy is considered the most adequate standard for this short-range wireless connectivity applications. Hence, a low-power and low-voltage CMOS RF transceivers and fractional-N PLL synthesizers are highly needed for this purpose. Operating power consumption can be reduced by using a reduced supply. The previous PLLs for the Bluetooth applications showed a typical supply voltage of 1.1 – 1. 4 V [1-3]. Although [4] was designed in 1-V supply, it was a all-digital PLL.

This paper presents a 65nm CMOS design of a fractional-N PLL synthesizer with a reduced supply voltage of 1 V rather than a nominal 1.2 V for low power consumption. Circuit designs and extensive simulation verifications of the synthesizer are described.

II. CIRCUIT DESIGN AND RESULTS

Fig. 1 shows the fractional-N PLL synthesizer architecture. It consists of an LC VCO, charge pump (CP), phase-frequency detector (PFD), loop filter (LPF), the frequency divider, and the 20-bit MASH 1-1-1 delta-sigma modulator (DSM). The output frequency band is determined by assuming that it intend to provide LOs for a sliding-IF receiver with IF=1/5×f_{RF} as well as a polar transmitter. For f_{RF} between 2.4 and 2.5 GHz, the Rx LO requires 1.9 – 2.0 GHz, and Tx LO requires 2.4 – 2.5 GHz, which leads to the combined band of 1.9 – 2.5 GHz.

Fig. 2 shows the schematic of the VCO and buffer amplifier. VCO is designed in a complementary cross-coupled structure, which enhances the negative g_m value at lower current consumption compared to a N/P-FET only cross-coupled structure. The bias current is controlled by using a PFET current source M5, which shows better 1/f noise than NFET current source. The total frequency band from 1.9 – 2.7 GHz, including some margin, is covered by 32 sub-bands by using a 5-bit

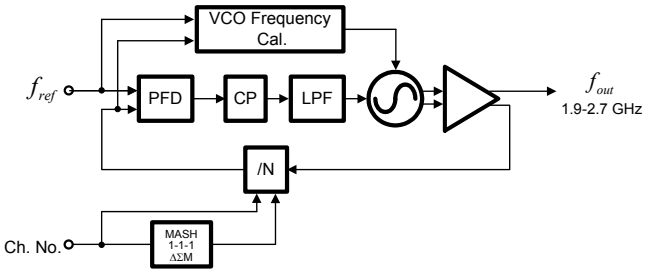

Fig. 1 Fractional-N PLL synthesizer architecture

switched capacitor bank. The tank inductor is 4.9 nH. Since the VCO output signal must be fed to PLL prescaler and Rx mixer, a stable and robust driving buffer of the VCO is needed. As shown in Fig. 2, the buffer is a complementary current-reuse class-AB common-source type. This circuit is suitable for low voltage and low power operation. The output swing and the current consumption are optimized by properly adjusting the gate bias voltages VBP and VBN of the FETs. In typical condition, the VBP and VBN are set to 650 and 350 mV. The VCO consumes 520 μA and the buffer consumes 0.6 μA at 1 V supply.

Fig. 3 shows the charge pump schematic. CP is an essential block to affect the nonlinearity during the conversion process of the input phase difference into a proportional charge amount. Thus, its nonlinearity has a great influence on the entire PLL [5]. In this design, a cascode current source is employed to enhance the output resistance and thus minimize the output current dependence on the output voltage. The differential type design of the current source maintains the tail FET always on and thus reduce the unwanted glitch at the output current. A servo loop feedback network is constructed using an op-amp to enhance the up- and down-current matching. The PFD D-flip-flop is designed in TSPC architecture because TSPC uses only a single-ended single-phase clock and more suitable for low voltage operation compared to the current-mode logic type. The PFD reset time is designed to be tuned between 110 and 220 psec in order to avoid the deadzone and minimize the spur.

Fig. 4 show that VCO tuning range of 1.9 - 2.7 GHz, which sufficiently covers the desired band. Fig. 5 shows that VCO phase noises at 1 MHz offset are -110 dBc at 2.7 GHz and -120 dBc at 1.9 GHz. Fig. 6 shows the lock time simulation results. The lock time simulations are carried out in mixed-mode, in which all digital gates are modeled in Verilog code, the VCO is modeled in analog behavioral code, and the charge pump, PFD, and loop filter are in transistor level. The lock time of the PLL is 12 μs. This lock time includes a fast VCO frequency

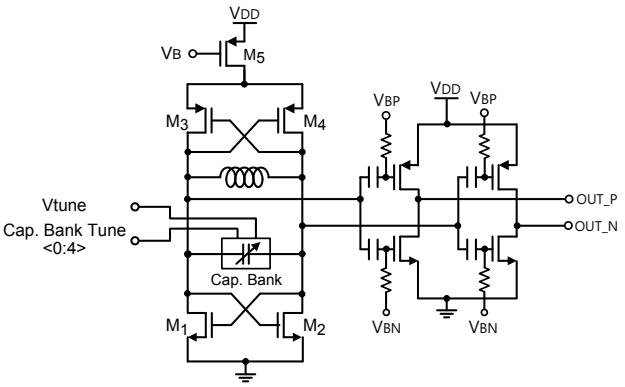

Fig. 2 VCO and buffer

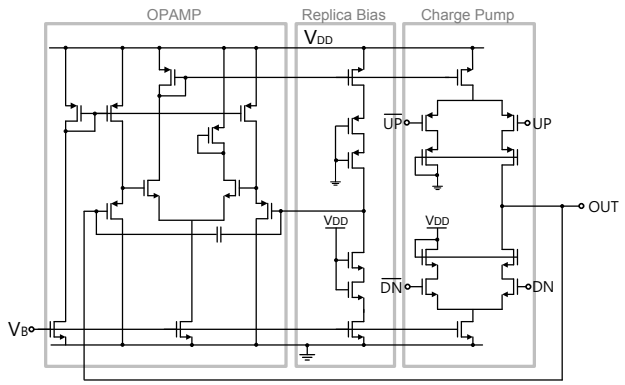

Fig. 3 Charge pump

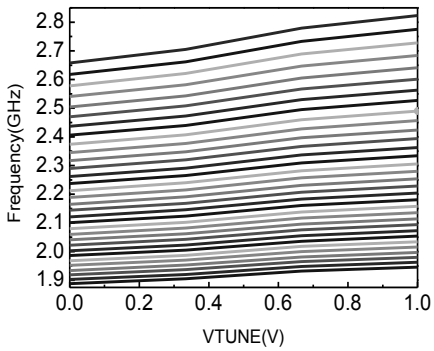

Fig.4 VCO tuning range

calibration process [6] and subsequently the closed-loop locking process. The total power consumption and its breakdown, and the PLL performances are summarized in Fig. 7.

ACKNOWLEDGMENT

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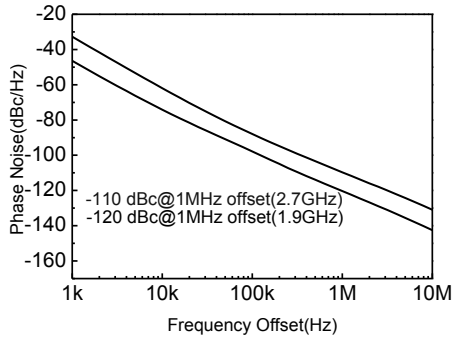
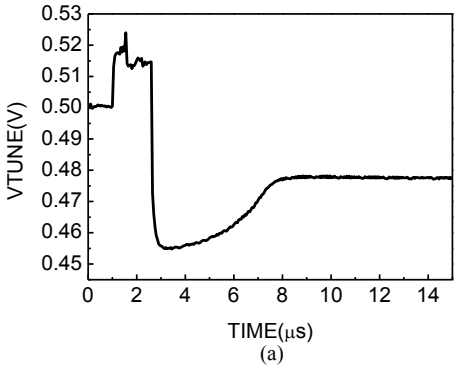


Fig. 5 Phase noises



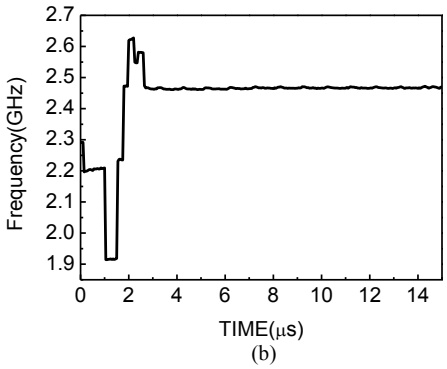
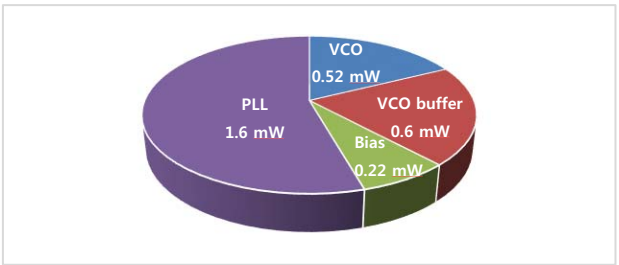


Fig . 6 Mixed-mode closed-loop locking simulation results. (a) Vtune (b) VCO Output Frequency



Total power consumption	Tuning range	Phase noise (2.7GHz)	Locking Time
2.94 mW	1.9-2.7 GHz	-110 dBc @ 1MHz offset	12us

Fig.7 Current Breakdown and Performance Summary

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