Features

- Using external 32.768kHz quartz crystal
- Supports I^2C-Bus's high speed mode (400 kHz)
- Includes time (Hour/Minute/Second) and calendar (Year/Month/Date/Day) counter functions (BCD code)
- Programmable square wave output signal
- Oscillator stop flag
- Low backup current: typ. 400nA at V_{DD}=3.0V and T_A=25℃
- Operating range: 1.7V to 5.5V

Description

The IT8563 serial real-time clock is a low-power clock/calendar with a programmable square-wave output.

Address and data are transferred serially via a 2-wire bidirectional bus. The clock/calendar provides seconds, minutes, hours, day, date, month, and year information. The date at the end of the month is automatically adjusted for months with fewer than 31 days, including corrections for leap year. The clock operates in the 24-hour format indicator.

Table 1 shows the basic functions of IT8563. More details are shown in section: overview of functions.

Ordering Information

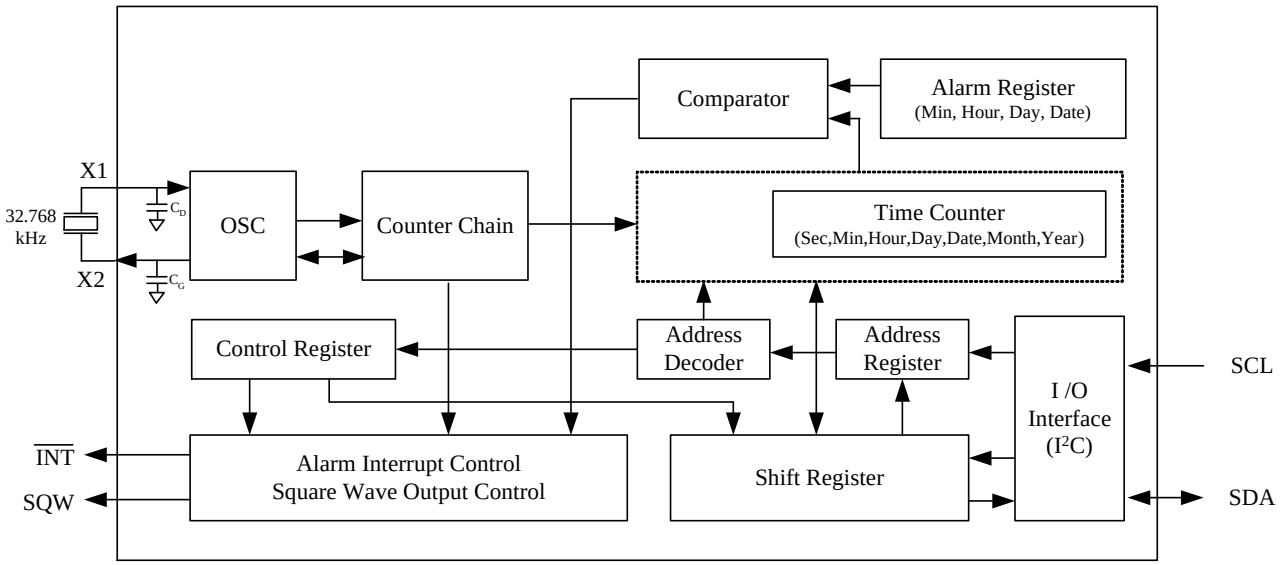
Part Number	Package
IT8563WEX	Lead free and Green 8-Pin SOIC
IT8563UEX	Lead free and Green 8-Pin MSOP
IT8563TEX	Lead free and Green 8-Pin TSSOP

Note---E：Green Package, X: Tape Reel

Table 1. Basic functions of IT8563

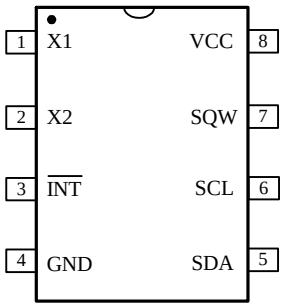
Item	Function			IT8563
1	Oscillator	Source: Crystal: 32.768kHz		√
		Oscillator enable/disable		-
		Oscillator fail detect		√
2	Time	Time display	12-hour	-
			24-hour	√
		Century bit		√
		Time count chain enable/disable		√
3	Interrupt	Alarm interrupt		√
4	Programmable square wave output (Hz)			1, 32, 1.024k, 32.768k
5	Communication	2-wire I^2C bus		√
		Burst mode		-
6	Control	Write protection		-
		External clock test mode		√
		Power-on reset override		√

Function Block



Note: Built in C_D=0, C_G=23pF

Pin Configuration



Pin Description

Pin no.	Pin	Type	Description
1	X1	I	**Oscillator Circuit Input.** Together with X2, 32.768kHz crystal is connected between them.
2	X2	O	**Oscillator Circuit Output.** Together with X1, 32.768kHz crystal is connected between them.
3	$\overline{INT}$	O	**Interrupt Output.** Open drain, active low.
4	GND	P	**Ground.**
5	SDA	I/O	**Serial Data Input/Output.** SDA is the input/output pin for the 2-wire serial interface. The SDA pin is open-drain output and requires an external pull-up resistor.
6	SCL	I	**Serial Clock Input.** SCL is used to synchronize data movement on the I^2C serial interface.
7	SQW	O	**Clock Output.** Open drain. Four frequencies selectable: 32.768k, 1.024k, 32, 1Hz when SQWE bit is set to 1.
8	VCC	P	**Power.**

Function Description

Overview of Functions

1. Clock function

CPU can read or write data including the year (last two digits), month, date, day, hour, minute, and second. Any (two-digit) year that is a multiple of 4 is treated as a leap year and calculated automatically as such until the year 2100.

2. Alarm function

These devices have one alarm system that outputs interrupt signals from INT of IT8563 when the date, day of the week, hour, minute or second correspond to the setting. Each of them may output interrupt signal separately at a specified time. The alarm may be selectable between on and off for matching alarm or repeating alarm.

3. Programmable square wave output

A square wave output enable bit controls square wave output at pin 7. 4 frequencies are selectable: 1, 32, 1.024k, 32.768k Hz.

4. Interface with CPU

Data is read and written via the I^2C bus interface using two signal lines: SCL (clock) and SDA (data).

Since the output of the I/O pin SDA is open drain, a pull-up resistor should be used on the circuit board if the CPU output I/O is also open drain.

The SCL's maximum clock frequency is 400 kHz, which supports the I^2C bus's high-speed mode.

5. Oscillator fail detect

When oscillator fail, OSF bit will be set.

6. Oscillator enable/disable

Only time count chain can be enable or disable by STOP bit.

7. Reset function

The IT8563 includes an internal reset circuit which is active whenever the oscillator is stopped. In the reset state the I^2C-bus logic is initialized and all registers, including the address pointer, are cleared with the exception of bits FE, OSF, TD1, TD0, TESTC and AE which are set to logic 1.

Registers

1. Allocation of registers

Addr. (hex) *1	Function (time range BCD format)	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00	Control/status 1	×	×	×	×	×	×	×	×
01	Control/status 2	×	×	×	×	AF*2	×	AIE*3	×
02	Seconds (00-59)	OSF*4	S40	S20	S10	S8	S4	S2	S1
03	Minutes (00-59)	×	M40	M20	M10	M8	M4	M2	M1
04	Hours (00-23)	×	×	H20	H10	H8	H4	H2	H1
05	Dates (01-31)	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week (00-06)	×	×	×	×	×	W4	W2	W1
07	Months (01-12)	×	×	×	MO10	MO8	MO4	MO2	MO1
08	Years (00-99)	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
09	Alarm: Minutes (00-59)	AE*5	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours (01-12)	AE*5	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates (01-31)	AE*5	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday (00-06)	AE*5	×	×	×	×	W4	W2	W1
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0

Caution points:

*1. IT8563 uses 8 bits for address. For excess 0FH address, IT8563 will not respond.

*2. Alarm interrupt flag bits.

*3. Alarm interrupt enable bits.

*4. Oscillator fail indicates. Indicate clock integrity.

*5. Alarm enable bit. Alarm will be active when related time is matching if AE = 0.

*6. All bits marked with "×" are not implemented.

2. Control and status register

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
00	Control/status 1	×	×	×	×	×	×	×	×
	(default)	0	Undefined	0	Undefined	1	Undefined	Undefined	Undefined
01	Control/status 2	×	×	×	×	AF	×	AIE	×
	(default)	Undefined	Undefined	Undefined	0	Undefined	Undefined	0	0
0D	SQW control	SQWE	×	×	×	×	×	RS1	RS0
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	0	0

a) Alarm Interrupt

- **AIE:** Alarm Interrupt Enable bit.

AIE	Data	Description	
Read / Write	0	Alarm interrupt disabled	Default
	1	Alarm interrupt enabled	

- **AF:** Alarm Flag

AF	Data	Description
Read	0	Alarm flag inactive
	1	Alarm flag active
Write	0	Alarm flag is cleared
	1	Alarm flag remains unchanged

b) SQW control

- **SQWE:** SQW output clock enable bit.

SQWE	Data	Description	
Read / Write	0	the SQW output is inhibited and SQW output is set to high impedance	
	1	the SQW output is activated	Default

- **RS1, RS0:** SQW output frequency select.

RS1, RS0	Data	SQW output freq. (Hz)	
Read / Write	00	32.768k	Default
	01	1.024k	
	10	32	
	11	1	

3. Time Counter

Time digit display (in BCD code):

- Second digits: Range from 00 to 59 and carried to minute digits when incremented from 59 to 00.
- Minute digits: Range from 00 to 59 and carried to hour digits when incremented from 59 to 00.
- Hour digits: See description on the /12, 24 bit. Carried to day and day-of-the-week digits when incremented from 11 p.m. to 12 a.m. or 23 to 00.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
02	Seconds	OSF*1	S40	S20	S10	S8	S4	S2	S1
	(default)	1	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
	(default)	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
04	Hours	×	×	H20	H10	H8	H4	H2	H1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

***1 Note:** Indicate clock integrity. When the bit is 1, the clock integrity is no longer guaranteed and the time need be adjusted.

4. Days of the week Counter

The day counter is a divide-by-7 counter that counts from 00 to 06 and up 06 before starting again from 00. Values that correspond to the day of week are user defined but must be sequential (i.e., if 0 equals Sunday, then 1 equals Monday, and so on). Illogical time and date entries result in undefined operation.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
06	Days of the week	×	×	×	×	×	W4	W2	W1
	(default)	0	0	0	0	0	Undefined	Undefined	Undefined

5. Calendar Counter

The data format is BCD format.

- Day digits: Range from 1 to 31 (for January, March, May, July, August, October and December).
  Range from 1 to 30 (for April, June, September and November).
  Range from 1 to 29 (for February in leap years).
  Range from 1 to 28 (for February in ordinary years).
  Carried to month digits when cycled to 1.
- Month digits: Range from 1 to 12 and carried to year digits when cycled to 1.
- Year digits: Range from 00 to 99 and 00, 04, 08, … , 92 and 96 are counted as leap years.

Addr. (hex)	Description	D7	D6	D5	D4	D3	D2	D1	D0
05	Dates	×	×	D20	D10	D8	D4	D2	D1
	(default)	0	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
07	Months	×	×	×	M10	M8	M4	M2	M1
	(default)	Undefined	0	0	Undefined	Undefined	Undefined	Undefined	Undefined
08	Years	Y80	Y40	Y20	Y10	Y8	Y4	Y2	Y1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined

6. Alarm Register

IT8563: Alarm Register

Addr.	Description	D7	D6	D5	D4	D3	D2	D1	D0
09	Alarm: Minutes	AE*1	M40	M20	M10	M8	M4	M2	M1
	(default)	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0A	Alarm: Hours	AE*2	×	H20	H10	H8	H4	H2	H1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0B	Alarm: Dates	AE*3	×	D20	D10	D8	D4	D2	D1
	(default)	Undefined	0	Undefined	Undefined	Undefined	Undefined	Undefined	Undefined
0C	Alarm: Weekday	AE*4	×	×	×	×	W4	W2	W1
	(default)	Undefined	0	0	0	0	Undefined	Undefined	Undefined

***1** Note: Minute alarm enable bit.

***2** Note: Hour alarm enable bit.

***3** Note: Date alarm enable bit.

***4** Note: Weekday alarm enable bit.

Alarm Function

Related register

	Function	Register definition							
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
01	Control/status 2	×	×	×	×	AF	×	AIE	×
02	Seconds	OSF	S40	S20	S10	S8	S4	S2	S1
03	Minutes	×	M40	M20	M10	M8	M4	M2	M1
04	Hours	×	×	H20	H10	H8	H4	H2	H1
05	Dates	×	×	D20	D10	D8	D4	D2	D1
06	Days of the week	×	×	×	×	×	W4	W2	W1
09	Alarm: Minutes	AE	M40	M20	M10	M8	M4	M2	M1
0A	Alarm: Hours	AE	×	H20	H10	H8	H4	H2	H1
0B	Alarm: Dates	AE	×	D20	D10	D8	D4	D2	D1
0C	Alarm: Weekday	AE	×	×	×	×	W4	W2	W1

When one or more of these registers are loaded with a valid minute, hour, day or weekday and its corresponding bit Alarm Enable (AE) is logic 0, then that information will be compared with the current minute, hour, day and weekday. When all enabled comparisons first match, the Alarm Flag (AF) is set. AF will remain set until cleared by software. Once AF has been cleared it will only be set again when the time increments to match the alarm condition once more. Alarm registers which have their bit AE at logic 1 will be ignored.

Communication

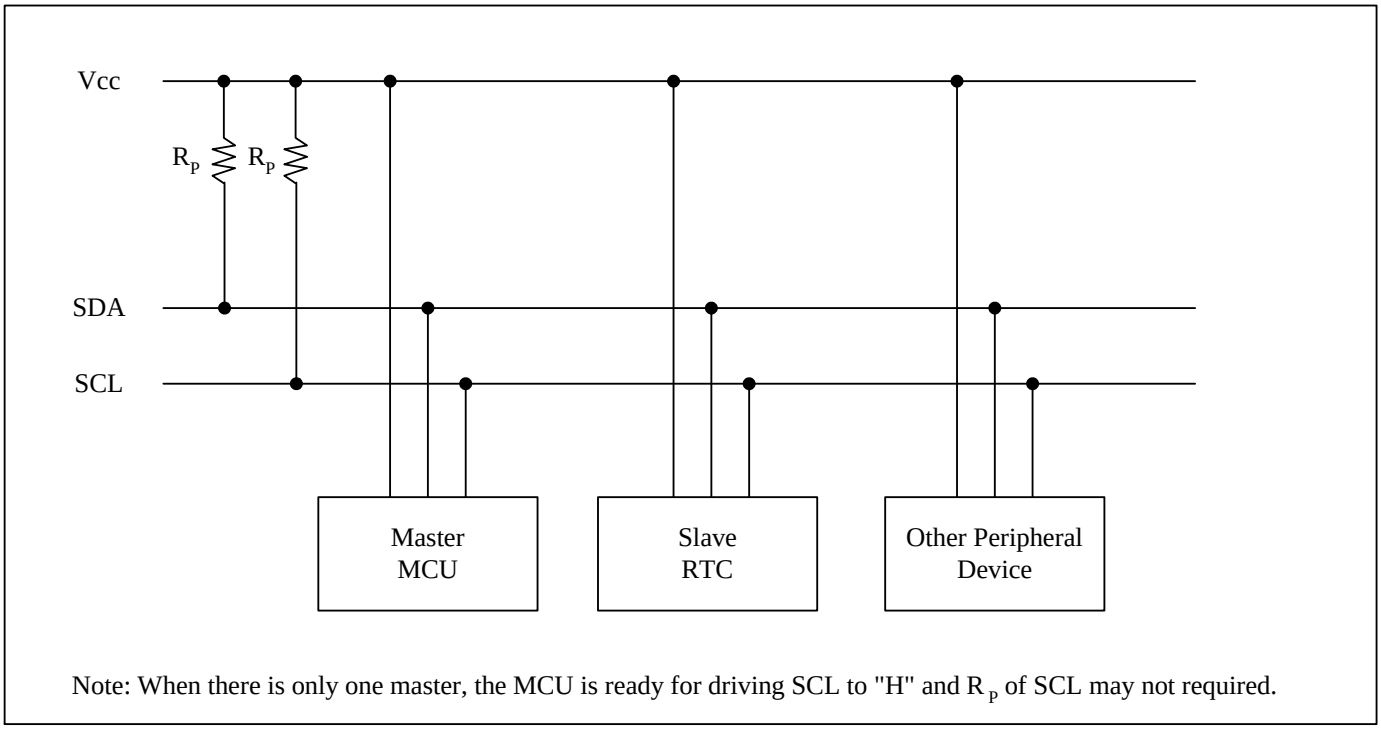
1. I²C Bus Interface

a) Overview of I²C-BUS

The I²C bus supports bi-directional communications via two signal lines: the SDA (data) line and SCL (clock) line. A combination of these two signals is used to transmit and receive communication start/stop signals, data signals, acknowledge signals, and so on. Both the SCL and SDA signals are held at high level whenever communications are not being performed. The starting and stopping of communications is controlled at the rising edge or falling edge of SDA while SCL is at high level. During data transfers, data changes that occur on the SDA line are performed while the SCL line is at low level, and on the receiving side the data is captured while the SCL line is at high level. In either case, the data is transferred via the SCL line at a rate of one bit per clock pulse. The I²C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device and the receiving device responds to communications only when its slave address matches the slave address in the received data.

b) System Configuration

All ports connected to the I²C bus must be either open drain or open collector ports in order to enable AND connections to multiple devices.
SCL and SDA are both connected to the VDD line via a pull-up resistance. Consequently, SCL and SDA are both held at high level when the bus is released (when communication is not being performed).



Note: When there is only one master, the MCU is ready for driving SCL to "H" and R_p of SCL may not required.

Fig.1 System configuration

c) Starting and Stopping I²C Bus Communications

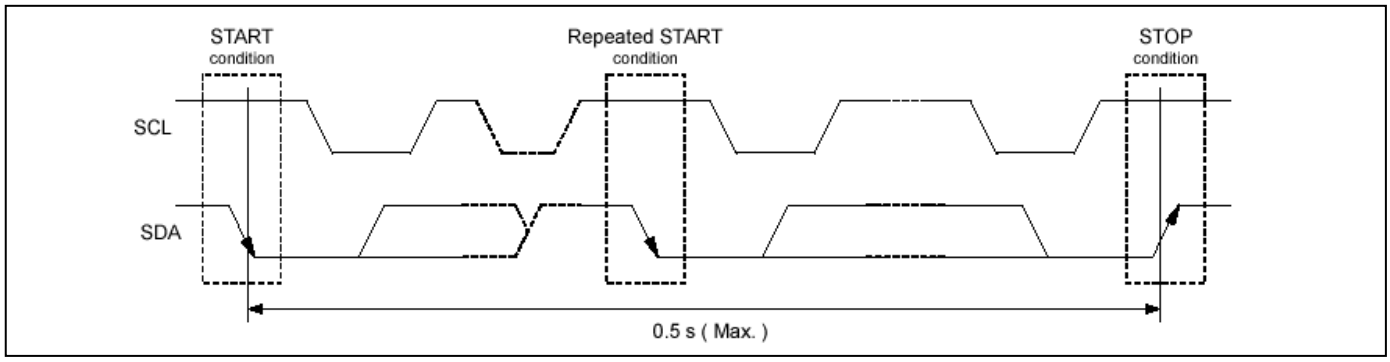


Fig.2 Starting and stopping on I²C bus

START condition, repeated START condition, and STOP condition

- START condition
  SDA level changes from high to low while SCL is at high level
- STOP condition
  SDA level changes from low to high while SCL is at high level
- Repeated START condition (RESTART condition)
  In some cases, the START condition occurs between a previous START condition and the next STOP condition, in which case the second START condition is distinguished as a RESTART condition. Since the required status is the same as for the START condition, the SDA level changes from high to low while SCL is at high level.

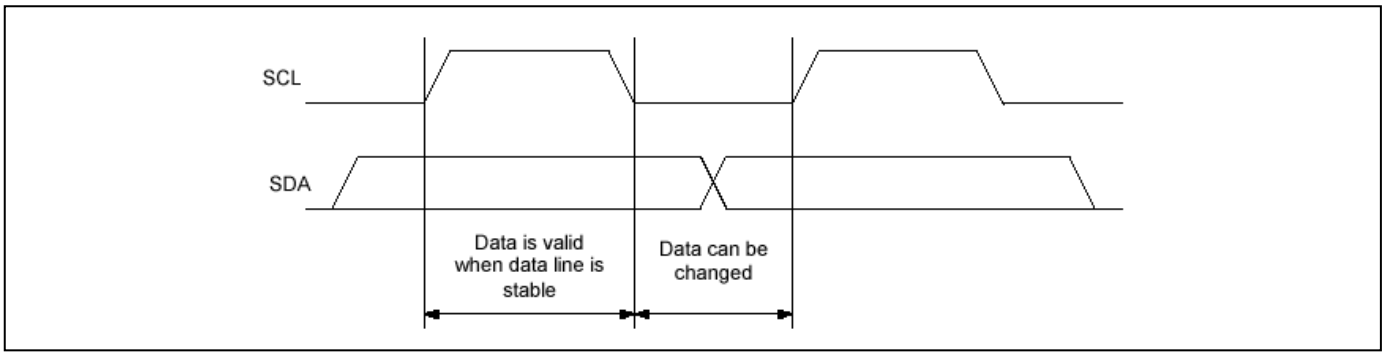
d) Data Transfers and Acknowledge Responses during I²C-BUS Communication

- **Data transfers**

Data transfers are performed in 8-bit (1 byte) units once the START condition has occurred. There is no limit on the amount (bytes) of data that are transferred between the START condition and STOP condition.

The address auto increment function operates during both write and read operations.

Updating of data on the transmitter (transmitting side)'s SDA line is performed while the SCL line is at low level.
The receiver (receiving side) captures data while the SCL line is at high level.

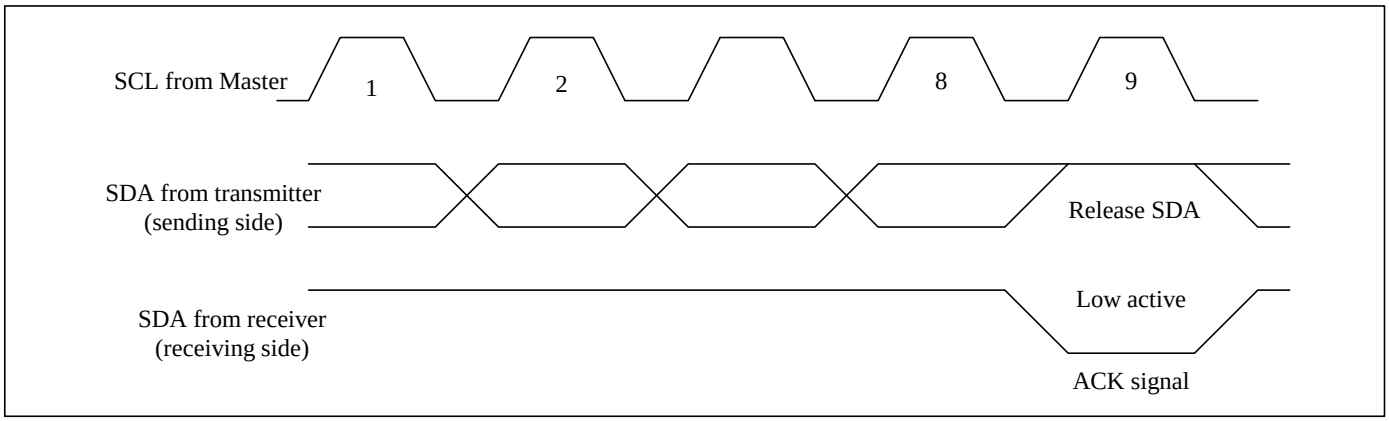


*Note with caution that if the SDA data is changed while the SCL line is at high level, it will be treated as a START, RESTART, or STOP condition.

- **Data acknowledge response (ACK signal)**

When transferring data, the receiver generates a confirmation response (ACK signal, low active) each time an 8-bit data segment is received. If there is no ACK signal from the receiver, it indicates that normal communication has not been established. (This does not include instances where the master device intentionally does not generate an ACK signal.)

Immediately after the falling edge of the clock pulse corresponding to the 8th bit of data on the SCL line, the transmitter releases the SDA line and the receiver sets the SDA line to low (= acknowledge) level.



After transmitting the ACK signal, if the Master remains the receiver for transfer of the next byte, the SDA is released at the falling edge of the clock corresponding to the 9th bit of data on the SCL line. Data transfer resumes when the Master becomes the transmitter.

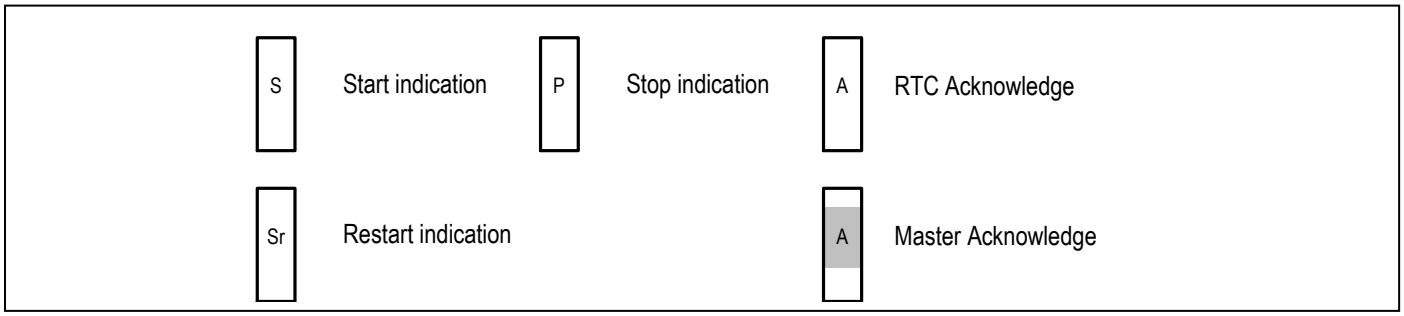
When the Master is the receiver, if the Master does not send an ACK signal in response to the last byte sent from the slave, that indicates to the transmitter that data transfer has ended. At that point, the transmitter continues to release the SDA and awaits a STOP condition from the Master.

e) Slave Address

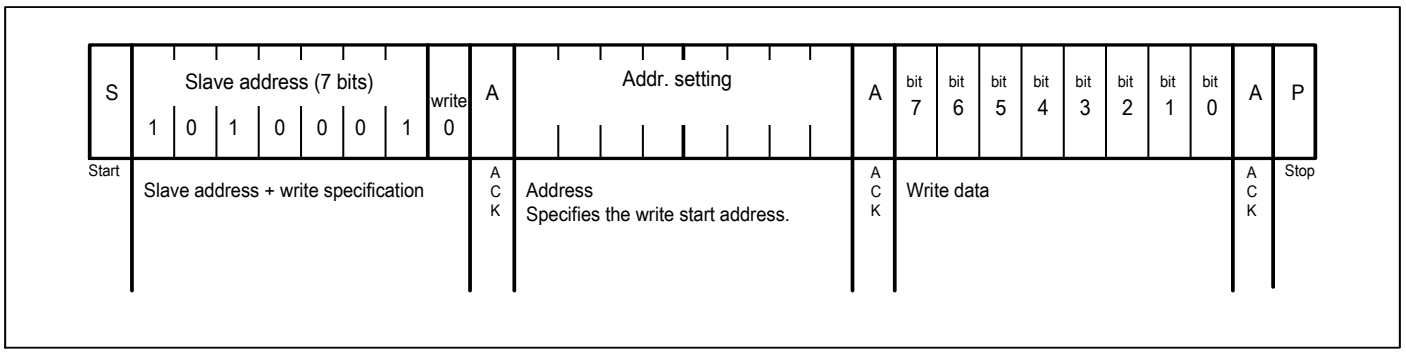
The I^2C bus device does not include a chip select pin such as is found in ordinary logic devices. Instead of using a chip select pin, slave addresses are allocated to each device.
All communications begin with transmitting the [START condition] + [slave address (+ R/$\overline{W}$ specification)]. The receiving device responds to this communication only when the specified slave address it has received matches its own slave address.
Slave addresses have a fixed length of 7 bits. See table for the details.
An R/$\overline{W}$ bit is added to each 7-bit slave address during 8-bit transfers.

Operation	Transfer data	Slave address							R / $\overline{W}$ bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	A3 h	1	0	1	0	0	0	1	1 (= Read)
Write	A2 h								0 (= Write)

2. I^2C Bus's Basic Transfer Format

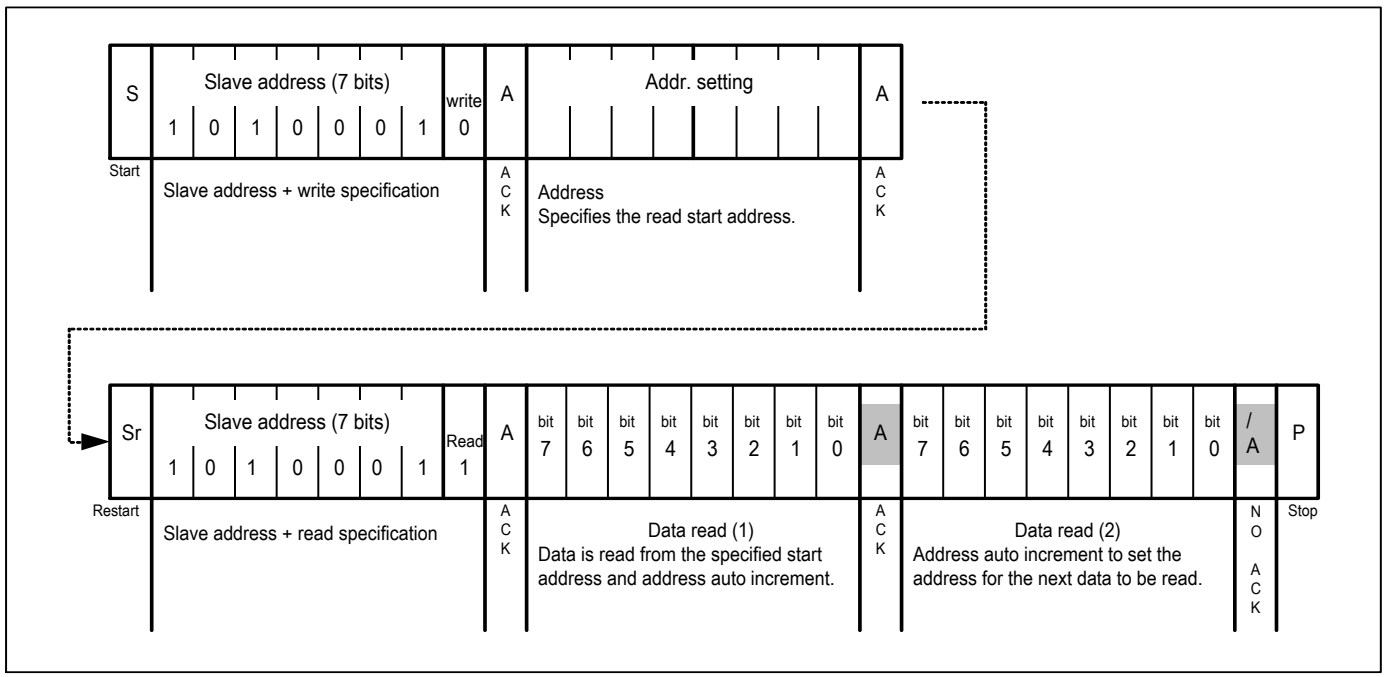


a) Write via I²C bus

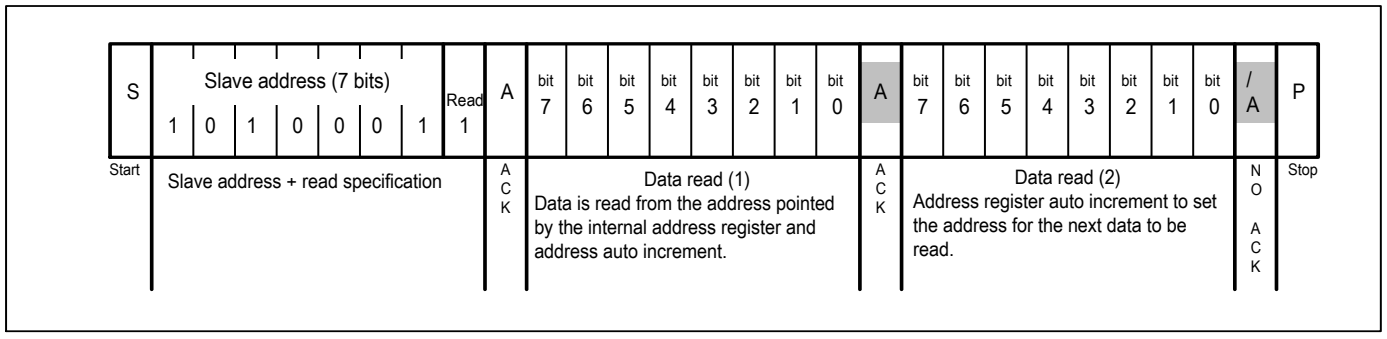


b) Read via I²C bus

- **Standard read**



- **Simplified read**



Note:

1. The above steps are an example of transfers of one or two bytes only. There is no limit to the number of bytes transferred during actual communications.
2. 49H, 4AH are used as test mode address. Customer should not use the addresses.

Maximum Ratings

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND)	-0.3V to +6.5V
DC Input (All Other Inputs except Vcc & GND)	-0.3V to (V_{cc}+0.3V)
DC Output Voltage (SDA, /INTA, /INTB pins)	-0.3V to +6.5V
Power Dissipation	320mW (Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

Symbol	Description	Min	Type	Max	Unit
V_{CC}	Power voltage	1.7	-	5.5	V
V_{IH}	Input high level	0.7 V_{CC}	-	V_{CC}+0.3	
V_{IL}	Input low level	-0.3	-	0.3 V_{CC}	
T_A	Operating temperature	-40	-	85	℃

DC Electrical Characteristics

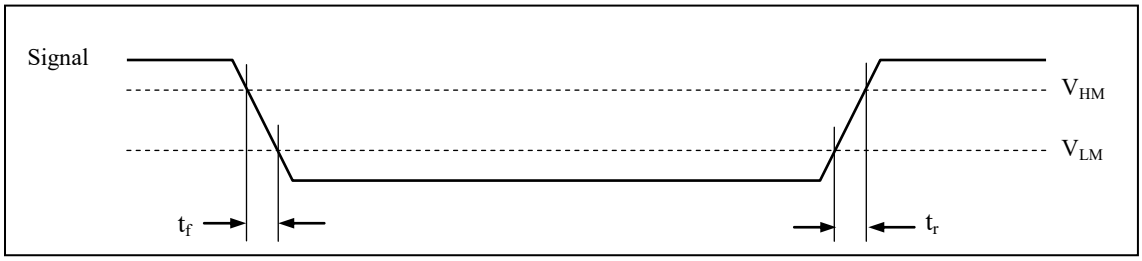
Unless otherwise specified, GND =0V, V_{CC} = 1.7 ~ 5.5 V, T_A = -40 ℃ to +85 ℃, f_{OSC} = 32.768kHz.

Sym.	Description	Pin	Conditions		Min	Typ	Max	Unit
V_{CC}	Supply voltage	V_{CC}	Interface inactive. T_A = 25 ℃ [1]		1.5	-	5.5	V
			Interface active. f_{SCL} = 400kHz [1]		1.7	-	5.5	
	Supply voltage for clock data integrity	V_{CC}	-		1.5	-	5.5	
I_{CC}	Supply current	V_{CC}	Interface active	f_{SCL} = 400kHz	-	-	25	µA
				f_{SCL} = 100kHz	-	-	15	
			Interface inactive (f_{SCL} = 0Hz), pin 7 disabled T_A=-40~85 ℃	V_{CC} = 5.0V	-	450	700	nA
				V_{CC} = 3.0V	-	400	650	
			Interface inactive (f_{SCL} = 0Hz), pin 7 enabled at 32kHz T_A=-40~85 ℃	V_{CC} = 5.0V	-	650	900	nA
				V_{CC} = 3.0V	-	600	850	
V_{IL1}	Low-level input voltage	SCL	-		0	-	0.3V_{CC}	V
V_{IH1}	High-level input voltage	SCL	-		0.7V_{CC}	-	V_{CC}	
I_{OL}	Low-level output voltage	SDA	V_{OL} = 0.4V, V_{CC} = 5V		-3	-	-	mA
		/INT, SQW	V_{OL} = 0.4V, V_{CC} = 5V		-1	-	-	
I_{IL}	Input leakage current	SCL	-		-	-	±1	µA
I_{OZ}	Output current when OFF	-	-		-	-	±1	µA

Note:
1) For reliable oscillator start-up at power-up: $V_{CC(min)power-up}$ = $V_{CC(min)}$ + 0.3 V.

AC Electrical Characteristics

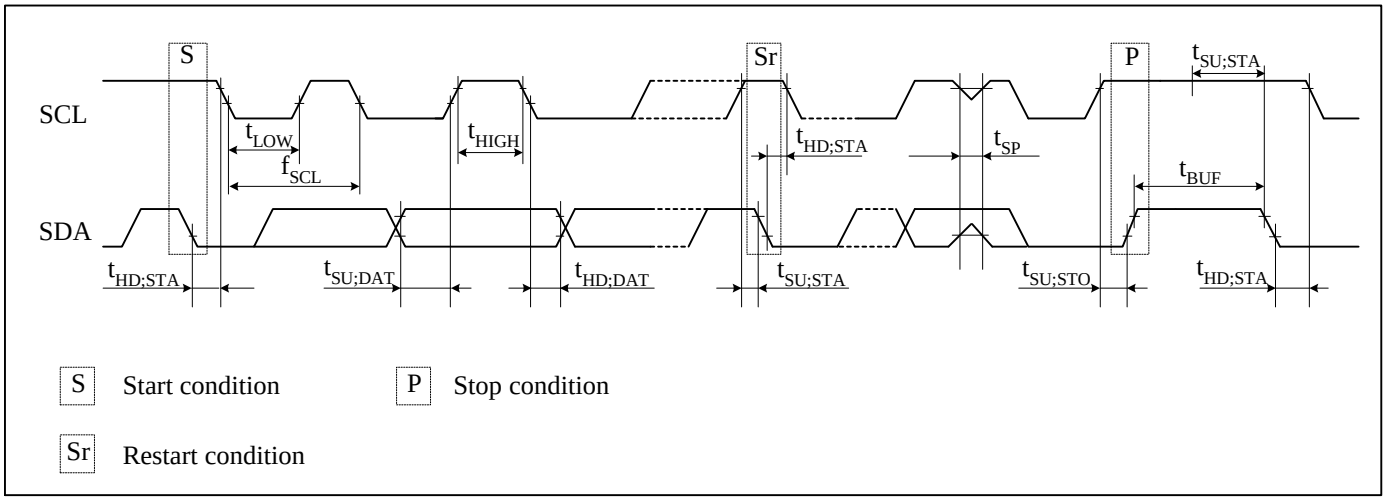
Sym	Description	Value	Unit
V_{HM}	Rising and falling threshold voltage high	0.8 V_{CC}	V
V_{HL}	Rising and falling threshold voltage low	0.2 V_{CC}	V



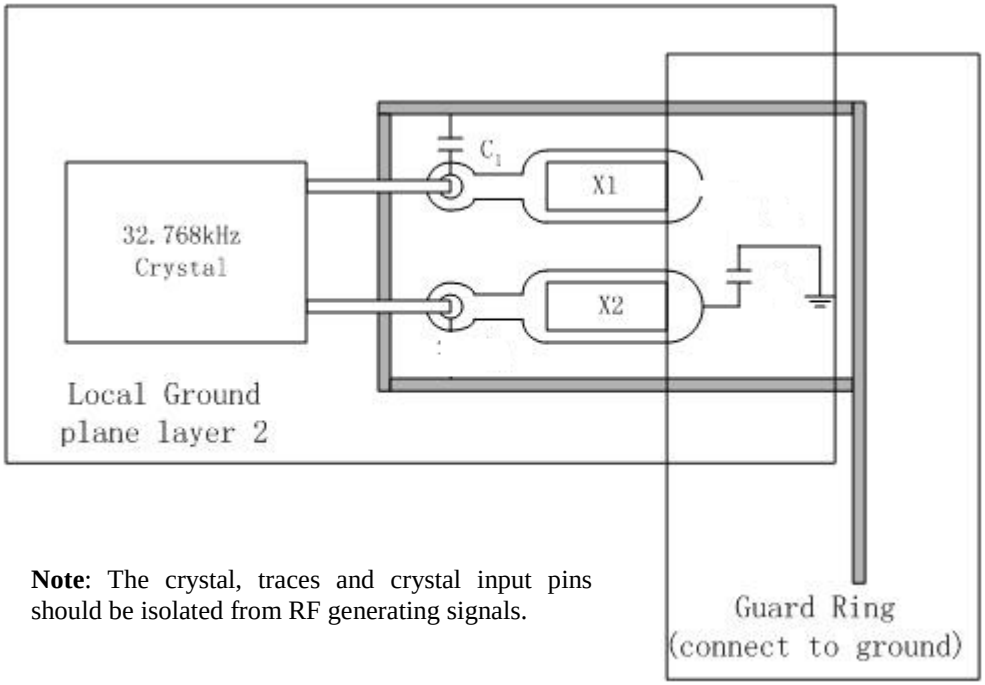
Over the operating range

Symbol	Item	Min.	Typ.	Max.	Unit
f_{SCL}	SCL clock frequency	-	-	400	kHz
$t_{SU;STA}$	START condition set-up time	0.6	-	-	µs
$t_{HD;STA}$	START condition hold time	0.6	-	-	µs
$t_{SU;DAT}$	Data set-up time (RTC read/write)	200	-	-	ns
$t_{HD;DAT1}$	Data hold time (RTC write)	35	-	-	ns
$t_{HD;DAT2}$	Data hold time (RTC read)	0	-	-	µs
$t_{SU;STO}$	STOP condition setup time	0.6	-	-	µs
t_{BUF}	Bus idle time between a START and STOP condition	1.3	-	-	µs
t_{LOW}	When SCL = "L"	1.3	-	-	µs
t_{HIGH}	When SCL = "H"	0.6	-	-	µs
t_r	Rise time for SCL and SDA	-	-	0.3	µs
t_f	Fall time for SCL and SDA	-	-	0.3	µs
t_{SP}*	Allowable spike time on bus	-	-	50	ns
C_B	Capacitance load for each bus line	-	-	400	pF

*** Note:** Only reference for design.



Recommended Layout for Crystal



Note: The crystal, traces and crystal input pins should be isolated from RF generating signals.

Built-in Capacitors Specifications and Recommended External Capacitors

Parameter		Symbol	Typ	Unit
Build-in capacitors	X1 to GND	C_D	0	pF
	X2 to GND	C_G	23	pF
Recommended External capacitors for crystal C_L=12.5pF	X1 to GND	C_1	22	pF
	X2 to GND	C_2	0	pF
Recommended External capacitors for crystal C_L=6pF	X1 to GND	C_1	7	pF
	X2 to GND	C_2	0	pF

Note: The frequency of crystal can be optimized by external capacitor C_1 and C_2, for frequency=32.768Hz, C_1 and C_2 should meet the equation as below:

$Cpar + [(C_1+C_G)*(C_2+C_D)]/ [(C_1+C_G)+(C_2+C_D)] = C_L$

Cpar is all parasitical capacitor between X1 and X2.

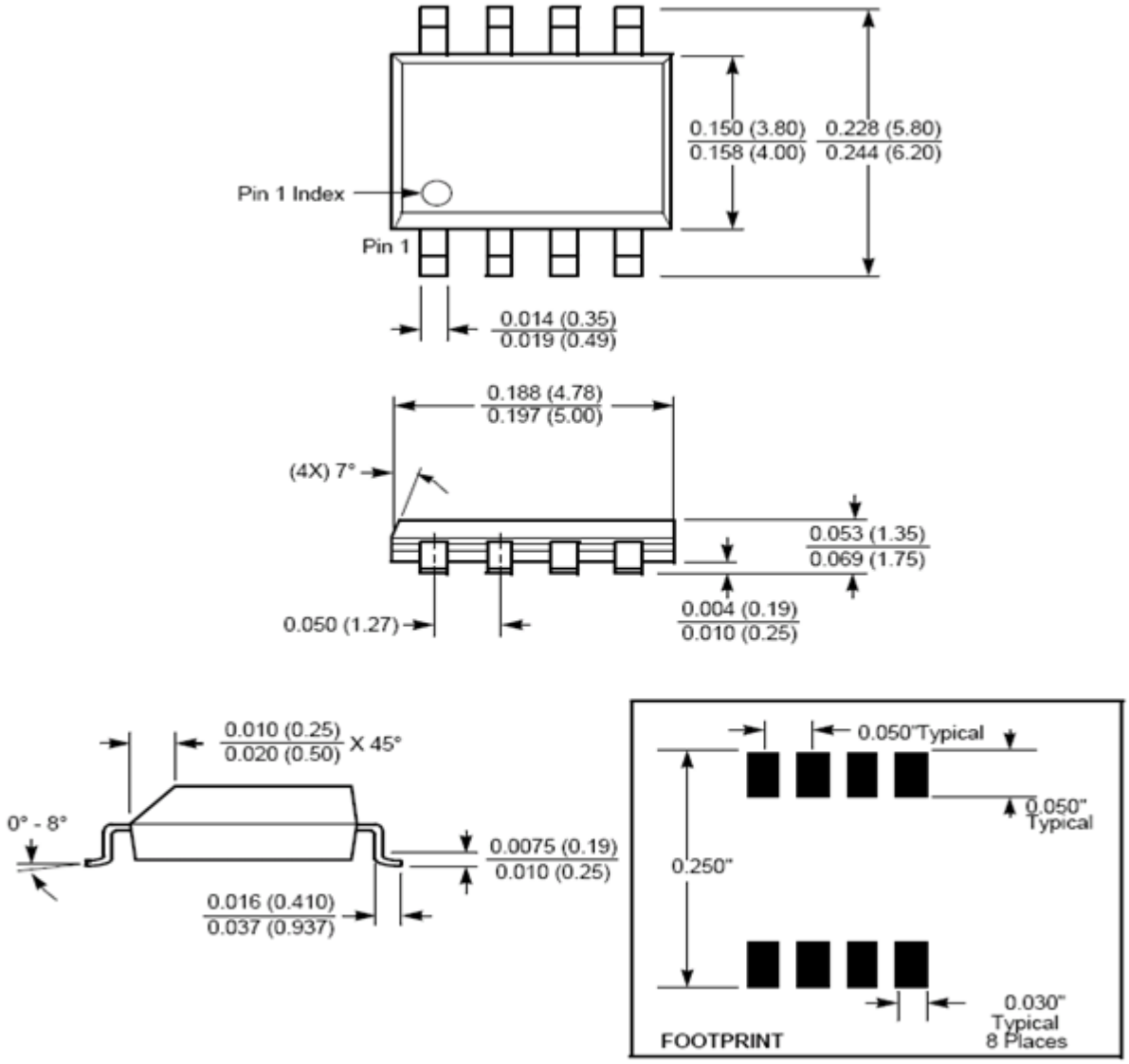
C_L is crystal's load capacitance.

Crystal Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Nominal Frequency	f_O	-	32.768	-	kHz
Series Resistance	ESR	-	-	70	kΩ
Load Capacitance	C_L	-	6/12.5	-	pF

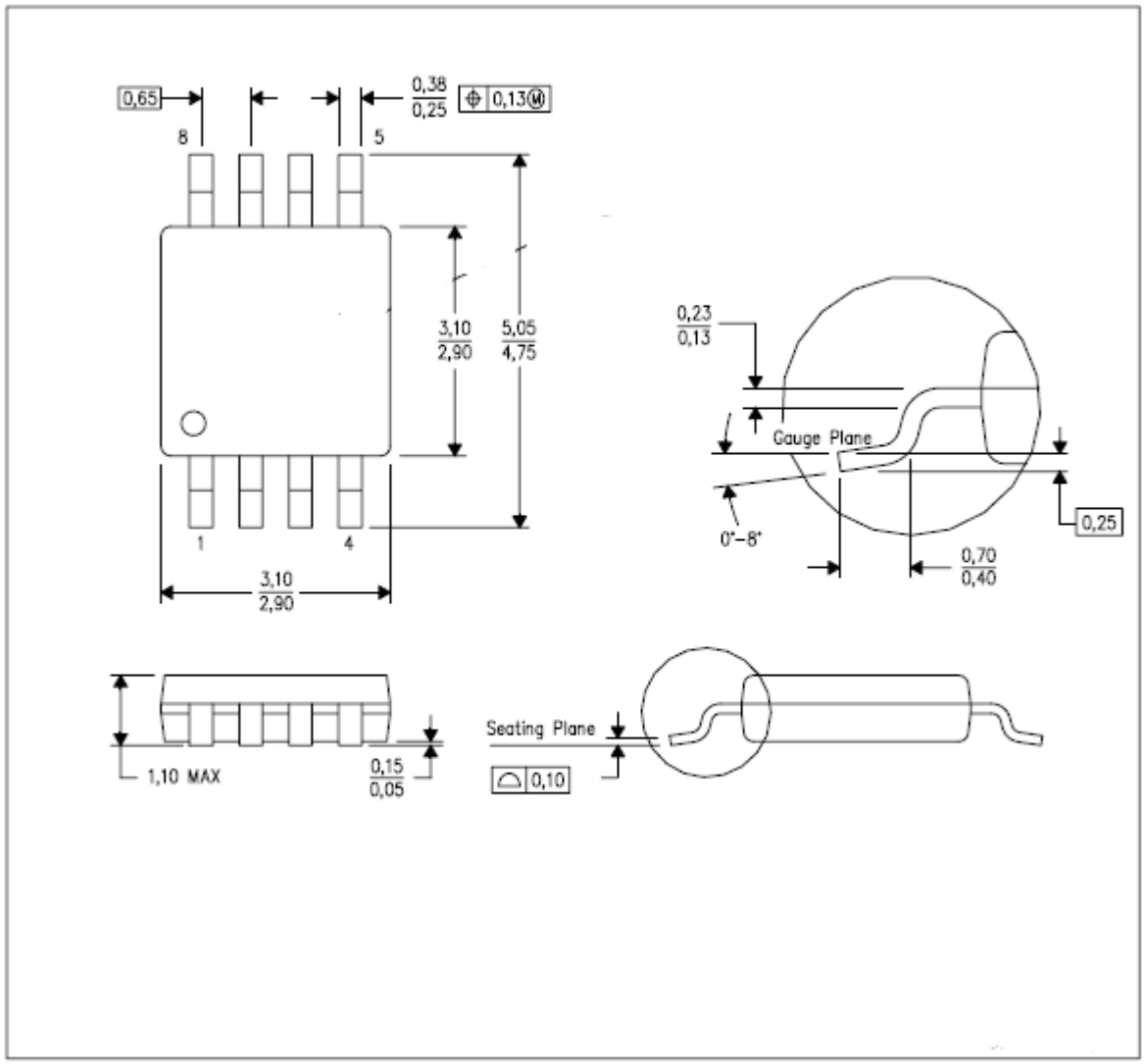
Mechanical Information

WE (Lead free SOP8)

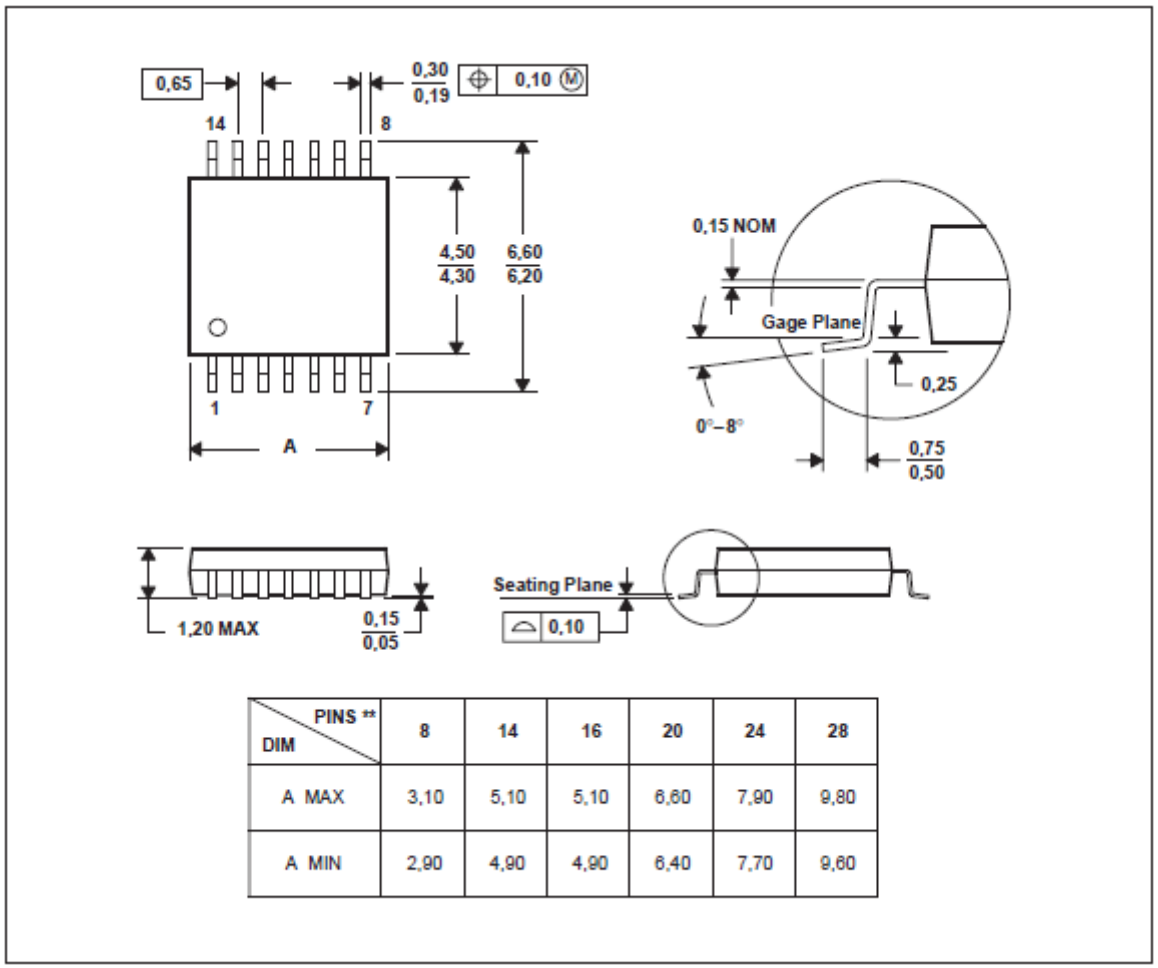


NOTE: All dimensions in inches (in parentheses in millimeters).

UE (Lead free and Green MSOP-8)



TE (Lead free and Green TSSOP-8)



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60