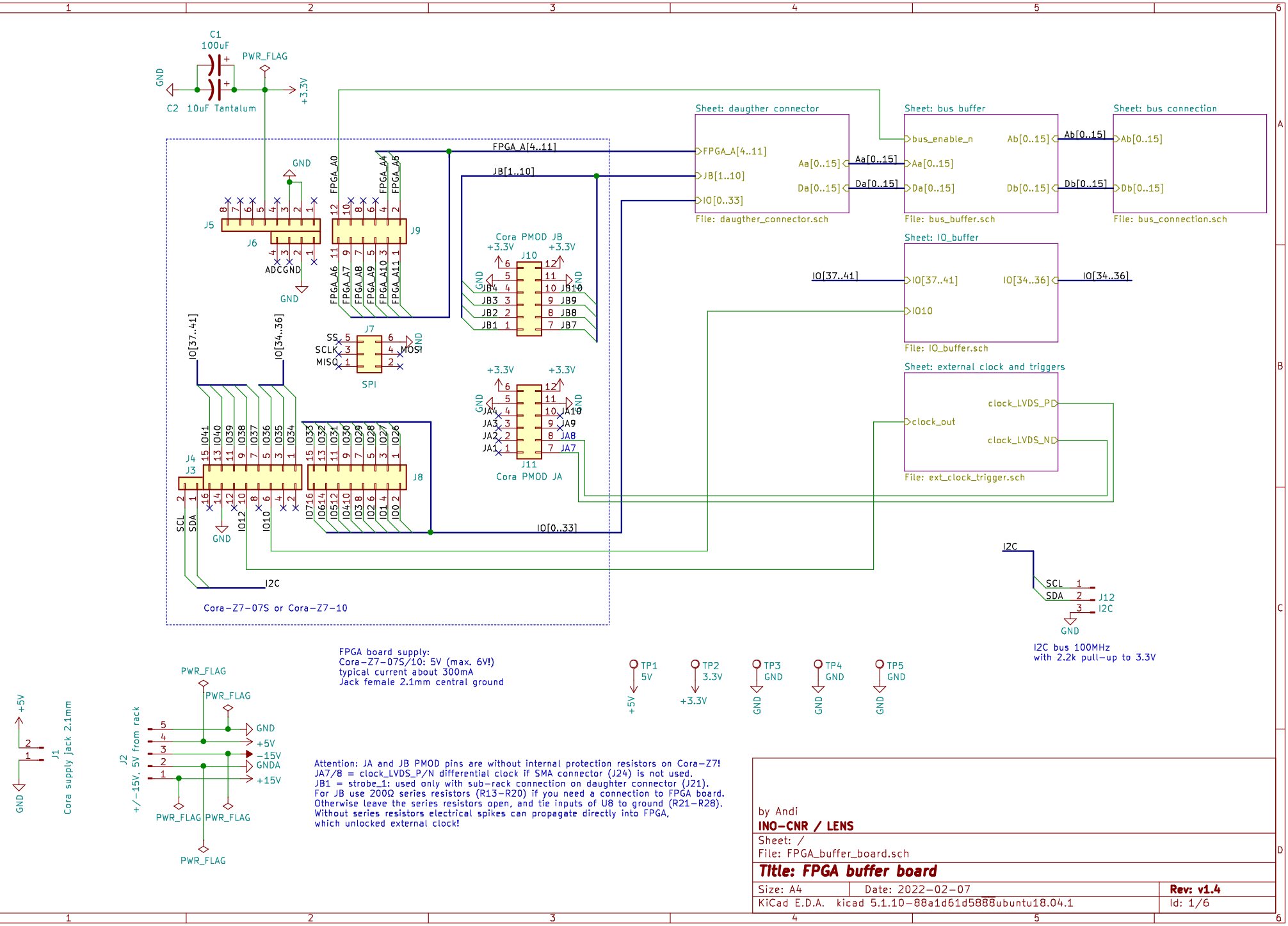
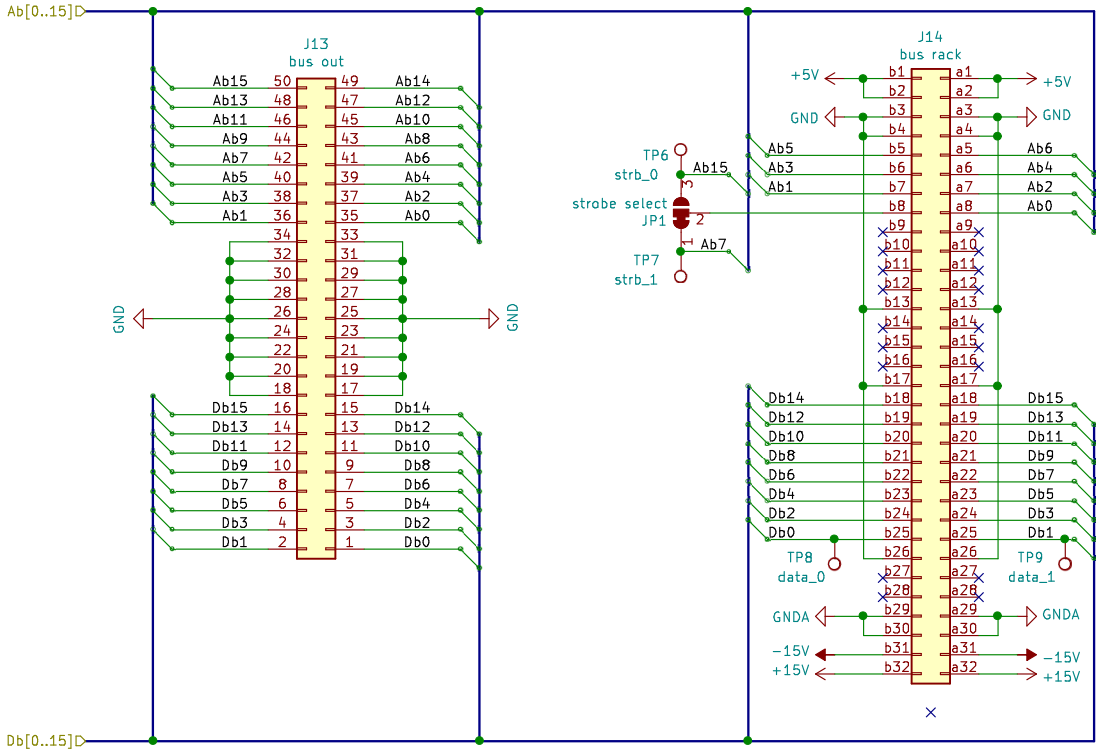

C1
100uF
PWR_FLAG
GND
C2 10uF Tantalum
+3.3V
FPGA_A[4..11]
JB[1..10]
IO[0..33]
Sheet: daugther connector
FPGA_A[4..11]
JB[1..10]
IO[0..33]
Aa[0..15]
Da[0..15]
File: daugther_connector.sch
Sheet: bus buffer
bus_enable_n
Ab[0..15]
Aa[0..15]
Da[0..15]
Db[0..15]
File: bus_buffer.sch
Sheet: bus connection
Ab[0..15]
Db[0..15]
File: bus_connection.sch
J5
J6
J9
ADCGND
FPGA_A0
FPGA_A4
FPGA_A5
FPGA_A6
FPGA_A7
FPGA_A8
FPGA_A9
FPGA_A10
FPGA_A11
Cora PMOD JB
J10
JB4
JB3
JB2
JB1
JB10
JB9
JB8
JB7
J7
SS
SCLK
MISO
MOSI
SPI
IO[37..41]
IO[34..36]
J4
J3
J8
SCL
SDA
I2C
Cora PMOD JA
J11
JA4
JA3
JA2
JA1
JA10
JA9
JA8
JA7
Cora-Z7-07S or Cora-Z7-10
Sheet: IO_buffer
IO[37..41]
IO[34..36]
IO10
File: IO_buffer.sch
Sheet: external clock and triggers
clock_out
clock_LVDS_PD
clock_LVDS_ND
File: ext_clock_trigger.sch
I2C
SCL
SDA
J12
I2C bus 100MHz
with 2.2k pull-up to 3.3V
FPGA board supply:
Cora-Z7-07S/10: 5V (max. 6V!)
typical current about 300mA
Jack female 2.1mm central ground
TP1 5V
TP2 3.3V
TP3 GND
TP4 GND
TP5 GND
J1
Cora supply jack 2.1mm
J2
+/-15V, 5V from rack
GND
+5V
-15V
GNDA
+15V
Attention: JA and JB PMOD pins are without internal protection resistors on Cora-Z7!
JA7/8 = clock_LVDS_P/N differential clock if SMA connector (J24) is not used.
JB1 = strobe_1: used only with sub-rack connection on daughter connector (J21).
For JB use 200Ω series resistors (R13-R20) if you need a connection to FPGA board.
Otherwise leave the series resistors open, and tie inputs of U8 to ground (R21-R28).
Without series resistors electrical spikes can propagate directly into FPGA,
which unlocked external clock!
by Andi
INO-CNR / LENS
Sheet: /
File: FPGA_buffer_board.sch
Title: FPGA buffer board
Size: A4
Date: 2022-02-07
Rev: v1.4
KiCad E.D.A. kicad 5.1.10-88a1d61d5888ubuntu18.04.1
Id: 1/6



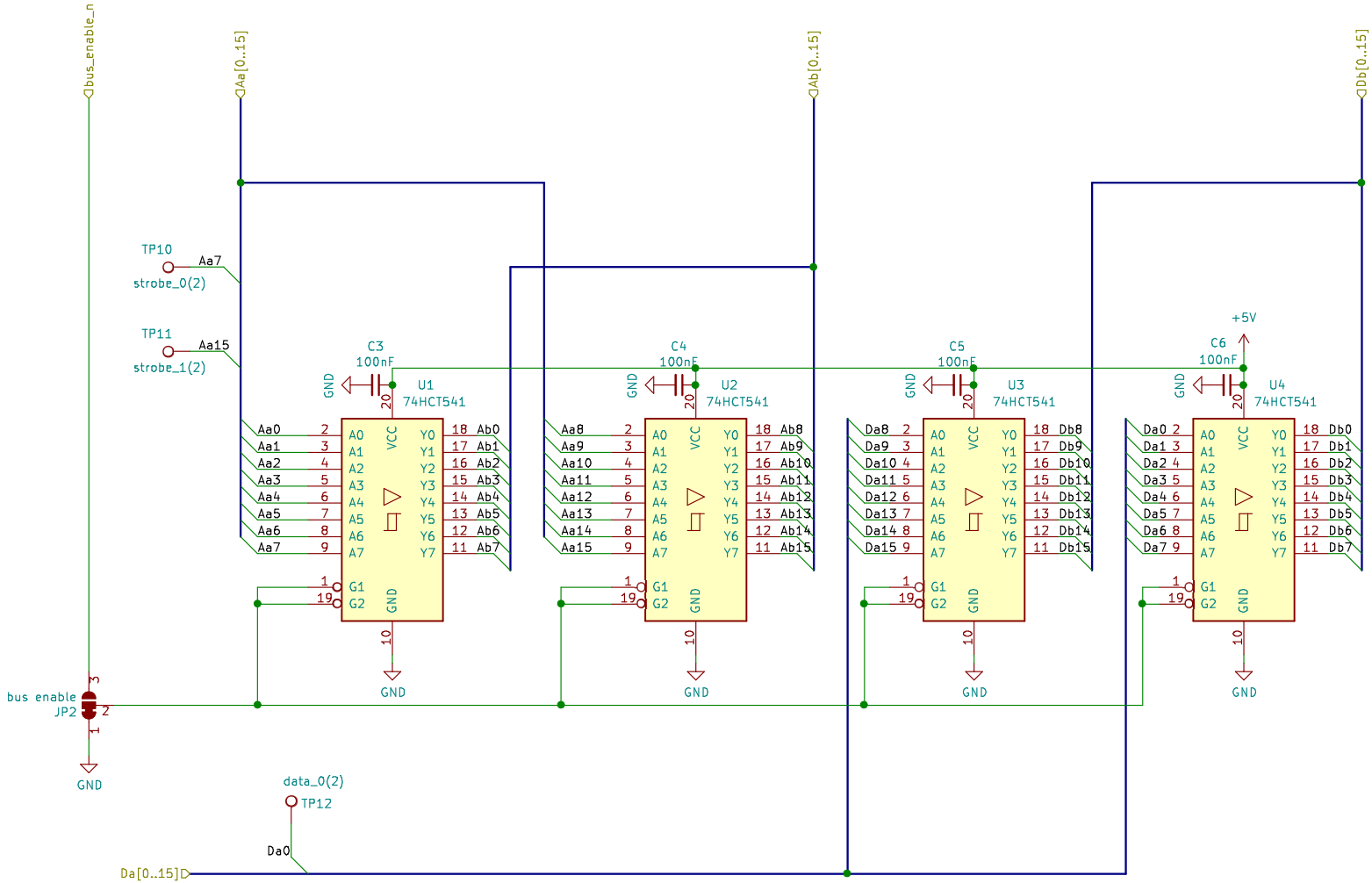
With jumper "strobe select" you can select if strb_0 or strb_1 is used on the bus.
One FPGA board can drive two sub−racks with both receiving the same data.
The daughter I/O connection allows to send buffered data to the 2nd sub−rack.
The FPGA board generates two strobe signals, which can be shifted in time independently,
to compensate for the different cable lenghts between the sub−racks.

by Andi
INO−CNR / LENS

Sheet: /bus connection/
File: bus_connection.sch

Title: FPGA buffer board

Size: A4	Date: 2022−02−07	**Rev: v1.4**
KiCad E.D.A. kicad 5.1.10−88a1d61d5888ubuntu18.04.1		Id: 2/6



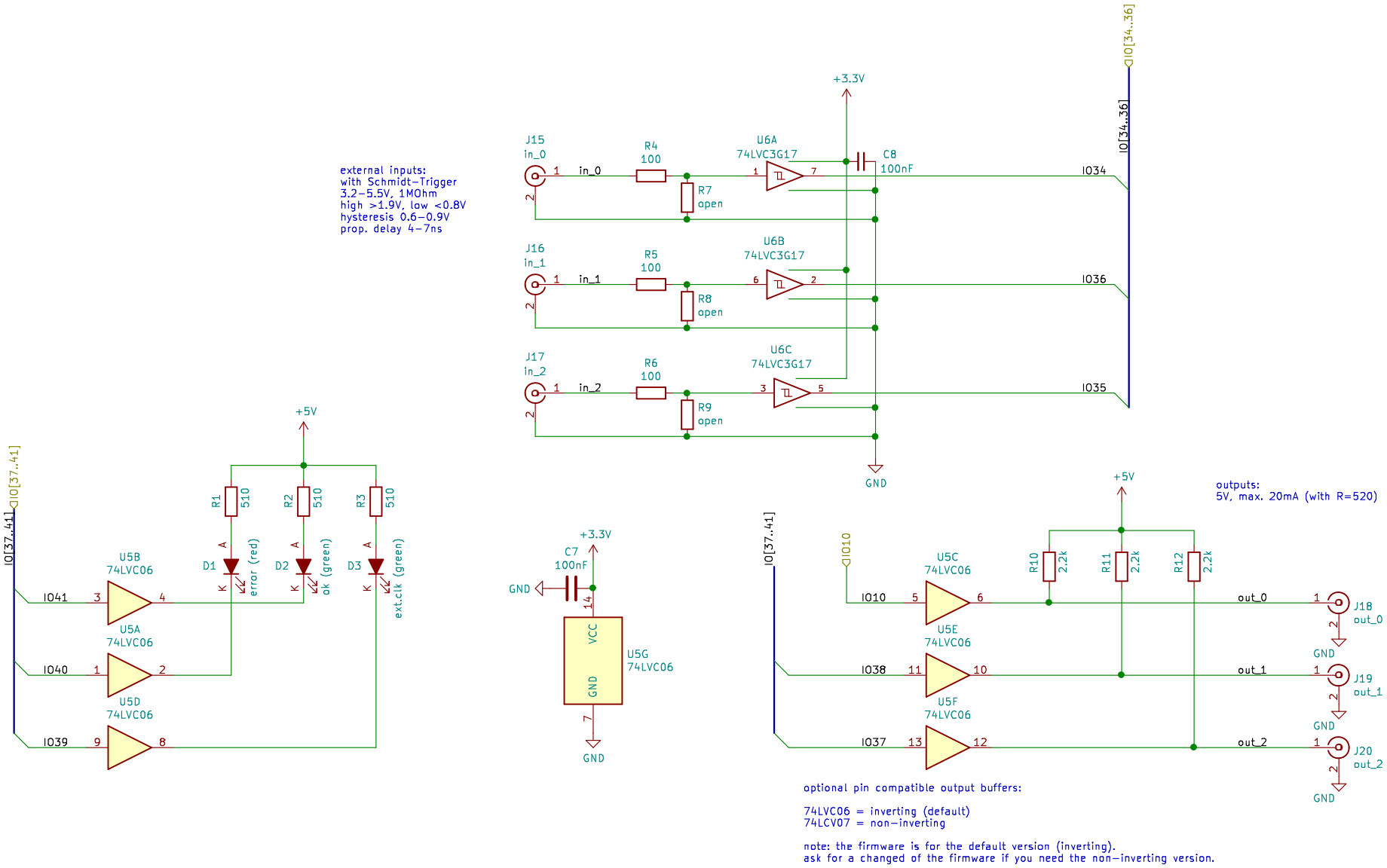
by Andi

INO-CNR / LENS

Sheet: /bus buffer/
File: bus_buffer.sch

Title: FPGA buffer board

Size: A4	Date: 2022-02-07	**Rev: v1.4**
KiCad E.D.A. kicad 5.1.10-88a1d61d5888ubuntu18.04.1		Id: 3/6



by Andi

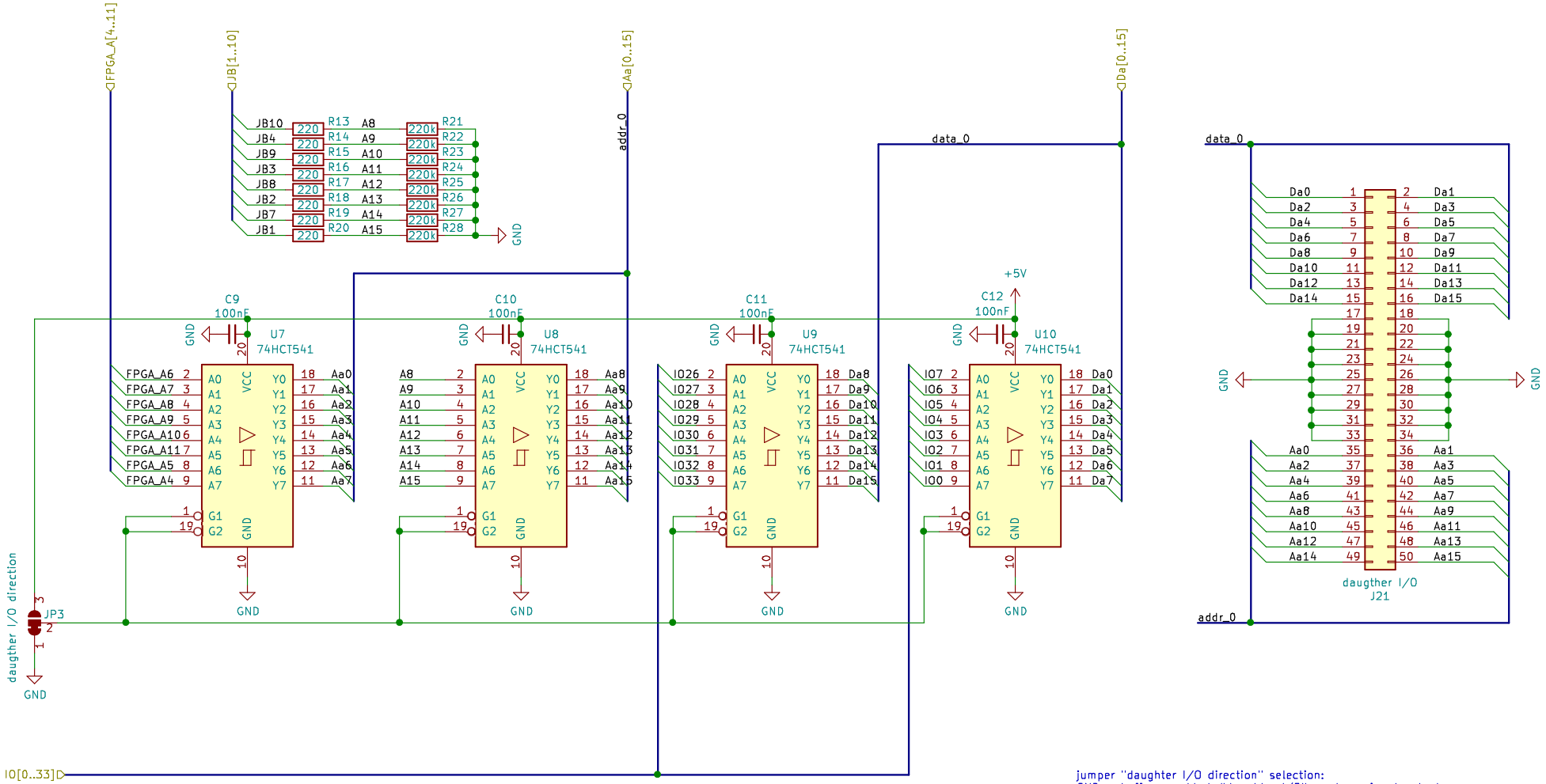
INO-CNR / LENS

Sheet: /IO_buffer/

File: IO_buffer.sch

Title: FPGA buffer board

Size: A4	Date: 2022-02-07	**Rev: v1.4**
KiCad E.D.A. kicad 5.1.10-88a1d61d58~ubuntu18.04.1		Id: 4/6



by Andi

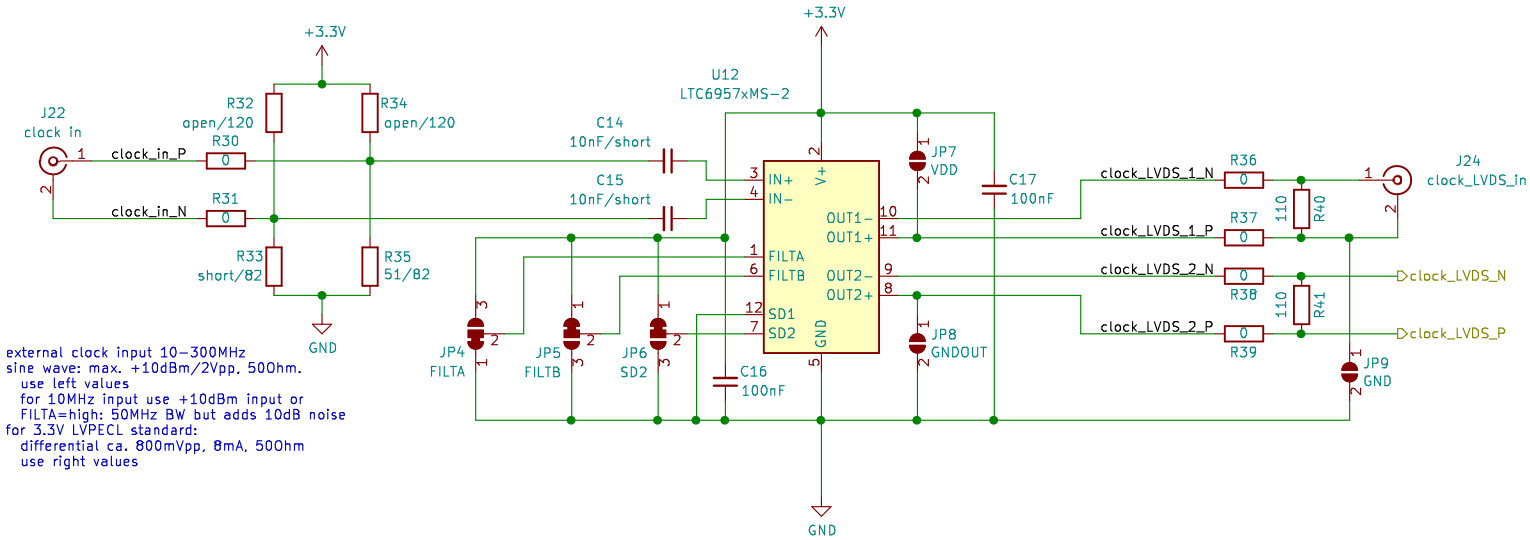
INO-CNR / LENS

Sheet: /daugther connector/

File: daugther_connector.sch

Title: FPGA buffer board

Size: A4	Date: 2022-02-07	**Rev: v1.4**
KiCad E.D.A. kicad 5.1.10-88a1d61d5888ubuntu18.04.1		Id: 5/6



several choices to connect external clock from buffer board into Cora–Z7 board:
on Cora use JA7/8 PMOD connection as inputs.

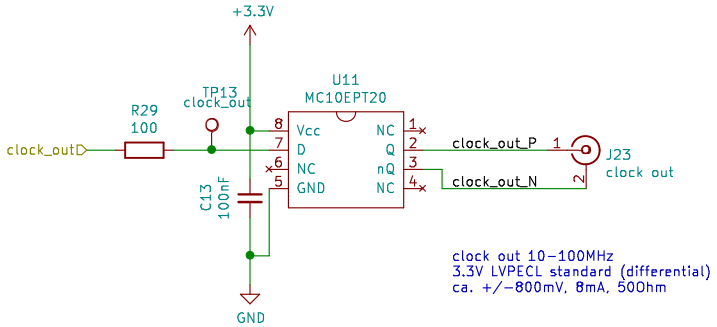
1. SD1 = GND: use short SMA coaxial cable from clock_LVDS_in (J24) to JA7/8 on Cora (default).

2. SD1 = 3.3V: use clock_LVDS_P/N via connector J11 to connect clock to JA7/8 on Cora.

A. differential (LVDS 2.5V) clock: requires U12 = LTC6957xMS–2 (default).
leave JP7, JP8 and JP9 open, R36–R39=0Ω, R40 = R41 = 110Ω.
polarity on JA7/8 pins does not matter.

B. single–ended (CMOS 3.3V) clock: requires U12 = LTC6957xMS–3 or –4 versions.
short JP7, JP8 and JP9, R36 = R38 = R39 = 0Ω, R37 open, R40 = R41 = 500Ω.
JA7 = positive. leave JA8 unconnected.

note: you need the right firmware for versions A or B. A is the default. ask if you need B.



by Andi
INO–CNR / LENS

Sheet: /external clock and triggers/		
File: ext_clock_trigger.sch		
Title: FPGA buffer board		
Size: A4	Date: 2022–02–07	**Rev: v1.4**
KiCad E.D.A. kicad 5.1.10–88a1d61d58~8ubuntu18.04.1		Id: 6/6