XiaoTianQuan Firmware

Control Protocol

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Contents

Work In Progress.

1 Supported Transport Protocols

Currently only I^2C protocol is supported. Serial is planned.

2 I^2C Protocol

2.1 Registers

2.1.1 Product Release Control, RC0-RC15

This register controls the slot to release the product.

Address 0x10

Offset 0-F

Bit	7	6	5	4	3	2	1	0
Description	S8	S7	S6	S5	S4	S3	S2	S1
Access	W	W	W	W	W	W	W	W

S1-8

Write 1 to start releasing product in slot. If there's multiple bits set, the least significant bit will be used.

2.1.2 Product Release Status, RS0-RS15

This register is the status of the slot of last release.

Address 0x20

Offset 0-F

Bit	7	6	5	4	3	2	1	0
Description	S8	S7	S6	S5	S4	S3	S2	S1
Access	R	R	R	R	R	R	R	R

S1-S8

0 indicates last release was successful or no release, 1 indicates the release failed.

2.1.3 Product Release Status Slot, RSS

Address 0x30

This register holds the slot ID of 2.1.4 RE. When written, contents of RE is changed to the slot ID of RSS.

Bit	7	6	5	4	3	2	1	0
Description	Slot ID							
Access	R/W							

Slot ID

The slot ID for register RSS.

2.1.4 Product Release Error, RE

Address 0x31

This register holds the error information of the slot in 2.1.3 RSS..

Bit	7	6	5	4	3	2	1	0
Description	Error ID							
Access	R							

Error ID

The error ID of the corresponding register.

2.1.5 Power Control, PWR

Address 0x80

Bit	7	6	5	4	3	2	1	0
Description	Reserved							AppPwr
Access	N/A							R/W

AppPwr

Write 1 to turn off power of app board.

2.1.6 Battery Voltage, BAT

These register holds the FP32 value battery voltage in Volt.

Address 0x81

Offset 0-1

Bit	7	6	5	4	3	2	1	0
Description	Low 16 bits of battery voltage in FP32							
Access	R							

Address 0x82

Bit	7	6	5	4	3	2	1	0
Description	High 16 bits of battery voltage in FP32							
Access	R							