XiaoTianQuan Firmware

Control Protocol

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Contents

Work In Progress.

1 Supported Transport Protocols

Currently only I^2C protocol is supported. Serial is planned.

2 I^2C Protocol

2.1 Registers

2.1.1 Product Release Control PRC0

Address: 0x10

Bit	7	6	5	4	3	2	1	0
Description	S8	S7	S6	S5	S4	S3	S2	S1
Access	W	W	W	W	W	W	W	W

S1-8

Write 1 to start releasing product in slot. If there's multiple bits set, the least significant 1 bit will be used.

2.1.2 Product Release Status PRS0

Bit	7	6	5	4	3	2	1	0
Description	S8	S7	S6	S5	S4	S3	S2	S1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

S1-S8

When read, 1 indicates last release was successful, 0 indicates there's no release or release failed. Write 1 to clear the bit.

2.1.3 Power Control