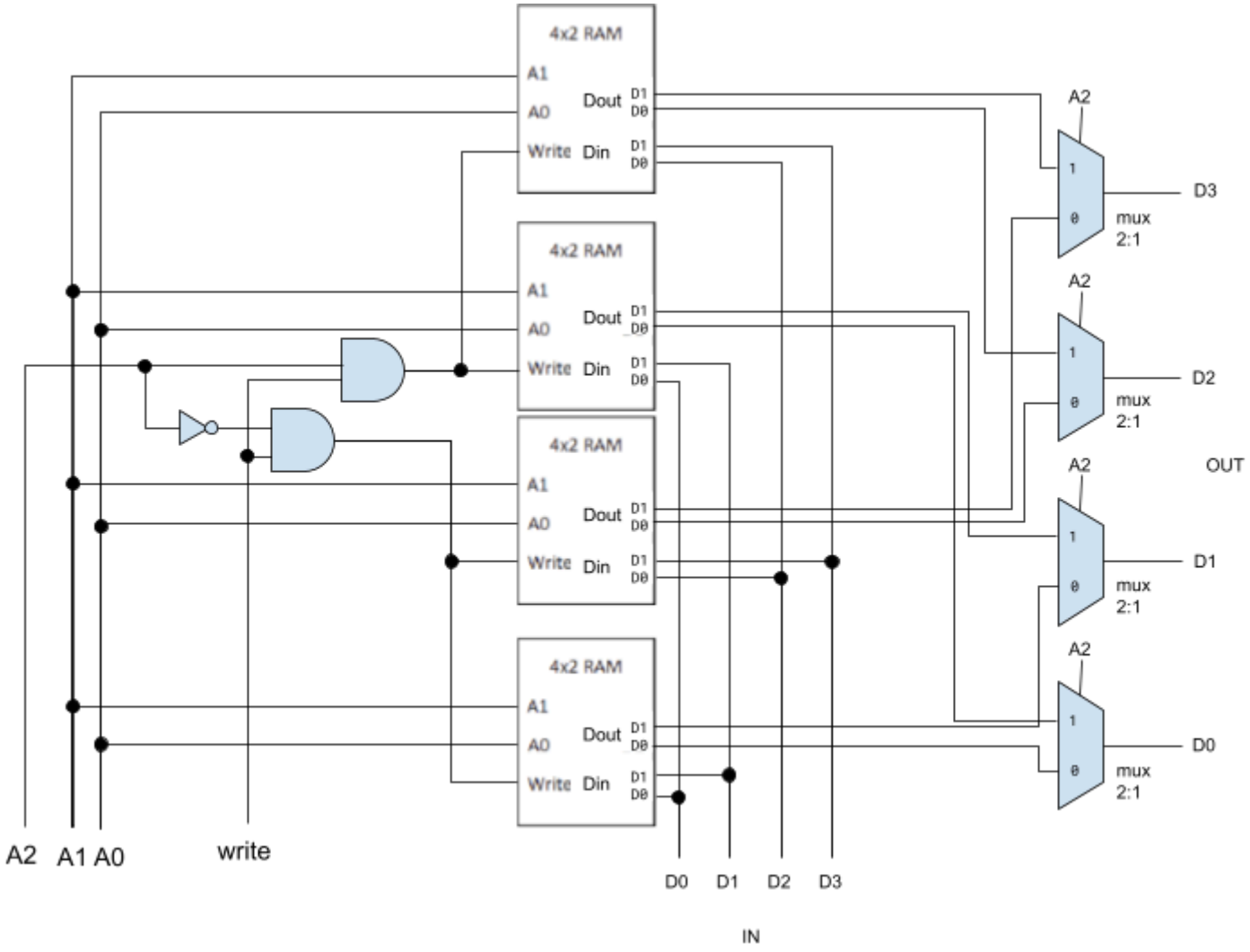
Christopher Andrade | andradec | 2221525

EE/CSE 469 Computer Architecture I
HW 1

1. Design an 8x4 RAM using 4x2 RAMs (shown in the figure). You may use any number of RAM units as you need and any necessary combinational logic.
In the figure below, A1 and A0 specify bit 1 and 0 of the 2-bit address input of the 4x2 RAM, respectively. D1 and D0 represent bit 1 and 0 of its input/output data, respectively.

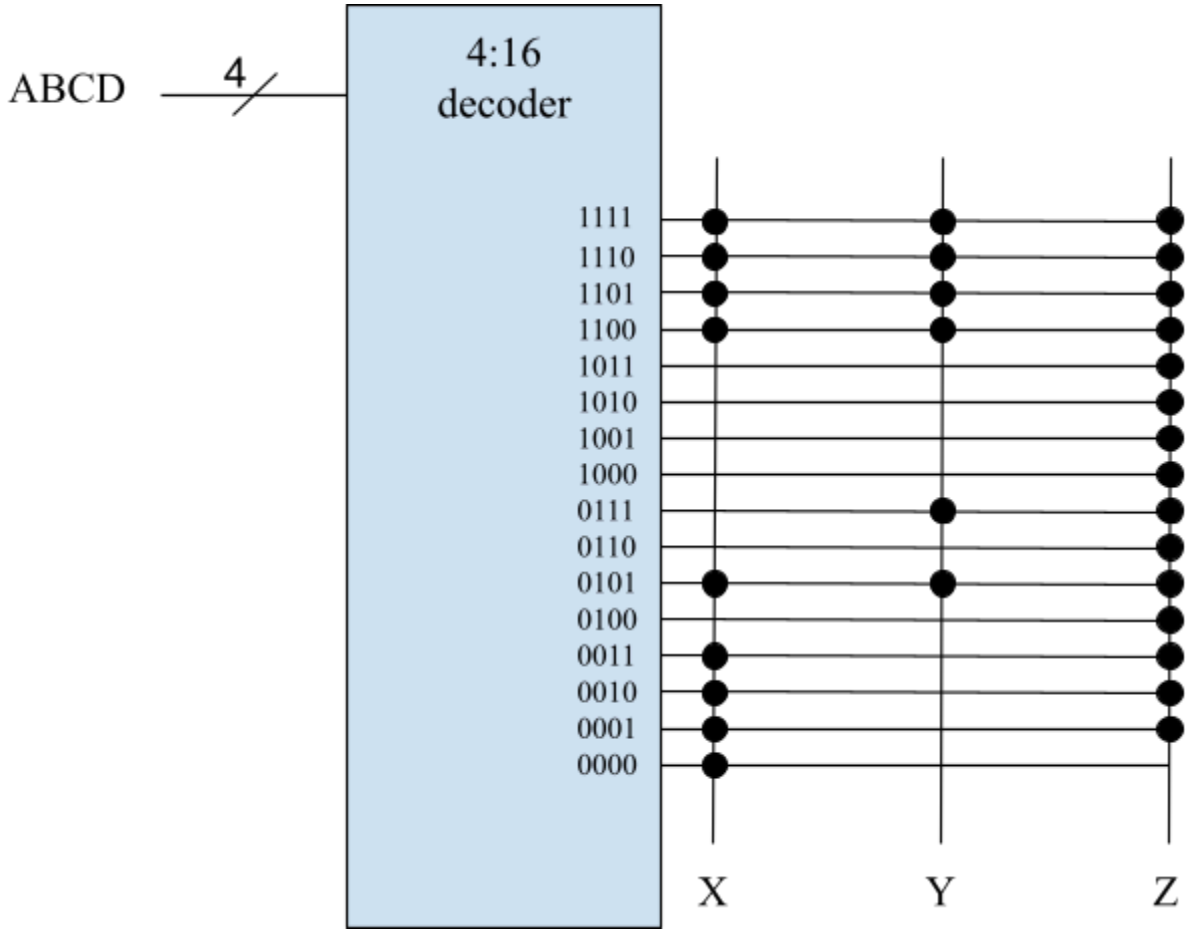


2. Implement the following functions using a single 16x3 ROM. Use dot notation to indicate the ROM content.

a. X = AB + BC'D + A'B'

b. Y = AB + BD

c. Z = A + B + C + D



3. Consider memory storage of a 32-bit word stored at memory word 42 in a byte-addressable memory. Keep in mind the indexing method described in lecture.

a. What is the byte address of memory word 42?

32 bits = 4 bytes, 4 x 42 = 168 (Decimal), 0xA8 (Hex)

Memory word 42 has the address 0xA8

b. What are the byte addresses that memory word 42 spans?

0xA8 (Hex) + 4 bytes = 0xAC, Address of memory word 43

Memory word 42 spans from 0xA8 to 0xAB.

c. Draw the number 0xFF223344 stored at word 42 in both big-endian and little-endian machines. Clearly label the byte address corresponding to each data byte value.

Word Address	Data				Word Number
0xA8	44	33	22	FF	Word 42
	0xAB	0xAA	0xA9	0xA8	

big-endian

Word Address	Data				Word Number
0xA8	FF	22	33	44	Word 42
	0xAB	0xAA	0xA9	0xA8	

little-endian