TÉCNICO LISBOA

Instituto Superior Técnico

Digital Systems Design

1º Semester 2021/2022

1º Report
Simple Logic-Arithmetic Unit

Group 7

Nome	Número
André Pereira	90016
Tiago Gonçalves	90195

Day of the week:Friday, from 10:00 AM to 1:00 PM.

Professor: Horácio Neto

1 Moore Machine

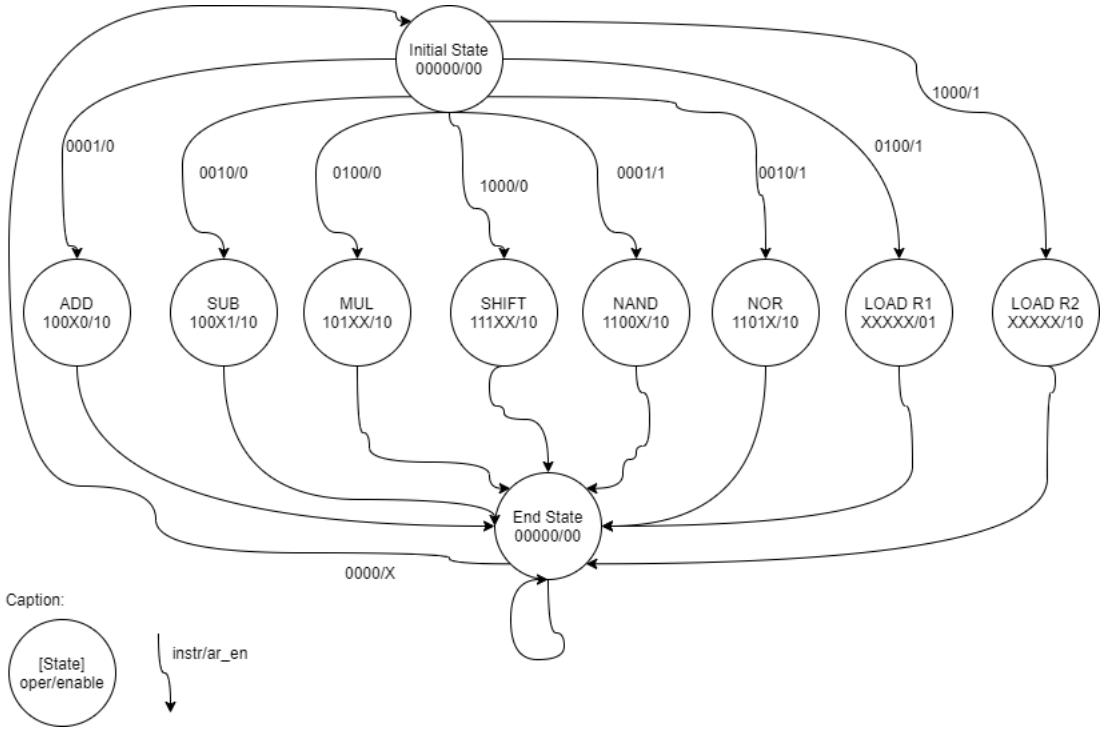

Figure 1: Moore state machine. Each circle represents the state, while showing the std_logic_vector ”oper” on the left and ”enable” on the right. Each arrow represents the next state decision making, made possible by the std_logic_vector ”instr” on the left side and the std_logic ”ar_en” on the right side.

2 Design

In our implementation, we decided to create a menu of operation choices based on the value of the L014 switch, to create a global system reset and to show the value stored in a register based on the value of the L015 switch.

- The numbers are stored internally using the two´s complement numeric representation. However, they are loaded into the registers using the sign-magnitude formate. We are only able to insert at the INPUT numbers using bits 0 to 12: bit_{12} (most significant bit, represented by the L012 switch) representing the signal, and the remaining 12 bits the whole number (from L011 to L00, respectively). To represent negative numbers, we take into account the most significant bit of the register, and, if it is 1, we activate a dot on the LED screen display to represent that the number is negative.

Table 1: Supported Ranges

	Bit Range	Decimal Range
Input	[bit_{12}, bit_0]	[- 4 095, + 4 095]
Register R1	[bit_{12}, bit_0]	[- 4 095, + 4 095]
Register R2	[bit_{16}, bit_0]	[- 65 535, + 65 535]

Whenever a number that is stored in Register R2 has less bits than it´s bit range, it is perfomed padding on the signal. The most significant bit is extended until we achieve the desired bit range.

- The std_logic ”ar_en” is coupled to the value of the L014 switch, allowing us to choose the operation such that:

Table 2: Available Operation

L014 value	Button pressed	Operation Performed
0	BTND	Addition
	BTNR	Subtraction
	BTNC	Multiplication
	BTNL	Shift Right
1	BTND	NAND
	BTNR	NOR
	BTNC	Load value to R1 register
	BTNL	Load value to R2 register
X	BTNU	Global system reset

- It is possible to occur overflow if the result of an operation would need more than the bit range supported by the register R2 to be represented.
- The global system reset clears out the values stored in both registers, by storing the value 0 on both of them.

3 Control Unit

The control Unit will be responsible to receive the input data and to transform it into intruction for the Datapath. In this project the Control Unit will receive a std_logic_vector instr of 4 bits, that simulates a click of a button on the fpga, it will also receive a std_logic ar_en, that is a switch on the fpga. The control unit will then create two std_logic_vectors one of 2 bits (enable) and one of 5 bits (oper).

4 Datapath Unit

The datapath Unit will be responsible to do the instructions recieved by the control unit. The enable vector is responsible for enable the R1 (bit 0) or R2 (bit 1) registors. The oper vector is responsible to control all the multiplexers in the datapath.

5 Timing analysis

Design Timing Summary

Setup		Hold		Pulse Width	
Worst Negative Slack (WNS):	2,865 ns	Worst Hold Slack (WHS):	0,266 ns	Worst Pulse Width Slack (WPWS):	4,500 ns
Total Negative Slack (TNS):	0,000 ns	Total Hold Slack (THS):	0,000 ns	Total Pulse Width Negative Slack (TPWS):	0,000 ns
Number of Failing Endpoints:	0	Number of Failing Endpoints:	0	Number of Failing Endpoints:	0
Total Number of Endpoints:	103	Total Number of Endpoints:	103	Total Number of Endpoints:	59

All user specified timing constraints are met.

Figure 2: Time Analysis

6 Resource Consumption

Resource	Utilization	Available	Utilization %
LUT	146	20800	0.70
FF	81	41600	0.19
DSP	1	90	1.11
IO	50	106	47.17

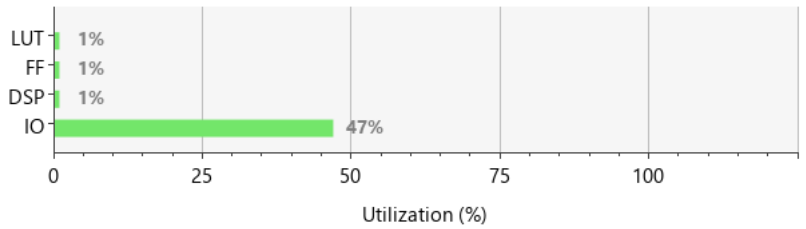

Figure 3: Resource Consumption