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EEEN313 Design Report
Variable output DC-DC Converter

1. Introduction

This report outlines the design of a controller circuit for a buck converter. The design implements a feedback loop and PI compensator to control the voltage output level of a buck converter. The result of the design was a control circuit capable of compensating to disturbances and changes to the input voltage to achieve a stable output. It is also able to produce a variety of output voltages on the buck ranging from 20% to 80% of V_{in}, The step response shows the system is slightly underdamped, but settles in approximately 45ms. The values for the buck converter the control circuitry was designed for are as follows.

$$V_{in} = 11V \; to \; 14V$$

$$V_{out} = 0.2V_{in} \; to \; 0.8V_{in}$$

$$L = 4mH$$

$$C = 10\mu F$$

$$r = 0.02\Omega$$

$$R_L = 100\Omega$$

Where r is the equivalent series resistance of the capacitor, R_L is the load resistance, L is the buck filter's inductor value, and C is the capacitor value. The design for the set point V_{out} used a nominal $V_{in} = 12V$.

2. Background

A buck converter is a device that is used to step DC voltages down to lower DC voltages with minimal losses. It achieves this using switching power poles and filtering. A PWM signal is used to drive the switching of the power poles, where the duty cycle indicates the theoretical output voltage, given Eq. 1. Due to switching and conduction losses in the switching power poles, as well as conduction losses in the filter elements, Eq. 1 will not exactly match the output voltage to a duty cycle, that is, if the desired $V_{in} = 0.5V_{out}$ this requires $d > 0.5$ to compensate for these losses.

$$V_{out} = dV_{in} \qquad (1)$$

In an open loop configuration, the required duty cycle to achieve the desired V_{out} from a static V_{in} can be determined, however the output voltage will change with disturbances or changes to the input voltage. To overcome this, a feedback loop with some control circuitry can be used. By comparing the output of the buck converter with some setpoint voltage to determine an error, a PI controller can be used to drive the PWM duty cycle up or down to compensate for disturbances or changes to the input voltage. Using this closed loop feedback configuration, a buck converter can be used to produce a stable output voltage. An adjustable setpoint can be implemented to create a converter capable of outputting a range of voltages.

The control circuit design implemented a hardware PI compensator using an OP-AMP, as opposed to a software approach. Figure 1 shows a schematic for an OP-AMP PI controller. Equations 2, 3, and 4

show how to find the K_i, K_p, and ω_c values for the c. R_i determines the current to the anode of the capacitor, where R_f determined the voltage. In this configuration, $V_i > 0V$ will cause the output to ramp down, and $V_i < 0V$ will cause the output to ramp up.

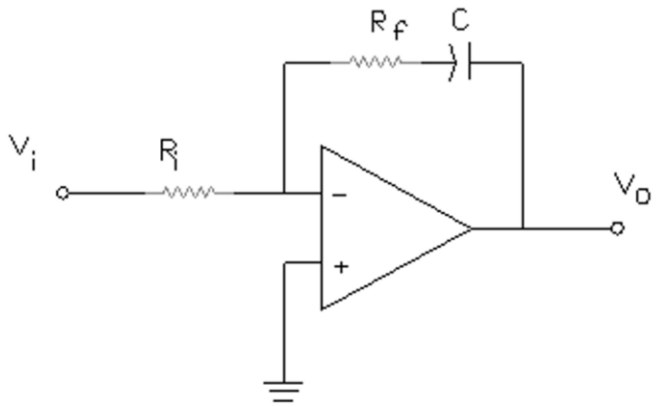

Figure 1: Schematic of OP-AMP PI controller

$$K_p = \frac{R_f}{R_i} \tag{2}$$

$$K_i = \frac{1}{R_i C} \tag{3}$$

$$\omega_c = \frac{1}{R_f C} \tag{4}$$

3. Design

Figure 2 shows the full schematic for the buck converter PI controller that was designed. The circuit can be broken down into sub blocks; the triangle wave generator, the setpoint voltage, the measured buck voltage, difference amplifier, the PI compensator, and the PWM output. This section describes the design and functionality of the main blocks of this circuit. Please observe in the top left of figure 2 that a voltage divider and buffer is used to produce $\frac{V_{cc}}{2}$ which is used as a reference voltage for several blocks. The design implemented TLE2082 OP-AMPS, the LM319 comparator, E12 resistors, a ceramic capacitor on the triangle wave generator, and an electrolytic on the PI compensator.

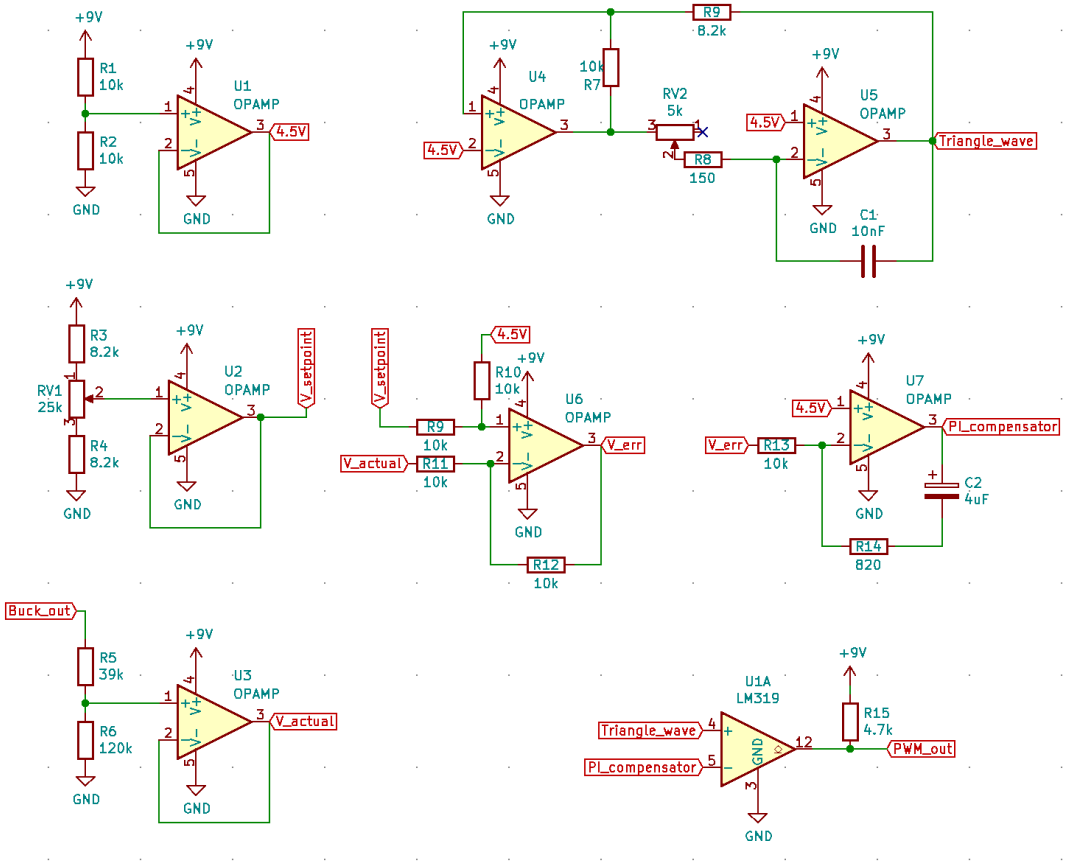

Figure 2: Schematic for buck boost PI controller

3.1 Triangle wave generator

The triangle wave generator uses 2 main blocks, a Schmitt trigger, and an integrator. The Schmitt trigger outputs to the integrator, which feeds back to the input of the Schmitt trigger. When the Schmitt trigger output is high, the integrator ramps down until it triggers the Schmitt trigger output to go low, where the integrator then begins to ramp down. Figure 3 shows a schematic of the triangle wave generator used in the design. This was designed to be tuneable so that the desired frequency could be achieved without having to rely on theoretical values. Equation 5 shows the equation given the resistor numbers shown in figure 3. As R_{v2} varies from 0Ω to $5k\Omega$ this gives a theoretical frequency range of $5.9kHz$ to $200kHz$.

$$f_{triangle} = \frac{R_7}{4R_9(R_{v2} + R_8)C_1} \quad (5)$$

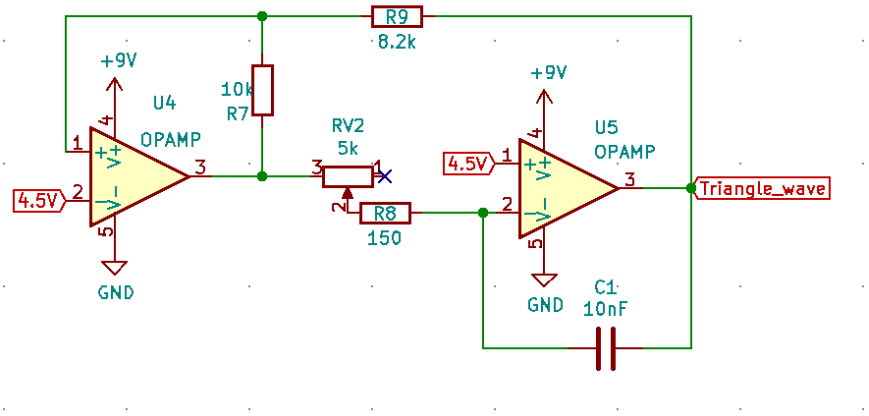

Figure 3: Schematic of the triangle wave generator used

3.2 Setpoint Voltage

An error is needed as the input to the PI compensator, for this there needs to be some setpoint voltage from which the buck output can be subtracted. To produce a setpoint voltage between 20% and 80% of V_{in} a potentiometer was used, with equal value resistors either side. The resistance values needed for this were found Using the voltage diver equation shown in Eq. 6. Figure 4 shows the schematic for this section of the circuit.

$$V_{in} \times \frac{R_2}{2R_1 + R_2} = 0.6V_{in} \tag{6}$$

From this equation it was determined that using 2 $8.2k\Omega$ resistors either side of a $25k\Omega$ potentiometer would produce voltages between 20% and 80% of V_{in}. Figure 4 shows the schematic for this section of the circuit.

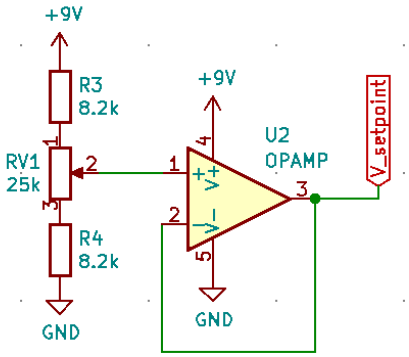

Figure 4: Schematic for setpoint section of controller circuit

3.3 Buck Voltage

The control circuit was designed to operate at 9V, so to produce a voltage to subtract from the setpoint, the buck output must be mapped to voltages between 0V and 9V. A voltage divider was used for this, assuming a nominal $V_{in} = 12V$. Where $V_{out} = 12V$ the voltage divider should bring this to 9V. By Eq. 7, this voltage divider needs $R_2 = 3R_1$ to achieve 9V on the divider node with a 12V input. Figure 5 shows the schematic for this part of the circuit. $120k\Omega$ and $39k\Omega$ were used in

the design as these were available E12 resistor values, and this will not impact the total output resistance on the buck in parallel with 100Ω. R6 in figure 5 can be replaced with a variable resistor which will allow for multiple V_{in} settings.

$$12V \times \frac{R_2}{R_1 + R_2} = 9V \tag{7}$$

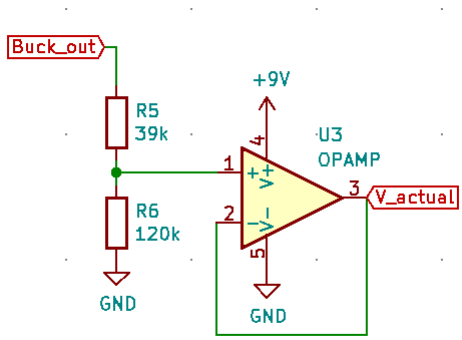

Figure 5: Schematic for mapping buck output to voltage between 0V and 9V

3.4 PI Compensator and PWM output

The set point voltage and buck out voltages were given as V_2 and V_1 to a difference amplifier, this is shown in figure 6. As the voltage divider with $V_{setpoint}$ goes to 4.5V and not ground, this "tricks" the op-amp into thinking it's on split rails, and the difference is output relative to 4.5V. This is done so when V_{actual} is greater than $V_{setpoint}$ it will not saturate the amplifier.

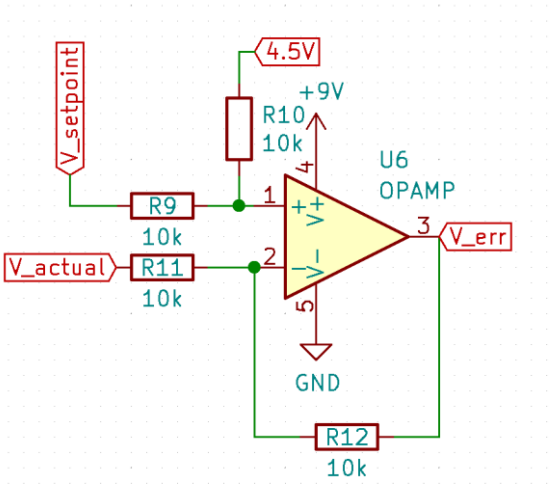

Figure 6: Schematic of difference amplifier

This error is given to the PI compensator which is given 4.5V on the non-inverting terminal instead of ground for the same reason as above. The PI compensator was designed given the values outlined in the introduction, and the transfer function shown in Eq. 8. Figure 7 shows a bode plot of the compensated system compared with the uncompensated system (see figure 14 in the appendix for a plot showing only the uncompensated buck). As there in no phase crossing, the focus of the design was to achieve 0 steady state error without impacting the phase of the system around the 0dB

crossing frequency. To achieve this, a PI compensator with $\omega_c = 250rad/s$ was chosen. Given an input resistor of $10k\Omega$, Eq. 2, Eq. 3, and Eq. 4, in section 2, $R_f = 1k\Omega$ and $C = 4\mu F$ will achieve this. Observe in figure 7 that this has not changed the phase around the area of interest, or introduce a $-180°$ phase crossing. Observe the 20dB per decade slope at low frequencies shows this compensator will produce 0 steady state error to a step input.

$$\frac{V_{out}}{d} = \frac{V_{in}}{LC} \times \frac{1 + srC}{s^2 + s\left(\frac{1}{RC} + \frac{r}{L}\right) + \frac{1}{LC}} \quad (8)$$

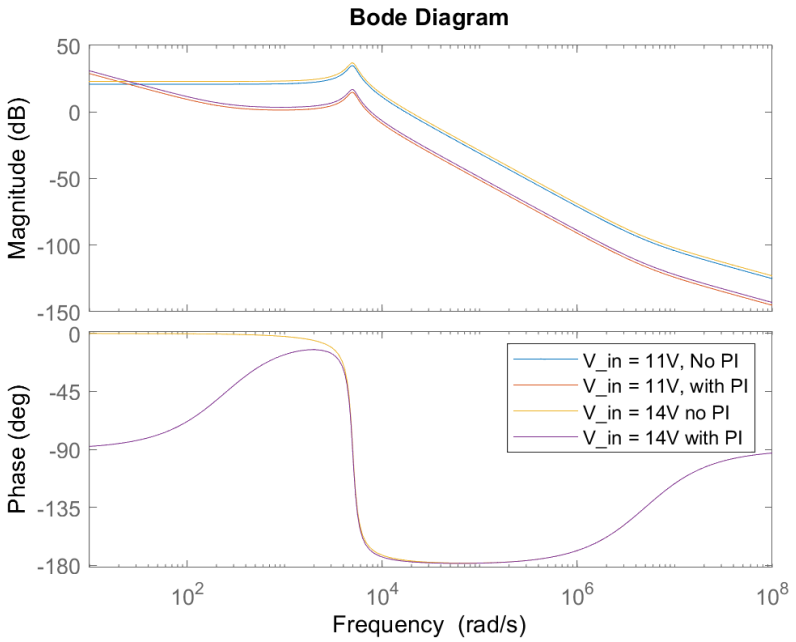

Figure 7: Compensated vs uncompensated buck bode plots

Figure 8 shows the schematic for this portion of the circuit. An 820Ω resistor was used in practise which corresponds to $\omega_c = 305rad/s$. The results section shows that this PI compensator is stable.

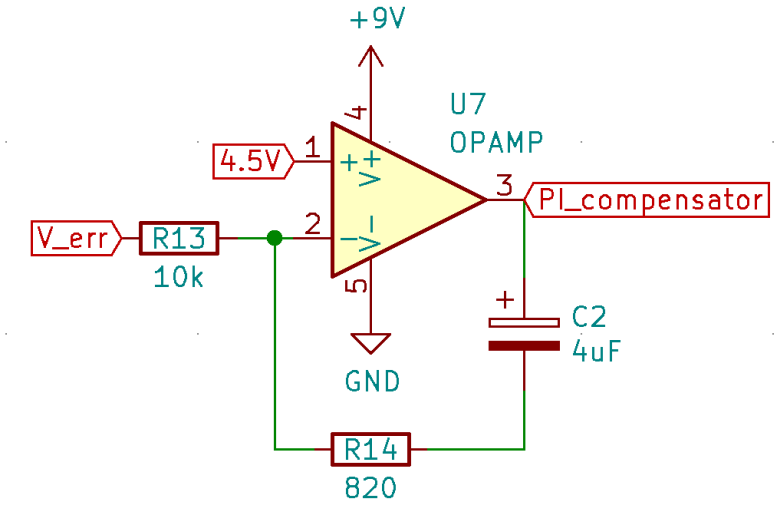

Figure 8: Schematic for PI compensator portion of the circuit

With this configuration, where $V_{err} > 4.5V$ current will go to the anode of the capacitor, and the op-amp will compensate by ramping down. The PWM used to drive the buck converter is produced using a comparator with the triangle wave on one input, and the PI output on the other. As a positive error corresponds $V_{actual} < V_{setpoint}$, a downward ramp needs to correspond with an increase in duty cycle on the buck converter, which is achieved by putting the triangle wave on the non-inverting terminal, and PI output on the inverting. Figure 9 shows the schematic of this portion of the circuit.

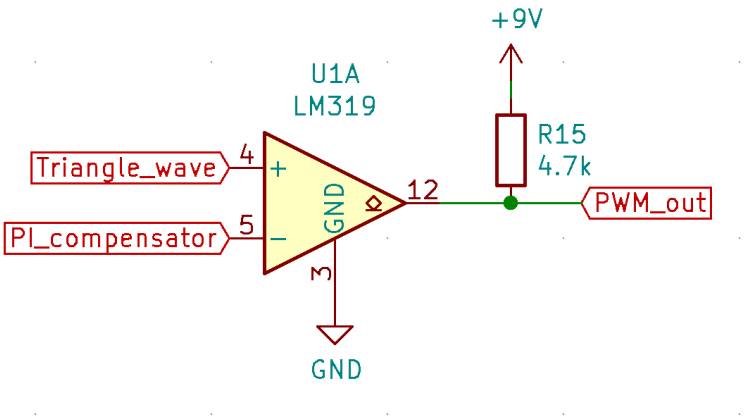

Figure 9: Schematic of PI compensator portion of the circuit

4. Results

The control circuit designed was used on the buck converter as described in the introduction. As seen in figure 10, a stable 5V output was achieved with a 12V input. Upon varying the input voltage, I found my circuit was able to maintain a 5V output for input voltages from 10V to 16V, figures showing this are included in the appendix.

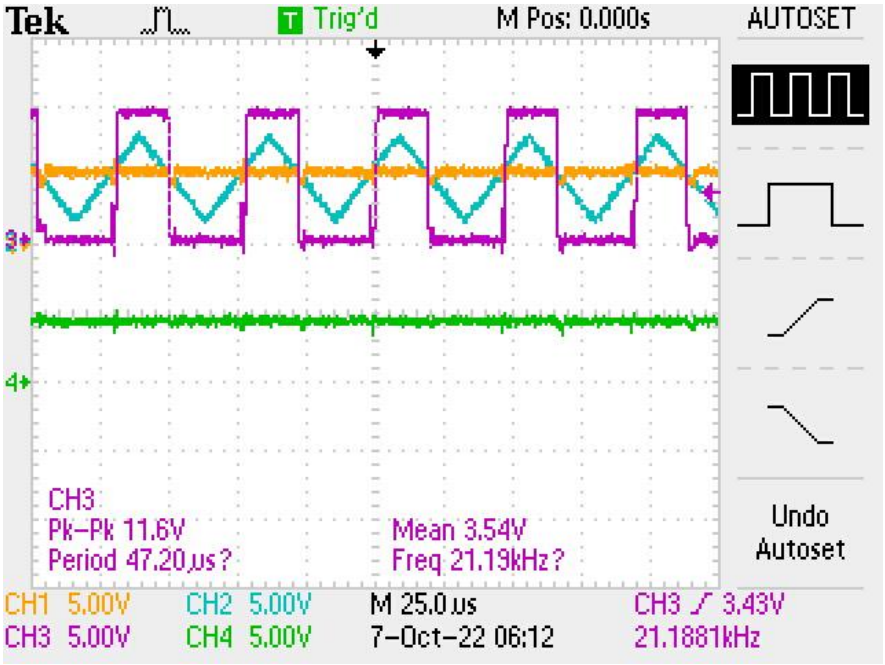

Figure 10: Scope view of $V_{setpoint} = 5V$ and $V_{in} = 12V$

Figures 11 and 12 show the outputs for $0.2V_{in}$ and $0.8V_{in}$ for $V_{in} = 12$. For figures 10, 11, and 12, channel 1 shows the output of the PI compensator, 2 the triangle wave, 3 the output PWM, and 4 the output voltage of the buck converter. Figure 13 shows the step response of the converter. This was done by replacing the voltage divider circuit shown in section 3.2 with a toggle switch that switched between $V_{setpoint} = 2.13V$ and $V_{setpoint} = 5V$. This corresponds with output voltages of $\approx 2.84V$ and $6.67V$.

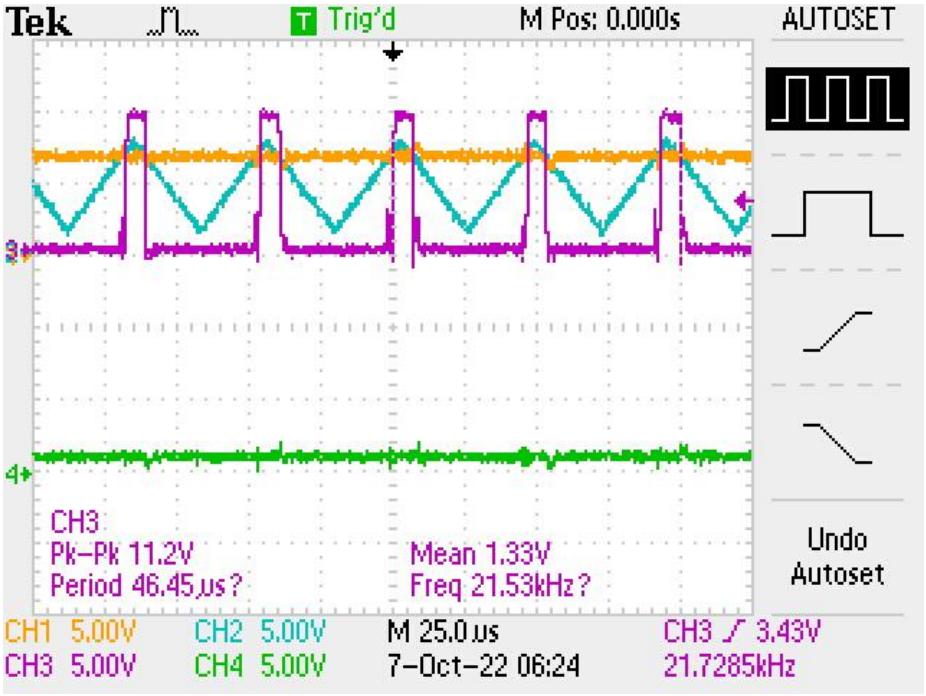

Figure 11: $V_{in} = 12V, V_{out} = 0.2V_{in}$

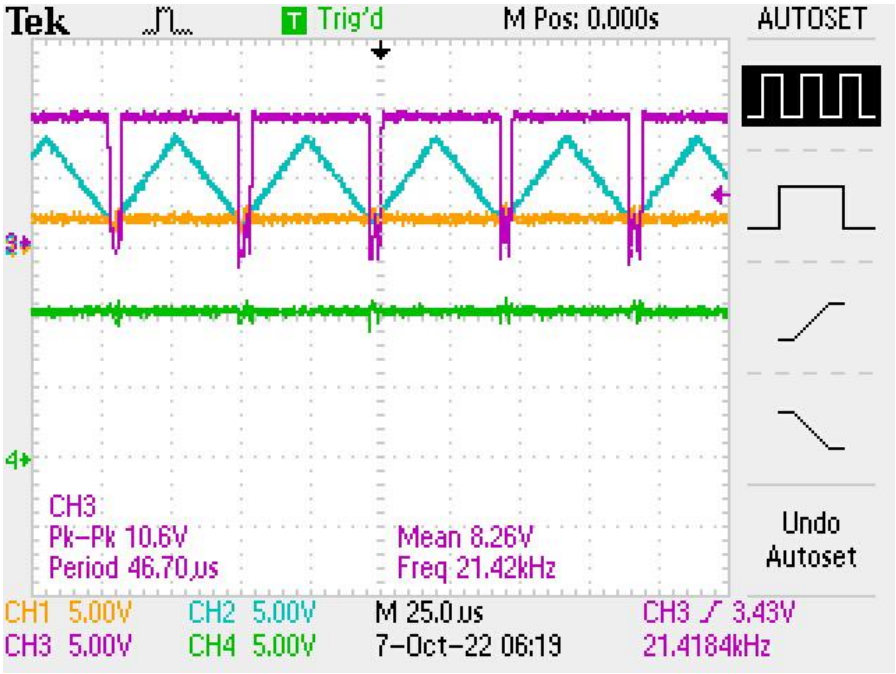

Figure 12: $V_{in} = 12V, V_{out} = 0.8V_{in}$

Figure 13 shows the feedback controlled buck converter is slightly over damped, and settles from a step input within roughly 45ms. Ideally, I would have liked to produce a step with a change in input voltage, however the toggle switch available was 150Ω which altered the transfer function of the buck, resulting in the applied compensation pushing the system into instability.

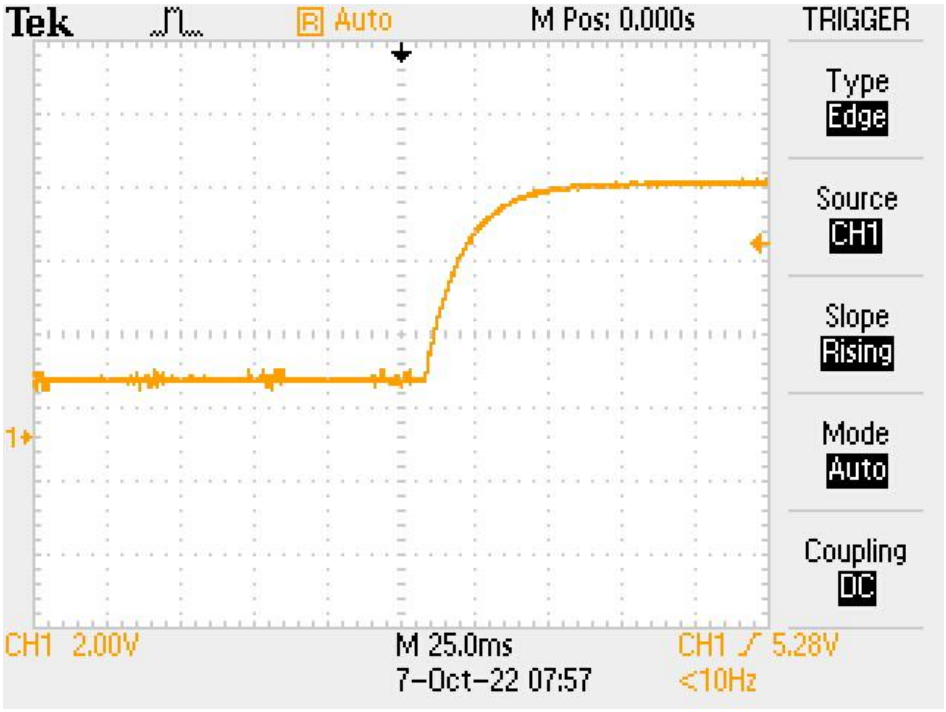

Figure 13: Step response of buck controller

5. Conclusion

To produce a buck converter capable of producing a range of stable output voltages, I designed and built a hardware PI controller circuit. The circuit designed maps the output voltage to voltages between 0V and 9V as is used by the control circuitry, this is done using a voltage divider that results in 9V on the tapped node for the nominal V_{in} determined to be 12V. A setpoint voltage is achieve using a potentiometer where the voltage on the wiper ranges from $\approx 1.8V$ to $\approx 7.2V$ which corresponds to 20% to 80% of V_{in}. The buck output and setpoint are given as V_1 and V_2 to a difference amplifier with gain 1 to produce an error relative to $4.5V$. The error voltage is given to a PI compensator, which outputs the inverting terminal on a comparator with a triangle wave on the other terminal. This configuration means decreases in the PI output will result in increases in duty cycle. Upon testing, the circuit I designed showed to be capable of compensating for changes or disturbances to the buck input voltage. It has shown to produce a static output for a variety of input voltages, and can alter the setpoint value to achieve output voltages from 20% to 80% of the nominal input voltage. When a step input was applied, the controller showed a slightly under damped response with a settling time of approximately 45ms.

6. Appendix

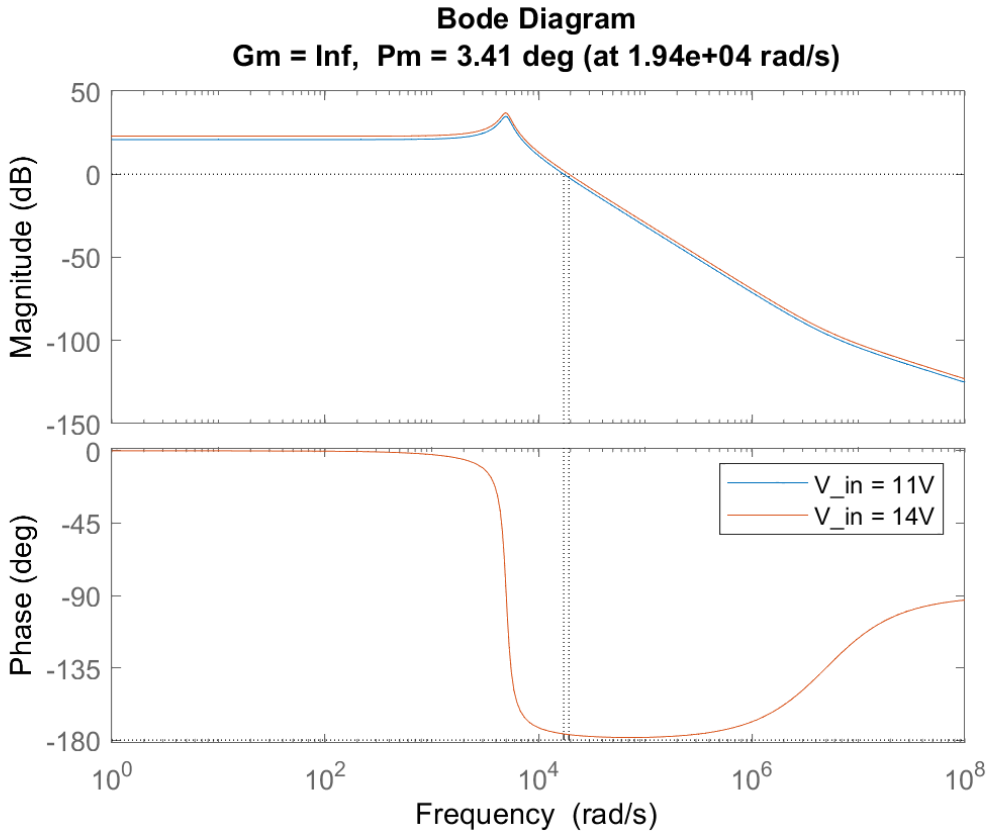

Figure 14: Bode plot of uncompensated buck converter

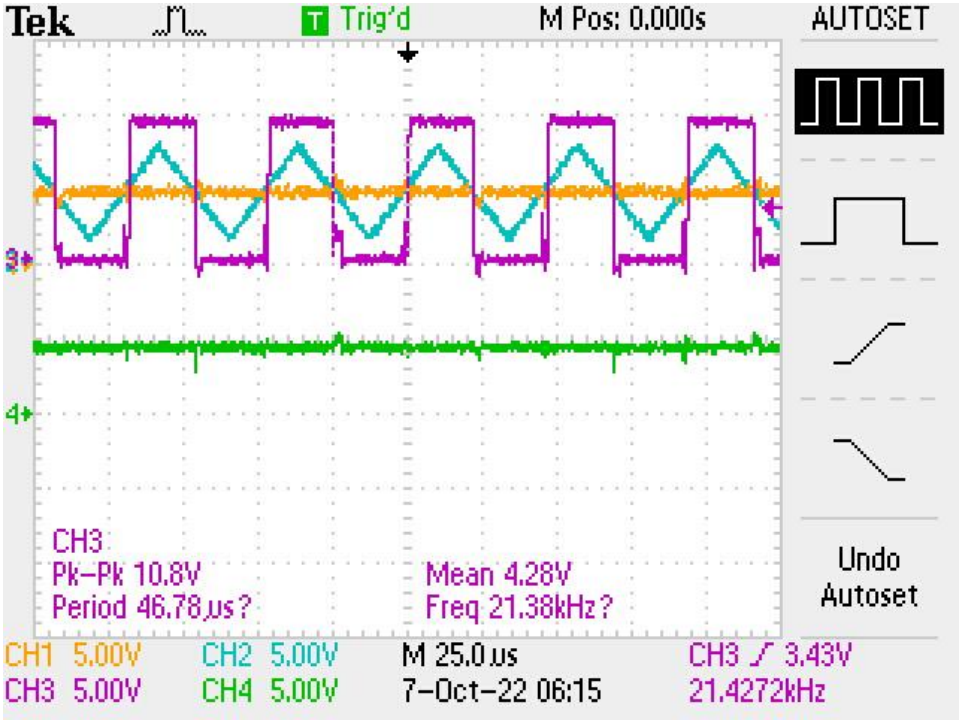

Figure 15: $V_{in} = 10V$, $V_{out} = 5V$

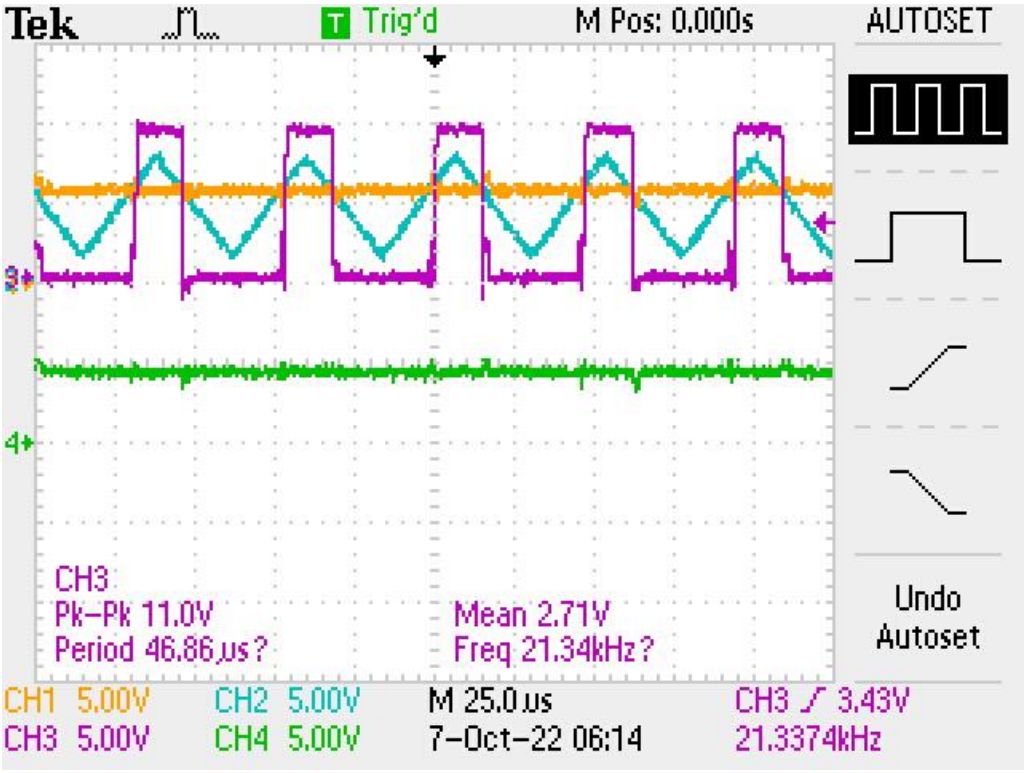

Figure 16: $V_{in} = 16V, V_{out} = 5V$

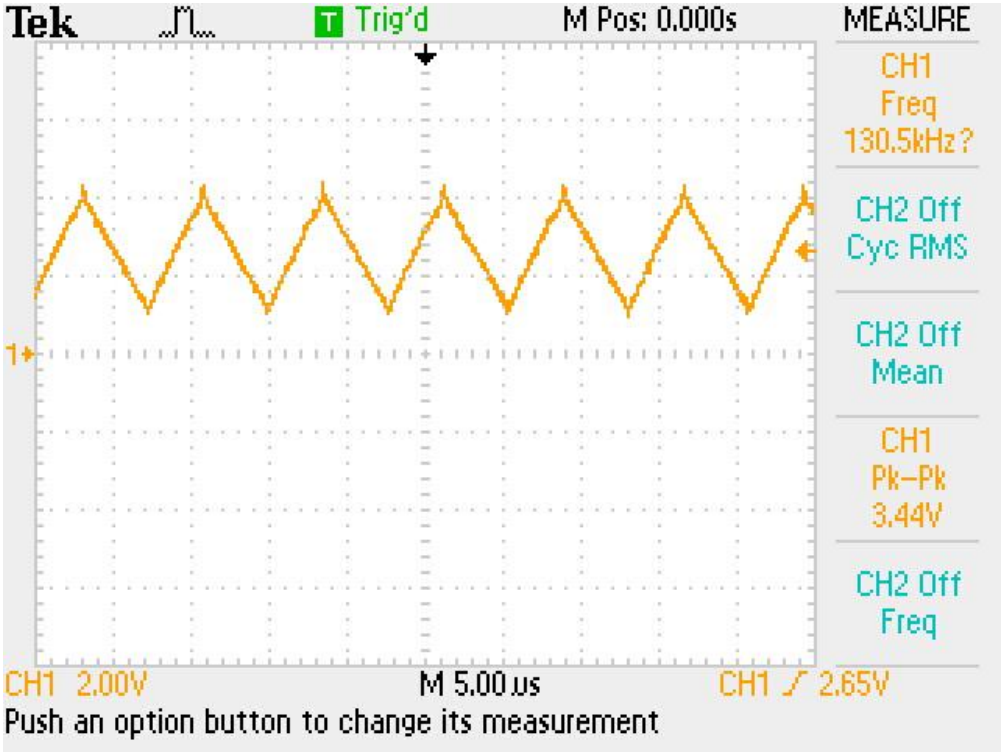

Figure 17: Triangle wave at 130kHz

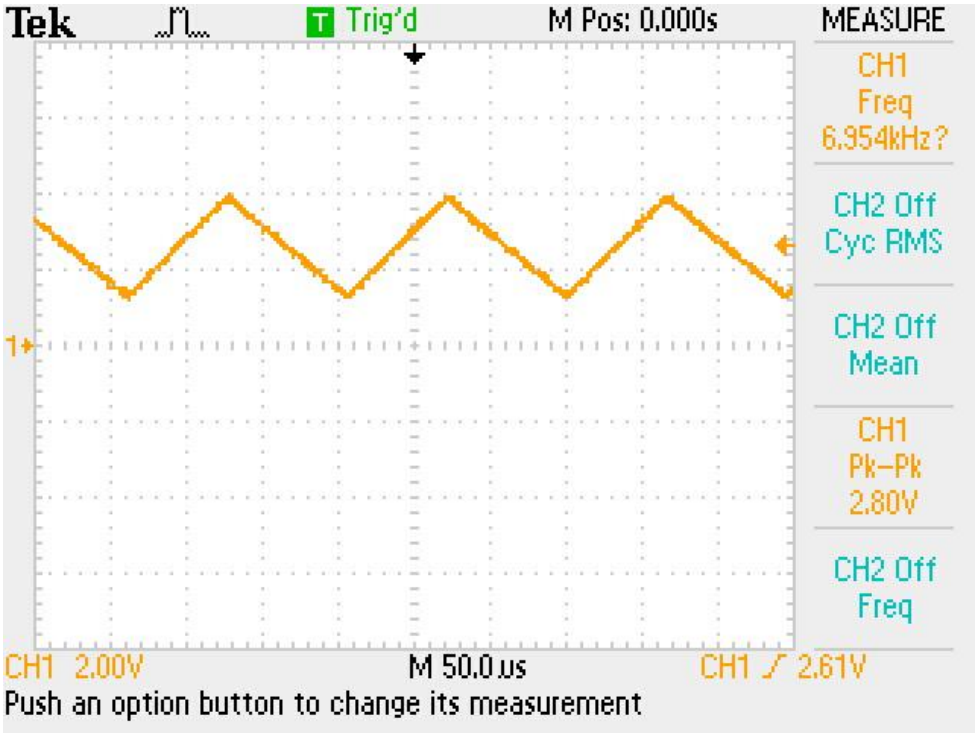

Figure 18: Triangle wave at 6kHz