UNIVERSIDADE PRESBITERIANA MACKENZIE
Faculdade de Computação e Informática

FCI – Faculdade de Computação e Informática

PROJETO 2 - AB&CD

DESCRITIVO TÉCNICO

Unidade Lógica e Aritmética de 8 bits

André Philipe Andriotti de Moraes
RA: 32013965

Gabriel Kazuiti Aiura
RA: 32047231

Índice

1. Apresentação

A Unidade Lógica e Aritmética (ULA) é um circuito digital que realiza operações lógicas e aritméticas, este compõe o bloco funcional fundamental de uma Unidade Central de Processamento (CPU).

Atualmente, todas as CPU's contêm ULA's e uma unidade de controle (UC). As operações efetuadas pela CPU são executadas pela ULA, que armazenam dados do registro de entrada.

O funcionamento da ULA depende da UC, que após registrar as entradas e compartilhar os dados com a ULA, permite que o circuito digital seja capaz de realizar operações diversas.

As ULA's atuam, principalmente, de duas maneiras diferentes, sendo estas adição e subtração. Além disso, pode atuar como outras portas lógicas, como NOT, AND, OR, XOR e realizar operações como deslocamento e comparação.

Link para o vídeo no YouTube: https://youtu.be/M_Xn-MVH2HU.

2. Descritivo Técnico

Este projeto consiste na construção de uma ULA de 8 bits. Para organizar sua montagem, o desenvolvimento é dividido em três fases:

- **Unidade Aritmética:** baseada no somador paralelo completo (CI 74HC283) para as operações de soma e subtração.
- **Unidade Lógica:** circuitos combinatórios baseados em circuitos integrados de portas lógicas e Multiplexadores.
- **Unidade Lógica e Aritmética:** a combinação das fases 1 e 2, unificando as entradas X_i,Y_i, variáveis de seleção S_i e as saídas G_i.

Tabela 1: Operações realizadas pela Unidade Aritmética

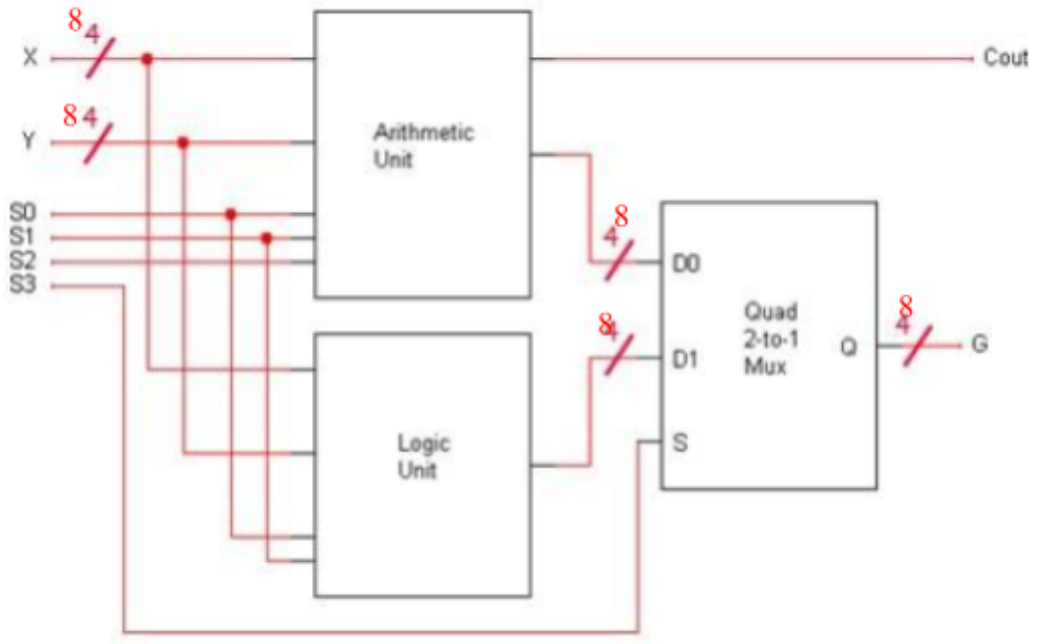
S_3	S_2	S_1	S_0	Operações
x	0	0	0	G = X
x	0	0	1	G = X + 1
x	0	1	0	G = X + Y
x	0	1	1	G = X + Y + 1

x	1	0	0	G = X + Y'
x	1	0	1	G = X + Y' + 1
x	1	1	0	G = X - 1
x	1	1	1	G = X

Tabela 2: Operações realizadas pela Unidade Lógica

S_3	S_2	S_1	S_0	Operações
x	x	0	0	G = X and Y
x	x	0	1	G = X or Y
x	x	1	0	G = X $\otimes$ Y
x	x	1	1	G = X'

Figura 1: Diagrama funcional da ULA



Entradas:

X_i: operando de 8 bits (X_7 X_6 X_5 X_4 X_3 X_2 X_1 X_0);
Y_i: operando de 8 bits (Y_7 Y_6 Y_5 Y_4 Y_3 Y_2 Y_1 Y_0);

S_i: variáveis de seleção de operação ($S_3S_2S_1S_0$).

Saídas:

G_i: resultado de 8 bits da operação gerada pela ULA ($G_7G_6G_5G_4G_3G_2G_1G_0$).
C_{OUT}: carry out ou G_8, somente válido para operações aritméticas.

Logo, observa-se que a variável de seleção S_3 controla qual tipo de operação será aplicada: Se S_3 não for ativado, serão realizadas operações aritméticas, porém se S_3 for ativado, serão realizadas operações lógicas.

A ULA projetada pode executar as seguintes operações, de acordo com as variáveis de seleção S_i, apresentadas na tabela a seguir:

Tabela 3: Operações realizadas pela ULA

S_3	S_2	S_1	S_0	Operações
0	0	0	0	G = X
0	0	0	1	G = X + 1
0	0	1	0	G = X + Y
0	0	1	1	G = X + Y + 1
0	1	0	0	G = X + Y’
0	1	0	1	G = X + Y’ + 1
0	1	1	0	G = X - 1
0	1	1	1	G = X
1	x	0	0	G = X and Y
1	x	0	1	G = X or Y
1	x	1	0	G = X $\otimes$ Y
1	x	1	1	G = X’

Sendo:

$S_3S_2S_1S_0$: variáveis de seleção;

Operações: operação a ser executada;
x: valor irrelevante.

Para a Unidade Aritmética, foram utilizados os seguintes componentes:

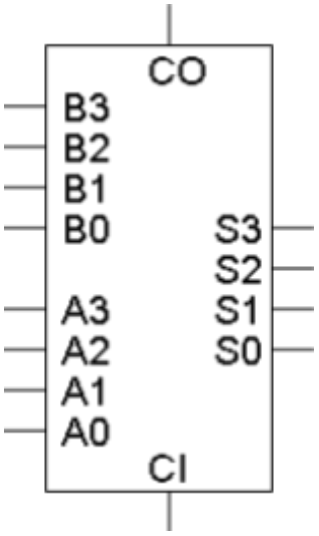
- C.I. 74HC08: circuito integrado de portas lógicas AND.
- C.I. 74HC32: circuito integrado de portas lógicas OR.
- C.I. 74HC04: circuito integrado de portas lógicas NOT
- C.I. 74HC283: somador completo de 4 bits.

Para a Unidade Lógica, foram utilizados os seguintes componentes:

- C.I. 74HC08: circuito integrado de portas lógicas AND.
- C.I. 74HC32: circuito integrado de portas lógicas OR.
- C.I. 74HC86: circuito integrado de portas lógicas XOR.
- C.I. 74HC04: circuito integrado de portas lógicas NOT
- C.I. 74LS253: multiplexador 4x1.

Portanto, para a combinação de ambas as unidades (ULA), foram utilizados os mesmos componentes, além de multiplexadores 2x1 (C.I. 74HC257).

Figura 2: Circuito lógico do somador completo (74HC283)

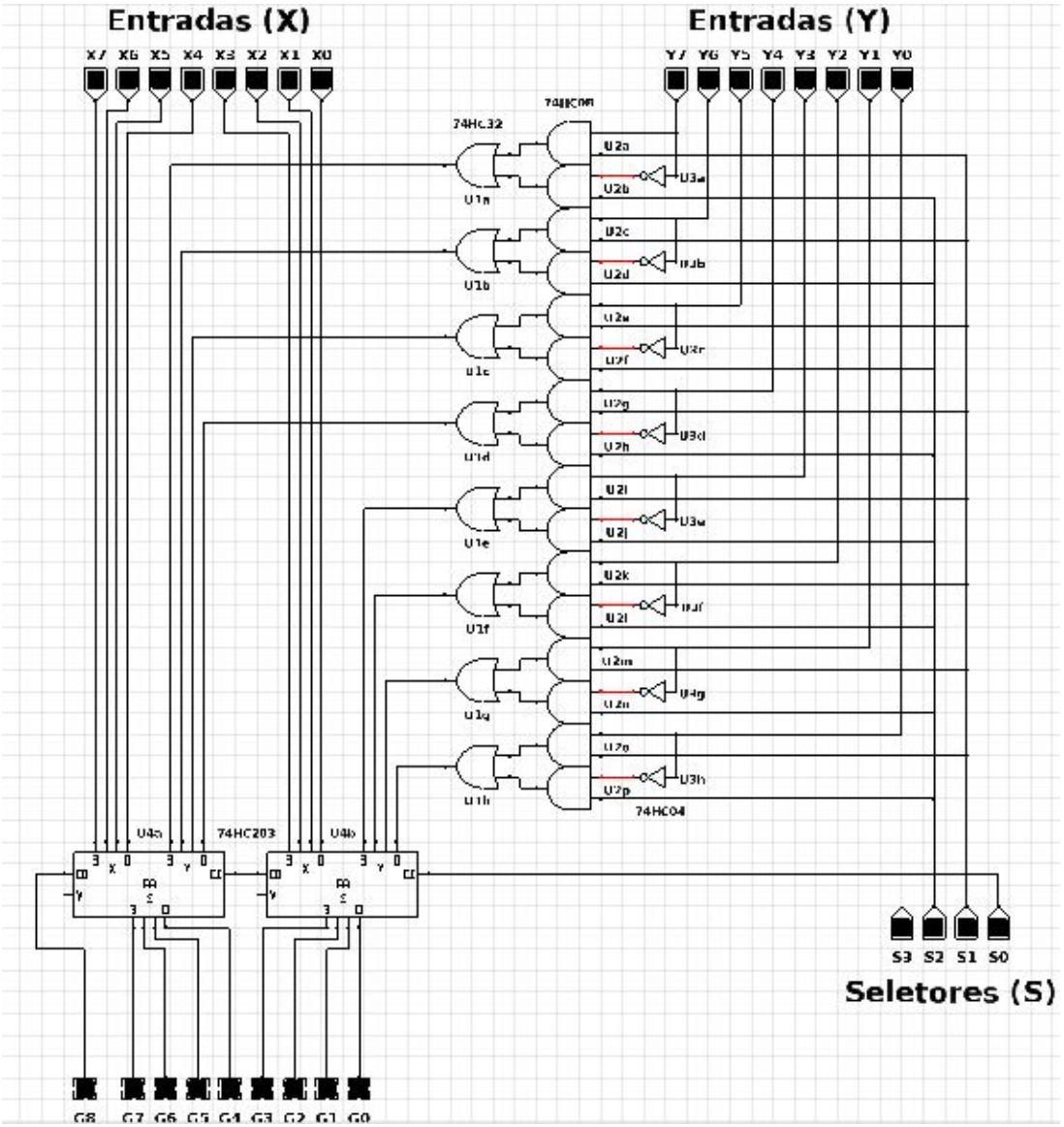


Esse componente é a base para realizar as operações aritméticas, onde A_i e B_i são entradas de 4 bits, C_i é o Carry In e C_o é o Carry Out, conforme a seguinte fórmula: **S = A + B + CI**.

3. Elaboração do projeto

3.1 Fase 1: Unidade Aritmética

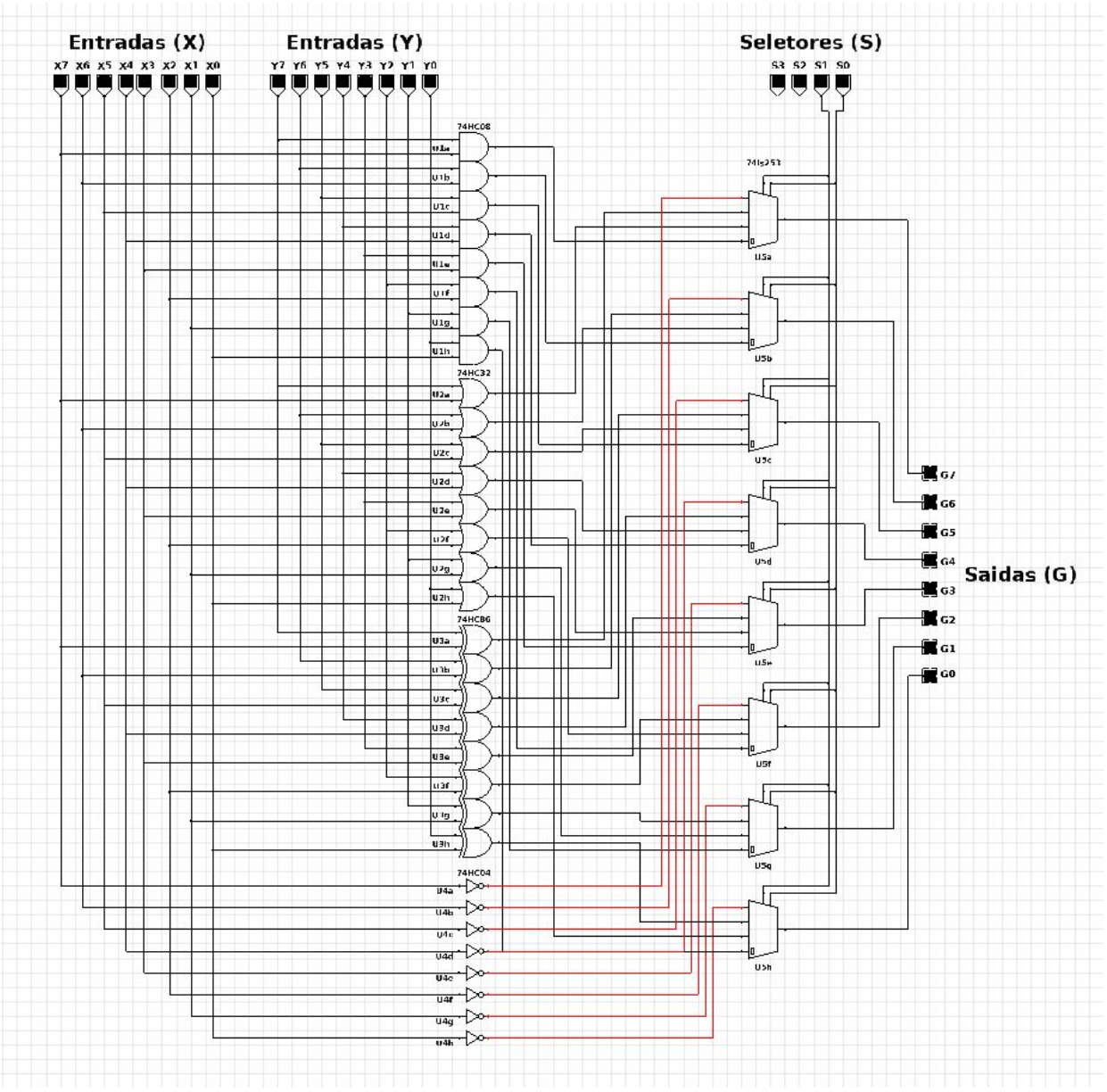
Figura 3: Unidade Aritmética implementada no CEDAR



Durante a fase 1 do projeto, utilizamos como entradas os valores X_i e Y_i, que são compilados e armazenados por meio de um somador completo, os quais são ligados a várias portas lógicas (AND, OR e NOT) seria capaz de realizar operações de acordo com a variável seletora (S_i) e emitir uma saída de 8 bits (G_i). A ferramenta essencial para o funcionamento do projeto é essa combinação de portas lógicas, que ao conectar as entradas de Y e o valor inserido em S_0, S_1 e S_2, é capaz de realizar diferentes funções, como soma de X+Y, X+1, X+Y+1, dentre outras operações apresentadas na tabela x.

3.2 Fase 2: Unidade Lógica

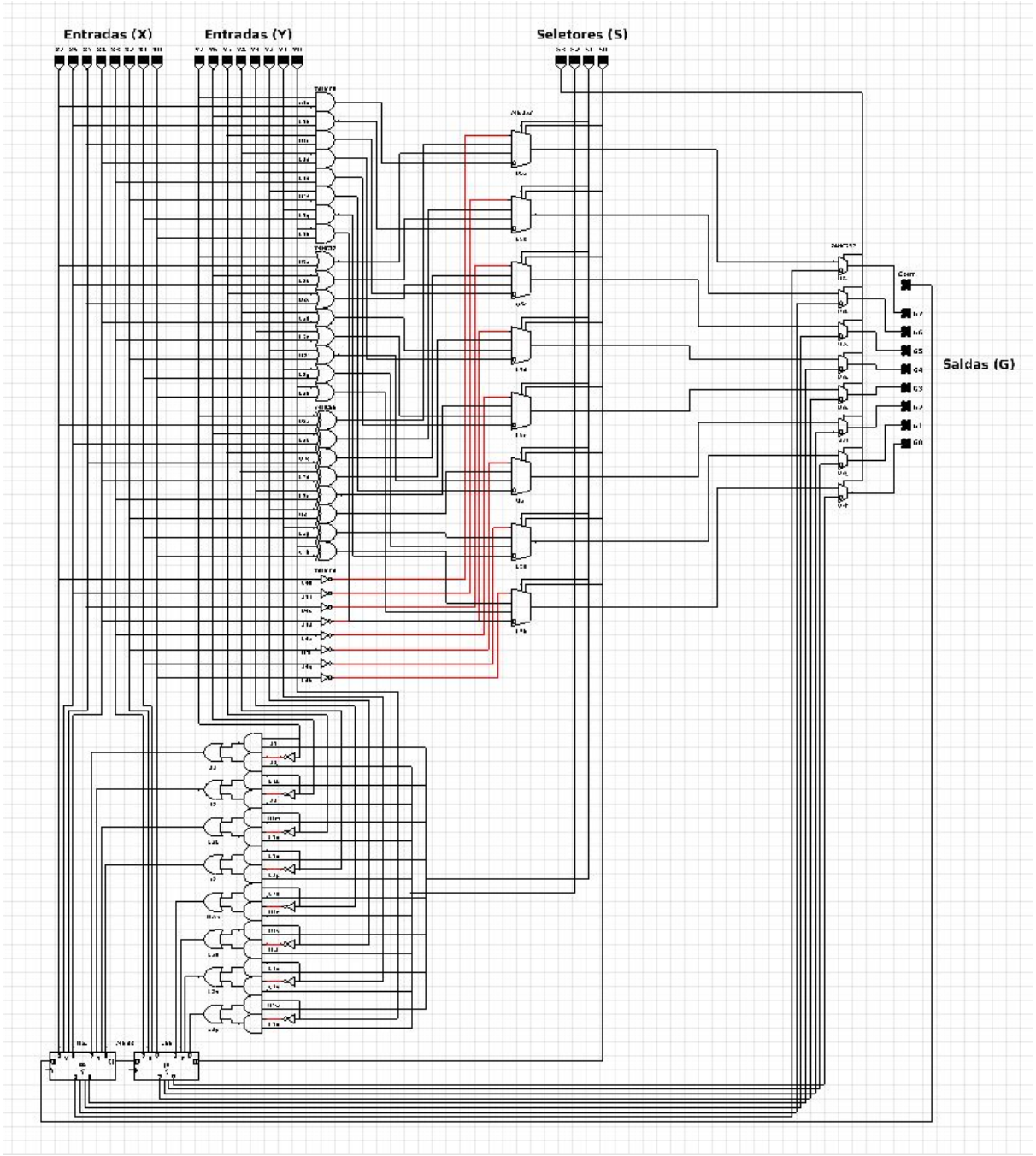
Figura 4: Unidade Lógica implementada no CEDAR



Na fase 2 do projeto, utilizamos como entradas X e Y, onde cada X_i e Y_i estão ligados a uma porta lógica AND, OR, NOT e XOR. Então, para compilar as informações transmitidas, fez-se necessário utilizar um multiplexador de 4 entradas, o qual recebia a saída de cada uma das portas lógicas. Dessa forma, é possível realizar diferentes operações as quais são influenciados pelo valor inserido nos seletores (S_i), conectados aos MUX para instruir qual operação este realizará com os dados recebidos através das portas lógicas, este é capaz de realizar operações impossíveis de efetuar na fase 1 do projeto, como por exemplo, G = X $\otimes$ Y, G = X or Y, G = X and Y.

3.3 Fase 3: Integração Unidade Lógica e Aritmética

Figura 5: Unidade Lógica e Aritmética implementada no CEDAR



A fase 3 do projeto, recebe os dados coletados pela fase 1 e fase 2 por meio de um multiplexador de 2 entradas, assim, compilando os dados recebidos este realizará as operações de acordo com os valores nos seletores (S_i), diferente das outras fases. Nesta etapa do projeto, é possível realizar tanto as operações da fase 1, quanto as operações da fase 2.

4. Simulações e avaliação de resultados

4.1 Fase 1: Unidade Aritmética

Tabela 4: Testes realizados na Fase 1 (Unidade Aritmética)

S3 S2 S1 S0	Operação	X($X_7X_6X_5X_4X_3X_2X_1X_0$)	Y($Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$)	Resultado ($G_8G_7G_6G_6G_5G_4G_3G_2G_1G_0$)
0 0 0 0	G = X	00001001	00010010	000001001
0 0 0 1	G = X+1	00001111	00001000	000010000
0 0 1 0	G = X+Y	00001111	00001000	000010111
0 0 1 1	G = X + Y + 1	00001111	00001000	000011000
0 1 0 0	G = X + Y'	00001111	00001000	100000110
0 1 0 1	G = X + Y' + 1	00001111	00001100	100000011
0 1 1 0	G = X - 1	00001111	00001100	100001110
0 1 1 1	G = X	00011111	00001100	100011111

Figura 6: Seleção 0000 - Operação: G = X

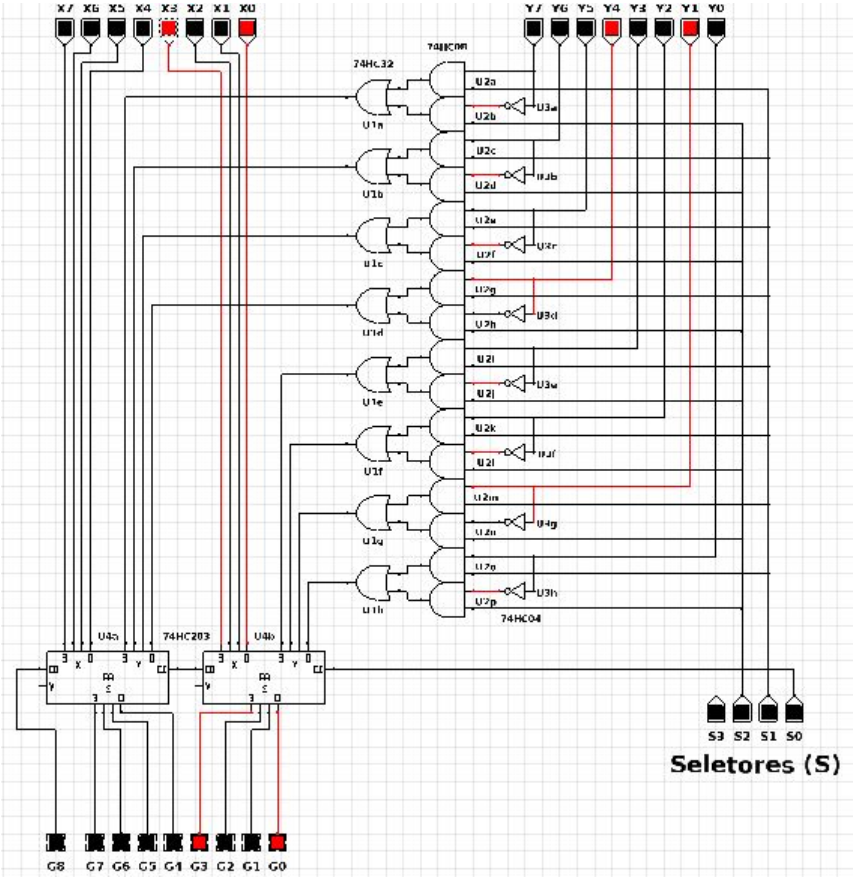


Figura 7: Seleção 0001 - Operação: G = X + 1

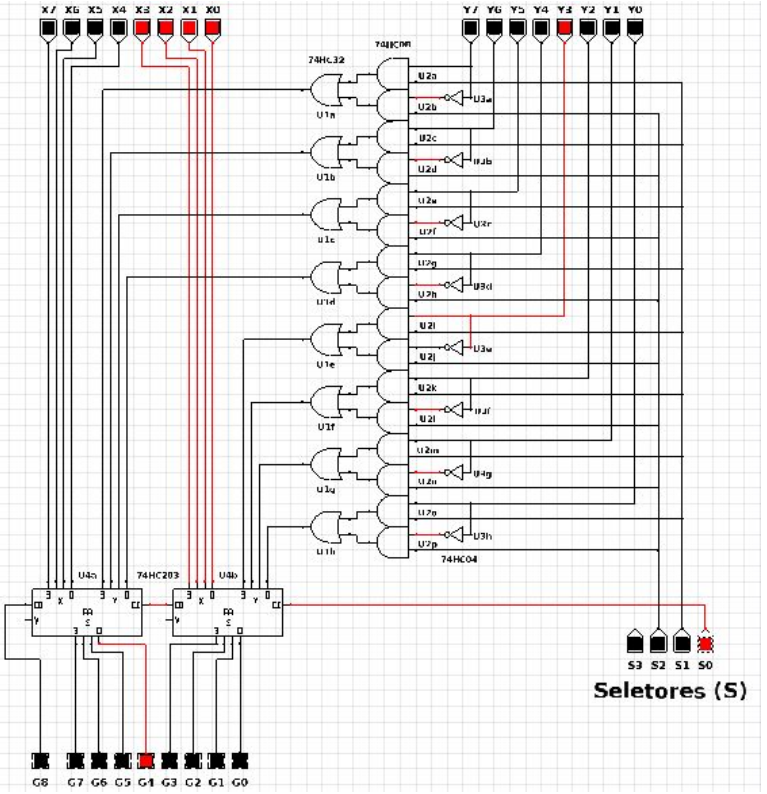


Figura 8: Seleção 0010 - Operação: G = X + Y

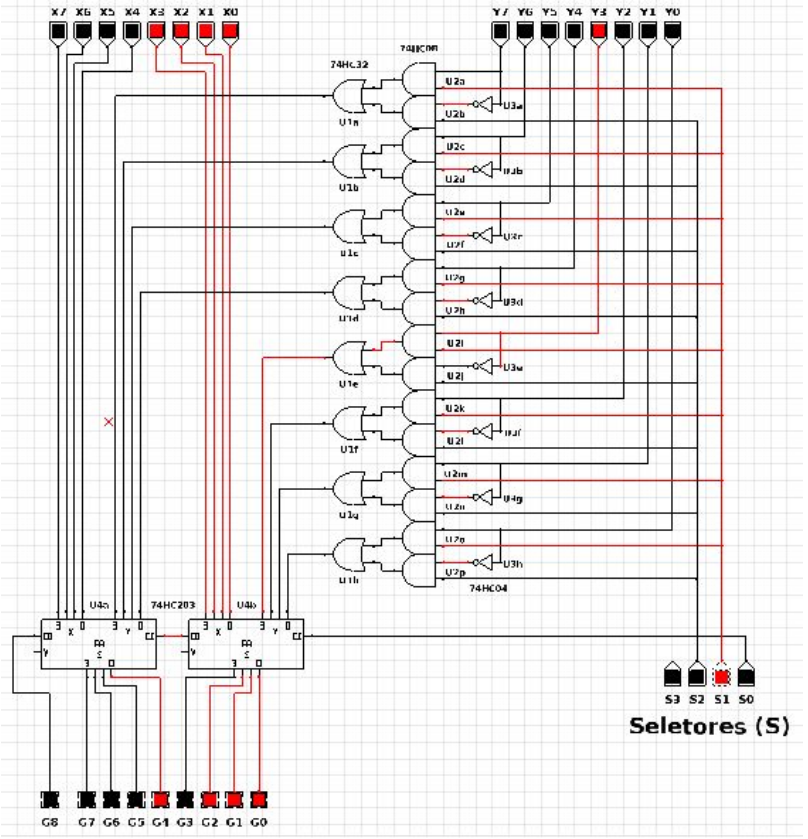


Figura 9: Seleção 0011 - Operação: G = X + Y + 1

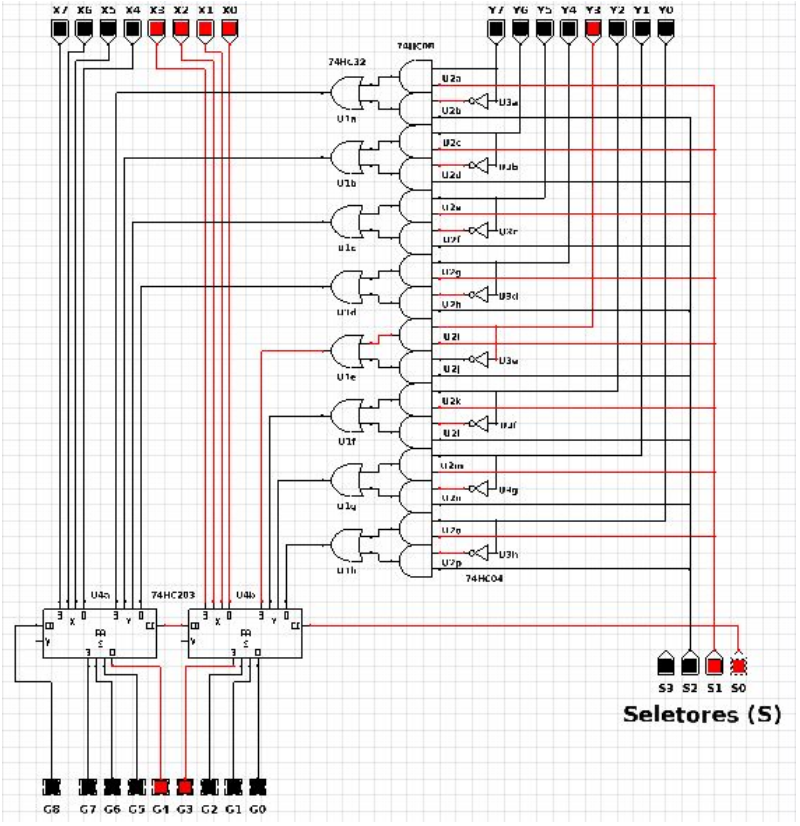


Figura 10: Seleção 0100 - Operação: G = X + Y'

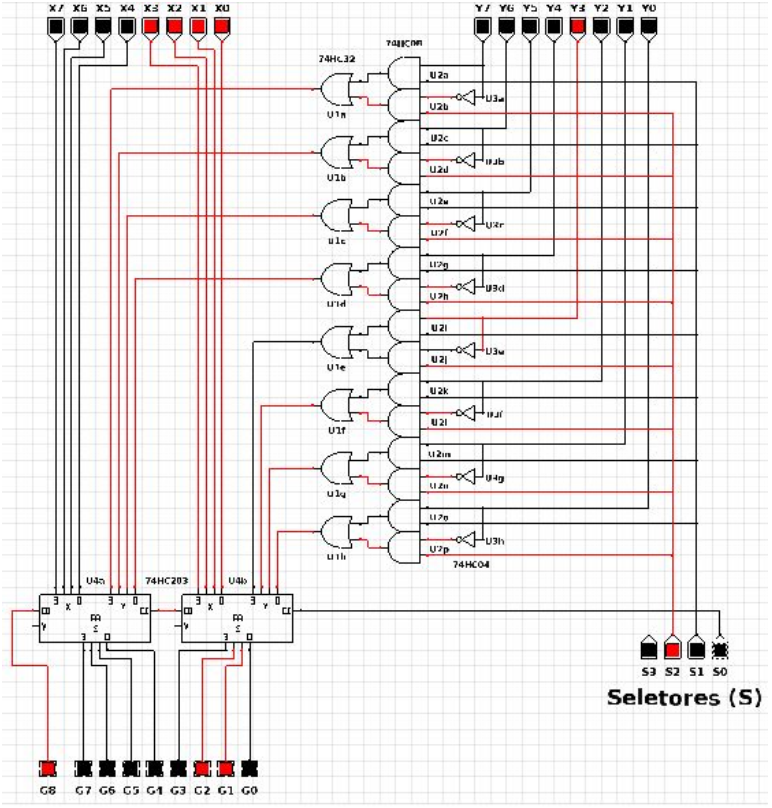


Figura 11: Seleção 0101 - Operação: G = X + Y' + 1

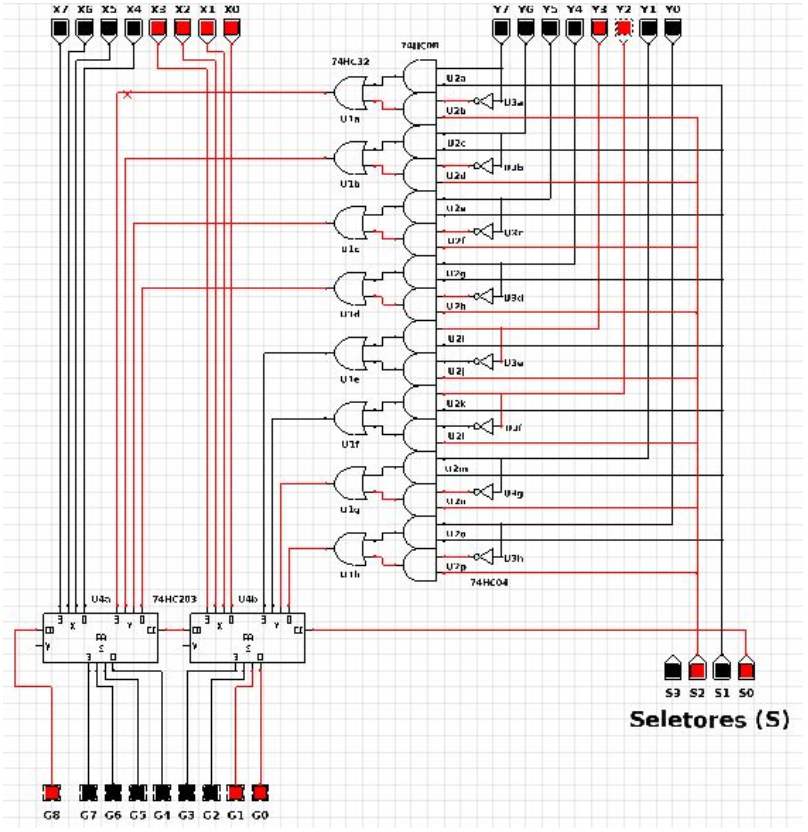


Figura 12: Seleção 0110 - Operação: G = X - 1

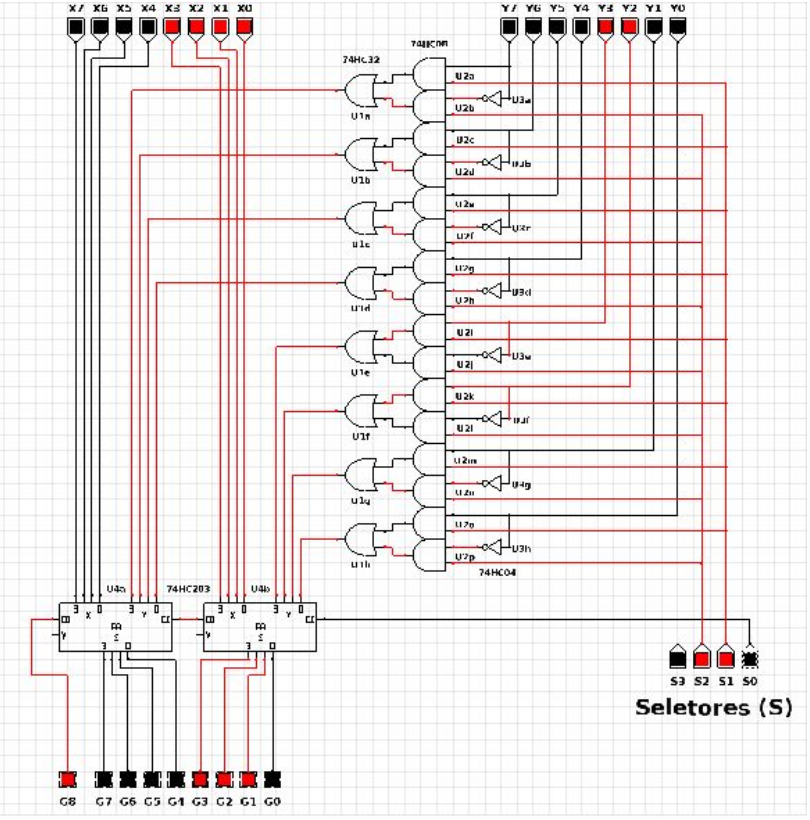
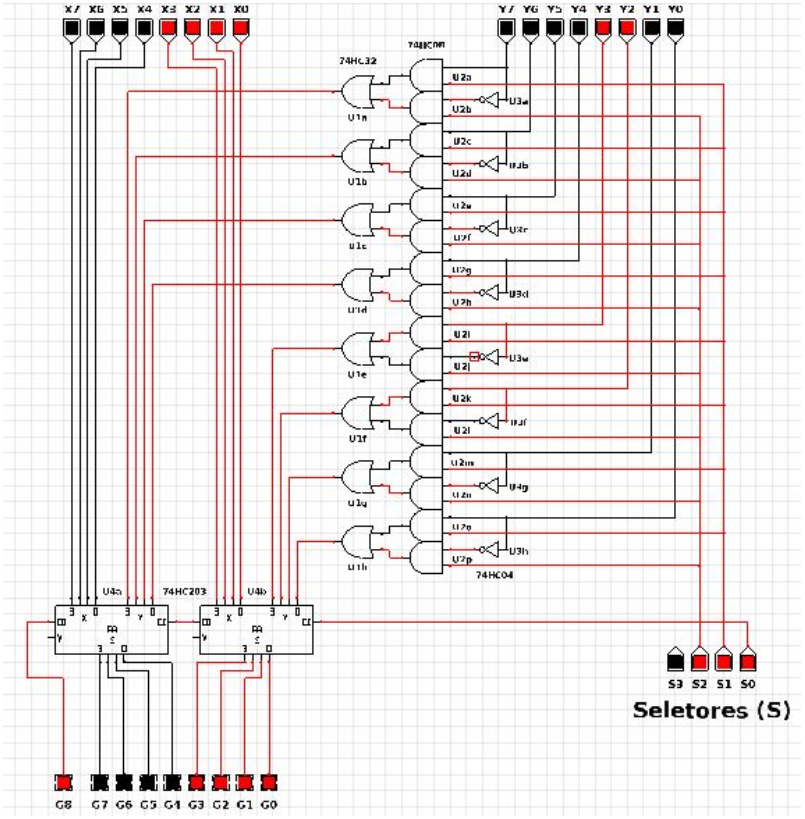


Figura 13: Seleção 0111 - Operação: G = X



4.2 Fase 2: Unidade Lógica

Tabela 5: Testes realizados na Fase 2 (Unidade Lógica)

S3 S2 S1 S0	Operação	X($X_7X_6X_5X_4X_3X_2X_1X_0$)	Y($Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$)	Resultado ($G_7G_6G_6G_5G_4G_3G_2G_1G_0$)
0 0 0 0	G = X and Y	01000011	00001111	00000011
0 0 0 1	G = X or Y	01010100	00001101	00000001
0 0 1 0	G = X $\otimes$ Y	01010100	00000010	00000110
0 0 1 1	G = X'	01010100	00001101	10101011

Figura 14: Seleção = 0000 - Operação: G = X and Y

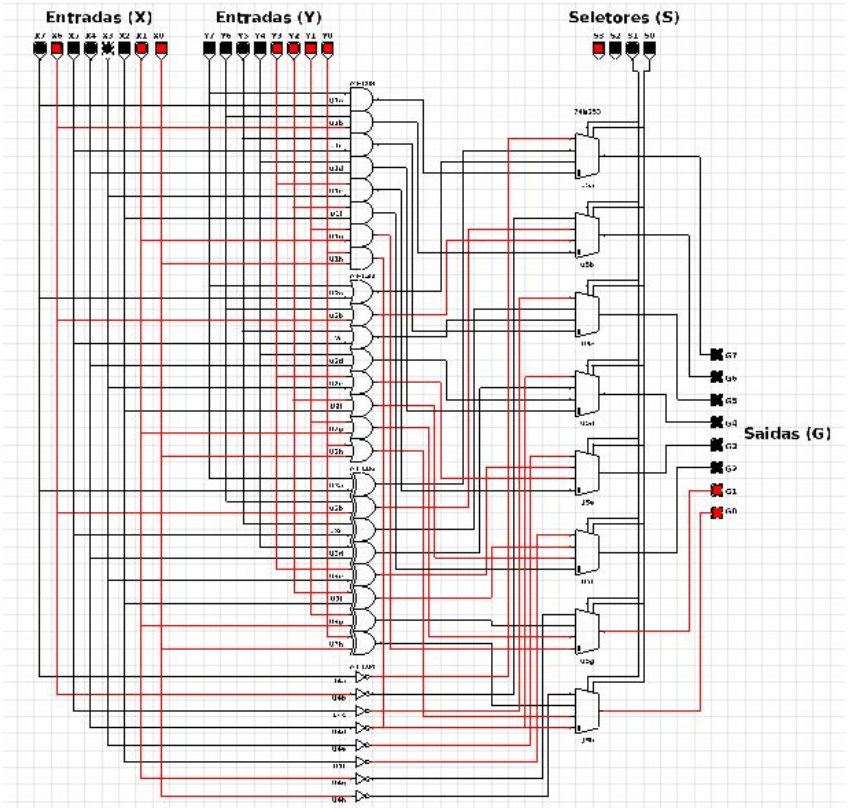


Figura 15: Seleção = 0001 - Operação: G = X or Y

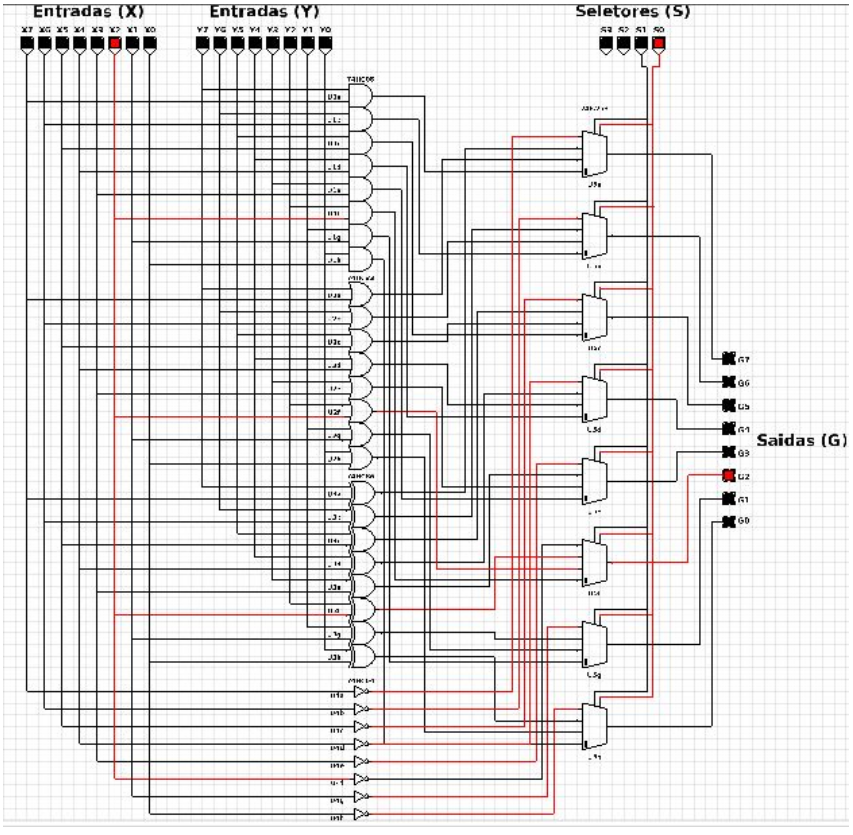


Figura 16: Seleção 0010 - Operação: G = X ⊗ Y

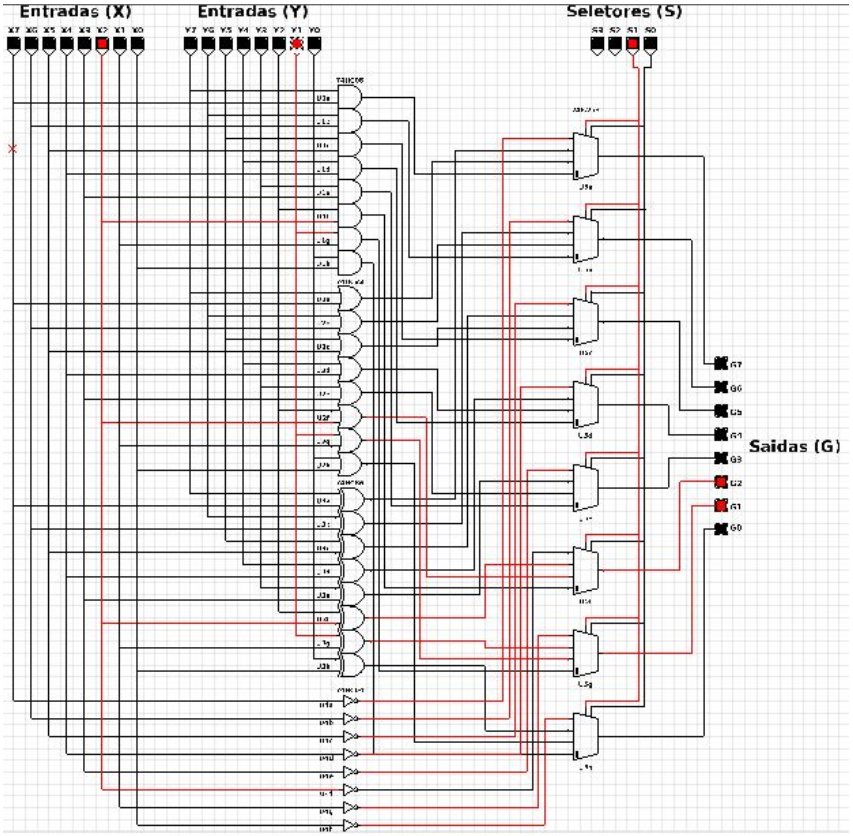
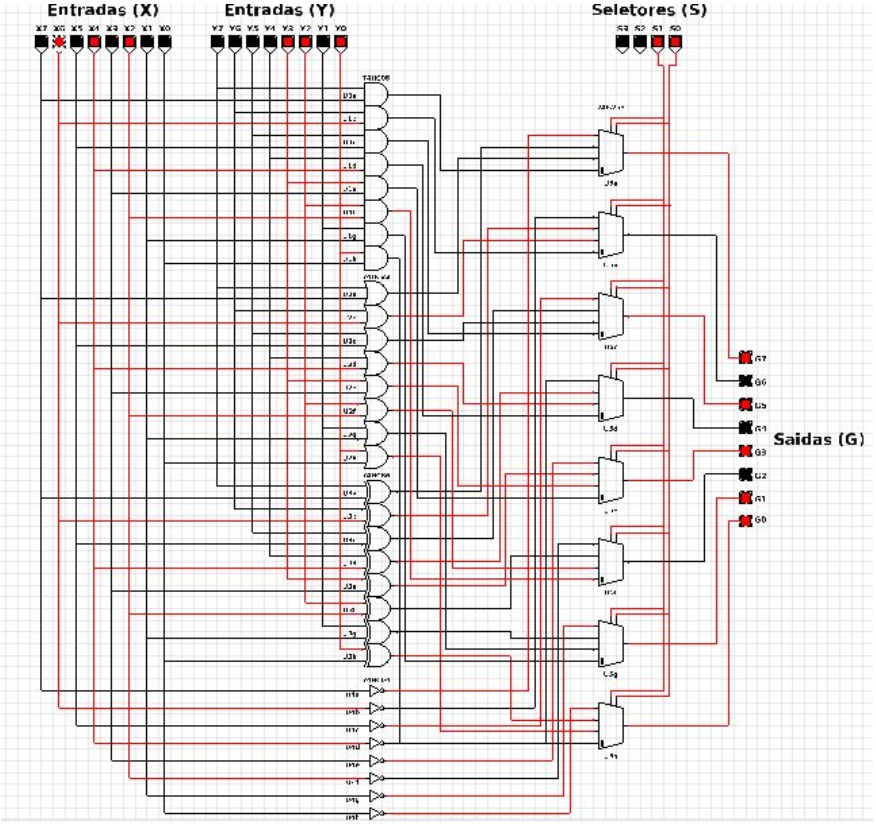


Figura 17: Seleção 0011 - Operação: G = X'



4.3 Fase 3: Integração Unidade Lógica e Aritmética

Tabela 6: Testes realizados na Fase 3 (Unidade Lógica e Aritmética)

S3 S2 S1 S0	Operação	X($X_7X_6X_5X_4X_3X_2X_1X_0$)	Y($Y_7Y_6Y_5Y_4Y_3Y_2Y_1Y_0$)	Resultado ($G_{COUT}G_7G_6G_6G_5G_4G_3G_2G_1G_0$)
0 0 0 0	G = X	01100110	00101010	001100110
0 0 0 1	G = X+1	01100110	00101010	001100111
0 0 1 0	G = X+Y	01100110	00101010	010010000
0 0 1 1	G = X + Y + 1	01100110	00101010	010010001
0 1 0 0	G = X + Y'	01100110	00101010	100111011
0 1 0 1	G = X + Y' + 1	01100110	00101010	100111100
0 1 1 0	G = X - 1	01100110	00101010	101100101
0 1 1 1	G = X	01100110	00101010	101100110
1 x 0 0	G = X and Y	10010010	01100111	000000010
1 x 0 1	G = X or Y	10010010	01100111	011110111
1 x 1 0	G = X ⊗ Y	10010010	01100111	011110101
1 x 1 1	G = X'	10010010	01100111	001101101

Figura 18: Seleção 0000 - Operação: G = X

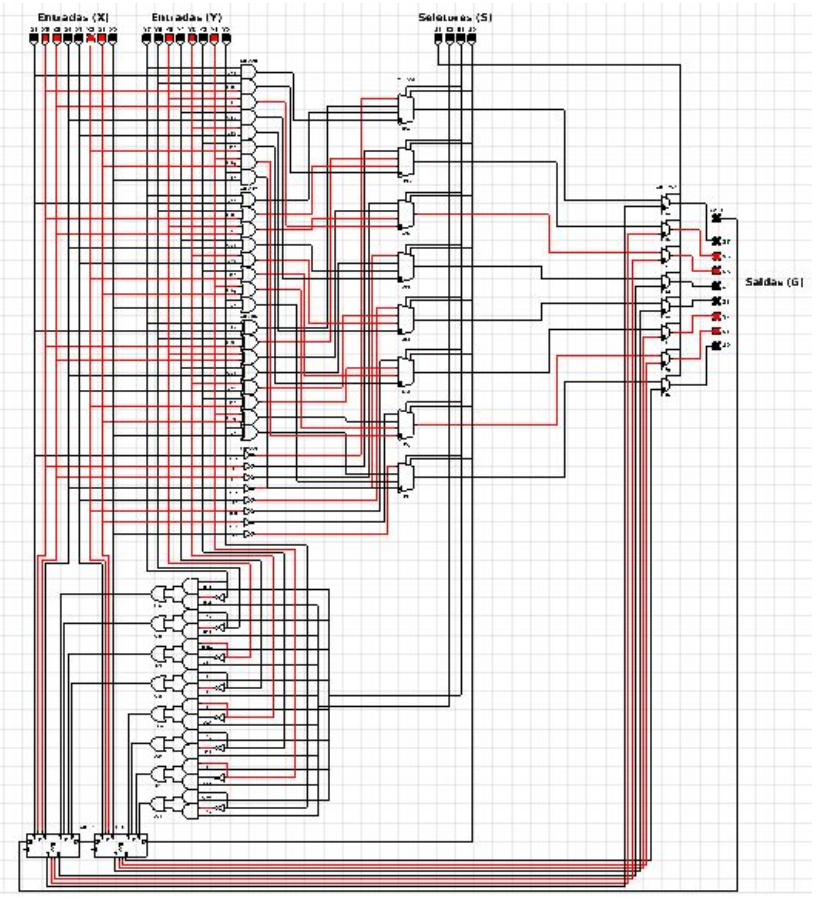


Figura 19: Seleção 0001 - Operação: G = X + 1

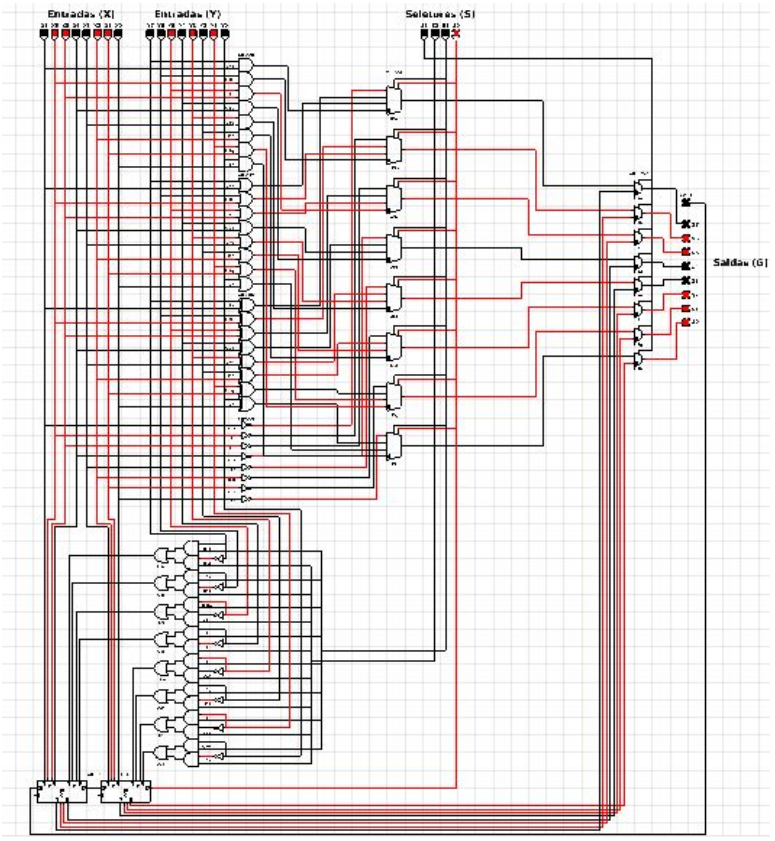


Figura 20: Seleção 0010 - Operação: G = X + Y

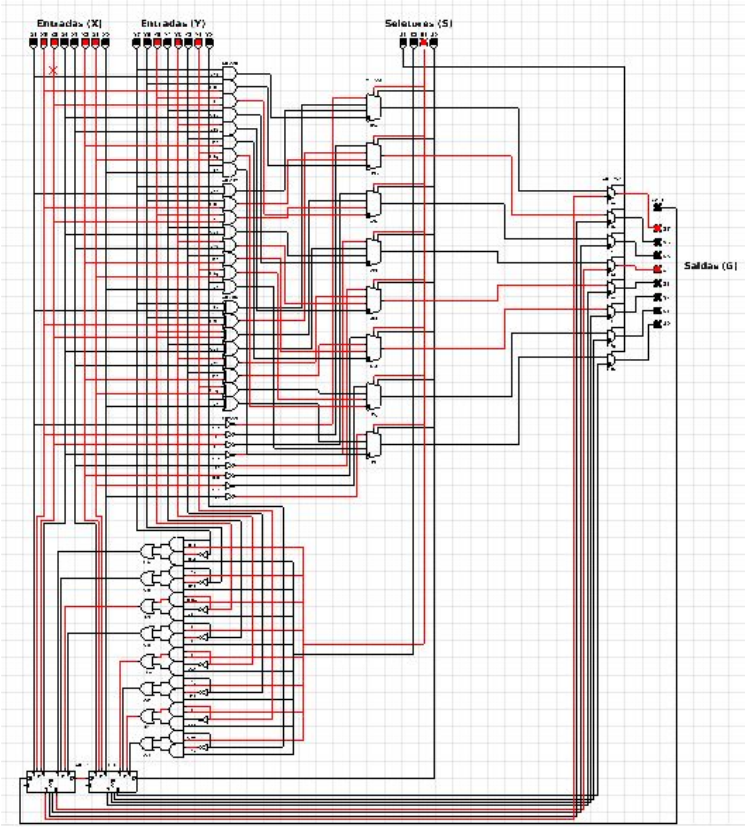


Figura 21: Seleção 0011 - Operação: G = X + Y + 1

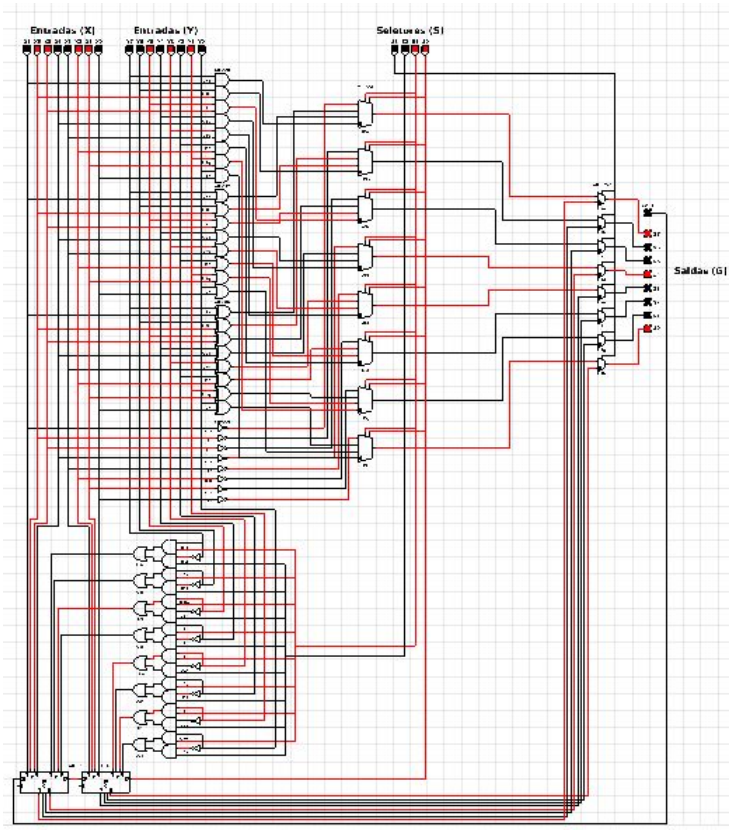


Figura 22: Seleção 0100 - Operação: G = X + Y'

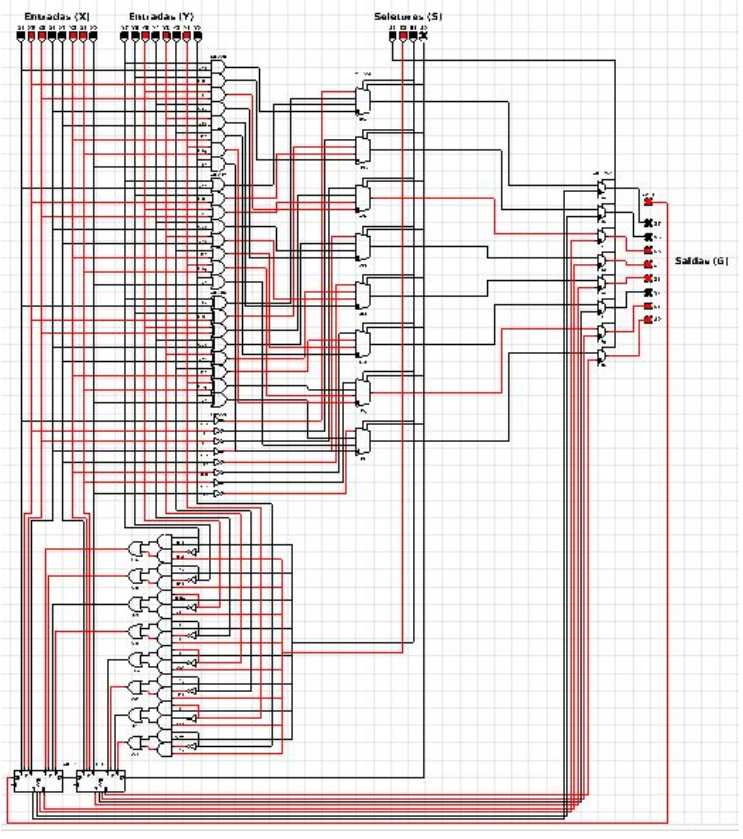


Figura 23: Seleção 0101 - Operação: G = X + Y' + 1

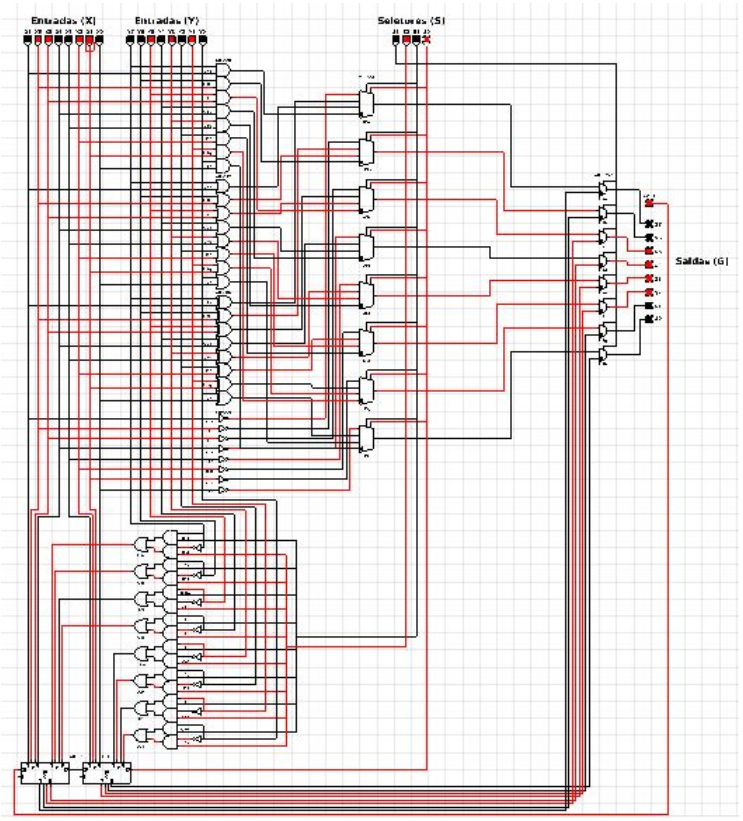


Figura 24: Seleção 0110 - Operação: G = X - 1

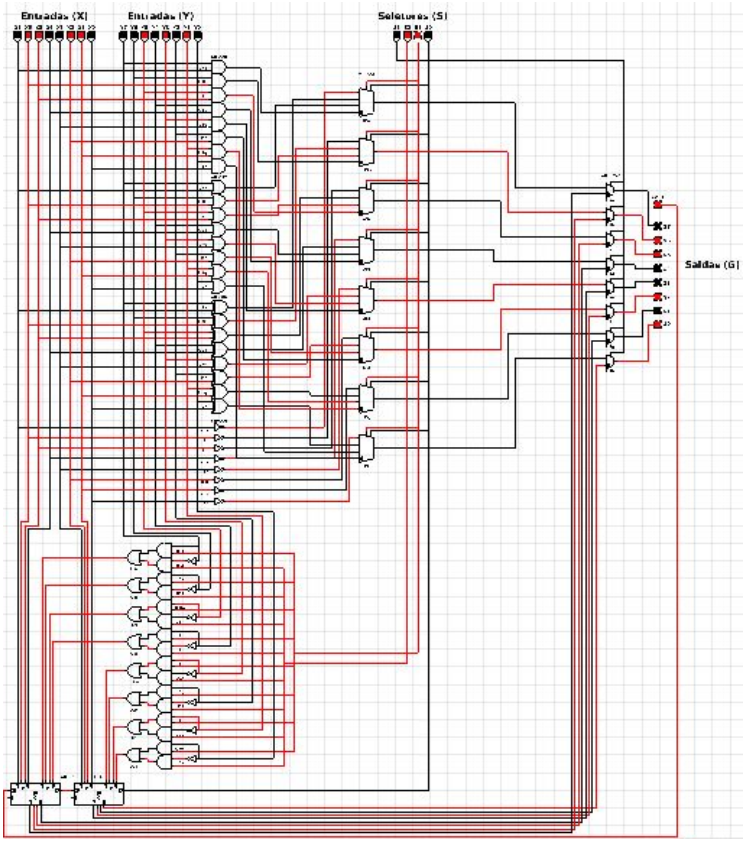


Figura 25: Seleção 0111 - Operação: G = X

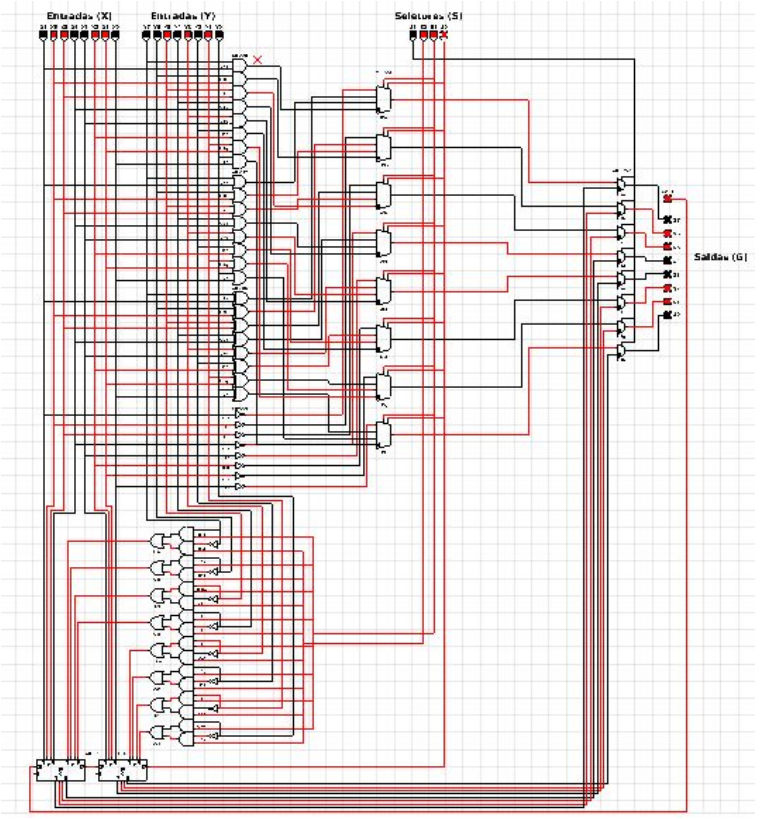


Figura 26: Seleção 1000 - Operação: G = X and Y

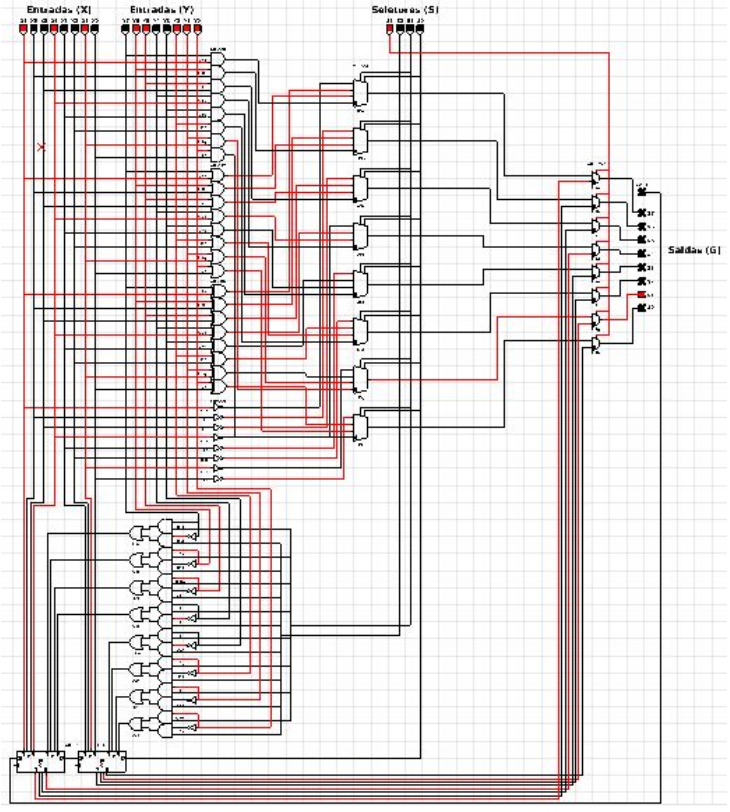


Figura 27: Seleção 1001 - Operação: G = X or Y

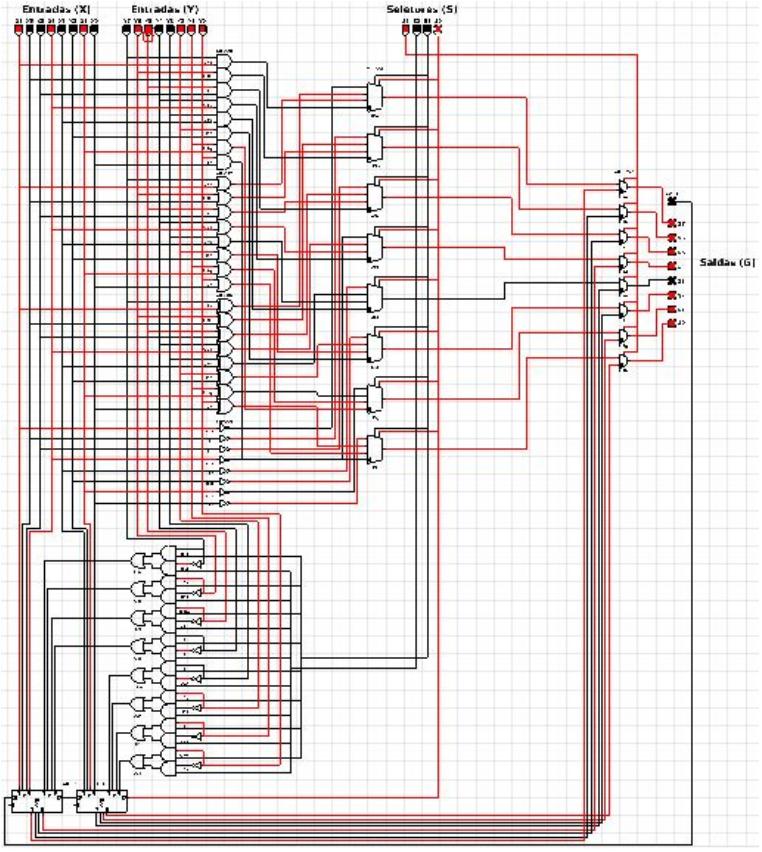


Figura 28: Seleção 1010 - Operação: G = X ⊗ Y

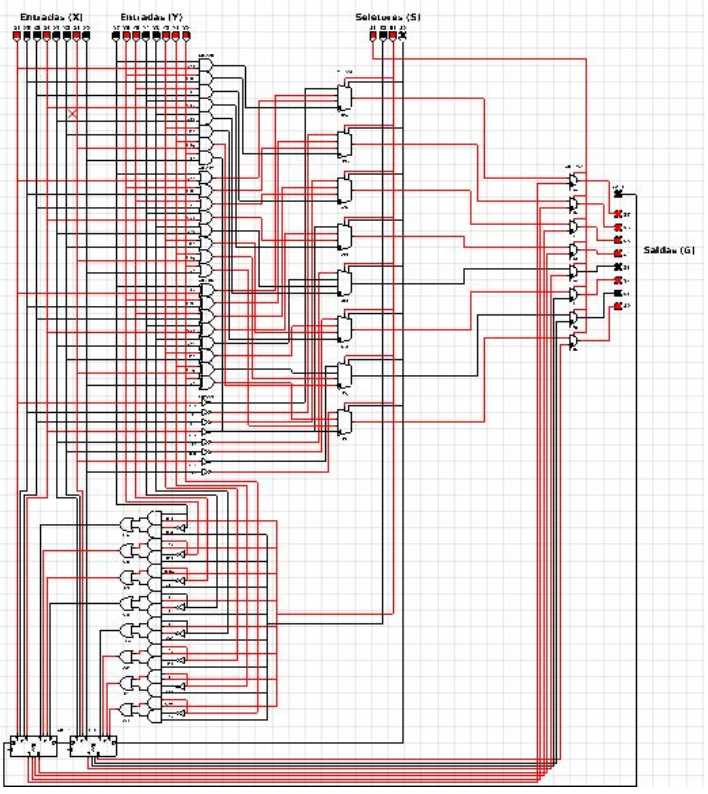
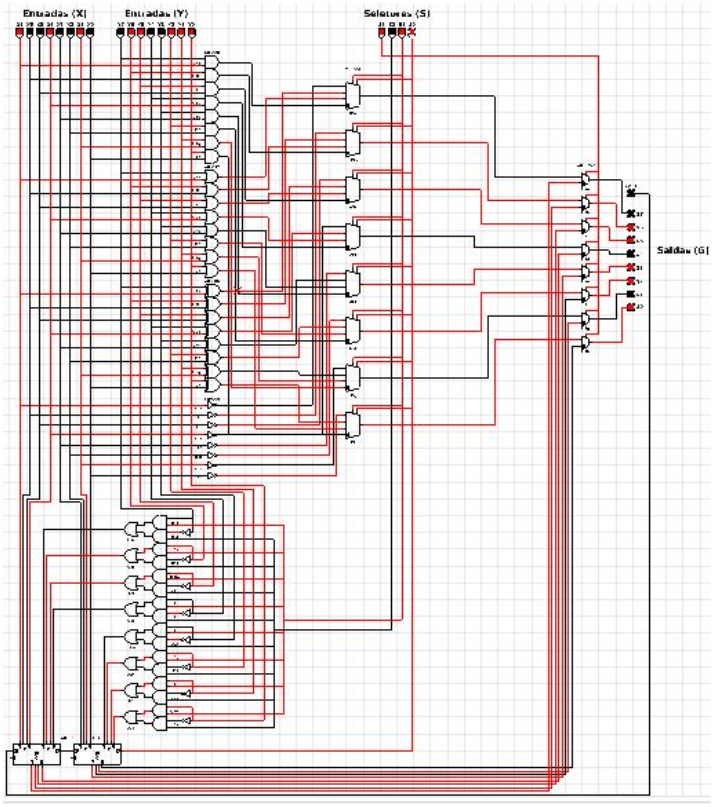


Figura 29: Seleção 1011 - Operação: G = X'



5. Referências Bibliográficas

74HC04 Datasheet (PDF) - NXP Semiconductors. [*S. l.*]: PHILIPS [NXP Semiconductors], 23 jul. 2003. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/106274/PHILIPS/74HC04.html>. Acesso em: 13 nov. 2020.

74HC08 Datasheet (PDF) - NXP Semiconductors. [*S. l.*]: PHILIPS [NXP Semiconductors], 25 jul. 2003. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/104081/PHILIPS/74HC08.html>. Acesso em: 13 nov. 2020.

74HC32 Datasheet (PDF) - Silicon Supplies. [*S. l.*]: SS [Silicon Supplies], 7 fev. 2019. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/1144810/SS/74HC32.html>. Acesso em: 13 nov. 2020.

74HC86 Datasheet (PDF) - NXP Semiconductors. [*S. l.*]: PHILIPS [NXP Semiconductors], dez. 1990. Disponível em:

<https://pdf1.alldatasheet.com/datasheet-pdf/view/15668/PHILIPS/74HC86.html>. Acesso em: 13 nov. 2020.

74HC283 Datasheet (PDF) - NXP Semiconductors. [*S. l.*]: PHILIPS [NXP Semiconductors], 11 nov. 2004. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/109543/PHILIPS/74HC283.html>. Acesso em: 13 nov. 2020.

74LS253 Datasheet (PDF) - Fairchild Semiconductor. [*S. l.*]: FAIRCHILD [Fairchild Semiconductor], ago. 1986. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/51058/FAIRCHILD/74LS253.html> . Acesso em: 13 nov. 2020.

74HC257 Datasheet (PDF) - NXP Semiconductors. [*S. l.*]: PHILIPS [NXP Semiconductors], 30 set. 1998. Disponível em: <https://pdf1.alldatasheet.com/datasheet-pdf/view/86441/PHILIPS/74HC257.html>. Acesso em: 13 nov. 2020.

6. Anexos

Figura 30: Datasheet do C.I. 74HC04 (NOT)

Hex inverter 74HC04; 74HCT04

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC04			74HCT04			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	–40	+25	+125	–40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

PINNING

PIN	SYMBOL	DESCRIPTION
1	1A	data input
2	1Y	data output
3	2A	data input
4	2Y	data output
5	3A	data input
6	3Y	data output
7	GND	ground (0 V)
8	4Y	data output
9	4A	data input
10	5Y	data output
11	5A	data input
12	6Y	data output
13	6A	data input
14	V_{CC}	supply voltage

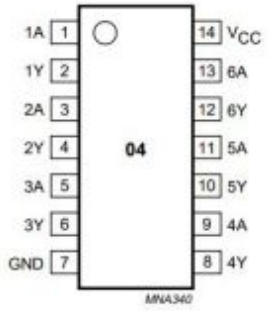


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.

Figura 31: Datasheet do C.I. 74HC08 (AND)

Quad 2-input AND gate 74HC08; 74HCT08

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	74HC08			74HCT08			UNIT
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	–	V_{CC}	0	–	V_{CC}	V
V_O	output voltage		0	–	V_{CC}	0	–	V_{CC}	V
T_{amb}	ambient temperature	see DC and AC characteristics per device	−40	+25	+125	−40	+25	+125	°C
t_r, t_f	input rise and fall times	V_{CC} = 2.0 V	–	–	1000	–	–	–	ns
		V_{CC} = 4.5 V	–	6.0	500	–	6.0	500	ns
		V_{CC} = 6.0 V	–	–	400	–	–	–	ns

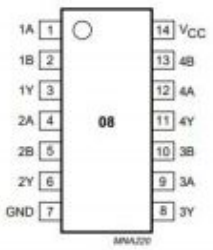
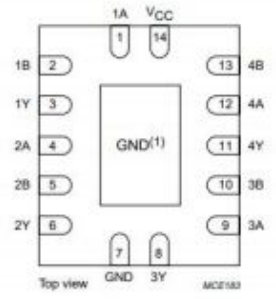


Fig.1 Pin configuration DIP14, SO14 and (T)SSOP14.



(1) The die substrate is attached to this pad using conductive die attach material. It can not be used as a supply pin or input.

Fig.2 Pin configuration DHVQFN14.

Figura 32: Datasheet do C.I. 74HC32 (OR)

High Speed CMOS Logic – 74HC32

Quad 2-Input OR Gate in bare die form

Rev 1.0
07/02/19

Description

The 74HC32 quad 2-input OR gate is fabricated on a .35µm CMOS process combining high speed LSTTL performance with CMOS low power. The device consists of four independent 2-input OR gates with standard push-pull outputs and performs the Boolean function $Y = \overline{\overline{A} \bullet \overline{B}}$ or Y = A + B. Device inputs are compatible with standard CMOS outputs; with pull-up resistors, they are compatible with LSTTL outputs. All inputs are protected against ESD and excess voltage transients.The die size is significantly smaller than industry peers due to its re-design and production using a more advanced CMOS process.

Features:

- Output Drive Capability: 10 LSTTL Loads
- Low Input Current: 1µA
- Outputs directly interface CMOS, NMOS and TTL
- Operating Voltage Range: 2V to 6V
- Function compatible with 74LS32
- High Noise Immunity CMOS process.

Rev 1.0
07/02/19

Absolute Maximum Ratings[1]

PARAMETER	SYMBOL	VALUE	UNIT
DC Supply Voltage (Referenced to GND)	V_{CC}	-0.5 to +7.0	V
DC Input Voltage (Referenced to GND)	V_{IN}	-0.5 to V_{CC} +0.5	V
DC Output Voltage (Referenced to GND)	V_{OUT}	-0.5 to V_{CC} +0.5	V
DC Input Current	I_{IN}	±20	mA
DC Output Current, per pad	I_{OUT}	±25	mA
DC Supply Current, V_{CC} or GND, per pad	I_{CC}	±50	mA
Power Dissipation in Still Air[2]	P_D	750	mW
Storage Temperature Range	T_{STG}	-65 to 150	°C

1. Operation above the absolute maximum rating may cause device failure. Operation at the absolute maximum ratings, for extended periods, may reduce device reliability. **2.** Measured in plastic DIP package, results in die form are dependent on die attach and assembly method.

Recommended Operating Conditions[3] (Voltages referenced to GND)

PARAMETER	SYMBOL		MIN	MAX	UNITS
Supply Voltage	V_{CC}		2	6	V
DC Input or Output Voltage	V_{IN}, V_{OUT}		0	V_{CC}	V
Operating Temperature Range	T_J		-40	+85	°C
Input Rise or Fall Times	t_r, t_f	V_{CC} = 2V	0	1000	ns
		V_{CC} = 4.5V	0	500	
		V_{CC} = 6.0V	0	400	

3. This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{IN} and V_{OUT} should be constrained to the range GND ≤ (V_{IN} or V_{OUT}) ≤ V_{CC}. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

Figura 33: Datasheet do C.I. 74HC86 (XOR)

Quad 2-input EXCLUSIVE-OR gate — 74HC/HCT86

FEATURES

- Output capability: standard
- I_{CC} category: SSI

GENERAL DESCRIPTION

The 74HC/HCT86 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.
The 74HC/HCT86 provide the EXCLUSIVE–OR function.

QUICK REFERENCE DATA

GND = 0 V; T_{amb} = 25 °C; $t_r = t_f$ = 6 ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
t_{PHL}/ t_{PLH}	propagation delay nA, nB to nY	C_L = 15 pF; V_{CC} = 5 V	11	14	ns
C_I	input capacitance		3.5	3.5	pF
C_{PD}	power dissipation capacitance per gate	notes 1 and 2	30	30	pF

PIN NO.	SYMBOL	NAME AND FUNCTION
1, 4, 9, 12	1A to 4A	data inputs
2, 5, 10, 13	1B to 4B	data inputs
3, 6, 8, 11	1Y to 4Y	data outputs
7	GND	ground (0 V)
14	V_{CC}	positive supply voltage

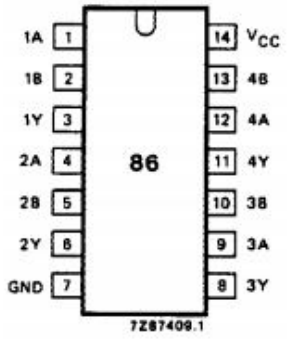


Fig.1 Pin configuration.

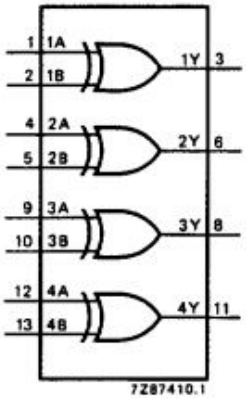


Fig.2 Logic symbol.

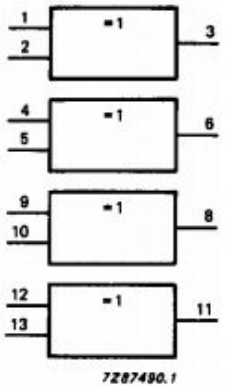


Fig.3 IEC logic symbol.

Figura 34: Datasheet do C.I. 74HC283 (Somador completo de 4 bits)

1. General description

The 74HC283 is a high-speed Si-gate CMOS device and is pin compatible with low power Schottky TTL (LSTTL). The 74HC283 is specified in compliance with JEDEC standard no. 7A.

The 74HC283 adds two 4-bit binary words (An plus Bn) plus the incoming carry (CIN). The binary sum appears on the sum outputs (S1 to S4) and the out-going carry (COUT) according to the equation:

CIN + (A1 + B1) + 2(A2 + B2) + 4(A3 + B3) + 8(A4 + B4) =
= S1 + 2S2 + 4S3 + 8S4 + 16COUT

Where (+) = plus.

Due to the symmetry of the binary add function, the 74HC283 can be used with either all active HIGH operands (positive logic) or all active LOW operands (negative logic). In case of all active LOW operands the results S1 to S4 and COUT should be interpreted also as active LOW. With active HIGH inputs, CIN must be held LOW when no carry in is intended. Interchanging inputs of equal weight does not affect the operation, thus CIN, A1, B1 can be assigned arbitrarily to pins 5, 6, 7, etc.

See the 74HC583 for the BCD version.

2. Features

- High-speed 4-bit binary addition
- Cascadable in 4-bit increments
- Fast internal look-ahead carry
- Low-power dissipation
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM EIA/JESD22-A114-B exceeds 2000 V
  - MM EIA/JESD22-A115-A exceeds 200 V.
- Multiple package options
- Specified from –40 °C to +80 °C and from –40 °C to +125 °C.

Table 2: Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC283N	–40 °C to +125 °C	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
74HC283D	–40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74HC283DB	–40 °C to +125 °C	SSOP16	plastic shrink small outline package; 16 leads; body width 5.3 mm	SOT338-1
74HC283PW	–40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

Figura 35: Datasheet do C.I. 74LS253 (Multiplexador 4x1)

DM74LS253
3-STATE Data Selector/Multiplexer

General Description

Each of these Schottky-clamped data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR gates. Separate output control inputs are provided for each of the two four-line sections.

The 3-STATE outputs can interface directly with data lines of bus-organized systems. With all but one of the common outputs disabled (at a high impedance state), the low impedance of the single enabled output will drive the bus line to a HIGH or LOW logic level.

Features

- 3-STATE version of DM74LS153 with same pinout
- Schottky-diode-clamped transistors
- Permit multiplexing from N-lines to one line
- Performs parallel-to-serial conversion
- Strobe/output control
- High fanout totem-pole outputs
- Typical propagation delay
  - Data to output 12 ns
  - Select to output 21 ns
- Typical power dissipation 35 mW

Recommended Operating Conditions

Symbol	Parameter	Min	Nom	Max	Units
V_{CC}	Supply Voltage	4.75	5	5.25	V
V_{IH}	HIGH Level Input Voltage	2			V
V_{IL}	LOW Level Input Voltage			0.8	V
I_{OH}	HIGH Level Output Current			−2.6	mA
I_{OL}	LOW Level Output Current			24	mA
T_A	Free Air Operating Temperature	0		70	°C

Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ (Note 2)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA			−1.5	V
V_{OH}	HIGH Level Output Voltage	V_{CC} = Min, I_{OH} = Max, V_{IL} = Max, V_{IH} = Min	2.4	3.1		V
V_{OL}	LOW Level Output Voltage	V_{CC} = Min, I_{OL} = Max, V_{IL} = Max, V_{IH} = Min			0.5	V
		I_{OL} = 12 mA, V_{CC} = Min			0.4	
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 7V			0.1	mA
I_{IH}	HIGH Level Input Current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	LOW Level Input Current	V_{CC} = Max, V_I = 0.4V			−0.4	mA
I_{OZH}	Off-State Output Current with HIGH Level Output Voltage Applied	V_{CC} = Max, V_O = 2.7V, V_{IH} = Min, V_{IL} = Max			20	µA
I_{OZL}	Off-State Output Current with LOW Level Output Voltage Applied	V_{CC} = Max, V_O = 0.4, V_{IH} = Min, V_{IL} = Max			−20	µA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 3)	−20		−100	mA
I_{CC1}	Supply Current	V_{CC} = Max (Note 4)		7	12	mA
I_{CC2}	Supply Current	V_{CC} = Max (Note 5)		8.5	14	mA

Figura 36: Datasheet do C.I. 74LS257 (Multiplexador 2x1)

Quad 2-input multiplexer; 3-state — 74HC/HCT257

FEATURES

- Non-inverting data path
- 3-state outputs interface directly with system bus
- Output capability: bus driver
- I_{CC} category: MSI

GENERAL DESCRIPTION

The 74HC/HCT257 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT257 have four identical 2-input multiplexers with 3-state outputs, which select 4 bits of data from two sources and are controlled by a common data select input (S).

The data inputs from source 0 ($1I_0$ to $4I_0$) are selected when input S is LOW and the data inputs from source 1 ($1I_1$ to $4I_1$) are selected when S is HIGH. Data appears at the outputs (1Y to 4Y) in true (non-inverting) form from the selected inputs.

The "257" is the logic implementation of a 4-pole, 2-position switch, where the position of the switch is determined by the logic levels applied to S. The outputs are forced to a high impedance OFF-state when $\overline{OE}$ is HIGH.

The logic equations for the outputs are:

$1Y = \overline{OE}.(1I_1.S + 1I_0.\overline{S})$
$2Y = \overline{OE}.(2I_1.S + 2I_0.\overline{S})$
$3Y = \overline{OE}.(3I_1.S + 3I_0.\overline{S})$
$4Y = \overline{OE}.(4I_1.S + 4I_0.\overline{S})$

The "257" is identical to the "258" but has non-inverting (true) outputs.

SYMBOL	PARAMETER	T_{amb} (°C)							UNIT	TEST CONDITIONS	
		74HC								V_{CC} (V)	WAVEFORMS
		+25			−40 to +85		−40 to +125				
		min.	typ.	max.	min.	max.	min.	max.			
t_{PHL}/t_{PLH}	propagation delay nI_0 to nY; nI_1 to nY		36	110		140		165	ns	2.0	Fig.6
			13	22		28		33		4.5	
			10	19		24		28		6.0	
t_{PHL}/t_{PLH}	propagation delay S to nY		47	150		190		225	ns	2.0	Fig.6
			17	30		38		45		4.5	
			14	26		33		38		6.0	
t_{PZH}/t_{PZL}	3-state output enable time $\overline{OE}$ to nY		33	150		190		225	ns	2.0	Fig.7
			12	30		38		45		4.5	
			10	26		33		38		6.0	
t_{PHZ}/t_{PLZ}	3-state output disable time $\overline{OE}$ to nY		41	150		190		225	ns	2.0	Fig.7
			15	30		38		45		4.5	
			12	26		33		38		6.0	
t_{THL}/t_{TLH}	output transition time		14	60		75		90	ns	2.0	Fig.6
			5	12		15		18		4.5	
			4	10		13		15		6.0	