adc10\_sam3u.o:

adc12\_sam3u.o:

adc\_sam3snxa.o:

pio.o:

00000000 T PIO\_Clear

00000000 T PIO\_Configure

00000000 T PIO\_DisableInterrupt

00000000 T PIO\_Get

00000000 T PIO\_GetOutputDataStatus

00000000 T PIO\_PullUp

00000000 T PIO\_Set

00000000 T PIO\_SetDebounceFilter

00000000 T PIO\_SetInput

00000000 T PIO\_SetOutput

00000000 T PIO\_SetPeripheral

pmc.o:

00000000 T pmc\_clr\_fast\_startup\_input

00000000 T pmc\_disable\_all\_pck

00000000 T pmc\_disable\_all\_periph\_clk

00000000 T pmc\_disable\_interrupt

00000000 T pmc\_disable\_pck

00000000 T pmc\_disable\_periph\_clk

00000000 T pmc\_disable\_pllack

00000000 T pmc\_disable\_udpck

00000000 T pmc\_disable\_upll\_clock

00000000 T pmc\_enable\_all\_pck

00000000 T pmc\_enable\_all\_periph\_clk

00000000 T pmc\_enable\_backupmode

00000000 T pmc\_enable\_interrupt

00000000 T pmc\_enable\_pck

00000000 T pmc\_enable\_periph\_clk

00000000 T pmc\_enable\_pllack

00000000 T pmc\_enable\_sleepmode

00000000 T pmc\_enable\_udpck

00000000 T pmc\_enable\_upll\_clock

00000000 T pmc\_enable\_waitmode

00000000 T pmc\_get\_interrupt\_mask

00000000 T pmc\_get\_status

00000000 T pmc\_get\_writeprotect\_status

00000000 T pmc\_is\_locked\_pllack

00000000 T pmc\_is\_locked\_upll

00000000 T pmc\_is\_pck\_enabled

00000000 T pmc\_is\_periph\_clk\_enabled

00000000 T pmc\_mck\_set\_prescaler

00000000 T pmc\_mck\_set\_source

00000000 T pmc\_osc\_disable\_fastrc

00000000 T pmc\_osc\_disable\_xtal

00000000 T pmc\_osc\_enable\_fastrc

00000000 T pmc\_osc\_is\_ready\_32kxtal

00000000 T pmc\_osc\_is\_ready\_mainck

00000000 T pmc\_pck\_set\_prescaler

00000000 T pmc\_pck\_set\_source

00000000 T pmc\_set\_fast\_startup\_input

00000000 T pmc\_set\_writeprotect

00000000 T pmc\_switch\_mainck\_to\_fastrc

00000000 T pmc\_switch\_mainck\_to\_xtal

00000000 T pmc\_switch\_mck\_to\_mainck

00000000 T pmc\_switch\_mck\_to\_pllack

00000000 T pmc\_switch\_mck\_to\_sclk

00000000 T pmc\_switch\_mck\_to\_upllck

00000000 T pmc\_switch\_pck\_to\_mainck

00000000 T pmc\_switch\_pck\_to\_pllack

00000000 T pmc\_switch\_pck\_to\_sclk

00000000 T pmc\_switch\_pck\_to\_upllck

00000000 T pmc\_switch\_sclk\_to\_32kxtal

00000000 T pmc\_switch\_udpck\_to\_pllack

00000000 T pmc\_switch\_udpck\_to\_upllck

pwmc.o:

00000000 t FindClockConfiguration

00000000 T PWMC\_ConfigureChannel

00000000 T PWMC\_ConfigureChannelExt

00000000 T PWMC\_ConfigureClocks

00000000 T PWMC\_ConfigureComparisonUnit

00000000 T PWMC\_ConfigureEventLineMode

00000000 T PWMC\_ConfigureSyncChannel

00000000 T PWMC\_DisableChannel

00000000 T PWMC\_DisableChannelIt

00000000 T PWMC\_DisableIt

00000000 T PWMC\_DisableOverrideOutput

00000000 T PWMC\_EnableChannel

00000000 T PWMC\_EnableChannelIt

00000000 T PWMC\_EnableFaultProtection

00000000 T PWMC\_EnableIt

00000000 T PWMC\_EnableOverrideOutput

00000000 T PWMC\_FaultClear

00000000 T PWMC\_SetDeadTime

00000000 T PWMC\_SetDutyCycle

00000000 T PWMC\_SetFaultMode

00000000 T PWMC\_SetFaultProtectionValue

00000000 T PWMC\_SetOverrideValue

00000000 T PWMC\_SetPeriod

00000000 T PWMC\_SetSyncChannelUpdatePeriod

00000000 T PWMC\_SetSyncChannelUpdateUnlock

00000000 T PWMC\_WriteBuffer

U \_\_assert\_func

00000000 r \_\_func\_\_.6793

00000000 r \_\_func\_\_.6804

00000000 r \_\_func\_\_.6819

00000000 r \_\_func\_\_.6830

00000000 r \_\_func\_\_.6841

00000000 r \_\_func\_\_.6848

00000000 r \_\_func\_\_.6932

00000000 r \_\_func\_\_.6938

rtc.o:

00000000 T RTC\_ClearSCCR

00000000 T RTC\_DisableIt

00000000 T RTC\_EnableIt

00000000 T RTC\_GetDate

00000000 T RTC\_GetHourMode

00000000 T RTC\_GetSR

00000000 T RTC\_GetTime

00000000 T RTC\_SetDate

00000000 T RTC\_SetDateAlarm

00000000 T RTC\_SetHourMode

00000000 T RTC\_SetTime

00000000 T RTC\_SetTimeAlarm

U \_\_assert\_func

00000000 r \_\_func\_\_.6790

00000000 r \_\_func\_\_.6799

00000000 r \_\_func\_\_.6804

rtt.o:

00000000 T RTT\_EnableIT

00000000 T RTT\_GetStatus

00000000 T RTT\_GetTime

00000000 T RTT\_SetAlarm

00000000 T RTT\_SetPrescaler

U \_\_assert\_func

00000000 r \_\_func\_\_.6797

00000000 r \_\_func\_\_.6805

spi.o:

00000000 T SPI\_Configure

00000000 T SPI\_ConfigureNPCS

00000000 T SPI\_Disable

00000000 T SPI\_DisableIt

00000000 T SPI\_Enable

00000000 T SPI\_EnableIt

00000000 T SPI\_GetStatus

00000000 T SPI\_IsFinished

00000000 T SPI\_Read

00000000 T SPI\_Write

U pmc\_enable\_periph\_clk

tc.o:

00000000 T TC\_Configure

00000000 T TC\_FindMckDivisor

00000000 T TC\_GetStatus

00000000 T TC\_ReadCV

00000000 T TC\_SetRA

00000000 T TC\_SetRB

00000000 T TC\_SetRC

00000000 T TC\_Start

00000000 T TC\_Stop

U \_\_assert\_func

00000000 r \_\_func\_\_.6792

00000000 r \_\_func\_\_.6798

00000000 r \_\_func\_\_.6804

timetick.o:

00000000 T GetTickCount

00000000 T Sleep

00000000 T TimeTick\_Configure

00000000 T TimeTick\_Increment

00000000 T Wait

00000000 b \_dwTickCount

twi.o:

00000000 T TWI\_ByteReceived

00000000 T TWI\_ByteSent

00000000 T TWI\_ConfigureMaster

00000000 T TWI\_ConfigureSlave

00000000 T TWI\_Disable

00000000 T TWI\_DisableIt

00000000 T TWI\_EnableIt

00000000 T TWI\_GetMaskedStatus

00000000 T TWI\_GetStatus

00000000 T TWI\_ReadByte

00000000 T TWI\_SendSTOPCondition

00000000 T TWI\_SetClock

00000000 T TWI\_StartRead

00000000 T TWI\_StartWrite

00000000 T TWI\_Stop

00000000 T TWI\_TransferComplete

00000000 T TWI\_WriteByte

U \_\_assert\_func

00000000 r \_\_func\_\_.7151

00000000 r \_\_func\_\_.7157

00000000 r \_\_func\_\_.7172

00000000 r \_\_func\_\_.7176

00000000 r \_\_func\_\_.7184

00000000 r \_\_func\_\_.7191

00000000 r \_\_func\_\_.7195

00000000 r \_\_func\_\_.7200

00000000 r \_\_func\_\_.7208

00000000 r \_\_func\_\_.7222

00000000 r \_\_func\_\_.7227

00000000 r \_\_func\_\_.7231

00000000 r \_\_func\_\_.7236

00000000 r \_\_func\_\_.7240

usart.o:

00000000 T USART\_Configure

00000000 T USART\_DisableIt

00000000 T USART\_EnableIt

00000000 T USART\_GetChar

00000000 T USART\_GetStatus

00000000 T USART\_IsDataAvailable

00000000 T USART\_IsRxReady

00000000 T USART\_PutChar

00000000 T USART\_Read

00000000 T USART\_ReadBuffer

00000000 T USART\_SetIrdaFilter

00000000 T USART\_SetReceiverEnabled

00000000 T USART\_SetTransmitterEnabled

00000000 T USART\_Write

00000000 T USART\_WriteBuffer

U \_\_assert\_func

00000000 r \_\_func\_\_.7068

wdt.o:

00000000 T WDT\_Disable

00000000 T WDT\_Enable

00000000 T WDT\_GetPeriod

00000000 T WDT\_GetStatus

00000000 T WDT\_Restart

system\_sam3xa.o:

00000000 D SystemCoreClock

00000000 T SystemCoreClockUpdate

00000000 T SystemInit

00000000 T system\_init\_flash

startup\_sam3xa.o:

U ADC\_Handler

U BusFault\_Handler

U CAN0\_Handler

U CAN1\_Handler

U DACC\_Handler

U DMAC\_Handler

U DebugMon\_Handler

U EFC0\_Handler

U EFC1\_Handler

U EMAC\_Handler

U HSMCI\_Handler

U HardFault\_Handler

U MemManage\_Handler

U NMI\_Handler

U PIOA\_Handler

U PIOB\_Handler

U PIOC\_Handler

U PIOD\_Handler

U PMC\_Handler

U PWM\_Handler

U PendSV\_Handler

U RSTC\_Handler

U RTC\_Handler

U RTT\_Handler

00000000 T Reset\_Handler

U SMC\_Handler

U SPI0\_Handler

U SSC\_Handler

U SUPC\_Handler

U SVC\_Handler

U SysTick\_Handler

U TC0\_Handler

U TC1\_Handler

U TC2\_Handler

U TC3\_Handler

U TC4\_Handler

U TC5\_Handler

U TC6\_Handler

U TC7\_Handler

U TC8\_Handler

U TRNG\_Handler

U TWI0\_Handler

U TWI1\_Handler

U UART\_Handler

U UOTGHS\_Handler

U USART0\_Handler

U USART1\_Handler

U USART2\_Handler

U USART3\_Handler

U UsageFault\_Handler

U WDT\_Handler

U \_erelocate

U \_estack

U \_etext

U \_ezero

U \_sfixed

U \_srelocate

U \_szero

00000000 R exception\_table

U main

adc.o:

00000000 T adc\_configure\_power\_save

00000000 T adc\_configure\_sequence

00000000 T adc\_configure\_timing

00000000 T adc\_configure\_trigger

00000000 T adc\_disable\_all\_channel

00000000 T adc\_disable\_anch

00000000 T adc\_disable\_channel

00000000 T adc\_disable\_channel\_differential\_input

00000000 T adc\_disable\_channel\_input\_offset

00000000 T adc\_disable\_interrupt

00000000 T adc\_disable\_tag

00000000 T adc\_disable\_ts

00000000 T adc\_enable\_all\_channel

00000000 T adc\_enable\_anch

00000000 T adc\_enable\_channel

00000000 T adc\_enable\_channel\_differential\_input

00000000 T adc\_enable\_channel\_input\_offset

00000000 T adc\_enable\_interrupt

00000000 T adc\_enable\_tag

00000000 T adc\_enable\_ts

00000000 T adc\_get\_actual\_adc\_clock

00000000 T adc\_get\_channel\_status

00000000 T adc\_get\_channel\_value

00000000 T adc\_get\_comparison\_mode

00000000 T adc\_get\_interrupt\_mask

00000000 T adc\_get\_latest\_value

00000000 T adc\_get\_overrun\_status

00000000 T adc\_get\_pdc\_base

00000000 T adc\_get\_status

00000000 T adc\_get\_tag

00000000 T adc\_get\_writeprotect\_status

00000000 T adc\_init

00000000 T adc\_set\_bias\_current

00000000 T adc\_set\_channel\_input\_gain

00000000 T adc\_set\_comparison\_channel

00000000 T adc\_set\_comparison\_mode

00000000 T adc\_set\_comparison\_window

00000000 T adc\_set\_resolution

00000000 T adc\_set\_writeprotect

00000000 T adc\_start

00000000 T adc\_start\_sequencer

00000000 T adc\_stop

00000000 T adc\_stop\_sequencer

udp.o:

udphs.o:

uotghs.o:

00000000 T UOTGHS\_Handler

00000000 B gpf\_isr

interrupt\_sam\_nvic.o:

00000000 D g\_interrupt\_enabled

uotghs\_device.o:

00000000 T UDD\_Attach

00000000 T UDD\_ClearIN

00000000 T UDD\_ClearOUT

00000000 T UDD\_ClearSetupInt

00000000 T UDD\_Detach

00000000 T UDD\_FifoByteCount

00000000 T UDD\_GetFrameNumber

00000000 T UDD\_Init

00000000 T UDD\_InitEP

00000000 T UDD\_InitEndpoints

00000000 T UDD\_ReadWriteAllowed

00000000 T UDD\_ReceivedSetupInt

00000000 T UDD\_Recv

00000000 T UDD\_Recv8

00000000 T UDD\_ReleaseRX

00000000 T UDD\_ReleaseTX

00000000 T UDD\_Send

00000000 T UDD\_Send8

00000000 T UDD\_SetAddress

00000000 T UDD\_SetStack

00000000 T UDD\_Stall

00000000 T UDD\_WaitForINOrOUT

00000000 T UDD\_WaitIN

00000000 T UDD\_WaitOUT

U g\_interrupt\_enabled

U gpf\_isr

U pmc\_enable\_periph\_clk

U pmc\_enable\_udpck

U pmc\_enable\_upll\_clock

U pmc\_switch\_udpck\_to\_upllck

00000000 b ul\_recv\_fifo\_ptr

00000000 b ul\_send\_fifo\_ptr

uotghs\_host.o:

00000000 T UHD\_BusReset

00000000 T UHD\_GetVBUSState

00000000 t UHD\_ISR

00000000 T UHD\_Init

00000000 T UHD\_Pipe0\_Alloc

00000000 T UHD\_Pipe\_Alloc

00000000 T UHD\_Pipe\_Free

00000000 T UHD\_Pipe\_Is\_Transfer\_Complete

00000000 T UHD\_Pipe\_Read

00000000 T UHD\_Pipe\_Send

00000000 T UHD\_Pipe\_Write

00000000 T UHD\_SetStack

U g\_interrupt\_enabled

U gpf\_isr

U pmc\_enable\_periph\_clk

U pmc\_enable\_udpck

U pmc\_enable\_upll\_clock

U pmc\_switch\_udpck\_to\_upllck

00000000 b uhd\_state

dacc.o:

00000000 T dacc\_disable\_channel

00000000 T dacc\_disable\_interrupt

00000000 T dacc\_disable\_trigger

00000000 T dacc\_enable\_channel

00000000 T dacc\_enable\_flexible\_selection

00000000 T dacc\_enable\_interrupt

00000000 T dacc\_get\_analog\_control

00000000 T dacc\_get\_channel\_status

00000000 T dacc\_get\_interrupt\_mask

00000000 T dacc\_get\_interrupt\_status

00000000 T dacc\_get\_pdc\_base

00000000 T dacc\_get\_writeprotect\_status

00000000 T dacc\_reset

00000000 T dacc\_set\_analog\_control

00000000 T dacc\_set\_channel\_selection

00000000 T dacc\_set\_power\_save

00000000 T dacc\_set\_timing

00000000 T dacc\_set\_transfer\_mode

00000000 T dacc\_set\_trigger

00000000 T dacc\_set\_writeprotect

00000000 T dacc\_write\_conversion\_data

can.o:

00000000 R can\_bit\_time

00000000 T can\_disable

00000000 T can\_disable\_autobaud\_listen\_mode

00000000 T can\_disable\_interrupt

00000000 T can\_disable\_low\_power\_mode

00000000 T can\_disable\_overload\_frame

00000000 T can\_disable\_time\_triggered\_mode

00000000 T can\_disable\_timer\_freeze

00000000 T can\_disable\_tx\_repeat

00000000 T can\_enable

00000000 T can\_enable\_autobaud\_listen\_mode

00000000 T can\_enable\_interrupt

00000000 T can\_enable\_low\_power\_mode

00000000 T can\_enable\_overload\_frame

00000000 T can\_enable\_time\_triggered\_mode

00000000 T can\_enable\_timer\_freeze

00000000 T can\_enable\_tx\_repeat

00000000 T can\_get\_internal\_timer\_value

00000000 T can\_get\_interrupt\_mask

00000000 T can\_get\_rx\_error\_cnt

00000000 T can\_get\_status

00000000 T can\_get\_timestamp\_value

00000000 T can\_get\_tx\_error\_cnt

00000000 T can\_global\_send\_abort\_cmd

00000000 T can\_global\_send\_transfer\_cmd

00000000 T can\_init

00000000 T can\_mailbox\_get\_status

00000000 T can\_mailbox\_init

00000000 T can\_mailbox\_read

00000000 T can\_mailbox\_send\_abort\_cmd

00000000 T can\_mailbox\_send\_transfer\_cmd

00000000 T can\_mailbox\_set\_timemark

00000000 T can\_mailbox\_tx\_remote\_frame

00000000 T can\_mailbox\_write

00000000 T can\_reset\_all\_mailbox

00000000 T can\_reset\_internal\_timer

00000000 T can\_reset\_mailbox\_data

00000000 T can\_set\_rx\_sync\_stage

00000000 T can\_set\_timestamp\_capture\_point

U memset

efc.o:

00000000 T efc\_disable\_frdy\_interrupt

00000000 T efc\_enable\_frdy\_interrupt

00000000 T efc\_get\_flash\_access\_mode

00000000 T efc\_get\_result

00000000 T efc\_get\_status

00000000 T efc\_get\_wait\_state

00000000 T efc\_init

00000000 T efc\_perform\_command

0000006c T efc\_perform\_fcr

00000000 T efc\_perform\_read\_sequence

00000000 T efc\_set\_flash\_access\_mode

00000000 T efc\_set\_wait\_state

00000068 T efc\_write\_fmr

00000000 b iap\_perform\_command.7049

gpbr.o:

00000000 T gpbr\_read

00000000 T gpbr\_write

ssc.o:

U memset

00000000 T ssc\_disable\_interrupt

00000000 T ssc\_disable\_rx

00000000 T ssc\_disable\_tx

00000000 T ssc\_disable\_tx\_frame\_sync\_data

00000000 T ssc\_enable\_interrupt

00000000 T ssc\_enable\_rx

00000000 T ssc\_enable\_tx

00000000 T ssc\_enable\_tx\_frame\_sync\_data

00000000 T ssc\_get\_interrupt\_mask

00000000 T ssc\_get\_rx\_access

00000000 T ssc\_get\_rx\_compare

00000000 T ssc\_get\_status

00000000 T ssc\_get\_tx\_access

00000000 T ssc\_get\_writeprotect\_status

00000000 T ssc\_i2s\_set\_receiver

00000000 T ssc\_i2s\_set\_transmitter

00000000 T ssc\_is\_rx\_enabled

00000000 T ssc\_is\_rx\_ready

00000000 T ssc\_is\_tx\_empty

00000000 T ssc\_is\_tx\_enabled

00000000 T ssc\_is\_tx\_ready

00000000 T ssc\_read

00000000 T ssc\_read\_sync\_data

00000000 T ssc\_reset

00000000 T ssc\_set\_clock\_divider

00000000 T ssc\_set\_loop\_mode

00000000 T ssc\_set\_normal\_mode

00000000 T ssc\_set\_receiver

00000000 T ssc\_set\_rx\_compare

00000000 T ssc\_set\_rx\_stop\_selection

00000000 T ssc\_set\_td\_default\_level

00000000 T ssc\_set\_transmitter

00000000 T ssc\_set\_writeprotect

00000000 T ssc\_write

00000000 T ssc\_write\_sync\_data

trng.o:

00000000 T trng\_disable

00000000 T trng\_disable\_interrupt

00000000 T trng\_enable

00000000 T trng\_enable\_interrupt

00000000 T trng\_get\_interrupt\_mask

00000000 T trng\_get\_interrupt\_status

00000000 T trng\_read\_output\_data

rstc.o:

00000000 T rstc\_disable\_user\_reset

00000000 T rstc\_disable\_user\_reset\_interrupt

00000000 T rstc\_enable\_user\_reset

00000000 T rstc\_enable\_user\_reset\_interrupt

00000000 T rstc\_get\_reset\_cause

00000000 T rstc\_get\_status

00000000 T rstc\_reset\_extern

00000000 T rstc\_set\_external\_reset

00000000 T rstc\_start\_software\_reset

emac.o:

00000000 t circ\_inc

00000000 T emac\_dev\_get\_tx\_load

00000000 T emac\_dev\_init

00000000 T emac\_dev\_read

00000000 T emac\_dev\_reset

00000000 T emac\_dev\_set\_rx\_callback

00000000 T emac\_dev\_set\_tx\_wakeup\_callback

00000000 T emac\_dev\_write

00000000 T emac\_handler

00000000 T emac\_phy\_read

00000000 T emac\_phy\_write

00000000 t emac\_reset\_rx\_mem

00000000 t emac\_reset\_tx\_mem

00000000 b gs\_rx\_desc

00000000 b gs\_tx\_callback

00000000 b gs\_tx\_desc

00000000 b gs\_uc\_rx\_buffer

00000000 b gs\_uc\_tx\_buffer

U memcpy